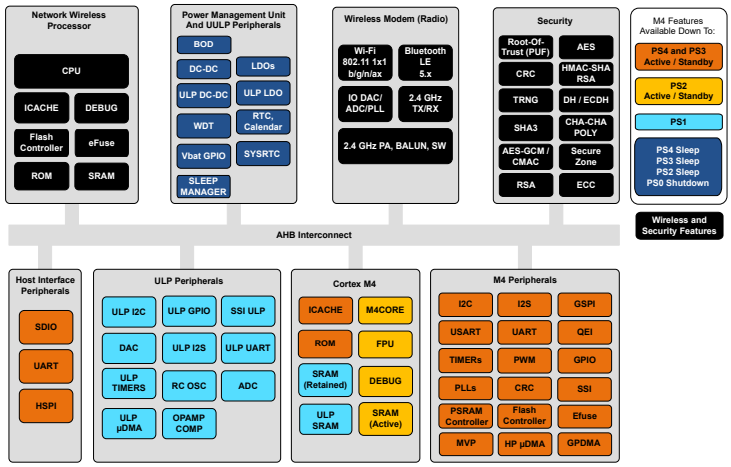
SiWG917 SoC Single Chip Wi-Fi and Bluetooth LE Wireless Secure MCU Solutions Data Sheet

Silicon Labs SiWG917 SoC is our lowest power Wi-Fi® 6 plus Bluetooth® LE 5.4 SoC, ideal for ultra-low power IoT wireless devices using Wi-Fi®, Bluetooth, Matter, and IP networking for secure cloud connectivity. It is optimal for developing battery operated devices that need long battery life. SiWG917 SoC includes an ultra-low power Wi-Fi 6 plus Bluetooth Low Energy (LE) 5.4 wireless CPU subsystem, and an integrated micro-controller (MCU) application subsystem, security, peripherals and power management subsystem all in a single 7x7 mm QFN package. The wireless subsystem consists of a multi-threaded Network Wireless Processor (NWP) running up to 160 MHz, baseband digital signal processing, analog front end, 2.4 GHz RF transceiver and integrated power amplifier. The application subsystem consists of an ARM® Cortex®-M4 running up to 180 MHz, embedded SRAM, flash, ultra-low power sensor hub, and matrix vector processor. The ARM® Cortex®-M4 is dedicated to peripheral and application-related processing, while the NWP runs the wireless and networking stacks on independent threads, thus providing a fully integrated solution that is ready for a wide range of embedded wireless IoT applications.

SiWG917 applications include:

- Smart Home
- Security Cameras
- HVAC
- Smart Sensors
- Smart Appliances
- Health and Fitness
- Pet Trackers
- Smart Cities
- Smart Meters
- Industrial Wearables
- Smart Buildings
- Asset Tracking
- Smart hospitals



KEY FEATURES

- Wi-Fi 6 Single Band 2.4 GHz 20 MHz 1x1 stream IEEE 802.11 b/g/n/ax
- Bluetooth LE 5.4
- Single chip Matter Over Wi-Fi Solution
- ARM® Cortex® M4 Processor with FPU subsystem up to 180 MHz with rich set of Digital and Analog Peripherals.
- Wi-Fi 6 Benefits: TWT for improved efficiency and longer battery life, DL MU-MIMO, DL/UL OFDMA for Higher Throughput, network capacity and low latency
- Best in Class Device and Wireless Security
- WLAN Tx power up to +19.5 dBm with integrated PA
- Bluetooth LE Tx power up to +19 dBm with integrated PA
- WLAN Rx sensitivity as low as -97.5 dBm
- Wi-Fi Standby Associated mode current: 65 µA @ 1-second listen interval
- Embedded Flash option up to 8 MB/ optional external Flash up to 16 MB
- Embedded PSRAM option up to 8 MB/ optional external PSRAM option up to 16 MB
- Ultra-low power sensor hub peripherals
- Matrix Vector Processor (MVP)
- Embedded Wi-Fi, Bluetooth LE, Matter, and networking stacks supporting wireless coexistence
- Three software-configurable MCU application memory options for sharing the RAM between the NWP and M4 (192/256/320 KB)
- Operating temperature: -40 ºC to +85 ºC
- Single or dual-supply operation:
  - Single supply: 3.3 V
  - Dual supply: 3.3 V and 1.8 V

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1. Feature List

- **Microcontroller**
  - ARM® Cortex® M4 core with up to 180 MHz, 225 DMIPS performance
  - Integrated FPU (Floating Point Unit), and NVIC (Nested Vectored Interrupt Controller).
  - SWD (Serial Wire Debug) and JTAG (Joint Test Action Group) debug options
  - Internal and external oscillators with Phase Locked Loops (PLLs)
  - IAP (In-Flash Application Programming), ISP (In-System Programming), and OTA (Over-the-Air) NWP Firmware Upgrade
  - Power-On Reset (POR), Brown-Out and Black-Out Detect (BOD)[2] with separate thresholds
  - M4 has 2 dedicated QSPI (Quad Serial Peripheral Interface) controllers; one for PSRAM (Pseudo Static Random Access Memory) and one for Flash
- **Matrix Vector Processor (MVP)**
  - Co-processor for offloading matrix math operations
  - Delivers faster Machine Learning (ML) inference with lower power consumption
  - Performs Real and Complex Matrix and Vector operations, providing manifold computing efficiency
- **Memory**
  - Embedded SRAM (Static Random Access Memory) up to 672 KB total for Application and Network Wireless Processor
  - On-chip SRAM of 192, 256, or 320 KB for M4 Application Processor based on the memory configuration
  - Support for Flash up to 8 MB (in-package), or Optional External Flash up to 16 MB[2]
  - Support for PSRAM option up to 8 MB (in-package), Optional External PSRAM up to 16 MB[2]
- **Digital Peripherals**
  - Secure Digital Input Output (SDIO) 2.0 secondary
  - 1x Universal Synchronous/Asynchronous Receiver Transmitter (USART)
  - 2x Universal Asynchronous Receiver Transmitter (UART)
  - 3x Synchronous Serial Interface (SSI)
  - 1x General SPI (GSPI)
  - 1x Host SPI (HSPI)
  - 3x Inter-Integrated Circuit (I2C)
  - 2x Inter-IC Sound Bus (I2S)
  - Pulse Width Modulation (MCPWM)
  - Quadrature Encoder Interface (QEI)
  - Timers: 4x 16/32-bit, 1x 24-bit, Watchdog Timer (WDT), Real-Time Clock (RTC)
  - Up to 45 General Purpose Input Outputs (GPIOs) with GPIO multiplexer
  - General Purpose DMA (GPDMA) controller
  - HP Micro-DMA (HP µDMA) controller
- **Security**
  - Secure Boot
  - Secure firmware upgrade through boot-loader, Secure OTA
  - Secure Key storage and HW device identity with PUF
  - Secure Zone
  - Encrypted XiP (Execute in Place) from flash/ PSRAM
  - Secure Attestation
  - Hardware Accelerators: Advanced Encryption Standard (AES) 128/256/192, Secure Hash Algorithm (SHA) 256/384/512, Hash Message Authentication Code (HMAC), Random Number Generator (RNG), Cyclic Redundancy Check (CRC), SHA3, AES-Galois Counter Mode (GCM), Cipher based Message Authentication Code (CMAC), Cha-Cha-poly, True Random Number Generator (TRNG)
  - Software Implementation: RSA, ECC
  - Anti Rollback
  - Debug Lock
- **Wi-Fi**
  - Compliant to single-spatial stream IEEE 802.11 b/g/n/ax with single band (2.4 GHz) support
  - Support for 20 MHz channel bandwidth for 802.11n and 802.11ax.
  - Operating Modes: Wi-Fi 4 STA, Wi-Fi 6 (802.11ax) STA, Wi-Fi 4 AP, Enterprise STA, Wi-Fi 6 STA + Wi-Fi 4 AP, Wi-Fi STA + BLE
  - Wi-Fi 6 Features: Individual Target wake-up time (iTWT), Broadcast TWT (bTWT)[2], Intra PPDU power save[2], SU extended range (ER), DCM (Dual Carrier Modulation), DL MU-MIMO, DL/UL OFDMA, MBSSID[2], BFRP, Spatial Re-use[2], BSS Coloring[2], and NDP feedback up to 4 antennas
  - Transmit power up to +19.5 dBm with integrated PA
  - Receive sensitivity as low as -97.5 dBm
  - Data Rates: 802.11b: 1, 2, 5.5, 11; 802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps; 802.11n: MCS0 to MCS7; 802.11ax: MCS0 to MCS7
  - Operating Frequency Range: 2412 MHz – 2484 MHz
  - PTA Coexistence with Zigbee/Thread/Bluetooth
- **Bluetooth**
  - Transmit power up to +19 dBm with integrated PA
  - Receive sensitivity — LE 1 Mbps: -96 dBm, LR 125 kbps: -107 dBm
  - Operating Frequency Range — 2.402 GHz - 2.480 GHz
  - Support LE (1 Mbps & 2 Mbps) and LR (125 kbps & 500 kbps) rates
  - Advertising extensions
  - Data length extensions
  - LL privacy
  - LE dual role
  - BLE acceptlist
  - 10 simultaneous BLE Connections (8 Peripheral & 2 Central)

- **Analog Peripherals**
  - 12-bit 16-ch, 2.5 Msps Analog to Digital Converter (ADC)
  - 10-bit Digital to Analog Converter (DAC)
  - 3x Op-amps
  - 2x Comparators
  - Temperature Sensor
- **Embedded Bluetooth Stack**
  - Support GAP profile
  - Support GATT profile
  - Support SMP
  - Support LE L2CAP
- **WiSeConnect SDK Features**
  - Simplified and Unified DX for Wi-Fi API and Platform APIs
  - Simplifies application development and presents clean and standardized APIs
  - UC (Universal Configurator) enables componentization, simplifying configuration of peripherals and examples
  - BSD and ARM IoT-compliant socket API
  - Available through Simplicity Studio and Command Line Development (SLT-CLI)
- **Intelligent Power Management**
  - Power optimizations leveraging multiple power domains and partitioned subsystems
  - Many system-, component-, and circuit-level innovations and optimizations
  - Multiple Power states: PS4 / PS3 / PS2 / PS1 / PS0
  - Voltage & Frequency Scaling for MCU
  - Application-based Gear Shifting (switches from one power state to another based on processing requirements) for MCU
  - Deep sleep mode with only timer active – with and without RAM retention
- **Ultra Low Power Sensor Hub System**
  - Offloads Sensor data collection without a need for MCU to be active
  - Extends battery life and recharging interval for IoT Sensors
- **MCU Sub-System Power Consumption**
  - Active current as low as 40.4 µA/MHz @ 20 MHz in low-power mode
  - Active current as low as 70.5 µA/MHz @ 180 MHz in high performance mode
  - Deep sleep mode current: ~2.5 µA
  - Voltage & frequency scaling
  - Deep sleep mode with only timer active – with and without RAM retention
- **Wireless Sub-System Power Consumption**
  - Wi-Fi 4 Standby Associated mode current: 65 µA @ 1-second beacon listen interval
  - Wi-Fi 1 Mbps Listen current: 16.5 mA
  - Wi-Fi LP chain Rx current: 22 mA
  - Deep sleep current ~2.5 µA, Standby current (352 KB RAM retention) ~10 µA
- **Host Interface Peripherals**
  - HSPI - up to 100 MHz
  - SDIO[2] - up to 50 MHz
  - UART - up to 921600 Baud
- **Ultra Low Power (ULP) Peripherals**
  - ULP I2C
  - ULP I2S
  - ULP UART
  - ULP GPIO
  - ULP Timers
  - ULP ADC
  - ULP DAC
  - ULP Micro DMA (ULP µDMA)
  - ULP SSI Primary
- **Ultra Ultra Low Power (UULP) Peripherals**
  - RTC (Calendar)
  - BOD
  - WDT
  - SYSRTC
- **RF & Modem Features**
  - Integrated baseband processor with calibration memory
  - Integrated RF transceiver, high-power amplifier, balun and T/R switch
- **Embedded Wi-Fi Stack**
  - Support for Embedded Wi-Fi STA mode, Wi-Fi access point mode, and concurrent (AP+STA) mode
  - Supports advanced Wi-Fi security features: WPA personal, WPA2 personal, WPA3 personal, WPA/WPA2/WPA3 enterprise in STA mode
  - Networking: Integrated IPv4/IPv6 stack, TCP, UDP, ICMP, ICMPv6, ARP, DHCP Client/Server, DHCPv6 Client/Server, DNS Client, SSL3.0/TLS1.3 Client, SNTP, mDNS, SNI
  - Applications: HTTP/s Client, HTTP/s Server[2], MQTT/s Client, AWS Client, Azure Client
  - Sockets: BSD sockets, IoT sockets
  - Over-the-Air (OTA) firmware update
  - Provisioning using Wi-Fi AP or BLE
- **Software and Regulatory Certifications**
  - Wi-Fi Alliance: Wi-Fi 4, Wi-Fi 6
  - Matter Certification
  - Bluetooth 5.4 Qualification
  - Verified for compliance with FCC, ISED, CE, UKCA, MIC regulatory requirements[1]
- **Advanced Software Features**
  - FreeRTOS, Zephyr[2]
  - Amazon AWS Cloud Connectivity, Microsoft Azure Cloud Connectivity
  - SensorHub (SensorHub framework which enables easier integration of new sensors)
  - Dual-Host: Support both embedded TCP-IP and TCP-IP bypass simultaneously[2]

- **Operating Conditions**
  - Single or dual-supply operation:
    - Single supply: 3.3 V
    - Dual supply: 3.3 V and 1.8 V
  - Operating temperature: -40 ºC to +85 ºC

Note:

1. For latest compliance information, refer to AN1437 regulatory app note.
2. For information about software roadmap features, and lists of available features and profiles, contact Silicon Labs or refer to Release Notes and Reference Manuals.

2. Ordering Information

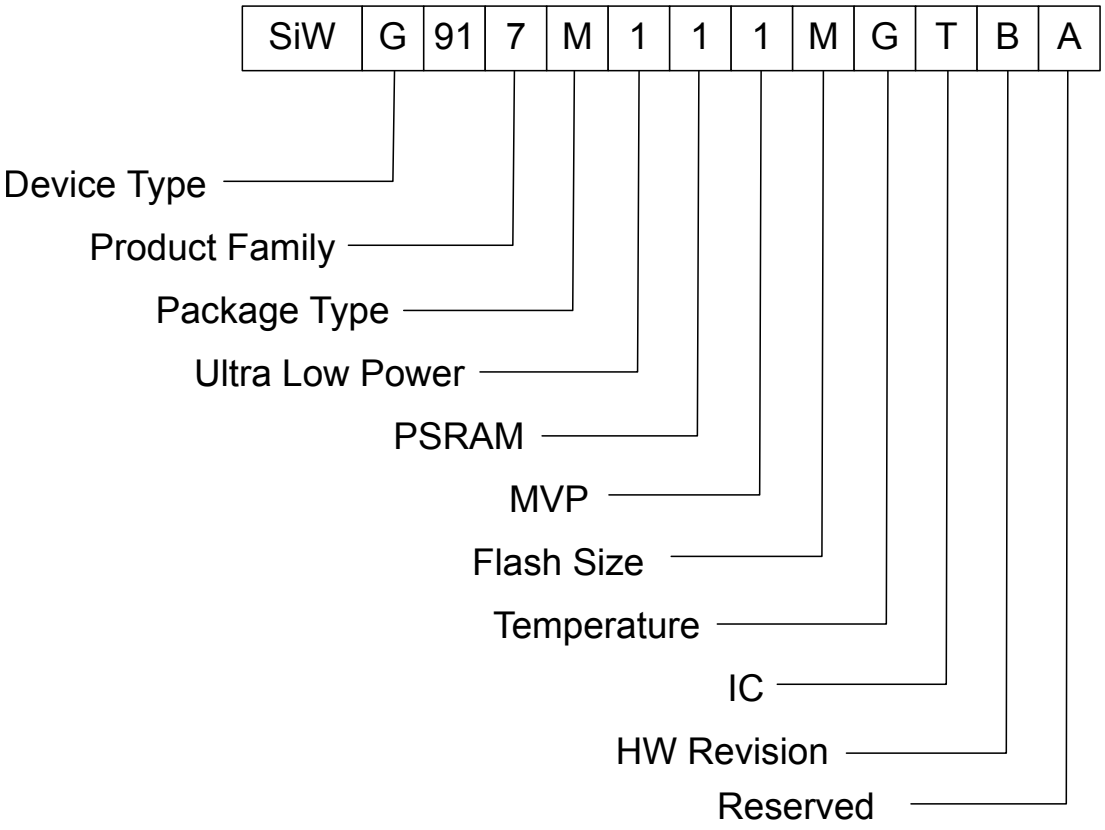


Figure 2.1. Ordering Guide

Table 2.1. OPN Decoder

Field	Options
Device Type	**T**: RCP (Transceiver) **N**: NCP **G**: SoC
Product Family	**7**: Ultra-low power
Package Type	**M**: DR-QFN
Ultra Low Power	**0**: ULP features disabled **1**: ULP Features enabled
PSRAM	**0**: No PSRAM Support **1**: External PSRAM **2**: 2 MB In-package PSRAM **4**: 8 MB In-package PSRAM
MVP	**0**: MVP features disabled **1**: MVP features enabled

Field	Options
Flash Size	**X**: No In-Package Flash **L**: 4 MB In-package Flash **M**: 8 MB In-package Flash
Temperature	**G**: -40ºC to 85ºC
IC/Module	**T**: IC Package
HW Revision	**B**: Revision B
Reserved	**A**: Reserved

Table 2.2. List of OPNs

Part Number	Common Features	PSRAM	MVP	Flash Size[2]	Temperature
SiWG917M111XGTBA	Wi-Fi 6, BLE Ultra low power SoC IC, 7x7 DR-QFN, Integrated 2.4 GHz Radio	External PSRAM	Enabled	No In-Package Flash	-40 to 85 ºC
SiWG917M110LGTBA		External PSRAM	Disabled	4 MB In-package Flash	-40 to 85 ºC
SiWG917M100MGTBA		No PSRAM support	Disabled	8 MB In-package Flash	-40 to 85 ºC
SiWG917M111MGTBA		External PSRAM	Enabled	8 MB In-package Flash	-40 to 85 ºC
SiWG917M121XGTBA		2 MB In-package PSRAM	Enabled	No In-Package Flash	-40 to 85 ºC
SiWG917M141XGTBA		8 MB In-package PSRAM	Enabled	No In-Package Flash	-40 to 85 ºC

Note:

1. Devices are shipped without firmware loaded. For custom parts with pre-loaded firmware, please contact Silicon Labs.
2. Parts with “No In-Package Flash” do not include internal flash. An external flash is required for operation with these parts.

Table of Contents

1. Feature List 2

2. Ordering Information 5

3. Applications. 11

4. Block Diagrams 12

5. System Overview 14

5.1 Introduction 14

5.2 ARM Cortex M4 14

5.2.1 Memory Architecture 15

5.3 Advanced Peripheral Bus (APB) 16

5.4 Interconnect. 17

5.5 Power Architecture 19

5.5.1 Highlights 19

5.5.2 Power Domains 20

5.5.3 Voltage Domains 22

5.5.4 Power States 23

5.5.5 Memory Retention in Sleep / Shutdown States 26

5.5.6 Wakeup Sources 27

5.5.7 System Power Supply Configurations 28

5.5.8 Power Management 28

5.6 Digital and Analog Peripherals and Interfaces 28

5.6.1 Digital Peripherals and Interfaces 29

5.6.2 Analog Peripherals and Interfaces 45

5.7 Bootloader 47

5.8 Security 47

5.8.1 Security Features 47

5.8.2 Secure Boot 48

5.8.3 Encrypted XiP 48

5.8.4 Secure Firmware Upgrade 48

5.8.5 Secure Zone 49

5.8.6 In-System Programming (ISP) 49

5.8.7 Debug Lock 49

5.9 Debug Support 49

5.10 WLAN 49

5.10.1 MAC 50

5.10.2 Baseband Processing 50

5.11 Bluetooth 50

5.11.1 MAC 50

5.11.2 Baseband Processing 51

5.12 RF Transceiver 51

5.12.1 Receiver and Transmitter Operating Modes 51

5.13 Host Interface Peripherals 51
5.13.1 Auto Host Detection 51
5.14 Embedded Wi-Fi Software 52
5.14.1 Security 52
5.15 Low Power Modes 52
5.15.1 ULP Mode 52
5.16 Wireless Subsystem Memory 52
5.16.1 On-Chip Memory 52
5.17 Pad Configuration 53
5.18 Interrupts 53
6. Pinout and Pin Description 54
6.1 Pin Diagram 54
6.2 Pin Description 55
6.2.1 RF and Control Interfaces 55
6.2.2 Power and Ground Pins 56
6.2.3 Peripheral Interfaces 57
6.2.4 Miscellaneous Pins 64
6.3 GPIO Pin Multiplexing 64
6.3.1 SoC GPIO Pin Multiplexing 65
6.3.2 ULP GPIO Pin Multiplexing 70
6.3.3 UULP VBAT GPIO Pin Multiplexing 73
6.3.4 Analog Functions 74
6.3.5 Digital Functions 75
6.4 Valid GPIO Sets for Peripherals 79
6.5 Functional Description 84
6.5.1 Digital Functions 84
6.5.2 Analog Functions 87
7. Electrical Specifications 89
7.1 Absolute Maximum Ratings 89
7.2 Recommended Operating Conditions 90
7.3 DC Characteristics 91
7.3.1 RESET_N and POC_IN Pins 91
7.3.2 Power On Control (POC) and Reset 92
7.3.3 Blackout Monitor 93
7.3.4 Nano Power Comparator and Brown Out Detection (BOD) 94
7.3.5 ULP Regulators 94
7.3.6 Power Management Unit 95
7.3.7 Thermal Characteristics 97
7.3.8 Digital I/O Signals 98
7.4 AC Characteristics 98
7.4.1 Clock Specifications 98
7.4.2 SDIO 2.0 Secondary 101
7.4.3 HSPI Secondary 102

7.4.4 GPIO Pins . . . 104
7.4.5 In-Package Flash Memory . . . 105
7.4.6 QSPI . . . 105
7.4.7 PSRAM . . . 107
7.4.8 I2C . . . 109
7.4.9 I2S/PCM Primary and Secondary . . . 111
7.4.10 ULP I2S/PCM Primary and Secondary . . . 113
7.4.11 SSI Primary/Secondary . . . 115
7.4.12 ULP SSI Primary . . . 118
7.4.13 GSPI Primary . . . 119
7.4.14 Cortex-M4 JTAG . . . 120
7.4.15 Cortex-M4 Trace . . . 121
7.4.16 Power State Wake Timing . . . 121
7.5 Analog Peripherals . . . 122
7.5.1 Analog Comparators . . . 122
7.5.2 AUX LDO Electrical Specifications - Regulation Mode . . . 123
7.5.3 AUX LDO Electrical Specifications - Bypass Mode . . . 123
7.5.4 Analog to Digital Converter . . . 124
7.5.5 Digital to Analog Converter . . . 125
7.5.6 Op-Amp . . . 126
7.5.7 Temperature Sensor . . . 127
7.6 RF Characteristics . . . 127
7.6.1 WLAN 2.4 GHz Transmitter Characteristics . . . 128
7.6.2 WLAN 2.4 GHz Receiver Characteristics on HP RF Chain . . . 129
7.6.3 WLAN 2.4 GHz Receiver Characteristics on LP RF Chain . . . 131
7.6.4 Bluetooth Transmitter Characteristics on High-Performance (HP) RF Chain . . . 133
7.6.5 Bluetooth Transmitter Characteristics on Low-Power (LP) 8 dBm RF Chain . . . 134
7.6.6 Bluetooth Transmitter Characteristics on Low-Power (LP) 0 dBm RF Chain . . . 135
7.6.7 Bluetooth Receiver Characteristics for 1 Mbps Data Rate . . . 136
7.6.8 Bluetooth Receiver Characteristics for 2 Mbps Data Rate . . . 138
7.6.9 Bluetooth Receiver Characteristics for 125 kbps Data Rate . . . 139
7.6.10 Bluetooth Receiver Characteristics for 500 kbps Data Rate . . . 139
7.7 Typical Current Consumption . . . 140
7.7.1 WLAN 2.4 GHz 3.3 V Current Consumption . . . 141
7.7.2 Bluetooth LE Current Consumption . . . 142
7.7.3 MCU Power State Current Consumption . . . 142
8. Reference Schematics, BOM and Layout Guidelines . . . 143
8.1 Schematics . . . 143
8.1.1 System Supplies . . . 143
8.1.2 RF Supplies . . . 144
8.1.3 GPIO Supplies . . . 145
8.1.4 RF Frontend . . . 146
8.1.5 LF Clock Options . . . 147
8.1.6 Flash Memory Configurations . . . 148
8.1.7 PSRAM Memory Configurations . . . 149
8.1.8 Reset . . . 150
8.1.9 Debug and In-System Programming . . . 151

8.2 BOM 153
8.3 Layout Guidelines for DR-QFN 156
8.4 Calibration Requirements 157
9. Package Specifications 158
9.1 Package Outline 158
9.2 PCB Land Pattern 161
9.3 Top Marking 163
10. SiWG917 Documentation and Support 164
11. Revision History 165

3. Applications

Smart Home

Smart Locks, Motion/Entrance Sensors, Water Leak sensors, Smart plugs/switches, Light Emitting Diode (LED) lights, Door-bell cameras, Washers/Dryers, Refrigerators, Thermostats, Consumer Security cameras, Voice Assistants, etc.

Other Consumer Applications

Toys, Anti-theft tags, Smart dispensers, Weighing scales, Fitness Monitors, Blood pressure monitors, Blood sugar monitors, Portable cameras, etc.

Other Applications (Medical, Industrial, Retail, Agricultural, Smart City, etc.)

Healthcare Tags, Industrial Wearables, Infusion pumps, Sensors/actuators in Manufacturing, Electronic Shelf labels, Agricultural sensors, Product tracking tags, Smart Meters, Parking sensors, Street LED lighting, Automotive After-market, Security Cameras, Gateways, etc.

4. Block Diagrams

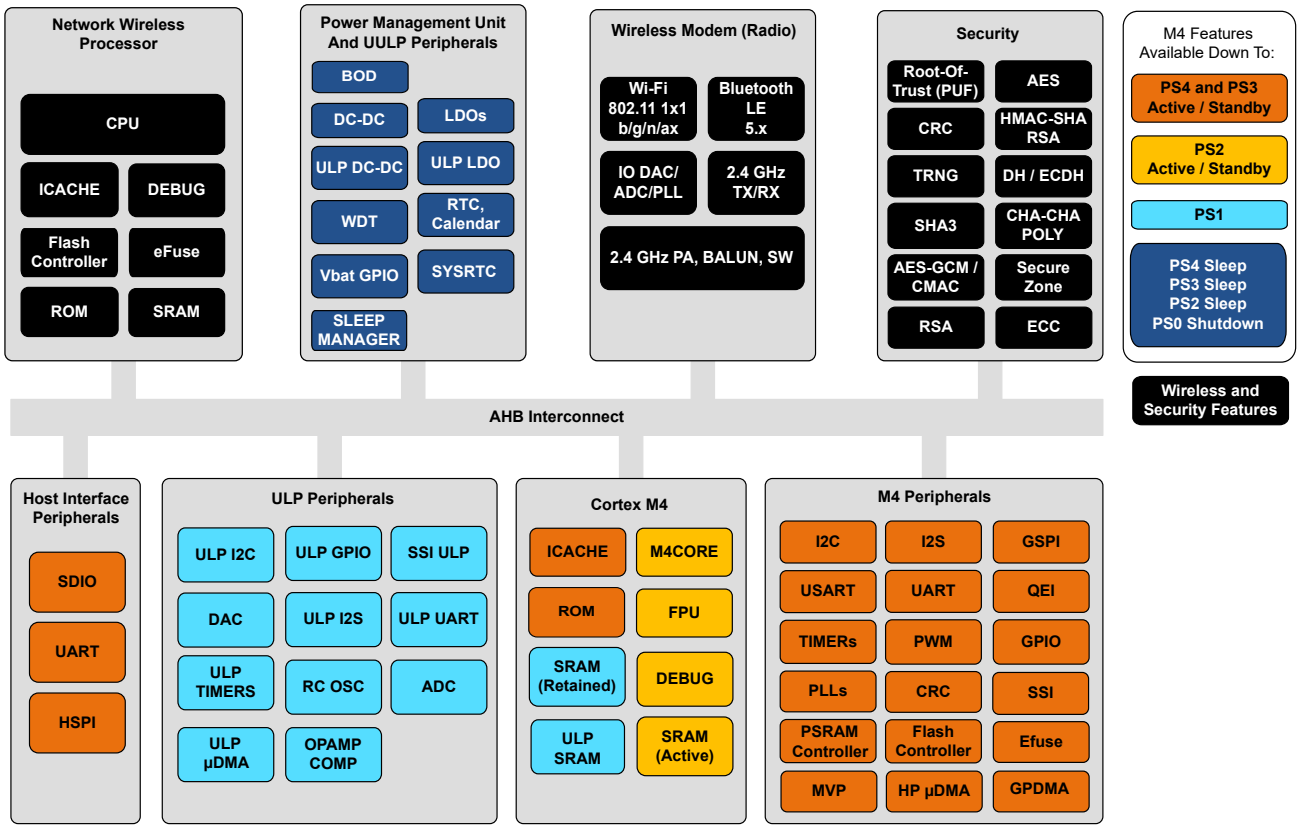


Figure 4.1. System Block Diagram

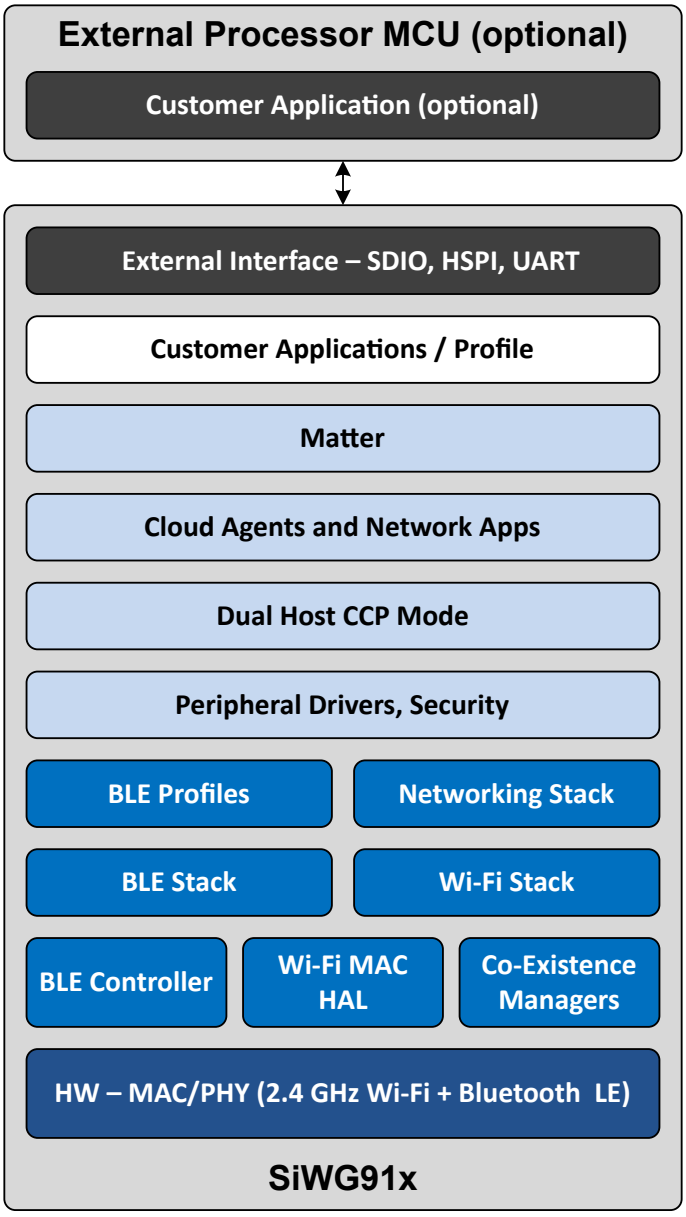


Figure 4.2. SiWG917 SoC Software Architecture

5. System Overview

5.1 Introduction

The SiWx91x SoC includes two processors: An ARM Cortex-M4 running up to 180 MHz and a Network Wireless Processor (NWP) 4-Threaded processor running up to 160 MHz. The Cortex-M4 is dedicated to peripheral and application related processing, whereas all the networking and wireless stacks run on independent threads of the NWP. In addition, in adherence to the Secure Execution Environment architecture, the NWP subsystem also acts as the secure processing domain and takes care of secure boot, secure firmware update, and provides access to security accelerators and secure peripherals through pre-defined APIs. The bus matrices of a Cortex-M4 and NWP are separate and asynchronous. Though the two processors are present in a single chip, it is ensured that the NWP Networking, Security, and Wireless subsystem is completely separated from the ARM Cortex-M4 based application subsystem. Thus, these two processors have separate power, clocks/PLLs, bus-matrices, and memory. This provides two key advantages: programming, operating and power-state independence between the two processors and enhanced security by restricting access to the NWP subsystem.

5.2 ARM Cortex M4

The ARM Cortex-M4 is the main application processor in the SiWx91x SoC. It is a high-performance 32-bit processor designed by ARM for the microcontroller market. It is built on a high-performance processor core, with a 3-stage pipeline Harvard architecture, making it ideal for demanding embedded applications. The M4 processor delivers exceptional power efficiency through an efficient instruction set and extensively optimized design, providing high-end processing hardware including IEEE754-compliant single-precision floating-point computation, a range of single-cycle and Single Instruction Multiple Data (SIMD) multiplication and multiply-with-accumulate capabilities, saturating arithmetic and dedicated hardware division. The Cortex M4 microcontroller integrated into SiWx91x supports the following features:

- FPU (Floating Point Unit), and NVIC (Nested Vectored Interrupt Controller) with 64 levels of interrupt priority.
- Debug port with both JTAG as well as Serial Wire Debug (SWD) interface; comprehensive debug functionality including data matching for a watch-point generation.
- To provide optimal power vs performance tradeoff, unique gear-shifting is available for the Cortex-M4 that enables optimal power consumption based on the required performance. The available power-states are Power State 4 (PS4) at up to 180 MHz, Power State 3 (PS3) at up to 90 MHz, and Power State 2 (PS2) at up to 32 MHz. More details are provided in Section 5.5.4 Power States .
- Architectural clock gates are included to minimize dynamic power dissipation.
- The Network Wireless Processor and Cortex-M4 communicate through thread to thread interrupting and memory.
- On-chip M4 SRAM of 192/256/320 KB based on the SiWx91x chip configuration.
- 8 KB is present in the ultra-low-power (ULP) peripheral subsystem. This memory is present on the S-bus of the Cortex-M4 and is primarily used by the ULP MCU peripherals like ULP I2S, etc.
- 64 KB of ROM which holds the Cortex-M4 peripheral drivers.
- 16 KB of instruction cache enabling eXecute In Place (XIP) with external quad/octal SPI Single Data Rate (SDR) flashes.
- Based on the SiWx91x package configuration, up to 8 MB of in-package Quad Serial Peripheral Interface (QSPI) flash is available for the Cortex-M4. This flash can be shared with the NWP in common flash mode.
- eFuse of 32 bytes (available for customer applications).
- 225 Dhrystone million instructions per second (DMIPS) performance.

The Cortex-M4 core includes the following core peripherals:

Nested Vectored Interrupt Controller

The NVIC is an embedded interrupt controller that supports low latency interrupt processing.

Floating-Point Unit

The Floating-point unit (FPU) provides IEEE754-compliant operations on single-precision, 32-bit, floating-point values. It supports addition, subtraction, multiplication, division and square root.

5.2.1 Memory Architecture

There are on chip Read Only Memory (ROM), Random Access Memory (RAM) and off-chip FLASH connectivity. Sizes of ROM/RAM/FLASH will vary depending on the chip configuration.

Highlights:

- Unified memory architecture - software can partition the memory between code and data usage.
- Multiport - RAMs support multi port access - allowing simultaneous access from different primaries (I, D, DMAs) to non overlapping regions without any cycle penalty.
- ROM/RAMs are tightly coupled to the M4 processor I/D buses to reduce the latency and power.

The Cortex-M4 processor has the following memory:

- On-chip M4 SRAM of 192/256/320 KB based on the chip configuration.
- 8 KB is present in the Ultra-low-power(ULP) peripheral subsystem. This memory is present on the S-bus of the Cortex-M4 and is primarily used by the ULP MCU peripherals like ULP I2S, ADC, DAC etc.
- 64 KB of ROM which holds the M4 peripheral drivers and bootloader.
- 16 KB of Instruction cache (I cache) enabling eXecute In Place (XIP) with external quad/octal SPI SDR flashes.
- Based on the package configuration up to 8 MB of "in-package" Quad SPI flash is available for the M4. This flash can be shared with the NWP in common flash mode .
- eFuse of 32 bytes (available for customer applications).
- Instruction cache (I cache) to execute code from PSRAM.
- Flash Memory:
  - Based on the package configuration (OPN) up to 8 MB of "in-package" Quad SPI flash is available.
  - In addition, IC can support external flash option.
    - IC has the support for 2-flash configuration
      - Common flash: Flash is common for both Cortex M4 and NWP.
      - Dual Flash: Separate flash can be used for Cortex M4 and NWP.

5.2.1.1 Flash Architecture

Details for Flash Architecture are explained in the Flash Memory Section of the Reference Manual.

5.2.1.2 SRAM Memory Sharing between Cortex M4 and Network Wireless Processor

A configurable SRAM feature for different processors can reduce the total on-chip memory requirement while addressing the memory requirements for different product modes.

The 91x SoC architecture allows different memory sizes allocated to the Cortex M4 and NWP processors based on the chip configuration at bootup time. The allocated memory will run on the respective processor clock. Through the efficient hardware design, memory sizes are divided and accessible by multiple processors in a single cycle using tightly coupled interfaces (TCM).

On-chip SRAM memory can be allocated to the two processors in four chunks: 352 KB, 64 KB, 64 KB, and 192 KB. The 352 KB chunk is always allocated to the NWP processor while the 192 KB chunk is always allocated to the Cortex M4. The remaining two 64 KB chunks can be allocated to either the Cortex M4 or the NWP processor. For example, if the NWP processor requires more than 352 KB, and the M4 does not need all 320 KB, an additional 64 KB or 128 KB can be allocated to the NWP.

Thus the available options are for the NWP to use 352, 416, or 480 KB SRAM, with the M4 using 320, 256, or 192 KB of SRAM, respectively.

Memory configuration between the MCU and Wireless Sub-system is shown in Table 5.11. Possible Memory Configurations between MCU and Wireless Sub-system

The NWP and M4 memory architecture is shown in Figure 5.1. NWP and M4 shared SRAM memory architecture. NWPSS is the Network Wireless Processor subsystem and M4SS is the Cortex M4 subsystem

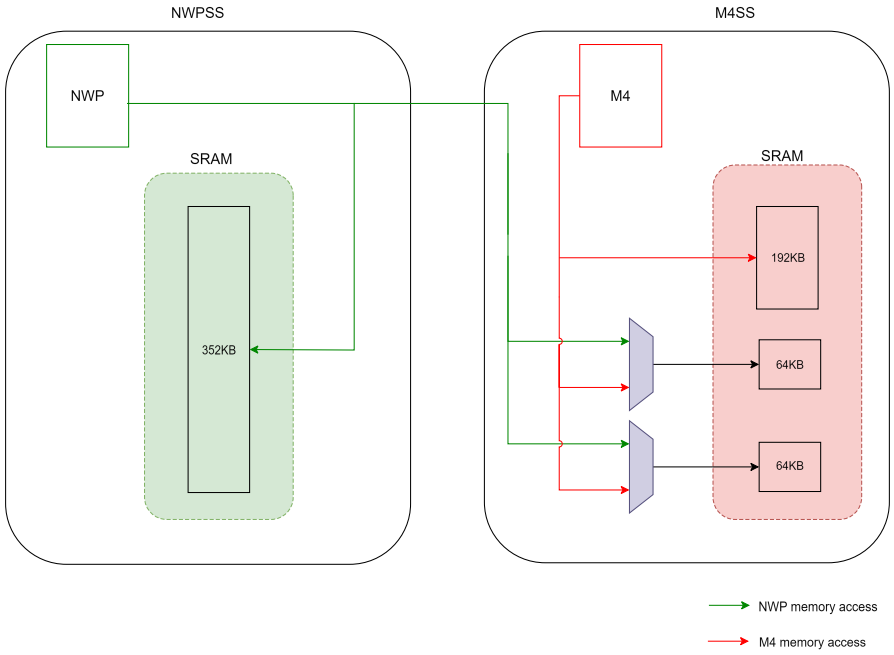


Figure 5.1. NWP and M4 shared SRAM memory architecture

5.3 Advanced Peripheral Bus (APB)

- The APB is part of the AMBA 3 protocol family.
- It provides a low-cost interface that is optimized for minimal power consumption and reduced interface complexity.
- The APB interfaces to any peripherals that are low-bandwidth and do not require the high performance of a pipelined bus interface.
- The APB has unpipelined protocol.
- All signal transitions are only related to the rising edge of the clock to enable the integration of APB peripherals easily into any design flow.
- Every transfer takes at least two cycles.
- It can be used to provide access to the programmable control registers of peripheral devices.

5.4 Interconnect

The following are the buses and bridges that form the interconnect in SiWx917 SoC. MCU refers to the Cortex-M4, and NWP refers to the Network Wireless Processor.

- High Performance (HP) MCU AHB Interconnect Matrix (ICM)
- MCU AHB-to-APB dual bridge
- MCU AHB-to-ULP MCU synchronous AHB bridge
- ULP MCU AHB ICM
- ULP MCU AHB-to-APB bridge
- MCU AHB - NWP AHB bridge
- High Performance NWP AHB ICM
- NWP AHB-to-APB dual bridge

The High Performance MCU AHB ICM is a multilayer interconnect implementation of the AHB protocol designed for higher performance and higher frequency systems.

Address Mapping

Table 5.1. MCU AHB Secondary Address Mapping has the base addresses of memories and high-speed peripherals.

Table 5.1. MCU AHB Secondary Address Mapping

Block Name	Size	Start Address
Memories		
LP SRAM	320 KB	0x0000_0000
ROM	64 KB	0x0030_0000
AHB Peripherals		
QSPI 1 Direct Access Mode	32 MB	0x0800_0000
QSPI 1 Indirect Access Mode	256 KB	0x1200_0000
QSPI 2 Direct Access Mode	32 MB	0x0A00_0000
QSPI 2 Indirect Access Mode	256 KB	0X1204_0000
SDIO/HSPI Secondary	64 KB	0x2020_0000
Icache	64 KB	0x2028_0000
GPDMA	512 KB	0x2108_0000
ULPSS AHB Bridge	256 KB	0x2404_0000
APB Bridge	64 MB	0x4400_0000
NWP AHB Bridge	512 MB	0x0010_0000 / 0x0040_0000 / 0x0060_0000 / 0x0400_0000 / 0x1000_0000 / 0x2010_0000 / 0x2040_0000 / 0x2100_0000 / 0x2200_0000 / 0x4000_0000
MVP Secondary	256 KB	0x2400_0000

Table 5.2. MCU APB Peripherals Address Mapping has the base addresses of all low-speed MCU peripherals.

Table 5.2. MCU APB Peripherals Address Mapping

Peripheral	Base Address
PERIPHERAL Power Domain	
UART0 (USART0 in asynchronous mode)	0x4400_0000
USART0 (USART0 in synchronous mode)	0x4400_0100
I2C0	0x4401_0000
SSI_MST	0x4402_0000
Micro DMA (µDMA)	0x4403_0000
SSI_SLV	0x4501_0000
UART1	0x4502_0000
GSPI	0x4503_0000
CONFIG_TIMER	0x4506_0000
CRC	0x4508_0000
HWRNG	0x4509_0000
I2C1	0x4704_0000
I2S0	0x4705_0000
QEI	0x4706_0000
MCPWM	0x4707_0000
Peripherals part of ALWAYS ON Domain	
VIC	0x4611_0000
ROM_PATCH	0x4612_0200
EGPIO	0x4613_0000
REG_SPI	0x4618_0000
PMU	0x4600_0000
PAD_CFG	0x4600_4000
MISC_CFG	0x4600_8000
EFUSE	0x4600_C000

Table 5.3. ULP MCU APB Address Mapping has the base addresses of all low-speed ULP MCU peripherals.

Table 5.3. ULP MCU APB Address Mapping

Peripheral	Starting Address
ULP_I2C	0x2404_0000
ULP_I2S	0x2404_0400
SSI_ULP	0x2404_0800
ULP Config	0x2404_1400
ULP_UART	0x2404_1800
ULP_TIMER	0x2404_2000
AUX ADC DAC Controller	0x2404_3800
UULP_APB	0x2404_8000
ULP_EGPIO	0x2404_C000
IPMU Reg Access SPI	0x2405_0000
ULP Memory	0x2406_0000
ULP Micro DMA (ULP µDMA)	0x2407_8000

5.5 Power Architecture

The Power Control Hardware implements the control sequences for transitioning between different power states (Active/Standby/Sleep/Shutdown) and the power control for different group of peripherals. In addition, wakeup from any of the Standby/Sleep/Shutdown states based on hardware events or peripheral interrupts is supported. The Standby and Shutdown states can be reached from Active mode only through a Wait for Interrupt (WFI) instruction. Wakeup from Standby/Sleep/Shutdown states is through a hardware event or interrupt (Peripheral or External).

5.5.1 Highlights

- Two integrated buck switching regulators enable efficient Voltage Scaling across wide operating mode currents.
- High performance and ultra-low-power MCU peripheral subsystems and buses.
- Multiple voltage domains with independent voltage scaling of each domain.
- Fine grained power-gating including peripherals, buses and pads, thereby reducing power consumption when the peripheral/buses/pads are inactive.
- Multiple active states using "gear-shifting" approach based on processing requirements, thereby reducing power consumption for low-power applications.
- Flexible switching between different active states with controls from software.
- Hardware based wakeup from Standby/Sleep/Shutdown states.
- All the peripherals are clock gated by default, thereby reducing the power consumption in inactive state.
- Timer-based wakeup configurable by software before going into sleep.

5.5.2 Power Domains

All the applications, high-speed interfaces, and peripherals are segregated into multiple power domains to achieve lower current consumption when they are inactive. At reset, all the domains are powered ON.

Table 5.4. List of Power Domains describes the different group of peripherals for which power is controlled through software.

Table 5.4. List of Power Domains

S.No	Section	Domain Name	Functionality of the Power Domain
1	APPLICATIONS	DEBUG_FPU	Debug Functionality for Cortex-M4, Floating Point Unit for Cortex-M4
		ROM	ROM Core/Interface
		SRAM	SRAM Banks
2	HIGH SPEED INTERFACE	QSPI_ICACHE	Quad/Octal 1 SPI SDR Flash Interface and ICache for the Cortex-M4 Processor, QSPI2 PSRAM interface
3	HP-PERIPHERALS	PERI_EFUSE	SPI/Synchronous Serial Interface (SSI) Primary, I2C, USART, Micro-DMA Controller, UART, SPI/SSI Secondary, Generic-SPI Primary, Config Timer, Random-Number Generator, CRC Accelerator, I2C, I2S Primary/Secondary, QEI, MCPWM and EFUSE for configuration information , MVP
		DMA	General Purpose DMA Controller
		SDIO-SPI	SDIO 2.0 Secondary, HSPI Secondary.
4	HIGH SPEED FLASH MEMORY	FLASH-LDO	Low DropOut (LDO)-FL 1.8 for Flash Memory
5	HIGH-FREQ-PLL	PLL-REGISTERS	PLL Programming Registers for High frequency clocks.
6	ULP-PERIPHERALS	DMA	Micro-DMA Controller
		ADC-DAC	ADC and DAC Controller
		I2C	I2C Primary/Secondary
		SSI	SPI/SSI Primary
		UART	UART
		TIMER	Timers
7	UULP-PERIPHERALS	WDT	Watch Dog Timer
		TS	Temperature Sensor Controller
		PS	Process Sensor Controller
		RTC	Real-Time Clock, MCU System Real-Time Clock (SYSRTC)
		STORAGE-DOMAIN1	Storage Flops - Set1. Contains 8 bytes
		STORAGE-DOMAIN2	Storage Flops - Set2. Contains 8 bytes
		STORAGE-DOMAIN3	Storage Flops - Set3. Contains 16 bytes
		SLEEP-FSM	Finite State Machine (FSM) for Sleep/Wakeup
		CLOCK-CALIB	Calibration block for Sleep Clock.
		BBFFS	Programming Registers which can be retained during sleep.
		DS-TIMER	DEEP SLEEP Timer.
		LP-FSM	Low-Power (LP) FSM
		RETEN	Retention Flops which can be retained during sleep.

S.No	Section	Domain Name	Functionality of the Power Domain
8	Analog-PERIPHERALS	Aux-ADC	Auxiliary ADC
		Aux-DAC	Auxiliary DAC
		BOD	Brown-Out Detector

The SRAM is also segregated into multiple power domains to achieve lower current consumption per the memory requirement. The power for the SRAM domains in active states can be controlled in the following manners:

- **Deep-Sleep with RAM Retention:** SRAM domains as described in the table below can be powered down for unused SRAM sections. This is configurable on a bank granularity. The RAM contents of powered down sections are not retained.
- **Deep-Sleep without RAM Retention:** No SRAM contents are retained, and the SRAM is not accessible in this state.

Table 5.5. Segregation of Power Domains for SRAM (328 KB) describes the segregation of power domains for SRAM (328 KB).

Table 5.5. Segregation of Power Domains for SRAM (328 KB)

S.No	Section	Domain Name	Functionality of the Power Domain
1	LP-SRAM	LP-SRAM-1	4 KB of SRAM (1x Banks)
		LP-SRAM-2	4 KB of SRAM (1x Banks)
		LP-SRAM-3	4 KB of SRAM (1x Banks)
		LP-SRAM-4	4 KB of SRAM (1x Banks)
		LP-SRAM-5	16 KB of SRAM (1x Banks)
		LP-SRAM-6	32 KB of SRAM (2x Banks)
		LP-SRAM-7	64 KB of SRAM (4x Banks)
		LP-SRAM-8	64 KB of SRAM (4x Banks)
		LP-SRAM-9	64 KB of SRAM (4x Banks)
		LP-SRAM-10	64 KB of SRAM (4x Banks)
2	ULP-SRAM	ULP-SRAM-1	2 KB of SRAM (1x Banks)
		ULP-SRAM-2	2 KB of SRAM (1x Banks)
		ULP-SRAM-3	2 KB of SRAM (1x Banks)
		ULP-SRAM-4	2 KB of SRAM (1x Banks)

5.5.3 Voltage Domains

All the applications, high-speed interfaces, and peripherals are segregated into multiple voltage domains to configure the operating voltages in different power states. This section describes the voltage domains and voltage source options available for each domain. These are configured based on the power state in which the device is operating. The voltage for each domain can be shut-off during sleep by configuring the source to SoC LDO (This supply is turned OFF during Sleep).

Table 5.6. List of Voltage Sources lists the different voltage sources and the possible output voltages of each source at different power states. The voltage sources are described in detail in Section 5.5.8 Power Management .

Table 5.6. List of Voltage Sources

S.No	Voltage Source	Possible Output Voltage
1	SoC LDO	1.15 V 1.05 V
2	SC-DC 1.05	1.05 V
3	LDO 0.75 V	0.75 V

Table 5.7. List of Voltage Domains lists the different voltage domains and the possible voltage sources for each domain.

Table 5.7. List of Voltage Domains

S.No	Voltage Domain	Functionality	SoC LDO	SC-DC 1.05 V	LDO 0.75 V
1	PROC-DOMAIN	M4 processor, DEBUG_FPU,	Yes	Yes	Yes
2	HIGH-VOLTAGE-DOMAIN	ICACHE, HIGH-SPEED-INTERFACES, HP-PERIPHERALS	Yes	No	No
3	LOW-VOLTAGE-LPRAM-16KB	LP-SRAM-1, LP-SRAM-2, LP-SRAM-3, LP-SRAM-4,	Yes	Yes	No
4	LOW-VOLTAGE-LPRAM	ROM LP-SRAM-5, LP-SRAM-6, LP-SRAM-7, LP-SRAM-8, LP-SRAM-9, LP-SRAM-10,	Yes	Yes	No
5	LOW-VOLTAGE-ULPPERIPH	ULP-PERIPHERALS	Yes	Yes	No
6	LOW-VOLTAGE-ULPRAM	ULP-SRAM	Yes	Yes	No
7	LOW-VOLTAGE-UULPPERIPH	UULP-PERIPHERALS	No	Yes	No

5.5.4 Power States

The power states available in different power modes (PS0, PS1, PS2, PS3, PS4) are listed below

- Reset State
- Active States
  - Power State1 (PS1)
  - Power State2 (PS2)
  - Power State3 (PS3)
  - Power State4 (PS4)
- Standby States
  - PS2-STANDBY
  - PS3-STANDBY
  - PS4-STANDBY
- Sleep States
  - PS2-SLEEP
  - PS3-SLEEP
  - PS4-SLEEP
- Shutdown States
  - Power State0 (PS0)

After reset, the M4 processor starts in the PS4 state which is the highest activity state where the full functionality is available. The other active states (PS2/PS3) will have limited functionality or processing power.

A transition from active states (PS2/PS3/PS4) to any other state (Sleep/Standby) can only be triggered by software.

A transition from Standby/Sleep/Shutdown states can be triggered by an enabled interrupt as configured by software before entering these states.

A transition from Standby/Sleep to active state is possible from where these states are entered.

There are different wakeup sources available in each Standby/Sleep/Shutdown state.

Figure 5.2. Power States shows the transitions between different power states.

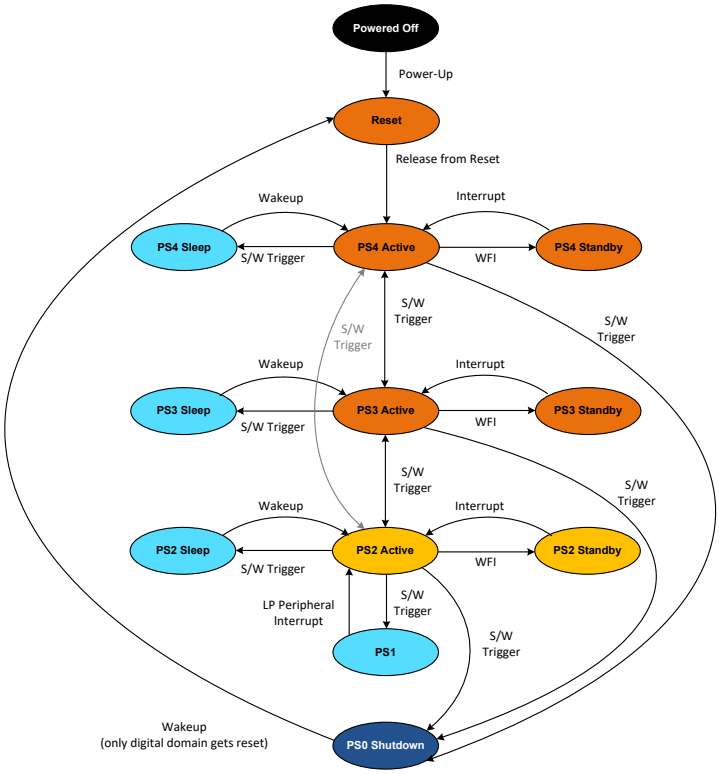


Figure 5.2. Power States

Note: Wakeup event from PS0, doesn't reset the complete system instead only digital domain undergoes a reset.

5.5.4.1 PS4

This is an active state where the complete functionality is available. The CPU, peripherals, and SRAM operate on the SoC LDO supply at voltage of 1.15 V.

The functionalities available in this state are mentioned below:

- Maximum CPU operating frequency of 180 MHz. The CPU can operate on the HIGH-FREQ-PLL output clocks.
- APPLICATIONS - DEBUG, FPU, ICACHE, and ROM.
- HIGH SPEED INTERFACE - as listed in Table 5.4. List of Power Domains.
- HIGH SPEED FLASH MEMORY - as listed in Table 5.4. List of Power Domains.
- HIGH-FREQ-PLL - as listed in Table 5.4. List of Power Domains.
- All the peripherals consisting of HP-PERIPHERALS, ULP-PERIPHERALS, Ultra Ultra Low Power (UULP-PERIPHERALS), and Analog-PERIPHERALS - as listed in the power domains section above.
- All GPIOs available: 30 (GPIO) + 11 (ULP_GPIO) + 4 (UULP_VBAT_GPIO)
- Complete SRAM of up to 328 KB (320 KB Low Power (LP)-SRAM and 8 KB ULP-SRAM).

5.5.4.2 PS3

This is an active state where the complete functionality is available, similar to PS4 state, but it operates at a lower voltage, thereby reducing current consumption. The CPU, peripherals, and SRAM operate on the SoC LDO supply with output voltage of 1.05 V. The Maximum CPU frequency is limited to 90 MHz in this state.

5.5.4.3 PS2

This is an active state where a limited set of functionality is available, and the device operates at a much lower voltage compared to PS3/PS4, thereby achieving lower current consumption. The CPU, peripherals, and SRAM can operate at different voltages and are configurable by software before entering this state.

The functionalities available in this state are mentioned below:

- CPU operating frequency depends on the voltage source selected for PS2 state. The CPU operates on the ULP-Peripheral AHB Interface clock.
  - If LDO 0.75 V is used, maximum frequency is 20 MHz.
  - If SC-DC 1.05 V is used, maximum frequency is 32 MHz.
- APPLICATIONS - DEBUG, FPU, and ROM.
- Limited peripherals consisting of ULP-PERIPHERALS, UULP-PERIPHERALS and Analog-PERIPHERALS - as listed in Table 5.4. List of Power Domains.
- GPIOs available: 11 (ULP_GPIO) + 4 (UULP_VBAT_GPIO)
- Total SRAM of up to 328 KB (320 KB Low Power (LP)-SRAM and 8 KB ULP-SRAM).

5.5.4.4 PS1

This state can be entered from PS2 only through a software instruction. The CPU is power-gated, and a limited set of peripherals are active. The peripheral interrupts are used as wakeup sources or to trigger sleep once the peripheral functionality is complete. The peripherals and SRAM operate at the same voltage as the PS2 state. The peripherals need to be configured by the software for the defined functionality in the PS2 state before entering this state.

The functionalities available in this state are mentioned below:

- Limited peripherals consisting of ULP-PERIPHERALS, UULP-PERIPHERALS, and Analog-PERIPHERALS - as listed in Table 5.4. List of Power Domains.
- GPIOs available: 11 (ULP_GPIO) + 4 (UULP_VBAT_GPIO)
- SRAM of 320 KB (Low Power (LP)-SRAM) can be retained in this state.
- SRAM of 8 KB (ULP-SRAM) is active for peripheral functionality.

5.5.4.5 STANDBY

This includes multiple states: PS4-STANDBY, PS3-STANDBY, and PS2-STANDBY. These are standby states entered from PS4/PS3/PS2 states through a WFI instruction. CPU is clock gated in this state. The STANDBY states allow for much faster wake times compared to PSx-SLEEP, PS1, and PS0.

All the interrupts in the NVIC table will act as a wakeup source in the PS4-STANDBY and PS3-STANDBY states. Wakeup sources for the PS2-STANDBY state are defined in the wakeup sources section below. See 5.5.6 Wakeup Sources for details.

5.5.4.6 SLEEP

This includes multiple states: PS4-SLEEP, PS3-SLEEP, and PS2-SLEEP. These sleep states can be entered from the PS4, PS3, and PS2 states respectively through a software instruction.

The status of resources in this state are as follows:

- UULP-PERIPHERALS and Analog-PERIPHERALS are available and are configured before entering this state.
- GPIOs available: 4 (UULP_VBAT_GPIO)
- SRAM can be retained.

Wakeup sources for these states are defined in 5.5.6 Wakeup Sources. While transitioning from sleep to active state, all the configuration related to peripheral registers are set to default.

5.5.4.7 PS0

This is a shutdown state entered from PS2, PS3, or PS4 state through a software instruction. The CPU is power-gated, and a much smaller set of peripherals are available.

The status of resources in this state are

- UULP-PERIPHERALS and Analog-PERIPHERALS are available and are configured before entering this state.
- GPIOs available: 4 (UULP_VBAT_GPIO)
- SRAM can not be retained.

5.5.5 Memory Retention in Sleep / Shutdown States

The table below indicates the SRAM banks and Backup Register Array which can be retained in each Sleep/Shutdown state.

Table 5.8. SRAM in Different States

S.No	Power State	LP-SRAM (320 KB)	ULP-SRAM (8 KB)	Backup Register Array (32 bytes)
1	PS4-SLEEP	Yes	Yes	Yes
2	PS3-SLEEP	Yes	Yes	Yes
3	PS2-SLEEP	Yes	Yes	Yes
4	PS1	Yes	Yes	Yes
5	PS0	No	No	Yes

5.5.6 Wakeup Sources

The table below indicates the wakeup sources available in Standby/Sleep/Shutdown states.

Table 5.9. List of Wakeup Sources in Different States

Wakeup Source	PS4 / PS3 STANDBY	PS2 STANDBY	PS4 / PS3 SLEEP	PS2 SLEEP	PS1	PS0
UULP VBAT GPIO	Yes	Yes	Yes	Yes	No[1]	Yes
Watch-Dog Interrupt	Yes	Yes	Yes	Yes	No[1]	Yes
Analog Comparator	Yes	Yes	No	No	Yes	No[1]
BOD	Yes	Yes	Yes	Yes	No[1]	Yes
ULP-Peripheral SDC	Yes	Yes	No	No	Yes	No
Network Wireless Processor Interrupt	Yes	No	Yes	No[1]	No[1]	No[1]
Deep-Sleep Timer Interrupt	No	No	Yes	Yes	No[1]	Yes
Alarm Interrupt	Yes	Yes	Yes	Yes	No[1]	Yes
Second Based Interrupt	Yes	Yes	Yes	Yes	No[1]	Yes
SysRTC	Yes	Yes	Yes	Yes	No[1]	Yes
ULP-Peripheral GPIO Group Interrupt	Yes	Yes	No	No	Yes	No
ULP-Peripheral GPIO Pin Interrupt	Yes	Yes	No	No	Yes	No
ULP-Peripheral SPI/SSI Primary Interrupt	Yes	Yes	No	No	No[1]	No
ULP-Peripheral I2S Interrupt	Yes	Yes	No	No	No[1]	No
ULP-Peripheral I2C Interrupt	Yes	Yes	No	No	No[1]	No
ULP-Peripheral UART Interrupt	Yes	Yes	No	No	Yes	No
ULP-Peripheral ADC/DAC Interrupt	Yes	Yes	No	No	Yes[3]	No
ULP-Peripheral DMA Interrupt	Yes	Yes	No	No	No[1]	No
ULP-Peripheral Timer Interrupt	Yes	Yes	No	No	Yes	No

1. Supported in hardware, but not supported in the SDK at the time of data sheet release.
2. For information about software roadmap features, contact Silicon Labs or refer to SDK Release Notes.
3. DAC is not supported in PS1 state.

5.5.7 System Power Supply Configurations

SiWG917 chipsets support highly flexible power supply configurations for various application scenarios. Two application scenarios are listed below.

- 3.3 V single supply - A single 3.3 V supply derived from the system PMU can be input to all I/O supplies.
- 1.8 V and 3.3 V supply - A 1.8 V supply derived from the system PMU can be input to all I/O supplies except PA2G_AVDD. A 3.3 V supply derived from system Power Management Unit (PMU) can be fed to the power amplifier supply pin PA2G_AVDD. There will be slight RF performance degradation if antenna select signals (ULP_GPIO_4, ULP_GPIO_5, ULP_GPIO_0) are powered at 1.8 V from the ULP_IO_VDD supply.

5.5.8 Power Management

The SiWG917 chipsets have an internal power management subsystem, including DC-DC converters and linear regulators. This subsystem generates all the voltages required by the chipset to operate from a wide variety of input sources.

- LC DC-DC switching converter for RF and digital blocks
  - Input voltage (1.8 V or 3.3 V) on pin VINBCKDC
  - Nominal Output - 1.45 V and 170 mA maximum load on pin VOUTBCKDC
- SC DC-DC - Switching converter for Always-ON core logic domain
  - Input voltage (1.8 V or 3.3 V) on pin UULP_VBATT_1 and UULP_VBATT_2
  - Nominal Outputs
    - 1.05 V on pin UULP_VOUTSCDC
    - 0.75 V on pin UULP_VOUTSCDC_RETN
- SoC LDO - Linear regulator for digital blocks
  - Input - 1.45 V from LC DC-DC or external regulated supply on pin VINLDOSOC
  - Nominal Output - 1.15 V and 100 mA maximum load on pin VOUTLDOSOC
- LDO RF and AFE - Linear regulator for RF and AFE
  - Input - 1.45 V from LC DC-DC or external regulated supply on pin RF_AVDD
  - Nominal Output - 1.21 V on pin VOUTLDOAFE

  Note: Output of VOUTLDOAFE will be 0.75 V - 1.05 V after initial power-up, until the RF has been initialized.

- Flash LDO - Linear regulator for In-package flash and external memories
  - Input voltage (1.8 V or 3.3 V) on pin VINLDO1P8
  - Nominal Output - 1.8 V and 48 mA maximum load on pin VOUTLDO1P8

5.6 Digital and Analog Peripherals and Interfaces

In addition to the wireless interfaces, SiWx91x provides a rich set of peripherals and interfaces - both digital and analog - thus enabling varied systems and applications. The following are the categories of the peripherals and interfaces, description of each category, and list of the peripherals in that category.

5.6.1 Digital Peripherals and Interfaces

5.6.1.1 I²C

- Up to three I²C primary/secondary controllers - two in MCU HP peripherals and one in the MCU ULP subsystem
- I²C standard compliant bus interface with open-drain pins
- Configurable as Primary or Secondary
- Four speed modes: Standard Mode (100 kbps), Fast Mode (400 kbps), Fast Mode Plus (1 Mbps), and High-Speed Mode (3.4 Mbps)
- 7 or 10-bit addressing
- 7 or 10-bit combined format transfers
- Support for Clock synchronization and Bus Clear
- Programmable SDA Hold time

The I²C controllers also support additional features listed below to reduce the load on the M4 processor:

- Integrated transmit and receive buffers with support for DMA
- Bulk transmit mode in I²C Secondary mode
- Interrupt based operation (polled mode also available)

5.6.1.2 UART/USART

- Up to two UART and one USART controllers
- 9-bit serial data support
- Multi-drop RS485 interface support
- 5, 6, 7, and 8-bit character encoding with even, odd, and no parity
- 1, 1.5 (only with 5 bit character encoding) and 2 stop bits
- Hardware Auto flow control (RTS/CTS)

The UART controllers also support additional features which are listed below and which help in achieving better performance and reducing the burden on the M4 processor:

- Programmable fractional baud rate support
- Programmable baud rate supporting up to 5 Mbps
- Programmable FIFO thresholds with maximum FIFO depth of 16 and support for DMA
- Prioritized interrupt identification

The following features are supported by the USART controller in the MCU HP peripherals (USART0):

- Support for both synchronous and asynchronous modes.
- Supports full duplex and half duplex (single wire) mode of communication.
- 5-8 bit wide character support.
- Supports programmable baud rates up to 20 Mbps in synchronous mode
- Programmable FIFO thresholds with maximum FIFO depth of 16 and support for DMA
- Supports generation of interrupt for different events.

The UART controller in the MCU ULP subsystem (ULP_UART) supports the following additional power-save features:

- After the DMA is programmed in PS2 state for UART transfers, the MCU can switch to PS1 state (M4 processor is turned off) while the UART controller continues with the data transfer
- In PS1 state (ULP Peripheral mode) the UART controller completes the data transfer and, triggered by the peripheral interrupt, shifts to the PS2 active state.

5.6.1.3 I²S / PCM

- Up to two I²S controllers
- Each I²S supports PCM mode of operation
- The I2S0 supports two stereo channels while the ULP_I2S and the NWP/Security subsystem I²S support one stereo channel
- Programmable audio data resolutions of 12, 16, 20, 24, and 32 bits.
- Supported audio sampling rates are 8, 11.025, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96, and 192 kHz
- Support for primary and secondary modes
- Full duplex communication due to the independence of transmitter and receiver

The PCM mode of operation supports the following additional features:

- Mono audio data is supported
- Supports two modes for data transmission with respect to the Frame Synchronization signal – the MS bit is transmitted in the same clock cycle that the Frame Synchronization signal is asserted or one clock cycle after the Frame Synchronization signal is asserted
- Programmable FIFO thresholds with maximum FIFO depth of 8 and support for DMA
- Supports generation of interrupts for different events

The I²S in the MCU ULP subsystem supports the following additional power-save features:

- After the DMA is programmed in PS2 state for I²S transfers, the MCU can switch to PS1 state (M4 processor is turned off) while the I²S controller continues with the data transfer
- In PS1 state (ULP Peripheral mode) the I²S controller completes the data transfer and, triggered by the Peripheral Interrupt, shifts to the PS2 active state.

5.6.1.4 Quadrature Encoder Interface (QEI)

- Tracks encoder wheel position
- Programmable for 1x, 2x, or 4x position counting. Increments/decrements depending on direction.
- Index counter for revolution counting
- Velocity capture using built-in timer
- Supports position counter reset for rollover/underflow or index pulse
- Position, index, and velocity compare registers with interrupts
- Supports logically swapping the A and B inputs
- Accepts decoded signal inputs (clock and direction) in timer mode

5.6.1.5 Motor Control PWM (MCPWM)

- Part of the MCU HP peripheral subsystem
- Supports up to eight PWM outputs with four duty cycle generators, with PWM outputs designed to be used in pairs
- Complementary and independent output modes are supported
- Dead time insertion in complementary mode
- Manual override option for PWM output pins. Output pin polarity is programmable
- Supports generation of interrupt for different events
- Supports two hardware fault input pins
- Special event trigger for synchronizing analog-to-digital conversions

5.6.1.6 Synchronous Serial Interface (SSI) Primary

- Up to two Synchronous Serial Interface (SSI) primaries
- The SSI_MST provides an option to connect up to four secondaries and supports single, dual, and quad modes.
- The SSI_ULP supports single-bit mode and can be connected to only one secondary
- Programmable receive sampling delay

In addition to the above features, the SSI primaries reduce the load on the M4 processor by supporting the features below:

- Programmable FIFO thresholds with maximum FIFO depth of 16 and support for DMA
- Supports generation of interrupt for different events
- Programmable division factor for generating SSI clock out

The SSI_ULP supports the following additional power-save features:

- After the DMA is programmed in the PS2 state for SSI transfers, the MCU can switch to PS1 state (M4 processor is turned off) while the SSI primary continues with the data transfer.
- In PS1 state (ULP Peripheral mode), the SSI primary completes the data transfer and, triggered by the peripheral interrupt, shifts to the PS2 active state.

5.6.1.7 Synchronous Serial Interface (SSI) Secondary

- Support for SSI Primaries which comply with Motorola SPI, TI SSP and National Semiconductors Microwire protocols
- Programmable FIFO thresholds with maximum FIFO depth of 16 and support for DMA
- Supports generation of interrupt for different events

5.6.1.8 Secure Digital I/O (SDIO) Secondary Interface

- Full throughput with SDIO 1.2 as well as with SDIO 2.0
- Supports up to 50 MHz
- Supports full-speed and high speed modes
- Supports SD-1 bit and SD-4 bit modes
- Supports only function 1
- Supports interrupt for host abort, CRC Error, CMD52 and CMD53 interrupts
- Supports single as well as multiple block transfers for CMD53 access
- Supports CMD52 while CMD53 data transfer is in progress
- Supports CMD52 Abort
- Supports Read Wait
- Does not support Suspend/Resume
- Provides primary and secondary interfaces on system side AHB Bus
- Supports CIS memory configuration during boot up
- Supports system soft reset from host

  There is a constraint on the minimum SoC clock relative to SDIO clock. SoC clock has to be a minimum half of SDIO clock. This constraint is due to the synchronization mechanism used between the SoC clock domain and SDIO clock domain.

5.6.1.9 HSPI Secondary

- 4-pin serial interface
- Supports 8-bit and 32-bit data
- Supports frequencies up to 100 MHz
- SPI clock can be at the max 4 times higher than AHB clock
- Support for DMA
- Supports AHB interface for accessing data from SoC
- Supports system soft reset from external host

5.6.1.10 State Configurable Timer (SCT)

- Supports 1 configurable input and 2 output signals.
- Supports two 16-bit configuration timer
- The timers accept clocks or events as input tick.
- Wide range of features like starting the counter, stopping the counter, continuing the counter from the stopped value, halt, increment the counter and capturing the events
- Support for PWM signals as output with any cycle/pulse length and superimpose a waveform on the PWM signal.
- Support for DMA flow control
- Generates interrupt for different events

5.6.1.11 CRC Accelerator

- Part of MCU HP peripheral subsystem
- Support for one 32 bit polynomials
- Support for one 32 bit stream-in data widths
- Supports DMA flow control

5.6.1.12 Enhanced GPIO (EGPIO)

- Two EGPIO controllers - one in MCU HP and MCU ULP subsystem
- Supports various alternate functions like set, clear, toggle on all the pins
- Option to program Mode for each GPIO pin independently
- Supports edge and level detection based interrupt generation

5.6.1.13 Generic SPI (GSPI) Primary

- Part of MCU HP peripheral subsystem
- Supports single bit SPI primary mode.
- Support for Mode-0 and Mode-3 (Motorola)
- Supports both Full speed and High speed modes
- SPI clock out is programmable to meet required baud rates
- Support for full duplex mode
- Connect up to three SPI peripheral devices
- Support byte swapping during read and write operation
- Support up to 32 KB of read data from a SPI device in a single read operation
- Programmable FIFO thresholds with maximum FIFO depth of 16 and support for DMA
- Generates interrupt for different events

5.6.1.14 Hardware Random Number Generator (HRNG)

- Part of MCU HP peripheral subsystem
- Supports 32-bit True Random Number Generator
- Supports 32-bit Pseudo Random Number Generator
- Option to selectively enable these random number generators

5.6.1.15 General Purpose DMA (GPDMA)

- Two primaries interface over AHB bus
- Supports 8 channels
- Linked-list based descriptors
- Has two AHB primaries for parallel data transfer. The Primary is selectable for descriptor fetch, per channel and per source and destination
- Dynamically configurable FIFO for 8 channels
- Programmable source and destination burst sizes
- Programmable beats per bursts
- Source and Destination address alignment
- Programmable Transfer Types: Memory to Memory, Memory to Peripheral and Peripheral to Memory
- Programmable priority encoded arbiter
- Supports generation of interrupt for different events
- Support for DMA squash
- Support for memory Zero Fill and One Fill

5.6.1.16 Micro DMA (µDMA)

- There are two Micro DMA controllers - one is a HP peripheral and the other is an ULP peripheral.
- Supports 32 channels
- Each DMA channel has dedicated handshake signals and programmable priority level
- Supported transfer types: memory-to-memory, memory-to-peripheral, peripheral-to-memory
- Supports multiple DMA cycle types and transfer data widths
- Programmable number of transfers in a single DMA cycle
- Average throughput is four cycles per one word reading
- Each DMA channel can access a primary, and alternate, channel control data structure
- Supports generation of interrupt for different events
- Support half-word (16 bit) and word (32 bit) size transfers

5.6.1.17 eFuse Controller

- Provides 32 bytes eFuse as one-time programmable memory locations
- Supports eFuse programming and read operations
- Supports memory mapped and FSM based read operation

5.6.1.18 SPI Flash Controllers

A serial flash device is a non-volatile memory that can be electrically erased and reprogrammed. It is used for storing executable code or data readily available for M4/NWP processor. After power-up, the executable code is read by the M4/NWP processor from the serial flash and then executed. The code in the serial flash is write-protected and cannot be altered.

Serial flash memories are controlled by many kinds of serial interface protocols (SPI, SSP, SSI, SMI, etc.). The SiWG917 supports SPI based flash. SPI flash memory is a secondary device.

To access it, dedicated QSPI flash controller is present which is Primary.

SiWG917 has a QSPI flash controller which has 2/4/8 - wired interface for serial access of data from flash. The QSPI controller can be used in either single, dual, quad or octal modes with support for SDR to read the processor's instructions and for data transfers to/from the flash. The controller supports inline decryption of encrypted instructions read from the flash before they are passed on to the M4/NWP processor's instruction cache. Instructions are read using the Direct Access mode while data transfers use the Indirect Access mode in case of the flash. The QSPI controllers in the MCU have been designed with programmable options for most of the single and multi-bit operations so that it can interface with flash ICs. The Direct Access mode is used to read instructions and data directly from flash. It supports inline decryption using an AES engine for the instructions or data transfer with flash. The Indirect Access mode is used to read and write data/instructions from flash. The two modes - Direct Access and Indirect Access - can be used to access the same flash or two different flashes (using CSN0 and CSN1) at a time by enabling hardware controlled mode. The QSPI controllers have independent AHB secondaries for these modes of access.

SiWG917 can use a single common SPI flash for executing instructions by both NWP and M4 processors. Each processor has dedicated QSPI flash controller. Dynamic arbitration has taken place between two controllers without any processor intervention for executing instructions from common flash. Arbitration multiplexes the two SPI interfaces into a single SPI interface connected to the flash. The flash memory is partitioned into two parts dedicated to each processor respectively.

There are two flash configurations available, as shown in the figures below.

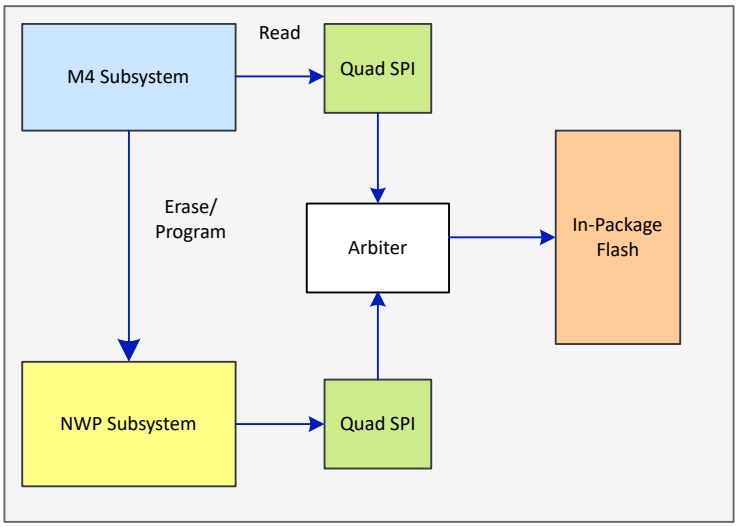


Figure 5.3. Common Flash Configuration

In the common flash configuration, flash is shared between both NWP and M4 processors. flash Initialization, configuration, program and erase can be done only by NWP processor. M4 processor can do only instruction fetching in direct access mode. Flash memory is divided into two regions, one each for the processor. M4 can only read M4 assigned memory region. NWP has no restriction and it can access complete flash memory.

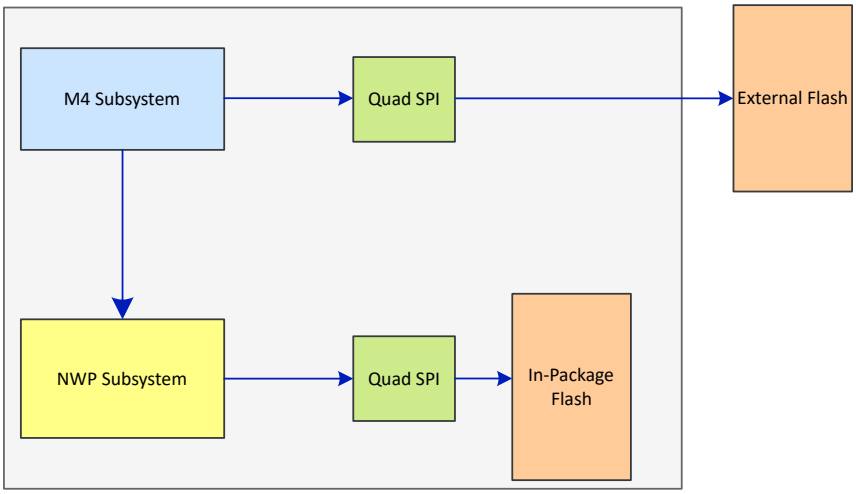


Figure 5.4. Dual Independent Flash Configuration

In the dual flash configuration, each processor has its own dedicated flash memory. In this configuration, M4 can access complete flash memory. M4 can perform flash initialization, configuration, programming and erase.

The features of the SPI flash primary controller are given below.

- Supports Single/Dual/Quad/Octal (S/D/Q/O) modes for reading M4/NWP processor instructions and data transfers to/from flash.
- Support for SPI Mode-0 and Mode-3
- Support for SDR mode flash
- Supports both 8 and 16-bit flash commands.

- Support both 24 and 32-bit addressing modes
- Supports inline decryption (AES) in XTS/CTR mode with 128-bit and 256-bit key sizes while reading encrypted instructions from the flash
- Supports up to two flashes connected to CSN0 and CSN1
- Direct Access Mode:
  - Instructions are read from flash using the Direct Access mode which does not need any processor involvement after the initial configuration of the controller. The read command used for this mode is programmable depending on the flash used.
  - Direct Access mode supports Wrap / Incremental / Single read operations.
  - Supports prefetch option - enabling this option makes the SPI controller prefetch the next instruction before the request is posted on the internal AHB bus. If the address for the next instruction is different from the prefetch address, the instruction is scrapped.
  - Supports continuous fetch option to reduce instruction fetch delay from flash - this option makes the SPI controller to post the Command and Address only once on the bus to read contiguous instructions by controlling only the CSN.
  - Supports programmable CSN high time.
- Indirect Access Mode:
  - Configuration of flash and reading/writing data from/to the flash uses the Indirect Access mode which requires the M4/NWP processor to program the SPI flash controller for each access.
  - Supports reading of up to 32 KB of data from flash in a single read operation.
  - In addition to 24 and 32-bit addressing, the SPI controller supports 9, 10 and 16-bit addressing in this mode.
- Common flash mode - flash can be accessed by both MCU and NWP simultaneously
- Clock Configuration
  - Support for selection of source clock between AHB bus clock and PLL clock.
  - Support for even division factors up to 64 to generate the SPI clock from the source clock.
- Transmission of Extra-byte after the address phase is supported. The contents of this byte are programmable. There is also an option to only transmit the first nibble of the extra byte and maintain a Hi-z on the bus for the next nibble.
- Each phase of a Read operation (Command, Address, Dummy Byte, Extra Byte, Read Data) can be in any of the S/D/Q/O modes depending on the flash requirements.
- The number of dummy bytes is programmable and can be programmed as per the instruction and the mode of operation.
- Supports DMA flow control and programmable FIFO thresholds
- Supports interrupt generation based on different events
- Supports dual flash mode - reading of data from two flashes simultaneously
- Supports flash Write Protect

The SPI controller in the MCU has been designed with programmable options for most of the single and multi-bit operations so that it can interface with flash ICs from multiple vendors.

Note: The QSPI controller interface is available only for interface to serial flash devices. It cannot be used as a general SPI peripheral.

5.6.1.19 SPI PSRAM Controllers

For applications that require additional RAM, an additional external RAM can be added in the form of pseudo static RAM (PSRAM). The PSRAM is an additional RAM of size that is selected e.g. 2/4/8/16 MB.

PSRAM memory is a QSPI secondary device. M4 microcontroller communicates with the PSRAM through dedicated Quad SPI Primary controller.

SiWG917 has SPI PSRAM controller which has 2/4/8 - wired interface for serial access of data from PSRAM. Dedicated SPI controllers are present for PSRAM. It can be used in either Single, Dual or Quad modes with support for SDR to read the M4 processor's instructions and for data transfers to/from the PSRAM. The controller supports inline decryption of encrypted instructions read from the PSRAM before they are passed on to the M4 processor's Instruction Cache. The SPI controllers in the MCU have been designed with programmable options for most of the single and multi-bit operations so that it can interface with PSRAM ICs. The Direct Access mode is used to read instructions and read/write data directly to/from PSRAM. It supports inline decryption using an AES engine for the instructions or data transfer with PSRAM. The Indirect Access mode is used to read and write data/instructions from PSRAM. The two modes - Direct Access and Indirect Access - can be used to access the same PSRAM or two different PSRAM (using CSN0 and CSN1) at a time by enabling hardware controlled mode. The SPI controllers have independent AHB secondaries for these modes of access.

The features of SPI PSRAM Primary controller is given below.

- Supports Single/Dual/Quad (S/D/Q/O) modes for reading M4 processor instructions and data transfers to/from PSRAM.
- Support for SPI Mode-0.
- Supports full duplex mode in single-bit SPI mode. Support for HOST SPI secondary interface.
- Support for SDR mode PSRAMs
- Supports both 8 and 16-bit PSRAM commands.
- Support both 24 and 32-bit addressing modes
- Supports only AES CTR mode encryption and decryption of PSRAM data with 128-bit and 256-bit key sizes
- Supports up to two PSRAMs connected to CSN0 and CSN1
- Supports Direct mode write
- Supports semi direct mode read operation for PSRAM
- Direct Access Mode:
  - Data transfer from/to PSRAM using the Direct Access mode which does not need any M4 processor involvement after the initial configuration of the controller. The read/write command used for this mode is programmable depending on the PSRAM used.
  - Direct Access mode supports Wrap / Incremental / Single read operations.
  - Supports prefetch option - enabling this option makes the SPI controller prefetch the next instruction before the request is posted on the internal AHB bus. If the address for the next instruction is different from the prefetch address, the instruction is scrapped.
  - Supports continuous fetch option to reduce instruction fetch delay from PSRAM - this option makes the SPI controller to post the Command and Address only once on the bus to read contiguous instructions by controlling only the CSN.
  - Supports programmable CSN high time.
- Indirect Access Mode:
  - Configuration of PSRAM and reading/writing data from/to the PSRAM uses the Indirect Access mode which requires the M4 processor to program the SPI controller for each access.
  - Supports reading of up to 32 KB bytes of data from PSRAM in a single read operation.
  - In addition to 24 and 32-bit addressing, the SPI controller supports 9, 10 and 16-bit addressing in this mode.
- Clock Configuration
  - Support for selection of source clock between AHB bus clock and PLL clock.
  - Support for even division factors up to 64 to generate the SPI clock from the source clock.
- Each phase of a Read operation (Command, Address, Dummy Byte, Extra Byte, Read Data) can be in any of the S/D/Q/O modes depending on the PSRAM requirements.
- The number of dummy bytes is programmable and can be programmed as per the instruction and the mode of operation.
- Supports DMA flow control and programmable FIFO thresholds
- Supports configurable memory ranges on which we can save code in encrypted form and the execution will happen with inline decryption.
- Supports dual PSRAM mode - reading and writing from/to two PSRAM simultaneously
- Supports interrupt generation based on different events

The SPI controllers in the MCU have been designed with programmable options for most of the single and multi-bit operations so that it can interface with PSRAM ICs from multiple vendors.

5.6.1.20 FLASH and PSRAM Supply Connections

There are four unique configuration options for flash and PSRAM connection to the SiWG917

1. In-package Flash/PSRAM
2. Only external Flash
3. In-package PSRAM and External Flash
4. In-package Flash and External PSRAM

For these combinations, either the in-package Flash LDO supply or an external supply can be used. The flash supply, PSRAM supply and I/O supply configurations are different for each case.

Refer to Application Note AN1494 for more details about various modes, configurations, GPIO pins, latest up-to-date list of supported Flashes & PSRAMs, and other information.

Table 5.10. Estimated Deepsleep/DTIMs current with PSRAM for different input supply options

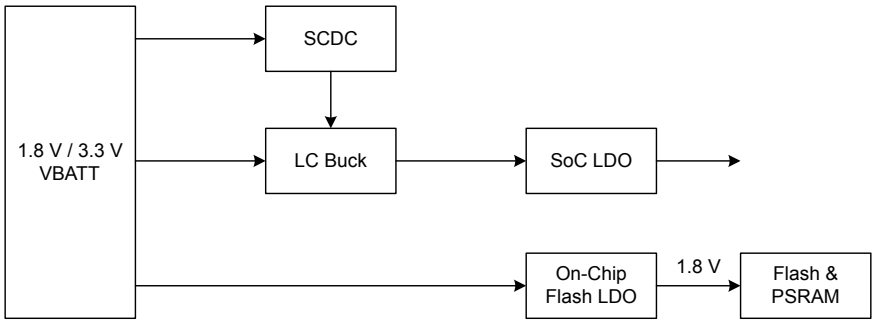
Options	Buck	SoC LDO	Flash LDO / PSRAM	Description	Estimated Deepsleep Current with PSRAM (for VBATT = 3.3 V)	Estimated DTIM-10 Standby Current with PSRAM (for VBATT = 3.3 V)	Estimated DTIM-3 Standby Current with PSRAM (for VBATT = 3.3 V)
1	In-package	In-package	In-package	Single VBATT supply is connected to Chip (either 1.8 V or 3.3 V) VBATT to be connected to LC Buck input and LC Buck output is 1.45 V LC Buck output (1.45 V) is connected to SoC LDO and its output is 1.05 V VBATT input is connected to Flash LDO and its output is 1.8 V In deep sleep mode: Keep LC buck in PFM mode, and SoC LDO output at 0.9 V	350 uA	390 uA	435 uA
2	In-package	In-package	External	VBATT to be connected to LC Buck input, LC Buck output is 1.45 V Connect external 1.8 V supply to PSRAM and IO supplies. Connect on-chip Flash LDO to in-package flash In deep sleep mode: Program Buck output as 0.9 V and keep SoC LDO in Bypass mode (SoC LDO output is 0.9 V) Switch-off on-chip Flash LDO	225 uA	265 uA	310 uA
3	External	In-package	External	Connect external BUCK output (1.45 V) to SoC LDO, and its output is 1.05 V Connect external 1.8 V supply to PSRAM, flash and IOs In deep sleep mode: Keep SoC LDO output to 0.9 V	75 uA	115 uA	160 uA

Options	Buck	SoC LDO	Flash LDO / PSRAM	Description	Estimated Deepsleep Current with PSRAM (for VBATT = 3.3 V)	Estimated DTIM-10 Standby Current with PSRAM (for VBATT = 3.3 V)	Estimated DTIM-3 Standby Current with PSRAM (for VBATT = 3.3 V)
4*	In-package	In-package	External with pull up on CS pin	VBATT to be connected to LC Buck input, LC Buck output is 1.45 V Connect external 1.8 V supply to PSRAM and IOs. Connect on-chip Flash LDO to in-package flash Connect weak pull up on external PSRAM CS pin In deep sleep mode: Switch off on-chip LC Buck, Flash LDO, and SoC LDO	40 uA + weak pull up current	80 uA+weak pull up current	125 uA +weak pull up current
Note: *Option4 is recommended to achieve minimum deep sleep currents while retaining the PSRAM contents.							

Options 1 through 4 are shown in the following diagrams. Different blocks shown in the diagrams have the following purposes:

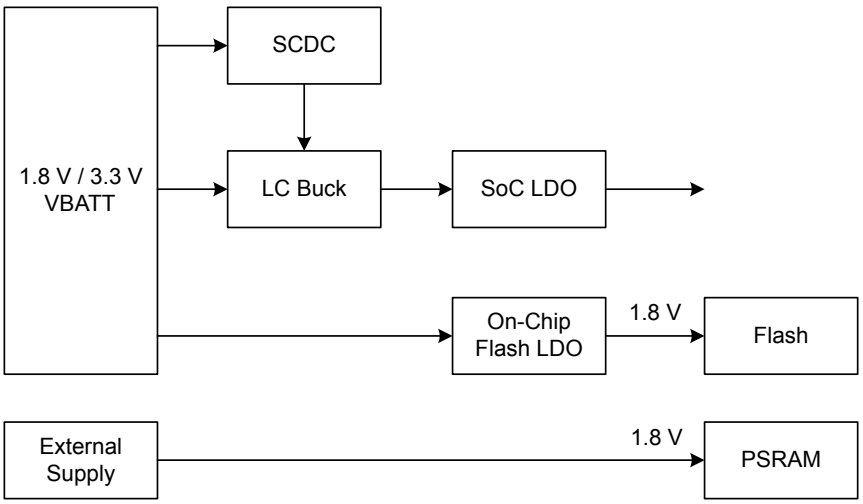
- VBATT - 3.3 V or 1.8 V input supply connected to UULP_VBATT_1, UULP_VBATT_2, and RF_VBATT supply pins.
- SCDC - This block generates a 1.05 V voltage rail which supplies the sleep state machine, always-ON domains and other internal digital blocks.
- SoC LDO - This block generates the supply voltage for many of the digital blocks on chip. Output varies based on power state.
- Flash LDO - This block generates a 1.8 V supply for in-package and/or external flash and PSRAM.
- LC Buck - This block generates a 1.45 V supply rail for RF circuits and the SoC LDO.

Option 1: All supplies are In-package



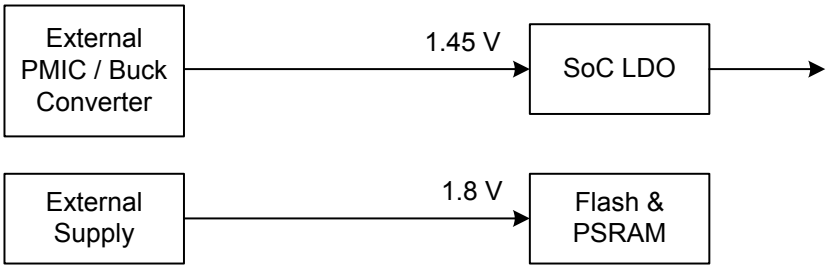
In this configuration, the on-chip LC Buck converter powers the SoC LDO, and the on-chip Flash LDO is used as a 1.8 V supply to both flash and PSRAM.

Option 2: PSRAM supply is External and other supplies are In-package



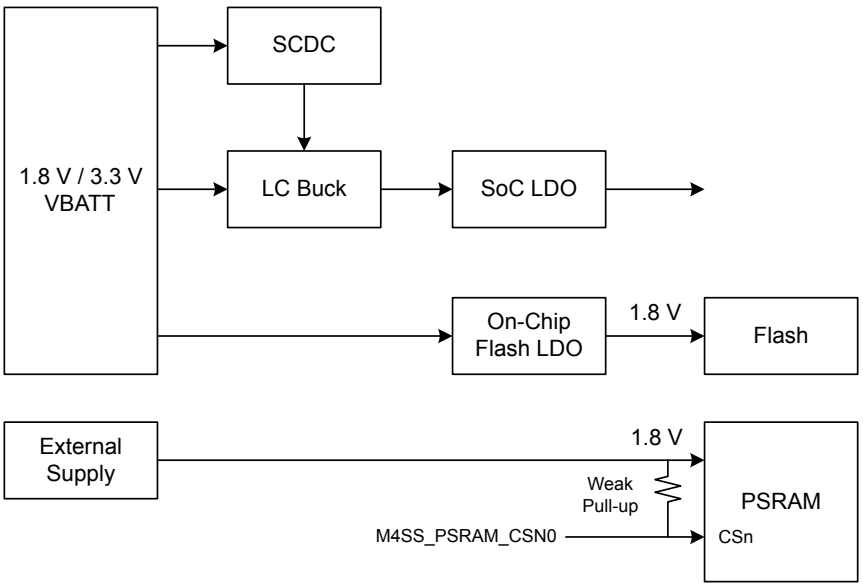
In this configuration, the on-chip LC Buck converter powers the SoC LDO, the on-chip Flash LDO is used as a 1.8 V supply to flash, and an external 1.8 V supply is connected to the PSRAM.

Option 3: External Buck and flash / PSRAM supplies



In this configuration, an external PMIC or Buck DCDC converter powers the SoC LDO,and an external 1.8 V supply is connected to flash and PSRAM.

Option 4: PSRAM supply is External with weak pull-up on CS pin and other supplies are on-chip



In this configuration, the on-chip LC Buck converter powers the SoC LDO, the on-chip Flash LDO is used as a 1.8 V supply to flash, and an external 1.8 V supply is connected to the PSRAM. Additionally the PSRAM chip select (CSn) has an external weak pull-up resistor to the supply.

5.6.1.21 Watchdog Timer

The WatchDog Timer is used to generate an interrupt on timeout and a reset in case of system failure which can be caused by an external event like ESD pulse or due to a software failure. Also the Interrupt can be used as a Wakeup source for transitioning from SLEEP/STANDBY to ACTIVE states.

- Independent watchdog timer.
- Interrupt is generated before the system reset is applied which can be used as a wakeup source.
- Generates reset upon Lockup indication from M4 processor.
- Configurable low frequency clock (RC and Xtal).
- Configurable timeout period.
- Able to operate when CPU is in SLEEP state during power-save applications
- Individually controllable power domain for low-power applications.

5.6.1.22 Calendar

Calendar block acts a RTC with time in seconds, minutes, hours, days, months, years and centuries. The real-time can also be read through APB with accuracy less than a second by reading the millisecond count value and further less also by reading the number of counts of APB clock in 1 millisecond of RTC clock. Accuracy is high.

- Calendar block can provide a seconds trigger and also a msec trigger.
- Calendar block takes care of no. of days in each month and also leap years. It can count up to 4 centuries.
- Real time is readable through APB and also programmable through APB.

5.6.1.23 General Purpose Timers

The MCU Timer block supports four 32 bit timers, which can be used to generate various timing events for the software. Each of the four timers can be independently programmed to work in periodic or one-shot mode and can be configured either as a microsecond timer or as a counter.

- Four independent 32 bit timers
- Supports per timer enable and disable.
- Option to configure each timer as a 32 bit counter or 32 bit microsecond timer.
- Supports 1 µs mode and 256 µs modes per timer.
- Accounts for integral and fractional value of the time units programmed.
- Microsecond timer supports two modes:
  - 1 microsecond mode: The time unit is 1 µs. Number of microseconds required to be counted has to be programmed.
  - 256 microsecond mode: The time unit is 256 µs. Number of 256 µs units required to be counted has to be programmed. This is useful when the timer is being used for counting large time values and microsecond based tracking not required.
- One shot and periodic modes per timer.
- Option to interrupt the M4 processor on timeout.

5.6.1.24 Secure Storage

The Block is used for storing configuration values with data protection feature.

- MCU has 3 set's for storage block
  - First chunk is 64 bits
  - Second chunk is 64 bits
  - Third Chunk is 128 bits
- Each chunk is a power domain.
- Secure mode is available for first and second Chunk.
- Storage space can be used for storing Configuration values

5.6.1.25 MVP

The Matrix Vector Processor (MVP) offloads floating point operations, particularly matrixed complex floating point multiplies and additions. The MVP was designed to offload the major computations of the Angle-of-Arrival (AoA) MUSIC algorithm, although the architecture can generally be used to offload other heavily floating-point computational problems such as Machine Learning (ML), Eigen, or BLAS acceleration.

- Instruction Set Architecture (ISA)
  - General purpose instruction set tailored towards algorithms built out of ALU, loop, and load/store instructions
  - Enables many high-level array functions, e.g.:
    - Matrix multiplication
    - Element-wise matrix multiplication
    - Matrix addition
    - Power series generation
    - Convolution
  - Program flexibility allows efficient iteration over N-dimensional array elements, including in-place processing of special matrix views:
    - Element-wise negate / conjugate
    - Transpose / adjoint / reverse
    - Matrix blocks (i.e., rectangular parts of matrix)
    - Matrix slices (i.e., taking rows, columns, or elements uniformly spaced within a matrix)
    - Row-major or column-major ordering
- Arithmetic Logic Unit (ALU)
  - Support for floating point real and complex numbers
    - Partial integer input support
      - Floating-point output operands, interpreted as 16-bit real or 32-bit complex number (16-bit real and 16-bit imaginary)
      - Register bank to hold all input/output operands
    - Includes 8 registers for temporary storage and/or accumulation
  - Hardware to support 1 complex floating point multiply-accumulate (MAC) per cycle
    - Four single-precision floating-point multipliers
    - Four single-precision floating-point adders
    - 6x performance of Cortex M33 FMAC operations
  - Operations supported at a rate of one operation per cycle:
    - Complex addition, multiplication, and MAC operations
    - Parallel real multiplication and MAC
    - Parallel real addition
    - Sum of 4 reals
    - Squared-magnitude of complex/real
    - Integer-to-float conversion
    - Conditional computation
  - Input transformations (per real/complex part of each input)
    - Negation (complex conjugate)
    - Zero-masking (real/imaginary part decomposition)
- Load/Store Unit (LSU)
  - Controls data streaming from memory-to-ALU and vice versa
  - Pipelined architecture to support two simultaneous 32-bit memory reads and one 32-bit memory write per cycle
  - Supports signed / unsigned 8-bit integer conversion for both load and store operations
  - Memory Access Ports
    - Used by load / store unit for handling accesses to external (system) memory addresses
    - Three independent 32-bit AHB manager ports for supporting 2 read channels and 1 write channel simultaneously
- Sequencer
  - Coordinates all MVP blocks to execute a sequence of instructions provided via the programming interface
  - Handles array iteration according to instruction sequence and static array configuration
  - Handles loop iteration according to instruction sequence and static loop configuration

- Programming interface
  - Control registers for starting / stopping engine
  - Status registers about ongoing and finished instruction sequences
    - Fault status
    - Useful information for debug
  - Breakpoint and stepping controls for debug
  - Interrupts and faults
    - Instruction sequence completion
    - Bus faults
    - Loop faults
    - Array faults
  - Array configuration registers
  - Loop configuration registers
  - Instruction queue registers
    - Array iteration
    - ALU operations
    - Looping

5.6.1.26 SYSRTC

The SYSRTC (System Real-Time Clock) is a highly configurable RTC capable of serving multiple cores. It contains up to 2 groups, where the number of capture and compare channels within each group is parametrized individually. Each group has its own interrupt and configuration registers. The main idea is to save power by letting all groups share a single counter.

- 32-bit counter
- 32 kHz / 1 kHz intended operation
- Low energy mode and wake-up
- Up to 2 groups
- 1-2 compare channels per group
- 0-1 capture channel per group
- Optional debug halting
- Optional alternate interrupt/wake-up per group
- Software Reset

5.6.2 Analog Peripherals and Interfaces

5.6.2.1 Analog to Digital Converter (ADC)

The ADC provides up to 12 bits of resolution at 2.5 Msps

- Programmable clock divider for ADC_CLK
- 12 bit ADC Output in 2's complement representation
- GPIOs in High Power mode for ADC Operation
  - Signal Ended Mode
    - 18 External configuration selection
    - 5 Internal configuration selection
      - Internal Temperature sensor
      - 3 Opamps Outputs
      - DAC output for internal reference
  - Differential Mode
    - 9 external differential mode configuration selection
    - 4 Internal configuration selection
      - 3 Opamps Outputs
      - DAC output for internal reference
- GPIOs in Low Power mode for ADC Operation
  - Signal Ended Mode
    - 12 External configuration selection.
  - Differential Mode
    - 6 external differential mode configuration selection
- 10 MHz to 32 kHz allowed ADC_CLK
- Configurable DMA to support 16 channels for storing AUXADC data in ULP SRAM
- Measurement range 0 to AUXADC_VREF (1.8 V to 3.3 V)

The ADC has five modes of operation:

- Single ended input with noise averaging
- Single ended input without noise averaging
- Differential input with noise averaging
- Differential input without noise averaging
- Shutdown mode

5.6.2.2 Digital to Analog Converter (DAC)

DAC can take 10 bit digital inputs and convert them into analog voltage within range 5*vdd/36 to 31*vdd/36. Vdd can vary from 1.8 volts to 3.63 volts.

- 10-bit resolution
- Single ended DAC
- Max sampling frequency is 2.5 MHz for DAC_CLK
- Supports Operational mode and Shutdown modes

5.6.2.3 OPAMP

- 3 general purpose Operational Amplifiers (OPAMP) offering rail-to-rail inputs and outputs.
- Each of the three opamps has 2 inputs (inp, inn) and 1 output.
- opamps can take inputs from GPIOs and their outputs can be seen on GPIOs
- configured in either low power mode or high power mode
- opamps can be configured as:
  - Unity gain amplifier
  - Trans-Impedance Amplifier(TIA)
  - Non-inverting Programmable Gain Amplifier (PGA)
  - Inverting Programmable Gain Amplifier
  - Non-inverting Programmable hysteresis comparator
  - Inverting Programmable hysteresis comparator
  - Cascaded Non-Inverting PGA
  - Cascaded Inverting PGA
  - Two opamps Differential Amplifier
  - Instrumentation Amplifier

5.6.2.4 Analog Comparators

Analog comparators peripheral consists of two analog comparators, a reference buffer, a scaler and a resistor bank. Both comparators can take inputs from GPIOs.

The comparator compares analog inputs p and n to produce a digital output, cmp_out according to:

p > n, cmp_out = 1

p < n, cmp_out = 0

The following cases of comparison are possible

- Compare external pin inputs
- Compare external pin input to internal voltages.
- Compare internal voltages.

The inputs of 2 comparators can be programmed independently. The reference buffer, scaler and resistor bank are shared between the two comparators and can be enabled only when at least one of the comparators is enabled.

5.6.2.5 Temperature Sensor

An BJT based temperature sensor is included on the device.

The BJT based sensor works for a temperature range from -40 °C to 125 °C across the supply range 1.8 V to 3.63 V. It outputs a digital word with a resolution of nearly 1 degree C. The conversion time is 2 clock cycles of ADC after turning ON the temperature sensor.

The temperature reading of the sensor is accessed by configuring the ADC inputs to temperature sensor.

5.7 Bootloader

The Bootloader controls the initial operation of the device after any form of reset. The Bootloader supports Flash programming and initial startup of the application code. Bootloader supports following features:

- Two Bootloaders - Security Bootloader and Application Bootloader
- Support for ISP (In-System Programming) through multiple interfaces - UART, HSPI and SDIO
- Auto-detection of ISP interface. The host interfaces are the external peripheral interfaces over which Bootloader can receive commands or firmware when in ISP mode. The Bootloader supports UART, HSPI and SDIO interfaces. Bootloader in ISP mode waits for data on any of these interfaces and can automatically detect which interface the data is being received.
- Support for secure boot
- Support for secure firmware upgrade using PUF based Roots-of-Trust (RoT)
- Anti-rollback protection. This feature prevents the firmware version from being downgraded. A new firmware is allowed to be upgraded only if it is be equal to or greater than the current firmware.
- Secure Key Management and Protection
- Support for different flash protection levels and write-protected Flash
- Encrypted XIP from Flash
- Fail-proof migration of current active firmware to new (update) firmware
- Public key cryptography (digital signature) based authentication

The SiWx91x includes two Bootloaders - Security Bootloader and Application Bootloader. The Security Bootloader runs on the Network Wireless Processor and the Application Bootloader runs on the Cortex M4 processor. On any reset, execution will always start in Security Bootloader, which is responsible for all security features, ISP and firmware upgrades. Once the Security Bootloader finishes its tasks, it enables the Application Bootloader. The Application bootloader will load and execute the application and also execute wakeup sequence on wakeup from sleep.

The following are the sources, which can trigger the Bootloader:

- Primary reset (RESET_N)
- Power on reset (POC_IN)
- Watchdog reset
- Black out monitor
- Reset request through SYSRESETREQn bit in the Cortex-M4 processor
- Wake-up from Sleep

5.8 Security

5.8.1 Security Features

- Secure Boot
- Secure OTA Firmware update
- TRNG: Generates high-entropy random numbers based on RF noise, increasing the effort/time needed to expose secret keys
- Secure Zone
- Secure Key storage : HW device identity and key storage with PUF
- Debug Lock
- Anti Rollback : Firmware downgrade to a lower version is prohibited through OTP to prevent the use of older, potentially vulnerable FW version
- Encrypted XIP from flash with XTS/CTR mode
- Secure Attestation : Allows a device to authenticate its identity using a cryptographically signed token and exchange of secret keys
- Hardware Accelerators: AES128/256/192, SHA256/384/512, HMAC, RNG, CRC, SHA3, AES-GCM/ CMAC, ChaCha-poly
- Software Implementation: RSA and ECC

5.8.2 Secure Boot

Key Features

- Ensures the device runs authentic code in the boot and OTA update to eliminate malware insertion threats
- Secure Immutable Bootloader in ROM.
- Authenticates signatures of all other SW using public keys.
- NWP and M4 flash images can be encrypted with separate keys.

On reset, the Security Bootloader configures the hardware based on the configuration present in the eFuse. It also passes the required information from the eFuse to the Application Bootloader. The Security Bootloader validates the integrity and authenticity of the firmware in the Flash and invokes the Application Bootloader. It detects and prevents execution of unauthorized software during the boot sequence. The Bootloader uses public & private key based digital signatures to recognize authentic software. The Bootloader provides 3 flash protection levels which can used to secure different sections of the Flash for different purposes:

- Protection level 1: Stored at manufacturing, not allowed to modify by the Security Bootloader
- Protection level 2: Allowed to modify by the Bootloader only, usually used to maintain secure information used/consumed by Bootloader
- Protection level 3: Allowed to modify by the Bootloader only, usually used to maintain protected firmware images. (Minimum 8 MB of flash is required for complete NWP image protection. For 4 MB flash OPNs, only partial protection is available for NWP image).

The protection levels are written to Flash during the manufacturing process. The write-protection feature prevents the application program from changing the Flash protection levels.

The Security configurations can be enabled or disabled during the manufacturing process.

5.8.3 Encrypted XiP

The Security Bootloader provides provision for inline execution (XIP) of encrypted firmware from flash.

- Execute SW directly from flash instead of copying it into RAM
- Images are saved in encrypted format and decrypted using device-specific PUF intrinsic keys while executing
- In-line decryption based on-the-fly AES engine (based on PUF keys)
- XTS/CTR modes supported

5.8.4 Secure Firmware Upgrade

Secure firmware upgrade via host interface :

The secure firmware upgrade feature of the Bootloader checks the authenticity of the new firmware image along with its integrity. The Bootloader automatically detects the host interface in use and configures the host interface hardware accordingly. The Bootloader updates the image only after successfully validating the authenticity and integrity of the image. It prevents downgrade to a lower version of firmware using the anti-rollback feature, if it is enabled. The Bootloader also supports transparent migration to a wirelessly updated image and protection against failures by providing recovery mechanisms.

Secure OTA :

- Secure OTA update to eliminate malware insertion threats.
- Wireless and Application image transfer over the air.
- Network Wireless Processor authenticates the signatures of OTA image using public keys
- Bootloader copies the OTA image to primary firmware location upon successful authentication .

5.8.5 Secure Zone

Secure Zone Key Features

- Secure Zone is a hardware enforced isolation between the NWP core from the Application (M4) core.
- No access to the:
  - NWP processor
  - NWP address space memory (except misc-registers that are used for bootloader command exchanges)
  - NWP HW registers from external peripherals and host interfaces
- Secure zone protects NWP internal keys (for example, secure boot keys), customer application keys, and certificates residing in the NWP by restricting direct access from the application M4 core.
- Secure zone can be enabled during the manufacturing process, at the user's discretion, by setting the secure_isolation_enabled OTP/MBR bit.

When Secure Zone is enabled, the Host Processor cannot reconfigure interfaces that are controlled by the NWP by default. For instance, ISP interfaces such as UART, HSPI, and SDIO will be mutually exclusive between the NWP and M4 when secure zone is enabled. This is because secure zone will not allow Host processor to program the registers (in NWP space) to get control of those interfaces. In such cases, configurations in MBR defines the default ownership of the interface.

5.8.6 In-System Programming (ISP)

In System Programming (ISP) is programming or reprogramming of the flash through a boot loader using UART (GPIO_8 and GPIO_9), HSPI (GPIO_25 to GPIO_29), or SDIO (GPIO_25 to GPIO_30) interfaces. This can be done after the part is integrated on the end-user board. The boot loader can be requested to boot in ISP mode by pulling down the JTAG_TDO_SWO pin. This pin has to be left unconnected during reset for the boot loader to bypass ISP and execute the code that is present in flash. ISP mode can be used to reprogram the flash, if the application code uses JTAG pins for functional use. On boot up, if the application code goes into a state where the JTAG interface is not functioning, ISP mode can be used to gain control and to reprogram the flash.

5.8.7 Debug Lock

Key Features

- Debug ports are disabled in HW by default.
- It can be enabled in SW using cryptographically secure host interface commands validated by immutable bootloader
- It allows the device's JTAG ports to be locked and unlocked.

5.9 Debug Support

MCU implements complete hardware debug solution. This provides high system visibility of the M4 processor and memory through either a traditional JTAG port or a 2-pin Serial Wire Debug (SWD) port that is ideal for microcontrollers and other small package devices.

In Serial Wire Viewer (SWV) mode, a one-bit serial protocol is used and this reduces the number of output signal to one. When combining SWV with Serial-Wire debug protocol, the Text Data Output (TDO) pin normally used for Joint Test Action Group (JTAG) protocol can be shared with SWV.

The Embedded Trace Macrocell (ETM) provides high bandwidth instruction trace via four dedicated trace. The MCU_CLK_OUT frequency must be in the range of 40 MHz to 90 MHz to Instruction trace using ETM component.

5.10 WLAN

- Compliant to single-spatial stream IEEE 802.11 b/g/n/ax with single band (2.4 GHz) support
- Support for 20 MHz channel bandwidth for 802.11n and 802.11ax.
- Operating Modes: Wi-Fi 4 STA, Wi-Fi 6 (802.11ax) STA, Wi-Fi 4 AP, Enterprise STA, Wi-Fi 6 STA + Wi-Fi 4 AP, Wi-Fi STA + BLE
- Wi-Fi 6 Features: Individual Target wake-up time (iTWT), Broadcast TWT (bTWT),SU extended range (ER), DCM (Dual Carrier Modulation), DL MU-MIMO, DL/UL OFDMA, MBSSID, BFRP, Spatial Reuse, BSS Coloring, and NDP feedback up to 4 antennas
- Integrated PA
- Data Rates—802.11b: up to 11 Mbps; 802.11g: up to 54 Mbps; 802.11n: MCS0 to MCS7; 802.11ax: MCS0 to MCS7
- Operating Frequency Range: 2412 MHz – 2484 MHz

5.10.1 MAC

- Conforms to IEEE 802.11b/g/n/j/ax standards for MAC
- Hardware accelerators for AES
- WPA, WPA2, WPA3 and WMM support
- AMPDU aggregation for high performance
- Firmware downloaded from host based on application
- Hardware accelerators for DH (for WPS) and ECDH

5.10.2 Baseband Processing

- Supports 11b: DSSS for 1, 2 Mbps and CCK for 5.5, 11 Mbps
- Supports all OFDM data rates
  - 802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps
  - 802.11ax, 802.11n: MCS 0 to MCS 7
- High-performance multipath handling in OFDM, DSSS, and CCK modes

5.11 Bluetooth

Key Features

- Transmit power up to +19 dBm with integrated PA
- Receive sensitivity — LE 1 Mbps: -96 dBm, LR 125 kbps: -107 dBm
- Operating Frequency Range — 2.402 GHz - 2.480 GHz
- Support LE (1 Mbps & 2 Mbps) and LR (125 kbps & 500 kbps) rates
- Advertising extensions
- Data length extensions
- LL privacy
- LE dual role
- BLE acceptlist
- 10 simultaneous BLE Connections (8 Peripheral & 2 Central)
- BLE Mesh (4 nodes) for limited switch use case.

5.11.1 MAC

Link Manager

- Creation, modification & release of physical links
- Connection establishment between Link managers of two Bluetooth devices
- Link supervision is implemented in Link Manager
- Link power control is done depending on the inputs from Link Controller
- Enabling & disabling of encryption & decryption on logical links
- AES hardware acceleration

Link Controller

- Encodes and decodes header of BLE packets
- Manages flow control, acknowledgment, re-transmission requests, etc.
- Stores the last packet status for all physical transports
- Indicates the success status of packet transmission to upper layers
- Indicates the link quality to the LMP layer

Device Manager

- Executes HCI Commands
- Controls Scan & Connection processes
- Controls all BLE Device operations except data transport operations
- BLE Controller state transition management
- Anchor point synchronization & management
- Scheduler

5.11.2 Baseband Processing

- Supports BLE 1 Mbps, 2 Mbps and long range 125 kbps, 500 kbps

5.12 RF Transceiver

- SiWG917 features two highly configurable RF transceivers supporting WLAN 11b/g/n/ax and Bluetooth LE wireless protocols. Both RF transceivers operate together in multiple modes covering High Performance (HP) and Low Power (LP) operations. List of operating modes are given in next section.
- It contains two fully integrated fractional-N frequency synthesizers having reference from internal oscillator with 40 MHz crystal. One of the synthesizer is a low power architecture which also caters single-bit data modulation feature for Bluetooth LE protocols.
- There are two transmitter chains in the chip. First one uses a direct conversion architecture getting carrier signal from the high-performance frequency synthesizer. It contains an on-chip balun and its output is terminated as single-ended output at “RF_TX” pin. This transmitter supports all the mentioned WLAN protocols, and Bluetooth LE protocol for high output power. The second transmitter is a low power architecture for supporting constant envelope modulation formats. This has two outputs differentiated by their maximum output power level. The 0 dBm output is shared with “RF_RX” pin and the 8 dBm output is terminated at “RF_BLETX” pin.
- The receiver contains two front end paths with a configurable common LNA catering HP and LP operations. This also has two analog base band blocks where one is zero-IF architecture supporting all the mentioned WLAN protocols and the other one is low-IF architecture supporting Bluetooth LE. Input to the pin is “RF_RX” sharing with 0 dBm Tx output.
- Impedance matching for each RF pin needs to be done separately for optimum performance.

5.12.1 Receiver and Transmitter Operating Modes

The available radio operating modes are

- WLAN HP TX - WLAN High-Performance Transmitter with up to 19.5 dBm PA
- WLAN HP RX - WLAN High-Performance Receiver
- WLAN LP RX - WLAN Low-Power Receiver
- BLE HP TX - Bluetooth LE High-Performance Transmitter with up to 19 dBm PA
- BLE HP RX - Bluetooth LE High-Performance Receiver
- BLE LP TX - Bluetooth LE Low-Power Transmitter with 8 dBm PA
- BLE LP TX - Bluetooth LE Low-Power Transmitter with 0 dBm PA
- BLE LP RX - Bluetooth LE Low-Power Receiver

Note: All the TX / RX modes are automatically controlled by radio firmware and not individually selectable.

5.13 Host Interface Peripherals

Three host interfaces are supported:

- SDIO
  - Version 2.0-compatible
  - Supports SD-SPI
  - 1-bit, and 4-bit SDIO modes
  - Operation up to a maximum clock speed of 50 MHz
- HSPI
  - Operation up to a maximum clock speed of 100 MHz
- UART
  - Supports various baud rates up to 921600 bps. Baud rates above 115200 bps require Hardware Flow control.

The Host Interface Peripherals are shared between NWP and M4 sub-systems. In SiWG917, these peripherals can be used by NWP in ISP mode only, whereas M4 can use these in non-ISP mode only.

5.13.1 Auto Host Detection

The SiWG917 detects the host interface automatically after connecting to respective host controllers like SDIO, HSPI, UART. The SDIO / HSPI host interface is detected through hardware packet exchanges. The UART host interface is detected through the software based on received packets on the UART interface. This Host configuration is stored in always-on domain registers after detection (on power up) and the information is reused at each NWP wakeup.

5.14 Embedded Wi-Fi Software

- The wireless software package supports Embedded Wi-Fi (802.11 b/g/n/ax) Client mode, Wi-Fi Access point mode (up to 4 clients), and Enterprise Security in client mode.
- The software package includes complete firmware and application profiles.
- It has a wireless coexistence manager to arbitrate between protocols.

5.14.1 Security

Wireless software supports multiple levels of security capabilities available for the development of IoT devices.

- Accelerators: AES128/256
- WPA/WPA2/WPA3-Personal, WPA/WPA2/WPA3 Enterprise for Client

5.15 Low Power Modes

It supports Ultra-low power consumption with multiple power modes to reduce system energy consumption.

- Voltage and Frequency Scaling
- Deep sleep (ULP) mode with only the sleep timer active – with and without RAM retention
- Wi-Fi standby associated mode with automatic periodic wake-up
- Automatic clock gating of the unused blocks or transit the system from Normal to ULP mode.

5.15.1 ULP Mode

In Ultra Low Power mode, the deep sleep manager has control over the other subsystems and M4 processors and controls their active and sleep states. During deep sleep, the always-on logic domain operates on a lowered supply and a low-frequency clock to reduce power consumption. The ULP mode supports the following wake-up options:

- Timeout wakeup - Exit sleep state after programmed timeout value.
- GPIO Based Wakeup: Exit sleep state when GPIO goes High/Low based on programmed polarity.
- Analog Comparator Based wakeup - Exit sleep state on an event at the analog comparator.
- RTC Timer wakeup - Exit Sleep state on timeout of RTC timer
- WatchDog Interrupt based wakeup - Exit Sleep state upon watchdog interrupt timeout.

5.16 Wireless Subsystem Memory

5.16.1 On-Chip Memory

The Network Wireless Processor has the following memory:

- On-chip SRAM of 480/416/352 KB based on chip configuration
- 448 KB of ROM which holds the Secure primary bootloader, Network Stack, Wireless stacks and security functions
- 16 KB of Instruction cache enabling eXecute In Place (XIP) with quad SPI flash memory.
- eFuse of 1024 bytes (used to store primary boot configuration, security and calibration parameters)

The following memory configuration between MCU and Wireless Sub-system are possible:

Table 5.11. Possible Memory Configurations between MCU and Wireless Sub-system

No.	MCU memory size	Wireless Subsystem memory size	Note
1.	320 KB	352 KB	PS4, PS3, and PS2 power states possible
2.	256 KB	416 KB	Only PS4 and PS3 power state possible For MCU RAM retention, MCU needs to retain complete 320 KB
3.	192 KB	480 KB	Only PS4 and PS3 power state possible For MCU RAM retention, MCU needs to retain complete 320 KB

5.17 Pad Configuration

There are multiple processor sub-systems containing SZP (Secure Zone Processor), MCU HP (High Performance) and MCU ULP (Ultra Low Power) which share these common set of GPIO pads. These GPIO pads are controllable by either SZP, MCU HP or MCU ULP. PAD selection register has to be programmed to control the PAD behavior for each GPIO. The SZP and MCU HPGPIOs are available only in PS4/PS3 power states whereas MCU ULP GPIOs are available in all the power states except sleep modes. The UULP Vbat GPIOs are available in all power states.

The SZP, MCU HP and MCU ULP GPIOs PAD are programmable, multi-voltage (1.8 V, 3.3 V) general purpose, bi-directional I/O buffer with a selectable LVCMOS (Low Voltage CMOS) input or LVCMOS Schmitt trigger input and programmable pull-up/pull-down. In the full-drive mode, this buffer can operate in excess of 100 MHz frequency with 15 pF external load and 125 MHz with 10 pF load, but actual frequency is load and system dependent. A maximum of 200 MHz can be achieved under small capacitive loads.

The following PAD configurations can be controlled by software for SZP, MCU HP and MCU ULP GPIOs.

- Bi-directional IO capability
- Multi-voltage DVDD capability (1.8 V, 3.3 V)
- Power-on-Start (POS) capable
- Optimized for EMC (low di/dt switching supply noise) with SSO (Simultaneous Switching Output) factor of 8
- Four (4) Programmable output drive strengths (rated 2 mA, 4 mA, 8 mA, and 12 mA)
- Selectable output slew-rate (slow / fast)
- Open drain output mode (Logic low or high on input and use OEN as data input)
- LVCMOS/LVTTL compatible input with selectable hysteresis
- Programmable input options (pull-up, pull-down, repeater, or plain input)
- No power sequence requirements, I/Os are tri-stated when core power is not valid (POC control). These are tri-stated even if the system is under reset or in the deep sleep power state.

The following PAD configurations can be controlled by software for UULP Vbat GPIOs.

- Bi-directional IO capability
- Multi-voltage DVDD capability (1.8 V, 3.3 V)

5.18 Interrupts

- Nested vectored interrupt controller (NVIC) for interrupts handling
- Supports 99 interrupts
- Flexible exception and interrupt management
- Nested exception/interrupt support
- Vectored exception/interrupt entry
- Interrupt configurations, prioritization, and interrupt masking

6. Pinout and Pin Description

6.1 Pin Diagram

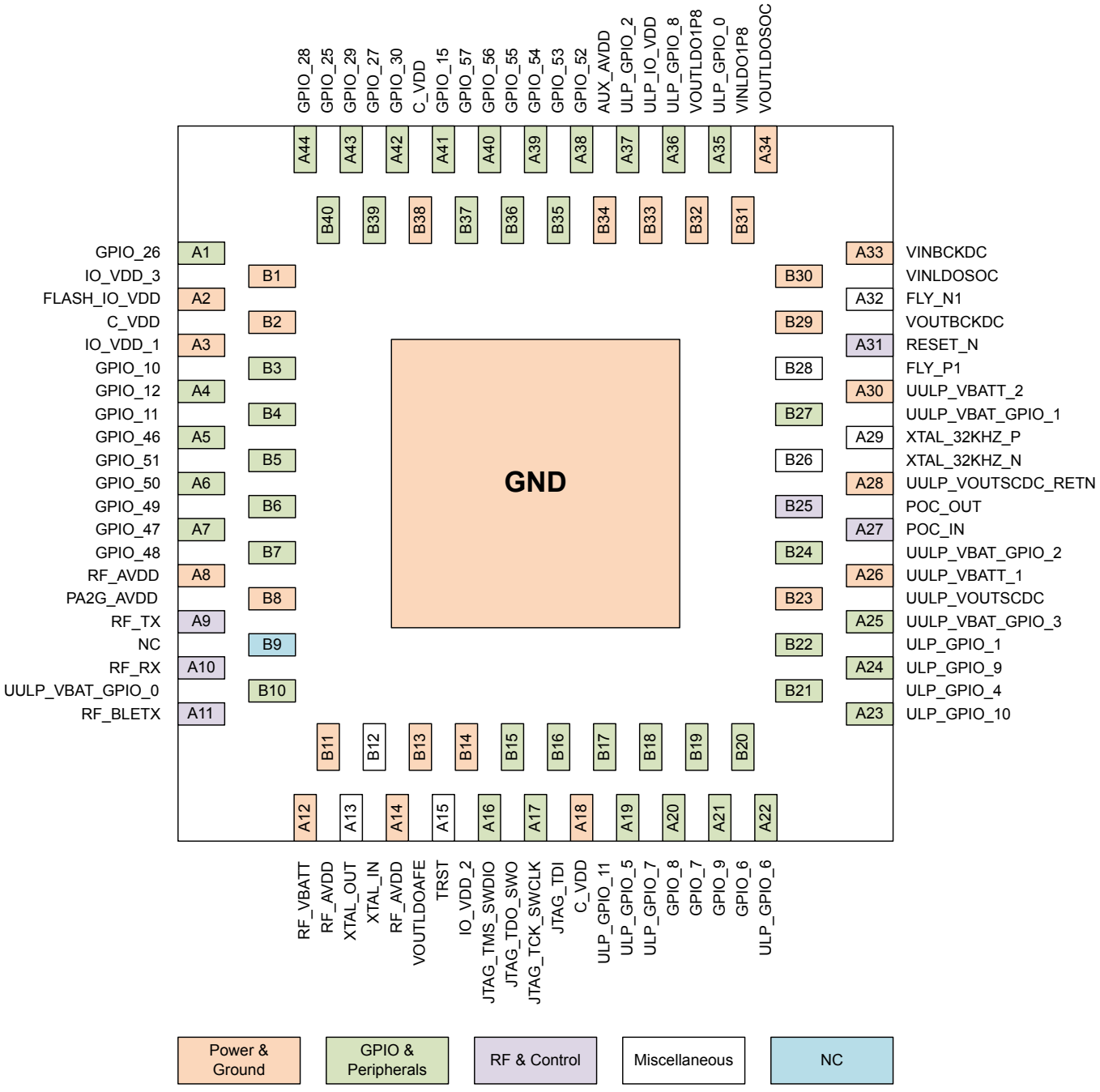


Figure 6.1. SiWx917xxxxxxxBA

6.2 Pin Description

6.2.1 RF and Control Interfaces

Table 6.1. Chip Packages - RF and Control Interfaces

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description
RF_TX	A9	PA2G_AVDD	Output	NA	2.4 GHz High Performance RF Output.
RF_RX	A10	RF_AVDD	Inout	NA	2.4 GHz RF Input for both High Performance and Low Power WLAN and BLE. It can also be used as 2.4 GHz RF output for BLE Low Power 0 dBm RF chain.
RF_BLETX	A11	RF_AVDD	Output	NA	2.4 GHz RF Output for Low Power BLE 8 dBm.
RESET_N	A31	UULP_VBATT_2	Inout	NA	Active-low asynchronous reset signal, which resets only digital blocks. RESET_N will be pulled low if POC_IN is low.
POC_IN	A27	UULP_VBATT_1	Input	NA	This is an input to the chip which resets all analog and digital blocks in the device. It should be made high only after supplies are valid to ensure the IC is in safe state until valid power supply is available.
POC_OUT	B25	UULP_VBATT_1	Output	NA	This is internally generated. Initially, it is low. But it becomes high when the supplies (UULP_VBATT_1, UULP_VOUTSCDC) are valid.
ULP_GPIO_0	A35	ULP_IO_VDD	Inout	NA	Antenna select pin for External switch configuration. Please refer to Reference schematics for more info. For internal RF switch configuration, may be used for GPIO functions.
ULP_GPIO_4	B21	ULP_IO_VDD	Inout	NA	Antenna select pin for External switch configuration. Please refer to Reference schematics for more info. For internal RF switch configuration, may be used for GPIO functions.
ULP_GPIO_5	A19	ULP_IO_VDD	Inout	NA	Antenna select pin for External switch configuration. Please refer to Reference schematics for more info. For internal RF switch configuration, may be used for GPIO functions.

6.2.2 Power and Ground Pins

Table 6.2. Chip Packages - Power and Ground Pins

Pin Name	Type	Pin Number	Direction	Description
UULP_VBATT_1	Power	A26	Input	Always-on VBATT Power supply to the UULP domains.
UULP_VBATT_2	Power	A30	Input	Always-on VBATT Power supply to the UULP domains.
RF_VBATT	Power	A12	Input	Always-on VBATT Power supply to the RF.
VINBCKDC	Power	A33	Input	Power supply for the on-chip buck DC-DC.
VOUTBCKDC	Power	B29	Output	Output of the on-chip buck DC-DC.
VINLDOSOC	Power	B30	Input	Power supply for SoC LDO. Connect to VOUTBCKDC as per the Reference Schematics.
VOUTLDOSOC	Power	A34	Output	Output of SoC LDO.
VINLDO1P8	Power	B31	Input	Power supply for 1.8 V LDO
VOUTLDO1P8	Power	B32	Output	Output of 1.8 V LDO.
VOUTLDOAFE	Power	B13	Output	Output of RF AFE LDO.
FLASH_IO_VDD	Power	A2	Input	I/O Supply for In-Package Flash/PSRAM. Connect to VOUTLDO1P8 as per the Reference Schematics.
IO_VDD_1	Power	A3	Input	I/O Supply for GPIOs. Refer to the GPIOs section for details on which GPIOs have this as the I/O supply.
IO_VDD_2	Power	B14	Input	I/O Supply for GPIOs. Refer to the GPIOs section for details on which GPIOs have this as the I/O supply.
IO_VDD_3 (SDIO_IO_VDD)	Power	B1	Input	I/O Supply for SDIO I/Os. Refer to the GPIOs section for details on which GPIOs have this as the I/O supply.
ULP_IO_VDD	Power	B33	Input	I/O Supply for ULP GPIOs.
PA2G_AVDD	Power	B8	Input	Power supply for the 2.4 GHz RF Power Amplifier.
RF_AVDD	Power	A8, A14, B11	Input	Power supply for the 2.4 GHz RF and AFE. Connect to VOUTBCKDC as per the Reference Schematics.
AUX_AVDD	Power	B34	Output	Auxiliary LDO Output supply for the Analog peripherals.
UULP_VOUTSCDC	Power	B23	Output	UULP Switched Cap DCDC Output.
UULP_VOUTSCDC_RETN	Power	A28	Output	UULP Retention Supply Output.
C_VDD	Power	B2, A18, B38	Input	Power supply for the digital core. Connect to the VOUTLDOSOC as per the Reference Schematics.
GND	Ground	GND Paddle	GND	Common ground pins.

6.2.3 Peripheral Interfaces

Table 6.3. Chip Packages - Peripheral Interfaces

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)		Description [1,2,3,4,5]
GPIO_6 / NWP_UART2_TX [6]	B20	IO_VDD_1	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Refer to GPIO Muxing Tables for configuration. **NWP**: UART2_TX For configuration refer to Boot Configuration Feature Bitmaps / Extended Custom Feature Bitmap of API Reference Guide
GPIO_7	B19	IO_VDD_1	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ **PTA_GRANT**: "PTA Grant" output signal is part of 3-wire coexistence (Packet Traffic Arbitration) interface. If PTA feature is enabled, use it as PTA_GRANT. If PTA feature is not enabled, refer to GPIO Muxing Tables for configuration.
GPIO_8 / ISP_UART_RX[7] / NWP_UART1_RX	A20	IO_VDD_1	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ **ISP**: UART_RX If ISP is not enabled, refer to GPIO Muxing Tables for configuration **NWP**: UART1_RX For configuration refer to Boot Configuration Feature Bitmaps / Extended Custom Feature Bitmap of API Reference Guide
GPIO_9 / ISP_UART_TX[7] / NWP_UART1_TX[6]	A21	IO_VDD_1	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ **ISP**: UART_TX If ISP is not enabled, refer to GPIO Muxing Tables for configuration **NWP**: UART1_TX For configuration refer to Boot Configuration Feature Bitmaps / Extended Custom Feature Bitmap of API Reference Guide

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)		Description [1,2,3,4,5]
GPIO_10 / NWP_UART2_RX	B3	IO_VDD_1	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Refer to GPIO Muxing Tables for configuration. **NWP**: UART2_RX For configuration refer to Boot Configuration Feature Bitmaps / Extended Custom Feature Bitmap of API Reference Guide
GPIO_11	B4	IO_VDD_1	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_12	A4	IO_VDD_1	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_15	A41	IO_VDD_3	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_25 / SDIO_CLK[7] / HSPI_CLK[7]	B40	IO_VDD_3	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ **ISP**: SDIO_CLK or HSPI_CLK If ISP is not enabled, refer to GPIO Muxing Tables for configuration
GPIO_26 / SDIO_CMD[7] / HSPI_CSN[7]	A1	IO_VDD_3	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ **ISP**: SDIO_CMD or HSPI_CSN If ISP is not enabled, refer to GPIO Muxing Tables for configuration
GPIO_27 / SDIO_D0[7] / HSPI_MOSI[7]	B39	IO_VDD_3	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ **ISP**: SDIO_D0 or HSPI_MOSI If ISP is not enabled, refer to GPIO Muxing Tables for configuration

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)		Description [1,2,3,4,5]
GPIO_28 / SDIO_D1[7] / HSPI_MISO[7]	A44	IO_VDD_3	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ **ISP**: SDIO_D1 or HSPI_MISO If ISP is not enabled, refer to GPIO Muxing Tables for configuration
GPIO_29 / SDIO_D2[7] / HSPI_INTR[7]	A43	IO_VDD_3	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ **ISP**: SDIO_D2 or HSPI_INTR If ISP is not enabled, refer to GPIO Muxing Tables for configuration
GPIO_30 / SDIO_D3[7]	A42	IO_VDD_3	Inout	Pullup		**Default**: High **Sleep**: HighZ **ISP**: SDIO_D3 If ISP is not enabled, refer to GPIO Muxing Tables for configuration
GPIO_46	A5	IO_VDD_1	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_47	A7	IO_VDD_1	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_48	B7	IO_VDD_1	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_49	B6	IO_VDD_1	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_50	A6	IO_VDD_1	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Refer to GPIO Muxing Tables for configuration.

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)		Description [1,2,3,4,5]
GPIO_51	B5	IO_VDD_1	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_52	A38	IO_VDD_1	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Refer to GPIO Muxing Tables for configuration
GPIO_53	B35	IO_VDD_1	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Refer to GPIO Muxing Tables for configuration
GPIO_54	A39	IO_VDD_1	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Refer to GPIO Muxing Tables for configuration
GPIO_55	B36	IO_VDD_1	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Refer to GPIO Muxing Tables for configuration
GPIO_56	A40	IO_VDD_1	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Refer to GPIO Muxing Tables for configuration
GPIO_57	B37	IO_VDD_1	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Refer to GPIO Muxing Tables for configuration
ULP_GPIO_0	A35	ULP_IO_VDD	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Antenna select pin for external switch configuration. Please refer to reference schematics for more info. For internal RF switch configuration, may be used for GPIO functions.

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)		Description [1,2,3,4,5]
ULP_GPIO_1	B22	ULP_IO_VDD	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ PTA_REQ: "PTA Request" input signal is part of 3-wire coexistence (Packet Traffic Arbitration) interface. If PTA feature is enabled, use it as PTA_REQ. If PTA feature is not enabled, refer to GPIO Muxing Tables for configuration.
ULP_GPIO_2	A37	ULP_IO_VDD	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Refer to GPIO Muxing Tables for configuration
ULP_GPIO_4	B21	ULP_IO_VDD	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Antenna select pin for external switch configuration. Please refer to reference schematics for more info. For internal RF switch configuration, may be used for GPIO functions.
ULP_GPIO_5	A19	ULP_IO_VDD	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Antenna select pin for external switch configuration. Please refer to reference schematics for more info. For internal RF switch configuration, may be used for GPIO functions.
ULP_GPIO_6	A22	ULP_IO_VDD	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ PTA_PRIO: "PTA Priority" input signal is part of 3-wire coexistence (Packet Traffic Arbitration) interface. If PTA feature is enabled, use it as PTA_PRIO. If PTA feature is not enabled, refer to GPIO Muxing Tables for configuration.
ULP_GPIO_7	B18	ULP_IO_VDD	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Refer to GPIO Muxing Tables for configuration
ULP_GPIO_8	A36	ULP_IO_VDD	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Refer to GPIO Muxing Tables for configuration

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)		Description [1,2,3,4,5]
ULP_GPIO_9 / NWP_UART2_TX[6]	A24	ULP_IO_VDD	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Refer to GPIO Muxing Tables for configuration **NWP**: UART2_TX For configuration refer to Boot Configuration Feature Bitmaps / Configuration Feature Bitmap of API Reference Guide
ULP_GPIO_10	A23	ULP_IO_VDD	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Refer to GPIO Muxing Tables for configuration
ULP_GPIO_11	B17	ULP_IO_VDD	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Refer to GPIO Muxing Tables for configuration
UULP_VBAT_GPIO_0	B10	UULP_VBATT_1	Output	High		**Default:** High **Sleep:** High Refer to GPIO Muxing Tables for configuration
UULP_VBAT_GPIO_1	B27	UULP_VBATT_1	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Refer to GPIO Muxing Tables for configuration
UULP_VBAT_GPIO_2	B24	UULP_VBATT_1	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Refer to GPIO Muxing Tables for configuration
UULP_VBAT_GPIO_3	A25	UULP_VBATT_1	Inout	HighZ		**Default**: HighZ **Sleep**: HighZ Refer to GPIO Muxing Tables for configuration
JTAG_TCK_SWCLK	A17	IO_VDD_2	Input	Pullup		JTAG interface clock or serial wire clock. Connect to a test point for debugging purposes.
JTAG_TDI	B16	IO_VDD_2	Input	Pullup		JTAG interface input data. Connect to a test point for debugging purposes.

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)		Description [1,2,3,4,5]
JTAG_TMS_SWDIO	A16	IO_VDD_2	Input	Pullup		JTAG interface Test Mode Select signal. Bi-directional data pin for SWD Interface. Connect to a test point for debugging purposes.
JTAG_TDO_SWO	B15	IO_VDD_2	Output	Pullup		JTAG interface output data. Serial wire output for SWD Interface. This pin can also be used as ISP_ENABLE. Pull down to enable ISP mode. In System Programming (ISP) is programming or reprogramming of the flash through boot loader using UART (GPIO_8, GPIO_9), HSPI (GPIO_25 to GPIO_28) and SDIO (GPIO_25 to GPIO_30) interfaces. This can be done after the part is integrated on end user board. Boot loader can be requested to boot in ISP mode by pulling down JTAG_TDO_SWO pin. This pin has to be left unconnected during reset for the boot loader to bypass ISP and execute the code that is present in flash. ISP mode can be used to reprogram the flash, if the application codes uses JTAG pins for other multiplexed functionalities. On boot up, if the application code goes into a state where JTAG interface is not functioning, ISP mode can be used to gain the control and to reprogram the flash. Connect to a test point for debugging purposes.

Note:

1. "Default" state refers to the state of the device after initial boot loading and firmware loading is complete.
2. "Sleep" state refers to the state of the device after entering Sleep state
3. Please refer to "Reference Manual" for hardware programming information
4. Please refer to "API Documentation" for software programming information
5. In the application, wherever SiWx91x is connected to an external host, during the power-off state, the host should ensure that all the pins (analog or digital) connected to the SiWx91x are not driven. Else, the pins must be grounded.
6. For signals NWP_UART1_TX or NWP_UART2_TX, it is recommended to have a test point available for NWP debug prints
7. ISP functionality for UART, SDIO, and HSPI is not available when Secure Zone is enabled.
8. Connect each of these pins to test point for debugging purposes - JTAG_TCK_SWCLK, JTAG_TDI, JTAG_TMS_SWDIO, JTAG_TDO_SWO.

6.2.4 Miscellaneous Pins

Table 6.4. Miscellaneous Pins

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description
FLY_P1	B28	NA	Input	NA	Fly Capacitor for Switched cap DCDC. Please refer to Reference Schematics
FLY_N1	A32	NA	Input	NA	Fly Capacitor for Switched cap DCDC. Please refer to Reference Schematics
XTAL_IN	B12	RF_VBATT	Input	NA	Input to the on-chip oscillator from the external 40 MHz crystal.
XTAL_OUT	A13	RF_VBATT	Output	NA	Output of the on-chip oscillator to the external 40 MHz crystal.
TRST	A15	IO_VDD_2	Input	HighZ	Test signal. Connect to Ground.
XTAL_32KHZ_N	B26	NA	Inout	NA	Analog Pin. 32.768 kHz crystal connection
XTAL_32KHZ_P	A29	NA	Inout	NA	Analog Pin. 32.768 kHz crystal connection
NC	B9	NA	NA	NA	No-Connect

6.3 GPIO Pin Multiplexing

Note:

1. SiWx917 has the support for 45 GPIOs. These GPIOs are grouped into SoC GPIOs, ULP GPIOs, and UULP GPIOs.
2. **The possible GPIO combinations for each Peripheral Interface are listed in 6.4 Valid GPIO Sets for Peripherals.**
3. The digital GPIOs SOCPERH_ON_ULP_GPIO_0 to SOCPERH_ON_ULP_GPIO_11 are mapped onto physical ULP GPIOs for SoC Peripheral functionality and digital GPIOs ULPPERH_ON_SOC_GPIO_0 to ULPPERH_ON_SOC_GPIO_11 are mapped onto physical SoC GPIOs for ULP Peripheral functionality. Refer to 6.3.5 Digital Functions for peripheral mapping on these GPIOs

6.3.1 SoC GPIO Pin Multiplexing

The SoC GPIOs shown in Table 6.5. SoC GPIO Pin Multiplexing (GPIO_6 to GPIO_57) are available in the normal mode of operation (Power-states 4 and 3). Default mode is mode0 (Mode = 0) if not explicitly mentioned. For a description of power-states, refer to the Power States section of the Reference Manual. Each of these GPIOs Pin function is controlled by the GPIO Mode register mentioned in SoC GPIOs section of the Reference Manual.

Table 6.5. SoC GPIO Pin Multiplexing

GPIO	GPIO Modes 0, 1, 2, 3, 4, 5	GPIO Modes 6, 7, 8, 9, 10, 11	GPIO Modes 12, 13, 14, 15
GPIO_6	0: GPIO_6 1: 2: USART0_CTS 3: SSI_MST_DATA2 4: I2C0_SDA 5: I2C1_SCL	6: UART1_RX 7: I2S0_DIN_1 8: PMU_TEST_1 9: ULPPERH_ON_SOC_GPIO_0 10: PWM_0L 11: M4SS_QSPI_D0	12: GSPI_MOSI 13: M4SS_TRACE_CLKIN 14: 15: NWP_GPIO_6
GPIO_7	0: GPIO_7 1: 2: USART0_DTR 3: SSI_MST_DATA3 4: I2C0_SCL 5: I2C1_SDA	6: UART1_TX 7: I2S0_DOUT_1 8: PMU_TEST_2 9: ULPPERH_ON_SOC_GPIO_1 10: PWM_0H 11: M4SS_QSPI_CSN0	12: M4SS_QSPI_CSN1 13: M4SS_TRACE_CLK 14: 15:
GPIO_8 / ISP_UART_RX	0: GPIO_8 1: 2: USART0_CLK 3: SSI_MST_CLK 4: GSPI_CLK 5: QEI_IDX	6: UART1_RS485_RE 7: I2S0_CLK 8: SSI_SLV_CLK 9: ULPPERH_ON_SOC_GPIO_2 10: PWM_1L 11: M4SS_QSPI_CLK	12: 13: M4SS_TRACE_D0 14: 15: NWP_GPIO_8
GPIO_9 / ISP_UART_TX	0: GPIO_9 1: 2: USART0_RTS 3: SSI_MST_CS0 4: GSPI_CS0 5: QEI_PHA	6: UART1_RS485_DE 7: I2S0_WS 8: SSI_SLV_CS 9: ULPPERH_ON_SOC_GPIO_3 10: PWM_1H 11: M4SS_QSPI_D1	12: 13: M4SS_TRACE_D1 14: 15: NWP_GPIO_9
GPIO_10	0: GPIO_10 1: 2: USART0_RX 3: SSI_MST_CS1 4: GSPI_CS1 5: QEI_PHB	6: UART1_RTS 7: I2S0_DIN_0 8: SSI_SLV_MOSI 9: ULPPERH_ON_SOC_GPIO_4 10: PWM_2L 11: M4SS_QSPI_D2	12: SSI_MST_DATA1 13: M4SS_TRACE_D2 14: 15: NWP_GPIO_10

GPIO	GPIO Modes 0, 1, 2, 3, 4, 5	GPIO Modes 6, 7, 8, 9, 10, 11	GPIO Modes 12, 13, 14, 15
GPIO_11	0: GPIO_11 1: 2: USART0_DSR 3: SSI_MST_DATA0 4: GSPI_MISO 5: QEI_DIR	6: UART1_CTS 7: I2S0_DOUT_0 8: SSI_SLV_MISO 9: ULPPERH_ON_SOC_GPIO_5 10: PWM_2H 11: M4SS_QSPI_D3	12: MCU_CLK_OUT 13: M4SS_TRACE_D3 14: 15: NWP_GPIO_11
GPIO_12	0: GPIO_12 1: 2: USART0_DCD 3: SSI_MST_DATA1 4: GSPI_MOSI 5:	6: UART1_RS485_EN 7: 8: MCU_CLK_OUT 9: ULPPERH_ON_SOC_GPIO_6 10: PWM_3L 11:	12: 13: 14: 15: NWP_GPIO_12
GPIO_15	0: GPIO_15 1: 2: USART0_TX 3: SSI_MST_CS2 4: GSPI_CS2 5:	6: M4SS_TRACE_CLKIN 7: 8: MCU_CLK_OUT 9: ULPPERH_ON_SOC_GPIO_7 10: PWM_3H 11:	12: 13: 14: 15: NWP_GPIO_15
GPIO_25 / SDIO_CLK / HSPI_CLK	0: GPIO_25 1: 2: USART0_CLK 3: SSI_MST_CLK 4: GSPI_CLK 5: QEI_IDX	6: 7: I2S0_CLK 8: SSI_SLV_CS 9: SCT_IN_0 10: PWM_FAULTA 11: ULPPERH_ON_SOC_GPIO_6	12: SOC_PLL_CLOCK 13: 14: TopGPIO_0 15:
GPIO_26 / SDIO_CMD / HSPI_CSN	0: GPIO_26 1: 2: USART0_CTS 3: SSI_MST_DATA0 4: GSPI_MISO 5: QEI_PHA	6: UART1_RS485_EN 7: I2S0_WS 8: SSI_SLV_CLK 9: 10: PWM_FAULTB 11: ULPPERH_ON_SOC_GPIO_7	12: INTERFACE_PLL_CLOCK 13: 14: TopGPIO_1 15:
GPIO_27 / SDIO_D0 / HSPI_MOSI	0: GPIO_27 1: 2: USART0_RI 3: SSI_MST_DATA1 4: GSPI_MOSI 5: QEI_PHB	6: UART1_RTS 7: I2S0_DIN_0 8: SSI_SLV_MOSI 9: 10: PWM_TMR_EXT_TRIG_1 11: ULPPERH_ON_SOC_GPIO_8	12: I2S_PLL_CLOCK 13: USART0_RS485_EN 14: TopGPIO_2 15:

GPIO	GPIO Modes 0, 1, 2, 3, 4, 5	GPIO Modes 6, 7, 8, 9, 10, 11	GPIO Modes 12, 13, 14, 15
GPIO_28 / SDIO_D1 / HSPI_MISO	0: GPIO_28 1: 2: USART0_RTS 3: SSI_MST_CS0 4: GSPI_CS0 5: QEI_DIR	6: UART1_CTS 7: I2S0_DOUT_0 8: SSI_SLV_MISO 9: 10: PWM_TMR_EXT_TRIG_2 11: ULPPERH_ON_SOC_GPIO_9	12: XTAL_ON_IN 13: USART0_RS485_RE 14: TopGPIO_3 15:
GPIO_29 / SDIO_D2 / HSPI_INTR	0: GPIO_29 1: 2: USART0_RX 3: SSI_MST_DATA2 4: GSPI_CS1 5: I2C1_SCL	6: UART1_RX 7: I2S0_DIN_1 8: PMU_TEST_1 9: SCT_OUT_0 10: PWM_TMR_EXT_TRIG_3 11: ULPPERH_ON_SOC_GPIO_10	12: USART0_DCD 13: USART0_RS485_DE 14: TopGPIO_4 15:
GPIO_30 / SDIO_D3	0: GPIO_30 1: 2: USART0_TX 3: SSI_MST_DATA3 4: GSPI_CS2 5: I2C1_SDA	6: UART1_TX 7: I2S0_DOUT_1 8: PMU_TEST_2 9: SCT_OUT_1 10: PWM_TMR_EXT_TRIG_4 11: ULPPERH_ON_SOC_GPIO_11	12: PMU_TEST_1 13: PMU_TEST_2 14: TopGPIO_5 15:
JTAG_TCK_SWCLK	0: GPIO_31 1: 2: 3: 4: 5:	6: 7: 8: 9: 10: 11: I2C0_SDA	12: UART1_RTS 13: QEI_IDX 14: 15:
JTAG_TDI	0: GPIO_32 1: 2: 3: 4: 5:	6: 7: 8: 9: 10: 11: I2C0_SCL	12: UART1_CTS 13: QEI_PHA 14: 15:
JTAG_TMS_SWDIO	0: GPIO_33 1: 2: 3: 4: 5:	6: 7: 8: 9: 10: 11: I2C1_SCL	12: UART1_RX 13: QEI_PHB 14: 15:

GPIO	GPIO Modes 0, 1, 2, 3, 4, 5	GPIO Modes 6, 7, 8, 9, 10, 11	GPIO Modes 12, 13, 14, 15
JTAG_TDO_SWO	0: GPIO_34 1: 2: 3: 4: 5:	6: 7: 8: 9: 10: 11: I2C1_SDA	12: UART1_TX 13: QEI_DIR 14: 15:
GPIO_46	0: GPIO_46 1: M4SS_QSPI_CLK 2: USART0_RI 3: QEI_IDX 4: GSPI_CLK 5:	6: M4SS_TRACE_CLKIN 7: I2S0_CLK 8: SSI_SLV_CS 9: ULPPERH_ON_SOC_GPIO_8 10: SOC_PLL_CLOCK 11: M4SS_PSRAM_CLK	12: 13: 14: 15: NWP_GPIO_46
GPIO_47	0: GPIO_47 1: M4SS_QSPI_D0 2: 3: QEI_PHA 4: GSPI_MISO 5:	6: M4SS_TRACE_CLK 7: I2S0_WS 8: SSI_SLV_CLK 9: ULPPERH_ON_SOC_GPIO_9 10: INTERFACE_PLL_CLOCK 11: M4SS_PSRAM_D0	12: 13: 14: 15: NWP_GPIO_47
GPIO_48	0: GPIO_48 1: M4SS_QSPI_D1 2: 3: QEI_PHB 4: GSPI_MOSI 5:	6: M4SS_TRACE_D0 7: I2S0_DIN_0 8: SSI_SLV_MOSI 9: ULPPERH_ON_SOC_GPIO_10 10: I2S_PLL_CLOCK 11: M4SS_PSRAM_D1	12: 13: 14: 15: NWP_GPIO_48
GPIO_49	0: GPIO_49 1: M4SS_QSPI_CSN0 2: USART0_RS485_EN 3: QEI_DIR 4: GSPI_CS0 5:	6: M4SS_TRACE_D1 7: I2S0_DOUT_0 8: SSI_SLV_MISO 9: ULPPERH_ON_SOC_GPIO_11 10: 11: M4SS_PSRAM_CSN0	12: 13: 14: 15: NWP_GPIO_49
GPIO_50	0: GPIO_50 1: M4SS_QSPI_D2 2: USART0_RS485_RE 3: SSI_MST_CS2 4: GSPI_CS1 5: I2C1_SCL	6: M4SS_TRACE_D2 7: I2S0_DIN_1 8: PWM_TMR_EXT_TRIG_4 9: UART1_RTS 10: MEMS_REF_CLOCK 11: M4SS_PSRAM_D2	12: 13: 14: 15: NWP_GPIO_50

GPIO	GPIO Modes 0, 1, 2, 3, 4, 5	GPIO Modes 6, 7, 8, 9, 10, 11	GPIO Modes 12, 13, 14, 15
GPIO_51	0: GPIO_51 1: M4SS_QSPI_D3 2: USART0_RS485_DE 3: SSI_MST_CS3 4: GSPI_CS2 5: I2C1_SDA	6: M4SS_TRACE_D3 7: I2S0_DOUT_1 8: PWM_TMR_EXT_TRIG_1 9: UART1_CTS 10: PLL_TESTMODE_SIG 11: M4SS_PSRAM_D3	12: 13: 14: 15: NWP_GPIO_51
GPIO_52	0: GPIO_52 1: 2: USART0_CLK 3: SSI_MST_CLK 4: GSPI_CLK 5: QEI_IDX	6: M4SS_TRACE_CLKIN 7: I2S0_CLK 8: SSI_SLV_CLK 9: M4SS_QSPI_CLK 10: SOC_PLL_CLOCK 11:	12: M4SS_PSRAM_CLK 13: 14: 15:
GPIO_53	0: GPIO_53 1: M4SS_QSPI_CSN1 2: USART0_RTS 3: SSI_MST_CS0 4: GSPI_CS0 5: QEI_PHA	6: M4SS_TRACE_CLK 7: I2S0_WS 8: SSI_SLV_CS 9: M4SS_QSPI_D0 10: INTERFACE_PLL_CLOCK 11: M4SS_PSRAM_CSN1	12: M4SS_PSRAM_D0 13: 14: 15:
GPIO_54	0: GPIO_54 1: M4SS_QSPI_D4 2: USART0_TX 3: SSI_MST_DATA2 4: GSPI_CS1 5: I2C1_SCL	6: M4SS_TRACE_D0 7: I2S0_DIN_1 8: PWM_TMR_EXT_TRIG_2 9: M4SS_QSPI_D1 10: I2S_PLL_CLOCK 11: M4SS_PSRAM_D4	12: M4SS_PSRAM_D1 13: 14: 15:
GPIO_55	0: GPIO_55 1: M4SS_QSPI_D5 2: USART0_RX 3: SSI_MST_DATA3 4: GSPI_CS2 5: I2C1_SDA	6: M4SS_TRACE_D1 7: I2S0_DOUT_1 8: PWM_TMR_EXT_TRIG_3 9: M4SS_QSPI_CSN0 10: 11: M4SS_PSRAM_D5	12: M4SS_PSRAM_CSN0 13: 14: 15:
GPIO_56	0: GPIO_56 1: M4SS_QSPI_D6 2: USART0_CTS 3: SSI_MST_DATA0 4: GSPI_MISO 5: QEI_PHB	6: M4SS_TRACE_D2 7: I2S0_DIN_0 8: SSI_SLV_MOSI 9: M4SS_QSPI_D2 10: MEMS_REF_CLOCK 11: M4SS_PSRAM_D6	12: M4SS_PSRAM_D2 13: 14: 15:

GPIO	GPIO Modes 0, 1, 2, 3, 4, 5	GPIO Modes 6, 7, 8, 9, 10, 11	GPIO Modes 12, 13, 14, 15
GPIO_57	0: GPIO_57 1: M4SS_QSPI_D7 2: USART0_DSR 3: SSI_MST_DATA1 4: GSPI_MOSI 5: QEI_DIR	6: M4SS_TRACE_D3 7: I2S0_DOUT_0 8: SSI_SLV_MISO 9: M4SS_QSPI_D3 10: XTAL_ON_IN 11: M4SS_PSRAM_D7	12: M4SS_PSRAM_D3 13: 14: 15:

Note:

1. GPIOs 25 to 30 can be used for Analog functions when GPIO Mode = 14. Multiple Analog functions are available on each pin as shown in the below Analog Pin Multiplexing Table. These analog functions are enabled and disabled through programming - refer to the Reference Manual for more details.
2. NWP GPIOs can be used for Network Processor functions when GPIO Mode = 15.

6.3.2 ULP GPIO Pin Multiplexing

The ULP GPIOs shown in Table 6.6. ULP GPIO Pin Multiplexing (ULP_GPIO_0 to ULP_GPIO_11) are available in the normal mode of operation (Power-states 4 and 3) and also in Ultra-low power mode of operation of the Microcontroller (Power-states 2 and 1). For a description of power-states, refer to the Power States section of the Reference Manual. Each of these GPIO's Pin function is controlled by the GPIO Mode register mentioned in ULP GPIO's section of the Reference Manual.

Table 6.6. ULP GPIO Pin Multiplexing

ULP_GPIO	ULP GPIO Modes 0, 1, 2, 3	ULP GPIO Modes 4, 5, 6, 7
ULP_GPIO_0	0: ULP_EGPIO_0	4: ULP_I2C_SDA
	1: ULP_SSI_CLK	5:
	2: ULP_I2S_DIN	6: SOCPERH_ON_ULP_GPIO_0
	3: ULP_UART_RTS	7: AGPIO_0
ULP_GPIO_1	0: ULP_EGPIO_1	4: ULP_I2C_SCL
	1: ULP_SSI_DOUT	5: Timer2
	2: ULP_I2S_DOUT	6: SOCPERH_ON_ULP_GPIO_1
	3: ULP_UART_CTS	7: AGPIO_1
ULP_GPIO_2	0: ULP_EGPIO_2	4:
	1: ULP_SSI_DIN	5: COMP1_OUT
	2: ULP_I2S_WS	6: SOCPERH_ON_ULP_GPIO_2
	3: ULP_UART_RX	7: AGPIO_2
ULP_GPIO_4	0: ULP_EGPIO_4	4: ULP_I2C_SDA
	1: ULP_SSI_CS1	5: AUX_ULP_TRIG_1
	2: ULP_I2S_WS	6: SOCPERH_ON_ULP_GPIO_4
	3: ULP_UART_RTS	7: AGPIO_4
ULP_GPIO_5	0: ULP_EGPIO_5	4: ULP_I2C_SCL
	1: IR_OUTPUT	5: AUX_ULP_TRIG_0
	2: ULP_I2S_DOUT	6: SOCPERH_ON_ULP_GPIO_5
	3: ULP_UART_CTS	7: AGPIO_5
ULP_GPIO_6	0: ULP_EGPIO_6	4: ULP_I2C_SDA
	1: ULP_SSI_CS2	5:
	2: ULP_I2S_DIN	6: SOCPERH_ON_ULP_GPIO_6
	3: ULP_UART_RX	7: AGPIO_6
ULP_GPIO_7	0: ULP_EGPIO_7	4: ULP_I2C_SCL
	1: IR_INPUT	5: Timer1
	2: ULP_I2S_CLK	6: SOCPERH_ON_ULP_GPIO_7
	3: ULP_UART_TX	7: AGPIO_7
ULP_GPIO_8	0: ULP_EGPIO_8	4: ULP_I2C_SCL
	1: ULP_SSI_CLK	5: Timer0
	2: ULP_I2S_CLK	6: SOCPERH_ON_ULP_GPIO_8
	3: ULP_UART_CTS	7: AGPIO_8

ULP_GPIO	ULP GPIO Modes 0, 1, 2, 3	ULP GPIO Modes 4, 5, 6, 7
ULP_GPIO_9	0: ULP_EGPIO_9	4: ULP_I2C_SDA
	1: ULP_SSI_DIN	5:
	2: ULP_I2S_DIN	6: SOCPERH_ON_ULP_GPIO_9
	3: ULP_UART_RX	7: AGPIO_9
ULP_GPIO_10	0: ULP_EGPIO_10	4: IR_INPUT
	1: ULP_SSI_CS0	5:
	2: ULP_I2S_WS	6: SOCPERH_ON_ULP_GPIO_10
	3: ULP_UART_RTS	7: AGPIO_10
ULP_GPIO_11	0: ULP_EGPIO_11	4: ULP_I2C_SDA
	1: ULP_SSI_DOUT	5: AUX_ULP_TRIG_0
	2: ULP_I2S_DOUT	6: SOCPERH_ON_ULP_GPIO_11
	3: ULP_UART_TX	7: AGPIO_11

Note:

1. All the ULP GPIOs can be used for Analog functions when ULP GPIO Mode = 7. Multiple Analog functions are available on each pin as shown in the below Analog Pin Multiplexing Table. These analog functions are enabled and disabled through programming - refer to the Reference Manual for more details.
2. All the ULP GPIO's can be used for Digital functions when ULP GPIO Mode = 6. The digital functions available on these GPIOs is shown in the below Digital Pin Multiplexing Table.

6.3.3 UULP VBAT GPIO Pin Multiplexing

The UULP VBAT GPIOs shown in Table 6.7. UULP VBAT GPIO Pin Multiplexing (UULP_VBAT_GPIO_0 to UULP_VBAT_GPIO_3) are available in the normal mode of operation (Power-states 4 and 3), in Ultra-low power mode of operation (Power-states 2 and 1) and also in the retention and deep sleep mode of operation (Retention and Power-state 0). For a description of power-states, refer to the Power States section of the Reference Manual. Each of this UULP VBAT GPIO's Pin function is controlled by the GPIO Mode register mentioned in UULP VBAT GPIO's section of the Reference Manual.

Table 6.7. UULP VBAT GPIO Pin Multiplexing

UULP VBAT GPIO	UULP VBAT GPIO Mode = 0, 1, 2, 3	UULP VBAT GPIO Mode = 4, 5, 6, 7	Default
UULP_VBAT_GPIO_0	0: UULP_VBAT_GPIO[0] 1: 2: MCU_GPIO0_WAKEUP 3: SYSRTC_PRS_IN_G0	4: SYSRTC_PRS_OUT_G0_1 5: 6: 7:	1: (no function)
UULP_VBAT_GPIO_1	0: UULP_VBAT_GPIO[1] 1: 2: MCU_GPIO1_WAKEUP 3:	4: SYSRTC_PRS_IN_G1 5: SYSRTC_PRS_OUT_G1_0 6: MCU_GPIO_TOGGLE 7:	1: (no function)
UULP_VBAT_GPIO_2	0: UULP_VBAT_GPIO[2] 1: NWP_GPIO0_WAKEUP 2: MCU_GPIO2_WAKEUP 3: MCU_GPIO_TOGGLE	4: 5: SYSRTC_PRS_OUT_G1_1 6: 7: VOLT_SENSE	NWP_GPIO0_WAKEUP
UULP_VBAT_GPIO_3	0: UULP_VBAT_GPIO[3] 1: NWP_GPIO1_WAKEUP 2: MCU_GPIO3_WAKEUP 3: SYSRTC_PRS_OUT_G0_0	4: MCU_GPIO_TOGGLE 5: 6: 7: COMP_P	UULP_VBAT_GPIO[3]

6.3.4 Analog Functions

Analog functions are available on several of the SoC GPIO and ULP_GPIO pins. The analog functions are mapped to ULP_GPIO pins on the AGPIO_x selections, and to SoC GPIO pins on the TopGPIO_x selections shown in the multiplexing tables. A summary of signals and potential GPIO mapping are shown in Table 6.8. Analog Functions for SoC/ULP GPIOs.

Table 6.8. Analog Functions for SoC/ULP GPIOs

Signal - GPIO	ADC Function	DAC Function	Comparator Function	OpAmp Function
AGPIO_0 - ULP_GPIO_0	ADCP[0]		COMP1_P0	OPAMP1_IN[2]
AGPIO_1 - ULP_GPIO_1	ADCP[10] ADCN[0]		COMP1_N0	
AGPIO_2 - ULP_GPIO_2	ADCP[1]		COMP2_P0	OPAMP1_IN[3]
AGPIO_4 - ULP_GPIO_4	ADCP[2]	DAC0	COMP1_N1	OPAMP1OUT0
AGPIO_5 - ULP_GPIO_5	ADCP[12] ADCN[2]		COMP1_P1	OPAMP2_IN[1]
AGPIO_6 - ULP_GPIO_6	ADCP[3]			OPAMP1_IN[4]
AGPIO_7 - ULP_GPIO_7	ADCP[15] ADCN[5]			OPAMP1_IN[1]
AGPIO_8 - ULP_GPIO_8	ADCP[4]			OPAMP1_IN[5]
AGPIO_9 - ULP_GPIO_9	ADCP[14] ADCN[4]			OPAMP2OUT0
AGPIO_10 - ULP_GPIO_10	ADCP[5]			OPAMP3_IN[0]
AGPIO_11 - ULP_GPIO_11	ADCP[13] ADCN[3]			OPAMP2_IN[0]
TopGPIO_0 - GPIO_25	ADCP[6]			
TopGPIO_1 - GPIO_26	ADCP[16] ADCN[6]			
TopGPIO_2 - GPIO_27	ADCP[7]		COMP2_P1	OPAMP3OUT0 OPAMP1_IN[0]
TopGPIO_3 - GPIO_28	ADCP[17] ADCN[7]		COMP2_N1	
TopGPIO_4 - GPIO_29	ADCP[8]			OPAMP3_IN[1]
TopGPIO_5 - GPIO_30	ADCP[18] ADCN[8]	DAC1		OPAMP1OUT1

Note:

1. Software can program above different functions.
2. ADCP and ADCN can be independently selected from any of the channels shown. Single-ended measurements use only ADCP, and differential measurements use both ADCP and ADCN.
3. Please refer to "Reference Manual" for software programming information.
4. Please refer to "API Documentation" for software programming information.

6.3.5 Digital Functions

The ULP GPIOs shown in Table 6.9. SoC on ULP GPIO Pin Multiplexing are configured for SoC peripheral functionality (SOCPERH_ON_ULP_GPIO_0 to SOCPERH_ON_ULP_GPIO_11) and are available only in the normal mode of operation (Power-states 4 and 3). For a description of power-states, refer to the Power States section of the Reference Manual. Each of these GPIO's Pin function is controlled by the GPIO Mode register mentioned in SoC GPIO's section of the Reference Manual."

Table 6.9. SoC on ULP GPIO Pin Multiplexing

GPIO	GPIO Modes 0, 1, 2, 3, 4	GPIO Modes 5, 6, 7, 8, 9	GPIO Modes 10, 11, 12, 13
SOCPERH_ON_ULP_GPIO_0	0: GPIO_64 1: 2: USART0_CLK 3: QEI_IDX 4: I2C0_SDA	5: I2C1_SCL 6: UART1_RS485_EN 7: SCT_IN_0 8: PWM_0L 9: UART1_RTS	10: 11: 12: PWM_0L 13: PMU_TEST_1
SOCPERH_ON_ULP_GPIO_1	0: GPIO_65 1: 2: USART0_RX 3: QEI_PHA 4: I2C0_SCL	5: I2C1_SDA 6: UART1_RS485_RE 7: 8: PWM_0H 9: UART1_CTS	10: 11: 12: PWM_0H 13: PMU_TEST_2
SOCPERH_ON_ULP_GPIO_2	0: GPIO_66 1: 2: 3: QEI_PHB 4: I2C0_SCL	5: I2C1_SCL 6: UART1_RS485_DE 7: 8: PWM_1L 9: UART1_RX	10: PMU_TEST_1 11: 12: 13:
SOCPERH_ON_ULP_GPIO_4	0: GPIO_68 1: 2: USART0_TX 3: QEI_IDX 4:	5: 6: UART1_RX 7: SCT_OUT_0 8: PWM_2L 9: SCT_IN_0	10: PWM_FAULTA 11: USART0_RI 12: PWM_1L 13:
SOCPERH_ON_ULP_GPIO_5	0: GPIO_69 1: 2: USART0_RTS 3: QEI_PHA 4:	5: 6: UART1_TX 7: SCT_OUT_1 8: PWM_2H 9:	10: PWM_FAULTB 11: USART0_RS485_EN 12: PWM_1H 13:
SOCPERH_ON_ULP_GPIO_6	0: GPIO_70 1: 2: USART0_CTS 3: QEI_PHB 4: USART0_RX	5: I2C1_SCL 6: UART1_RTS 7: 8: PWM_3L 9:	10: PWM_TMR_EXT_TRIG_1 11: USART0_RS485_RE 12: PMU_TEST_1 13:

GPIO	GPIO Modes 0, 1, 2, 3, 4	GPIO Modes 5, 6, 7, 8, 9	GPIO Modes 10, 11, 12, 13
SOCPERH_ON_ULP_GPIO_7	0: GPIO_71 1: 2: 3: QEI_DIR 4: USART0_TX	5: I2C1_SDA 6: UART1_CTS 7: 8: PWM_3H 9:	10: PWM_TMR_EXT_TRIG_2 11: USART0_RS485_DE 12: PMU_TEST_2 13:
SOCPERH_ON_ULP_GPIO_8	0: GPIO_72 1: 2: 3: QEI_IDX 4:	5: 6: UART1_RX 7: 8: PWM_SLP_EVENT_TRIG 9: UART1_RTS	10: PWM_TMR_EXT_TRIG_3 11: 12: 13:
SOCPERH_ON_ULP_GPIO_9	0: GPIO_73 1: 2: USART0_RS485_EN 3: QEI_PHA 4:	5: 6: UART1_TX 7: 8: PWM_FAULTA 9: UART1_CTS	10: PWM_TMR_EXT_TRIG_4 11: 12: 13:
SOCPERH_ON_ULP_GPIO_10	0: GPIO_74 1: 2: USART0_RS485_RE 3: QEI_PHB 4: I2C0_SDA	5: 6: UART1_RS485_RE 7: 8: PWM_FAULTB 9: UART1_RX	10: PMU_TEST_1 11: 12: 13:
SOCPERH_ON_ULP_GPIO_11	0: GPIO_75 1: 2: USART0_RS485_DE 3: QEI_DIR 4: I2C0_SCL	5: 6: UART1_RS485_DE 7: 8: PWM_TMR_EXT_TRIG_1 9: UART1_TX	10: PMU_TEST_2 11: 12: 13:

The SoC GPIOs shown in Table 6.10. ULP on SoC GPIO Pin Multiplexing are configured for ULP peripheral functionality (ULPPERH_ON_SOC_GPIO_0 to ULPPERH_ON_SOC_GPIO_11) and are available only in the normal mode of operation (Power-states 4 and 3). For a description of power-states, refer to the Power States section of the Reference Manual. Each of these GPIO's Pin function is controlled by the GPIO Mode register mentioned in ULP GPIO's section of the Reference Manual.

Table 6.10. ULP on SoC GPIO Pin Multiplexing

ULP_GPIO	ULP GPIO Mode = 0, 1, 2, 3	ULP GPIO Mode = 4, 5, 6, 7
ULPPERH_ON_SOC_GPIO_0	0: ULP_EGPIO[0]	4: ULP_I2C_SDA
	1: ULP_SSI_CLK	5:
	2: ULP_I2S_DIN	6:
	3: ULP_UART_RTS	7:
ULPPERH_ON_SOC_GPIO_1	0: ULP_EGPIO[1]	4: ULP_I2C_SCL
	1: ULP_SSI_DOUT	5: Timer0
	2: ULP_I2S_DOUT	6:
	3: ULP_UART_CTS	7:
ULPPERH_ON_SOC_GPIO_2	0: ULP_EGPIO[2]	4:
	1: ULP_SSI_DIN	5: COMP1_OUT
	2: ULP_I2S_WS	6:
	3: ULP_UART_RX	7:
ULPPERH_ON_SOC_GPIO_3	0: ULP_EGPIO[3]	4: COMP2_OUT
	1: ULP_SSI_CS0	5:
	2: ULP_I2S_CLK	6:
	3: ULP_UART_TX	7:
ULPPERH_ON_SOC_GPIO_4	0: ULP_EGPIO[4]	4: ULP_I2C_SDA
	1: ULP_SSI_CS1	5:
	2: ULP_I2S_WS	6:
	3: ULP_UART_RTS	7:
ULPPERH_ON_SOC_GPIO_5	0: ULP_EGPIO[5]	4: ULP_I2C_SCL
	1: IR_OUTPUT	5: AUX_ULP_TRIG_0
	2: ULP_I2S_DOUT	6:
	3: ULP_UART_CTS	7:
ULPPERH_ON_SOC_GPIO_6	0: ULP_EGPIO[6]	4: ULP_I2C_SDA
	1: ULP_SSI_CS2	5:
	2: ULP_I2S_DIN	6:
	3: ULP_UART_RX	7:
ULPPERH_ON_SOC_GPIO_7	0: ULP_EGPIO[7]	4: ULP_I2C_SCL
	1: IR_INPUT	5: Timer1
	2: ULP_I2S_CLK	6:
	3: ULP_UART_TX	7:

ULP_GPIO	ULP GPIO Mode = 0, 1, 2, 3	ULP GPIO Mode = 4, 5, 6, 7
ULPPERH_ON_SOC_GPIO_8	0: ULP_EGPIO[8] 1: ULP_SSI_CLK 2: ULP_I2S_CLK 3: ULP_UART_CTS	4: ULP_I2C_SCL 5: Timer0 6: 7:
ULPPERH_ON_SOC_GPIO_9	0: ULP_EGPIO[9] 1: ULP_SSI_DIN 2: ULP_I2S_DIN 3: ULP_UART_RX	4: ULP_I2C_SDA 5: COMP1_OUT 6: 7:
ULPPERH_ON_SOC_GPIO_10	0: ULP_EGPIO[10] 1: ULP_SSI_CS0 2: ULP_I2S_WS 3: ULP_UART_RTS	4: IR_INPUT 5: 6: 7:
ULPPERH_ON_SOC_GPIO_11	0: ULP_EGPIO[11] 1: ULP_SSI_DOUT 2: ULP_I2S_DOUT 3: ULP_UART_TX	4: ULP_I2C_SDA 5: AUX_ULP_TRIG_0 6: 7:

6.4 Valid GPIO Sets for Peripherals

Functions can be split pin wise across all GPIOs except for below restrictions. For synchronous interfaces there are some restrictions on clubbing of GPIOs into synchronous buses to ensure the timings mentioned in section SiWx917 SoC Specifications. For example a single synchronous interface should not be split across ULP & SoC GPIO's. Table 6.11. Peripheral Interface Options shows recommended locations for each function. For GPIO mode related information refer to 6.3 GPIO Pin Multiplexing .

Table 6.11. Peripheral Interface Options

ULP SSI (Synchronous Serial Interface) Primary		
IO Functionality	Combinations possible on ULP GPIOs	Combinations possible on SoC GPIOs
ULP_SSI_CLK	ULP_GPIO_0 / ULP_GPIO_8	GPIO_6 / GPIO_46
ULP_SSI_CS0	ULP_GPIO_10	GPIO_48
ULP_SSI_CS1	ULP_GPIO_4	GPIO_10
ULP_SSI_CS2	ULP_GPIO_6	GPIO_12
ULP_SSI_DIN	ULP_GPIO_2 / ULP_GPIO_9	GPIO_8 / GPIO_47
ULP_SSI_DOUT	ULP_GPIO_1 / ULP_GPIO_11	GPIO_7 / GPIO_49
ULP I2S Primary/Secondary		
IO Functionality	Combinations possible on ULP GPIOs	Combinations possible on SoC GPIOs
ULP_I2S_CLK	ULP_GPIO_7 / ULP_GPIO_8	GPIO_15 / GPIO_46
ULP_I2S_WS	ULP_GPIO_4 / ULP_GPIO_10	GPIO_8 / GPIO_10 / GPIO_48
ULP_I2S_DIN	ULP_GPIO_0 / ULP_GPIO_6 / ULP_GPIO_9	GPIO_6 / GPIO_12 / GPIO_47
ULP_I2S_DOUT	ULP_GPIO_1 / ULP_GPIO_5 / ULP_GPIO_11	GPIO_7 / GPIO_11 / GPIO_49
ULP I2C INTERFACE		
IO Functionality	Combinations possible on ULP GPIOs	Combinations possible on SoC GPIOs
ULP_I2C_SCL	ULP_GPIO_1 / ULP_GPIO_5 / ULP_GPIO_7 / ULP_GPIO_8	GPIO_7 / GPIO_11 / GPIO_15 / GPIO_46
ULP_I2C_SDA	ULP_GPIO_0 / ULP_GPIO_4 / ULP_GPIO_6 / ULP_GPIO_9 / ULP_GPIO_11	GPIO_6 / GPIO_10 / GPIO_12 / GPIO_47 / GPIO_49
ULP UART INTERFACE		
IO Functionality	Combinations possible on ULP GPIOs	Combinations possible on SoC GPIOs
ULP_UART_TX	ULP_GPIO_7 / ULP_GPIO_11	GPIO_9 / GPIO_15 / GPIO_49

ULP_UART_RX	ULP_GPIO_2 / ULP_GPIO_6 / ULP_GPIO_9	GPIO_8 / GPIO_12 / GPIO_47
ULP_UART_CTS	ULP_GPIO_1 / ULP_GPIO_5 / ULP_GPIO_8	GPIO_7 / GPIO_11 / GPIO_46
ULP_UART_RTS	ULP_GPIO_0 / ULP_GPIO_4 / ULP_GPIO_10	GPIO_6 / GPIO_10 / GPIO_48
Timer Interrupt Interface		
IO Functionality	Combinations possible on ULP GPIOs	Combinations possible on SoC GPIOs
Timer0	ULP_GPIO_8	GPIO_46
Timer1	ULP_GPIO_7	GPIO_15
Timer2	ULP_GPIO_1	GPIO_7
MCU SSI (Synchronous Serial Interface) Primary[1]		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
SSI_MST_CLK	GPIO_8 / GPIO_25 / GPIO_52	
SSI_MST_CS0	GPIO_9 / GPIO_28 / GPIO_53	
SSI_MST_CS1	GPIO_10	
SSI_MST_CS2	GPIO_15 / GPIO_50	
SSI_MST_CS3	GPIO_51	
SSI_MST_DATA0	GPIO_11 / GPIO_26 / GPIO_56	
SSI_MST_DATA1	GPIO_12 / GPIO_27 / GPIO_57	
SSI_MST_DATA2	GPIO_6 / GPIO_29 / GPIO_54	
SSI_MST_DATA3	GPIO_7 / GPIO_30 / GPIO_55	
MCU SSI (Synchronous Serial Interface) Secondary[1]		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
SSI_SLV_CLK	GPIO_8 / GPIO_26 / GPIO_47 / GPIO_52	
SSI_SLV_CS	GPIO_9 / GPIO_25 / GPIO_46 / GPIO_53	
SSI_SLV_MISO	GPIO_11 / GPIO_28 / GPIO_49 / GPIO_57	
SSI_SLV_MOSI	GPIO_10 / GPIO_27 / GPIO_48 / GPIO_56	
GSPI (General SPI) Interface[2]		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
GSPI_CLK	GPIO_8 / GPIO_25 / GPIO_46 / GPIO_52	

GSPI_CS0	GPIO_9 / GPIO_28 / GPIO_49 / GPIO_53	
GSPI_CS1	GPIO_10 / GPIO_29 / GPIO_50 / GPIO_54	
GSPI_CS2	GPIO_15 / GPIO_30 / GPIO_51 / GPIO_55	
GSPI_MISO	GPIO_11 / GPIO_26 / GPIO_47 / GPIO_56	
GSPI_MOSI	GPIO_6 / GPIO_12 / GPIO_27 / GPIO_48 / GPIO_57	
QSPI (Quad SPI) Interface		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
M4SS_QSPI_CLK	GPIO_8 / GPIO_46 / GPIO_52	
M4SS_QSPI_CSN0	GPIO_7 / GPIO_49 / GPIO_55	
M4SS_QSPI_CSN1	GPIO_7 / GPIO_53	
M4SS_QSPI_D0	GPIO_6 / GPIO_47 / GPIO_53	
M4SS_QSPI_D1	GPIO_9 / GPIO_48 / GPIO_54	
M4SS_QSPI_D2	GPIO_10 / GPIO_50 / GPIO_56	
M4SS_QSPI_D3	GPIO_11 / GPIO_51 / GPIO_57	
M4SS_QSPI_D4	GPIO_54	
M4SS_QSPI_D5	GPIO_55	
M4SS_QSPI_D6	GPIO_56	
M4SS_QSPI_D7	GPIO_57	
QSPI_PSRAM Interface		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
M4SS_PSRAM_CLK	GPIO_46 / GPIO_52	
M4SS_PSRAM_CSN0	GPIO_49 / GPIO_55	
M4SS_PSRAM_D0	GPIO_47 / GPIO_53	
M4SS_PSRAM_D1	GPIO_48 / GPIO_54	
M4SS_PSRAM_D2	GPIO_50 / GPIO_56	
M4SS_PSRAM_D3	GPIO_51 / GPIO_57	
I2S Primary/Secondary		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
I2S0_CLK	GPIO_8 / GPIO_25 / GPIO_46 / GPIO_52	
I2S0_WS	GPIO_9 / GPIO_26 / GPIO_47 / GPIO_53	

I2S0_DIN_0	GPIO_10 / GPIO_27 / GPIO_48 / GPIO_56	
I2S0_DIN_1	GPIO_6 / GPIO_29 / GPIO_50 / GPIO_54	
I2S0_DOUT_0	GPIO_11 / GPIO_28 / GPIO_49 / GPIO_57	
I2S0_DOUT_1	GPIO_7 / GPIO_30 / GPIO_51 / GPIO_55	
I2C0 INTERFACE		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
I2C0_SCL	GPIO_7 / JTAG_TDI	ULP_GPIO_1 / ULP_GPIO_11
I2C0_SDA	GPIO_6 / JTAG_TCK_SWCLK	ULP_GPIO_0 / ULP_GPIO_10
I2C1 INTERFACE		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
I2C1_SCL	GPIO_6 / JTAG_TMS_SWDIO / GPIO_50 / GPIO_54	ULP_GPIO_0 / ULP_GPIO_6
I2C1_SDA	GPIO_7 / JTAG_TDO_SWO / GPIO_51 / GPIO_55	ULP_GPIO_1 / ULP_GPIO_7
MCPWM Interface		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
PWM_0H	GPIO_7	ULP_GPIO_1
PWM_0L	GPIO_6	ULP_GPIO_0
PWM_1H	GPIO_9	ULP_GPIO_5
PWM_1L	GPIO_8	ULP_GPIO_2 / ULP_GPIO_4
PWM_2H	GPIO_11	ULP_GPIO_5
PWM_2L	GPIO_10	ULP_GPIO_4
PWM_3H	GPIO_15	ULP_GPIO_7
PWM_3L	GPIO_12	ULP_GPIO_6
PWM_FAULTA	GPIO_25	ULP_GPIO_4 / ULP_GPIO_9
PWM_FAULTB	GPIO_26	ULP_GPIO_5 / ULP_GPIO_10
PWM_SLP_EVENT_TRIG		ULP_GPIO_8
PWM_TMR_EXT_TRIG_1	GPIO_27 / GPIO_51	ULP_GPIO_6 / ULP_GPIO_11
PWM_TMR_EXT_TRIG_2	GPIO_28 / GPIO_54	ULP_GPIO_1 / ULP_GPIO_7
PWM_TMR_EXT_TRIG_3	GPIO_29 / GPIO_55	ULP_GPIO_8
PWM_TMR_EXT_TRIG_4	GPIO_30 / GPIO_50	ULP_GPIO_9
QEI Interface		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
QEI_DIR	GPIO_11 / GPIO_28 / JTAG_TDO_SWO / GPIO_49 / GPIO_57	ULP_GPIO_7 / ULP_GPIO_11

QEI_IDX	GPIO_8 / GPIO_25 / JTAG_TCK_SWCLK/ GPIO_46 / GPIO_52	ULP_GPIO_0 / ULP_GPIO_4 / ULP_GPIO_8
QEI_PHA	GPIO_9 / GPIO_26 / JTAG_TDI / GPIO_47 / GPIO_53	ULP_GPIO_1 / ULP_GPIO_5 / ULP_GPIO_9
QEI_PHB	GPIO_10 / GPIO_27 / JTAG_TMS_SWDIO / GPIO_48 / GPIO_56	ULP_GPIO_6 / ULP_GPIO_10
USART0		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
USART0_CLK	GPIO_8 / GPIO_25 / GPIO_52	ULP_GPIO_0
USART0_CTS	GPIO_6 / GPIO_26 / GPIO_56	ULP_GPIO_6
USART0_RTS	GPIO_9 / GPIO_28 / GPIO_53	ULP_GPIO_5
USART0_DCD	GPIO_12 / GPIO_29	
USART0_DSR	GPIO_11 / GPIO_57	
USART0_DTR	GPIO_7	
USART0_RI	GPIO_27 / GPIO_46	ULP_GPIO_4
USART0_RS485_DE	GPIO_29 / GPIO_51	ULP_GPIO_7 / ULP_GPIO_11
USART0_RS485_EN	GPIO_27 / GPIO_49	ULP_GPIO_5 / ULP_GPIO_9
USART0_RS485_RE	GPIO_28 / GPIO_50	ULP_GPIO_6 / ULP_GPIO_10
USART0_RX	GPIO_10 / GPIO_29 / GPIO_55	ULP_GPIO_1 / ULP_GPIO_6
USART0_TX	GPIO_15 / GPIO_30 / GPIO_54	ULP_GPIO_4 / ULP_GPIO_7
SCT		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
SCT_IN_0	GPIO_25	ULP_GPIO_0 / ULP_GPIO_4
SCT_OUT_0	GPIO_29	ULP_GPIO_4
SCT_OUT_1	GPIO_30	ULP_GPIO_5
UART1 INTERFACE		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
UART1_TX	GPIO_7 / GPIO_30	ULP_GPIO_5 / ULP_GPIO_9 / ULP_GPIO_11
UART1_RX	GPIO_6 / GPIO_29	ULP_GPIO_4 / ULP_GPIO_8 / ULP_GPIO_10
UART1_CTS	GPIO_11 / GPIO_28 / GPIO_51	ULP_GPIO_7 / ULP_GPIO_1 / ULP_GPIO_9
UART1_RTS	GPIO_10 / GPIO_27 / GPIO_50	ULP_GPIO_6 / ULP_GPIO_0 / ULP_GPIO_8
UART1_RS485_EN	GPIO_12 / GPIO_26	ULP_GPIO_0
UART1_RS485_RE	GPIO_8	ULP_GPIO_1 / ULP_GPIO_10
UART1_RS485_DE	GPIO_9	ULP_GPIO_2 / ULP_GPIO_11
M4SS TRACE		

IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
M4SS_TRACE_CLKIN	GPIO_6 / GPIO_15 / GPIO_46 / GPIO_52	
M4SS_TRACE_CLK	GPIO_7 / GPIO_47 / GPIO_53	
M4SS_TRACE_D0	GPIO_8 / GPIO_48 / GPIO_54	
M4SS_TRACE_D1	GPIO_9 / GPIO_49 / GPIO_55	
M4SS_TRACE_D2	GPIO_10 / GPIO_50 / GPIO_56	
M4SS_TRACE_D3	GPIO_11 / GPIO_51 / GPIO_57	
Miscellaneous Interface		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
MCU_CLK_OUT	GPIO_11 / GPIO_12 / GPIO_15	

Note:

1. For SSI (Synchronous Serial Interface) use the combinations on SoC GPIOs from these set of GPIOs only – GPIO_8 to GPIO_15, GPIO_25 to GPIO_30, GPIO_46 to GPIO_51 and GPIO_52 to GPIO_57.
2. For GSPI (General SPI) use the combinations on SoC GPIOs from these set of GPIOs only – GPIO_6 to GPIO_15, GPIO_25 to GPIO_30, GPIO_46 to GPIO_51 and GPIO_52 to GPIO_57

6.5 Functional Description

6.5.1 Digital Functions

Pin Name	Direction	Description
GSPI (General SPI) Interface		
GSPI_CLK	Output	Output Clock from the GSPI primary to external secondary
GSPI_CS0 to GSPI_CS2	Output	Active low chip select. GSPI primary can select a maximum of 3 secondaries.
GSPI_MISO	Input	Input data to primary from external secondaries
GSPI_MOSI	Output	Output data from primary to external secondary
I2C (Inter-integrated Circuit) Interface		
I2C0_SCL I2C1_SCL ULP_I2C_SCL	Inout	I2C Serial Clock
I2C0_SDA I2C1_SDA ULP_I2C_SDA	Inout	I2C Serial Data
2 Channel I2S (Inter-IC Sound) Interface		

Pin Name	Direction	Description
I2S0_CLK ULP_I2S_CLK	Output/ Input	I2S Clock Output in Primary Mode and Input in Secondary Mode
I2S0_WS ULP_I2S_WS	Output/ Input	Active high I2S Word Select Output in Primary Mode and Input in Secondary Mode
I2S0_DIN_0 to I2S0_DIN_1 ULP_I2S_DIN	Input	I2S Input Data
I2S0_DOUT_0 to I2S0_DOUT_1 ULP_I2S_DOUT	Output	I2S Output Data
QSPI (Quad SPI) Interface		
MCU_QSPI_CLK	Output	Output clock to the external SPI secondary.
MCU_QSPI_CSN0 to MCU_QSPI_CSN1	Output	Active Low Chip Select to select a maximum of two secondaries.
MCU_QSPI_D0 to MCU_QSPI_D7	Inout	QSPI Data. Supports both QUAD and OCTA Data. In Quad Mode, only Bits M4SS_QSPI_D0 to M4SS_QSPI_D3 are valid. In Octa Mode, all the bits are valid
QSPI_PSRAM		
M4SS_PSRAM_CLK	Output	Output clock to the external PSRAM.
M4SS_PSRAM_CSN0	Output	Active Low Chip Select to select a maximum of two secondaries.
M4SS_PSRAM_D0 to M4SS_PSRAM_D3	Inout	QSPI Data. Supports QUAD Data only. In Quad Mode, only Bits M4SS_QSPI_D0 to M4SS_QSPI_D3 are valid.
MCPWM (Pulse Width Modulation) Interface		
PWM_xH	Output	PWM output signals. The output pins are grouped in pairs, to facilitate driving the low side and high side of a power half-bridge. x = 0,1,2,3
PWM_xL	Output	
PWM_FAULTA	Input	External fault signal A
PWM_FAULTB	Input	External fault signal B
PWM_SLP_EVENT_TRIG	Output	Special event trigger for synchronizing analog to digital conversions.
PWM_TMR_EXT_TRIG_1 to PWM_TMR_EXT_TRIG_4	Input	External trigger for base timers to increment. Each Channel has separate trigger input.
QEI (Quadrature Encode Interface)		
QEI_DIR	Output	Position counter direction. ‘1’ means counter direction is positive. ‘0’ means counter direction is negative.
QEI_IDX	Input	QE Index. Index pulse occurs once per mechanical revolution and is used as a reference to indicate an absolute position.
QEI_PHA	Input	QE Phase A input
QEI_PHB	Input	QE Phase B input
SCT (State Configurable Timer) Interface		
SCT_IN_0	Input	Timer input event
SCT_OUT_0 to SCT_OUT_1	Output	Timer output event
SSI (Synchronous Serial Interface) Primary		
SSI_MST_CLK ULP_SSI_CLK	Output	Output clock from SSI Primary

Pin Name	Direction	Description
SSI_MST_CS0 to SSI_MST_CS3 ULP_SSI_CS0 to ULP_SSI_CS2	Output	Active Low Chip select
SSI_MST_DATA0 to SSI_MST_DATA3	Inout	Single Bit Mode: DATA0 = Output Data, DATA1 = Input Data Quad Bit Mode: Bidirectional Data
ULP_SSI_DOUT	Output	Primary Output Data
ULP_SSI_DIN	Input	Primary Input Data
SSI (Synchronous Serial Interface) Secondary		
SSI_SLV_CLK	Input	Input clock to SSI Secondary
SSI_SLV_CS	Input	Active Low Chip select
SSI_SLV_MISO	Output	Secondary Output Data
SSI_SLV_MOSI	Input	Secondary Input Data
SYSRTC (System Real-Time Clock) Interface		
SYSRTC_PRS_IN_G0	Input	Group 0 input to trigger capture operation
SYSRTC_PRS_IN_G1	Input	Group 1 input to trigger capture operation
SYSRTC_PRS_OUT_G0_0	Output	Group 0 compare 0 match interrupt
SYSRTC_PRS_OUT_G0_1	Output	Group 0 compare 1 match interrupt
SYSRTC_PRS_OUT_G1_0	Output	Group 1 compare 0 match interrupt
SYSRTC_PRS_OUT_G1_1	Output	Group 1 compare 1 match interrupt
UART (Universal Asynchronous Receiver Transmitter) Interface		
UART1_CTS, ULP_UART_CTS	Input	Active low Clear to Send
UART1_RTS, ULP_UART_RTS	Output	Active low Request to Send
UART1_RS485_DE	Output	Driver Enable. Polarity is programmable.
UART1_RS485_EN	Output	Active High RS485 Enable
UART1_RS485_RE	Output	Receiver Enable. Polarity is programmable.
UART1_RX, ULP_UART_RX	Input	Serial Input
UART1_TX, ULP_UART_TX	Output	Serial Output
USART (Universal Synchronous Asynchronous Receiver Transmitter) Interface		
USART0_CLK	Inout	Serial interface clock
USART0_CTS	Input	Active low Clear to Send
USART0_RTS	Output	Active low Request to Send
USART0_DCD	Input	Active low Data Carrier Detect
USART0_DSR	Input	Active low Data Set Ready
USART0_DTR	Output	Active low Data Terminal Ready
USART0_RI	Input	Active low Ring Indicator
UART0_RS485_DE	Output	Driver Enable. Polarity is programmable.
UART0_RS485_EN	Output	Active High RS485 Enable

Pin Name	Direction	Description
UART0_RS485_RE	Output	Receiver Enable. Polarity is programmable.
USART0_RX	Input	Serial Input
USART0_TX	Output	Serial Output
Timers Interrupt Interface		
Timer0, Timer1,Timer2	Output	Active-high interrupts from Timers
Miscellaneous Interface		
MCU_CLK_OUT	Output	All the Clocks that are used by Cortex-M4 SoC are multiplexed and connected on this pin
ULP_EGPIO_*	Inout	ULP GPIO's controlled by Cortex M4 Processor. * represents 0,1,2,4,5,6,7,8,9,10,11
AUX_ULP_TRIG_0, AUX_ULP_TRIG_1	Input	External trigger to ADC.
NWP_GPIO_*	Inout	NWP GPIO's controlled by Network Wireless Processor. * represents 6,8,9,10,11,12,15,46,47,48,49,50,51
UULP VBAT Pin Interface		
MCU_GPIO0/1/2/3_WAKEUP	Input	GPIOs that can be used as Wakeup interrupt to MCU while in Retention or Deep sleep mode
NWP_GPIO0/1_WAKEUP	Input	GPIOs that can be used to wake the Network Processor
MCU_GPIO_TOGGLE	Input	Input pulse counting function
TRACE Pins		
M4SS_TRACE_CLKIN	Input	
M4SS_TRACE_CLK	Output	
M4SS_TRACE_D0	Output	Trace Packet, bit 0.
M4SS_TRACE_D1	Output	Trace Packet, bit 1
M4SS_TRACE_D2	Output	Trace Packet, bit 2
M4SS_TRACE_D3	Output	Trace Packet, bit 3

6.5.2 Analog Functions

Pin Name	Direction	Description
ADC Interface		
ADCP[0] - ADCP[18]	Input	The 18 single ended input channels that are multiplexed onto the ADCP positive input These can be used alone for single-ended measurements, or selected with ADCN inputs for differential measurements
ADCN[0] - ADCN[8]	Input	The 9 channels that are multiplexed onto the ADCN negative input. These are used together with ADCP inputs for differential measurements
DAC Interface		
DAC0, DAC1	Output	Possible output pins from the internal DAC
OpAmp Interface		

Pin Name	Direction	Description
OPAMPxyz	Input	Multiplexed inputs of the three OpAmps. xyz denote the OpAmp number, the terminal and the multiplexing on that pin of the OpAmp x = OpAmp number (1, 2 or 3) y = P or N terminal of OpAmp z = 0, 1, 2, 3, 4, 5 (Multiplexing at OpAmp input pin). Note that OPAMP1P is available at 6 locations, OPAMP2P, 3P and 1N are available at 2 locations each and OPAMP2N and 3N pins are available at only one location
OPAMP1OUT0/1, OPAMP2/3OUT0	Output	Outputs of the three OpAmps. Note that OPAMP1 output is available at two possible pin locations whereas OPAMP2 and 3 outputs are available at a fixed pin
Comparator Interface		
COMPx_yz		Multiplexed inputs of the two Comparators. xyz denote the Comparator number, the terminal and the multiplexing on that pin of the Comparator x = Comparator number (1 or 2) y = P or N terminal of OpAmp z = 0, 1 (Multiplexing at Comparator Input pin). Note that each input pin of both comparators is available on two possible GPIO pins.

7. Electrical Specifications

7.1 Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions beyond those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at https://www.silabs.com/about-us/quality.

Table 7.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature	T_{store}		-40	—	125	°C
Maximum junction temperature	T_{j_max}		—	—	125	°C
Always-on VBATT supply to the UULP Domains	$V_{UULP_VBATT_1}$		-0.5	—	3.63	V
Always-on VBATT supply to the UULP Domains	$V_{UULP_VBATT_2}$		-0.5	—	3.63	V
Always-on VBATT Power supply to the RF	V_{RF_VBATT}		-0.5	—	3.63	V
Power supply for the on-chip Buck	$V_{VINBCKDC}$		-0.5	—	3.63	V
Power supply for SoC LDO	$V_{VINLDOSOC}$		-0.5	—	1.8	V
Power supply for 1.8 V LDO	$V_{VINLDO1P8}$		-0.5	—	3.63	V
I/O supply for In-Package Flash/PSRAM	$V_{FLASH_IO_VDD}$		-0.5	—	3.63	V
I/O supplies for GPIOs	$V_{IO_VDD_1}$		-0.5	—	3.63	V
I/O supplies for GPIOs	$V_{IO_VDD_2}$		-0.5	—	3.63	V
I/O supplies for GPIOs	$V_{IO_VDD_3}$		-0.5	—	3.63	V
I/O supplies for ULP GPIOs	$V_{ULP_IO_VDD}$		-0.5	—	3.63	V
DC voltage on any I/O pin [1]	V_{IO_PIN}		-0.5	—	VDD + 0.5	V
Current per I/O pin	I_{IOMAX}	Sink	—	—	100	mA
		Source	—	—	100	mA
Power supply for the 2.4 GHz RF Power Amplifier	V_{PA2G_AVDD}		-0.5	—	3.63	V
Power supply for the 2.4 GHz RF and AFE	V_{RF_AVDD}		-0.5	—	1.98	V
Power supply for the digital core	V_{C_VDD}		-0.5	—	1.21	V
Total average max current into chip	I_{Pmax}		—	—	500	mA

Note:

1. VDD = I/O supply domain pin. Refer to pin description tables for supply domain associated with each I/O.

7.2 Recommended Operating Conditions

Note: The device may operate continuously at the maximum allowable ambient $T_{ambient}$ rating as long as the maximum junction $T_{junction(max)}$ is not exceeded. For an application with significant power dissipation, the allowable $T_{ambient}$ may be lower than the maximum $T_{ambient}$ rating. $T_{ambient} = T_{junction(max)} - (\Theta_{JA} \times \text{Power Dissipation})$. Refer to the Thermal Characteristics table for Θ_{JA}.

Table 7.2. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient temperature	$T_{ambient}$		-40	25	85	°C
Junction temperature	$T_{junction}$		—	—	105	°C
Power supply for UULP_VBATT_1, UULP_VBATT_2, and RF_VBATT [1]	V_{VBATT}	3.3 V nominal operation	2.97	3.3	3.63	V
		1.8 V nominal operation	1.71	1.8	1.98	V
Power supply for the on-chip Buck [1]	$V_{VINBCKDC}$	3.3 V nominal operation	2.97	3.3	3.63	V
		1.8 V nominal operation	1.71	1.8	1.98	V
Power supply for 1.8 V LDO [1]	$V_{VINLDO1P8}$	Regulation mode	2.97	3.3	3.63	V
		Bypass mode	1.71	1.8	1.98	V
Power supply for SoC LDO	$V_{VINLDOSOC}$		1.35	1.45	1.55	V
I/O supply for In-Package Flash/PSRAM	$V_{FLASH_IO_VDD}$		1.71	1.8	1.98	V
Power supply for the 2.4 GHz RF Power Amplifier	V_{PA2G_AVDD}		2.97	3.3	3.63	V
Power supply for IO_VDD_1 [1]	$V_{IO_VDD_1}$	3.3 V nominal operation	2.97	3.3	3.63	V
		1.8 V nominal operation	1.71	1.8	1.98	V
Power supply for IO_VDD_2 [1]	$V_{IO_VDD_2}$	3.3 V nominal operation	2.97	3.3	3.63	V
		1.8 V nominal operation	1.71	1.8	1.98	V
Power supply for IO_VDD_3 [1]	$V_{IO_VDD_3}$	3.3 V nominal operation	2.97	3.3	3.63	V
		1.8 V nominal operation	1.71	1.8	1.98	V
Power supply for ULP_IO_VDD [1]	$V_{ULP_IO_VDD}$	3.3 V nominal operation	2.97	3.3	3.63	V
		1.8 V nominal operation	1.71	1.8	1.98	V

Note:

1. Supplies can operate at a nominal 3.3 V or 1.8 V level independent of the other supplies in the system.

7.3 DC Characteristics

7.3.1 RESET_N and POC_IN Pins

Table 7.3. RESET_N and POC_IN Pins

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High level input voltage	V_{IH}	RESET_N pin, UULP_VBATT_2 = 3.3 V	0.8 * UULP_VBATT_2	—	—	V
		RESET_N pin, UULP_VBATT_2 = 1.8 V	1.17	—	—	V
		POC_IN pin, UULP_VBATT_1 = 3.3 V	2.76	—	—	V
		POC_IN pin, UULP_VBATT_1 = 1.8 V	1.38	—	—	V
Low level input voltage	V_{IL}	RESET_N pin, UULP_VBATT_2 = 3.3 V	—	—	0.3 * UULP_VBATT_2	V
		RESET_N pin, UULP_VBATT_2 = 1.8 V	—	—	0.63	V
		POC_IN pin, UULP_VBATT_1 = 3.3 V	—	—	1.10	V
		POC_IN pin, UULP_VBATT_1 = 1.8 V	—	—	0.24	V

7.3.2 Power On Control (POC) and Reset

There are three signals involved in power-on control and reset of the device:

- POC_IN: When pulled low, POC_IN will reset all of the internal blocks in the device. The POC_IN signal can be controlled either by external circuitry, by POC_OUT, or both.
- RESET_N: RESET_N is an open-drain signal which will be pulled low during a chip reset. It is released after POC_IN is high. RESET_N should be connected to an RC circuit to fulfill the timing requirements shown in Figure 7.1. Power Up Sequence.
- POC_OUT: The POC_OUT signal is the output of the internal blackout supply monitor. POC_OUT is distributed to all I/O cells to prevent the I/O cells from powering up in an undesired configuration and is also used inside the IC to place the IC in a safe state until a valid supply is available for proper operation. During power up, POC_OUT stays low until the UULP_VBATT_1 reaches 1.6 V. After the VBATT supply exceeds 1.6 V, POC_OUT becomes high and normal operation begins. If VBATT becomes lower than the blackout threshold voltage, POC_OUT will return low. POC_OUT can be used to provide chip reset by connecting to POC_IN in a loopback configuration.

The recommended schematic for the reset signals is shown in 8.1 Schematics.

Figure 7.1. Power Up Sequence shows the signal timing when POC_OUT, POC_IN, and RESET_N are connected per the recommended schematic. The POC_IN-to-RESET_N delay will occur when POC_IN transitions from low to high. VBATT in the figure refers to the connection of UULP_VBATT_1 and UULP_VBATT_2 (connected together in the schematic).

In this configuration the system only has to control the supply (VBATT) during power-up and power down and need not control POC_IN externally. On power-up the chip will be reset internally. The power-down sequence will follow VBATT and external control of POC_IN is not required.

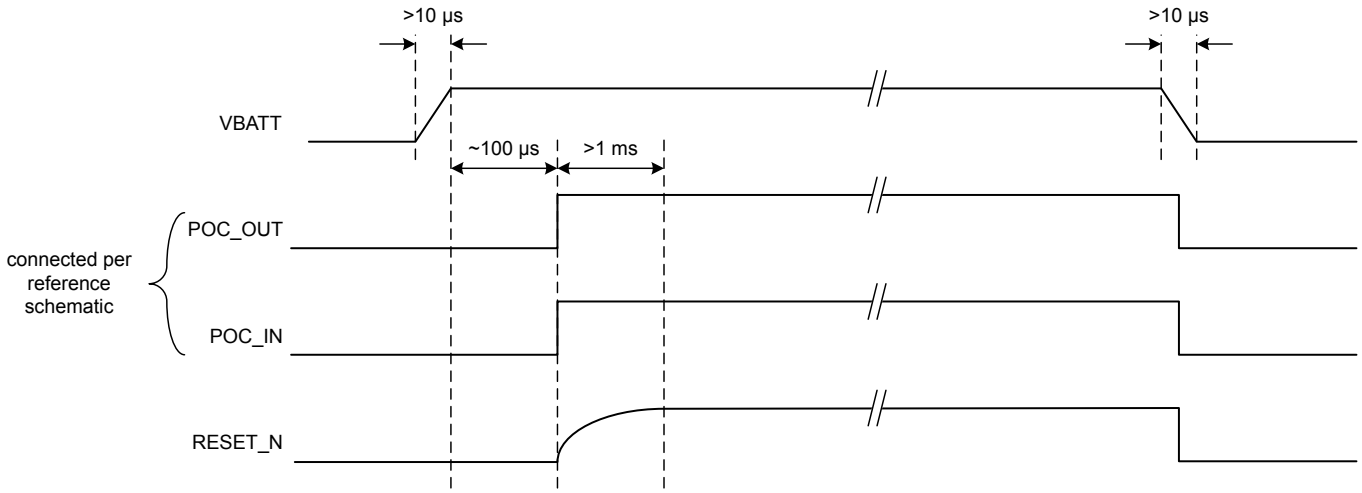


Figure 7.1. Power Up Sequence

If the chip is to be reset from an external host device while powered up, the POC_IN signal should be pulled low for at least 10 ms as shown in Figure 7.2. External Reset via POC_IN. Upon release of POC_IN, the POC_IN-to-RESET_N delay will occur.

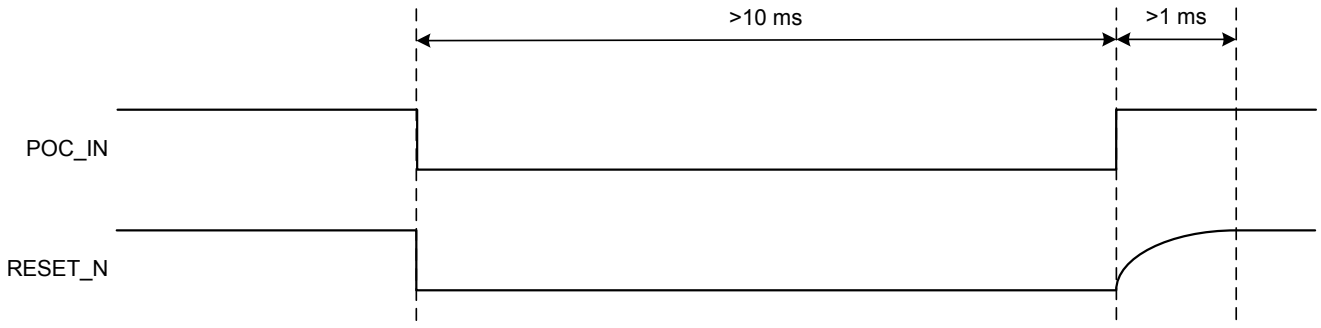


Figure 7.2. External Reset via POC_IN

In the above timing diagrams, it is assumed that all supplies including VBATT are connected together. If they are not connected together and independently controlled, then the guidance below must be followed.

- **Case1**: POC is looped back and there is no external control for POC_IN
  - All supplies can be enabled at the same time, if possible
  - If supplies cannot be enabled at the same time, the VBATT supplies should be powered up first and all other supplies should be powered on at least 1 ms before RESET_N is high. The RC circuit controlling RESET_N must be adjusted to provide the appropriate delay.
  - While powering down, supplies can be powered off simultaneously, or with VBATT the last to be disabled.
- **Case2**: POC is looped back and there is external control for POC_IN during power-up / power-down.
  - All supplies can be enabled at the same time, or VBATT may be enabled before other supplies.
  - POC_IN should be kept low for at least 600 us after all the supplies have settled.
  - On power-down, POC_IN can be driven low before disabling the supplies. Supplies can be powered off simultaneously, or with VBATT the last to be disabled.

7.3.3 Blackout Monitor

The blackout comparator is enabled by default upon power up. Blackout is typically asserted when the UULP_VBATT_1 or UULP_VBATT_2 (VBATT) supply goes lower than 1.6 V (see table below), and it is de-asserted when VBATT supply goes higher than 1.625 V. The blackout monitor circuit will reset the device when POC_OUT is connected to POC_IN as recommended.

The blackout monitor will be disabled after power up. The functionality should be enabled by the SoC firmware if required in the system. The blackout monitor block should be enabled to monitor the VBATT voltage only in high power modes. In low power modes battery level detection can be implemented using the Nano-Power Brownout detection comparator.

When the system is in low power mode, the blackout comparator is automatically enabled upon a brownout event.

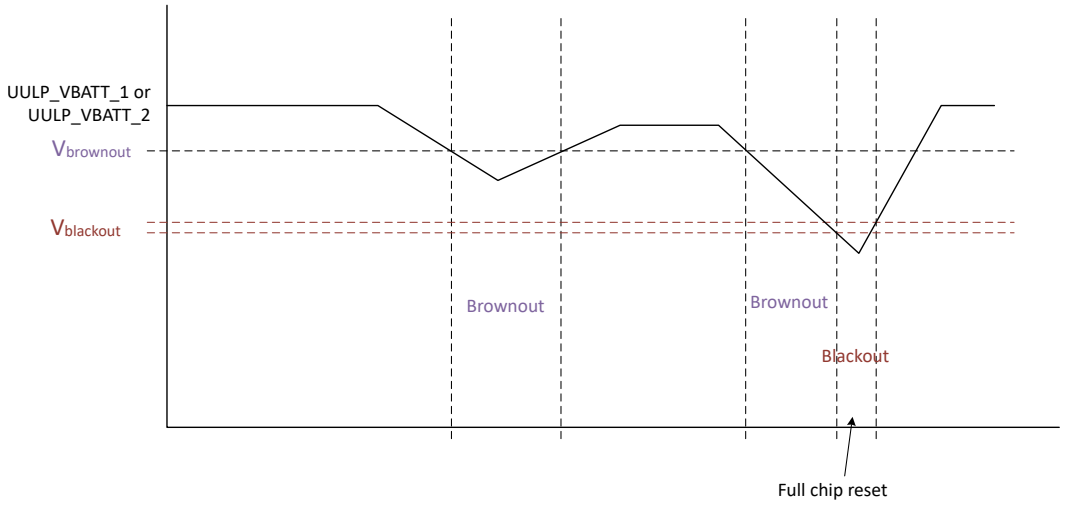


Figure 7.3. Blackout Monitor

Table 7.4. Blackout Monitor Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VBATT voltage at which the Blackout monitor resets the IC	$VTL_{blackout}$		—	1.56	1.65	V
VBATT voltage at which the Blackout monitor releases the IC from reset	$VTH_{blackout}$		—	1.59	1.675	V

7.3.4 Nano Power Comparator and Brown Out Detection (BOD)

The Nano Power comparator subsystem consists of a sampled comparator, reference buffer and resistor bank.

Features

- Battery voltage measurement
- Brownout detection
- Three button wakeup is supported using single VOLT_SENSE signal

Table 7.5. Nano Power BOD Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Battery status accuracy	V_{batt_status}		—	+/-100	—	mV
Brownout detection accuracy	V_{BOD}		—	+/-100	—	mV

7.3.5 ULP Regulators

ULP (Ultra Low Power) regulators are used to power low power Always-ON digital and analog power management circuitry inside the IC. The ULP regulators include two high power LDOs, a Low power LDO, and a switched capacitor DC-DC regulator. These regulators operate directly off of UULP_VBATT_2.

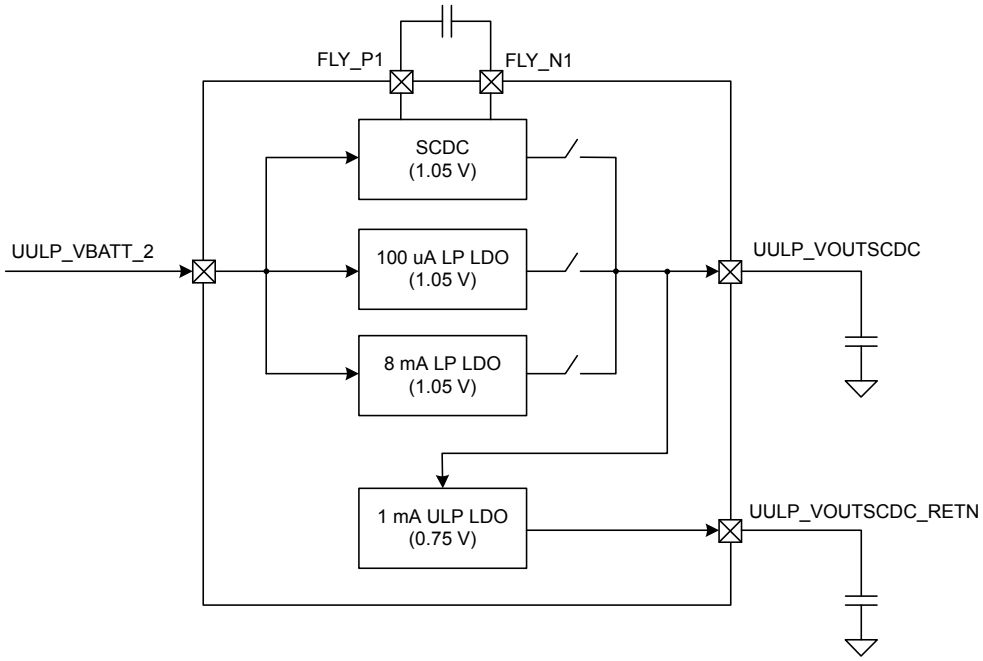


Figure 7.4. Block Diagram

7.3.5.1 SC-DCDC

SC-DCDC stands for a Switched Capacitor DC-DC regulator. It operates from UULP_VBATT_2 and generates a programmable output voltage. It has two major modes of operation, viz. LDO mode and DC-DC mode. And further each of these modes have a low power and high power option.

The IC starts up in the LDO mode and later switches to DC-DC Mode.

Table 7.6. SC-DCDC - Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage Range [1]	V_{IN}		1.71	—	3.63	V
Output Voltage at UULP_VOUTSCDC	$V_{OUTSCDC}$		—	1.05	—	V
Output Voltage at UULP_VOUTSCDC_RETN	$V_{OUTRETN}$		—	0.75	—	V

Note:

1. The ULP regulator switches from SC-DCDC mode to LDO mode for V_{in} lower than 2.4 V

7.3.6 Power Management Unit

This section describes and specifies the Power Management Unit solution for the mixed signal System on Chip (SoC).

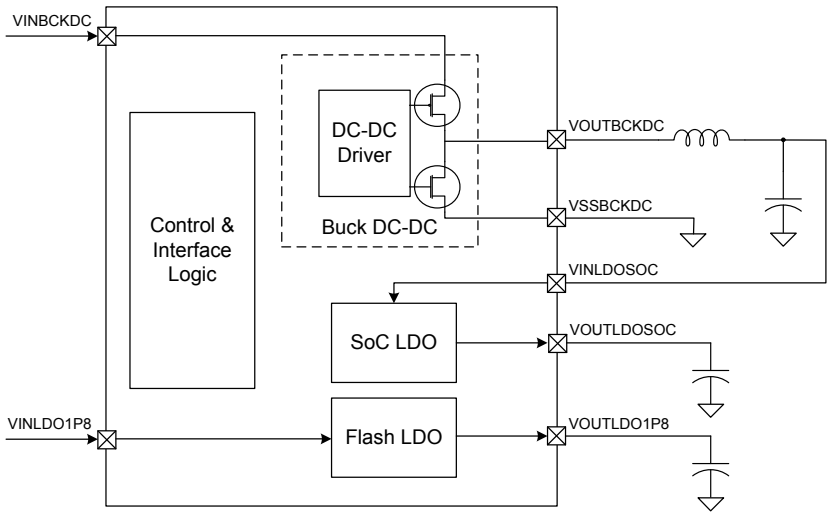


Figure 7.5. Power Management Block Diagram

Power Management Unit

The major features are

- 1.45 V DCDC switching converter
- 1.15 V LDO for SOC digital supply
- 1.8 V LDO for Flash supply

7.3.6.1 DCDC Switching Converter

- Power save mode at light load currents.
- 100% duty cycle for lowest dropout.
- Soft start

Table 7.7. DCDC Switching Converter Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Supply Voltage (VINBCKDC)	V_{in}		1.71	3.3	3.63	V
Output Voltage Range (VOUTBCKDC)	V_{out}		1.35	1.45	1.6	V
Load current	I_{load}	Active mode	—	—	170	mA

7.3.6.2 SoC LDO Electrical Specifications

Table 7.8. SoC LDO Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Supply Voltage (VINLDOSOC)	V_{in}		1.35	1.45	1.55	V
Output Voltage Range (VOUTLDOSOC)	V_{out}		1.05	1.15	1.20	V
Load current	I_{load}		—	—	100	mA

7.3.6.3 Flash LDO Electrical Specifications - Regulation Mode

Table 7.9. Flash LDO Electrical Specifications - Regulation Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Supply Voltage (VINLDO1P8)	V_{in}	Flash LDO in Regulation Mode	2.97	3.3	3.63	V
Output Voltage Range (VOUTLDO1P8)	V_{out}		1.75	1.88	1.95	V
Load current	I_{load}		—	—	48	mA
Line Regulation	REG_{line}	V_{in} Changed from 2.97 V to 3.63 V	—	—	0.6	%
Load Regulation	REG_{load}	I_{load} changed from 5 µA to 48 mA	—	—	3	%

7.3.6.4 Flash LDO Electrical Specifications - Bypass Mode

Table 7.10. Flash LDO Electrical Specifications - Bypass Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Supply Voltage (VINL-DO1P8) [1]	V_{in}	Flash LDO in Bypass Mode	1.71	1.8	1.98	V
On Resistance between V_{in} and V_{out}	R_{on}		—	0.87	—	Ω
Voltage across the VIN and V_{out} pin of the Flash LDO	V_{drop}	Load = 48 mA (Max)	—	42	70	mV

Note:

1. For higher load currents, the input supply should be increased to compensate the V_{drop} across the R_{on} of the pass transistor of Flash LDO.

7.3.7 Thermal Characteristics

Table 7.11. Thermal Characteristics

Package	Board	Parameter	Symbol	Test Condition	Value	Unit
84 Pin DR-QFN (7 mm x 7 mm)	JEDEC - High Thermal Cond. (2s2p)[1]	Thermal Resistance, Junction to Ambient	Θ_{JA}	Still Air	30	°C/W

Note:

1. PCB: 76.2 mm x 114.3 mm x 1.6 mm (JEDEC High Effective); 2s2p = 2 signals, 2 planes.
2. The absolute maximum device current when transmitting at highest transmit power will not exceed 400 mA.

7.3.8 Digital I/O Signals

Table 7.12. Digital I/O Signals

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High level input voltage	V_{IH}	IO_VDDx = 3.3 V	2	—	—	V
		IO_VDDx = 1.8 V	1.17	—	—	V
Low level input voltage	V_{IL}	IO_VDDx = 3.3 V	—	—	0.8	V
		IO_VDDx = 1.8 V	—	—	0.63	V
Low level output voltage	V_{OL}		—	—	0.4	V
High level output voltage	V_{OH}		IO_VDDx - 0.4	—	—	V
Low level output current (programmable)	I_{OL}	GPIO_* and ULP_GPIO_* pins	2	4	12	mA
		UULP_GPIO_* pins	1	—	2	mA
High level output current (programmable)	I_{OH}	GPIO_* and ULP_GPIO_* pins	2	4	12	mA
		UULP_GPIO_* pins	1	—	2	mA
Pull-up resistance	R_{PU}	GPIO_* and ULP_GPIO_* pins	—	53	—	kΩ
Pull-down resistance	R_{PD}	GPIO_* and ULP_GPIO_* pins	—	63	—	kΩ
Leakage current	I_{LEAK_IO}	IO_VDDx = 1.8 V	—	+/-0.1	—	µA
		IO_VDDx = 3.3 V	—	+/-0.1	—	µA
		IO_VDDx = 3.3 V, T_A = 85 °C	—	—	+/-0.5	µA

7.3.8.1 Open-Drain I2C Pins

Table 7.13. Open-Drain I2C Pins

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High level input voltage	V_{IH}		0.7 * IO_VDDx	—	—	V
Low level input voltage	V_{IL}		—	—	0.3 * IO_VDDx	V

7.4 AC Characteristics

7.4.1 Clock Specifications

SiWG917 chipsets include the following clock options:

- Low frequency clock options for sleep manager and RTC
  - 32.768 kHz on-chip crystal oscillator for an external crystal at pins XTAL_32KHZ_P and XTAL_32KHZ_N. **Required for MCU timing accuracy and all power-sensitive Wi-Fi, BLE, and Coex use cases.**
  - Internal 32 kHz RC oscillator. Suitable only for applications with low timing accuracy requirements, and no critical timing. Typical accuracy is +/- 1.2%.
- High frequency clock options
  - 40 MHz on-chip crystal oscillator with external crystal at XTAL_IN and XTAL_OUT pins for RF reference
  - Internal RC oscillator, used during device boot-up
  - Internal high-frequency ring oscillator

7.4.1.1 Low Frequency Clocks

Low-frequency clock selection can be done through software. The RC oscillator clock is not suited for high timing accuracy applications and may increase overall system current consumption in duty-cycled power modes.

Table 7.14. 32 kHz RC Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillator Frequency	f_{osc}		—	32	—	kHz
Frequency variation across temperature	f_{osc_Acc}		—	1.2	—	%

32.768 kHz XTAL Oscillator

There is an option to use 32.768 kHz low-frequency XTAL clock with a crystal attached to the XTAL_32KHZ_P and XTAL_32KHZ_N pins. Below are the recommended external crystal specs that need to connect to the internal xtal oscillator.

Table 7.15. 32.768 kHz XTAL Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillator Frequency[1]	f_{osc}		—	32.768	—	kHz
Drive Level	Drive		0.5	—	—	uW
Frequency Variation with Temp and Voltage[2]	f_{osc_Acc}		—	+/-250	—	ppm
Equivalent series resistance	ESR		—	—	80	kΩ
Load capacitance range	C_L		4	—	12.5	pF

Note:

1. XTAL Oscillator specified for fundamental mode, parallel resonant crystal
2. Combined frequency offset must be below this limit, including temperature induced changes, tolerance, and the variance of load capacitances (load capacitor and parasitic trace impedance)

7.4.1.2 40 MHz Clock

The 40 MHz internal oscillator mode can be used by connecting a 40 MHz crystal between the pins XTAL_P and XTAL_N. Load capacitance is integrated inside the chipset and calibrated and the calibrated value can be stored in eFuse using calibration software.

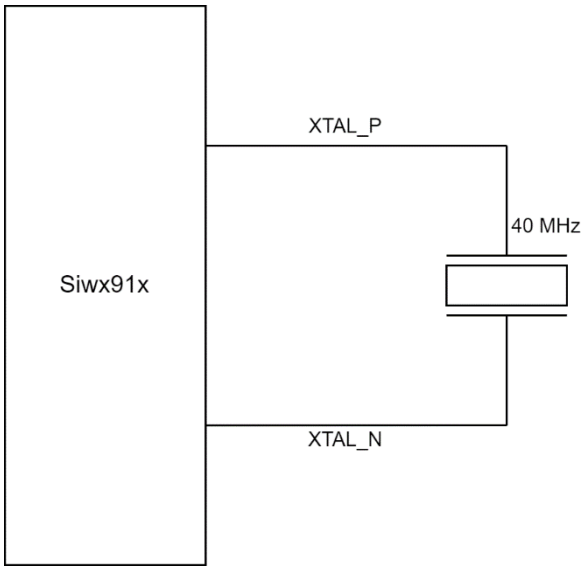


Table 7.16. 40 MHz Crystal Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillator Frequency [1]	f_{osc}		—	40	—	MHz
Drive Level	Drive		100	—	—	uW
Frequency Variation with Temp and Voltage	f_{osc_Acc}		-20	—	20	ppm
Equivalent series resistance	ESR		—	—	60	Ω
Load capacitance range	C_L		7	—	10	pF

Note:

1. Oscillator specified for fundamental mode, parallel resonant crystal.
2. Software has the default "Crystal Good Time" value for the recommended crystal part listed in Table 8.1. If a non-recommended crystal part is used, "Crystal Good time" value has to be determined as per Application Note AN1436.

7.4.2 SDIO 2.0 Secondary

7.4.2.1 Full Speed Mode

Table 7.17. SDIO 2.0 Secondary Full Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SDIO_CLK	f_{sdio_clk}		—	—	25	MHz
SDIO_DATA, SDIO_CMD input setup time	t_s		4	—	—	ns
SDIO_DATA, SDIO_CMD input hold time	t_h		1.2	—	—	ns
SDIO_DATA, clock to output delay	t_{od}		—	—	13	ns
Output Load	C_L		5	—	10	pF

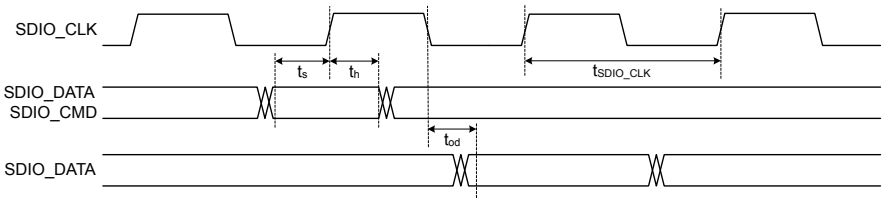


Figure 7.6. Interface Timing Diagram for SDIO 2.0 Secondary Full Speed Mode

7.4.2.2 High Speed Mode

Table 7.18. SDIO 2.0 Secondary High Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SDIO_CLK	f_{sdio_clk}		25	—	50	MHz
SDIO_DATA, input setup time	t_s		4	—	—	ns
SDIO_DATA, input hold time	t_h		1.2	—	—	ns
SDIO_DATA, clock to output delay	t_{od}		2.5	—	13	ns
Output Load	C_L		5	—	10	pF

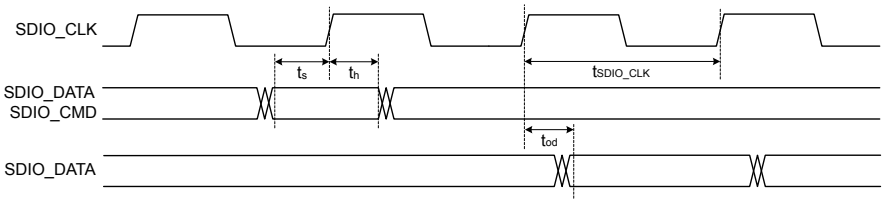


Figure 7.7. Interface Timing Diagram for SDIO 2.0 Secondary High Speed Mode

7.4.3 HSPI Secondary

7.4.3.1 Low Speed Mode

Table 7.19. HSPI Secondary Low Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
HSPI_CLK	f_{hspi}		0	—	25	MHz
HSPI_CSN to output delay	t_{cs}		—	—	7.5	ns
HSPI_CSN to input setup time	t_{cst}		4.5	—	—	ns
HSPI_MOSI, input setup time	t_s		1.4	—	—	ns
HSPI_MOSI, input hold time	t_h		1.5	—	—	ns
HSPI_MISO, clock to output delay	t_{od}		—	—	8.75	ns
Output Load	C_L		5	—	10	pF

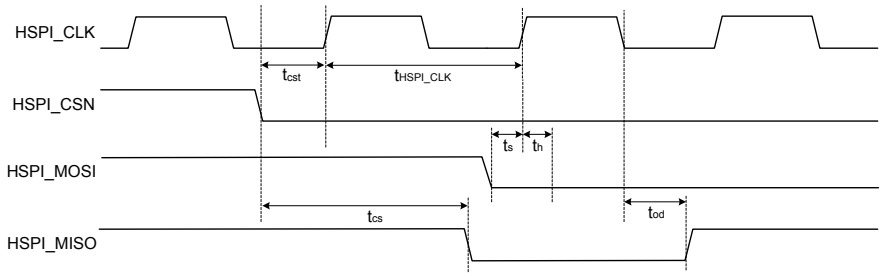


Figure 7.8. Interface Timing Diagram for HSPI Secondary Low Speed Mode

In low speed mode, HSPI_MISO data is driven on the falling edge of HSPI_CLK, and HSPI_MOSI is read on the rising edge of HSPI_CLK.

7.4.3.2 High Speed Mode

Table 7.20. HSPI Secondary High Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
HSPI_CLK	f_{hspi}		25	—	80	MHz
HSPI_CSN to output delay	t_{cs}		—	—	7.5	ns
HSPI_CSN to input setup time	t_{cst}		4.5	—	—	ns
HSPI_MOSI, input setup time	t_s		1.4	—	—	ns
HSPI_MOSI, input hold time	t_h		1.4	—	—	ns
HSPI_MISO, clock to output delay	t_{od}		1.5	—	8.75	ns
Output Load	C_L		5	—	10	pF

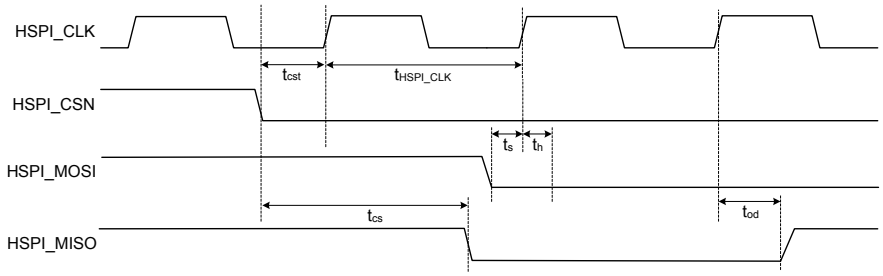


Figure 7.9. Interface Timing Diagram for HSPI Secondary High Speed Mode

In high speed mode, HSPI_MISO data is driven on the rising edge of HSPI_CLK, and HSPI_MOSI is read on the rising edge of HSPI_CLK.

7.4.3.3 Ultra High Speed Mode

Table 7.21. HSPI Secondary Ultra High Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
HSPI_CLK	f_{hspi}		80	—	100	MHz
HSPI_MOSI, input setup time	t_s		1.4	—	—	ns
HSPI_MOSI, input hold time	t_h		1.4	—	—	ns
HSPI_MISO, clock to output delay	t_{od}		1.5	—	8.75	ns
Output Load	C_L		5	—	10	pF

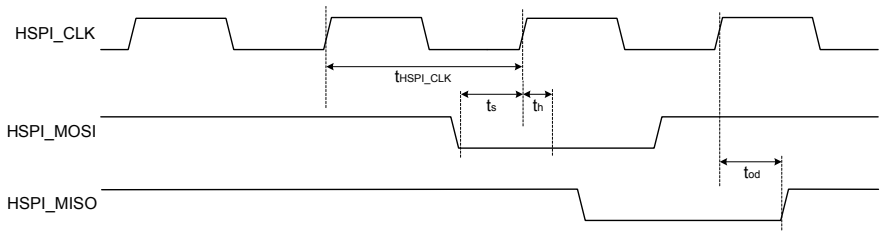


Figure 7.10. Interface Timing Diagram for HSPI Secondary Ultra High Speed Mode

In ultra high speed mode, HSPI_MISO data is driven on the rising edge of HSPI_CLK, and HSPI_MOSI is read on the rising edge of HSPI_CLK.

7.4.4 GPIO Pins

Table 7.22. GPIO Pins

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rise time	t_{rf}	Pin configured as output; SLEW = 1 (fast mode)	1	—	4	ns
Fall time	t_{ff}	Pin configured as output; SLEW = 1 (fast mode)	0.9	—	4	ns
Rise time	t_{rs}	Pin configured as output; SLEW = 0 (standard mode)	1.9	—	5	ns
Fall time	t_{fs}	Pin configured as output; SLEW = 0 (standard mode)	1.9	—	5	ns
Rise time	t_r	Pin configured as input	0.3	—	1.3	ns
Fall time	t_f	Pin configured as input	0.2	—	1.2	ns

7.4.5 In-Package Flash Memory

Table 7.23. In-Package Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Endurance	N_{endu}	Sector erase/program	10000	—	—	cycles
		Page erase/program, page in large sector	10000	—	—	cycles
		Page erase/program, page in small sector	10000	—	—	cycles
Retention time	t_{ret}	Powered	10	—	—	years
		Unpowered	10	—	—	years
Block Erase time (32 KB)	t_{er}	Page, sector or multiple consecutive sectors	—	150	1400	ms
Page programming time	t_{prog}		—	0.5	3	ms
Chip Erase time	t_{ce}		—	20	65	s

7.4.6 QSPI

7.4.6.1 Full Speed Mode (Rising Edge Sampling)

Table 7.24. QSPI Full Speed Mode (Rising Edge Sampling)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
qspi_clk	f_{qspi}		0	—	40	MHz
qspi_cs, to clock edge(this is achieved functionally)	t_{cs}		8.6	—	—	ns
qspi_miso, setup time	t_s		4	—	—	ns
qspi_miso, hold time	t_h		2.5	—	—	ns
qspi_mosi, clock to output valid	t_{od}		-2	—	2	ns
Output Load	C_L		5	—	10	pF

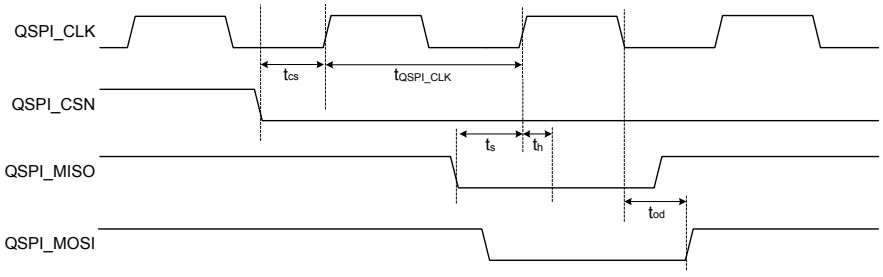


Figure 7.11. Interface Timing Diagram for QSPI Full Speed Mode (Rising Edge Sampling)

7.4.6.2 High Speed Mode (Falling Edge Sampling)

Table 7.25. QSPI High Speed Mode (Falling Edge Sampling)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
qspi_clk	f_{qspi}		40	—	80	MHz
qspi_cs, to clock edge(this is achieved functionally)	t_{cs}		4.3	—	—	ns
qspi_miso, setup time	t_s		4	—	—	ns
qspi_miso, hold time	t_h		2.5	—	—	ns
qspi_mosi, clock to output valid	t_{od}		-2	—	2	ns
Output Load	C_L		5	—	10	pF

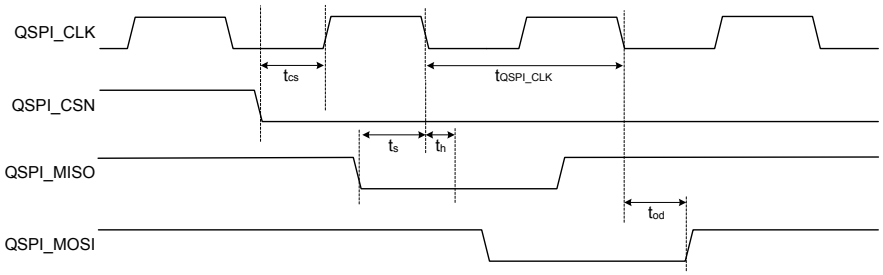


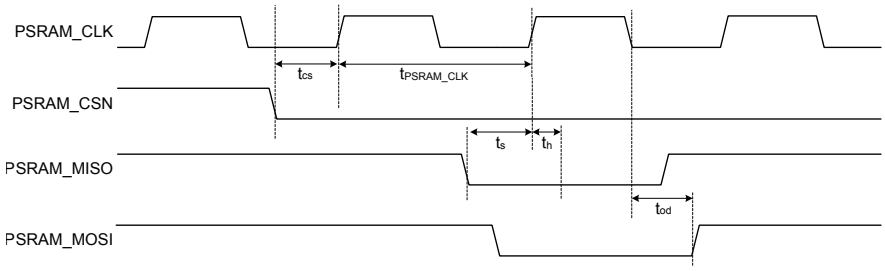
Figure 7.12. Interface Timing Diagram for QSPI High Speed Mode (Falling Edge Sampling)

7.4.7 PSRAM

7.4.7.1 Full Speed Mode (Rising Edge Sampling)

Table 7.26. PSRAM Full Speed Mode (Rising Edge Sampling)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
psram_clk	f_{psram}		0	—	40	MHz
psram_cs, to clock edge(this is achieved functionally)	t_{cs}		8.6	—	—	ns
psram_miso, setup time	t_s		4	—	—	ns
psram_miso, hold time	t_h		2.5	—	—	ns
psram_mosi, clock to output valid	t_{od}		-2	—	2	ns
Output Load	C_L		5	—	10	pF



Interface Timing Diagram for PSRAM Full Speed Mode (Rise Edge Sampling)

7.4.7.2 High Speed Mode (Falling Edge Sampling)

Table 7.27. PSRAM High Speed Mode (Falling Edge Sampling)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
psram_clk	f_{psram}		40	—	80	MHz
psram_cs, to clock edge(this is achieved functionally)	t_{cs}		4.3	—	—	ns
psram_miso, setup time	t_s		4	—	—	ns
psram_miso, hold time	t_h		2.5	—	—	ns
psram_mosi, clock to output valid	t_{od}		-2	—	2	ns
Output Load	C_L		5	—	10	pF

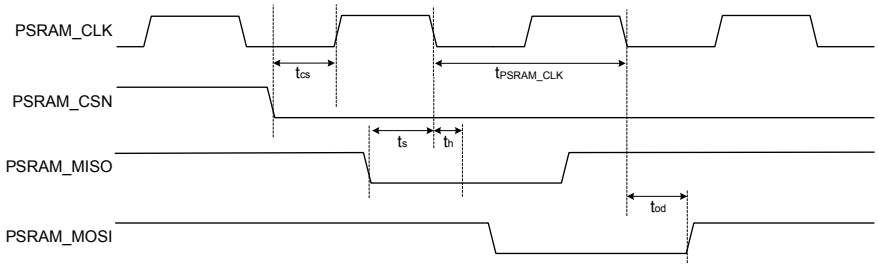


Figure 7.13. Interface Timing Diagram for PSRAM High Speed Mode (Falling Edge Sampling)

7.4.8 I2C

7.4.8.1 Standard Mode

Table 7.28. I2C Standard Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL	f_{i2c}		0	—	100	kHz
clock low period	t_{low}		4.7	—	—	µs
clock high period	t_{high}		4.0	—	—	µs
start condition, setup time	t_{sstart}		4.7	—	—	µs
start condition, hold time	t_{hstart}		4.0	—	—	µs
data, setup time	t_s		250	—	—	ns
stop condition, setup time	t_{sstop}		4.0	—	—	µs
Output Load	C_L		5	—	10	pF

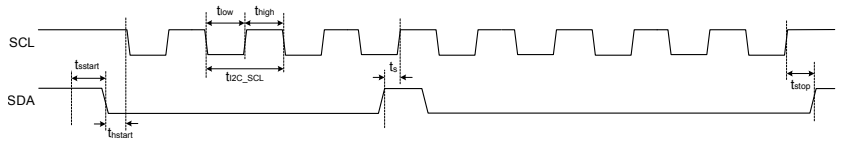


Figure 7.14. Interface Timing Diagram for I2C Standard Mode

7.4.8.2 Fast Speed Mode

Table 7.29. I2C Fast Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL	f_{i2c}		100	—	400	kHz
clock low period	t_{low}		1.3	—	—	µs
clock high period	t_{high}		0.6	—	—	µs
start condition, setup time	t_{sstart}		0.6	—	—	µs
start condition, hold time	t_{hstart}		0.6	—	—	µs
data, setup time	t_s		100	—	—	ns
stop condition, setup time	t_{sstop}		0.6	—	—	µs
Output Load	C_L		5	—	10	pF

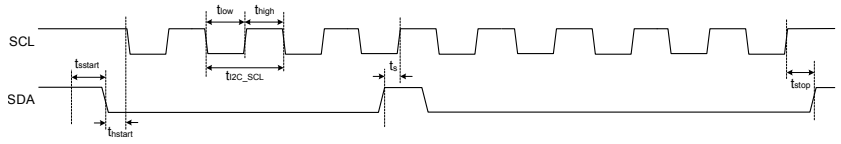


Figure 7.15. Interface Timing Diagram for I2C Fast Speed Mode

7.4.8.3 Fast Mode Plus

Table 7.30. I2C Fast Mode Plus

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL	f_{i2c}		400	—	1000	kHz
clock low period	t_{low}		0.5	—	—	µs
clock high period	t_{high}		0.26	—	—	µs
start condition, setup time	t_{sstart}		0.26	—	—	µs
start condition, hold time	t_{hstart}		0.26	—	—	µs
data, setup time	t_s		50	—	—	ns
stop condition, setup time	t_{sstop}		0.26	—	—	µs
Output Load	C_L		5	—	10	pF

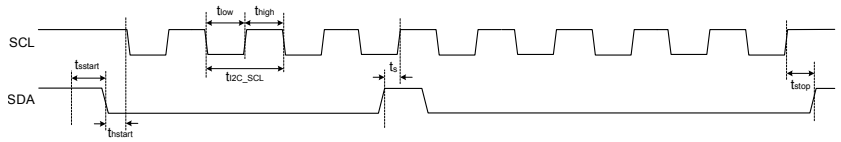


Figure 7.16. Interface Timing Diagram for I2C Fast Speed Mode

7.4.8.4 High Speed Mode

Table 7.31. I2C High Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL	f_{i2c}		1	—	3.4	MHz
clock low period	t_{low}		160	—	—	ns
clock high period	t_{high}		60	—	—	ns
start condition, setup time	t_{sstart}		160	—	—	ns
start condition, hold time	t_{hstart}		160	—	—	ns
data, setup time	t_s		10	—	—	ns
data, hold time	t_h		0	—	70	ns
stop condition, setup time	t_{sstop}		160	—	—	ns
Output Load	C_L		5	—	10	pF

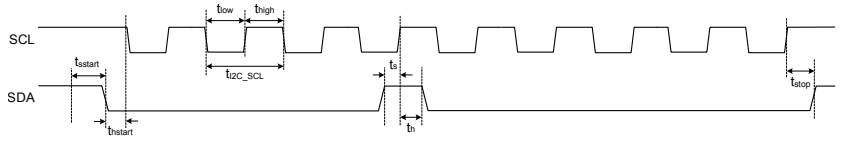


Figure 7.17. Interface Timing Diagram for I2C High Speed Mode

7.4.9 I2S/PCM Primary and Secondary

7.4.9.1 Primary Mode

Negedge driving and posedge sampling for I2S
Posedge driving and negedge sampling for PCM

Table 7.32. I2S/PCM Primary Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
i2s_clk	f_{i2s}		0	—	25	MHz
i2s_din,i2s_ws setup time	t_s		10	—	—	ns
i2s_din,i2s_ws hold time	t_h		3	—	—	ns
i2s_dout output delay	t_{od}		0	—	15	ns
i2s_dout output load	C_L		5	—	10	pF

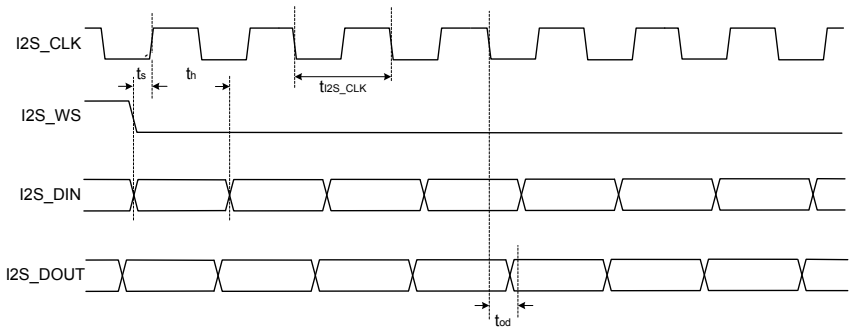


Figure 7.18. Interface Timing Diagram for I2S Primary Mode

7.4.9.2 Secondary Mode

Negedge driving and posedge sampling for I2S

Posedge driving and negedge sampling for PCM

Table 7.33. I2S/PCM Secondary Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
i2s_clk	f_{i2s}		0	—	25	MHz
i2s_din,i2s_ws setup time	t_s		7.5	—	—	ns
i2s_din,i2s_ws hold time	t_h		2	—	—	ns
i2s_dout output delay	t_{od}		0	—	17	ns
i2s_dout output load	C_L		5	—	10	pF

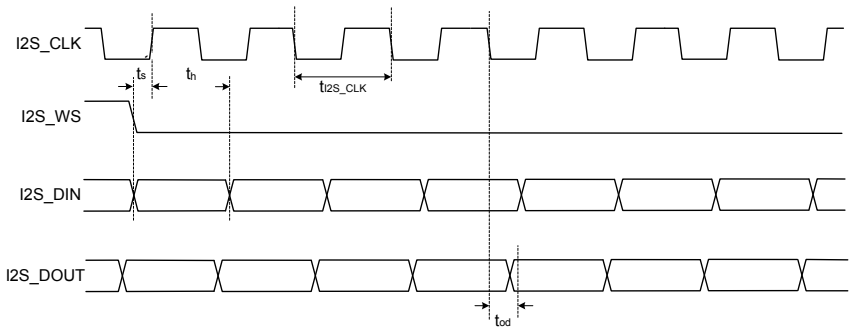


Figure 7.19. Interface Timing Diagram for I2S Secondary Mode

7.4.10 ULP I2S/PCM Primary and Secondary

7.4.10.1 Primary Mode

Negedge driving and posedge sampling for I2S
posedge driving and negedge sampling for PCM

Table 7.34. ULP I2S/PCM Primary Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
i2s_clk	f_{i2s}		0	—	10	MHz
i2s_din,i2s_ws setup time w.r.t negedge	t_s		15	—	—	ns
i2s_din,i2s_ws hold time w.r.t negedge	t_h		0	—	—	ns
i2s_dout output delay	t_{od}		0	—	20	ns
i2s_dout output load	C_L		5	—	10	pF

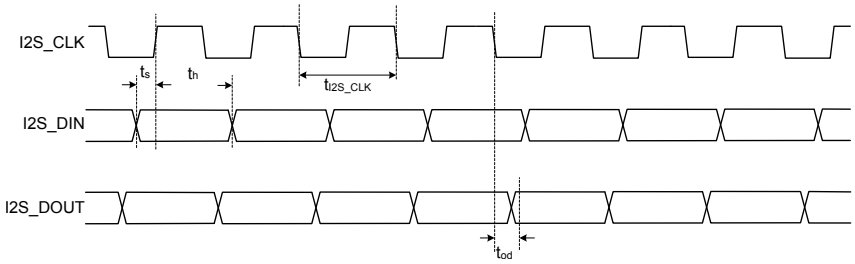


Figure 7.20. Interface timing Diagram for ULP I2S/PCM Primary

7.4.10.2 Secondary Mode

Negedge driving and posedge sampling for I2S
Posedge driving and negedge sampling for PCM

Table 7.35. ULP I2S/PCM Secondary Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
i2s_clk	f_{i2s}		0	—	10	MHz
i2s_din,i2s_ws setup time w.r.t negedge	t_s		10	—	—	ns
i2s_din,i2s_ws hold time w.r.t negedge	t_h		3	—	—	ns
i2s_dout output delay	t_{od}		0	—	20	ns
i2s_dout output load	C_L		5	—	10	pF

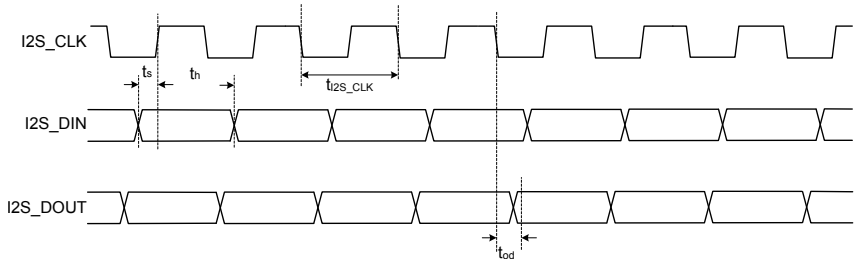


Figure 7.21. Interface Timing Diagram for ULPI2S Secondary

7.4.11 SSI Primary/Secondary

7.4.11.1 Primary Full Speed Mode

Negedge driving and posedge sampling

Table 7.36. SSI Primary Full Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SSI_CLK	f_{ssi}		0	—	20	MHz
SSI_MISO, input setup time	t_s		17	—	—	ns
SSI_MISO, input hold time	t_h		2	—	—	ns
SSI_MOSI, clock to output valid	t_{od}		0	—	16	ns
Output Load	C_L		5	—	10	pF

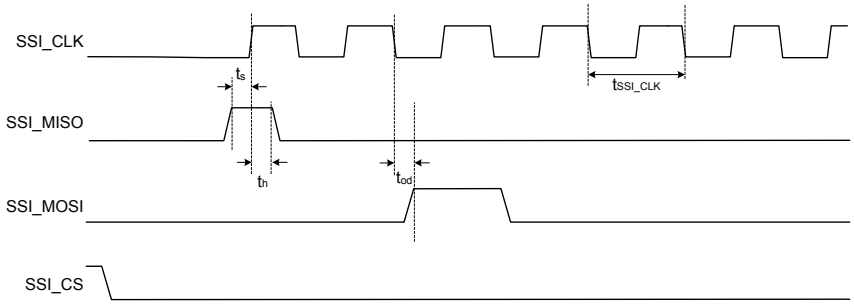


Figure 7.22. Interface Timing Diagram for SSI Primary Full Speed Mode

7.4.11.2 Primary High Speed Mode

Posedge driving and posedge sampling

Table 7.37. SSI Primary High Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SSI_CLK	f_{ssi}		20	—	40	MHz
SSI_MISO, input setup time	t_s		17	—	—	ns
SSI_MISO, input hold time	t_h		2	—	—	ns
SSI_MOSI, clock to output valid	t_{od}		1	—	16	ns
Output Load	C_L		5	—	10	pF

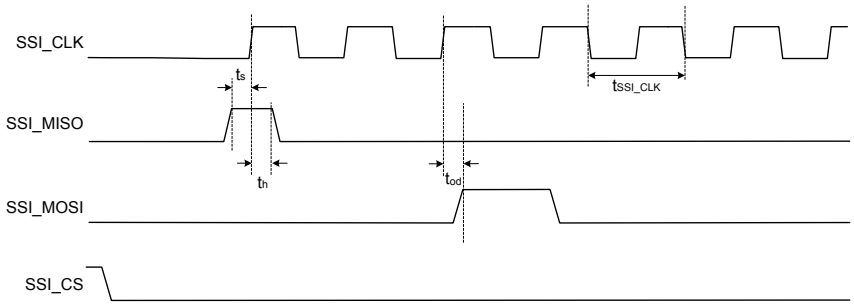


Figure 7.23. Interface Timing Diagram for SSI Primary High Speed Mode

7.4.11.3 Secondary Full Speed Mode

Negedge driving and posedge sampling

Table 7.38. SSI Secondary Full Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SSI_CLK	f_{ssi}		0	—	20	MHz
SSI_MOSI or SSI_CS, input setup time	t_s		5	—	—	ns
SSI_MOSI, input hold time	t_h		0	—	—	ns
SSI_MISO, clock to output delay	t_{od}		—	—	24	ns
Output Load	C_L		5	—	10	pF

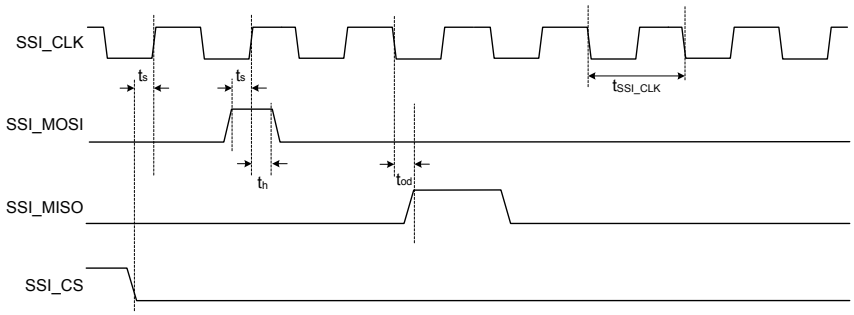


Figure 7.24. Interface Timing Diagram for SSI Secondary Full Speed Mode

7.4.12 ULP SSI Primary

7.4.12.1 Primary Full Speed Mode

Negedge driving and posedge sampling

Table 7.39. ULP SSI Primary Full Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SSI_CLK	f_{ssi}		0	—	10	MHz
SSI_MISO, input setup time	t_s		20	—	—	ns
SSI_MISO, input hold time	t_h		0	—	—	ns
SSI_CS, SSI_MOSI, clock to output valid	t_{od}		0	—	25	ns
Output Load	C_L		5	—	10	pF

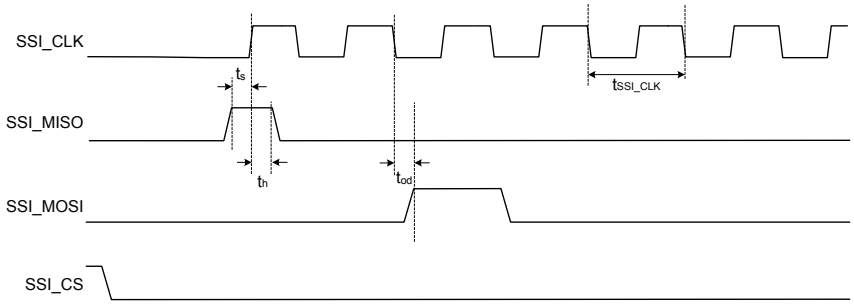


Figure 7.25. Interface Timing Diagram for ULP SSI -- Full Speed Mode

7.4.13 GSPI Primary

7.4.13.1 Full Speed Mode

Negedge driving and posedge sampling

Table 7.40. GSPI Primary Full Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
gspi_clk	f_{gspi}		0	—	58	MHz
gspi_csn, to clock edge(this is achieved functionally)	t_{cs}		4.16	—	—	ns
gspi_miso, setup time	t_s		2	—	—	ns
gspi_miso, hold time	t_h		2	—	—	ns
gspi_csn, gspi_mosi, clock to output valid	t_{od}		0	—	8	ns
Output Load	C_L		5	—	10	pF

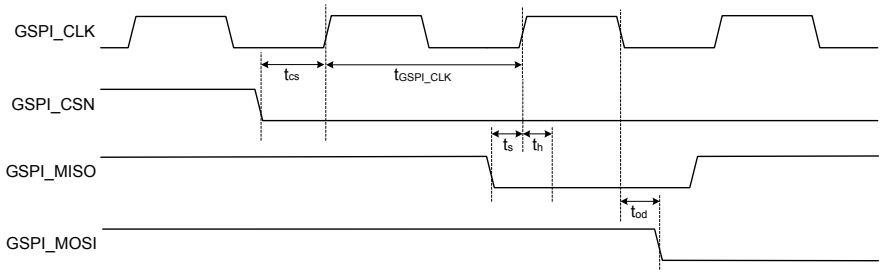


Figure 7.26. Interface Timing Diagram for GSPI Primary Full Speed Mode

7.4.13.2 High Speed Mode

Negedge driving and negedge sampling

Table 7.41. GSPI Primary High Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
gspi_clk	f_{gspi}		58	—	116	MHz
gspi_csn, to clock edge(this is achieved functionally)	t_{cs}		4.16	—	—	ns
gspi_miso, setup time	t_s		2	—	—	ns
gspi_miso, hold time	t_h		2	—	—	ns
gspi_csn, gspi_mosi, clock to output valid	t_{od}		0	—	8	ns
Output Load	C_L		5	—	10	pF

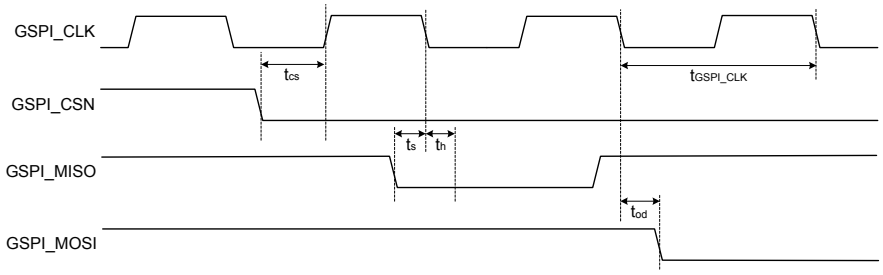


Figure 7.27. Interface Timing Diagram for GSPI Primary High Speed Mode

7.4.14 Cortex-M4 JTAG

Table 7.42. Cortex-M4F JTAG

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TCK period	f_{tck}		—	—	20	MHz
Setup	t_s		5	—	—	ns
Hold	t_h		4	—	—	ns
Output Delay	t_{od}		0	—	38.5	ns
Output Load	C_L		5	—	10	pF

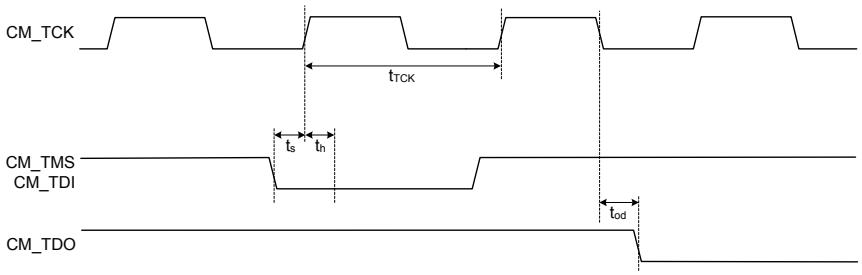


Figure 7.28. Interface Timing Diagram for Cortex-M4 JTAG

7.4.15 Cortex-M4 Trace

Table 7.43. Cortex-M4F Trace

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TRACECLK Period	f_{trace}		0	—	100	MHz
Output Delay	t_{od}		1.2	—	8	ns
Output Load	C_L		5	—	10	pF

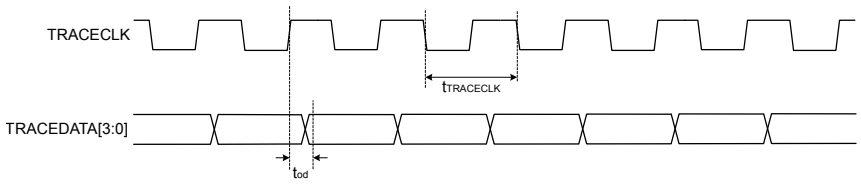


Figure 7.29. Interface Timing Diagram for Cortex-M4 Trace

7.4.16 Power State Wake Timing

Table 7.44. Power State Wake Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transition time from PS4 standby to PS4 active	t_{PS4SB_TR}		—	0.8	—	µs
Transition time from PS3 standby to PS3 active	t_{PS3SB_TR}		—	1.0	—	µs
Transition time from PS2 standby to PS2 active	t_{PS2SB_TR}		—	2.7	—	µs
Wake up time from PS4 sleep to PS4 active[1]	t_{PS4SLP_WU}	320 KB RAM retained in sleep	—	1.1	—	ms
Wake up time from PS3 sleep to PS3 active[1]	t_{PS3SLP_WU}	320 KB RAM retained in sleep	—	1.05	—	ms
Wake up time from PS2 sleep to PS2 active[1]	t_{PS2SLP_WU}	320 KB RAM retained in sleep	—	15.8	—	µs
Transition time from PS1 to PS2 active	t_{PS1_TR}		—	5.1	—	ms
Wake up time from PS0 to PS4 active[1]	t_{PS0_WU}	RC oscillator configured to 20 MHz	—	12.3	—	ms

Note:

1. The Wake up timings presented in the table are measured using the code running from SRAM to reflect the actual hardware wakeup performance. However, the reference examples provided in the software release has the additional code executing from flash, which results in longer wakeup times due to the additional flash initialization process in end-to-end applications.

7.5 Analog Peripherals

The following analog peripherals are available:

- 2x Analog Comparators
- 3x General purpose Op-Amp
- 16 channel, 12 bit, 5 MSPS Analog to Digital Converter with both single ended and differential modes
- 10 bit, 5 MSPS Digital to Analog Converter

7.5.1 Analog Comparators

Analog comparator is a peripheral circuit that compares two analog voltage inputs and gives a logical output based on comparison.

There are 9 different inputs for each pin of comparator, and 2 of the 9 are external pin inputs.
The following cases of comparison are possible

1. Compare external pin inputs
2. Compare external pin input to internal voltages.
3. Compare internal voltages.

The comparator compares inputs p and n to produce an output, cmp_out.

p > n, cmp_out = 1

p < n, cmp_out = 0

Analog Peripherals consists of 2 comparators whose inputs can be programmed independently. The reference buffer and resistor bank are shared between the two comparators and can be enabled only when at least one of the comparators is enabled.

Table 7.45. Analog Comparator Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
	V_{supply}	Supply is AUX_AVDD	1.72	—	3.63	
Programmable voltage reference minimum	V_{ref_min}		—	0.1	—	V
Programmable voltage reference maximum	V_{ref_max}		—	1.1	—	V
Programmable voltage reference step size	V_{ref_step}		—	0.1	—	V
The minimum voltage difference required between inputs to make output high	V_{os_comp}		—	5	—	mV
Hysteresis	V_{hyst_comp}	Hysteresis = 2'd1	—	60	—	mV
		Hysteresis = 2'd3	—	95	—	mV
Input common-mode range	$ICMR_{comp}$		0.15	—	ULP_IO_VDD - 0.15	V
Current consumption on VBATT with all blocks enabled	I_{q_comp}		—	305	—	µA

7.5.2 AUX LDO Electrical Specifications - Regulation Mode

Table 7.46. AUX LDO Electrical Specifications - Regulation Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Supply Voltage	V_{in}	AUX LDO in Regulation Mode	2.97	3.3	3.63	V
Max programmable output voltage at AUX_AVDD	V_{outmax}		—	2.8	—	V
Min programmable output voltage at AUX_AVDD	V_{outmin}		—	1.6	—	V
Output voltage programmable step size [1]	V_{step}		—	80	—	mV
Load current capability	I_{load}		—	—	10	mA
Quiescent current	I_q		—	80	—	µA

Note:

1. Programmable output voltage step, Vstep, can vary up to ± 5%.

7.5.3 AUX LDO Electrical Specifications - Bypass Mode

Table 7.47. AUX LDO Electrical Specifications - Bypass Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Supply Voltage	V_{in}	AUX LDO in Bypass Mode	1.71	1.8	1.98	V
ON Resistance between V_{in} to V_{out} pins of AUX LDO	R_{on}		—	6.3	—	Ω
Voltage drop from V_{in} to V_{out}	V_{drop}	Load = 10 mA (Max)	—	100	—	mV
Output voltage at AUX_AVDD [1]	V_{out}	Load = 10 mA at Vin = 1.71 V [2]	—	1.63	—	V

Note:

1. $V_{out} = V_{in} - R_{on} * I_{load}$
2. Maximum load current is possible when the three op-amps, two analog comparators, ADC, and DAC are all enabled.

7.5.4 Analog to Digital Converter

- 12 bit precision ADC
- Single ended mode and differential mode configuration
- Two clock latency
- ADC performance not guaranteed below -20 ^{o}C

Table 7.48. ADC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution of ADC	N		—	12	—	bits
Number of channels	$N_{channel}$	Single ended Mode	—	18	—	channel
		Differential Mode	—	9	—	channel
ADC sampling and input clock frequency	f_{ADC}		—	—	2.5	MHz
Input voltage range	V_{AIN}	Single ended Mode, Positive terminal	0	—	AUX_AVDD	V
		Differential Mode, Positive and negative terminals	0	—	AUX_AVDD / 2	V
Input resistance	R_{in}	Single Channel input conversion	—	100	—	kΩ
ADC internal sample and hold capacitor	$C_{sampled}$		—	3	—	pF
Fixed capacitance from multiplexers and ESD protection	C_{fixed}		—	2	—	pF
Sampling time	t_s		0.1	—	—	uS
Gain Error[1]	G_{err}	Internal Reference voltage, AUX_AVDD = 2.5V	—	2	—	%
Offset Error[1]	$Offset_{err}$	Internal Reference voltage, AUX_AVDD = 2.5V	—	10	—	mV
Effective number of bits	ENOB	Input frequency 100 kHz at 2.5 Msps	—	10	—	bits
Signal to noise and distortion ratio	SNDR	Input frequency 100 kHz at 2.5 Msps	—	59	—	dB
Active current consumption	I_{active}	Input frequency 100 kHz at 2.5 Msps	—	1.55	—	mA

Note:

1. Gain Error and Offset Error will be proportional to Internal Reference voltage, AUX_AVDD.

7.5.5 Digital to Analog Converter

- 10 bit precision DAC
- Single ended voltage outputs
- 1.71 to 3.63 V supply operation
- DAC performance not guaranteed below -20 ^{o}C.

Table 7.49. DAC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Lowest output voltage	VOL		—	0.15 * AUX_AVDD	—	V
Highest output voltage	VOH		—	0.85 * AUX_AVDD	—	V
Resistive load	R_{load}	Connect to ground	5	—	—	kΩ
Load capacitance	C_{load}		—	—	50	pF
Signal to noise and distortion ratio	SNDR	40 kHz sine wave output and sampling frequency of 2 MHz	—	50	—	dB
Effective number of bits	ENOB	40 kHz sine wave output and sampling frequency of 2 MHz	—	8	—	bits

7.5.6 Op-Amp

There are 3 general purpose Operational Amplifiers (Op-Amps) offering rail-to-rail inputs and outputs.
The Op-Amps can be configured as:

1. Unity gain amplifier
2. Trans-Impedance Amplifier (TIA)
3. Non-inverting Programmable Gain Amplifier (PGA)
4. Inverting Programmable Gain Amplifier (PGA)
5. Non-inverting Programmable hysteresis comparator
6. Inverting Programmable hysteresis comparator
7. Cascaded Non-Inverting PGA
8. Cascaded Inverting PGA
9. Two Op-Amps Differential Amplifier
10. Instrumentation Amplifier

Note:

- In the above list, #7, #8, #9 are configured by cascading 2 Op-Amps
- In the above list, #10 is configured by cascading 3 Op-Amps

Table 7.50. Opamp Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage range	V_{in}		0	—	AUX_AVDD	V
output voltage range	V_{out}	source or sink 1 mA	0.1	—	AUX_AVDD - 0.1	V
output current capability, source or sink	I_{out}	0.5 < V_{out} < AUX_AVDD-0.5	—	—	3	mA
Input offset voltage (1 sigma)	V_{os}	Power mode = high, C_L = 50 pF	—	2.2	—	mV
		Power mode = low, C_L = 50 pF	—	2.2	—	mV
Gain error, unity gain buffer mode, R_L = 1 kΩ	Ge1	Power mode = high, C_L = 50 pF	—	1	—	%
		Power mode = low, C_L = 50 pF	—	1	—	%
Phase margin, in UGB mode	PM	Power mode = high, C_L = 50 pF	—	59	—	°C
		Power mode = low, C_L = 50 pF	—	63	—	°C
Gain-bandwidth product	GBW	Power mode = high, C_L = 50 pF	—	17	—	MHz
		Power mode = low, C_L = 50 pF	—	7.5	—	MHz
Total Harmonic Distortion, at 100 kHz (UGB mode)	THD_{UGB}	Power mode = high, C_L = 50 pF	—	-64	—	dB
		Power mode = low, C_L = 50 pF	—	-62	—	dB
Total Harmonic Distortion, at 10 kHz (Non inv amp mode, gain = 51)	THD	Power mode = high, C_L = 50 pF	—	-58	—	dB
		Power mode = low, C_L = 50 pF	—	-56	—	dB
DC Power supply rejection ratio	PSRR	Power mode = high, C_L = 50 pF	—	85	—	dB
		Power mode = low, C_L = 50 pF	—	85	—	dB
DC Common mode rejection ratio	CMRR	Power mode = high, C_L = 50 pF	—	70	—	dB
		Power mode = low, C_L = 50 pF	—	71	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Quiescent current - 1 Op-Amp	I_{dd}	Power mode = high, C_L = 50 pF	—	0.95	—	mA
		Power mode = low, C_L = 50 pF	—	315	—	µA

7.5.7 Temperature Sensor

- Generates PTAT Voltage from BJT based band gap.
- Buffered PTAT voltage is given at ADC Input.
- Output of the ADC is linear function of temperature.

The BJT based sensor works over the full operating temperature and supply range of the device. It outputs a digital word having a resolution of nearly 1 ºC. The conversion time is 2 clock cycles of ADC after turning ON the temperature sensor. Typically, the block consumes 110 uA of current and leakage current is 800 pA.

Table 7.51. BJT Based Temperature Sensor Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Accuracy	T_{acc}		—	6	—	°C

7.6 RF Characteristics

In the sub-sections below,

- All numbers are measured at T_A = 25°C, PA2G_AVDD = VINBCKDC = 3.3 V using an external 40 MHz crystal, unless otherwise stated.
- Please refer to 8. Reference Schematics, BOM and Layout Guidelines. As shown in Figure 8.4. Option 1: RF Frontend with External Switch, there are three RF pins at the IC: RF_TX, RF_RX, and RF_BLETX. The RF front end for testing includes the matching network, RF switch and a band-pass filter. Typical front-end loss is about 2 dB. Silicon Labs recommends using the suggested reference design to meet these specs.
- All reported Receiver Sensitivity and Transmit Power numbers are based on the RF front end option shown in Figure 8.4. Option 1: RF Frontend with External Switch. The value at the antenna port (ANT1) will be based on front end loss, which is typically 2 dB lower than pins RF1, RF2, and RF3 of the RF switch (SW2). Using the internal switch option incurs 1-1.5 dBm performance degradation, unless otherwise specified.
- Supported WLAN channels for different regions include:
  - US: Channels 1 (2412 MHz) through 11 (2462 MHz)
  - Europe: Channels 1 (2412 MHz) through 13 (2472 MHz)
  - Japan: Channels 1 (2412 MHz) through 14 (2484 MHz), Channel 14 supports 1 and 2 Mbps data rates only

7.6.1 WLAN 2.4 GHz Transmitter Characteristics

7.6.1.1 WLAN 2.4 GHz Transmitter Characteristics with 3.3 V Supply

Unless otherwise indicated, typical conditions are: T_A = 25 °C. PA2G_AVDD = VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are referred at IC pin (RF_TX).

Table 7.52. WLAN 2.4 GHz Transmitter Characteristics with 3.3 V Supply

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit Power for 20 MHz Bandwidth, with EVM limits [1] [2] [3]	POUT	802.11b 1 Mbps DSSS, EVM< -9 dB	—	19	—	dBm
		802.11b 11 Mbps CCK, EVM< -9 dB	—	19	—	dBm
		802.11g 6 Mbps OFDM, EVM< -5 dB [4]	—	19.5	—	dBm
		802.11g 54 Mbps OFDM, EVM< -25 dB [4]	—	15.5	—	dBm
		802.11n HT20 MCS0 Mixed Mode, EVM< -5 dB [4]	—	19.5	—	dBm
		802.11n HT20 MCS7 Mixed Mode, EVM< -27 dB [4]	—	14.5	—	dBm
		802.11ax HE20 MCS0 SU, EVM< -5 dB [5] [4]	—	18.5	—	dBm
		802.11ax HE20 MCS7 SU, EVM< -27 dB [5] [4]	—	13	—	dBm
Power variation across channels[6]	$POUT_{VAR_CH}$		—	2	—	dB
Power variation across temperature[7]	$POUT_{VAR_T}$	-40 to +85 °C	—	3	—	dB

Note:

1. Transmit power listed in this table is average power across channels 1 to 13. Customers should calibrate crystal error and follow application note guildelines to achieve regulatory compliance.
2. TX power in edge channels will be limited by Restricted band edge in the FCC region.
3. Refer to the Wi-Fi Gain Table section in AN1437 for details on TX power backoff for compliance with regulatory limits.
4. 11ax TB_PPDU @ Channels(1-13) TX power will be limited by antenna conducted output power test case (dBm/MHz) in MIC region.
5. 11ax TB_PPDU TX power will be limited by PSD in the ETSI region.
6. This variation is measured independently and is not derived from or referenced to the typical values listed in the table.
7. Variation is noted at channel-6. This variation is measured independently and is not derived from or referenced to the typical values listed in the table.

7.6.2 WLAN 2.4 GHz Receiver Characteristics on HP RF Chain

Unless otherwise indicated, typical conditions are: T_A = 25 °C. PA2G_AVDD = VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are referred at IC pin RF_RX

Table 7.53. WLAN 2.4 GHz Receiver Characteristics on HP RF Chain

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sensitivity for 20 MHz Bandwidth [1] [2] [3]	SENS	802.11b 1 Mbps DSSS [4]	—	-97.5	—	dBm
		802.11b 11 Mbps CCK [4]	—	-88	—	dBm
		802.11g 6 Mbps OFDM [5]	—	-93	—	dBm
		802.11g 54 Mbps OFDM [5]	—	-76.5	—	dBm
		802.11n HT20 MCS0 Mixed Mode [6]	—	-92	—	dBm
		802.11n HT20 MCS7 Mixed Mode [6]	—	-73	—	dBm
		802.11ax HE20 MCS0 SU [7]	—	-91.5	—	dBm
		802.11ax HE20 MCS7 SU [7]	—	-72	—	dBm
		802.11ax HE20 MCS0 ER [7]	—	-92.5	—	dBm
Maximum Input Level for PER below 10%	RX_{SAT}	802.11b	—	3	—	dBm
		802.11g	—	-2.5	—	dBm
		802.11n	—	-4.5	—	dBm
		802.11ax	—	-2.5	—	dBm
RSSI Accuracy Range[11]	$RSSI_{RNG}$	Input level from +2 dBm to -87 dBm	—	+/-4	—	dB
Adjacent Channel Interference [8]	ACI	802.11b 1 Mbps DSSS [4] [9]	—	43	—	dB
		802.11b 11 Mbps CCK [4] [9]	—	35	—	dB
		802.11g 6 Mbps OFDM [5] [10]	—	38	—	dB
		802.11g 54 Mbps OFDM [5] [10]	—	18	—	dB
		802.11n HT20 MCS0 Mixed Mode [6] [10]	—	32	—	dB
		802.11n HT20 MCS7 Mixed Mode [6] [10]	—	10	—	dB
		802.11ax HE20 MCS0 SU [7] [10]	—	20	—	dB
		802.11ax HE20 MCS7 SU [7] [10]	—	3	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Alternate Adjacent Channel Interference [8]	AACI	802.11b 1 Mbps DSSS [4 9]	—	49	—	dB
		802.11b 11 Mbps CCK [4 9]	—	42	—	dB
		802.11g 6 Mbps OFDM [5 10]	—	49	—	dB
		802.11g 54 Mbps OFDM [5 10]	—	27	—	dB
		802.11n HT20 MCS0 Mixed Mode [6 10]	—	48	—	dB
		802.11n HT20 MCS7 Mixed Mode [6 10]	—	26	—	dB
		802.11ax HE20 MCS0 SU [7 10]	—	48	—	dB
		802.11ax HE20 MCS7 SU [7 10]	—	25	—	dB

Note:

1. RX Sensitivity Variation within these channels (1, 2, 3, 4, 5, 9, and 10) is up to 2dB at typical / room temperature. These variations are measured independently and are not derived from or referenced to the typical values listed in the table.
2. RX Sensitivity may be degraded for these channels (6, 7, 8, 11, 12 and 13) by up to 3dB from the min value of all channels 1 to 13, at typical / room temperature. These variations are measured independently and are not derived from or referenced to the typical values listed in the table.
3. Sensitivity variation across temperature -40 °C to 85 °C is up to 3 dB at channel-6. These variations are measured independently and are not derived from or referenced to the typical values listed in the table.
4. 802.11b, Packet size is 1024 bytes, < 8% PER limit.
5. 802.11g, Packet size is 1024 bytes, < 10% PER limit.
6. 802.11n, Packet size is 4096 bytes, < 10% PER limit.
7. 802.11ax, Packet size is 4096 bytes, < 10% PER limit, Carrier modulation is non-DCM
8. ACI / AACI is calculated as Interferer Power(dBm)- Inband power(dBm)
9. Desired signal power is 6 dB above standard defined sensitivity level
10. Desired signal power is 3 dB above standard defined sensitivity level
11. RSSI error may increase up to ±10 dB for Receive input levels below -87 dBm.

7.6.3 WLAN 2.4 GHz Receiver Characteristics on LP RF Chain

Unless otherwise indicated, typical conditions are: T_A = 25 °C. PA2G_AVDD = VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are referred at IC pin RF_RX

Table 7.54. WLAN 2.4 GHz Receiver Characteristics on LP RF Chain

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sensitivity for 20 MHz Bandwidth [1] [2] [3]	SENS	802.11b 1 Mbps DSSS [4]	—	-97	—	dBm
		802.11b 11 Mbps CCK [4]	—	-87.5	—	dBm
		802.11g 6 Mbps OFDM [5]	—	-92.5	—	dBm
		802.11g 36 Mbps OFDM [5]	—	-81.5	—	dBm
		802.11n HT20 MCS0 Mixed Mode [6]	—	-91.5	—	dBm
		802.11n HT20 MCS4 Mixed Mode [6]	—	-80.5	—	dBm
Maximum Input Level for PER below 10%	RX_{SAT}	802.11b	—	-8	—	dBm
		802.11g	—	-0.5	—	dBm
		802.11n	—	-1	—	dBm
RSSI Accuracy Range[10]	$RSSI_{RNG}$	Input level from +2 dBm to -83 dBm	—	+/-4	—	dB
Adjacent Channel Interference [7]	ACI	802.11b 1 Mbps DSSS [4] [8]	—	43	—	dB
		802.11b 11 Mbps CCK [4] [8]	—	36	—	dB
		802.11g 6 Mbps OFDM [5] [9]	—	38	—	dB
		802.11g 36 Mbps OFDM [5] [9]	—	25	—	dB
		802.11n HT20 MCS0 Mixed Mode [6] [9]	—	32	—	dB
		802.11n HT20 MCS4 Mixed Mode [6] [9]	—	18	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Alternate Adjacent Channel Interference [7]	AACI	802.11b 1 Mbps DSSS [4] [8]	—	46	—	dB
		802.11b 11 Mbps CCK [4] [8]	—	40	—	dB
		802.11g 6 Mbps OFDM [5] [9]	—	43	—	dB
		802.11g 36 Mbps OFDM [5] [9]	—	31	—	dB
		802.11n HT20 MCS0 Mixed Mode [6] [9]	—	43	—	dB
		802.11n HT20 MCS4 Mixed Mode [6] [9]	—	30	—	dB

Note:

1. RX Sensitivity Variation within these channels (1, 2, 3, 4, 5, 9, and 10) is up to 2dB at typical / room temperature. These variations are measured independently and are not derived from or referenced to the typical values listed in the table.
2. RX Sensitivity may be degraded for these channels (6, 7, 8, 11, 12 and 13) by up to 3dB from the min value of all channels 1 to 13, at typical / room temperature. These variations are measured independently and are not derived from or referenced to the typical values listed in the table.
3. Sensitivity variation across temperature -40 °C to 85 °C is up to 3 dB at channel-6. These variations are measured independently and are not derived from or referenced to the typical values listed in the table.
4. 802.11b, Packet size is 1024 bytes, < 8% PER limit.
5. 802.11g, Packet size is 1024 bytes, < 10% PER limit.
6. 802.11n, Packet size is 4096 bytes, < 10% PER limit.
7. ACI / AACI is calculated as Interferer Power(dBm)- Inband power(dBm)
8. Desired signal power is 6 dB above standard defined sensitivity level
9. Desired signal power is 3 dB above standard defined sensitivity level
10. RSSI error may increase up to ±10 dB for Receive input levels below -83 dBm.

7.6.4 Bluetooth Transmitter Characteristics on High-Performance (HP) RF Chain

Unless otherwise indicated, typical conditions are: T_A = 25 °C. PA2G_AVDD = VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are refered at IC pin (RF_TX).

Table 7.55. Bluetooth Transmitter Characteristics on High-Performance (HP) RF Chain

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit Power [1] [2]	POUT	LE 1 Mbps[3]	—	19	—	dBm
		LE 2 Mbps [5]	—	19	—	dBm
		LR 500 kbps[4]	—	19	—	dBm
		LR 125 kbps [4]	—	19	—	dBm
Power variation across channels[6]	$POUT_{VAR_CH}$		—	2	—	dB
Power variation across temperature[7]	$POUT_{VAR_T}$	-40 to +85 °C	—	3	—	dB
Adjacent Channel Power |M-N| = 2	ACP_{eq2}	LE	—	-25	—	dBm
Adjacent Channel Power |M-N| > 2	ACP_{gt2}	LE	—	-31	—	dBm
BLE Modulation Characteristics at 1 Mbps	MOD_{CHAR}	Δf1 Avg	—	250	—	kHz
		Δf2 Max	—	250	—	kHz
		Δf2 Avg/Δf1 Avg	—	1.3	—	

Note:

1. ETSI Max Power should be limited to 10 dBm because device falls under DTS, non-adaptive
2. Refer to the BLE Gain Table section in AN1437 for details on TX power backoff for compliance with regulatory limits.
3. In FCC, for 1 Mbps data rates, in channels 2476 - 2480 MHz, TX output power will be limited by band edge.
4. In FCC - LR 125 kbps, 500 kbps Max Power should be limited to 12 dBm to meet PSD requirement because, device falls under DTS, non-adaptive
5. Channel 2480 MHz is not supported in 2 Mbps
6. This variation is measured independently and is not derived from or referenced to the typical values listed in the table.
7. Variation is noted at channel-6. This variation is measured independently and is not derived from or referenced to the typical values listed in the table.

7.6.5 Bluetooth Transmitter Characteristics on Low-Power (LP) 8 dBm RF Chain

Unless otherwise indicated, typical conditions are: T_A = 25 °C. PA2G_AVDD = VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are referred at IC pin (RF_BLETX).

Table 7.56. Bluetooth Transmitter Characteristics on Low-Power (LP) 8 dBm RF Chain

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit Power [1]	POUT	LE 1 Mbps	—	8	—	dBm
		LE 2 Mbps [2]	—	8	—	dBm
		LR 500 kbps	—	8	—	dBm
		LR 125 kbps	—	8	—	dBm
Power variation across channels[3]	$POUT_{VAR_CH}$		—	2	—	dB
Power variation across temperature[4]	$POUT_{VAR_T}$	-40 to +85 °C	—	3	—	dB
Adjacent Channel Power |M-N| = 2	ACP_{eq2}	LE	—	-32	—	dBm
Adjacent Channel Power |M-N| > 2	ACP_{gt2}	LE	—	-36	—	dBm
BLE Modulation Characteristics at 1 Mbps	MOD_{CHAR}	Δf1 Avg	—	248	—	kHz
		Δf2 Max	—	249	—	kHz
		Δf2 Avg/Δf1 Avg	—	1.3	—	kHz

Note:

1. Refer to the BLE Gain Table section in AN1437 for details on TX power backoff for compliance with regulatory limits.
2. Channel 2480 MHz is not supported in 2 Mbps.
3. This variation is measured independently and is not derived from or referenced to the typical values listed in the table.
4. Variation is noted at channel-6. This variation is measured independently and is not derived from or referenced to the typical values listed in the table.

7.6.6 Bluetooth Transmitter Characteristics on Low-Power (LP) 0 dBm RF Chain

Unless otherwise indicated, typical conditions are: T_A = 25 °C. PA2G_AVDD = VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are referred at IC pin (RF_RX).

Table 7.57. Bluetooth Transmitter Characteristics on Low-Power (LP) 0 dBm RF Chain

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit Power	POUT	LE 1 Mbps	—	-0.5	—	dBm
		LE 2 Mbps[1]	—	-0.5	—	dBm
		LR 500 kbps	—	-0.5	—	dBm
		LR 125 kbps	—	-0.5	—	dBm
Power variation across channels[2]	$POUT_{VAR_CH}$		—	2	—	dB
Power variation across temperature[3]	$POUT_{VAR_T}$	-40 to +85 °C	—	2	—	dB
Adjacent Channel Power |M-N| = 2	ACP_{eq2}	LE	—	-41	—	dBm
Adjacent Channel Power |M-N| > 2	ACP_{gt2}	LE	—	-47	—	dBm
BLE Modulation Characteristics	MOD_{CHAR}	Δf1 Avg	—	248	—	kHz
		Δf2 Max	—	249	—	kHz
		Δf2 Avg/Δf1 Avg	—	1.3	—	kHz

Note:

1. Channel 2480 MHz is not supported in 2 Mbps.
2. This variation is measured independently and is not derived from or referenced to the typical values listed in the table.
3. Variation is noted at channel-6. This variation is measured independently and is not derived from or referenced to the typical values listed in the table.

7.6.7 Bluetooth Receiver Characteristics for 1 Mbps Data Rate

Unless otherwise indicated, specifications apply to both HP and LP chains. Typical conditions are: T_A = 25 °C, PA2G_AVDD = VINBCKDC = 3.3 V, remaining supplies are at typical operating conditions, packet length is 37 bytes, parameters are referred at IC pin RF_RX

Table 7.58. Bluetooth Receiver Characteristics for 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	RX_{SAT}	Signal is reference signal, 255 byte payload, BER = 0.017%, HP Chain	—	2	—	dBm
		Signal is reference signal, 255 byte payload, BER = 0.017%, LP Chain	—	-2	—	dBm
Sensitivity [1] [2]	SENS	Signal is reference signal, 37 byte payload, BER = 0.1%	—	-96	—	dBm
		Signal is reference signal, 255 byte payload, BER = 0.017%	—	-94	—	dBm
Signal to co-channel interferer [3]	C/I_{CC}	(see notes)[4] [5]	—	-12	—	dB
N ± 1 Adjacent channel selectivity [3]	C/I_1	Interferer is reference signal at +1 MHz offset[4] [6] [5] [7]	—	-6	—	dB
		Interferer is reference signal at -1 MHz offset[4] [6] [5] [7]	—	-4	—	dB
N ± 2 Alternate channel selectivity [3]	C/I_2	Interferer is reference signal at +2 MHz offset[4] [6] [5] [7]	—	19	—	dB
		Interferer is reference signal at -2 MHz offset[4] [6] [5] [7]	—	24	—	dB
N ± 3 Alternate channel selectivity [3]	C/I_3	Interferer is reference signal at +3 MHz offset[4] [6] [5] [7]	—	20	—	dB
		Interferer is reference signal at -3 MHz offset[4] [6] [5] [7]	—	31	—	dB
N ≥ | ± 4| Alternate channel selectivity [3]	C/I_4	Interferer is reference signal at ≥ | ± 4| MHz offset[4] [6] [5] [7]	—	33	—	dB
Selectivity to image frequency [3]	C/I_{IM}	Interferer is reference signal at image frequency[4] [5] [7] [8]	—	17	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Selectivity to image frequency ± 1 MHz [3]	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz[4 5 7 8]	—	29	—	dB
		Interferer is reference signal at image frequency -1 MHz[4 5 7 8]	—	20	—	dB

Note:

1. Sensitivities may be degraded for channels 19, 39 by up to 2 dB from the min value of all channels 0 to 39, at typical/room temperature.
2. Sensitivity variation across temperature -40 °C to 85 °C is up to 4 dB at channel-19. These variations are measured independently and are not derived from or referenced to the typical values listed in the table.
3. C/I is calculated as Interferer Power(dBm)- Inband power(dBm)
4. 0.1% BER, 37 byte packet size
5. Desired signal = -67 dBm
6. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz
7. With allowed exceptions
8. Image frequency is at +4 MHz offset

7.6.8 Bluetooth Receiver Characteristics for 2 Mbps Data Rate

Unless otherwise indicated, specifications apply to both HP and LP chains. Typical conditions are: T_A = 25 °C, PA2G_AVDD = VINBCKDC = 3.3 V, remaining supplies are at typical operating conditions, packet length is 37 bytes, parameters are referred at IC pin RF_RX

Table 7.59. Bluetooth Receiver Characteristics for 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	RX_{SAT}	Signal is reference signal, 255 byte payload, BER = 0.017%, HP Chain	—	2	—	dBm
		Signal is reference signal, 255 byte payload, BER = 0.017%, LP Chain	—	-6	—	dBm
Sensitivity [1] [2]	SENS	Signal is reference signal, 37 byte payload, BER = 0.1%	—	-93	—	dBm
		Signal is reference signal, 255 byte payload, BER = 0.017%	—	-91	—	dBm
Signal to co-channel interferer [3]	C/I_{CC}	(see notes)[4] [5]	—	-10	—	dB
N ± 1 Adjacent channel selectivity [3]	C/I_1	Interferer is reference signal at +2 MHz offset[4] [6] [5] [7]	—	5	—	dB
		Interferer is reference signal at -2 MHz offset[4] [6] [5] [7]	—	1	—	dB
N ± 2 Alternate channel selectivity [3]	C/I_2	Interferer is reference signal at +4 MHz offset[4] [6] [5] [7]	—	14	—	dB
		Interferer is reference signal at -4 MHz offset[4] [6] [5] [7]	—	20	—	dB
Selectivity to image frequency [3]	C/I_{IM}	Interferer is reference signal at image frequency[4] [5] [7] [8]	—	14	—	dB
Selectivity to image frequency ± 2 MHz [3]	C/I_{IM_2}	Interferer is reference signal at image frequency +2 MHz[4] [5] [7] [8]	—	24	—	dB
		Interferer is reference signal at image frequency -2 MHz[4] [5] [7] [8]	—	5	—	dB

Note:

1. Sensitivities may be degraded for channels 19, 39 by up to 2 dB from the min value of all channels 0 to 39, at typical/room temperature.
2. Sensitivity variation across temperature -40 °C to 85 °C is up to 4 dB at channel-19. These variations are measured independently and are not derived from or referenced to the typical values listed in the table.
3. C/I is calculated as Interferer Power(dBm)- Inband power(dBm)
4. 0.1% BER, 37 byte packet size
5. Desired signal = -67 dBm
6. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz
7. With allowed exceptions
8. Image frequency is at +4 MHz offset

7.6.9 Bluetooth Receiver Characteristics for 125 kbps Data Rate

Unless otherwise indicated, specifications apply to both HP and LP chains. Typical conditions are: T_A = 25 °C, PA2G_AVDD = VINBCKDC = 3.3 V, remaining supplies are at typical operating conditions, packet length is 37 bytes, parameters are referred at IC pin RF_RX

Table 7.60. Bluetooth Receiver Characteristics for 125 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	RX_{SAT}	Signal is reference signal, 255 byte payload, BER = 0.017%, HP Chain	—	3	—	dBm
		Signal is reference signal, 255 byte payload, BER = 0.017%, LP Chain	—	0	—	dBm
Sensitivity [1] [2]	SENS	Signal is reference signal, 37 byte payload, BER = 0.1%	—	-107	—	dBm
		Signal is reference signal, 255 byte payload, BER = 0.017%	—	-106	—	dBm

Note:

1. Sensitivities may be degraded for channels 19, 39 by up to 2 dB in External Switch configuration (Figure 8.4) and up to 8 dB in Internal Switch configuration (Figure 8.5), from the min value of all channels 0 to 39, at typical/room temperature.
2. Sensitivity variation across temperature -40 °C to 85 °C is up to 4 dB at channel-19. These variations are measured independently and are not derived from or referenced to the typical values listed in the table.

7.6.10 Bluetooth Receiver Characteristics for 500 kbps Data Rate

Unless otherwise indicated, specifications apply to both HP and LP chains. Typical conditions are: T_A = 25 °C, PA2G_AVDD = VINBCKDC = 3.3 V, remaining supplies are at typical operating conditions, packet length is 37 bytes, parameters are referred at IC pin RF_RX

Table 7.61. Bluetooth Receiver Characteristics for 500 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	RX_{SAT}	Signal is reference signal, 255 byte payload, BER = 0.017%, HP Chain	—	3	—	dBm
		Signal is reference signal, 255 byte payload, BER = 0.017%, LP Chain	—	0	—	dBm
Sensitivity [1] [2]	SENS	Signal is reference signal, 37 byte payload, BER = 0.1%	—	-102.5	—	dBm
		Signal is reference signal, 255 byte payload, BER = 0.017%	—	-101.5	—	dBm

Note:

1. Sensitivities may be degraded for channels 19, 39 by up to 2 dB in External Switch configuration (Figure 8.4) and up to 8 dB in Internal Switch configuration (Figure 8.5), from the min value of all channels 0 to 39, at typical/room temperature.
2. Sensitivity variation across temperature -40 °C to 85 °C is up to 4 dB at channel-19. These variations are measured independently and are not derived from or referenced to the typical values listed in the table.

7.7 Typical Current Consumption

Figure 7.30. Supply Connection for Current Measurements shows the supply connection and measurement point for supply current numbers in this section. Note that for WLAN and BLE supply current measurements, the MCU is in deep sleep mode with no RAM retained. A 32.768 kHz crystal is used at pins XTAL_32KHZ_P and XTAL_32KHZ_N. All measurements are taken on devices with in-package flash. The impact of external SRAM on current consumption is detailed in Table 5.10. Estimated Deepsleep/DTIMs current with PSRAM for different input supply options.

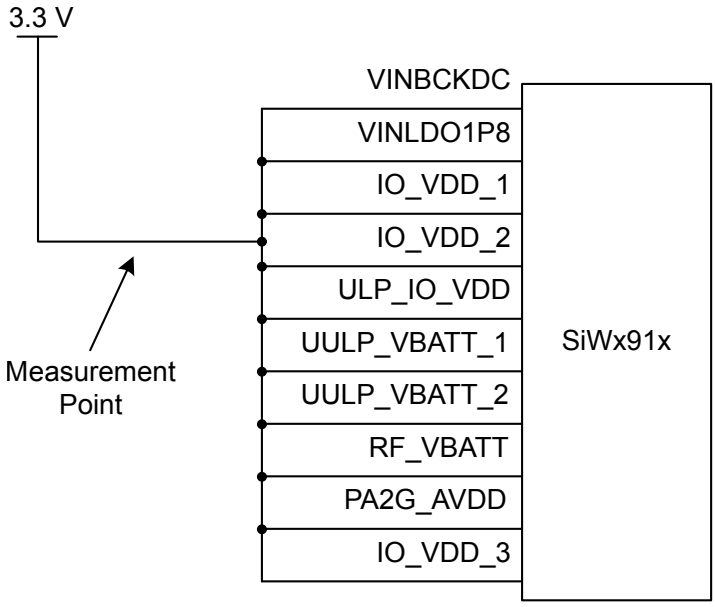


Figure 7.30. Supply Connection for Current Measurements

7.7.1 WLAN 2.4 GHz 3.3 V Current Consumption

T_A = 25 °C. PA2G_AVDD = VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions. NWP clock is running at 80 MHz and Cortex-M4 is in PS0 mode.

Table 7.62. WLAN 2.4 GHz 3.3 V Current Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Listen current	I_{RX_LISTEN}	LP Chain, 1 Mbps Listen	—	16.5	—	mA
Active Receive Current	I_{RX_ACTIVE}	1 Mbps RX Active, LP Chain	—	22	—	mA
		HT20 MCS0, HP Chain	—	51	—	mA
		HT20 MCS7, HP Chain	—	51	—	mA
		HE20 MCS0, HP Chain	—	51	—	mA
		HE20 MCS7, HP Chain	—	51	—	mA
Transmit Current [1]	I_{TX}	1 Mbps, HP Chain	—	240	—	mA
		HT20 MCS0, HP Chain	—	230	—	mA
		HT20 MCS7, HP Chain	—	180	—	mA
		HE20 MCS0, HP Chain	—	220	—	mA
		HE20 MCS7, HP Chain	—	170	—	mA
Deep Sleep	I_{SLEEP}	No RAM retained	—	2.5	—	µA
		352 KB RAM retained	—	10	—	µA
Standby Associated, DTIM = 10	I_{STBY_ASSOC}	WLAN Keep Alive Every 30 s with 352 KB RAM Retained, Without TCP Keep Alive	—	65	—	µA
		WLAN Keep Alive Every 30 s with 352 KB RAM Retained, TCP Keep Alive Every 240 s	—	73	—	µA
11ax TWT, Auto Config Enabled, Without TCP Keep Alive	I_{STBY_AX}	RX latency 2 s with 8 ms wakeup duration, WLAN Keep Alive Every 30 s with 352 KB RAM Retained	—	92	—	µA
		RX latency 30 s with 8 ms wakeup duration, WLAN Keep Alive Every 30 s with 352 KB RAM Retained	—	32	—	µA
		RX latency 60 s with 8 ms wakeup duration, WLAN Keep Alive Every 60 s with 352 KB RAM Retained	—	22	—	µA
11ax TWT, Auto Config Enabled, With TCP Keep Alive Every 240 s	$I_{STBY_AX_TCP}$	RX latency 2 s with 8 ms wakeup duration, WLAN Keep Alive Every 30 s with 352 KB RAM Retained	—	97	—	µA
		RX latency 30 s with 8 ms wakeup duration, WLAN Keep Alive Every 30 s with 352 KB RAM Retained	—	35	—	µA
		RX latency 60 s with 8 ms wakeup duration, WLAN Keep Alive Every 60 s with 352 KB RAM Retained	—	26	—	µA

Note:

1. The absolute maximum device current when transmitting at highest transmit power will not exceed 400 mA.

7.7.2 Bluetooth LE Current Consumption

T_A = 25 °C. PA2G_AVDD = VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions. NWP clock running at 80 MHz.

Table 7.63. Bluetooth LE Current Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TX Active Current	I_{TX}	LP chain, Tx Power = 0 dBm	—	10	—	mA
		LP chain, Tx Power = Max TX power	—	18	—	mA
RX Active Current	I_{RX}	LP chain	—	11	—	mA
Advertising, Unconnectable	I_{ADV_UC}	Advertising on all 3 channels, 37 Byte payload, Interval = 1.28 s, Tx Power = 0 dBm, LP chain	—	37	—	µA
Advertising, Connectable	I_{ADV_CN}	Advertising on all 3 channels, 37 Byte payload, Interval = 1.28 s, Tx Power = 0 dBm, LP chain	—	41	—	µA
Connected	I_{CONN}	Connection Interval = 1.28s, No data, Tx Power = 0 dBm, LP chain	—	48	—	µA
		Connection Interval = 200 ms, No data, Tx Power = 0 dBm, LP chain	—	149	—	µA

7.7.3 MCU Power State Current Consumption

T_A = 25 °C. PA2G_AVDD = VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions. All numbers taken with NWP in shutdown mode.

Table 7.64. MCU Power State Current Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PS4 Supply Current	I_{PS4}	Sleep, 320 KB RAM retained, SRAM PERI ON, SCDC = 1.05 V, ULP LDO = 0.75 V	—	13.7	—	µA
		Active - Default configuration	—	12.7	—	mA
PS3 Supply Current	I_{PS3}	Sleep, 320 KB RAM retained, SRAM PERI ON, SCDC = 1.05 V, ULP LDO = 0.75 V	—	13.7	—	µA
		Active - Default configuration	—	7.6	—	mA
PS2 Supply Current	I_{PS2}	Sleep, 320 KB RAM retained, SRAM PERI ON, SCDC = 1.05 V, ULP LDO = 0.75 V	—	13.7	—	µA
		Active - Default configuration	—	808	—	µA
PS1 Supply Current	I_{PS1}	320 KB RAM retained, SRAM PERI ON, SCDC = 1.05 V, ULP LDO = 0.75 V	—	309	—	µA
PS0 Supply Current	I_{PS0}	Without RAM retention, SRAM PERI ON, SCDC = 1.05 V, ULP LDO = 0.75 V	—	1.44	—	µA

8. Reference Schematics, BOM and Layout Guidelines

8.1 Schematics

Typical schematic connections are shown in this section. Please refer to following documents for more information.

- Follow guidelines in Application Note AN1436 for calibrating the external 40 MHz crystal.
- Follow guidelines in Application Note AN1440 for calibrating the power of RF front-end circuitry.
- Follow guidelines in Application Note AN1423 for RF design related aspects.

1. Customers should include provision for programming or updating the firmware and calibration at manufacturing.
   a. If using UART, we recommend bringing out the HSPI or SDIO lines to test points, so designers could use the faster interface for programming the firmware as needed.
   b. If using HSPI or SDIO as host interface, then firmware programming or update can be done through the host MCU, or if designer prefers to program standalone at manufacturing, then it is recommended to have test points on the HSPI or SDIO signals.
2. The reference schematics should be followed for optimal RF performance.
3. Use recommended MPNs (Manufacturer Part Number) shown near components wherever possible.

8.1.1 System Supplies

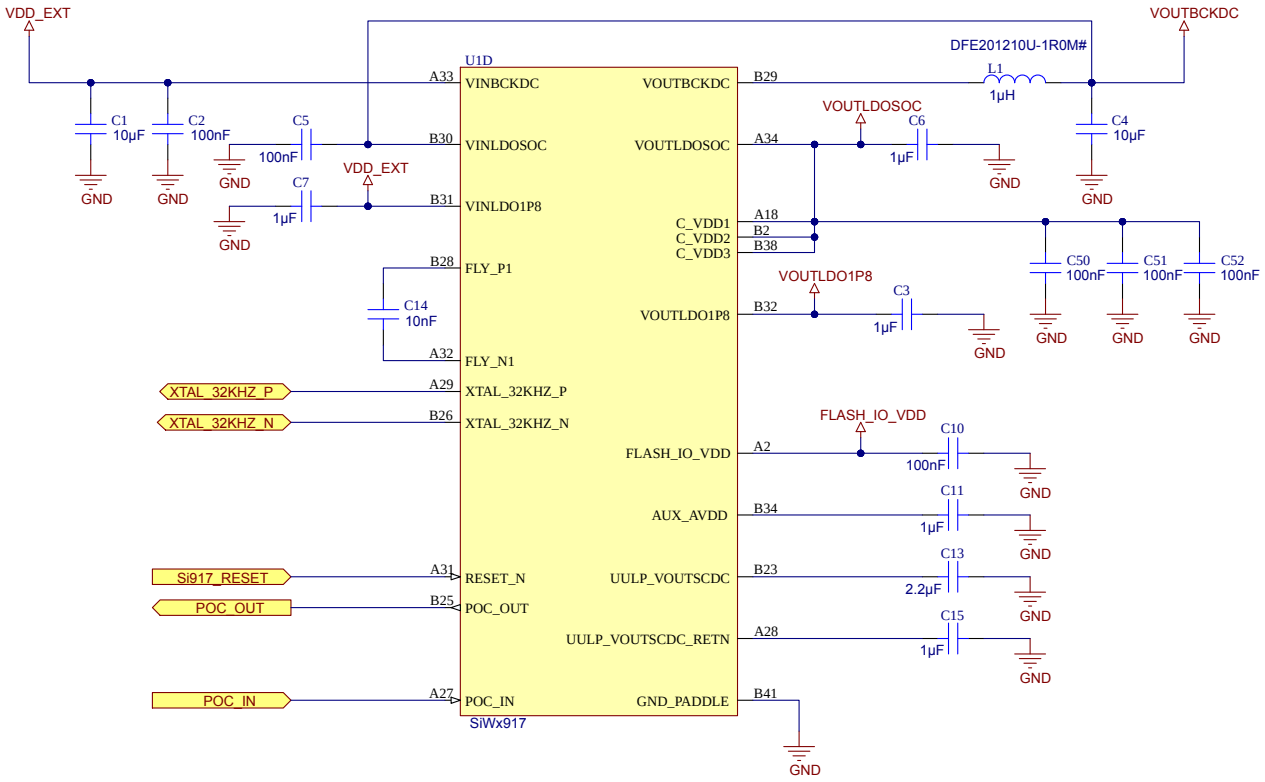


Figure 8.1. System Power Supplies

Note:

1. Place all the decoupling capacitors close to the IC pins.
2. It is recommended to follow star routing for the supply pins from main supply source and add test points to all supply pins.
3. VDD_EXT supply voltage must match the recommended operating conditions of power supply pins.

8.1.2 RF Supplies

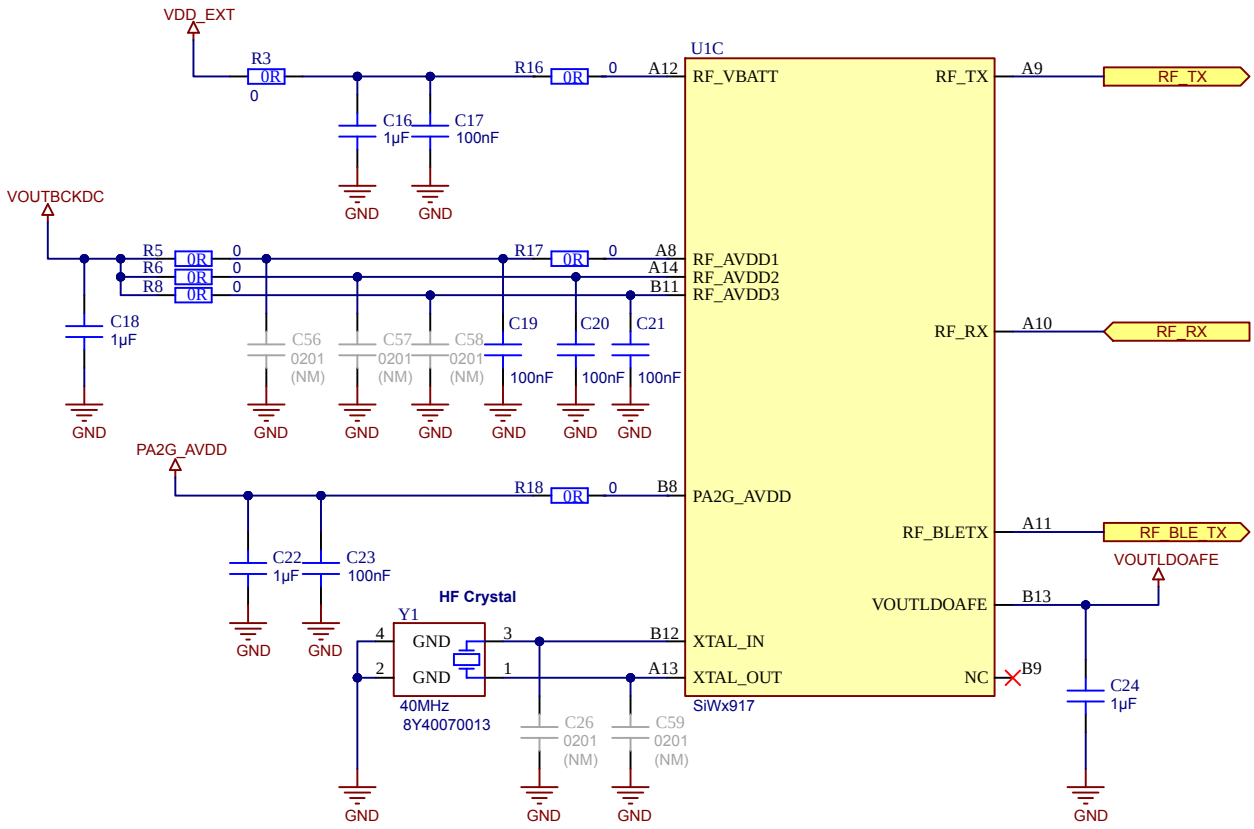


Figure 8.2. RF Power and HF Crystal Support

Note:

1. Do not share routing between PA2G_AVDD and RF_VBATT. Use star routing for PA2G_AVDD and RF_VBATT.
2. VOUTBCKDC should be star routed to RF_AVDD supply pins.
3. VDD_EXT supply voltage must match the recommended operating conditions of power supply pins.
4. Use recommended part for high frequency crystal 40 MHz. This 40 MHz crystal can be tuned with the internal capacitors in the device.
5. PA2G_AVDD can be independent of other supplies and it must be operated at 3.3V only.
6. C26 and C59 are optional tuning capacitors.
7. R5, C56, R6, C57, R8 and C58 are placeholder components for power supply noise filtering.
8. R3 is a placeholder component for power supply noise filtering.
9. It is recommended to add test points to all supply pins.
10. R16, R17, R18 are placeholder components for 2.4 GHz Harmonics filtering. Place these close to the IC pins. If needed, these resistors should be replaced with inductors selected based on their self-resonance frequency being close to the harmonic(s) to be attenuated.
11. C24 component on VOUTLDOAFE must be mounted, either for Internal or External switch RF frontend design shown in Section 8.1.4.

8.1.3 GPIO Supplies

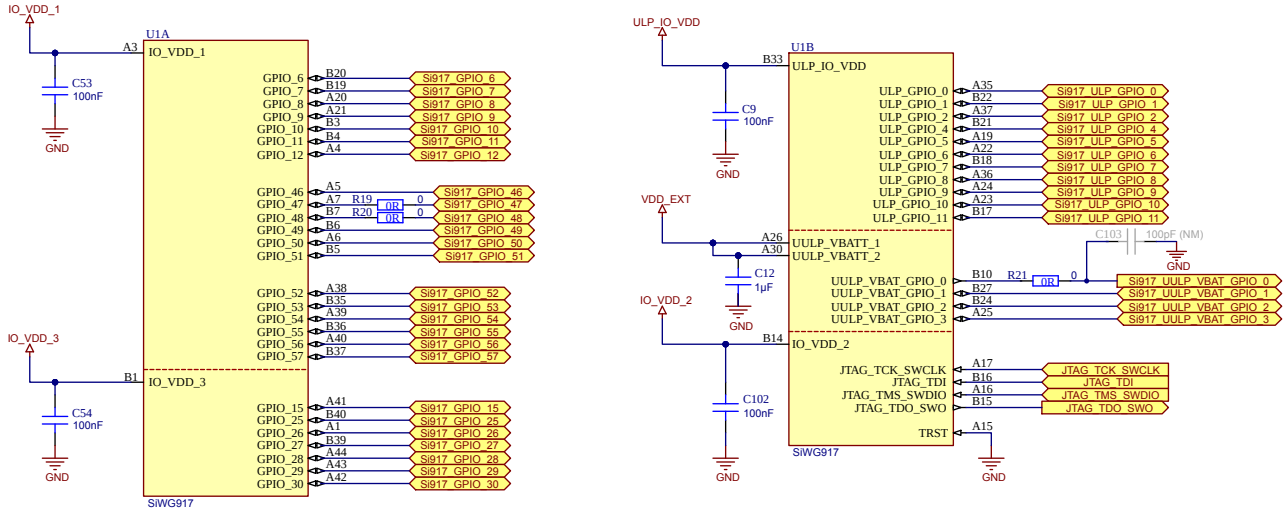


Figure 8.3. GPIO Supply Domains

Note:

1. IO_VDD_1, IO_VDD_2, IO_VDD_3, ULP_IO_VDD can be powered independently by different Voltage Sources based on their corresponding signals voltage levels requirements. Voltages must be as per the recommended Operating conditions.
2. Place C12 close to UULP_VBATT_2 pin.
3. If 917 IC variant with in-package flash is used, IO_VDD_1 supply can be either 1.8 V or 3.3 V based on the peripherals connected on GPIO 6:12 and GPIO 46:57. If external PSRAM or external flash is connected on GPIO 46:57, then the signalling voltage on GPIO_6 to GPIO_12 must be same as external PSRAM/flash supply voltage.
4. Even if GPIOs are not used, their respective IO domains must still be connected to the power supply.
5. VDD_EXT supply voltage must match the recommended operating conditions of power supply pins.
6. It is recommended to add test points to all supply pins.
7. R19, R20, R21 are placeholder components for 2.4 GHz Harmonics filtering. Place these close to the IC pins. If needed, these resistors should be replaced with inductors selected based on their self-resonance frequency being close to the harmonic(s) to be attenuated.
8. C103 is placeholder component for improving Bluetooth Receiver sensitivity performance at 125 kbps data rate. Mount 100 pF capacitor, if required. Place it close to the resistor.

8.1.4 RF Frontend

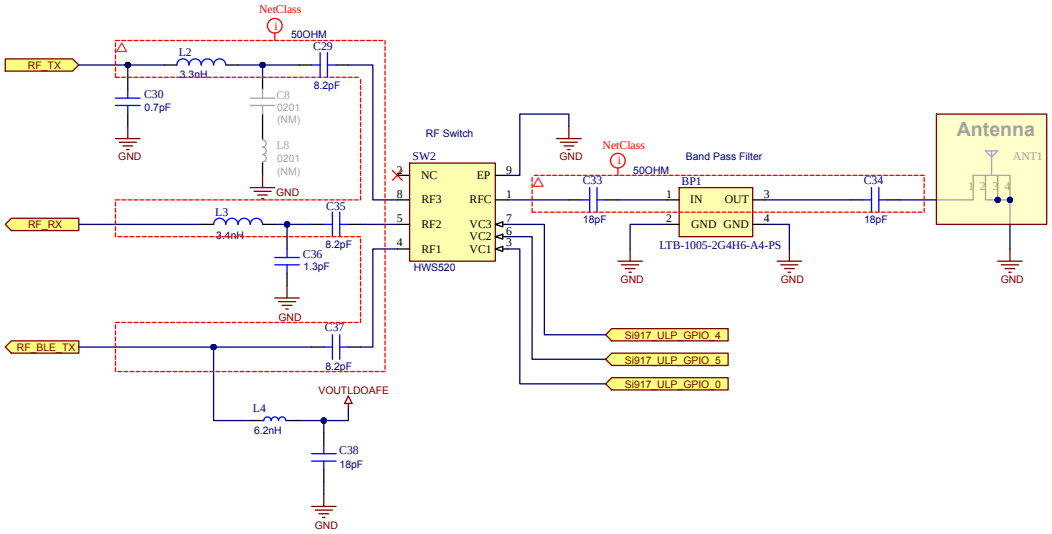


Figure 8.4. Option 1: RF Frontend with External Switch

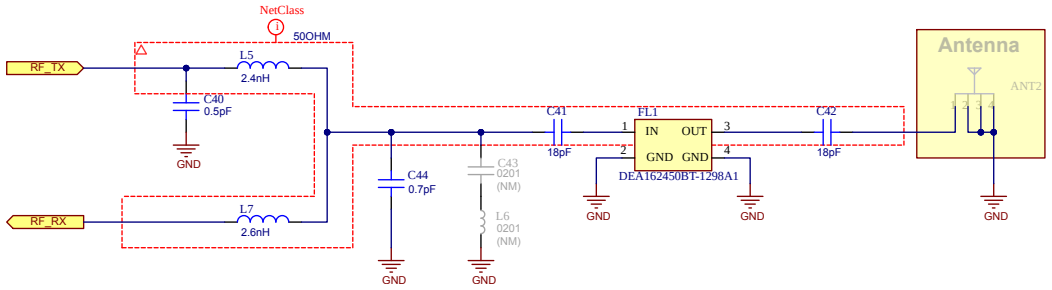


Figure 8.5. Option 2: RF Frontend with Internal Switch

Note:

1. ANT1 and ANT2: In-built antenna or an external antenna (with U.FL connector) can be used.
2. The 8 dBm BLE LP transmit path on RF_BLETX is not available for the internal switch option.
3. Maintain 50 ohm characteristic impedance for RF traces.
4. It is recommended to add microwave coaxial switch connector (Example : Murata's MM8430-2610RA1) or U.FL connector for conducted measurements.
5. Additional matching circuit to be provided near the antenna, based on antenna used and location on the board.
6. For the external RF switch option, follow the reference layout for RF front-end circuit from IC pins up to at least RF switch.
   - Provision C38 on the VOUTLDOAFE trace. C38 must be placed close to L4.
   - Trace routing from the VOUTLDOAFE pin to inductor L4 must be short, with a maximum length of 15 mm.
   - If the trace length is between 7.5 mm and 15 mm, mount capacitor C38.
7. For the internal RF switch option, follow the reference layout for RF front-end circuit from IC pins up to at least the FL1 band pass filter.
8. C8 and L8 (external switch) or C43 and L6 (internal switch) are placeholder components for harmonic emission filtering.
9. Follow guidelines in Application Note AN1440 for calibrating the power of RF front-end circuitry.
10. Follow guidelines in Application Note AN1423 for RF design related aspects.
11. There will be significant RF performance degradation if antenna select signals (ULP_GPIO_4, ULP_GPIO_5,ULP_GPIO_0) are powered at 1.8 V from the ULP_IO_VDD supply. It is recommended to supply ULP_IO_VDD from the 3.3 V supply.

12. There will be RF performance degradation with the internal RF switch option. Refer to Application Note AN1423 for details.
13. ULP_GPIO_0/4/5 are used to control the switch in external switch configuration. These signals map to the following functions:
    - ULP_GPIO_0: RF_BLETX pin active
    - ULP_GPIO_4: RF_TX pin active
    - ULP_GPIO_5: RF_RX pin active
14. Apart from the required RF Frontend components shown above in either Figure 8.4 or Figure 8.5, C24 is the mandatory component to be mounted on VOUTLDOAFE pin as shown in Figure 8.2, either for Internal or External switch RF frontend design.
15. An RF shield is strongly recommended for designs using an internal RF switch configuration. For external RF switch-based designs, shielding should be provisioned and added as needed based on RF test results.

8.1.5 LF Clock Options

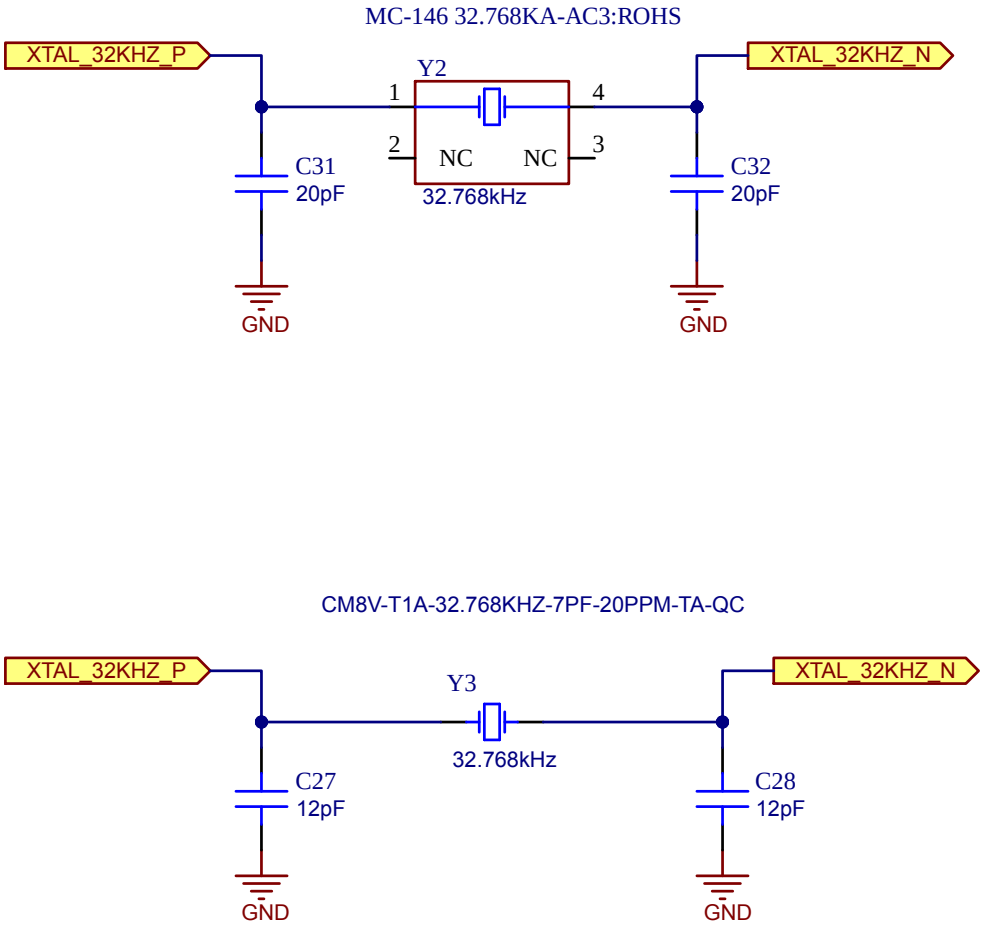


Figure 8.6. 32.768 kHz Clock Options

Note:

1. Two different crystals and their circuits are shown in the figure. Use one of them only.
2. Load capacitors for external crystals must be fine-tuned based on the layout design.

8.1.6 Flash Memory Configurations

Figure 8.7. Option 1: In-Package Common Flash (NWP + MCU) Powered From On-Chip LDO Supply

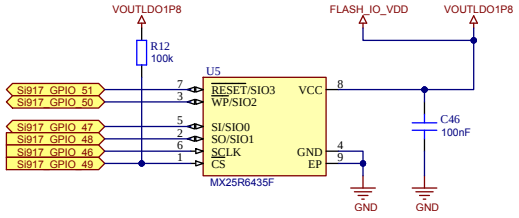


Figure 8.8. Option 2: In-Package NWP Flash + External 1.8 V MCU Flash Powered From On-Chip LDO Supply

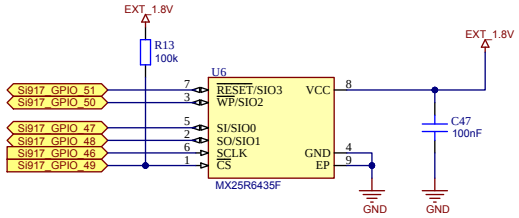


Figure 8.9. Option 3: External 1.8 V Common Flash (NWP + MCU) Powered From External 1.8 V Supply

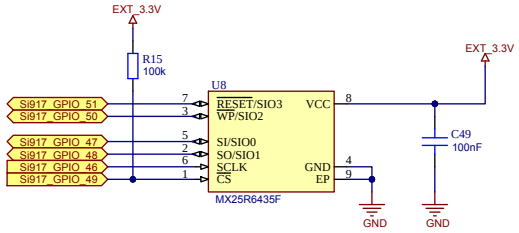


Figure 8.10. Option 4: External 3.3 V Common Flash (NWP + MCU) Powered From External 3.3 V Supply

Note:

1. Option 3 and Option 4 show single common flash to be used with both the NWP and MCU. A dual external flash configuration is also possible. The flash used for NWP must be connected to GPIO 46:51. A second external flash for MCU can be attached to GPIO 52:57.
2. IO_VDD_1 and its corresponding GPIOs in IO_VDD_1 domain must be 1.8 V when 1.8 V external flash is used
3. IO_VDD_1 and its corresponding GPIOs in IO_VDD_1 domain must be 3.3 V when 3.3 V external flash is used
4. See 5.6.1.18 SPI Flash Controllers for more information on external flash interface capabilities, and refer to Application Note AN1494 for recommended external flash ICs.
5. Connect FLASH_IO_VDD pin to the correct power source for all OPNs, regardless of whether the device includes in-package Flash or PSRAM.

8.1.7 PSRAM Memory Configurations

Figure 8.11. Option 1: In-Package PSRAM Powered From On-Chip LDO Supply

Figure 8.12. Option 2: In-Package PSRAM Powered From External 1.8 V Supply

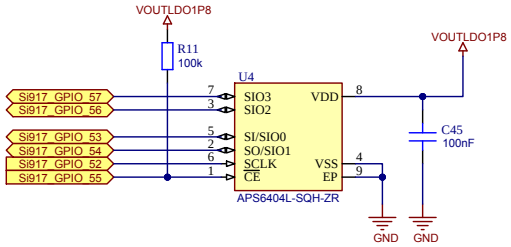


Figure 8.13. Option 3: External PSRAM Powered From On-Chip LDO Supply

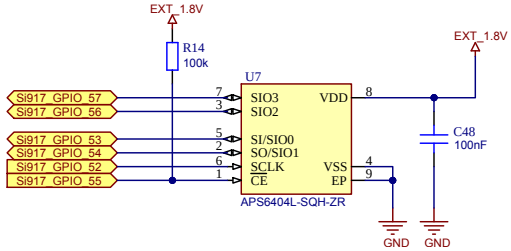


Figure 8.14. Option 4: External PSRAM Powered From External 1.8 V Supply

Note:

1. IO_VDD_1 and its corresponding GPIOs in the IO_VDD_1 domain must be same as PSRAM supply in case of external PSRAM.
2. Either GPIO 46:51 or GPIO 52:57 can be used as the external PSRAM interface. For external common flash mode, the flash device must be connected to GPIO 46:51, and PSRAM must be connected to GPIO 52:57.
3. Standby associated current numbers vary based on the above option used.
4. The reference schematics represent a sample of configurations. See 5.6.1.20 FLASH and PSRAM Supply Connections for more details on possible configurations.
5. Refer to Application Note AN1494 for recommended external PSRAM ICs.
6. Connect FLASH_IO_VDD pin to the correct power source for all OPNs, regardless of whether the device includes in-package Flash or PSRAM.

8.1.8 Reset

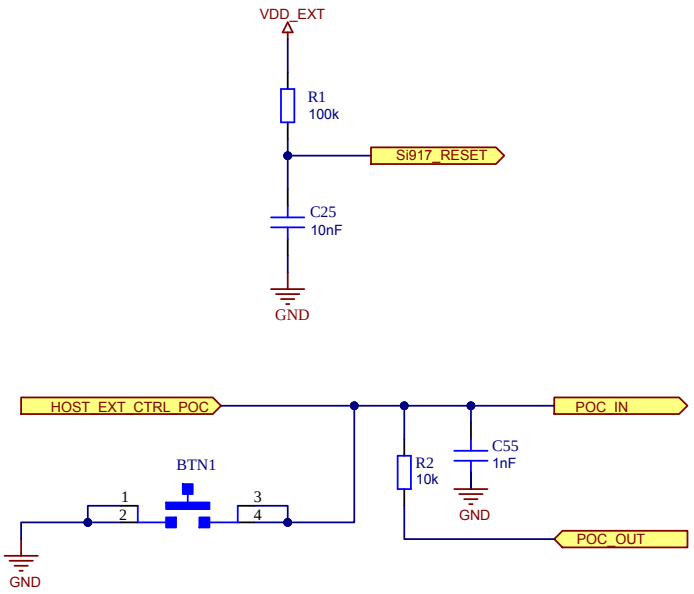


Figure 8.15. Reset Configuration

Note:

1. The configuration shown allows for blackout monitor functionality along with external reset of the SiWx917 IC.
2. The POC_IN signal connects to the POC_IN pin on the SiWx917. POC_IN resets all the internal blocks of the IC.
3. The Si917_RESET signal connects to the RESET_N pin on the SiWx917. It is recommended to use the RC filter as shown. RESET_N is an open-drain output pin that will be pulled low when POC_IN goes low.
4. The POC_OUT signal connects to the POC_OUT pin on the SiWx917. POC_OUT is an active-low, push-pull output from the internal blackout monitor. In this configuration, it is isolated from the external HOST_EXT_CTRL_POC signal with a series resistor. In applications without external host control (HOST_EXT_CTRL_POC), POC_OUT may be directly connected to POC_IN. Without external host control to the POC_IN pin, the IC cannot be reset multiple times after power-on.
5. The HOST_EXT_CTRL_POC signal connects to a GPIO of an external host processor. In this configuration, HOST_EXT_CTRL_POC must be an open-drain output to allow POC_OUT to control POC_IN.
6. VDD_EXT must be at the same voltage level as the UULP_VBATT_2 supply pin.
7. HOST_EXT_CTRL_POC must be at the same voltage level as the UULP_VBATT_1 supply pin.

8.1.9 Debug and In-System Programming

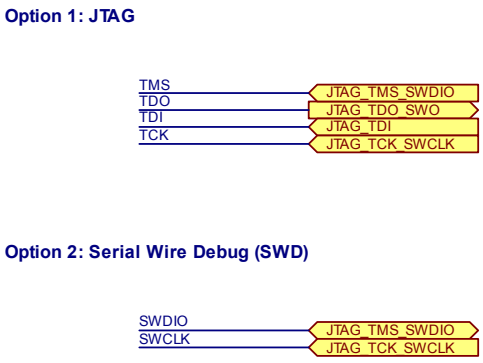


Figure 8.16. JTAG or Serial Wire Debug Interface

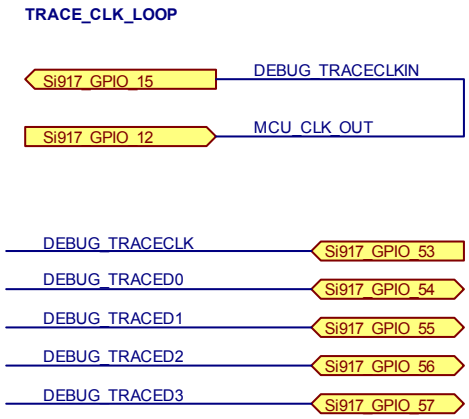


Figure 8.17. ETM Trace Interface

Note:

1. It is recommended to use GPIO 53:57 for ETM trace. GPIO 47:51 can also be used.
2. If external flash or external PSRAM are connected on GPIO 46:51 and GPIO 52:57 then ETM trace is not available.
3. Connect each of these pins to test point for debugging purposes, irrespective of whether JTAG or Serial Wire debug interface is used - JTAG_TCK_SWCLK, JTAG_TDI, JTAG_TMS_SWDIO, JTAG_TDO_SWO.

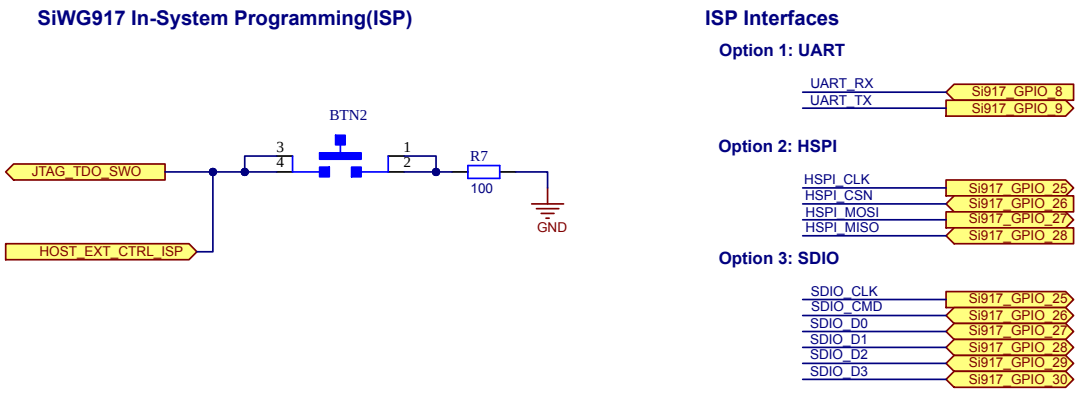


Figure 8.18. In-System Programming (ISP) Options

Note:

1. In UART mode, ensure that the input signal, UART_RX is not floating when the device is powered up and reset is de-asserted. This can be done by ensuring that the host processor configures its signals (outputs) before de-asserting the reset.
2. In HSPI mode, ensure that the input signals, HSPI_CSN and HSPI_CLK are not floating when the device is powered up and reset is de-asserted. This can be done by ensuring that the external Host processor configures its signals (outputs) before de-asserting the reset. HSPI_INTR is the interrupt signal driven by the secondary device. This signal may be configured as Active-high or Active-low. If it is active-high, an external pull-down resistor is required. If it is active-low, an external pull-up resistor is required.

   The following actions can be carried out by the host processor during power-up of the device, and before/after ULP Sleep mode.

   a. To use the signal in the Active-high or Active-low mode, ensure that during the power up of the device, the Interrupt is disabled in the Host processor before de-asserting the reset. After de-asserting the reset, the Interrupt needs to be enabled only after the HSPI initialization is done and the Interrupt mode is programmed to either Active-high or Active-low mode as required.

   b. The Host processor needs to disable the interrupt before the ULP Sleep mode is entered and enable it after HSPI interface is reinitialized upon wakeup from ULP Sleep.
3. In SDIO mode, pull-up resistors should be present on SDIO_CMD & SDIO Data lines as per the SDIO physical layer specification version 2.0.
4. HOST_EXT_CTRL_ISP must be at the same voltage level as IO_VDD_2.
5. IC enters ISP mode by driving JTAG_TDO_SWO low.

8.2 BOM

Manufacturer part numbers provided in this section are a guideline, and may be replaced with suitably equivalent components as needed. Device characteristics and performance are measured using the specified crystals, supply filtering, and RF frontend circuitry.

Table 8.1. SiWG917 Circuitry: Mandatory Components (Power Management + Crystal + SiWG917 IC)

S.No.	Quantity	Designator	Value	Manufacturer	Manufacturer PN	Description
1	1	C1	10 µF	Murata	GRM188R61C106MAALD	CAP CER 0603 X5R 10uF 16V 20%
2	10	C2, C5, C9, C10, C50, C51, C52, C53, C54, C102	100 nF	Murata	GRT155R71H104KE01D	CAP CER 0402 X7R 0.1uF 50V 10%
3	10	C3, C6, C7, C11, C12, C15, C16, C18, C22, C24	1 µF	Murata	GRM033R61C105ME15D	CAP CER 0201 X5R 1uF 16V 20%
4	1	C4	10 µF	CalChip	GMC21X7R106K25NT	CAP CER 0805 X7R 10uF 25V 10%
5	1	C13	2.2 µF	Murata	GRM033R61A225ME47D	CAP CER 0201 X5R 2.2uF 10V 20%
6	1	C14	10 nF	Murata	GRM033R61C103KA12D	CAP CER 0201 X5R 10nF 16V 10%
7	5	C17, C19, C20, C21, C23	100 nF	Murata	GRM033R61C104KE14J	CAP CER 0201 X5R 100nF 16V 10%
8	1	L1	1 µH	Murata	DFE201210U-1R0M=P2	IND Fixed 0805 1uH 2A 95mOhm 20%
9	10	R3, R5, R6, R8, R16, R17, R18, R19, R20, R21	0 Ω	Yageo	RC0201FR-07200RL	RES 0201 0R
10	1	U1	SiWG917	Silicon Labs	SiWG917	Choose a suitable OPN from the OPN list in Ordering Information.
11	1	Y1	40 MHz	TXC	8Y40070013	CRYSTAL 2.0X1.6mm 40MHz 8pF 8ppm

Table 8.2. SiWG917: RF Front-End Options (One of these options must be used)

S. No.	Quantity	Designator	Value	Manufacturer	Manufacturer PN	Description
Option 1: RF Matching +External RF Switch + Band Pass Filter						
12	1	ANT1	2.45 GHz	Johanson	2450AT18D0100001	ANT SMD 3.2X1.6X1.2MM 2.4GHz
13	1	BP1	2.45 GHz	Maglayers	LTB-1005-2G4H6-A4-PS	FILTER BAND PASS 0402-4Pin 2.45GHz 100MHz
14	3	C29, C35, C37	8.2 pF	Murata	GJM0335C1E8R2BB01	CAP CER 0201 C0G 8.2pF 25V ±0.1pF
15	1	C30	0.7 pF	Murata	GJM0335C1HR70WB01	CAP CER 0201 C0G 0.7pF 50V ±0.05pF
16	2	C33, C34, C38	18 pF	Murata	GRM0335C1H180GA01	CAP CER 0201 C0G 18pF 50V 2%
17	1	C36	1.3 pF	Murata	GJM0335C1E1R3WA01D	CAP CER 0201 C0G 1.3pF 50V ±0.05pF
18	1	L2	3.3 nH	Murata	LQP03HQ3N3B02	IND Fixed 0201 3.3nH 500mA 170mOhm ±0.1nH
19	1	L3	3.4 nH	Murata	LQP03TN3N4C02	IND Fixed 0201 3.4nH 450mA 250mOhm ±0.2nH
20	1	L4	6.2 nH	Murata	LQP03HQ6N2H02	IND Fixed 0201 6.2nH 400mA 250mOhm 3%
21	1	SW2	HWS520	Hexawave	HWS520	IC RF SWITCH SP3T 6GHz USON8L
Option 2: Internal RF Switch + Matching+BPF						
22	1	ANT2	2.4 GHz	Johanson	2450AT18D0100001	ANT SMD 3.2X1.6X1.2MM 2.4GHz
23	2	C41, C42	18 pF	Murata	GJM0335C1E180GB01D	CAP CER 0201 C0G 18pF 25V 2%
24	1	C40	0.5 pF	Murata	GJM0335C1ER50WB01	CAP CER 0201 C0G 0.5pF 25V ±0.05pF
25	1	C44	0.7 pF	Murata	GJM0335C1ER70WB01	CAP CER 0201 C0G 0.7pF 25V ±0.05pF
26	1	FL1	2.45 GHz	TDK	DEA162450BT-1298A1	FILTER BAND PASS 1608 2400MHz 2500MHz
27	1	L5	2.4 nH	Murata	LQP03TN2N4B02	IND Fixed 0201 2.4nH 500mA 200mOhm ±0.1nH
28	1	L7	2.6 nH	Murata	LQP03TN2N6B02	IND Fixed 0201 2.6nH 500mA 200mOhm ±0.1nH

Table 8.3. SiWG917: External 32.768 kHz Clock Options

S. No.	Quantity	Designator	Value	Manufacturer	Manufacturer PN	Description
Option 1a: 32.768 kHz Crystal						
29	1	Y2	32.768 kHz	Epson	MC-146 32.768KA-AC3:ROHS	CRYSTAL 7.0x1.5mm 32.768kHz 9pF 20ppm
30	2	C31, C32	20 pF	Murata	GRM0335C1H200GA01	CAP CER 0201 C0G 20pF 50V 2%
Option 1b: 32.768 kHz Crystal						
31	2	C27, C28	12 pF	Murata	GRM0335C1H120FA01	CAP CER 0201 C0G 12pF, 50V, 1%
32	1	Y3	32.768 kHz	Micro Crystal	CM8V-T1A-32.768KHZ-7PF-20PPM-TA-QC	CRYSTAL 2.0x1.2mm 32.768kHz 7pF 20ppm

Table 8.4. SiWG917: External Flash & PSRAM BOM Options (these are optional and need not be used for every use-case)

S. No.	Quantity	Designator	Value	Manufacturer	Manufacturer PN	Description
33	5	C45, C46, C47, C48, C49	100 nF	Murata	GRM033R61C104KE14J	CAP CER 0201 X5R 100nF 16V 10%
34	5	R11, R12, R13, R14, R15	100 kΩ	Yageo	RC0201FR-07100KL	RES 0201 100K 1/20W 1% 200ppm
35	2	U4, U7	APS6404L-SQH-ZR	AP Memory	APS6404L-SQH-ZR	IC PSRAM 64Mbit QSPI USON8
36	3	U5, U6, U8	MX25R6435F	Macronix	MX25R6435FM2IL0	IC FLASH 64MBIT SPI/QUAD 8SOP

Table 8.5. SiWG917: Discrete Parts (BTN1, BTN2 are optional and need not be used for every use-case)

S. No.	Quantity	Designator	Value	Manufacturer	Manufacturer PN	Description
37	2	BTN1,BTN2	PTS810 SJM 250 SMTR LFS	C&K	PTS810 SJM 250 SMTR LFS	Tactile Switch SPST-NO 0.05A 16V
38	1	R1	100 kΩ	Yageo	RC0201FR-07100KL	RES 0201 100K 1/20W 1% 200ppm
39	1	C25	10 nF	Murata	GRM033R61C103KA12D	CAP CER 0201 X5R 10nF 16V 10%
40	1	R2	10 kΩ	Yageo	RC0201FR-0710KL	RES 0201 10K 1/20W 1% 200ppm
41	1	R7	100 Ω	Yageo	RC0201FR-07100RL	RES 0201 100R 1/20W 1% 200ppm
42	1	C55	1 nF	Murata	GRM033R71C102KA01D	CAP CER 0201 X7R 1nF 16V 10%

8.3 Layout Guidelines for DR-QFN

The following guidelines outline the integration of the DR-QFN:

1. The following supply pins must be star routed from the supply source:
   a. VINBCKDC
   b. VINLDO1P8
   c. IO_VDD_1, IO_VDD_2, IO_VDD_3
   d. ULP_IO_VDD
   e. UULP_VBATT_1
   f. UULP_VBATT_2
   g. RF_VBATT
   h. PA2G_AVDD
2. The RF traces must have a characteristic impedance of 50 Ohms. Any standard 50 Ohms RF trace (Microstrip or Coplanar wave guide) may be used. The width of the 50 Ohms line depends on the PCB stack, e.g., the dielectric of the PCB, thickness of the copper, thickness of the dielectric and other factors. Consult the PCB fabrication unit to get these factors right.
3. Each GND pin must have a separate GND via.
4. All decoupling capacitors placement must be as much close as possible to the corresponding power pins, and the trace lengths as short as possible.
5. Ensure all power supply traces widths are sufficient enough to carry corresponding currents.
6. Add GND copper pour underneath IC in all layers, for better thermal dissipation.
7. Provision an RF shield around the IC and RF circuitry, excluding antenna portion. RF shield requirements depend on the matching circuit type, refer to section 8.1.4 RF Frontend for the details.
8. Refer to RF Matching and Layout Design Guide Application Note AN1423 for more details about following RF related design aspects.
9. Add 5 x 5 thermal vias (25 total) of at least 10-mils drill size equally placed on the "GND paddle" for better thermal dissipation.
10. The layout guidelines for the buck DC-DC are as follows:

    Minimize the loop area formed by inductor switching node, output capacitors & input capacitors. This helps keep high current paths as short as possible. Keeping high current paths shorter and wider would help decrease trace inductance & resistance. This would significantly help increase the efficiency in high current applications. This reduced loop area would also help in reducing the radiated EMI that may affect nearby components.

    a. The capacitor for VINBCKDC (C1) should be very close to the IC pin and the ground pad of the capacitor should have direct vias to the ground plane.
    b. The inductor (L1) should be close to IC pin VOUTBCKDC and the buck capacitor (C4) should be placed close to the inductor. The ground pad of the capacitor should have direct vias to the ground plane underneath.
    c. The ground plane underneath the buck inductor (L1) in the top layer should be made as an isolated copper patch and should descend down to the main ground layer through multiple vias.
    d. The path from VOUTBCKDC to VINLDOSOC is a high current path. The trace should be as short and wide as possible and it is recommended to run grounded shield traces on either side of this high current trace.
    e. The capacitor on VINLDOSOC (C4) should be very close to the IC pin & the ground pad of the capacitor should have direct vias to the ground plane underneath.
11. Refer to Silicon Labs' radio board designs and Application Note AN1423 for layout examples.

8.4 Calibration Requirements

The IC design circuit, as shown in Section 8.1 Schematics, involves discrete components in the RF path and 50-ohm PCB traces. There can be variations in manufacturing tolerances from these discrete components and part-to-part IC variation leading to board-to-board performance variation in power level.

Accurate control over TX power is required for regulatory purposes. It is recommended that one performs TX Gain offset calibration on the end-product to compensate for these board-to-board power variations. This requires provision for conducted power measurement on end-product. If the customer does not have the capability for conducted power measurement and this calibration, then fixed TX power back off may be required to ensure regulatory compliance.

Refer to the following Application Notes for detailed calibration procedures:

- Application Note AN1436 for calibrating the external 40 MHz crystal.
- Application Note AN1440 for calibrating the power of RF front-end circuitry.

9. Package Specifications

9.1 Package Outline

Table 9.1. Package Dimensions - DR-QFN

Parameter	Value (LxWxH)	Units
Package Dimensions	7 x 7 x 0.85	mm
Tolerance	±0.1	mm

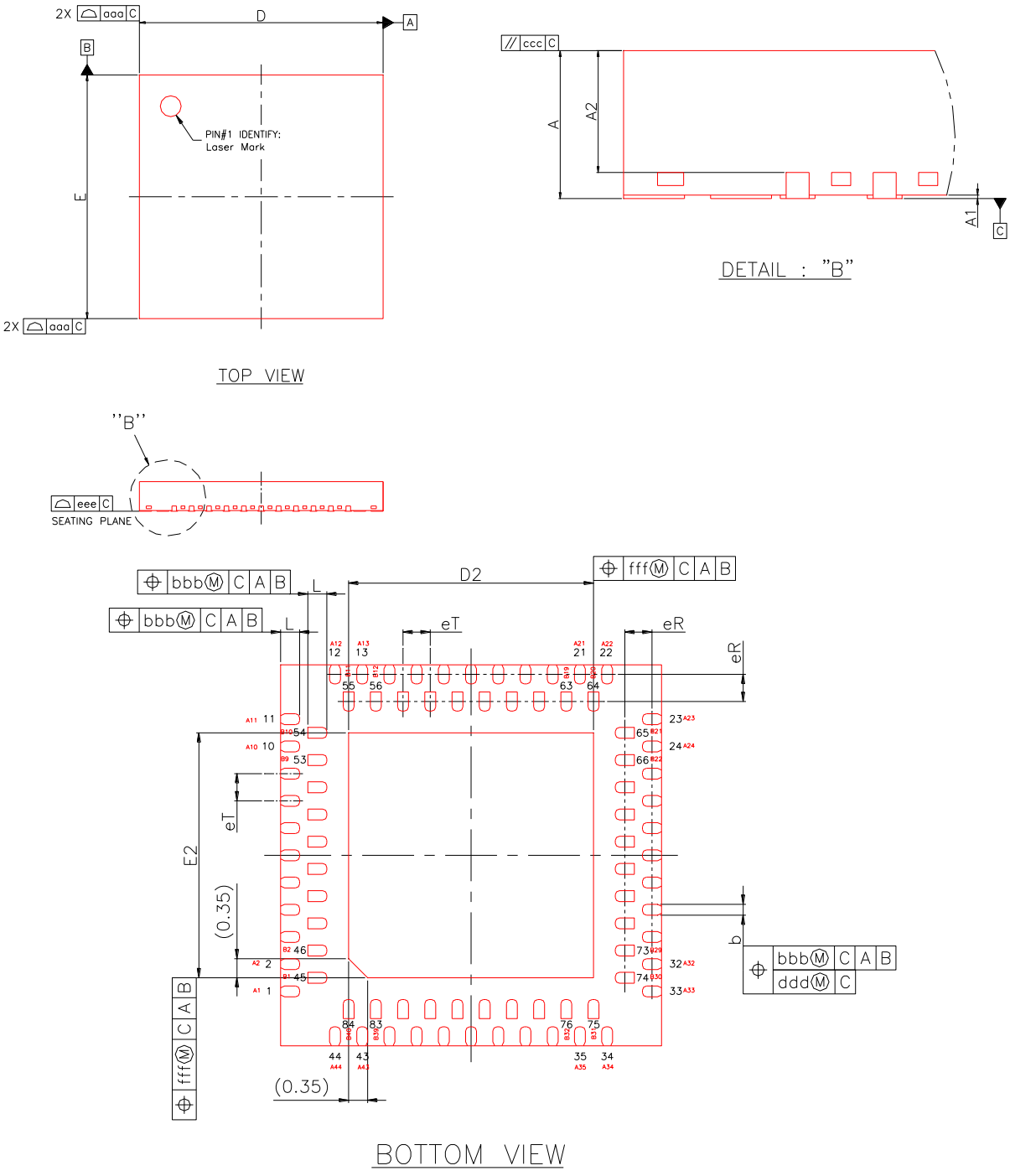


Figure 9.1. Package Outline - DR-QFN

Table 9.2. PCB Landing Pattern - DR-QFN

Dimension	MIN	NOM	MAX
A	0.75	0.85	0.95
A1	0.00	0.02	0.05
A2	0.65	0.70	0.75
b	0.15	0.20	0.25
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D2	4.40	4.50	4.60
E2	4.40	4.50	4.60
eT	0.50 BSC		
eR	0.50 BSC		
L	0.30	0.35	0.40
aaa	0.10		
bbb	0.10		
ccc	0.20		
ddd	0.05		
eee	0.08		
fff	0.10		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.2 PCB Land Pattern

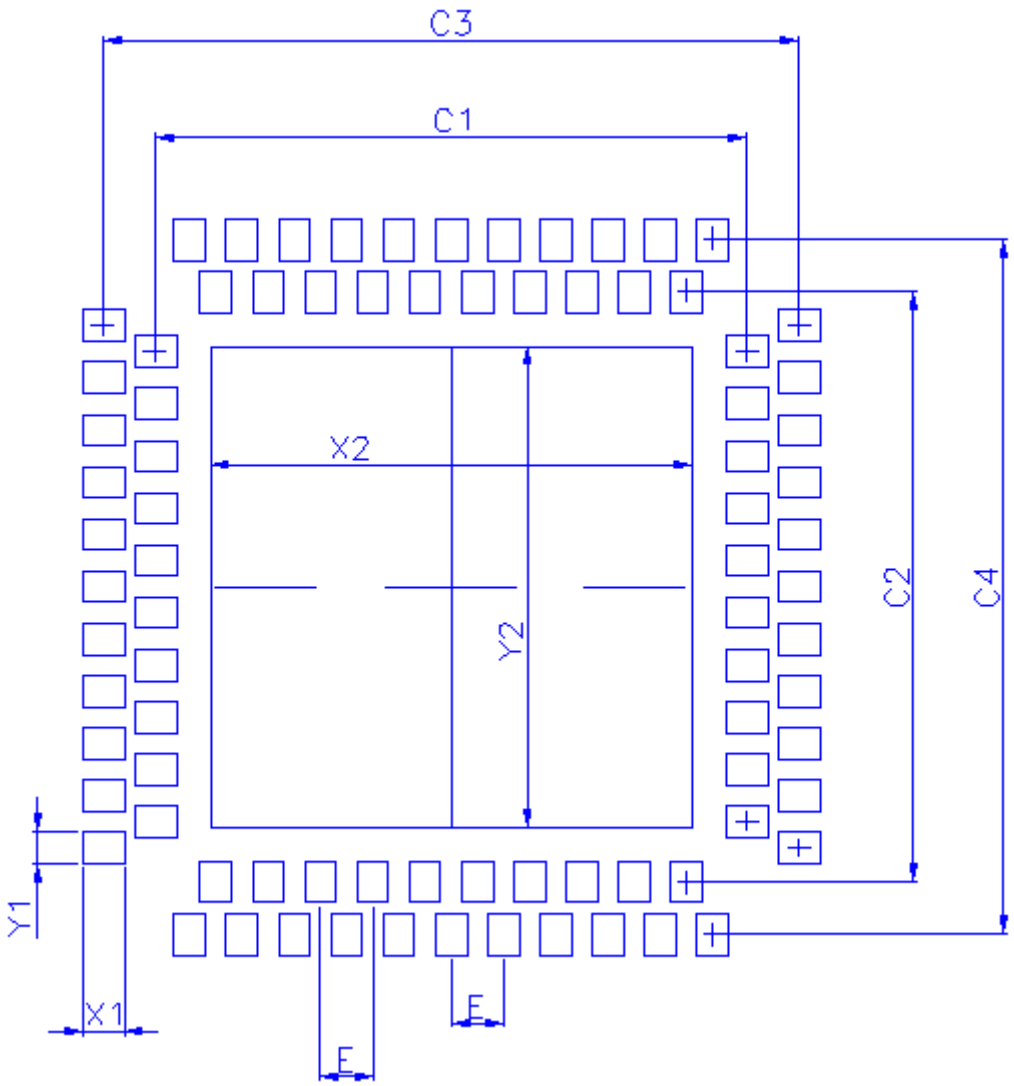


Figure 9.2. PCB Landing Pattern - DR-QFN

Table 9.3. Dimension Table

Dimension	mm
C1	5.65
C2	5.65
C3	6.65
C4	6.65
E	0.5 BSC
X1	0.40
X2	4.60
Y1	0.25
Y2	4.60

Note:

General

1. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.

Solder Mask Design

1. All pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 10 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.100 mm (4 mils).
3. The stencil aperture to land pad size recommendation is 80% paste coverage.

*Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.

9.3 Top Marking

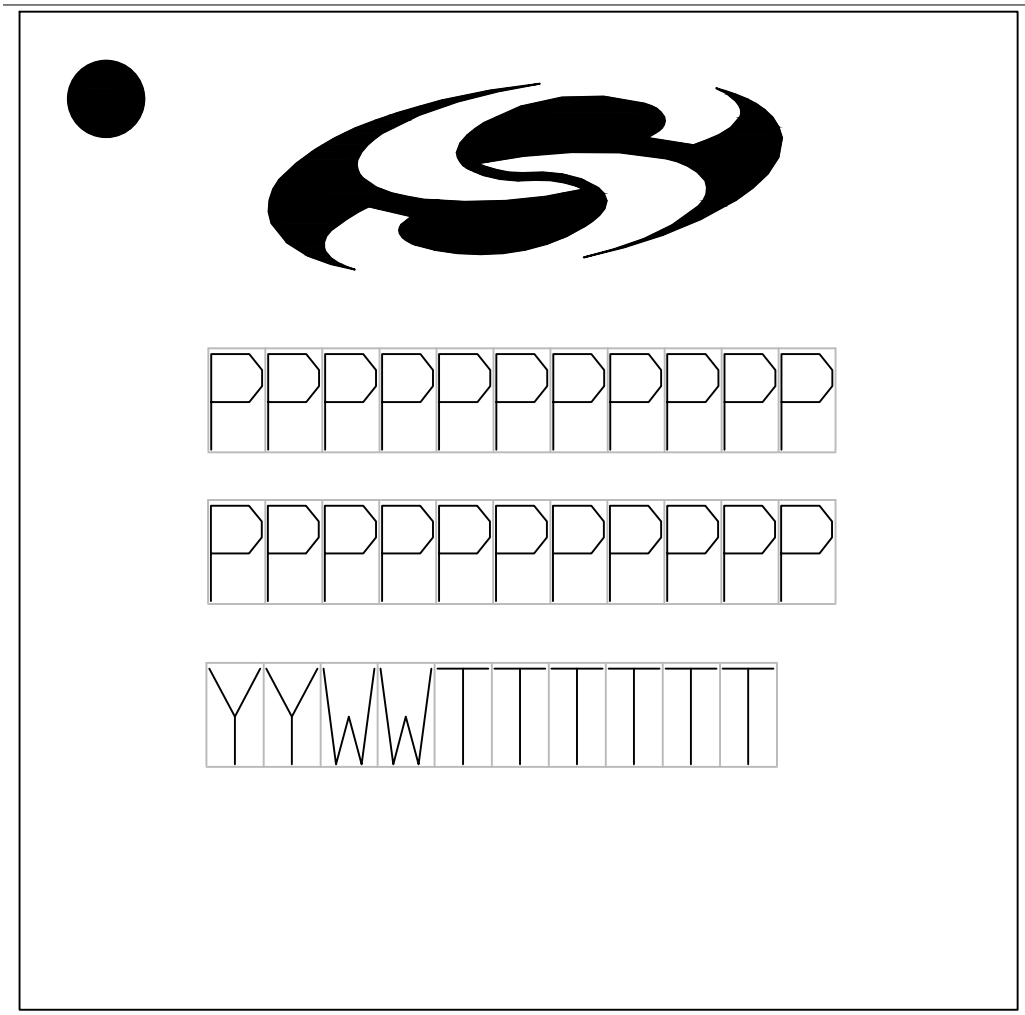


Figure 9.3. Top Marking

Mark Description

The package marking consists of:

- PPPPPPPPPPP - Part number designation in both the rows
- YYWWTTTTTT
  - YY – Last two digits of the assembly year
  - WW – Two-digit workweek when the device was assembled
  - TTTTTT – A trace or manufacturing code. The first letter is the device revision.

10. SiWG917 Documentation and Support

Silicon Labs offers a set of documents which provide further information required for evaluating, and developing products and applications using SiWG917. These documents will be available on the Silicon Labs website. The documents include information related to Software releases, Evaluation Kits, User Guides, Programming Reference Manuals, Application Notes, and others.

For further assistance, you can contact Silicon Labs Technical Support here.

Resource Location

SiWG917 Document Library: https://docs.silabs.com/wiseconnect/latest/wiseconnect-developing-with-wiseconnect-sdk/

Technical Support: http://www.silabs.com/support/

Command Line Development: https://docs.silabs.com/command-line-development/latest/ssv6-command-line-development/

Github: https://github.com/SiliconLabs/wiseconnect

11. Revision History

Revision 1.2

February, 2026

- Replaced MU-MIMO/OFDMA with DL MU-MIMO, DL/UL OFDMA in Key Features section.
- Updated Block Diagram
- Following are the updates in 1. Feature List:
  - Updates in Digital Peripherals:
    - Added General Purpose DMA (GPDMA) controller
    - Added HP Micro-DMA (HP µDMA) controller
  - Updated Bluetooth: 2 Simultaneous BLE Connections (2 Peripheral, 2 Central, or 1 Central & 1 Peripheral) to 10 simultaneous BLE Connections (8 Peripheral & 2 Central).
  - Revised WiSeConnect SDK feature availability from Simplicity Studio and GitHub to Simplicity Studio and Command-Line Development (SLT-CLI).
  - Updated Host Interface Peripherals by replacing SPI with HSPI.
  - Updates in Ultra Low Power (ULP) Peripherals:
    - Removed RTC and BOD from Ultra Low Power (ULP) Peripherals.
    - Updated ULP UDMA to ULP Micro DMA (ULP µDMA).
  - Added Ultra Ultra Low Power (UULP) Peripherals section.
  - Updates in Software and Regulatory Certifications:
    - Updated Bluetooth SIG Qualification to Bluetooth 5.4 Qualification.
    - Updated Regulatory pre-certifications (FCC, IC, RED, UKCA, MIC) to Verified for compliance with FCC, ISED, CE, UKCA, MIC regulatory requirements.
  - Added Host Interface Peripherals section.
  - Removed Advanced Software Features: SoC communication to external host via Co-Processor Communication (CPC) - Supported host interfaces are SDIO.
  - Updated Note section.
- Updated Table 2.2. List of OPNs
- Updated: Figure 4.1. System Block Diagram
- Updated: Figure 4.2. SiWG917 SoC Software Architecture
- Following are the updates in 5. System Overview :
  - Removed D-cache data fetching with PSRAM from 5.2.1 Memory Architecture
  - Updated Table 5.2. MCU APB Peripherals Address Mapping:
    - UDMA to Micro DMA (µDMA)
    - Removed DCACHE.
  - Updated Table 5.3. ULP MCU APB Address Mapping:
    - NPSS_APB to UULP_APB
    - ULP_UDMA to ULP Micro DMA (ULP µDMA)
  - Updated Table 5.4. List of Power Domains: Removed DCACHE functionality from QSPI_ICACHE and TIMESTAMP from UULP-PERIPHERALS.
  - Updated Table 5.7. List of Voltage Domains: Removed DCACHE functionality from HIGH-VOLTAGE-DOMAIN
  - Updated Table 5.9. List of Wakeup Sources in Different States.
  - Updated 5.6.1.16 Micro DMA (µDMA)
  - 5.6.1.20 FLASH and PSRAM Supply Connections: Following are the updates:
    - Removed Table 5.10. PSRAM and Flash Package Options and added a Note about AN1494
    - Removed Table 5.11. Flash
    - Removed Table 5.12. PSRAM
  - Updated 5.6.2.2 Digital to Analog Converter (DAC) Max sampling frequency is 5 MHz for DAC_CLK to Max sampling frequency is 2.5 MHz for DAC_CLK.
  - Replaced SPI with HSPI in sections 5.7 Bootloader, 5.8.5 Secure Zone and 5.8.6 In-System Programming (ISP).
  - Updated 5.11 Bluetooth Two simultaneous BLE connections (2 peripheral or 2 central, or 1 central and 1 peripheral) to 10 simultaneous BLE Connections (8 Peripheral & 2 Central).
  - Added new section 5.13 Host Interface Peripherals and 5.13.1 Auto Host Detection.

- Following are the updates in 6. Pinout and Pin Description
  - Updated FLASH_IO_VDD Description Table 6.1. Chip Packages - RF and Control Interfaces
  - Updated Table 6.3. Chip Packages - Peripheral Interfaces: Replaced HighZ default state with High for GPIO_30/SDIO_D3 pin; Added test points notes for JTAG/SWD pins. Updated JTAG_TDO_SWO description by replacing SPI with HSPI.
  - Updated some of the modes configurations in Table 6.5. SoC GPIO Pin Multiplexing
  - Removed column ULP GPIO Modes 8, 9, 10, 11 Table 6.6. ULP GPIO Pin Multiplexing
  - Removed AGPIO_3 - ULP_GPIO_3 information Table 6.8. Analog Functions for SoC/ULP GPIOs
  - Updated some of the modes configurations in Table 6.9. SoC on ULP GPIO Pin Multiplexing
  - Removed column ULP GPIO Mode = 8, 9, 10, 11 Table 6.10. ULP on SoC GPIO Pin Multiplexing
  - Updated Table 6.11. Peripheral Interface Options
  - Updated 6.5.1 Digital Functions
- Following are the updates in 7. Electrical Specifications
  - Updated Parameter (I/O supply for Flash) to (I/O supply for In-Package Flash/PSRAM) in Table 7.1. Absolute Maximum Ratings.
  - Updated Parameter (I/O supply for Flash) to (I/O supply for In-Package Flash/PSRAM) in Table 7.2. Recommended Operating Conditions.
  - Updated Note Table 7.16. 40 MHz Crystal Specifications.
  - Updated Table 7.44. Power State Wake Timing
  - Updated Table 7.48. ADC Electrical Specifications
  - Updated Table 7.52. WLAN 2.4 GHz Transmitter Characteristics with 3.3 V Supply
  - Updated Table 7.53. WLAN 2.4 GHz Receiver Characteristics on HP RF Chain
  - Updated Table 7.54. WLAN 2.4 GHz Receiver Characteristics on LP RF Chain
  - Updated Table 7.55. Bluetooth Transmitter Characteristics on High-Performance (HP) RF Chain
  - Updated Table 7.56. Bluetooth Transmitter Characteristics on Low-Power (LP) 8 dBm RF Chain
  - Updated Table 7.57. Bluetooth Transmitter Characteristics on Low-Power (LP) 0 dBm RF Chain
  - Updated Table 7.58. Bluetooth Receiver Characteristics for 1 Mbps Data Rate
  - Updated Table 7.59. Bluetooth Receiver Characteristics for 2 Mbps Data Rate
  - Updated Table 7.60. Bluetooth Receiver Characteristics for 125 kbps Data Rate
  - Updated Table 7.61. Bluetooth Receiver Characteristics for 500 kbps Data Rate
  - Updated Table 7.63. Bluetooth LE Current Consumption:
    - Typical current consumption for the 1.28s connected interval parameter by changing the value from 36 µA to 48 µA.
    - Typical current consumption for the 200 ms connected interval parameter by changing the value from 115 µA to 149 µA.
- Following are the updates in 8. Reference Schematics, BOM and Layout Guidelines
  - Updated Note section 8.1.2 RF Supplies
  - Updated Note section 8.1.4 RF Frontend
  - Updated Note section 8.1.6 Flash Memory Configurations
  - Updated Note section 8.1.7 PSRAM Memory Configurations
  - Updated Note section 8.1.9 Debug and In-System Programming
  - Removed C103 part information from Table 8.1. SiWG917 Circuitry: Mandatory Components (Power Management + Crystal + SiWG917 IC)
  - Updated C27, C28 parts information in Table 8.3. SiWG917: External 32.768 kHz Clock Options
  - Updated Point 7 in Section 8.3 Layout Guidelines for DR-QFN
- Updated Resource Location in 10. SiWG917 Documentation and Support:
  - SiWG917 Document Library: https://docs.silabs.com/wiseconnect/latest/wiseconnect-developing-with-wiseconnect-sdk/
  - Command Line Development: https://docs.silabs.com/command-line-development/latest/ssv6-command-line-development/
  - Github: https://github.com/SiliconLabs/wiseconnect

Revision 1.1

July, 2025

- Updated Block Diagram
- Following are the updates in 1. Feature List:
  - Removed MPU (Memory Protection Unit) from the of Cortex-M4.
  - Updated minimum active current from 32 to 40.4 µA/MHz @ 20 MHz in low-power mode.
  - Updated minimum active current from 50 to 70.5 µA/MHz @ 180 MHz in high performance mode.
- Following are the updates in 2. Ordering Information:
  - AI/ML Matrix Vector Processor (MVP) features are available from WiseConnect SDK 3.5.0. Removed Note 2.
- Following are the updates in 4. Block Diagrams:
  - Updated: Figure 4.1. System Block Diagram.
- Following are the updates in 5. System Overview :
  - Removed section "Memory Protection Unit".
  - 5.2.1 Memory Architecture: Removed "Supports memory protection - generates trap if unintended primary accesses the memory".
  - 5.4 Interconnect: Removed IR address mapping from Table 5.3. ULP MCU APB Address Mapping.
  - 5.5.4 Power States : Following are the updates:
    - Updated: Figure 5.2. Power States.
    - Added Note.
  - 5.5.6 Wakeup Sources: Updated Table 5.9. List of Wakeup Sources in Different States.
  - 5.6.1.8 Secure Digital I/O (SDIO) Secondary Interface: Updated content from " Supports up to five functions" to " Supports only function 1".
  - State Configurable Timer (SCT): Following are the updates:
    - 32-bit configuration timer option for SCT is not supported.
    - Removed the content "It can start the ADC at any time in sync with PWM signal".
  - 5.6.1.20 FLASH and PSRAM Supply Connections: Following are the updates:
    - Corrected the table header from Flash Density (in Mbit) to ‘PSRAM Density (in Mbit)’ in Table 5.12 on page 41.
    - Updated Table 5.10. Estimated Deepsleep/DTIMs current with PSRAM for different input supply options with VBATT = 3.3V supply.
  - Renamed ‘First-party DMA ports’ to ‘Memory access ports’ in 5.6.1.25 MVP.
- Following are the updates in 6. Pinout and Pin Description
  - Fixed the description of RF_RX pin in Table 6.1. Chip Packages - RF and Control Interfaces.
  - Removed the wording "Recommended" from the heading of Table 6.11. Peripheral Interface Options.
- Following are the updates in 7. Electrical Specifications
  - 7.5.4 Analog to Digital Converter : Following are the updates:
    - Content added: ADC performance not guaranteed below -20 ^{o}C.
    - ADC Electrical Specification: ADC gain error (typical) changed to 2 % (removed min and max specs)
    - ADC Electrical Specification: ADC offset error (typical) changed to 10 mV (removed min and max specs)
  - 7.5.5 Digital to Analog Converter: Content added: DAC performance not guaranteed below -20 ^{o}C.
  - Corrected BLE data rates related to FCC compliance and noted that channel 2480 MHz is not supported in 2 Mbps in 7.6.4 Bluetooth Transmitter Characteristics on High-Performance (HP) RF Chain, 7.6.5 Bluetooth Transmitter Characteristics on Low-Power (LP) 8 dBm RF Chain, and 7.6.6 Bluetooth Transmitter Characteristics on Low-Power (LP) 0 dBm RF Chain.
  - Corrected pin name to RF_RX in 7.6.6 Bluetooth Transmitter Characteristics on Low-Power (LP) 0 dBm RF Chain.
  - Added Cortex-M4 condition in 7.7.1 WLAN 2.4 GHz 3.3 V Current Consumption.
  - 7.7.3 MCU Power State Current Consumption: Replaced "Ret LDO" with "ULP LDO" in Table 7.64. MCU Power State Current Consumption and updated the table.

- Following are the updates in 8. Reference Schematics, BOM and Layout Guidelines
  - Modified the reference schematics and the BOM in Figure 8.2. RF Power and HF Crystal Support, Figure 8.3. GPIO Supply Domains, and Table 8.1. SiWG917 Circuitry: Mandatory Components (Power Management + Crystal + SiWG917 IC).
  - Updated Note 10 from "R16, R17, R18 are placeholder components for 2.4 GHz Harmonics filtering. Place these close to the IC pins." to "R16, R17, R18 are placeholder components for 2.4 GHz Harmonics filtering. Place these close to the IC pins. If needed, these resistors should be replaced with inductors selected based on their self-resonance frequency being close to the harmonic(s) to be be attenuated." in 8.1.2 RF Supplies.
  - Updated Note 7 from "R19, R20, R21 are placeholder components for 2.4 GHz Harmonics filtering. Place these close to the IC pins." to "R19, R20, R21 are placeholder components for 2.4 GHz Harmonics filtering. Place these close to the IC pins. If needed, these resistors should be replaced with inductors selected based on their self-resonance frequency being close to the harmonic(s) to be attenuated." in 8.1.3 GPIO Supplies.
  - Updated Note 8 from "C103 is placeholder component for improving Bluetooth Receiver sensitivity performance at 125 kbps data rate. Place it close to the pin." to "C103 is placeholder component for improving Bluetooth Receiver sensitivity performance at 125 kbps data rate. Mount 100 pF capacitor, if required. Place it close to the resistor." in 8.1.3 GPIO Supplies.
  - Added R16, R17, R18, R19, R20, R21 placeholder components for 2.4 GHz harmonics filtering.
  - Added C103 placeholder component for an optional 100 pF capacitor for improving Bluetooth Receiver sensitivity performance at 125 kbps data rate.

Revision 1.0

December, 2024

- Removed LVCMOS external 32.768 kHz clock option. A 32.768 kHz crystal is mandatory for all applications requiring accurate timing or low-power Wi-Fi, BLE, and Coex sleep.
- Removed capacitive touch sensor feature.
- Updated hardware block diagram with missing blocks and corrected power state availability key
- Marked PS1 power state with software roadmap superscript in feature list
- Updated language used for security features throughout document
- Figure 5.4. Dual Independent Flash Configuration: Corrected diagram to show external flash on M4 and in-package flash on NWP
- Table 5.9. List of Wakeup Sources in Different States: Updated table to show availability in current SDK
- Table 5.10 PSRAM and Flash Package Options on page 40: Corrected GPIO pins used for Mode 2
- 6.1 Pin Diagram: Corrected name of UULP_VOUTSCDC pin
- 6.2.3 Peripheral Interfaces: Added NWP debug print signals to associated pins
- Table 6.11. Peripheral Interface Options: Corrected PWM_3H possible combination to GPIO_15
- Aligned signal naming for SSI_ULP block with software, using ULP_SSI_signal
- 7. Electrical Specifications:
  - Added 7.4.8.1 Standard Mode and 7.4.8.3 Fast Mode Plus
  - Added Table 7.44. Power State Wake Timing
  - Table 7.64. MCU Power State Current Consumption: Removed PS1 supply current
  - 7.5.1 Analog Comparators : Split voltage reference range into V_{ref_min} and V_{ref_max} lines to express as possible setting range instead of absolute max range
  - Table 7.9. Flash LDO Electrical Specifications - Regulation Mode: Load regulation maximum changed to 3%
  - Removed specification table for internal RC boot oscillator and clarified this is only for boot-up
  - All electrical specifications updated with final char results and test limits
- 8. Reference Schematics, BOM and Layout Guidelines:
  - Updated schematic images with text-searchable versions
  - Corrected manufacturer part details for C36, L2, L3, C41, C42, C40, C44, L5, and L7
  - Added notes for position and usage of capacitor C38

Revision 0.7

September, 2024

- Replaced references to "ThreadArch" with "Network Wireless Processor" and / or "NWP"
- Changed AI/ML mentions to more directly refer to the MVP block capabilities
- Corrected last character of OPN decoder, which is Reserved for these products
- Updated peripheral and signal names for consistency with software libraries
- Corrected package name to DR-QFN throughout document
- Removed unsupported features: SIO, IrDA, RO temperature sensor, SCT input 1-3, SCT output 2-7
- 5.6.1.18 SPI Flash Controllers: Updated section to clarify QSPI operation and note that QSPI only available as flash interface
- Table 5.9. List of Wakeup Sources in Different States: Corrected availability of wake sources in each power state
- 5.6.1.20 FLASH and PSRAM Supply Connections:
  - Removed detailed examples of each supply configuration (moved to AN1494).
  - Simplified Table 5.10 PSRAM and Flash Package Options on page 40, added example OPNs
  - Added example flash and PSRAM external device tables: Table 5.11 Flash on page 41 and Table 5.12 PSRAM on page 41
  - Updated sections describing PSRAM supply connection options
- Updated typical electrical characteristics with characterization results
- 7.1 Absolute Maximum Ratings: Added absolute maximum voltage and current ratings for I/O pins
- Figure 5.1. NWP and M4 shared SRAM memory architecture Corrected 192 KB SRAM bank memory multiplexing
- 7.3.2 Power On Control (POC) and Reset Clarified POC and Reset functionality
- 7.6 RF Characteristics Added supported WLAN channels for different regions
- 8. Reference Schematics, BOM and Layout Guidelines
  - Split schematics into separate figures with in-text notes for legibility
  - Updated component recommendations per final design guidelines
- Figure 9.2. PCB Landing Pattern - DR-QFN: Corrected dimensions C1, C2, C3, C4
- Presentation and formatting changes throughout document, including figure and table title assignments, units, cross-references, specification table formats, GPIO mux table formats, etc.

Revision 0.51

December, 2023

- Updated Table 6.3. Chip Packages - Peripheral Interfaces
- Updated 7.3.5.1 SC-DCDC
- Updated Table 7.8. SoC LDO Electrical Specifications
- Updated Section 7.7.1 WLAN 2.4 GHz 3.3 V Current Consumption

Revision 0.5

November, 2023

- Updated RF specs based on validation data
- Update Power consumption tables and numbers
- Updated Notes in RF performance section based on the validation data.
- Updated Reference schematics section

Revision 0.45

November, 2023

- Updated for IP status

Revision 0.4

September, 2023

- Updated cover page
- Updated Feature List
- Updated Ordering Information
- Updated Applications
- Updated Electrical Specifications
- Updated Boot Process and Bootloader
- Updated Schematics
- Updated PCB Landpattern

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