# EFR32ZG23 Wireless SoC Family Data Sheet

The EFR32ZG23 Z-Wave SoC is an ideal solution for sub-GHz “Internet of Things” for smart home, security, lighting and building automation. The high-performance sub-GHz radio provides long range capabilities and is not susceptible to 2.4 GHz interference from 2.4 GHz technologies like Wi-Fi.

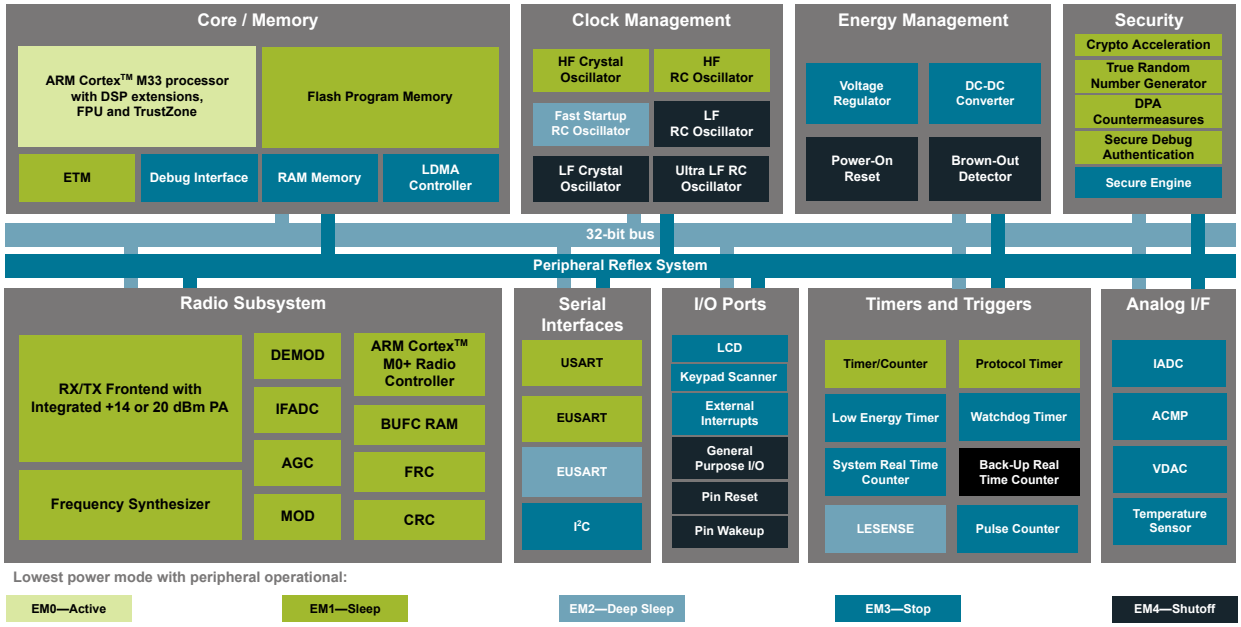
The single die, multi-core solution, provides industry leading security, low power consumption with fast wakeup times, and an integrated power amplifier to enable the next level of secure connectivity for Z-Wave gateways, controllers, and end devices.

EFR32ZG23 applications include:

- Smart Home
- Security
- Lighting
- Building Automation

**KEY FEATURES**

- Low Power Z-Wave Wireless SoC
- 32-bit ARM® Cortex®-M33 core with 78 MHz maximum operating frequency
- Up to 512 kB of flash and 64 kB of RAM
- Integrated sub-GHz PA with up to 20 dBm TX power
- Integrated LNA with RX Sensitivity as low as -109.8 dBm.
- Secure Element with Secure Vault
- Robust peripheral set and up to 31 GPIO

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# 1. Feature List

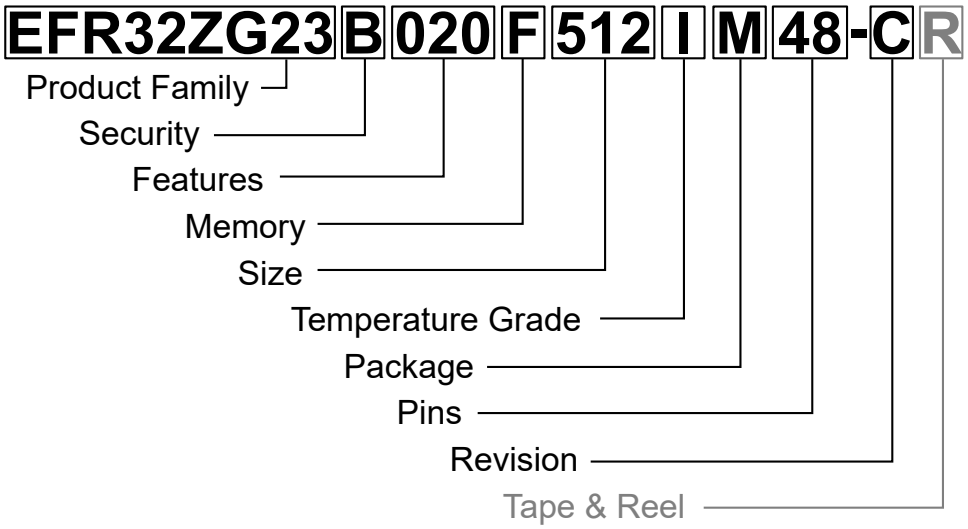
The EFR32ZG23 highlighted features are listed below.

- **Low Power Wireless System-on-Chip**
  - High Performance 32-bit 78 MHz ARM Cortex®-M33 with DSP instruction and floating-point unit for efficient signal processing
  - Up to 512 kB flash program memory
  - Up to 64 kB RAM data memory
  - Sub-GHz radio operation
  - TX power up to +20 dBm
- **Low Energy Consumption**
  - 4.0 mA RX current at 868 MHz (9.6 kbps FSK)
  - 4.0 mA RX current at 868 MHz (100 kbps GFSK)
  - 4.0 mA RX current at 908.42 MHz (9.6 kbps FSK)
  - 4.0 mA RX current at 916 MHz (100 kbps GFSK)
  - 9.8 mA TX current @ 0 dBm output power at 916 MHz
  - 25.0 mA TX current @ 14 dBm output power at 916 MHz
  - 85.5 mA TX current @ 20 dBm output power at 916 MHz
  - 26 µA/MHz in Active Mode (EM0) at 39.0 MHz
  - 1.5 µA EM2 DeepSleep current (64 kB RAM retention and RTC running from LFXO)
  - 1.2 µA EM2 DeepSleep current (16 kB RAM retention and RTC running from LFRCO)
- **High Receiver Performance**
  - -109.9 dBm sensitivity @ 9.6 kbps 868 MHz FSK
  - -110.0 dBm sensitivity @ 40 kbps 868 MHz FSK
  - -108.6 dBm sensitivity @ 100 kbps 868 MHz GFSK
  - -109.3 dBm sensitivity @ 9.6 kbps 908.42 MHz FSK
  - -109.7 dBm sensitivity @ 40 kbps 908.4 MHz FSK
  - -108.1 dBm sensitivity @ 100 kbps 916 MHz GFSK
  - -109.8 dBm sensitivity @ 100 kbps 912 MHz O-QPSK
- **Supported Modulation Format**
  - 2/4 (G)FSK with fully configurable shaping
  - OQPSK DSSS
  - (G)MSK
  - OOK
- **Protocol Support**
  - Z-Wave
  - Z-Wave LR
  - Sidewalk
  - Proprietary
- **Wide Selection of MCU Peripherals**
  - Analog to Digital Converter (ADC)
    - 12-bit @ 1 Msps
    - 16-bit @ 76.9 ksps
  - 2 × Analog Comparator (ACMP)
  - 2-Channel Digital to Analog Converter (VDAC)
  - Low-Energy Sensor Interface (LESENSE)
  - Up to 31 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller
  - 12 Channel Peripheral Reflex System (PRS)
  - 4× 16-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 1× 32-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 32-bit Real Time Counter
  - 24-bit Low Energy Timer for waveform generation
  - 16-bit Pulse Counter with asynchronous operation (PCNT)
  - 2× Watchdog Timer
  - 3× Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)
  - 1× Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/$I^2S$)
  - 2× $I^2C$ interface with SMBus support
  - Integrated Low-Energy LCD Controller supporting up to 80 segments
  - Keypad scanner supporting up to 6×8 matrix (KEYSCAN)
  - Die temperature sensor with ±2 °C typical accuracy across temperature range
- **Secure Vault**
  - Hardware Cryptographic Acceleration for AES128/192/256, ChaCha20-Poly1305, SHA-1, SHA-2/256/384/512, ECDSA +ECDH(P-192, P-256, P-384, P-521), Ed25519 and Curve25519, J-PAKE, PBKDF2
  - True Random Number Generator (TRNG)
  - ARM® TrustZone®
  - Secure Boot (Root of Trust Secure Loader)
  - Secure Debug Unlock
  - DPA Countermeasures
  - Secure Key Management with PUF
  - Anti-Tamper
  - Secure Attestation
- **Wide Operating Range**
  - 1.71 to 3.8 V single power supply
  - -40 ° to +125 °C
- **Packages**
  - **QFN40** 5 × 5 × 0.85 mm
  - **QFN48** 6 × 6 × 0.85 mm

## 2. Ordering Information

**Table 2.1. Ordering Information**

| Ordering Code | Max TX Power | Flash (kB) | RAM (kB) | Secure Vault | GPIO | LCD | Package / Pinout | Temp Range |
|---|---|---|---|---|---|---|---|---|
| EFR32ZG23B021F512IM40-C | 20 dBm | 512 | 64 | High | 22 | No | QFN40 with HFCLKOUT | -40 to 125 °C |
| EFR32ZG23B020F512IM48-C | 20 dBm | 512 | 64 | High | 31 | Yes | QFN48 | -40 to 125 °C |
| EFR32ZG23B020F512IM40-C | 20 dBm | 512 | 64 | High | 23 | No | QFN40 | -40 to 125 °C |
| EFR32ZG23B011F512IM40-C | 14 dBm | 512 | 64 | High | 22 | No | QFN40 with HFCLKOUT | -40 to 125 °C |
| EFR32ZG23B010F512IM48-C | 14 dBm | 512 | 64 | High | 31 | Yes | QFN48 | -40 to 125 °C |
| EFR32ZG23B010F512IM40-C | 14 dBm | 512 | 64 | High | 23 | No | QFN40 | -40 to 125 °C |
| EFR32ZG23A020F512GM48-C | 20 dBm | 512 | 64 | Mid | 31 | Yes | QFN48 | -40 to 85 °C |
| EFR32ZG23A020F512GM40-C | 20 dBm | 512 | 64 | Mid | 23 | No | QFN40 | -40 to 85 °C |
| EFR32ZG23A010F512GM48-C | 14 dBm | 512 | 64 | Mid | 31 | Yes | QFN48 | -40 to 85 °C |
| EFR32ZG23A010F512GM40-C | 14 dBm | 512 | 64 | Mid | 23 | No | QFN40 | -40 to 85 °C |




| Field | Options |
|---|---|
| Product Family | • **EFR32ZG23**: Wireless Z-Wave 23 Family |
| Security | • **A**: Secure Vault Mid<br>• **B**: Secure Vault High |
| Features [f1][f2][f3] | • f1<br>  • **0**: Unused<br>• f2<br>  • **1**: 14 dBm PA Transmit Power<br>  • **2**: 20 dBm PA Transmit Power<br>• f3<br>  • **0**: Unused<br>  • **1**: High Quality HFCLKOUT Pin Available |
| Memory | • **F**: Flash |
| Size | • **Memory Size** in kBytes |
| Temperature Grade | • **G**: -40 to +85 °C<br>• **I**: -40 to +125 °C |
| Package | • **M**: QFN |
| Pins | • **Number of Package Pins** |
| Revision | • **C**: Revision C |
| Tape & Reel | • **R**: Tape & Reel (optional) |

**Figure 2.1. Ordering Code Key**

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# 3. System Overview

## 3.1 Introduction

The EFR32 product family combines an energy-friendly MCU with a high performance radio transceiver. The devices are well suited for secure connected IoT multi-protocol devices requiring high performance and low energy consumption. This section gives a short introduction to the full radio and MCU system. The detailed functional description can be found in the EFR32xG23 Reference Manual.

A block diagram of the EFR32ZG23 family is shown in Figure 3.1 Detailed EFR32ZG23 Block Diagram on page 9. The diagram shows a superset of features available on the family, which vary by part number. For more information about specific device features, consult 2. Ordering Information.

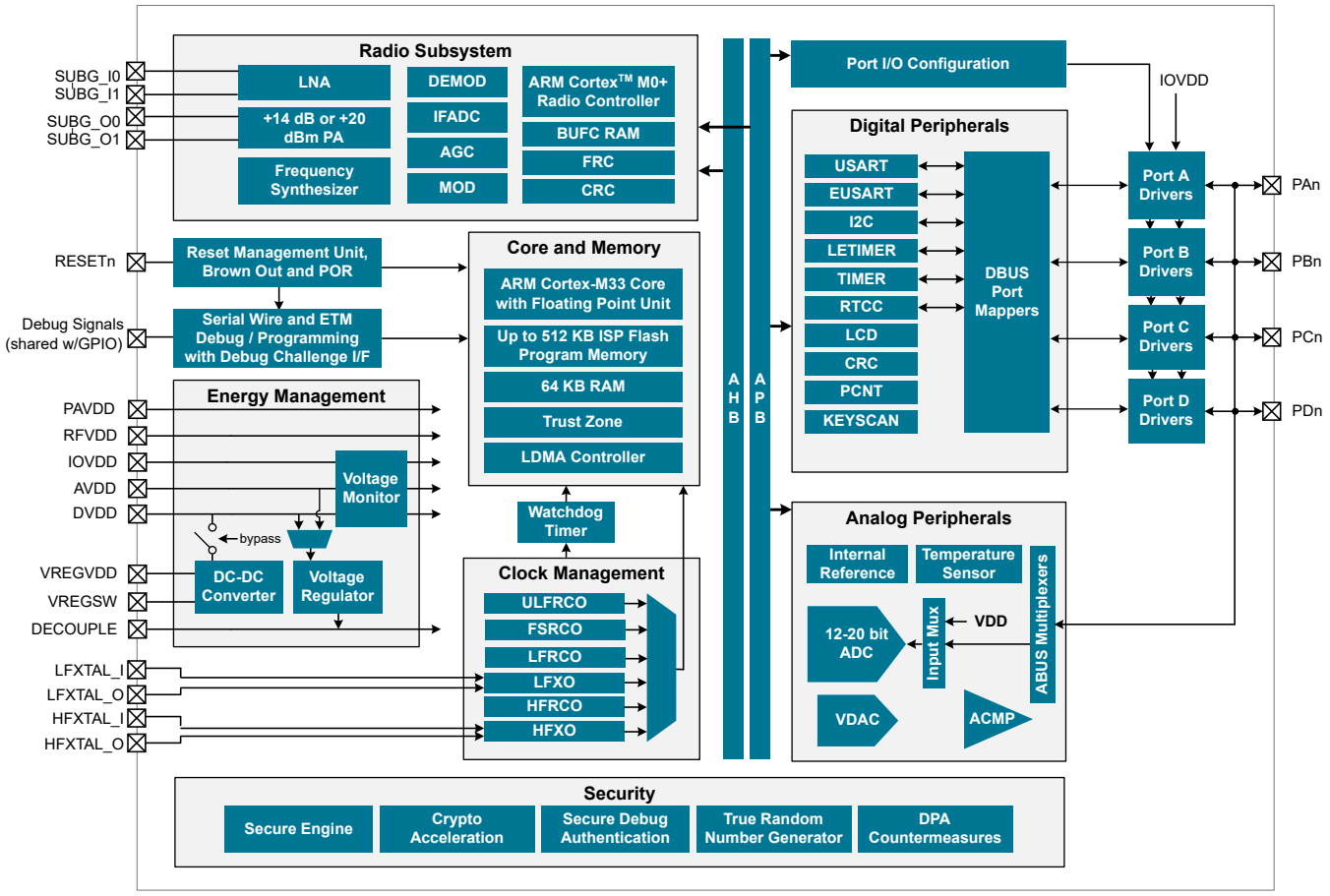


**Figure 3.1. Detailed EFR32ZG23 Block Diagram**

## 3.2 Radio

The EFR32ZG23 family features a radio transceiver supporting Z-Wave and proprietary wireless protocols.

### 3.2.1 Antenna Interface

The sub-GHz antenna interface consists of two single-ended input pins (SUBG_I0 and SUBG_I1) that interface directly to two LNAs and two single-ended output pins that interface directly to two +14 dBm or +20 dBm PA (SUBG_O0 and SUBG_O1). Integrated switches select either SUBG_O0 or SUBG_O1 to be the active path. The RF0 interface uses SUBG_I0 and SUBG_O0, while the RF1 interface uses SUBG_I1 and SUBG_O1.

The external components and power supply connections for the antenna interface typical applications are shown in the RF Matching Networks section.

### 3.2.2 Fractional-N Frequency Synthesizer

The EFR32ZG23 contains a high performance, low phase noise, fully integrated fractional-N frequency synthesizer. The synthesizer is used in receive mode to generate the LO frequency for the down-conversion mixer. It is also used in transmit mode to directly generate the modulated RF carrier.

The fractional-N architecture provides excellent phase noise performance, frequency resolution better than 24.8 Hz, and low energy consumption. The synthesizer's fast frequency settling allows for very short receiver and transmitter wake up times to reduce system energy consumption.

### 3.2.3 Receiver Architecture

The EFR32ZG23 uses a low-IF receiver architecture, consisting of a Low-Noise Amplifier (LNA) followed by an I/Q down-conversion mixer, employing a crystal reference. The I/Q signals are further filtered and amplified before being sampled by the IF analog-to-digital converter (IFADC).

The IF frequency is configurable from 150 kHz to 1371 kHz. The IF can further be configured for high-side or low-side injection, providing flexibility with respect to known interferers at the image frequency.

The Automatic Gain Control (AGC) module adjusts the receiver gain to optimize performance and avoid saturation for excellent selectivity and blocking performance. The sub-GHz radio can be calibrated on-demand by the user for the desired frequency band.

Demodulation is performed in the digital domain. The demodulator performs configurable decimation and channel filtering to allow receive bandwidths ranging from 0.1 to 2530 kHz. High carrier frequency and baud rate offsets are tolerated by active estimation and compensation. Advanced features supporting high quality communication under adverse conditions include forward error correction by block and convolutional coding as well as Direct Sequence Spread Spectrum (DSSS).

A Received Signal Strength Indicator (RSSI) is available for signal quality metrics, for level-based proximity detection, and for RF channel access by Collision Avoidance (CA) or Listen Before Talk (LBT) algorithms. An RSSI capture value is associated with each received frame and the dynamic RSSI measurement can be monitored throughout reception.

The EFR32ZG23 features integrated support for antenna diversity to improve link budget configuration in the sub-GHz band, using complementary control outputs to an external switch. Internal configurable hardware controls automatic switching between antennae during RF receive detection operations.

### 3.2.4 Transmitter Architecture

The EFR32ZG23 uses a direct-conversion transmitter architecture. For constant envelope modulation formats, the modulator controls phase and frequency modulation in the frequency synthesizer. Transmit symbols or chips are optionally shaped by a digital shaping filter. The shaping filter is fully configurable, including the BT product, and can be used to implement Gaussian or Raised Cosine shaping.

Carrier Sense Multiple Access - Collision Avoidance (CSMA-CA) or Listen Before Talk (LBT) algorithms can be automatically timed by the EFR32ZG23. These algorithms are typically defined by regulatory standards to improve interoperability in a given bandwidth between devices that otherwise lack synchronized RF channel access.

### 3.2.5 Packet and State Trace

The EFR32ZG23 Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data, and state information
- Data observability on a single-pin UART data output or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data, and state / meta information in a single serial data stream

### 3.2.6 Data Buffering

The EFR32ZG23 features an advanced Radio Buffer Controller (BUFC) capable of handling up to four buffers of adjustable size from 64 to 4096 bytes. Each buffer can be used for RX, TX, or for both. The buffer data is located in RAM, enabling zero-copy operations.

### 3.2.7 Radio Controller (RAC)

The Radio Controller controls the top level state of the radio subsystem in the EFR32ZG23. It performs the following tasks:

- Precisely-timed control of enabling and disabling of the receiver and transmitter circuitry
- Run-time calibration of receiver, transmitter, and frequency synthesizer
- Detailed frame transmission timing with optional LBT or CSMA-CA

### 3.2.8 Preamble Sense Mode

Preamble Sense Mode (PSM) is a radio receiver mode suitable for very low power applications. PSM takes advantage of fast preamble detection and, when combined with duty cycling of the receiver, can significantly reduce the average receive current in a system. PSM is only supported by 2(G)FSK modulation and the power saving is dependent on the protocol. PSM has higher benefit with long preambles and lower data rates. PSM can be used via the Signal Qualifier (SQ) feature.

## 3.3 General Purpose Input/Output (GPIO)

EFR32ZG23 has up to 31 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

All of the pins on ports A and port B are EM2 capable. These pins may be used by low-energy peripherals in EM2/3 and may also be used as EM2/3 pin wake-ups. Pins on ports C and D are latched/retained in their current state when entering EM2 until EM2 exit upon which internal peripherals could once again drive those pads.

A few GPIOs also have EM4 wake functionality. These pins are listed in 6.4 Alternate Function Table.

## 3.4 Keypad Scanner (KEYSCAN)

A low-energy keypad scanner (KEYSCAN) is included, which can scan up to a 6 x 8 matrix of keyboard switches. The KEYSCAN peripheral contains logic for debounce and settling time, allowing it to scan through the switch matrix autonomously in EM0 and EM1, and interrupt the processor when a key press is detected. A wake-on-keypress feature is also supported, allowing for the detection of any key press down to EM3.

## 3.5 Clocking

### 3.5.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFR32ZG23. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

### 3.5.2 Internal and External Oscillators

The EFR32ZG23 supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. The HFXO provides excellent RF clocking performance using a 39.0 MHz crystal. The HFXO can also support an external clock source such as a TCXO for applications that require an extremely accurate clock frequency over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast start-up at minimal energy consumption combined with a wide frequency range, from 1 MHz to 80 MHz.
- An integrated fast start-up RC oscillator (FSRCO) that runs at a fixed 20 MHz
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) for low power operation where high accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

## 3.6 Counters/Timers and PWM

### 3.6.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs, and trigger timed actions in other peripherals through the Peripheral Reflex System (PRS). The core of each TIMER is a 16-bit or 32-bit counter with up to 3 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers. In addition, some timers offer dead-time insertion.

See 3.14 Configuration Summary for information on the feature set of each timer.

### 3.6.2 Low Energy Timer (LETIMER)

The unique LETIMER is a 24-bit timer that is available in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Peripheral Reflex System (PRS), and can be configured to start counting on compare matches from other peripherals such as the Real Time Clock.

### 3.6.3 System Real Time Clock with Capture (SYSRTC)

The System Real Time Clock (SYSRTC) is a 32-bit counter providing timekeeping down to EM3. The SYSRTC can be clocked by any of the on-board low-frequency oscillators, and it is capable of providing system wake-up at user defined intervals.

### 3.6.4 Back-Up Real Time Counter (BURTC)

The Back-Up Real Time Counter (BURTC) is a 32-bit counter providing timekeeping in all energy modes, including EM4. The BURTC can be clocked by any of the on-board low-frequency oscillators, and it is capable of providing system wake-up at user-defined intervals.

### 3.6.5 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by the Peripheral Reflex System (PRS).

## 3.7 Communications and Other Digital Peripherals

### 3.7.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire, and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- $I^2S$

### 3.7.2 Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)

The Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter supports full duplex asynchronous UART communication with hardware flow control, RS-485, and IrDA support. The EUSART also supports high-speed SPI. In EM0 and EM1, the EUSART provides a high-speed, buffered communication interface.

When routed to GPIO ports A or B, the EUSART0 may also be used in a low-energy mode and operate in EM2. A 32.768 kHz clock source allows full duplex UART communication up to 9600 baud. EUSART0 can also act as a SPI secondary device in EM2 and EM3, and wake the system when data is received from an external bus controller.

### 3.7.3 Inter-Integrated Circuit Interface ($I^2C$)

The $I^2C$ module provides an interface between the MCU and a serial $I^2C$ bus. It is capable of acting as a main or secondary interface and supports multi-drop buses. Standard-mode, fast-mode, and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Bus arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the $I^2C$ module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of addresses is provided in active and low energy modes. Not all instances of $I^2C$ are available in all energy modes.

### 3.7.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality, such as simple logic operations (AND, OR, NOT), can be applied by the PRS to the signals. The PRS allows peripherals to act autonomously without waking the MCU core, saving power.

### 3.7.5 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface LESENSE™ is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators, ADC, and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable finite state machine which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

### 3.8 Secure Vault Features

A dedicated hardware secure engine containing its own CPU enables the Secure Vault functions. It isolates cryptographic functions and data from the host Cortex-M33 core, and provides several additional security features. The EFR32ZG23 family includes devices with Secure Vault High and Secure Vault Mid capabilities, which are summarized in the table below.

**Table 3.1. Secure Vault Features**

| Feature | Secure Vault Mid | Secure Vault High |
|---|---|---|
| True Random Number Generator (TRNG) | Yes | Yes |
| Secure Boot with Root of Trust and Secure Loader (RTSL) | Yes | Yes |
| Secure Debug with Lock/Unlock | Yes | Yes |
| DPA Countermeasures | Yes | Yes |
| Anti-Tamper | | Yes |
| Secure Attestation | | Yes |
| Secure Key Management | | Yes |
| Symmetric Encryption | • AES 128 / 192 / 256 bit<br>  • ECB, CTR, CBC, CFB, CCM, GCM, CBC-MAC, and GMAC | • AES 128 / 192 / 256 bit<br>  • ECB, CTR, CBC, CFB, CCM, GCM, CBC-MAC, and GMAC<br>• ChaCha20 |
| Public Key Encryption - ECDSA / ECDH / EdDSA | • p192 and p256<br>• Curve25519 (ECDH)[1]<br>• Ed25519 (EdDSA)[1] | • p192, p256, p384 and p521<br>• Curve25519 (ECDH)<br>• Ed25519 (EdDSA) |
| Key Derivation | • ECJ-PAKE p192 and p256 | • ECJ-PAKE p192, p256, p384, and p521<br>• PBKDF2<br>• HKDF |
| Hashes | • SHA-1<br>• SHA-2/256 | • SHA-1<br>• SHA-2 256, 384, and 512<br>• Poly1305 |

**Note:**
1. These curves are supported in devices running SE v2.1.7 and higher

#### 3.8.1 Secure Boot with Root of Trust and Secure Loader (RTSL)

The Secure Boot with RTSL authenticates a chain of trusted firmware that begins from an immutable memory (ROM).

It prevents malware injection, prevents rollback, ensures that only authentic firmware is executed, and protects Over The Air updates.

For more information about this feature, see AN1218: Series 2 Secure Boot with RTSL.

### 3.8.2 Cryptographic Accelerator

The Cryptographic Accelerator is an autonomous hardware accelerator with Differential Power Analysis (DPA) countermeasures to protect keys.

It supports AES encryption and decryption with 128/192/256-bit keys, ChaCha20 encryption, and Elliptic Curve Cryptography (ECC) to support public key operations and hashes.

Supported block cipher modes of operation for AES include:

- Electronic Code Book (ECB)
- Counter Mode (CTR)
- Cipher Block Chaining (CBC)
- Cipher Feedback (CFB)
- Galois Counter Mode (GCM)
- Counter with CBC-MAC (CCM)
- Cipher Block Chaining Message Authentication Code (CBC-MAC)
- Galois Message Authentication Code (GMAC)

The Cryptographic Accelerator accelerates Elliptical Curve Cryptography and supports the National Institute of Standards and Technology (NIST) recommended curves including P-192, P-256, P-384, and P-521 for Elliptic Curve Diffie-Hellman (ECDH) key derivation, and Elliptic Curve Digital Signature Algorithm (ECDSA) sign and verify operations. Also supported is the non-NIST Curve25519 for ECDH and Ed25519 for Edwards-curve Digital Signature Algorithm (EdDSA) sign and verify operations.

Secure Vault also supports Elliptic Curve variant of Password Authenticated Key Exchange by Juggling (ECJ-PAKE) and Password-Based Key Derivation Function 2 (PBKDF2).

Supported hashes include SHA-1, SHA-2/256/384/512 and Poly1305.

This implementation provides a fast and energy efficient solution to state of the art cryptographic needs.

### 3.8.3 True Random Number Generator

The TRNG module is a non-deterministic random number generator that harvests entropy from a thermal energy source. It includes start-up health tests for the entropy source as required by NIST SP800-90B and AIS-31, as well as online health tests required for NIST SP800-90C.

The TRNG is suitable for periodically generating entropy to seed an approved pseudo random number generator.

### 3.8.4 Secure Debug with Lock/Unlock

For obvious security reasons, it is critical for a product to have its debug interface locked before being released in the field.

Secure Vault also provides a secure debug unlock function that allows authenticated access based on public key cryptography. This functionality is particularly useful for supporting failure analysis while maintaining confidentiality of IP and sensitive end-user data.

For more information about this feature, see AN1190: Series 2 Secure Debug.

### 3.8.5 DPA Countermeasures

The AES and ECC accelerators have Differential Power Analysis (DPA) countermeasures support. This makes it very expensive from a time and effort standpoint to use DPA to recover secret keys.

### 3.8.6 Secure Key Management with PUF

Key material in Secure Vault High products is protected by "key wrapping" with a standardized symmetric encryption mechanism. This method has the advantage of protecting a virtually unlimited number of keys, limited only by the storage that is accessible by the Cortex-M33, which includes off-chip storage as well. The symmetric key used for this wrapping and unwrapping must be highly secure because it can expose all other key materials in the system. The Secure Vault Key Management system uses a Physically Unclonable Function (PUF) to generate a persistent device-unique seed key on power up to dynamically generate this critical wrapping/unwrapping key which is only visible to the AES encryption engine and is not retained when the device loses power.

### 3.8.7 Anti-Tamper

Secure Vault High devices provide internal tamper protection which monitors parameters such as voltage, temperature, and electromagnetic pulses as well as detecting tamper of the security sub-system itself. Additionally, 8 external configurable tamper pins support external tamper sources, such as enclosure tamper switches.

For each tamper event, the user is able to select the severity of the tamper response ranging from an interrupt, to a reset, to destroying the PUF reconstruction data which will make all protected key materials un-recoverable and effectively render the device inoperable. The tamper system also has an internal resettable event counter with programmable trigger threshold and refresh periods to mitigate false positive tamper events.

For more information about this feature, see AN1247: Anti-Tamper Protection Configuration and Use.

### 3.8.8 Secure Attestation

Secure Vault High products support Secure Attestation, which begins with a secure identity that is created during the Silicon Labs manufacturing process. During device production, each device generates its own public/private keypair and securely stores the wrapped private key into immutable OTP memory and this key never leaves the device. The corresponding public key is extracted from the device and inserted into a binary DER-encoded X.509 device certificate, which is signed into a Silicon Labs CA chain and then programmed back into the chip into an immutable OTP memory.

The secure identity can be used to authenticate the chip at any time in the life of the product. The production certification chain can be requested remotely from the product. This certification chain can be used to verify that the device was authentically produced by Silicon Labs. The device unique public key is also bound to the device certificate in the certification chain. A challenge can be sent to the chip at any point in time to be signed by the device private key. The public key in the device certificate can then be used to verify the challenge response, proving that the device has access to the securely-stored private key, which prevents counterfeit products or impersonation attacks.

For more information about this feature, see AN1268: Authenticating Silicon Labs Devices Using Device Certificates.

## 3.9 Analog

### 3.9.1 Analog to Digital Converter (IADC)

The IADC is a hybrid architecture combining techniques from both SAR and Delta-Sigma style converters. It has a resolution of 12 bits at 1 Msps and 16 bits at up to 76.9 ksps. Hardware oversampling reduces system-level noise over multiple front-end samples. The IADC includes integrated voltage reference options. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

### 3.9.2 Analog Comparator (ACMP)

The ACMP is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

### 3.9.3 Digital to Analog Converter (VDAC)

The VDAC can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksps, 12-bit converter. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

### 3.9.4 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD with up to 4x20 segments. A voltage boost function enables it to provide the LCD with higher voltage than the supply voltage for the device. A patented charge redistribution driver can reduce the LCD peripheral supply current by up to 40%. In addition, an animation feature can run custom animations on the LCD without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

## 3.10 Power

The EFR32ZG23 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An integrated DC-DC buck regulator can optionally be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFR32ZG23 device family includes support for internal supply voltage scaling, as well as two different power domains groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

### 3.10.1 Energy Management Unit (EMU)

The EMU manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to implement system-wide voltage scaling and turn off the power to unused RAM blocks to optimize the energy consumption in the target application. The DC-DC regulator operation is tightly integrated with the EMU.

### 3.10.2 Voltage Scaling

The EFR32ZG23 supports supply voltage scaling for the LDO powering DECOUPLE, with independent selections for EM0 / EM1 and EM2 / EM3. Voltage scaling helps to optimize the energy efficiency of the system by operating at lower voltages when possible. The EM0 / EM1 voltage scaling level defaults to VSCALE2, which allows the core to operate in active mode at full speed. The intermediate level, VSCALE1, allows operation in EM0 and EM1 at up to 40 MHz. The lowest level, VSCALE0, can be used to conserve power further in EM2 and EM3. The EMU will automatically switch the target voltage scaling level when transitioning between energy modes.

### 3.10.3 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents, providing high efficiency in energy modes EM0, EM1, EM2, and EM3. RF noise mitigation allows operation of the DC-DC converter without significantly degrading sensitivity of radio components. An on-chip supply-monitor signals when the supply voltage is low to allow bypass of the regulator via programmable software interrupt. It employs soft switching at boot and DCDC regulating-to-bypass transitions to limit the max supply slew-rate and mitigate inrush current.

### 3.10.4 Power Domains

Peripherals may exist on several independent power domains which are powered down to minimize supply current when not in use. Power domains are managed automatically by the EMU.

The lowest-energy power domain is the "high-voltage" power domain (PDHV), which supports extremely low-energy infrastructure and peripherals. Circuits powered from PDHV are always on and available in all energy modes down to EM4.

The next power domain is the low power domain (PD0), which is further divided to power subsets of peripherals. All PD0 power domains are shut down in EM4. Circuits powered from PD0 power domains may be available in EM0, EM1, EM2, and EM3.

Low power domain A (PD0A) is the base power domain for EM2 and EM3 and will always remain on in EM0-EM3. It powers the most commonly-used EM2 and EM3-capable peripherals and infrastructure required to operate in EM2 and EM3. Auxiliary PD0 power domains (PD0B, PD0C, PD0D, PD0E) power additional EM2- and EM3-capable peripherals on demand. If any peripherals on one of the auxiliary power domains is enabled, that power domain will be active in EM2 and EM3. Otherwise, the auxiliary PD0 power domains will be shut down to reduce current.

**Note:** Power domain PD0E is also turned on when peripherals on PD0B, PD0C, or PD0D are used.

The active power domain (PD1) powers the rest of the device circuitry, including the CPU core and EM0 / EM1 peripherals. PD1 is always powered on in EM0 and EM1. PD1 is always shut down in EM2, EM3, and EM4.

Table 3.2 Peripheral Power Subdomains on page 18 shows the peripherals on the PDHV and PD0x domains. Any peripheral not listed is on PD1.

**Table 3.2. Peripheral Power Subdomains**

| Always On in EM2/EM3 | | Selectively On in EM2/3 | | | |
|---|---|---|---|---|---|
| PDHV[1] | PD0A | PD0B[2] | PD0C[2] | PD0D[2] | PD0E |
| LFRCO | SYSRTC | LETIMER0 | HFRCOEM23 | DEBUG | GPIO |
| LFXO | FSRCO | IADC0 | HFXO | WDOG0 | KEYSCAN |
| BURTC | LCD | PCNT0 | | WDOG1 | PRS |
| ULFRCO | | ACMP0 | | EUSART0 | |
| | | ACMP1 | | I2C0 | |
| | | LESENSE | | | |
| | | VDAC0 | | | |

**Note:**
1. Peripherals on PDHV are also available in EM4.
2. If any of PD0B, PD0C, or PD0D are enabled, PD0E will also be automatically enabled.

### 3.11 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFR32ZG23. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

## 3.12 Core and Memory

### 3.12.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M33 RISC processor achieving 1.50 Dhrystone MIPS/MHz
- ARM TrustZone security technology
- Embedded Trace Macrocell (ETM) for real-time trace and debug
- Up to 512 KB flash program memory
- Up to 64 KB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

### 3.12.2 Memory System Controller (MSC)

The MSC is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M33 and LDMA. In addition to the main flash array where program code is normally written, the MSC also provides an information block where additional information, such as special user information or flash-lock bits, is stored. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

### 3.12.3 Linked Direct Memory Access Controller (LDMA)

The LDMA controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

### 3.13 Memory Map

The EFR32ZG23 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

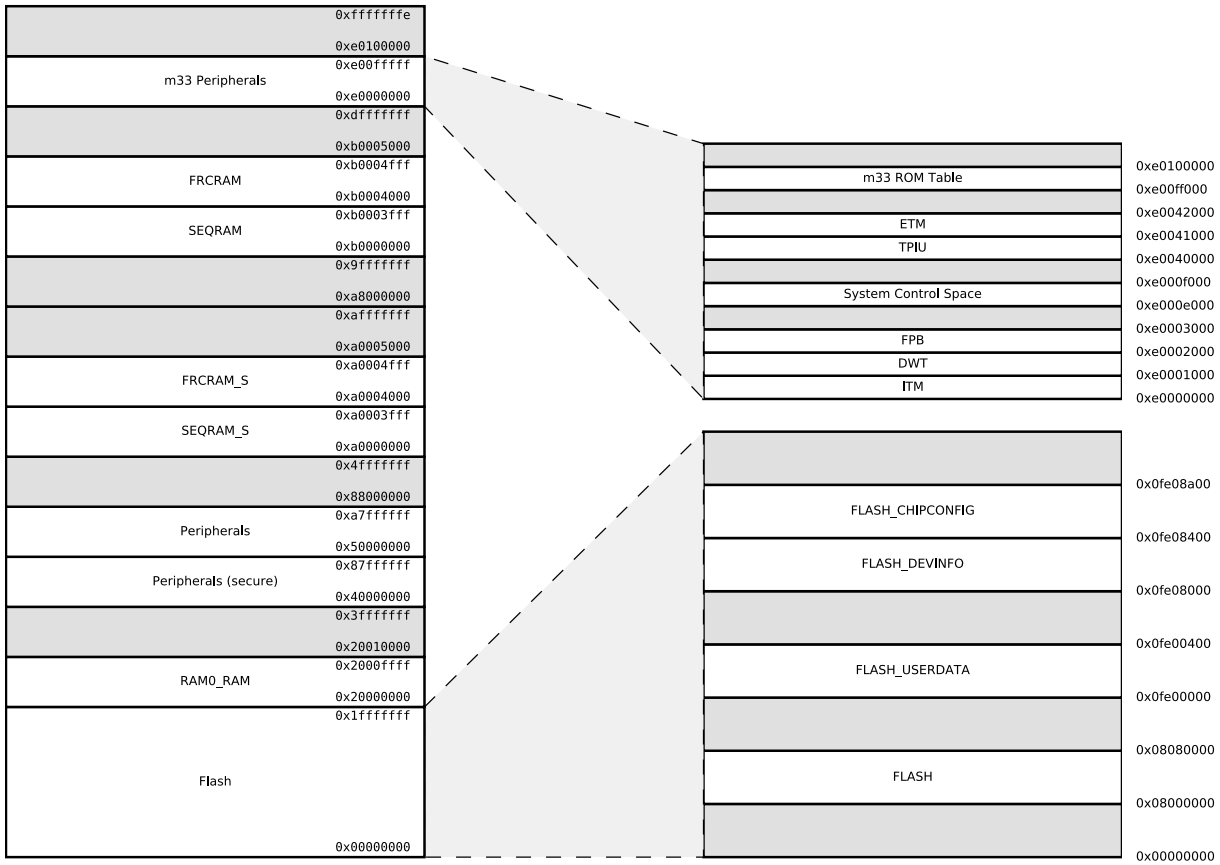


**Figure 3.2. EFR32ZG23 Memory Map — Core Peripherals and Code Space**

### 3.14 Configuration Summary

The features of the EFR32ZG23 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

**Table 3.3. Configuration Summary**

| Module | Lowest Energy Mode | Configuration |
|---|---|---|
| I2C0 | EM2/EM3[1] | |
| I2C1 | EM1 | |
| IADC0 | EM2/EM3 | |
| LETIMER0 | EM2/EM3[1] | |
| TIMER0 | EM1 | 32-bit, 3-channels, +DTI |
| TIMER1 | EM1 | 16-bit, 3-channels, +DTI |
| TIMER2 | EM1 | 16-bit, 3-channels, +DTI |
| TIMER3 | EM1 | 16-bit, 3-channels, +DTI |
| TIMER4 | EM1 | 16-bit, 3-channels, +DTI |
| EUSART0 | EM1 - Full high-speed operation, all modes<br>EM2[1] - Low-energy UART operation, 9600 Baud<br>EM2 or EM3[1] - Low-energy SPI secondary receiver | |
| EUSART1 | EM1 - Full high-speed operation | |
| EUSART2 | EM1 - Full high-speed operation | |
| USART0 | EM1 | +IrDA, +I2S, +SmartCard |

**Note:**

1. EM2 and EM3 operation is only supported for digital peripheral I/O on Port A and Port B. All GPIO ports support digital peripheral operation in EM0 and EM1.

# 4. Electrical Specifications

## 4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on $T_A$=25 °C and all supplies at 3.3 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Due to on-chip circuitry (e.g., diodes), some EFR32ZG23 power supply pins have a dependent relationship with one or more other power supply pins. These internal relationships between the external voltages applied to the various EFR32ZG23 supply pins are defined below. Exceeding the below constraints can result in damage to the device and/or increased current draw.

- VREGVDD and DVDD
  - In systems using the DCDC converter, DVDD (the buck converter output) should not be driven externally and VREGVDD (the buck converter input) must be greater than DVDD (VREGVDD ≥ DVDD)
  - In systems not using the DCDC converter, DVDD must be shorted to VREGVDD on the PCB (VREGVDD = DVDD)
- AVDD, IOVDD: No dependency with each other or any other supply pin. Additional leakage may occur if DVDD remains unpowered with power applied to these supplies.
- DVDD ≥ DECOUPLE
- PAVDD ≥ RFVDD

### 4.2 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 4.1. Absolute Maximum Ratings**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Storage temperature range | $T_{STG}$ | | -50 | — | +150 | °C |
| Voltage on any supply pin | $V_{DDMAX}$ | | -0.3 | — | 3.8 | V |
| Junction temperature | $T_{JMAX}$ | -G grade | — | — | +105 | °C |
| | | -I grade | — | — | +125 | °C |
| Voltage ramp rate on any supply pin | $V_{DDRAMPMAX}$ | | — | — | 1.0 | V / µs |
| Voltage on HFXO pins | $V_{HFXOPIN}$ | | -0.3 | — | 1.2 | V |
| DC voltage on any GPIO pin[1] | $V_{DIGPIN}$ | | -0.3 | — | $V_{IOVDD}$ + 0.3 | V |
| DC voltage on RESETn pin[2] | $V_{RESETn}$ | | -0.3 | — | 3.8 | V |
| Absolute voltage on Sub-GHz RF pins | $V_{MAXSUBG}$ | SUBG_O pins | -0.3 | — | 1.2 | V |
| | | SUBG_I pins | -0.3 | — | 0.3 | V |
| Total current into VDD power lines | $I_{VDDMAX}$ | Source | — | — | 200 | mA |
| Total current into VSS ground lines | $I_{VSSMAX}$ | Sink | — | — | 200 | mA |
| Current per I/O pin | $I_{IOMAX}$ | Sink | — | — | 50 | mA |
| | | Source | — | — | 50 | mA |
| Current for all I/O pins | $I_{IOALLMAX}$ | Sink | — | — | 200 | mA |
| | | Source | — | — | 200 | mA |

**Note:**

1. When operating as an LCD driver, the output voltage on a GPIO may safely exceed this specification. The pin output voltage may be up to 3.8 V in this case.
2. The RESETn pin has a pull-up device to the DVDD supply. For minimum leakage, RESETn should not exceed the voltage at DVDD.

### 4.3 General Operating Conditions

**Table 4.2. General Operating Conditions**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating ambient temperature range | $T_A$ | -G temperature grade [1] | -40 | — | +85 | °C |
| | | -I temperature grade [1] | -40 | — | +125 | ° C |
| DVDD supply voltage | $V_{DVDD}$ | EM0/1 | 1.71 | 3.3 | 3.8 | V |
| | | EM2/3/4[2] | 1.71 | 3.3 | 3.8 | V |
| AVDD supply voltage | $V_{AVDD}$ | | 1.71 | 3.3 | 3.8 | V |
| IOVDD operating supply voltage | $V_{IOVDD}$ | | 1.71 | 3.3 | 3.8 | V |
| PAVDD operating supply voltage | $V_{PAVDD}$ | | 1.71 | 3.3 | 3.8 | V |
| VREGVDD operating supply voltage | $V_{VREGVDD}$ | DCDC in regulation | 2.2 | 3.3 | 3.8 | V |
| | | DCDC in bypass 60 mA load | 1.8 | 3.3 | 3.8 | V |
| | | DCDC in bypass 120 mA load | 1.9 | 3.3 | 3.8 | V |
| | | DCDC not in use. DVDD externally shorted to VREGVDD | 1.71 | 3.3 | 3.8 | V |
| RFVDD operating supply voltage | $V_{RFVDD}$ | | 1.71 | 3.3 | $V_{PAVDD}$ | V |
| DECOUPLE output capacitor[3] | $C_{DECOUPLE}$ | 1.0 µF ± 10% X8L capacitor used for performance characterization. | 0.75 | 1.0 | 2.75 | µF |
| HCLK and SYSCLK frequency | $f_{HCLK}$ | VSCALE2, MODE = WS1 | — | — | 78 | MHz |
| | | VSCALE2, MODE = WS0 | — | — | 40 | MHz |
| | | VSCALE1, MODE = WS1 | — | — | 40 | MHz |
| | | VSCALE1, MODE = WS0 | — | — | 20 | MHz |
| PCLK frequency | $f_{PCLK}$ | VSCALE2 or VSCALE1 | — | — | 40 | MHz |
| EM01 Group A clock frequency | $f_{EM01GRPACLK}$ | VSCALE2 | — | — | 80 | MHz |
| | | VSCALE1 | — | — | 40 | MHz |
| EM01 Group C clock frequency | $f_{EM01GRPCCLK}$ | VSCALE2 | — | — | 80 | MHz |
| | | VSCALE1 | — | — | 40 | MHz |
| HCLK Radio frequency[4] | $f_{RHCLK}$ | VSCALE2 or VSCALE1 | — | 39.0 | 40 | MHz |
| External Clock Input | $f_{CLKIN}$ | VSCALE2 or VSCALE1, IOVDD ≥ 2.7 V | — | — | 40 | MHz |
| DPLL Reference Clock | $f_{DPLLREFCLK}$ | VSCALE2 or VSCALE1 | — | — | 40 | MHz |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|

**Note:**

1. The device may operate continuously at the maximum allowable ambient $T_A$ rating as long as the absolute maximum $T_{JMAX}$ is not exceeded. For an application with significant power dissipation, the allowable $T_A$ may be lower than the maximum $T_A$ rating. $T_A$ = $T_{JMAX}$ - ($THETA_{JA}$ x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for $T_{JMAX}$ and $THETA_{JA}$.
2. The DVDD supply is monitored by the DVDD BOD in EM0/1 and the LE DVDD BOD in EM2/3/4.
3. The system designer should consult the characteristic specs of the capacitor used on DECOUPLE to ensure its capacitance value stays within the specified bounds across temperature and DC bias.
4. The recommended radio crystal frequency for the sub-GHz radio is 39.0 MHz. The minimum and maximum RHCLK frequency in this table represent the design timing limits, which are much wider than the typical crystal tolerance.

### 4.4 DC-DC Converter

Test conditions: $L_{DCDC}$ = 2.2 µH (Samsung CIG22H2R2MNE), $C_{DCDC}$ = 4.7 µF (TDK CGA5L3X8R1C475K160AB), $V_{VREGVDD}$ = 3.3 V, $V_{OUT}$ = 1.8 V, IPKVAL in EM0/1 modes is set to 150 mA, and in EM2/3 modes is set to 90 mA, unless otherwise indicated.

**Table 4.3. DC-DC Converter**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input voltage range at VREGVDD pin | $V_{VREGVDD}$ | DCDC in regulation, $I_{LOAD}$ = $I_{LOAD}$ MAX[1], EM0/EM1 mode | 2.2 | — | 3.8 | V |
| | | DCDC in regulation, $I_{LOAD}$ = 5 mA, EM0/EM1 or EM2/EM3 mode | 1.8 | — | 3.8 | V |
| | | Bypass Mode, $I_{LOAD}$ ≤ 60 mA | 1.8 | — | 3.8 | V |
| | | Bypass Mode, $I_{LOAD}$ ≤ 120 mA | 1.9 | — | 3.8 | V |
| Regulated output voltage | $V_{OUT}$ | | — | 1.8 | — | V |
| Regulation DC accuracy | $ACC_{DC}$ | $V_{VREGVDD}$ ≥ 2.2 V, Steady state in EM0/EM1 mode or EM2/EM3 mode | -2.5 | — | 4.0 | % |
| Regulation total accuracy | $ACC_{TOT}$ | All error sources (including DC errors, overshoot, undershoot) | -5 | — | 7 | % |
| Steady-state output ripple | $V_R$ | $I_{LOAD}$ = 20 mA in EM0/EM1 mode | — | 12 | — | mVpp |
| DC line regulation | $V_{REG}$ | $I_{LOAD}$ = $I_{LOAD}$ MAX[2]in EM0/EM1 mode, $V_{VREGVDD}$ ≥ 2.2 V | — | -2.6 | — | mV/V |
| Efficiency | EFF | Load current between 100 µA and 60 mA in EM0/EM1 mode | — | 90 | — | % |
| | | Load current between 10 µA and 5 mA in EM2/EM3 mode | — | 89 | — | % |
| DC load regulation | $I_{REG}$ | Load current between 100 µA and $I_{LOAD}$ MAX[2] in EM0/EM1 mode | — | -0.08 | — | mV/mA |
| Output load current | $I_{LOAD}$ | EM0/EM1 mode, DCDC in regulation, DCDC_EM01CTRL0.IPKVAL = 9, Pulse-pairing disabled, Radio not transmitting[2] | — | — | 60 | mA |
| | | EM0/EM1 mode, DCDC in regulation, Radio in receive mode, with pulse-pairing enabled [2] | — | — | 36 | mA |
| | | EM0/EM1 mode, DCDC in regulation, Radio transmitting[1] | — | — | 120 | mA |
| | | EM2/EM3 mode, DCDC in regulation | — | — | 5 | mA |
| | | Bypass mode, 1.8 V ≤ $V_{VREGVDD}$ ≤ 3.8 V | — | — | 60 | mA |
| | | Bypass mode, 1.9 V ≤ $V_{VREGVDD}$ ≤ 3.8 V | — | — | 120 | mA |
| Nominal output capacitor | $C_{DCDC}$ | 4.7 µF ± 10% X7R capacitor used for performance characterization[3] | — | 4.7 | 10 | µF |
| Nominal inductor | $L_{DCDC}$ | ± 20% tolerance | — | 2.2 | — | µH |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Nominal input capacitor | $C_{IN}$ | | $C_{DCDC}$ | — | — | µF |
| Resistance in bypass mode | $R_{BYP}$ | Bypass switch from VREGVDD to DVDD, $V_{VREGVDD}$ = 1.8 V | — | 0.45 | 0.8 | Ω |
| | | Powertrain PFET switch from VREGVDD to VREGSW, $V_{VREGVDD}$ = 1.8 V | — | 0.6 | 0.9 | Ω |
| Supply monitor threshold programming range | $V_{CMP_RNG}$ | Programmable in 0.1 V steps | 2 | — | 2.3 | V |
| Supply monitor threshold accuracy | $V_{CMP_ACC}$ | Supply falling edge trip point | -5 | — | 5 | % |
| Supply monitor threshold hysteresis | $V_{CMP_HYST}$ | Positive hysteresis on the supply rising edge referred to the falling edge trip point | — | 4 | — | % |
| Supply monitor response time | $t_{CMP_DELAY}$ | Supply falling edge at -100 mV / µs | — | 0.6 | — | µs |

**Note:**

1. During radio transmit operations, the RAIL library will place the DCDC into a mode that increases the maximum load current, to support higher TX output power supplied from the DCDC converter.
2. Pulse-pairing is an optional feature to improve performance at radio frequencies below 550 MHz, but has limited output current. It is enabled by default when using RAIL with an IPKVAL setting of 3 or less. Pulse pairing may be disabled from application code by setting IPKVAL > 3. This must be done before RAIL software is initialized.
3. TDK CGA5L3X8R1C475K160AB used for performance characterization. Actual capacitor values can be significantly de-rated from their specified nominal value by the rated tolerance, as well as the application's AC voltage, DC bias, and temperature. The minimum capacitance counting all error sources should be no less than 3.6 µF.

### 4.5 Thermal Characteristics

**Table 4.4. Thermal Characteristics**

| Package | Board | Parameter | Symbol | Test Condition | Value | Unit |
|---|---|---|---|---|---|---|
| 40QFN (5x5mm) | JEDEC - High Thermal Cond. (2s2p)[1] | Thermal Resistance, Junction to Ambient | $\Theta_{JA}$ | Still Air | 29.2 | °C/W |
| | | Thermal Resistance, Junction to Board | $\Theta_{JB}$ | | 15.2 | °C/W |
| | | Thermal Resistance, Junction to Top Center | $\Psi_{JT}$ | | 0.3 | °C/W |
| | | Thermal Resistance, Junction to Board | $\Psi_{JB}$ | | 11.2 | °C/W |
| | No Board | Thermal Resistance, Junction to Case | $\Theta_{JC}$ | Temperature controlled heat sink on top of package, all other sides of package insulated to prevent heat flow. | 24.6 | °C/W |
| 48QFN (6x6mm) | JEDEC - High Thermal Cond. (2s2p)[1] | Thermal Resistance, Junction to Ambient | $\Theta_{JA}$ | Still Air | 27.7 | °C/W |
| | | Thermal Resistance, Junction to Board | $\Theta_{JB}$ | | 14.6 | °C/W |
| | | Thermal Resistance, Junction to Top Center | $\Psi_{JT}$ | | 0.69 | °C/W |
| | | Thermal Resistance, Junction to Board | $\Psi_{JB}$ | | 11.85 | °C/W |
| | No Board | Thermal Resistance, Junction to Case | $\Theta_{JC}$ | Temperature controlled heat sink on top of package, all other sides of package insulated to prevent heat flow. | 23.0 | °C/W |

**Note:**

1. Based on 4 layer PCB with dimension 3" x 4.5", PCB Thickness of 1.6 mm, per JEDEC. PCB Center Land with 9 Via to top internal plane of PCB.

## 4.6 Current Consumption

### 4.6.1 MCU Current Consumption using DC-DC at 3.3 V Input

Unless otherwise indicated, typical conditions are: VREGVDD = 3.3 V. AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V from DC-DC. Voltage scaling level = VSCALE1. $T_A$ = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at $T_A$ = 25 °C.

**Table 4.5. MCU Current Consumption using DC-DC at 3.3 V Input**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in EM0 mode with all peripherals disabled | $I_{ACTIVE}$ | 78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running Prime from flash, VSCALE2 | — | 28 | — | µA/MHz |
| | | 78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running while loop from flash, VSCALE2 | — | 26 | — | µA/MHz |
| | | 78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running CoreMark loop from flash, VSCALE2 | — | 36 | — | µA/MHz |
| | | 39 MHz crystal, CPU running Prime from flash | — | 27 | — | µA/MHz |
| | | 39 MHz crystal, CPU running while loop from flash | — | 26 | — | µA/MHz |
| | | 39 MHz crystal, CPU running CoreMark loop from flash | — | 36 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running while loop from flash | — | 22 | — | µA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 24 | — | µA/MHz |
| | | 16 MHz HFRCO, CPU running while loop from flash | — | 29 | — | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 206 | — | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled | $I_{EM1}$ | 78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, VSCALE2 | — | 17 | — | µA/MHz |
| | | 39 MHz crystal | — | 18 | — | µA/MHz |
| | | 38 MHz HFRCO | — | 14 | — | µA/MHz |
| | | 26 MHz HFRCO | — | 16 | — | µA/MHz |
| | | 16 MHz HFRCO | — | 21 | — | µA/MHz |
| | | 1 MHz HFRCO | — | 197 | — | µA/MHz |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in EM2 mode, VSCALE0 | $I_{EM2_VS}$ | 64 kB RAM and full Radio RAM retention, RTC running from LFXO | — | 1.5 | — | µA |
| | | 64 kB RAM and full Radio RAM retention, RTC running from LFRCO | — | 1.5 | — | µA |
| | | 16 kB RAM and full Radio RAM retention, RTC running from LFRCO | — | 1.2 | — | µA |
| | | 16 kB RAM and full Radio RAM retention, RTC running from LFXO | — | 1.2 | — | µA |
| Current consumption in EM3 mode, VSCALE0 | $I_{EM3_VS}$ | 64 kB RAM and full Radio RAM retention, RTC running from ULFRCO | — | 1.3 | — | µA |
| | | 16 kB RAM and full Radio RAM retention, RTC running from ULFRCO | — | 1.0 | — | µA |
| Current consumption for retained RAM bank in EM2 or EM3 | $I_{RAM}$ | Per 16 kB RAM bank | — | 0.1 | — | µA |
| Additional current in EM2 or EM3 when any peripheral in PD0B is enabled[1] | $I_{PD0B_VS}$ | | — | 0.85 | — | µA |
| Additional current in EM2 or EM3 when any peripheral in PD0C is enabled[1] | $I_{PD0C_VS}$ | | — | 0.13 | — | µA |
| Additional current in EM2 or EM3 when any peripheral in PD0D is enabled[1] | $I_{PD0D_VS}$ | | — | 0.98 | — | µA |
| Additional current in EM2 or EM3 when any peripheral in PD0E is enabled[1] | $I_{PD0E_VS}$ | | — | 0.06 | — | µA |

**Note:**

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.10.4 Power Domains for a list of the peripherals in each power domain. Note that if the PD0B, PD0C, or PD0D domains are enabled, PD0E will also automatically be enabled.

### 4.6.2 MCU Current Consumption at 3.3 V

Unless otherwise indicated, typical conditions are: AVDD = DVDD = RFVDD = PAVDD = VREGVDD = 3.3 V. DC-DC not used. Voltage scaling level = VSCALE1. $T_A$ = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at $T_A$ = 25 °C.

**Table 4.6. MCU Current Consumption at 3.3 V**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in EM0 mode with all peripherals disabled | $I_{ACTIVE}$ | 78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running Prime from flash, VSCALE2 | — | 45 | — | µA/MHz |
| | | 78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running while loop from flash, VSCALE2 | — | 41 | — | µA/MHz |
| | | 78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running CoreMark loop from flash, VSCALE2 | — | 57 | — | µA/MHz |
| | | 39 MHz crystal, CPU running Prime from flash | — | 44 | — | µA/MHz |
| | | 39 MHz crystal, CPU running while loop from flash | — | 42 | — | µA/MHz |
| | | 39 MHz crystal, CPU running CoreMark loop from flash | — | 58 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running while loop from flash | — | 35 | 56 | µA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 38 | — | µA/MHz |
| | | 16 MHz HFRCO, CPU running while loop from flash | — | 46 | — | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 329 | 1100 | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled | $I_{EM1}$ | 78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, VSCALE2 | — | 27 | — | µA/MHz |
| | | 39 MHz crystal | — | 29 | — | µA/MHz |
| | | 38 MHz HFRCO | — | 22 | 42 | µA/MHz |
| | | 26 MHz HFRCO | — | 25 | — | µA/MHz |
| | | 16 MHz HFRCO | — | 33 | — | µA/MHz |
| | | 1 MHz HFRCO | — | 315 | 1086 | µA/MHz |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in EM2 mode, VSCALE0 | $I_{EM2_VS}$ | 64 kB RAM and full Radio RAM retention, RTC running from LFXO | — | 2.4 | — | µA |
| | | 64 kB RAM and full Radio RAM retention, RTC running from LFRCO | — | 2.4 | 4.1 | µA |
| | | 16 kB RAM and full Radio RAM retention, RTC running from LFRCO | — | 1.92 | — | µA |
| | | 16 kB RAM and full Radio RAM retention, RTC running from LFXO | — | 1.93 | — | µA |
| | | 16 kB RAM retention and RTC running from LFXO, Sequencer RAM and CPU cache not retained | — | 1.71 | — | µA |
| | | 16 kB RAM retention and RTC running from LFXO, Sequencer RAM, CPU cache, and EM0/1 peripheral states not retained | — | 1.69 | — | µA |
| | | 16 kB RAM retention and RTC running from LFXO, Sequencer RAM, FRC RAM, CPU cache, and EM0/1 peripheral states not retained | — | 1.62 | — | µA |
| Current consumption in EM3 mode, VSCALE0 | $I_{EM3_VS}$ | 64 kB RAM and full Radio RAM retention, RTC running from ULFRCO | — | 2.0 | — | µA |
| | | 16 kB RAM and full Radio RAM retention, RTC running from ULFRCO | — | 1.59 | 2.5 | µA |
| Current consumption for retained RAM bank in EM2 or EM3 | $I_{RAM}$ | Per 16 kB RAM bank | — | 0.14 | — | µA |
| Current consumption in EM4 mode | $I_{EM4}$ | No BURTC, no LF oscillator | — | 0.32 | 0.65 | µA |
| | | BURTC with LFXO | — | 0.70 | — | µA |
| Current consumption during reset | $I_{RST}$ | Hard pin reset held | — | 462 | — | µA |
| Additional current in EM2 or EM3 when any peripheral in PD0B is enabled[1] | $I_{PD0B_VS}$ | | — | 1.37 | — | µA |
| Additional current in EM2 or EM3 when any peripheral in PD0C is enabled[1] | $I_{PD0C_VS}$ | | — | 0.20 | — | µA |
| Additional current in EM2 or EM3 when any peripheral in PD0D is enabled[1] | $I_{PD0D_VS}$ | | — | 1.57 | — | µA |
| Additional current in EM2 or EM3 when any peripheral in PD0E is enabled[1] | $I_{PD0E_VS}$ | | — | 0.09 | — | µA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|

**Note:**

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.10.4 Power Domains for a list of the peripherals in each power domain. Note that if the PD0B, PD0C, or PD0D domains are enabled, PD0E will also automatically be enabled.

### 4.6.3 MCU Current Consumption at 1.8 V

Unless otherwise indicated, typical conditions are: AVDD = DVDD = RFVDD = PAVDD = VREGVDD = 1.8 V. DC-DC not used. Voltage scaling level = VSCALE1. $T_A$ = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at $T_A$ = 25 °C.

**Table 4.7. MCU Current Consumption at 1.8 V**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in EM0 mode with all peripherals disabled | $I_{ACTIVE}$ | 78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running Prime from flash, VSCALE2 | — | 45 | — | µA/MHz |
| | | 78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running while loop from flash, VSCALE2 | — | 41 | — | µA/MHz |
| | | 78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running CoreMark loop from flash, VSCALE2 | — | 57 | — | µA/MHz |
| | | 39 MHz crystal, CPU running Prime from flash | — | 44 | — | µA/MHz |
| | | 39 MHz crystal, CPU running while loop from flash | — | 42 | — | µA/MHz |
| | | 39 MHz crystal, CPU running CoreMark loop from flash | — | 58 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running while loop from flash | — | 35 | — | µA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 38 | — | µA/MHz |
| | | 16 MHz HFRCO, CPU running while loop from flash | — | 46 | — | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 323 | — | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled | $I_{EM1}$ | 78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, VSCALE2 | — | 26 | — | µA/MHz |
| | | 39 MHz crystal | — | 29 | — | µA/MHz |
| | | 38 MHz HFRCO | — | 22 | — | µA/MHz |
| | | 26 MHz HFRCO | — | 25 | — | µA/MHz |
| | | 16 MHz HFRCO | — | 32 | — | µA/MHz |
| | | 1 MHz HFRCO | — | 309 | — | µA/MHz |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in EM2 mode, VSCALE0 | $I_{EM2_VS}$ | 64 kB RAM and full Radio RAM retention, RTC running from LFXO | — | 2.2 | — | µA |
| | | 64 kB RAM and full Radio RAM retention, RTC running from LFRCO | — | 2.2 | — | µA |
| | | 16 kB RAM and full Radio RAM retention, RTC running from LFRCO | — | 1.72 | — | µA |
| | | 16 kB RAM and full Radio RAM retention, RTC running from LFXO | — | 1.75 | — | µA |
| Current consumption in EM3 mode, VSCALE0 | $I_{EM3_VS}$ | 64 kB RAM and full Radio RAM retention, RTC running from ULFRCO | — | 1.84 | — | µA |
| | | 16 kB RAM and full Radio RAM retention, RTC running from ULFRCO | — | 1.4 | — | µA |
| Current consumption for retained RAM bank in EM2 or EM3 | $I_{RAM}$ | Per 16 kB RAM bank | — | 0.15 | — | µA |
| Current consumption in EM4 mode | $I_{EM4}$ | No BURTC, no LF oscillator | — | 0.16 | — | µA |
| | | BURTC with LFXO | — | 0.52 | — | µA |
| Current consumption during reset | $I_{RST}$ | Hard pin reset held | — | 384 | — | µA |
| Additional current in EM2 or EM3 when any peripheral in PD0B is enabled[1] | $I_{PD0B_VS}$ | | — | 1.38 | — | µA |
| Additional current in EM2 or EM3 when any peripheral in PD0C is enabled[1] | $I_{PD0C_VS}$ | | — | 0.21 | — | µA |
| Additional current in EM2 or EM3 when any peripheral in PD0D is enabled[1] | $I_{PD0D_VS}$ | | — | 1.59 | — | µA |
| Additional current in EM2 or EM3 when any peripheral in PD0E is enabled[1] | $I_{PD0E_VS}$ | | — | 0.10 | — | µA |

**Note:**

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.10.4 Power Domains for a list of the peripherals in each power domain. Note that if the PD0B, PD0C, or PD0D domains are enabled, PD0E will also automatically be enabled.

### 4.6.4 Z-Wave Radio Current Consumption at 3.3 V with DCDC

RF current consumption measured with HCLK = 39.0 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: VREGVDD = 3.3 V. AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V from DC-DC. $T_A$ = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at $T_A$ = 25 °C.

**Table 4.8. Z-Wave Radio Current Consumption at 3.3 V with DCDC**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in receive mode, active packet reception, VSCALE1, EM1P[1] | $I_{RX_ACTIVE}$ | f = 868.4 MHz, 2-FSK, 40 kbps | — | 4.0 | — | mA |
| | | f = 868.42 MHz, 2-FSK, 9.6 kbps | — | 4.0 | — | mA |
| | | f = 869.85 MHz, 2-GFSK, 100 kbps | — | 4.0 | — | mA |
| | | f = 908.42 MHz, 2-FSK, 9.6 kbps | — | 4.0 | — | mA |
| | | f = 908.4 MHz, 2-FSK, 40 kbps | — | 4.0 | — | mA |
| | | f = 916 MHz, 2-GFSK, 100 kbps | — | 4.0 | — | mA |
| | | f = 912 MHz, O-QPSK 100 kbps | — | 4.5 | — | mA |
| Current consumption in receive mode, listening for packet, VSCALE1, EM1P[1] | $I_{RX_LISTEN}$ | f = 868.4 MHz, 2-FSK, 40 kbps | — | 4.1 | — | mA |
| | | f = 868.42 MHz, 2-FSK, 9.6 kbps | — | 4.1 | — | mA |
| | | f = 869.85 MHz, 2-GFSK, 100 kbps | — | 4.1 | — | mA |
| | | f = 908.42 MHz, 2-FSK, 9.6 kbps | — | 4.1 | — | mA |
| | | f = 908.4 MHz, 2-FSK, 40 kbps | — | 4.1 | — | mA |
| | | f = 916 MHz, 2-GFSK, 100 kbps | — | 4.1 | — | mA |
| | | f = 912 MHz, O-QPSK 100 kbps | — | 4.4 | — | mA |
| Current consumption in transmit mode, VSCALE2, EM1 | $I_{TX}$ | f = 916 MHz, CW, 14 dBm PA, 0 dBm output power[2] | — | 9.8 | — | mA |
| | | f = 916 MHz, CW, 14 dBm PA, 4 dBm output power[2] | — | 11.8 | — | mA |
| | | f = 916 MHz, CW, 14 dBm PA, 10 dBm output power[2] | — | 17.5 | — | mA |
| | | f = 916 MHz, CW, 14 dBm PA, 14 dBm output power[2] | — | 25.0 | — | mA |
| | | f = 916 MHz, CW, 20 dBm PA, 20 dBm output power[3], PAVDD = 3.3V | — | 85.5 | — | mA |

**Note:**

1. EM1P operation is 0.22 mA lower than EM1 operation
2. Using the +14 dBm matching network for 868/915/920 MHz Bands.
3. Using the +20 dBm matching network for 868/915/920 MHz Bands.

### 4.6.5 Z-Wave Radio Current Consumption at 3.3 V

RF current consumption measured with HCLK = 39.0 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: AVDD = DVDD = IOVDD = RFVDD = PAVDD = 3.3 V. $T_A$ = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at $T_A$ = 25 °C.

**Table 4.9. Z-Wave Radio Current Consumption at 3.3 V**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in receive mode, active packet reception, VSCALE1, EM1P[1] | $I_{RX_ACTIVE}$ | f = 868.4 MHz, 2-FSK, 40 kbps | — | 6.8 | — | mA |
| | | f = 868.42 MHz, 2-FSK, 9.6 kbps | — | 6.8 | — | mA |
| | | f = 869.85 MHz, 2-GFSK, 100 kbps | — | 6.8 | — | mA |
| | | f = 908.42 MHz, 2-FSK, 9.6 kbps | — | 6.8 | — | mA |
| | | f = 908.4 MHz, 2-FSK, 40 kbps | — | 6.8 | — | mA |
| | | f = 916 MHz, 2-GFSK, 100 kbps | — | 6.8 | — | mA |
| | | f = 912 MHz, O-QPSK 100 kbps | — | 7.6 | — | mA |
| Current consumption in receive mode, listening for packet, VSCALE1, EM1P[1] | $I_{RX_LISTEN}$ | f = 868.4 MHz, 2-FSK, 40 kbps | — | 6.9 | — | mA |
| | | f = 868.42 MHz, 2-FSK, 9.6 kbps | — | 6.8 | — | mA |
| | | f = 869.85 MHz, 2-GFSK, 100 kbps | — | 6.9 | — | mA |
| | | f = 908.42 MHz, 2-FSK, 9.6 kbps | — | 6.8 | — | mA |
| | | f = 908.4 MHz, 2-FSK, 40 kbps | — | 6.9 | — | mA |
| | | f = 916 MHz, 2-GFSK, 100 kbps | — | 6.9 | — | mA |
| | | f = 912 MHz, O-QPSK 100 kbps | — | 7.4 | — | mA |
| Current consumption in transmit mode, VSCALE2, EM1 | $I_{TX}$ | f = 916 MHz, CW, 14 dBm PA, 0 dBm output power[2] | — | 16.0 | — | mA |
| | | f = 916 MHz, CW, 14 dBm PA, 4 dBm output power[2] | — | 19.6 | — | mA |
| | | f = 916 MHz, CW, 14 dBm PA, 10 dBm output power[2] | — | 28.8 | — | mA |
| | | f = 916 MHz, CW, 14 dBm PA, 14 dBm output power[2] | — | 41.3 | — | mA |
| | | f = 916 MHz, CW, 20 dBm PA, 20 dBm output power[3] | — | 92 | — | mA |

**Note:**

1. EM1P operation is 0.35 mA lower than EM1 operation
2. Using the +14 dBm matching network for 868/915/920 MHz Bands.
3. Using the +20 dBm matching network for 868/915/920 MHz Bands.

### 4.6.6 Z-Wave Radio Current Consumption at 1.8 V

RF current consumption measured with HCLK = 39.0 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8V. $T_A$ = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at $T_A$ = 25 °C.

**Table 4.10. Z-Wave Radio Current Consumption at 1.8 V**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in receive mode, active packet reception, VSCALE1, EM1P[1] | $I_{RX_ACTIVE}$ | f = 868.4 MHz, 2-FSK, 40 kbps | — | 6.8 | — | mA |
| | | f = 868.42 MHz, 2-FSK, 9.6 kbps | — | 6.8 | — | mA |
| | | f = 869.85 MHz, 2-GFSK, 100 kbps | — | 6.8 | — | mA |
| | | f = 908.42 MHz, 2-FSK, 9.6 kbps | — | 6.8 | — | mA |
| | | f = 908.4 MHz, 2-FSK, 40 kbps | — | 6.8 | — | mA |
| | | f = 916 MHz, 2-GFSK, 100 kbps | — | 6.8 | — | mA |
| | | f = 912 MHz, O-QPSK 100 kbps | — | 7.5 | — | mA |
| Current consumption in receive mode, listening for packet, VSCALE1, EM1P[1] | $I_{RX_LISTEN}$ | f = 868.4 MHz, 2-FSK, 40 kbps | — | 6.9 | — | mA |
| | | f = 868.42 MHz, 2-FSK, 9.6 kbps | — | 6.8 | — | mA |
| | | f = 869.85 MHz, 2-GFSK, 100 kbps | — | 6.9 | — | mA |
| | | f = 908.42 MHz, 2-FSK, 9.6 kbps | — | 6.8 | — | mA |
| | | f = 908.4 MHz, 2-FSK, 40 kbps | — | 6.9 | — | mA |
| | | f = 916 MHz, 2-GFSK, 100 kbps | — | 6.9 | — | mA |
| | | f = 912 MHz, O-QPSK 100 kbps | — | 7.4 | — | mA |
| Current consumption in transmit mode, VSCALE2, EM1 | $I_{TX}$ | f = 916 MHz, CW, 14 dBm PA, 0 dBm output power[2] | — | 16.0 | — | mA |
| | | f = 916 MHz, CW, 14 dBm PA, 4 dBm output power[2] | — | 19.6 | — | mA |
| | | f = 916 MHz, CW, 14 dBm PA, 10 dBm output power[2] | — | 28.8 | — | mA |
| | | f = 916 MHz, CW, 14 dBm PA, 14 dBm output power[2] | — | 41.3 | — | mA |

**Note:**
1. EM1P operation is 0.35 mA lower than EM1 operation
2. Using the +14 dBm matching network for 868/915/920 MHz Bands.

### 4.7 Energy Mode Wake-up and Entry Time

Unless otherwise specified, these times are measured using the HFRCO at 19 MHz, with the DPLL disabled.

**Table 4.11. Energy Mode Wake-up and Entry Time**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Wake-up Time from EM1 | $t_{EM1_WU}$ | Code execution from flash | — | 3 | — | HCLKs |
| | | Code execution from RAM | — | 1.43 | — | µs |
| Wake-up Time from EM2 | $t_{EM2_WU}$ | Code execution from flash, No Voltage Scaling | — | 13.7 | — | µs |
| | | Code execution from RAM, No Voltage Scaling | — | 5.1 | — | µs |
| | | Voltage scaling up one level[1] | — | 37.8 | — | µs |
| | | Voltage scaling up two levels[2] | — | 51.0 | — | µs |
| Wake-up Time from EM3 | $t_{EM3_WU}$ | Code execution from flash, No Voltage Scaling | — | 13.7 | — | µs |
| | | Code execution from RAM, No Voltage Scaling | — | 5.1 | — | µs |
| | | Voltage scaling up one level[1] | — | 37.8 | — | µs |
| | | Voltage scaling up two levels[2] | — | 51.0 | — | µs |
| Wake-up Time from EM4 | $t_{EM4_WU}$ | Code execution from flash | — | 31.0 | — | ms |
| Entry time to EM1 | $t_{EM1_ENT}$ | Code execution from flash | — | 1.29 | — | µs |
| Entry time to EM2 | $t_{EM2_ENT}$ | Code execution from flash | — | 5.9 | — | µs |
| Entry time to EM3 | $t_{EM3_ENT}$ | Code execution from flash | — | 5.7 | — | µs |
| Entry time to EM4 | $t_{EM4_ENT}$ | Code execution from flash | — | 10.7 | — | µs |
| Voltage scaling time in EM0[3] | $t_{SCALE}$ | Up from VSCALE1 to VSCALE2 | — | 32 | — | µs |
| | | Down from VSCALE2 to VSCALE1 | — | 172 | — | µs |

**Note:**

1. Voltage scaling one level is between VSCALE0 and VSCALE1 or between VSCALE1 and VSCALE2.
2. Voltage scaling two levels is between VSCALE0 and VSCALE2.
3. During voltage scaling in EM0, RAM is inaccessible and processor will be halted until complete.

## 4.8 Flash Characteristics

**Table 4.12. Flash Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Flash Supply voltage during write or erase | $V_{FLASH}$ | | 1.71 | — | 3.8 | V |
| Flash data retention[1] | $RET_{FLASH}$ | | 10 | — | — | years |
| Flash erase cycles before failure[1] | $EC_{FLASH}$ | | 10,000 | — | — | cycles |
| Program Time | $t_{PROG}$ | one word (32-bits) | 41 | 44.4 | 47.9 | µs |
| | | average per word over 128 words | 10.2 | 11.2 | 12.1 | µs |
| Page Erase Time[2] | $t_{PERASE}$ | | 11.8 | 12.5 | 14.6 | ms |
| Mass Erase Time[3] [4] | $t_{MERASE}$ | 512 kB | 47.2 | 50.1 | 58.3 | ms |
| Program Current | $I_{WRITE}$ | $T_A$ = 25 °C | — | — | 2.4 | mA |
| Page Erase Current | $I_{ERASE}$ | $T_A$ = 25 °C | — | — | 1.9 | mA |
| Mass Erase Current | $I_{MERASE}$ | $T_A$ = 25 °C | — | — | 1.9 | mA |

**Note:**

1. Flash data retention information is published in the Quarterly Quality and Reliability Report.
2. Page Erase time is measured from setting the ERASEPAGE bit in the MSC_WRITECMD register until the BUSY bit in the MSC-STATUS register is cleared to 0. Internal set-up and hold times are included.
3. Mass Erase is issued by the CPU and erases all of User space.
4. Mass Erase time is measured from setting the ERASEMAIN0 bit in the MSC_WRITECMD register until the BUSY bit in the MSC-STATUS register is cleared to 0. Internal set-up and hold times are included.

## 4.9 Sub-GHz RF Transceiver Characteristics

### 4.9.1 RF Transmitter Characteristics

#### 4.9.1.1 916 MHz Band +20 dBm RF Transmitter Characteristics

This table is for devices with a output power rating of +20 dBm using the 868/915/920 MHz +20 dBm matching network as shown in the typical connections section. Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VREGVDD = 3.3 V, AVDD = DVDD = IOVDD = RFVDD = 1.8 V powered from DCDC. PAVDD = 3.3V. Crystal frequency= 39.0 MHz. RFVDD and external PA supply paths filtered using ferrites. RF center frequency 916 MHz.

**Table 4.13. 916 MHz Band +20 dBm RF Transmitter Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 902 | — | 928 | MHz |
| Maximum TX Power | $POUT_{MAX}$ | PAVDD = 3.3V, 20 dBm devices, +20 dBm match[1 2 3] | 17.7 | 20 | 21.4 | dBm |
| Minimum active TX Power | $POUT_{MIN}$ | | — | -20.6 | — | dBm |
| Output power variation vs supply at $POUT_{MAX}$ | $POUT_{VAR_V}$ | 1.8 V < $V_{PAVDD}$ < 3.8 V, T = 25 °C | — | 4.7 | — | dB |
| Output power variation vs temperature, peak to peak | $POUT_{VAR_T}$ | $T_A$ = -40 to +85 °C with PAVDD = 3.3 V | — | 0.6 | 1.0 | dB |
| | | $T_A$ = -40 to +125 °C with PAVDD = 3.3 V | — | 1.0 | 1.4 | dB |
| Output power variation vs RF frequency | $POUT_{VAR_F}$ | PAVDD = 3.3 V, $T_A$ = 25 °C | — | 0.5 | 0.9 | dB |
| Spurious emissions of harmonics, Conducted measurement, Test Frequency = 916 MHz | $SPUR_{HARM_FCC}$ | In non-restricted bands, per FCC 47 CFR §15.247[4] | — | -58.3 | -20 | dBc |
| | | In restricted bands, per FCC 47 CFR §15.205 & §15.209[5 6] | — | -50.2 | -41.2 | dBm |
| Unwanted signal emissions over frequency domain, Conducted measurement, Test Frequency = 916 MHz | $SPUR_{OOB_FCC}$ | In non-restricted bands, per FCC 47 CFR §15.247[4] | — | -60.0 | -20 | dBc |
| | | In restricted bands (30-88 MHz),per FCC 47 CFR §15.205 & §15.209[5 6] | — | -62.7 | -55.2 | dBm |
| | | In restricted bands (88-216 MHz), per FCC 47 CFR §15.205 & §15.209[5 6] | — | -60.7 | -51.7 | dBm |
| | | In restricted bands (216-960 MHz), per FCC 47 CFR §15.205 & §15.209[5 6] | — | -61.1 | -49.2 | dBm |
| | | In restricted bands (>960 MHz), per FCC 47 CFR §15.205 & §15.209[5 6] | — | -50.6 | -41.2 | dBm |
| Error Vector Magnitude, Offset at +20 dBm output power | EVM | Reference Signal is 100 kbps DSSS-OQPSK, continuous pseudo random binary sequence. Modulated according to Z-Wave Long Range PHY/MAC Layer specification from the Z-Wave Alliance | — | 0.3 | 20 | %rms |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Average Power spectral density limit | $PSD_{AVG_20}$ | PSD per FCC Part 15.247, 100 kbps O-QPSK, Continuous PN9 sequence, Average method per ANSI C63.10-2020 11.10.3 AVGPSD-1 | — | -3.1 | +8 | dBm/ 3kHz |
| Peak Power spectral density limit | $PSD_{PEAK_20}$ | PSD per FCC Part 15.247, 100 kbps O-QPSK, Continuous PN9 sequence, Peak method per ANSI C63.10-2020 11.10.2 Method PKPSD | — | 7.3 | +8 | dBm/ 3kHz |

**Note:**

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.
2. The transmit power for the 902 MHz to 928 Band MHz is normally supports +20 dBm or higher when frequency hopping or DSSS is used. Only the +20 dBm devices are recommended with the +20 dBm match.
3. The 20 dBm match is optimized for best efficiency at maximum power. The maximum output power can go up to the maximum rating. Emissions are tested with the output power set to 20 dBm.
4. FCC Title 47 CFR Part 15 Section 15.247 Operation within the bands 902-928 MHz, 2400-2483.5 MHz, and 5725-5850 MHz.
5. FCC Title 47 CFR Part 15 Section 15.205 Restricted bands of operation.
6. FCC Title 47 CFR Part 15 Section 15.209 Radiated emission limits; general requirements.

#### 4.9.1.2 916 MHz Band +14 dBm RF Transmitter Characteristics

This table is for devices with a output power rating of +14 dBm using the 868/915/920 MHz 14 dBm matching network as shown in the typical connections section. Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VREGVDD = 3.3 V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency= 39.0 MHz. RFVDD and external PA supply paths filtered using ferrites. RF center frequency 916 MHz.

**Table 4.14. 916 MHz Band +14 dBm RF Transmitter Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 902 | — | 928 | MHz |
| Maximum TX Power | $POUT_{MAX}$ | PAVDD connected to DC-DC output, 14 dBm devices, 14 dBm match[1] [2] | 12.6 | 14.3 | 15.3 | dBm |
| Minimum active TX Power | $POUT_{MIN}$ | | — | -22.7 | — | dBm |
| Output power variation vs supply at $POUT_{MAX}$ | $POUT_{VAR_V}$ | 2.2 V < $V_{VREGVDD}$ < 3.8 V, PAVDD connected to DC-DC output, T = 25 °C | — | 0.01 | — | dB |
| Output power variation vs temperature, peak to peak | $POUT_{VAR_T}$ | $T_A$ = -40 to +85 °C with PAVDD connected to DC-DC output | — | 0.6 | 0.9 | dB |
| | | $T_A$ = -40 to +125 °C with PAVDD connected to DC-DC output | — | 0.8 | 1.4 | dB |
| Output power variation vs RF frequency | $POUT_{VAR_F}$ | PAVDD connected to DC-DC output, T = 25 °C | — | 0.6 | 0.9 | dB |
| Spurious emissions of harmonics, Conducted measurement, Test Frequency = 916 MHz | $SPUR_{HARM_FCC}$ | In non-restricted bands, per FCC 47 CFR §15.247[3] | — | -67.6 | -20 | dBc |
| | | In restricted bands, per FCC 47 CFR §15.205 & §15.209[4] [5] | — | -53.5 | -41.2 | dBm |
| Unwanted signal emissions over frequency domain, Conducted measurement, Test Frequency = 916 MHz | $SPUR_{OOB_FCC}$ | In non-restricted bands, per FCC 47 CFR §15.247[3] | — | -68.0 | -20 | dBc |
| | | In restricted bands (30-88 MHz),per FCC 47 CFR §15.205 & §15.209[4] [5] | — | -68.3 | -55.2 | dBm |
| | | In restricted bands (88-216 MHz), per FCC 47 CFR §15.205 & §15.209[4] [5] | — | -68.3 | -51.7 | dBm |
| | | In restricted bands (216-960 MHz), per FCC 47 CFR §15.205 & §15.209[4] [5] | — | -68.1 | -49.2 | dBm |
| | | In restricted bands (>960 MHz), per FCC 47 CFR §15.205 & §15.209[4] [5] | — | -56.4 | -41.2 | dBm |
| Error Vector Magnitude, Offset at +14 dBm output power | EVM | Reference Signal is 100 kbps DSSS-OQPSK, continuous pseudo random binary sequence. Modulated according to Z-Wave Long Range PHY/MAC Layer specification from the Z-Wave Alliance | — | 0.4 | 20 | %rms |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Average Power spectral density limit | $PSD_{AVG_14}$ | PSD per FCC Part 15.247, 100 kbps O-QPSK, Continuous PN9 sequence, Average method per ANSI C63.10-2020 11.10.3 AVGPSD-1 | — | -8.7 | +8 | dBm/ 3kHz |
| Peak Power spectral density limit | $PSD_{PEAK_14}$ | PSD per FCC Part 15.247, 100 kbps O-QPSK, Continuous PN9 sequence, Peak method per ANSI C63.10-2020 11.10.2 Method PKPSD | — | 1.4 | +8 | dBm/ 3kHz |

**Note:**

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.
2. The 14 dBm match is optimized for best efficiency at 14 dBm. The maximum output power can go up to the maximum rating. Emissions are tested with the output power set to 14 dBm.
3. FCC Title 47 CFR Part 15 Section 15.247 Operation within the bands 902-928 MHz, 2400-2483.5 MHz, and 5725-5850 MHz.
4. FCC Title 47 CFR Part 15 Section 15.205 Restricted bands of operation.
5. FCC Title 47 CFR Part 15 Section 15.209 Radiated emission limits; general requirements.

#### 4.9.1.3 916 MHz Band 0 dBm RF Transmitter Characteristics

Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VREGVDD = 3.3 V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency= 39.0 MHz. RFVDD and external PA supply paths filtered using ferrites. RF center frequency 908.4 MHz.

**Table 4.15. 916 MHz Band 0 dBm RF Transmitter Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 902 | — | 928 | MHz |
| Maximum TX Power | $POUT_{MAX}$ | PAVDD connected to DC-DC output, 14 dBm devices, +14 dBm match[1] [2] for operation mode under FCC 15.249 | -1.9 | 0.4 | 2.0 | dBm |
| Minimum active TX Power | $POUT_{MIN}$ | | — | -22.7 | — | dBm |
| Output power variation vs supply at $POUT_{MAX}$ | $POUT_{VAR_V}$ | 2.2 V < $V_{VREGVDD}$ < 3.8 V, PAVDD connected to DC-DC output, T = 25 °C | — | 0.01 | — | dB |
| Output power variation vs temperature, peak to peak | $POUT_{VAR_T}$ | $T_A$ = -40 to +85 °C with PAVDD connected to DC-DC output | — | 1.2 | 1.9 | dB |
| | | $T_A$ = -40 to +125 °C with PAVDD connected to DC-DC output | — | 1.5 | 2.4 | dB |
| Output power variation vs RF frequency | $POUT_{VAR_F}$ | PAVDD connected to DC-DC output, T = 25 °C | — | 0.6 | 0.9 | dB |
| Spurious emissions of harmonics at 0 dBm output power, Conducted measurement, 0dBm match, Test Frequency = 908.4 MHz | $SPUR_{HARM_FCC}$ | Per FCC 47 CFR §15.205 & §15.209[3] [4] | — | -52.8 | -41.2 | dBm |
| Spurious emissions out-of-band at 0 dBm output power, Conducted measurement, 0dBm match, Test Frequency = 908.4 MHz | $SPUR_{OOB_FCC}$ | (30-88 MHz),per FCC 47 CFR §15.205 & §15.209[3] [4] | — | -79.4 | -55.2 | dBm |
| | | (88-216 MHz), per FCC 47 CFR §15.205 & §15.209[3] [4] | — | -76.6 | -51.7 | dBm |
| | | (216-960 MHz), per FCC 47 CFR §15.205 & §15.209[3] [4] | — | -69.5 | -49.2 | dBm |
| | | (>960 MHz), per FCC 47 CFR §15.205 & §15.209[3] [4] | — | -70.7 | -41.2 | dBm |

**Note:**

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.
2. The 14 dBm match is optimized for best efficiency at 14 dBm. The maximum output power can go up to the maximum rating. All parameters are tested with the output power set to 0 dBm.
3. FCC Title 47 CFR Part 15 Section 15.205 Restricted bands of operation.
4. FCC Title 47 CFR Part 15 Section 15.209 Radiated emission limits; general requirements.

#### 4.9.1.4 868 MHz Band +20 dBm RF Transmitter Characteristics

This table is for devices with a output power rating of +20 dBm using the 868/915/920 MHz +20 dBm matching network as shown in the typical connections section. Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VREGVDD = 3.3 V, AVDD = DVDD = IOVDD = RFVDD = 1.8 V powered from DCDC. PAVDD = 3.3V. Crystal frequency= 39.0 MHz. RFVDD and external PA supply paths filtered using ferrites. RF center frequency 869.5 MHz.

**Table 4.16. 868 MHz Band +20 dBm RF Transmitter Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 869.4 | — | 869.65 | MHz |
| Maximum TX Power | $POUT_{MAX}$ | PAVDD = 3.3V, 20 dBm devices, +20 dBm match[1] [2] | 18.4 | 20.3 | 21.5 | dBm |
| Minimum active TX Power | $POUT_{MIN}$ | | — | -20.4 | — | dBm |
| Output power variation vs supply at $POUT_{MAX}$ | $POUT_{VAR_V}$ | 1.8 V < $V_{PAVDD}$ < 3.8 V, T = 25 °C | — | 4.4 | — | dB |
| Output power variation vs temperature, peak to peak | $POUT_{VAR_T}$ | $T_A$ = -40 to +85 °C, PAVDD = 3.3 V | — | 0.5 | 0.8 | dB |
| | | $T_A$ = -40 to +125 °C, PAVDD = 3.3 V | — | 0.8 | 1.2 | dB |
| Output power variation vs RF frequency | $POUT_{VAR_F}$ | PAVDD = 3.3 V, T = 25 °C | — | 0.02 | 0.08 | dB |
| Spurious emissions of harmonics, +20 dBm match, $P_{OUT}$ = +20 dBm, 869.5 MHz | $SPUR_{HARM_ETSI}$ | (frequencies above 1 GHz)[3] | — | -39.5 | -30 | dBm |
| Unwanted emissions in spurious domain, Per ETSI EN 300-220-1[4],+20 dBm match, $P_{OUT}$ = +20 dBm, 869.5 MHz | $SPUR_{OOB_ETSI}$ | (47-74 MHz, 87.5-118 MHz, 174-230 MHz, and 470-862 MHz)[3] | — | -60.3 | -54 | dBm |
| | | (other frequencies below 1 GHz)[3] | — | -56.9 | -36 | dBm |
| | | (frequencies above 1 GHz)[3] | — | -52.1 | -30 | dBm |
| Error Vector Magnitude, per 802.15.4-2020 | EVM | Signal is 100 kbps DSSS-OQPSK reference packet. Modulated according to 802.15.4-2020 in the 868MHz band, with pseudo-random packet data content. $P_{OUT}$ = +20 dBm. | — | 6.1 | 35 | % |

**Note:**

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.
2. The 20 dBm match is optimized for best efficiency at 20 dBm. The maximum output power can go up to the maximum rating. Emissions are tested with the output power set to 20 dBm.
3. Spurious emission limits per EN 300-220-1 v3.1.1 5.9.2
4. Conducted measurement per EN 300-220-1 v3.1.1 5.9.3.3.1

#### 4.9.1.5 868 MHz Band +14 dBm RF Transmitter Characteristics

This table is for devices with a output power rating of +14 dBm using the 868/915/920 MHz +14 dBm matching network as shown in the typical connections section. Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VREGVDD = 3.3 V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency= 39.0 MHz. RFVDD and external PA supply paths filtered using ferrites. RF center frequency 868.3 MHz

**Table 4.17. 868 MHz Band +14 dBm RF Transmitter Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 863 | — | 869.2 | MHz |
| Maximum TX Power | $POUT_{MAX}$ | PAVDD connected to DC-DC output, 14 dBm devices, 14 dBm match[1] [2] | 13.3 | 14.5 | 15.3 | dBm |
| Minimum active TX Power | $POUT_{MIN}$ | | — | -22.1 | — | dBm |
| Output power variation vs supply at $POUT_{MAX}$ | $POUT_{VAR_V}$ | 2.2 V < $V_{VREGVDD}$ < 3.8 V, PAVDD connected to DC-DC output, T = 25 °C | — | 0.01 | — | dB |
| Output power variation vs temperature, peak to peak | $POUT_{VAR_T}$ | $T_A$ = -40 to +85 °C with PAVDD connected to DC-DC output | — | 0.4 | 0.8 | dB |
| | | $T_A$ = -40 to +125 °C with PAVDD connected to DC-DC output | — | 0.6 | 1.2 | dB |
| Output power variation vs RF frequency | $POUT_{VAR_F}$ | PAVDD connected to DC-DC output, T = 25 °C | — | 0.04 | 0.1 | dB |
| Spurious emissions of harmonics, Conducted measurement, +14 dBm match, $P_{OUT}$ = +14 dBm, 868.4 MHz | $SPUR_{HARM_ETSI}$ | (frequencies above 1 GHz)[3] | — | -42.5 | -30 | dBm |
| Spurious emissions out-of-band, Conducted measurement, +14 dBm match, $P_{OUT}$ = +14 dBm, 868.4 MHz | $SPUR_{OOB_ETSI}$ | Per ETSI EN 300-220, Section 7.8.2.1 (47-74 MHz, 87.5-118 MHz, 174-230 MHz, and 470-862 MHz) | — | -67.0 | -54 | dBm |
| | | Per ETSI EN 300-220, Section 7.8.2.1 (other frequencies below 1 GHz) | — | -64.2 | -36 | dBm |
| | | Per ETSI EN 300-220, Section 7.8.2.1 (frequencies above 1 GHz) | — | -58.9 | -30 | dBm |

**Note:**

1. The output power level can be adjusted to suit specific regulatory requirements for the region in which the device is used.
2. The 14 dBm match is optimized for best efficiency at 14 dBm. The maximum output power can go up to the maximum rating. Emissions are tested with the output power set to 14 dBm.
3. Spurious emission limits per EN 300-220-1 v3.1.1 5.9.2

#### 4.9.1.6 433 MHz Band +10 dBm RF Transmitter Characteristics

This table is for devices with a output power rating of +14 dBm using the 433 MHz 10 dBm matching network as shown in the typical connections section. Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VREGVDD = 3.3 V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency= 39.0 MHz. RFVDD and external PA supply paths filtered using ferrites. RF center frequency 433.92 MHz.

**Table 4.18. 433 MHz Band +10 dBm RF Transmitter Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 433 | — | 434.79 | MHz |
| Maximum TX Power | $POUT_{MAX}$ | PAVDD connected to DC-DC output, 14 dBm devices, 10dBm match[1][2][3] | 10.8 | 12.3 | 13.2 | dBm |
| Minimum active TX Power | $POUT_{MIN}$ | | — | -19.1 | — | dBm |
| Output power variation vs supply, peak to peak, Pout = 10dBm | $POUT_{VAR_V}$ | 2.2 V < $V_{VREGVDD}$ < 3.8 V, PAVDD connected to DC-DC output, T = 25 °C | — | 0.01 | — | dB |
| Output power variation vs temperature, peak to peak, Pout= 10dBm | $POUT_{VAR_T}$ | $T_A$ = -40 to +85 °C with PAVDD connected to DC-DC output | — | 0.5 | 0.9 | dB |
| | | $T_A$ = -40 to +125 °C with PAVDD connected to DC-DC output | — | 0.6 | 1.2 | dB |
| Output power variation vs RF frequency, Pout = 10dBm | $POUT_{VAR_F}$ | T = 25 °C | — | 0.06 | 0.09 | dB |
| Unwanted emissions in spurious domain, Per ETSI EN 300-220-1[4],+10 dBm match, $P_{OUT}$ = +10 dBm, 433.92 MHz | $SPUR_{OOB_ETSI}$ | (47-74 MHz, 87.5-118 MHz, 174-230 MHz, and 470-862 MHz)[5] | — | -70.1 | -54 | dBm |
| | | (other frequencies below 1 GHz)[5] | — | -69.0 | -36 | dBm |
| | | (frequencies above 1 GHz)[5] | — | -45.3 | -30 | dBm |
| Spurious emissions of harmonics ETSI, Conducted measurement, +10 dBm match, $P_{OUT}$ = +10 dBm, 433.92 MHz | $SPUR_{HARM_ETSI}$ | (other frequencies below 1 GHz)[5] | — | -58 | -36 | dBm |
| | | (frequencies above 1 GHz)[5] | — | -48.5 | -30 | dBm |
| Spurious emissions of harmonics FCC, Conducted measurement, +10 dBm match, $P_{OUT}$ = 10 dBm, 433.0 MHz[6] | $SPUR_{HARM_FCC}$ | Per FCC 47 CFR §15.205 & §15.209[7][8][9] | — | -48.2 | -41.2 | dBm |
| Spurious emissions out-of-band FCC, Conducted measurement, +10 dBm match, $P_{OUT}$ = 10 dBm, 433.0 MHz[6] | $SPUR_{OOB_FCC}$ | 30-88 MHz, per FCC 47 CFR §15.205 & §15.209[7][8][9] | — | -68.8 | -55.2 | dBm |
| | | 88-216 MHz, per FCC 47 CFR §15.205 & §15.209[7][8][9] | — | -69.8 | -51.7 | dBm |
| | | 216-960 MHz, per FCC 47 CFR §15.205 & §15.209[7][8][9] | — | -66.7 | -49.2 | dBm |
| | | >960 MHz, per FCC 47 CFR §15.205 & §15.209[7][8][9] | — | -75.3 | -41.2 | dBm |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|

**Note:**

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.
2. Using the +10 dBm matching network for the 433 MHz Band. The 10 dBm match is optimized for best efficiency at 10 dBm. The maximum output power can go up to the maximum rating. Emissions are tested with the output power set to 10 dBm.
3. Specific regional requirements for this band normally limit the maximum Tx power in this band to 10 dBm or less. Only the 14 dBm part numbers are reccomended for this band.
4. Conducted measurement per EN 300-220-1 v3.1.1 5.9.3.3.1
5. Spurious emission limits per EN 300-220-1 v3.1.1 5.9.2
6. FCC emissions are specificed at a power level of 10 dBm conducted. A lower power setting may be required to meet the FCC limit specified in µV at 3m.
7. FCC Title 47 CFR Part 15 Section 15.231 Periodic operation in the band 40.66-40.70 MHz and above 70 MHz.
8. FCC Title 47 CFR Part 15 Section 15.205 Restricted bands of operation.
9. FCC Title 47 CFR Part 15 Section 15.209 Radiated emission limits; general requirements.

### 4.9.2 RF Receiver Characteristics

#### 4.9.2.1 916 MHz Band RF Receiver Characteristics for Z-Wave

Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VREGVDD = 3.3 V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency= 39.0 MHz. RFVDD and external PA supply paths filtered using ferrites. RF center frequency 916 MHz.

**Table 4.19. 916 MHz Band RF Receiver Characteristics for Z-Wave**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 902 | — | 928 | MHz |
| Rx Max Strong Signal Input Level for 1% FER | $RX_{SAT}$ | Desired is reference 100 kbps GFSK signal[1] | — | — | 10.0 | dBm |
| Sensitivity | SENS | Desired is reference 9.6 kbps 2FSK signal[2], 1% FER, frequency = 908.42 MHz | — | -109.3 | — | dBm |
| | | Desired is reference 40 kbps 2FSK signal[3], 1% FER, frequency = 908.4 MHz | — | -109.7 | — | dBm |
| | | Desired is reference 100 kbps GFSK signal[1], 1% FER, frequency = 916 MHz | — | -108.1 | — | dBm |
| | | Desired is reference 100 kbps O-QPSK signal[4], 1% FER, frequency = 912 MHz | — | -109.8 | — | dBm |
| Image rejection, Interferer is CW at image frequency | IR | Desired is reference 9.6 kbps 2FSK signal[2] at 3dB above sensitivity level, 1% FER, frequency = 908.42 MHz | — | 50.7 | — | dB |
| | | Desired is reference 40 kbps 2FSK signal[3] at 3dB above sensitivity level, 1% FER, frequency = 908.4 MHz | — | 50.9 | — | dB |
| | | Desired is 100 kbps GFSK signal[1] at 3dB above sensitivity level, 1% FER, frequency = 916 MHz | — | 49.6 | — | dB |
| | | Desired is reference 100 kbps O-QPSK signal[4], 1% FER, frequency = 912 MHz | — | 53.3 | — | dB |
| Blocking selectivity, 1% FER. Desired is 9.6 kbps 2FSK signal[2] at 3dB above sensitivity level, frequency = 908.42 MHz | $BLOCK_{9p6}$ | Interferer CW at Desired ± 1 MHz | — | 58.7 | — | dB |
| | | Interferer CW at Desired ± 2 MHz | — | 63.5 | — | dB |
| | | Interferer CW at Desired ± 5 MHz | — | 73.0 | — | dB |
| | | Interferer CW at Desired ± 10 MHz | — | 79.0 | — | dB |
| | | Interferer CW at Desired ± 100 MHz | — | 82.5 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Blocking selectivity, 1% FER. Desired is 40 kbps 2FSK signal[3] at 3dB above sensitivity level, frequency = 908.4 MHz | $BLOCK_{40}$ | Interferer CW at Desired ± 1 MHz | — | 59.3 | — | dB |
| | | Interferer CW at Desired ± 2 MHz | — | 63.7 | — | dB |
| | | Interferer CW at Desired ± 5 MHz | — | 73.6 | — | dB |
| | | Interferer CW at Desired ± 10 MHz | — | 79.4 | — | dB |
| | | Interferer CW at Desired ± 100 MHz | — | 82.1 | — | dB |
| Blocking selectivity, 1% FER. Desired is 100 kbps GFSK signal[1] at 3dB above sensitivity level, frequency = 916 MHz | $BLOCK_{100}$ | Interferer CW at Desired ± 1 MHz | — | 49.6 | — | dB |
| | | Interferer CW at Desired ± 2 MHz | — | 63.1 | — | dB |
| | | Interferer CW at Desired ± 5 MHz | — | 72.3 | — | dB |
| | | Interferer CW at Desired ± 10 MHz | — | 78.0 | — | dB |
| | | Interferer CW at Desired ± 100 MHz | — | 80.3 | — | dB |
| Blocking selectivity, 1% FER. Desired is 100 kbps O-QPSK signal[4] at 3dB above reference sensitivity of -89dBm, frequency = 912 MHz | $BLOCK_{OQPSK}$ | Interferer CW at Desired ± 2 MHz | — | 58.4 | — | dB |
| | | Interferer CW at Desired ± 5 MHz | — | 72.2 | — | dB |
| | | Interferer CW at Desired ± 10 MHz | — | 78.9 | — | dB |
| | | Interferer CW at Desired ± 100 MHz | — | 84.3 | — | dB |
| Intermod selectivity, 1% FER. CW interferers at 400 kHz and 800 kHz offsets | IM | Desired is 100 kbps GFSK signal[1] at 3dB above sensitivity level | — | 43.4 | — | dB |
| Upper limit of input power range over which RSSI resolution is maintained | $RSSI_{MAX}$ | | — | — | 10.0 | dBm |
| Lower limit of input power range over which RSSI resolution is maintained | $RSSI_{MIN}$ | | -90.0 | — | — | dBm |
| RSSI resolution | $RSSI_{RES}$ | Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range | — | 0.25 | — | dB |
| Max spurious emissions during active receive mode, per FCC Part 15.109(a) | $SPUR_{RX_FCC}$ | 216-960 MHz | — | -81.7 | -49.2 | dBm |
| | | Above 960 MHz | — | -78.7 | -41.2 | dBm |

**Note:**

1. Definition of reference signal is 100 kbps 2GFSK, BT=0.6, Δf = 58 kHz, NRZ, '0' = F_center + Δf/2, '1' = F_center - Δf/2
2. Definition of reference signal is 9.6 kbps 2FSK, Δf = 40 kHz, Manchester, '0' = Transition from (F_center + Δf/2), '1' = Transition from (F_center - Δf/2)
3. Definition of reference signal is 40 kbps 2FSK, Δf = 40 kHz, NRZ, '0' = F_center + Δf/2, '1' = F_center - Δf/2
4. Definition of reference signal is 100 kbps O-QPSK, 800 kcps chip rate, 8x spreading factor, 32 bit chip length, 4 bits per symbol

#### 4.9.2.2 915 MHz Band RF Receiver Characteristics

Band is 902 to 928 MHz. Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VREGVDD = 3.3 V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency= 39.0 MHz. RFVDD and external PA supply paths filtered using ferrites. RF center frequency 915 MHz.

**Table 4.20. 915 MHz Band RF Receiver Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 902 | — | 928 | MHz |
| Rx Max Strong Signal Input Level for 0.1% BER | $RX_{SAT}$ | Desired is reference 2 Mbps 2GFSK signal[1] | — | — | 10 | dBm |
| Sensitivity | SENS | Desired is reference 4.8 kbps OOK signal, PER<20%[2] | — | -113.1 | — | dBm |
| | | Desired is reference 50 kbps 2FSK signal, Δf = ± 25 kHz, PER<10%[3] | — | -110.1 | — | dBm |
| | | Desired is reference 50 kbps 2FSK signal, Δf = ± 25 kHz, PER<10% with FEC[4] | — | -114.2 | — | dBm |
| | | Desired is reference 150 kbps 2FSK signal, Δf = ± 37.5 kHz, PER<10%[5] | — | -107.5 | — | dBm |
| | | Desired is reference 2 Mbps 2GFSK signal, Δf = ± 500 kHz, BER<0.1%[1] | — | -96.9 | — | dBm |
| | | Desired is reference 4.8 kbps O-QPSK signal, spreading factor=8, PER<1%[6] | — | -125.8 | — | dBm |
| | | Desired is reference 250 kbps O-QPSK DSSS signal, PER<1%[7] | — | -103.5 | — | dBm |
| | | Desired is reference 120 kbps OOK signal[8], PER<20% | — | -102.6 | — | dBm |
| Adjacent channel rejection, Interferer is CW at ± 1 × channel spacing | ACR1 | Desired is reference 4.8 kbps OOK signal[2] at 3dB above sensitivity level | — | 49.6 | — | dB |
| | | Desired is reference 50 kbps 2FSK signal[3] at 3dB above sensitivity level | — | 44.1 | — | dB |
| | | Desired is reference 150 kbps 2FSK signal[5] at 3dB above sensitivity level | — | 43.8 | — | dB |
| | | Desired is reference 250 kbps O-QPSK DSSS signal[7] at 3dB above sensitivity level | — | 46.6 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Alternate channel rejection, Interferer is CW at ± 2 × channel spacing | ACR2 | Desired is reference 4.8 kbps OOK signal[2] at 3dB above sensitivity level | — | 64.0 | — | dB |
| | | Desired is reference 50 kbps 2FSK signal[3] at 3dB above sensitivity level | — | 51.5 | — | dB |
| | | Desired is reference 150 kbps 2FSK signal[5] at 3dB above sensitivity level | — | 57.7 | — | dB |
| | | Desired is reference 250 kbps O-QPSK DSSS signal[7] at 3dB above sensitivity level | — | 50.7 | — | dB |
| Image rejection, Interferer is CW at image frequency | IR | Desired is reference 4.8 kbps OOK signal[2] at 3dB above sensitivity level | — | 43.0 | — | dB |
| | | Desired is reference 50 kbps 2FSK signal[3] at 3dB above sensitivity level | — | 44.0 | — | dB |
| | | Desired is reference 150 kbps 2FSK signal[5] at 3dB above sensitivity level | — | 44.5 | — | dB |
| | | Desired is reference 250 kbps O-QPSK DSSS signal[7] at 3dB above sensitivity level | — | 52.3 | — | dB |
| Blocking Selectivity U/D ratio for 1% PER. Desired signal at 3 dB above required sensitivity. Undesired signal is CW at ± 1 MHz frequency offset. | $BLOCK_{1M}$ | 50 kbps 2GFSK[9] | — | 63.9 | — | dB |
| Blocking Selectivity U/D ratio for 1% PER. Desired signal at 3 dB above required sensitivity. Undesired signal is CW at ± 2 MHz frequency offset. | $BLOCK_{2M}$ | 50 kbps 2GFSK[9] | — | 71.3 | — | dB |
| Blocking Selectivity U/D ratio for 1% PER. Desired signal at 3 dB above required sensitivity. Undesired signal is CW at ± 10 MHz frequency offset. | $BLOCK_{10M}$ | 50 kbps 2GFSK[9] | — | 81.4 | — | dB |
| Intermod selectivity, PER < 10%. CW interferers at 400 kHz and 800 kHz offsets | IM | Desired is reference 50 kbps 2GFSK signal[3] at 3dB above sensitivity level | — | 48.2 | — | dB |
| Upper limit of input power range over which RSSI resolution is maintained | $RSSI_{MAX}$ | | — | — | 10.0 | dBm |
| Lower limit of input power range over which RSSI resolution is maintained | $RSSI_{MIN}$ | | -97.0 | — | — | dBm |
| RSSI resolution | $RSSI_{RES}$ | Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range | — | 0.25 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Max spurious emissions during active receive mode, per FCC Part 15.109(a) | $SPUR_{RX_FCC}$ | 216-960 MHz | — | -81.7 | -49.2 | dBm |
| | | Above 960 MHz | — | -78.7 | -41.2 | dBm |

**Note:**

1. The modulation bandwidth may not be suitable for regional regulatory requirements in this band. Crystal tolerance = 0 ppm.
2. Definition of reference signal is 4.8 kbps Manchester-encoded OOK, RX channel BW = 350 kHz, channel spacing = 500 kHz.
3. Definition of reference signal is 50 kbps 2FSK, BT = 2, mi = 1.0, PER<10%, Channel Spacing = 200 kHz, Data Whitening, no FEC. Per Wi-SUN PHY 1.0 standard mode #1b.
4. Definition of reference signal is 50 kbps 2FSK, BT = 2, mi = 1.0, PER<10%, Channel Spacing = 200 kHz, Data Whitening, with FEC. Per Wi-SUN PHY 1.0 standard mode #1b.
5. Definition of reference signal is 150 kbps 2FSK, BT = 2, mi = 0.5, PER<10%, Channel Spacing = 400 kHz, Data Whitening, no FEC. Per Wi-SUN FAN PHY 1.0 standard mode #3.
6. Definition of reference signal is 4.8 kbps O-QPSK DSSS long-range PHY, 38.4 kcps chip rate, chipping code length 32, PER<1%. Crystal tolerance = 0 ppm.
7. Definition of reference signal is O-QPSK DSSS, Data rate = 250 kbps, 32-chip PN sequence mapping, <1% PER, Channel Spacing = 2 MHz, payload length = 20 octets. Crystal tolerance = 0 ppm.
8. Definition of reference signal is 120 kbps OOK, RX channel BW = 350 kHz, channel spacing = 500 kHz.
9. Definition of reference signal is 50 kbps 2GFSK, BT=1, mi=1.0, PER<1%, Δf = ± 25 kHz, Channel Spacing = 200 kHz.

#### 4.9.2.3 868 MHz Band RF Receiver Characteristics for Z-Wave

Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VREGVDD = 3.3 V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency= 39.0 MHz. RFVDD and external PA supply paths filtered using ferrites. RF center frequency 868.4 MHz.

**Table 4.21. 868 MHz Band RF Receiver Characteristics for Z-Wave**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 863 | — | 870 | MHz |
| Rx Max Strong Signal Input Level for 1% FER | $RX_{SAT}$ | Desired is reference 100 kbps GFSK signal[1] | — | — | 10.0 | dBm |
| Sensitivity | SENS | Desired is reference 9.6 kbps 2FSK signal[2], 1% FER, frequency = 868.42 MHz | — | -109.9 | — | dBm |
| | | Desired is reference 40 kbps 2FSK signal[3], 1% FER, frequency = 868.4 MHz | — | -110.0 | — | dBm |
| | | Desired is reference 100 kbps GFSK signal[1], 1% FER, frequency = 869.85 MHz | — | -108.6 | — | dBm |
| Image rejection, Interferer is CW at image frequency | IR | Desired is reference 9.6 kbps 2FSK signal[2] at 3dB above sensitivity level, 1% FER, frequency = 868.42 MHz | — | 49.6 | — | dB |
| | | Desired is reference 40 kbps 2FSK signal[3] at 3dB above sensitivity level, 1% FER, frequency = 868.4 MHz | — | 49.8 | — | dB |
| | | Desired is 100kbps GFSK signal[1] at 3dB above sensitivity level, 1% FER, frequency = 869.85 MHz | — | 48.1 | — | dB |
| Blocking selectivity, 1% FER. Desired is 9.6 kbps 2FSK signal[2] at 3 dB above sensitivity level, frequency = 868.42 MHz | $BLOCK_{9p6}$ | Interferer CW at Desired ± 1 MHz | — | 59.4 | — | dB |
| | | Interferer CW at Desired ± 2 MHz | — | 64.2 | — | dB |
| | | Interferer CW at Desired ± 5 MHz | — | 73.7 | — | dB |
| | | Interferer CW at Desired ± 10 MHz | — | 79.6 | — | dB |
| | | Interferer CW at Desired ± 100 MHz | — | 83.3 | — | dB |
| Blocking selectivity, 1% FER. Desired is 40 kbps 2FSK signal[3] at 3 dB above sensitivity level, frequency = 868.4 MHz | $BLOCK_{40}$ | Interferer CW at Desired ± 1 MHz | — | 59.7 | — | dB |
| | | Interferer CW at Desired ± 2 MHz | — | 64.3 | — | dB |
| | | Interferer CW at Desired ± 5 MHz | — | 74.0 | — | dB |
| | | Interferer CW at Desired ± 10 MHz | — | 79.8 | — | dB |
| | | Interferer CW at Desired ± 100 MHz | — | 83.8 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Blocking selectivity, 1% FER. Desired is 100 kbps GFSK signal[1] at 3 dB above sensitivity level, frequency = 869.85 MHz | $BLOCK_{100}$ | Interferer CW at Desired ± 1 MHz | — | 48.1 | — | dB |
| | | Interferer CW at Desired ± 2 MHz | — | 63.4 | — | dB |
| | | Interferer CW at Desired ± 5 MHz | — | 72.6 | — | dB |
| | | Interferer CW at Desired ± 10 MHz | — | 78.3 | — | dB |
| | | Interferer CW at Desired ± 100 MHz | — | 80.6 | — | dB |
| Upper limit of input power range over which RSSI resolution is maintained | $RSSI_{MAX}$ | | — | — | 10 | dBm |
| Lower limit of input power range over which RSSI resolution is maintained | $RSSI_{MIN}$ | | -90.0 | — | — | dBm |
| RSSI resolution | $RSSI_{RES}$ | Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range | — | 0.25 | — | dB |
| Max spurious emissions during active receive mode | $SPUR_{RX}$ | 30 MHz to 1 GHz | — | -81.7 | -57 | dBm |
| | | 1 GHz to 6 GHz | — | -71.7 | -47 | dBm |

**Note:**

1. Definition of reference signal is 100 kbps 2GFSK, BT=0.6, Δf = 58 kHz, NRZ, '0' = F_center + Δf/2, '1' = F_center - Δf/2
2. Definition of reference signal is 9.6 kbps 2FSK, Δf = 40 kHz, Manchester, '0' = Transition from (F_center + Δf/2), '1' = Transition from (F_center - Δf/2)
3. Definition of reference signal is 40 kbps 2FSK, Δf = 40 kHz, NRZ, '0' = F_center + Δf/2, '1' = F_center - Δf/2

#### 4.9.2.4 868 MHz Band RF Receiver Characteristics

Band is 868 to 870 MHz. Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VREGVDD = 3.3 V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency= 39.0 MHz. RFVDD and external PA supply paths filtered using ferrites. RF center frequency 868.3 MHz.

**Table 4.22. 868 MHz Band RF Receiver Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 863 | — | 870 | MHz |
| Rx Max Strong Signal Input Level for 0.1% BER | $RX_{SAT}$ | Desired is reference 500 kbps 2GMSK signal[1] | — | — | 10.0 | dBm |
| Sensitivity | SENS | Desired is reference 2.4 kbps 2GFSK signal, Δf = ± 1.2 kHz, BER<0.1%[2] | — | -125.3 | — | dBm |
| | | Desired is reference 38.4 kbps 2GFSK signal, Δf = ± 20 kHz, BER<0.1%[3] | — | -113.3 | — | dBm |
| | | Desired is reference 50 kbps 2FSK signal, Δf = ± 12.5 kHz, PER<10%[4] | — | -111.5 | — | dBm |
| | | Desired is reference 100 kbps 2FSK signal, Δf = ± 25 kHz, PER<10%[5] | — | -109.2 | — | dBm |
| | | Desired is reference 500 kbps 2GMSK signal, Δf = ± 125 kHz[1], BER<0.1%[6] | — | -103.2 | — | dBm |
| | | Desired is reference 100 kbps O-QPSK DSSS signal, PER<1%[7] | — | -110.9 | — | dBm |
| Adjacent channel rejection, Interferer is CW at ± 1 × channel spacing | ACR1 | Desired is reference 2.4 kbps 2GFSK signal[2] at 3dB above sensitivity level | — | -43.9 | — | dBm |
| | | Desired is reference 38.4 kbps 2GFSK signal[3] at 3dB above sensitivity level | — | 45.0 | — | dB |
| | | Desired is reference 50 kbps 2FSK signal[4] at 3dB above sensitivity level | — | 43.5 | — | dB |
| | | Desired is reference 100 kbps 2FSK signal[5] at 3dB above sensitivity level | — | 44.2 | — | dB |
| | | Desired is reference 100 kbps O-QPSK DSSS signal [7] at 3dB above sensitivity level | — | 57.4 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Alternate channel rejection, Interferer is CW at ± 2 × channel spacing | ACR2 | Desired is reference 2.4 kbps 2GFSK signal[2] at 3dB above sensitivity level | — | -44.4 | — | dBm |
| | | Desired is reference 38.4 kbps 2GFSK signal[3] at 3dB above sensitivity level | — | 37.9 | — | dB |
| | | Desired is reference 50 kbps 2FSK signal[4] at 3dB above sensitivity level | — | 42.8 | — | dB |
| | | Desired is reference 100 kbps 2FSK signal[5] at 3dB above sensitivity level | — | 51.2 | — | dB |
| | | Desired is reference 100 kbps O-QPSK DSSS signal [7] at 3dB above sensitivity level | — | 65.7 | — | dB |
| Image rejection, Interferer is CW at image frequency | IR | Desired is reference 2.4 kbps 2GFSK signal[2] at 3dB above sensitivity level | — | -51.0 | — | dBm |
| | | Desired is reference 38.4 kbps 2GFSK signal[3] at 3dB above sensitivity level | — | 38.0 | — | dB |
| | | Desired is reference 50 kbps 2FSK signal[4] at 3dB above sensitivity level | — | 43.7 | — | dB |
| | | Desired is reference 100 kbps 2FSK signal[5] at 3dB above sensitivity level | — | 44.9 | — | dB |
| | | Desired is reference 100 kbps O-QPSK DSSS signal [7] at 3dB above sensitivity level | — | 50.3 | — | dB |
| Blocking selectivity, 0.1% BER. Desired is 2.4 kbps 2GFSK signal[2] at 3 dB above sensitivity level | $BLOCK_{24}$ | Interferer CW at Desired ± 2 MHz | — | -17.0 | — | dBm |
| | | Interferer CW at Desired ± 10 MHz | — | -6.7 | — | dBm |
| | | Interferer CW at Desired ± 43.4 MHz | — | -4.5 | — | dBm |
| Blocking Selectivity U/D ratio for 1% PER. Desired signal at 3 dB above required sensitivity. Undesired signal is CW at ± 1 MHz frequency offset. | $BLOCK_{1M}$ | 50 kbps 2GFSK signal[8] | — | 65.5 | — | dB |
| Blocking Selectivity U/D ratio for 1% PER. Desired signal at 3 dB above required sensitivity. Undesired signal is CW at ± 2 MHz frequency offset. | $BLOCK_{2M}$ | 50 kbps 2GFSK signal[8] | — | 72.3 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Blocking Selectivity U/D ratio for 1% PER. Desired signal at 3 dB above required sensitivity. Undesired signal is CW at ± 10 MHz frequency offset. | $BLOCK_{10M}$ | 50 kbps 2GFSK signal[8] | — | 80.8 | — | dB |
| Upper limit of input power range over which RSSI resolution is maintained | $RSSI_{MAX}$ | | — | — | 10 | dBm |
| Lower limit of input power range over which RSSI resolution is maintained | $RSSI_{MIN}$ | | -103 | — | — | dBm |
| RSSI resolution | $RSSI_{RES}$ | Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range | — | 0.25 | — | dB |
| Max spurious emissions during active receive mode | $SPUR_{RX}$ | 30 MHz to 1 GHz | — | -81.7 | -57 | dBm |
| | | 1 GHz to 12 GHz | — | -71.7 | -47 | dBm |

**Note:**

1. Definition of reference signal is 500 kbps 2GMSK, BT = 0.5, mi = 0.5, BER<0.1%, RX channel BW = 753.320 kHz. Crystal tolerance = 0 ppm.
2. Definition of reference signal is 2.4 kbps 2GFSK, BT = 0.5, mi = 1.0, BER<0.1%, RX channel BW = 10 kHz, channel spacing = 25 kHz.
3. Definition of reference signal is 38.4 kbps 2GFSK, BT = 0.5, mi = 1.04, BER<0.1%, RX channel BW = 74.809 kHz, channel spacing = 100 kHz. Crystal tolerance = 0 ppm.
4. Definition of reference signal is 50 kbps 2FSK, BT = 2, mi = 0.5, PER<10%, Channel Spacing = 100 kHz, Data Whitening, no FEC. Per Wi-SUN FAN PHY 1.0 standard mode #1a.
5. Definition of reference signal is 100 kbps 2FSK, BT = 2, mi = 0.5, PER<10%, Channel Spacing = 200 kHz, Data Whitening, no FEC. Per Wi-SUN FAN PHY 1.0 standard mode #2a.
6. The modulation bandwidth may not be suitable for regional regulatory requirements in this band. Crystal tolerance = 0 ppm.
7. Definition of reference signal is O-QPSK DSSS per IEEE802.15.4, Data rate = 100 kbps, 4 bit to 16 chip PN sequence mapping, PER<1%, Channel Spacing = 2 MHz, payload length=20 octets.
8. Definition of reference signal is 50 kbps 2GFSK, BT=1, mi=1.0, PER<1%, Δf = ± 25 kHz, Channel Spacing = 200 kHz.

#### 4.9.2.5 433 MHz Band RF Receiver Characteristics

Band is 433.05 MHz to 434.79 MHz. Unless otherwise indicated, typical conditions are: $T_A$ = 25 °C, VREGVDD = 3.3 V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency= 39.0 MHz. RFVDD and external PA supply paths filtered using ferrites. RF center frequency 433.92 MHz.

**Table 4.23. 433 MHz Band RF Receiver Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF test frequency range | $F_{RANGE}$ | | 433 | — | 434.79 | MHz |
| Rx Max Strong Signal Input Level for 0.1% BER | $RX_{SAT}$ | Desired is reference 100 kbps 2GFSK signal, BER<0.1%[1] | — | — | 10 | dBm |
| Sensitivity | SENS | Desired is reference 2.4 kbps 2GFSK signal, Δf = ± 1.2 kHz, BER<0.1%[2] | — | -126.9 | — | dBm |
| | | Desired is reference 4.8 kbps OOK signal, PER<20%[3] | — | -114.2 | — | dBm |
| | | Desired is reference 100 kbps 2GFSK signal, Δf = ± 50 kHz, BER<0.1%[1] | — | -110.7 | — | dBm |
| | | Desired is reference 50 kbps 2GFSK signal, Δf = ± 25 kHz, BER<0.1%[4] | — | -113.8 | — | dBm |
| | | Desired is reference 50 kbps 4GFSK signal, $\Delta f_o$ = ± 25 kHz, $\Delta f_i$ = ± 8.33 kHz, PER<1%[5] | — | -112.1 | — | dBm |
| | | Desired is reference 460 MHz 4.8 kbps 2FSK signal, Δf = ± 2.4 kHz, PER<10%[6] | — | -122.5 | — | dBm |
| Adjacent channel rejection, Interferer is CW at ± 1 × channel spacing | ACR1 | Desired is reference 4.8 kbps OOK signal[3] at 3dB above sensitivity level | — | 54.7 | — | dB |
| | | Desired is reference 2.4 kbps 2GFSK signal[2] at 3dB above sensitivity level | — | 63.9 | — | dB |
| Alternate channel rejection, Interferer is CW at ± 2 × channel spacing | ACR2 | Desired is reference 4.8 kbps OOK signal[3] at 3dB above sensitivity level | — | 67.5 | — | dB |
| | | Desired is reference 2.4 kbps 2GFSK signal[2] at 3dB above sensitivity level | — | 63.9 | — | dB |
| Image rejection, Interferer is CW at image frequency | IR | Desired is reference 4.8 kbps OOK signal[3] at 3dB above sensitivity level | — | 49.6 | — | dB |
| | | Desired is reference 2.4 kbps 2GFSK signal[2] at 3dB above sensitivity level | — | 73.9 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Blocking selectivity, 0.1% BER. Desired is 2.4 kbps 2GFSK signal[2] at 3dB above sensitivity level | BLOCK | Interferer CW at Desired ± 1 MHz | — | 84.1 | — | dB |
| | | Interferer CW at Desired ± 2 MHz | — | 90.6 | — | dB |
| | | Interferer CW at Desired ± 10 MHz | — | 95.8 | — | dB |
| Intermod selectivity, 0.1% BER. CW interferers at 12.5 kHz and 25 kHz offsets | IM | Desired is reference 2.4 kbps 2GFSK signal[2] at 3dB above sensitivity level | — | 56.1 | — | dB |
| Upper limit of input power range over which RSSI resolution is maintained | $RSSI_{MAX}$ | | — | — | 10 | dBm |
| Lower limit of input power range over which RSSI resolution is maintained | $RSSI_{MIN}$ | | -111.0 | — | — | dBm |
| RSSI resolution | $RSSI_{RES}$ | Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range | — | 0.25 | — | dB |
| Max spurious emissions during active receive mode, per FCC Part 15.109(a) | $SPUR_{RX_FCC}$ | 216-960 MHz | — | -81.0 | -49.2 | dBm |
| | | Above 960 MHz | — | -79.4 | -41.2 | dBm |
| Max spurious emissions during active receive mode, per ETSI 300-220 Section 8.6 | $SPUR_{RX_ETSI}$ | Below 1000 MHz | — | -81.4 | -57 | dBm |
| | | Above 1000 MHz | — | -72.2 | -47 | dBm |
| Max spurious emissions during active receive mode, per ARIB STD T67 Section 3.3(5) | $SPUR_{RX_ARIB}$ | Below 710 MHz, RBW=100kHz | — | -84.8 | -54 | dBm |

**Note:**

1. Definition of reference signal is 100 kbps 2GFSK, BT = 0.5, mi = 1.0, BER<0.1%, RX channel BW = 200 kHz, Crystal tolerance = 0 ppm.
2. Definition of reference signal is 2.4 kbps 2GFSK, BT = 0.5, mi = 1.0, BER<0.1%, Channel Spacing = 12.5 kHz, RX channel BW = 4.8 kHz.
3. Definition of reference signal is 4.8 kbps Manchester-encoded OOK, RX channel BW = 350 kHz, channel spacing = 500 kHz.
4. Definition of reference signal is 50 kbps 2GFSK, BT = 0.5, mi = 1.0, BER<0.1%, RX channel BW = 100 kHz, Crystal tolerance = 0 ppm.
5. Definition of reference signal is 50 kbps 4GFSK, BT = 1.0, mi = 0.66, PER<1%, RX channel BW = 74.98 kHz, Crystal tolerance = 0 ppm.
6. Definition of reference signal is 4.8 kbps 2FSK, BT = 2, mi = 1.0, PER<10%, Channel Spacing = 12.5 kHz, Data Whitening, no FEC, 460 MHz center frequency. Per IEEE 802.15.4g 450 MHz band, mode 2.

## 4.10 Frequency Synthesizer

**Table 4.24. Frequency Synthesizer**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF synthesizer frequency range | $f_{RANGE}$ | 742 - 970 MHz | 742 | — | 970 | MHz |
| | | 557 - 727 MHz | 557 | — | 727 | MHz |
| | | 372 - 557 MHz | 372 | — | 557 | MHz |
| | | 223 - 372 MHz | 223 | — | 372 | MHz |
| | | 110 - 223 MHz | 110 | — | 223 | MHz |
| LO tuning frequency resolution with 39.0 MHz crystal | $f_{RES}$ | 742 - 970 MHz | — | — | 24.8 | Hz |
| | | 557 - 727 MHz | — | — | 18.6 | Hz |
| | | 372 - 557 MHz | — | — | 12.4 | Hz |
| | | 223 - 372 MHz | — | — | 7.4 | Hz |
| | | 110 - 223 MHz | — | — | 5.0 | Hz |
| Frequency deviation resolution with 39.0 MHz crystal | $df_{RES}$ | 742 - 970 MHz | — | — | 24.8 | Hz |
| | | 557 - 727 MHz | — | — | 18.6 | Hz |
| | | 372 - 557 MHz | — | — | 12.4 | Hz |
| | | 223 - 372 MHz | — | — | 7.4 | Hz |
| | | 110 - 223 MHz | — | — | 5.0 | Hz |
| Maximum frequency deviation with 39.0 MHz crystal | $df_{MAX}$ | 742 - 970 MHz | — | — | 617 | kHz |
| | | 557 - 727 MHz | — | — | 463 | kHz |
| | | 372 - 557 MHz | — | — | 308 | kHz |
| | | 223 - 372 MHz | — | — | 185 | kHz |
| | | 110 - 223 MHz | — | — | 116 | kHz |

## 4.11 Oscillators

### 4.11.1 High Frequency Crystal Oscillator

Unless otherwise indicated, typical conditions are: AVDD = DVDD = 3.3 V. $T_A$ = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

**Table 4.25. High Frequency Crystal Oscillator**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Crystal Frequency | $F_{HFXO}$ | see note[1] | 38.0 | 39.0 | 40.0 | MHz |
| Supported range of crystal load capacitance[2] | $C_{L_HFXO}$ | 39.0 MHz[3] | — | 10 | — | pF |
| Supported crystal maximum equivalent series resistance (ESR) | $ESR_{HFXO}$ | 39.0 MHz[4] | — | — | 60 | Ω |
| Supply Current | $I_{HFXO}$ | | — | 498 | — | µA |
| Startup Time[5] | $T_{STARTUP}$ | 39.0 MHz, $C_L$ = 10 pF[3] | — | 178 | — | µs |
| On-chip tuning cap step size[6] | $SS_{HFXO}$ | | — | 0.04 | — | pF |
| HFCLKOUT load capacitance | $C_{HFCLKOUT}$ | | — | 20 | 30 | pF |
| HFCLKOUT output voltage | $V_{HFCLKOUT}$ | | 0 | — | 1.2 | V |
| HFCLKOUT AC output amplitude, XOUTBIASANA = 5, $C_{HFCLKOUT}$ = 20 pF | $VAC_{HFCLKOUT}$ | XOUTCFANA = 0 | — | 470 | — | mVpp |
| | | XOUTCFANA = 1 | — | 510 | — | mVpp |
| | | XOUTCFANA = 2 | — | 560 | — | mVpp |
| | | XOUTCFANA = 3 | — | 615 | — | mVpp |
| HFCLKOUT current consumption | $I_{HFCLKOUT}$ | $C_{HFCLKOUT}$ ≤ 10 pF, XOUTBIASANA = 3 | — | 3.1 | — | mA |
| | | 10 pF < $C_{HFCLKOUT}$ ≤ 20 pF, XOUTBIASANA = 5 | — | 3.9 | — | mA |
| | | 20 pF < $C_{HFCLKOUT}$ ≤ 30 pF, XOUTBIASANA = 15 | — | 6.3 | — | mA |
| Frequency shift of HFXTAL when HFCLKOUT is active | $FS_{HFCLKOUT}$ | Assuming crystal pullability of 13 ppm/pF | -1.5 | — | 4.5 | ppm |
| HFCLKOUT shorting output resistance | $RS_{HFCLKOUT}$ | When output is disabled | — | 150 | — | Ω |
| Total harmonic distortion, XOUTBIASANA = 5, $C_{HFCLKOUT}$ = 20 pF | $THD_{HFCLKOUT}$ | XOUTCFANA = 0 | — | 8.53 | — | % |
| | | XOUTCFANA = 1 | — | 10.05 | — | % |
| | | XOUTCFANA = 2 | — | 11.98 | — | % |
| | | XOUTCFANA = 3 | — | 14.39 | — | % |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|

**Note:**

1. All sub-GHz RF measurements made using a 39 MHz crystal. Other crystal frequencies supported, but RF performance may vary.
2. Total load capacitance as seen by the crystal.
3. RF performance characteristics have been determined using crystals with a maximum ESR of 35 Ω and $C_L$ of 10 pF.
4. The crystal should have a maximum ESR less than or equal to this maximum rating.
5. Startup time does not include time implemented by programmable TIMEOUTSTEADY delay.
6. The tuning step size is the effective step size when incrementing both of the tuning capacitors by one count. The step size for the each of the individual tuning capacitors is twice this value.

### 4.11.2 Low Frequency Crystal Oscillator

**Table 4.26. Low Frequency Crystal Oscillator**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Crystal Frequency | $F_{LFXO}$ | | — | 32.768 | — | kHz |
| Supported Crystal equivalent series resistance (ESR) | $ESR_{LFXO}$ | GAIN = 0 | — | — | 80 | kΩ |
| | | GAIN = 1 to 3 | — | — | 100 | kΩ |
| Supported range of crystal load capacitance [1] | $C_{L_LFXO}$ | GAIN = 0 | 4 | — | 6 | pF |
| | | GAIN = 1 | 6 | — | 10 | pF |
| | | GAIN = 2 (see note[2]) | 10 | — | 12.5 | pF |
| | | GAIN = 3 (see note[2]) | 12.5 | — | 18 | pF |
| Current consumption | $I_{CL12p5}$ | ESR = 70 kΩ, $C_L$ = 12.5 pF, GAIN[3] = 2, AGC[4] = 1 | — | 290 | — | nA |
| Startup Time | $T_{STARTUP}$ | ESR = 70 kΩ, $C_L$ = 7 pF, GAIN[3] = 1, AGC[4] = 1 | — | 52 | — | ms |
| On-chip tuning cap step size | $SS_{LFXO}$ | | — | 0.26 | — | pF |
| On-chip tuning capacitor value at minimum setting[5] | $C_{LFXO_MIN}$ | CAPTUNE = 0 | — | 4 | — | pF |
| On-chip tuning capacitor value at maximum setting[5] | $C_{LFXO_MAX}$ | CAPTUNE = 0x4F | — | 24.5 | — | pF |

**Note:**

1. Total load capacitance seen by the crystal
2. Crystals with a load capacitance of greater than 12 pF require external load capacitors.
3. In LFXO_CAL Register
4. In LFXO_CFG Register
5. The effective load capacitance seen by the crystal will be $C_{LFXO}/2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal

### 4.11.3 High Frequency RC Oscillator (HFRCO)

Unless otherwise indicated, typical conditions are: AVDD = DVDD = 3.3 V. $T_A$ = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

**Table 4.27. High Frequency RC Oscillator (HFRCO)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Frequency Accuracy | $F_{HFRCO_ACC}$ | For all production calibrated frequencies | -3 | — | 3 | % |
| Current consumption on all supplies[1] | $I_{HFRCO}$ | $F_{HFRCO}$ = 4 MHz | — | 28 | — | µA |
| | | $F_{HFRCO}$ = 5 MHz[2] | — | 29 | — | µA |
| | | $F_{HFRCO}$ = 7 MHz | — | 59 | — | µA |
| | | $F_{HFRCO}$ = 10 MHz[2] | — | 63 | — | µA |
| | | $F_{HFRCO}$ = 13 MHz | — | 77 | — | µA |
| | | $F_{HFRCO}$ = 16 MHz | — | 87 | — | µA |
| | | $F_{HFRCO}$ = 19 MHz | — | 90 | — | µA |
| | | $F_{HFRCO}$ = 20 MHz[2] | — | 107 | — | µA |
| | | $F_{HFRCO}$ = 26 MHz | — | 116 | — | µA |
| | | $F_{HFRCO}$ = 32 MHz | — | 139 | — | µA |
| | | $F_{HFRCO}$ = 38 MHz[3] | — | 170 | — | µA |
| | | $F_{HFRCO}$ = 40 MHz[2] | — | 172 | — | µA |
| | | $F_{HFRCO}$ = 48 MHz[3] | — | 207 | — | µA |
| | | $F_{HFRCO}$ = 56 MHz[3] | — | 228 | — | µA |
| | | $F_{HFRCO}$ = 64 MHz[3] | — | 269 | — | µA |
| | | $F_{HFRCO}$ = 80 MHz[3] | — | 285 | — | µA |
| Clock Out current for HFRCODPLL[4] | $I_{CLKOUT_HFRCODPLL}$ | FORCEEN bit of HFRCO0_CTRL = 1 | — | 3.0 | — | µA/MHz |
| Clock Out current for HFRCOEM23[4] | $I_{CLKOUT_HFRCOEM23}$ | FORCEEN bit of HFRCOEM23_CTRL = 1 | — | 1.6 | — | µA/MHz |
| Startup Time[5] | $T_{STARTUP}$ | FREQRANGE = 0 to 7 | — | 1.2 | — | µs |
| | | FREQRANGE = 8 to 15 | — | 0.6 | — | µs |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Band Frequency Limits[6] | $f_{HFRCO_BAND}$ | FREQRANGE = 0 | 3.71 | — | 5.24 | MHz |
| | | FREQRANGE = 1 | 4.39 | — | 6.26 | MHz |
| | | FREQRANGE = 2 | 5.25 | — | 7.55 | MHz |
| | | FREQRANGE = 3 | 6.22 | — | 9.01 | MHz |
| | | FREQRANGE = 4 | 7.88 | — | 11.6 | MHz |
| | | FREQRANGE = 5 | 9.9 | — | 14.6 | MHz |
| | | FREQRANGE = 6 | 11.5 | — | 17.0 | MHz |
| | | FREQRANGE = 7 | 14.1 | — | 20.9 | MHz |
| | | FREQRANGE = 8 | 16.4 | — | 24.7 | MHz |
| | | FREQRANGE = 9 | 19.8 | — | 30.4 | MHz |
| | | FREQRANGE = 10 | 22.7 | — | 34.9 | MHz |
| | | FREQRANGE = 11 | 28.6 | — | 44.4 | MHz |
| | | FREQRANGE = 12 | 33.0 | — | 51.0 | MHz |
| | | FREQRANGE = 13 | 42.2 | — | 64.6 | MHz |
| | | FREQRANGE = 14 | 48.8 | — | 74.8 | MHz |
| | | FREQRANGE = 15 | 57.6 | — | 87.4 | MHz |

**Note:**

1. Does not include additional clock tree current. See specifications for additional current when selected as a clock source for a particular clock multiplexer.
2. This frequency is calibrated for the HFRCOEM23 only.
3. This frequency is calibrated for the HFRCODPLL (HFRCO0) only.
4. When the HFRCO is enabled for characterization using the FORCEEN bit, the total current will be the HFRCO core current plus the specified CLKOUT current. When the HFRCO is enabled on demand, the clock current may be different.
5. Hardware delay ensures settling to within ± 0.5%. Hardware also enforces this delay on a band change.
6. The frequency band limits represent the lowest and highest frequency which each band can achieve over the operating range.

### 4.11.4 Fast Start_Up RC Oscillator (FSRCO)

**Table 4.28. Fast Start_Up RC Oscillator (FSRCO)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| FSRCO frequency | $F_{FSRCO}$ | | 17.2 | 20 | 21.2 | MHz |

### 4.11.5 Low Frequency RC Oscillator (LFRCO)

**Table 4.29. Low Frequency RC Oscillator (LFRCO)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Nominal oscillation frequency | $F_{LFRCO}$ | | — | 32.768 | — | kHz |
| Frequency accuracy | $F_{LFRCO_ACC}$ | | -3 | — | 3 | % |
| Frequency calibration step | $F_{TRIM_STEP}$ | Typical trim step at mid-scale | — | 0.33 | — | % |
| Startup time | $t_{STARTUP}$ | | — | 220 | — | µs |
| Current consumption | $I_{LFRCO}$ | | — | 186 | — | nA |

### 4.11.6 Ultra Low Frequency RC Oscillator

**Table 4.30. Ultra Low Frequency RC Oscillator**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Oscillation Frequency | $F_{ULFRCO}$ | | 0.944 | 1.0 | 1.095 | kHz |

### 4.12 GPIO Pins (3V GPIO pins)

**Table 4.31. GPIO Pins (3V GPIO pins)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Leakage current | $I_{LEAK_IO}$ | MODEx = DISABLED, IOVDD = 1.71 V | — | 1.9 | — | nA |
| | | MODEx = DISABLED, IOVDD = 3.3 V | — | 2.5 | — | nA |
| | | MODEx = DISABLED, IOVDD = 3.8 V, $T_A$ = 125 °C, Pins PA00, PB00-PB01, and PC06-PC09 | — | — | 250 | nA |
| | | MODEx = DISABLED, IOVDD = 3.8 V, $T_A$ = 125 °C, all other GPIO | — | — | 200 | nA |
| Input low voltage[1] | $V_{IL}$ | Any GPIO pin | — | — | 0.3 * IOVDD | V |
| | | RESETn | — | — | 0.3 * DVDD | V |
| Input high voltage[1] | $V_{IH}$ | Any GPIO pin | 0.7 * IOVDD | — | — | V |
| | | RESETn | 0.7 * DVDD | — | — | V |
| Hysteresis of input voltage | $V_{HYS}$ | Any GPIO pin | 0.05 * IOVDD | — | — | V |
| | | RESETn | 0.05 * DVDD | — | — | V |
| Output high voltage | $V_{OH}$ | Sourcing 20mA, IOVDD = 3.3 V | 0.8 * IOVDD | — | — | V |
| | | Sourcing 8mA, IOVDD = 1.71 V | 0.6 * IOVDD | — | — | V |
| Output low voltage | $V_{OL}$ | Sinking 20mA, IOVDD = 3.3 V | — | — | 0.2 * IOVDD | V |
| | | Sinking 8mA, IOVDD = 1.71 V | — | — | 0.4 * IOVDD | V |
| GPIO rise time | $T_{GPIO_RISE}$ | IOVDD = 3.3 V, $C_{load}$ = 50pF, SLEWRATE = 4, 10% to 90% | — | 8.4 | — | ns |
| | | IOVDD = 1.7 V, $C_{load}$ = 50pF, SLEWRATE = 4, 10% to 90% | — | 13 | — | ns |
| GPIO fall time | $T_{GPIO_FALL}$ | IOVDD = 3.3 V, $C_{load}$ = 50pF, SLEWRATE = 4, 90% to 10% | — | 7.1 | — | ns |
| | | IOVDD = 1.7 V, $C_{load}$ = 50pF, SLEWRATE = 4, 90% to 10% | — | 11.9 | — | ns |
| Pull up/down resistance[2] | $R_{PULL}$ | Any GPIO pin. Pull-up to IOVDD: MODEn = DISABLE DOUT=1. Pull-down to VSS: MODEn = WIREDORPULLDOWN DOUT = 0. | 33 | 44 | 55 | kΩ |
| | | RESETn pin. Pull-up to DVDD | 33 | 44 | 55 | kΩ |
| Maximum filtered glitch width | $T_{GF}$ | MODE = INPUT, DOUT = 1 | — | 27 | — | ns |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RESETn low time to ensure pin reset | $T_{RESET}$ | | 100 | — | — | ns |

**Note:**

1. GPIO input thresholds are proportional to the IOVDD pin. RESETn input thresholds are proportional to DVDD.
2. GPIO pull-ups connect to IOVDD supply, pull-downs connect to VSS. RESETn pull-up connects to DVDD.

### 4.13 Analog to Digital Converter (IADC)

**Table 4.32. Analog to Digital Converter (IADC)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Main analog supply | $V_{AVDD}$ | Normal mode | 1.71 | — | 3.8 | V |
| Maximum Input Range[1] | $V_{IN_MAX}$ | Maximum allowable input voltage | 0 | — | AVDD | V |
| Full-Scale Voltage | $V_{FS}$ | Voltage required for Full-Scale measurement | — | $V_{REF}$ / Gain | — | V |
| Input Measurement Range | $V_{IN}$ | Differential Mode - Plus and Minus inputs | $-V_{FS}$ | — | $+V_{FS}$ | V |
| | | Single Ended Mode - One input tied to ground | 0 | — | $V_{FS}$ | V |
| Input Sampling Capacitance | Cs | Analog Gain = 1x | — | 1.8 | — | pF |
| | | Analog Gain = 2x | — | 3.6 | — | pF |
| | | Analog Gain = 3x | — | 5.4 | — | pF |
| | | Analog Gain = 4x | — | 7.2 | — | pF |
| | | Analog Gain = 0.5x | — | 0.9 | — | pF |
| ADC clock frequency | $f_{ADC_CLK}$ | Normal mode, Gain = 1x or 0.5x | — | — | 10 | MHz |
| | | Normal mode, Gain = 2x | — | — | 5 | MHz |
| | | Normal mode, Gain = 3x or 4x | — | — | 2.5 | MHz |
| Input sampling frequency | $f_S$ | Normal Mode | — | $f_{ADC_CLK}/4$ | — | MHz |
| Throughput rate | $f_{SAMPLE}$ | Normal mode, $f_{ADC_CLK}$ = 10 MHz, OSR = 2 | — | — | 1 | Msps |
| | | Normal mode, $f_{ADC_CLK}$ = 10 MHz, OSR = 32 | — | — | 76.9 | ksps |
| Current from all supplies, Continuous operation | $I_{ADC_CONT}$ | Normal Mode, 1 Msps, OSR = 2, $f_{ADC_CLK}$ = 10 MHz | — | 305 | 385 | µA |
| Current in Standby mode. ADC is not functional but can wake up in 1us. | $I_{STBY}$ | Normal mode | — | 17 | — | µA |
| ADC Startup Time | $t_{startup}$ | From power down state | — | 5 | — | µs |
| | | From standby state | — | 1 | — | µs |
| Normal Mode ADC Resolution[2] | Resolution | OSR = 2 | — | 12 | — | bits |
| | | OSR = 32 | — | 16 | — | bits |
| Differential Nonlinearity | DNL | Normal mode. Differential Input. OSR = 2 (No missing codes) | -1 | +/- 0.25 | 1.5 | LSB12 |
| Integral Nonlinearity | INL | Normal mode. Differential Input, OSR = 2 | -2.5 | +/- 0.65 | 2.5 | LSB12 |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Effective number of bits[3] | ENOB | Normal Mode, Differential Input. Gain = 1x, OSR = 2, $f_{IN}$ = 10 kHz, Internal VREF = 1.21V | 10.7 | 11.7 | — | bits |
| | | Normal Mode, Differential Input. Gain = 1x, OSR = 32, $f_{IN}$ = 2.5 kHz, Internal VREF = 1.21 V. | — | 13.5 | — | bits |
| | | Normal Mode, Differential Input. Gain = 1x, OSR = 32, $f_{IN}$ = 2.5 kHz, External VREF = 1.25 V. | — | 14.3 | — | bits |
| Signal to Noise + Distortion Ratio Normal Mode[3] | SNDR | Differential Input. Gain=1x, OSR = 2, $f_{IN}$ = 10 kHz, Internal VREF = 1.21V | 66 | 72.3 | — | dB |
| | | Differential Input. Gain=2x, OSR = 2, $f_{IN}$ = 10 kHz, Internal VREF = 1.21V | — | 72.3 | — | dB |
| | | Differential Input. Gain=4x, OSR = 2, $f_{IN}$ = 10 kHz, Internal VREF = 1.21V | — | 68.8 | — | dB |
| | | Differential Input. Gain=0.5x, OSR = 2, $f_{IN}$ = 10 kHz, Internal VREF = 1.21V | — | 72.5 | — | dB |
| | | Differential Input. Gain = 1x, OSR = 64, $f_{IN}$ = 1.25 kHz, Internal VREF = 1.21 V | — | 83.9 | — | dB |
| Total Harmonic Distortion | THD | Normal mode, Differential Input. Gain = 1x, OSR = 2, $f_{IN}$ = 10 kHz, Internal VREF = 1.21 V | — | -80.8 | -70 | dB |
| Spurious-Free Dynamic Range | SFDR | Normal mode, Differential Input. Gain = 1x, OSR = 2, $f_{IN}$ = 10 kHz, Internal VREF = 1.21 V | 72 | 86.5 | — | dB |
| Common Mode Rejection Ratio | CMRR | Normal mode. DC to 100 Hz | — | 87.0 | — | dB |
| | | Normal mode. AC high frequency. | — | 68.6 | — | dB |
| Power Supply Rejection Ratio | PSRR | Normal mode. DC to 100 Hz | — | 80.4 | — | dB |
| | | Normal mode. AC high frequency, using internal VBGR | — | 33.4 | — | dB |
| | | Normal mode. AC high frequency, using VREF pad | — | 65.2 | — | dB |
| External reference voltage range[1] | $V_{EVREF}$ | | 1.0 | — | AVDD | V |
| Offset Error, Normal mode | OFFSET | GAIN = 1 and 0.5, Differential Input | -3 | 0.27 | 3 | LSB12 |
| | | GAIN = 2, Differential Input | -4 | 0.27 | 4 | LSB12 |
| | | GAIN = 3, Differential Input | -4 | 0.25 | 4 | LSB12 |
| | | GAIN = 4, Differential Input | -4 | 0.29 | 4 | LSB12 |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Gain Error, Normal mode | GE | GAIN = 1 and 0.5, using external VREF, direct mode, $f_{ADC_CLK}$ = 10 MHz | -0.3 | 0.069 | 0.3 | % |
| | | GAIN = 2, using external VREF, direct mode, $f_{ADC_CLK}$ = 5 MHz | -0.4 | 0.151 | 0.4 | % |
| | | GAIN = 3, using external VREF, direct mode, $f_{ADC_CLK}$ = 2.5 MHz | -0.7 | 0.186 | 0.7 | % |
| | | GAIN = 4, using external VREF, direct mode, $f_{ADC_CLK}$ = 2.5 MHz | -1.1 | 0.227 | 1.1 | % |
| | | Internal VREF [4], all GAIN settings | -1.5 | 0.023 | 1.5 | % |
| Internal Reference voltage | $V_{IVREF}$ | | — | 1.21 | — | V |

**Note:**

1. When inputs are routed to external GPIO pins, the maximum pin voltage is limited to the lower of the IOVDD and AVDD supplies.
2. ADC output resolution depends on the OSR and digital averaging settings. With no digital averaging, ADC output resolution is 12 bits at OSR = 2, 13 bits at OSR = 4, 14 bits at OSR = 8, 15 bits at OSR = 16, 16 bits at OSR = 32 and 17 bits at OSR = 64. Digital averaging has a similar impact on ADC output resolution. See the product reference manual for additional details.
3. The relationship between ENOB and SNDR is specified according to the equation: ENOB = (SNDR - 1.76) / 6.02.
4. Includes error from internal VREF drift.

### 4.14 Analog Comparator (ACMP)

**Table 4.33. Analog Comparator (ACMP)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ACMP Supply current | $I_{ACMP}$ | BIAS = 2 [1], HYST = DISABLED | — | 510 | — | nA |
| | | BIAS = 3 [1], HYST = DISABLED | — | 1.8 | — | µA |
| | | BIAS = 4, HYST = DISABLED | — | 5.3 | — | µA |
| | | BIAS = 5, HYST = DISABLED | — | 10.2 | — | µA |
| | | BIAS = 6, HYST = DISABLED | — | 24.6 | — | µA |
| | | BIAS = 7, HYST = DISABLED | — | 45.6 | 100 | µA |
| ACMP Supply current with Hysteresis | $I_{ACMP_WHYS}$ | BIAS = 2 [1], HYST = SYM30MV | — | 760 | — | nA |
| | | BIAS = 3 [1], HYST = SYM30MV | — | 2.7 | — | µA |
| | | BIAS = 4, HYST = SYM30MV | — | 7.1 | — | µA |
| | | BIAS = 5, HYST = SYM30MV | — | 14.2 | — | µA |
| | | BIAS = 6, HYST = SYM30MV | — | 35.1 | — | µA |
| | | BIAS = 7, HYST = SYM30MV | — | 65.7 | — | µA |
| Current consumption from VREFDIV in continuous mode | $I_{VREFDIV}$ | NEGSEL = VREFDIVAVDD | — | 3.4 | — | µA |
| | | NEGSEL = VREFDIV1V25 | — | 4.2 | — | µA |
| | | NEGSEL = VREFDIV2V5 | — | 6.9 | — | µA |
| Current consumption from VREFDIV in sample/hold mode | $I_{VREFDIV_SH}$ | NEGSEL = VREFDIV2V5LP | — | 76 | — | nA |
| | | NEGSEL = VREFDIV1V25LP | — | 73 | — | nA |
| | | NEGSEL = VREFDIVAVDDLP | — | 72 | — | nA |
| Current consumption from VSENSEDIV in continuous mode | $I_{VSENSEDIV}$ | NEGSEL = VSENSE01DIV4 | — | 1.8 | — | µA |
| Current consumption from VSENSEDIV in sample/hold mode | $I_{VSENSEDIV_SH}$ | NEGSEL = VSENSE01DIV4LP | — | 58 | — | nA |
| Hysteresis (BIAS = 4) | $V_{HYST_4}$ | HYST = SYM10MV[2] | — | 18 | — | mV |
| | | HYST = SYM20MV[2] | — | 34 | — | mV |
| | | HYST = SYM30MV[2] | — | 48 | — | mV |
| Reference Voltage | $V_{ACMPREF}$ | Internal 1.25 V Reference | 1.19 | 1.25 | 1.31 | V |
| | | Internal 2.5 V Reference | 2.34 | 2.5 | 2.75 | V |
| Input offset voltage | $V_{OFFSET}$ | BIAS = 2, VCM = 0.15 to AVDD - 0.15 V | -25 | — | 25 | mV |
| | | BIAS = 4, VCM = 0.15 to AVDD - 0.15 V | -25 | — | 25 | mV |
| | | BIAS = 7, VCM = 0.15 to AVDD - 0.15 V | -30 | — | 30 | mV |
| Input Range | $V_{IN}$ | Input Voltage Range | 0 | — | AVDD | V |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Comparator delay with 100 mV overdrive | $T_{DELAY}$ | BIAS = 2 | — | 0.87 | — | µs |
| | | BIAS = 3 | — | 0.28 | — | µs |
| | | BIAS = 4 | — | 160 | — | ns |
| | | BIAS = 5 | — | 94 | — | ns |
| | | BIAS = 6 | — | 60 | — | ns |
| | | BIAS = 7 | — | 49 | — | ns |
| Capacitive Sense Oscillator Resistance | $R_{CSRESSEL}$ | CSRESSEL = 0 | — | 14 | — | kΩ |
| | | CSRESSEL = 1 | — | 24 | — | kΩ |
| | | CSRESSEL = 2 | — | 43 | — | kΩ |
| | | CSRESSEL = 3 | — | 60 | — | kΩ |
| | | CSRESSEL = 4 | — | 80 | — | kΩ |
| | | CSRESSEL = 5 | — | 99 | — | kΩ |
| | | CSRESSEL = 6 | — | 120 | — | kΩ |

**Note:**

1. When using the 1.25 V or 2.5 V VREF in continuous mode (VREFDIV1V25 or VREFDIV2V5) and BIAS < 4, an additional 1 µA of supply current is required.
2. $V_{CM}$ = 1.25 V

### 4.15 Digital to Analog Converter (VDAC)

**Table 4.34. Digital to Analog Converter (VDAC)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output voltage | $V_{DACOUT}$ | | 0 | — | VREF | V |
| Output Current | $I_{DACOUT}$ | | -10 | — | 10 | mA |
| DAC clock frequency | $f_{DAC}$ | | — | — | 1 | MHz |
| Sample rate | $SR_{DAC}$ | $f_{DAC} = f_{DAC(max)}$ | — | — | 500 | ksps |
| Resolution | $N_{RESOLUTION}$ | | — | 12 | — | bits |
| Load Capacitance[1] | $C_{LOAD}$ | High Power and Lower Power Modes | — | — | 50 | pF |
| | | High Capacitance Load Mode | 25 | — | — | nF |
| Load Resistance | $R_{LOAD}$ | | 5 | — | — | kΩ |
| Current consumption, Dynamic, 500 ksps, 1 channel active[2] | $I_{DAC_1_500}$ | High Power Mode | — | 255 | — | µA |
| | | Low Power Mode | — | 150 | — | µA |
| Current consumption, Dynamic, 500 ksps, 2 channels active[2] | $I_{DAC_2_500}$ | High Power Mode | — | 421 | — | µA |
| | | Low Power Mode | — | 216 | — | µA |
| Current consumption, Static, 1 channel active[3] | $I_{DAC_1_STAT}$ | High Power Mode | — | 136 | — | µA |
| | | Low Power Mode | — | 31 | — | µA |
| | | High Capacitance Mode | — | 44 | — | µA |
| Current consumption, Static, 2 channels active[3] | $I_{DAC_2_STAT}$ | High Power Mode | — | 263 | 400 | µA |
| | | Low Power Mode | — | 53 | 90 | µA |
| | | High Capacitance Mode | — | 78 | — | µA |
| Startup time | $t_{DACSTARTUP}$ | Enable to 90% full scale output, settling to 10 LSB | — | 4.5 | 4.9 | µs |
| Settling time | $t_{DACSETTLE}$ | High Power Mode, 25% to 75% of full scale, settling to 10 LSB | — | 1.1 | 1.6 | µs |
| | | Low Power Mode, 25% to 75% of full scale, settling to 1% | — | 2.7 | — | µs |
| Output impedance | $R_{OUT}$ | Main Output, High Power Mode | — | 2.3 | — | Ω |
| | | Main Output, Low Power Mode | — | 3.2 | — | Ω |
| Power supply rejection ratio[4] | PSRR | Vout = 50% full scale, DC output | — | 72 | — | dB |
| Signal to noise and distortion ratio | $SNDR_{DAC}$ | High Power mode, 500 ksps, internal 2.5 V reference, 1 kHz sine wave input, BW limited to 250 kHz | 61 | 64.8 | — | dB |
| | | High Power mode, 500 ksps, internal 2.5 V reference, 1 kHz sine wave input, BW limited to 22 kHz | 61.8 | 67.4 | — | dB |
| Total Harmonic Distortion | THD | High Power Mode, internal 2.5 V reference, 1 kHz sine wave input | — | -68.8 | -62.4 | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Integral Non-Linearity | $INL_{DAC}$ | High Power Mode, Across full temperature range | -6 | — | 6 | LSB |
| Differential Non-Linearity[5] | $DNL_{DAC}$ | High Power Mode, Across full temperature range | -1 | — | 1.3 | LSB |
| Offset error[6] | $V_{OFFSET}$ | High Power mode | -15 | — | 15 | mV |
| | | Low Power Mode | -25 | — | 25 | mV |
| | | High Capacitance Load mode | -35 | — | 35 | mV |
| Gain error[6] | $V_{GAIN}$ | 1.25 V internal reference | -1.5 | — | 1.5 | % |
| | | 2.5 V internal reference | -2 | — | 2 | % |
| | | External Reference | -0.6 | — | 0.6 | % |
| External Reference Voltage[7] | $V_{EXTREF}$ | | 1.1 | — | V_AVDD | V |

**Note:**

1. Main outputs only.
2. Dynamic current specifications are for VDAC circuitry operating at max clock frequency with the output updated at the specified sampling rate using DMA transfers. Output is a 1 kHz sine wave from 10% to 90% full scale. Specified current does not include current required to drive the external load. Measurement includes all current from AVDD and DVDD supplies.
3. Static current specifications are for VDAC circuitry operating after a one-time update to a static output at 50% full scale, with the VDAC APB clock disabled. Specified current does not include current required to drive the external load. Measurement includes all current from AVDD and DVDD supplies.
4. PSRR calculated as 20 * $\log_{10}(\Delta VDD / \Delta V_{OUT})$.
5. Entire range is monotonic and has no missing codes.
6. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain.
7. External reference voltage on VREFP pin or PA00 when used for VREFP

### 4.16 LCD

**Table 4.35. LCD**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| LCD Temperature Range | $T_{RANGE}$ | | -40 | — | 105 | °C |
| Frame rate | $f_{LCDFR}$ | | 30 | — | 100 | Hz |
| LCD supply range[1] [2] | $V_{LCDIN}$ | | 1.71 | — | 3.8 | V |
| LCD output voltage range[2] | $V_{LCD}$ | Step-down mode with external LCD capacitor | 2.4 | — | MIN(3.6, $V_{LCDIN}$ - 0.1) | V |
| | | Charge pump mode with external LCD capacitor | 2.4 | — | MIN(3.6, 1.9 * $V_{LCDIN}$) | V |
| Contrast control step size | $STEP_{CONTRAST}$ | Charge pump or Step-down mode | — | 50 | — | mV |
| Contrast control step accuracy[3] | $ACC_{CONTRAST}$ | | — | +/-1.5 | — | % |

**Note:**

1. $V_{LCDIN}$ is selectable between the AVDD or DVDD supply pins, depending on EMU_PWRCTRL_ANASW.
2. $V_{LCDIN}$ and $V_{LCD}$ should be a maximum of 2 V above $V_{IOVDD}$to avoid additional leakage through the GPIO pins used for LCD functions.
3. Step size accuracy is measured relative to the typical step size, and typ value represents one standard deviation.

## 4.17 Temperature Sensor

**Table 4.36. Temperature Sensor**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Temperature sensor range[1] | $T_{RANGE}$ | | -40 | — | 125 | °C |
| Temperature sensor resolution | $T_{RESOLUTION}$ | | — | 0.25 | — | °C |
| Measurement noise (RMS) | $T_{NOISE}$ | Single measurement | — | 0.6 | — | °C |
| | | 16-sample average (TEMPAVGNUM = 0) | — | 0.17 | — | °C |
| | | 64-sample average (TEMPAVGNUM = 1) | — | 0.12 | — | °C |
| Temperature offset | $T_{OFF}$ | Mean error of uncorrected output across full temperature range | — | 3.7 | — | °C |
| Temperature sensor accuracy[2] [3] | $T_{ACC}$ | Direct output accuracy after mean error ($T_{OFF}$) removed | — | +/-3 | — | °C |
| | | After linearization in software, no calibration | — | +/-2 | — | °C |
| | | After linearization in software, with single-temperature calibration at 25 °C[4] | — | +/-1.5 | — | °C |
| Measurement interval | $t_{MEAS}$ | | — | 250 | — | ms |

**Note:**

1. The sensor reports absolute die temperature in Kelvin (K). All specifications are in °C to match the units of the specified product temperature range.
2. Error is measured as the deviation of the mean temperature reading from the expected die temperature. Accuracy numbers represent statistical minimum and maximum using ± 4 standard deviations of measured error.
3. The raw output of the temperature sensor is a predictable curve. It can be linearized with a polynomial function for additional accuracy.
4. Assuming calibration accuracy of ± 0.25 °C.

## 4.18 Brown Out Detectors

### 4.18.1 DVDD BOD

BOD thresholds on DVDD in EM0 and EM1 only, unless otherwise noted. Typical conditions are at $T_A$ = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

**Table 4.37. DVDD BOD**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| BOD threshold | $V_{DVDD_BOD}$ | Supply Rising | — | 1.67 | 1.71 | V |
| | | Supply Falling | 1.62 | 1.65 | — | V |
| BOD response time | $t_{DVDD_BOD_DELAY}$ | Supply dropping at 100 mV/µs slew rate[1] | — | 0.95 | — | µs |
| BOD hysteresis | $V_{DVDD_BOD_HYST}$ | | — | 22 | — | mV |

**Note:**
1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

### 4.18.2 LE DVDD BOD

BOD thresholds on DVDD pin for low energy modes EM2 to EM4, unless otherwise noted.

**Table 4.38. LE DVDD BOD**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| BOD threshold | $V_{DVDD_LE_BOD}$ | Supply Falling | 1.5 | — | 1.71 | V |
| BOD response time | $t_{DVDD_LE_BOD_DELAY}$ | Supply dropping at 2 mV/µs slew rate[1] | — | 50 | — | µs |
| BOD hysteresis | $V_{DVDD_LE_BOD_HYST}$ | | — | 20 | — | mV |

**Note:**
1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

### 4.18.3 AVDD and IOVDD BODs

BOD thresholds for AVDD BOD and IOVDD BOD. Available in all energy modes.

**Table 4.39. AVDD and IOVDD BODs**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| BOD threshold | $V_{BOD}$ | Supply falling | 1.45 | — | 1.71 | V |
| BOD response time | $t_{BOD_DELAY}$ | Supply dropping at 2 mV/µs slew rate[1] | — | 50 | — | µs |
| BOD hysteresis | $V_{BOD_HYST}$ | | — | 20 | — | mV |

**Note:**
1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

## 4.19 Pulse Counter

**Table 4.40. Pulse Counter**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input frequency | $F_{IN}$ | Asynchronous Single and Quadrature Modes | — | — | 1.0 | MHz |
| | | Sampled Modes with Debounce filter set to 0. | — | — | 8 | kHz |
| Setup time in asynchronous external clock mode | $t_{SU_S1N_S0N}$ | S1N (data) to S0N (clock) | 50 | — | — | ns |
| Hold time in asynchronous external clock mode | $t_{HD_S0N_S1N}$ | S0N (clock) to S1N (data) | 50 | — | — | ns |

### 4.20 USART SPI Main Timing

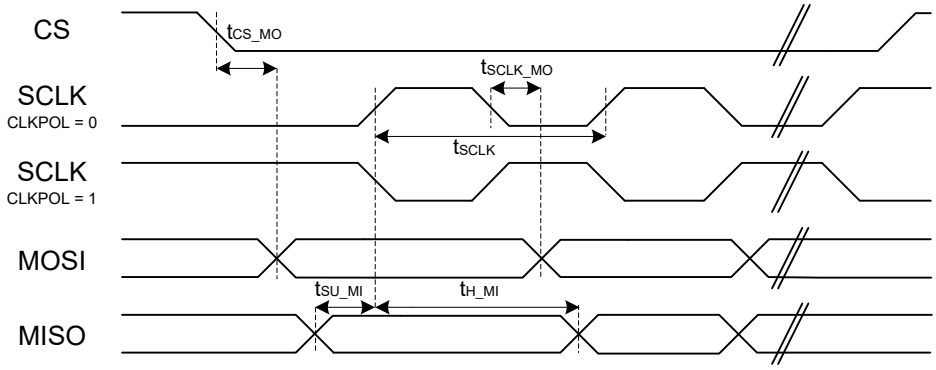


**Figure 4.1. SPI Main Timing (SMSDELAY = 0)**

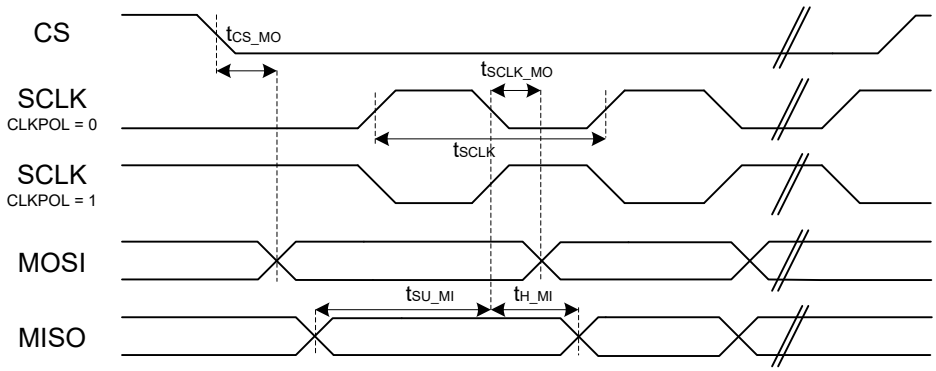


**Figure 4.2. SPI Main Timing (SMSDELAY = 1)**

### 4.20.1 USART SPI Main Timing, Voltage Scaling = VSCALE2

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

**Table 4.41. USART SPI Main Timing, Voltage Scaling = VSCALE2**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCLK period[1 2 3] | $t_{SCLK}$ | | 2 * $t_{PCLK}$ | — | — | ns |
| CS to MOSI[1 2] | $t_{CS_MO}$ | | -17 | — | 22 | ns |
| SCLK to MOSI[1 2] | $t_{SCLK_MO}$ | | -12 | — | 12 | ns |
| MISO setup time[1 2] | $t_{SU_MI}$ | IOVDD = 1.62 V | 39 | — | — | ns |
| | | IOVDD = 3.3 V | 28 | — | — | ns |
| MISO hold time[1 2] | $t_{H_MI}$ | | -10 | — | — | ns |

**Note:**
1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply.
3. $t_{PCLK}$ is one period of the selected PCLK.

### 4.20.2 USART SPI Main Timing, Voltage Scaling = VSCALE1

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

**Table 4.42. USART SPI Main Timing, Voltage Scaling = VSCALE1**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCLK period[1 2 3] | $t_{SCLK}$ | | 2 * $t_{PCLK}$ | — | — | ns |
| CS to MOSI[1 2] | $t_{CS_MO}$ | | -24 | — | 32 | ns |
| SCLK to MOSI[1 2] | $t_{SCLK_MO}$ | | -12 | — | 20 | ns |
| MISO setup time[1 2] | $t_{SU_MI}$ | IOVDD = 1.62 V | 47 | — | — | ns |
| | | IOVDD = 3.3 V | 39 | — | — | ns |
| MISO hold time[1 2] | $t_{H_MI}$ | | -11 | — | — | ns |

**Note:**
1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply.
3. $t_{PCLK}$ is one period of the selected PCLK.

### 4.21 USART SPI Secondary Timing

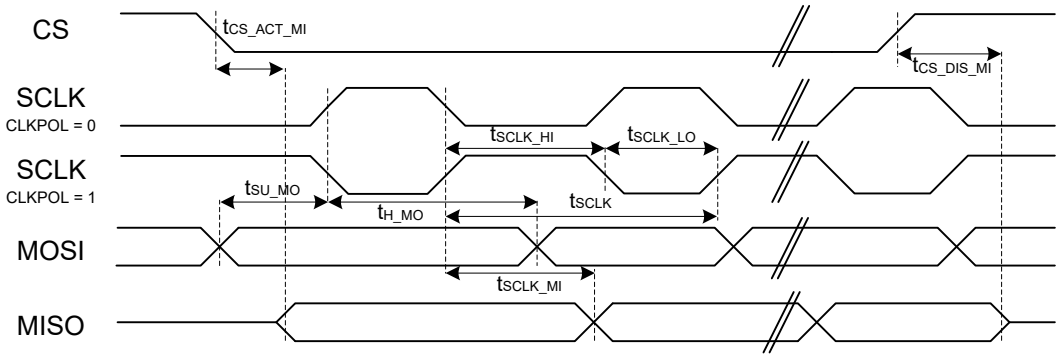


**Figure 4.3. SPI Secondary Timing (SSSEARLY = 0)**

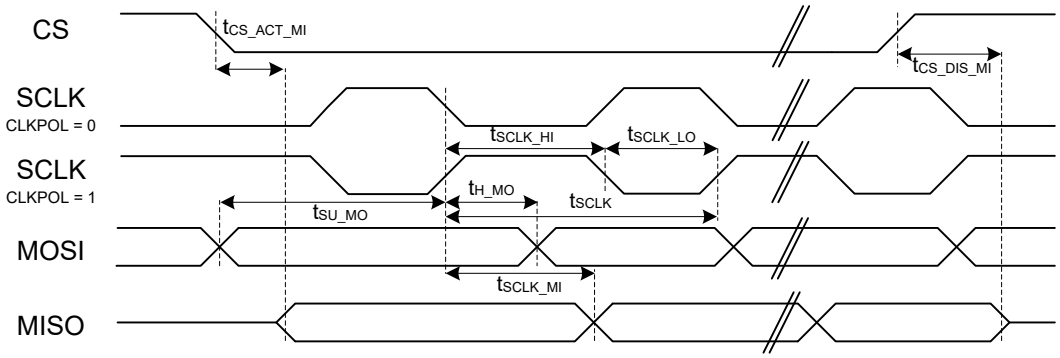


**Figure 4.4. SPI Secondary Timing (SSSEARLY = 1)**

### 4.21.1 USART SPI Secondary Timing, Voltage Scaling = VSCALE2

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

**Table 4.43. USART SPI Secondary Timing, Voltage Scaling = VSCALE2**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCLK period[1 2 3] | $t_{SCLK}$ | | 6 * $t_{PCLK}$ | — | — | ns |
| SCLK high time[1 2 3] | $t_{SCLK_HI}$ | | 2.5 * $t_{PCLK}$ | — | — | ns |
| SCLK low time[1 2 3] | $t_{SCLK_LO}$ | | 2.5 * $t_{PCLK}$ | — | — | ns |
| CS active to MISO[1 2] | $t_{CS_ACT_MI}$ | | 18 | — | 75 | ns |
| CS disable to MISO[1 2] | $t_{CS_DIS_MI}$ | | 16 | — | 66 | ns |
| MOSI setup time[1 2] | $t_{SU_MO}$ | | 6 | — | — | ns |
| MOSI hold time[1 2 3] | $t_{H_MO}$ | | 5 | — | — | ns |
| SCLK to MISO[1 2 3] | $t_{SCLK_MI}$ | | 14 + 1.5 * $t_{PCLK}$ | — | 29 + 2.5 * $t_{PCLK}$ | ns |

**Note:**
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply (figure shows 50%).
3. $t_{PCLK}$ is one period of the selected PCLK.

### 4.21.2 USART SPI Secondary Timing, Voltage Scaling = VSCALE1

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

**Table 4.44. USART SPI Secondary Timing, Voltage Scaling = VSCALE1**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCLK period[1 2 3] | $t_{SCLK}$ | | 6*$t_{PCLK}$ | — | — | ns |
| SCLK high time[1 2 3] | $t_{SCLK_HI}$ | | 2.5 * $t_{PCLK}$ | — | — | ns |
| SCLK low time[1 2 3] | $t_{SCLK_LO}$ | | 2.5 * $t_{PCLK}$ | — | — | ns |
| CS active to MISO[1 2] | $t_{CS_ACT_MI}$ | | 23 | — | 102 | ns |
| CS disable to MISO[1 2] | $t_{CS_DIS_MI}$ | | 22 | — | 93 | ns |
| MOSI setup time[1 2] | $t_{SU_MO}$ | | 9 | — | — | ns |
| MOSI hold time[1 2 3] | $t_{H_MO}$ | | 9 | — | — | ns |
| SCLK to MISO[1 2 3] | $t_{SCLK_MI}$ | | 18 + 1.5 * $t_{PCLK}$ | — | 36 + 2.5 * $t_{PCLK}$ | ns |

**Note:**
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply (figure shows 50%).
3. $t_{PCLK}$ is one period of the selected PCLK.

## 4.22 EUSART SPI Main Timing

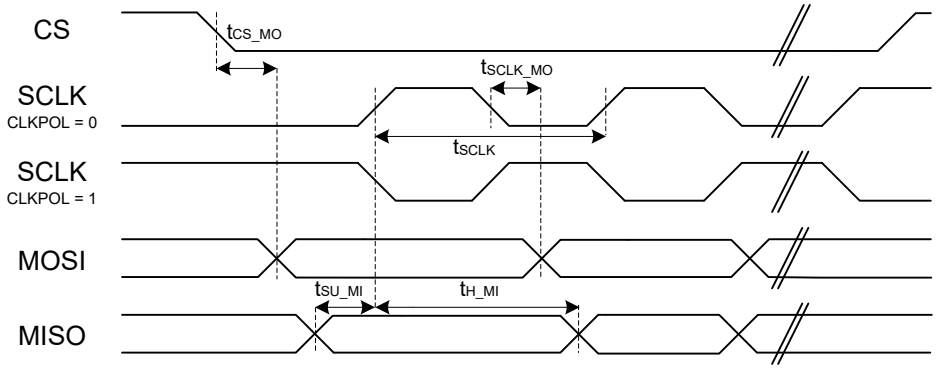


**Figure 4.5. SPI Main Timing**

### 4.22.1 EUSART SPI Main Timing, Voltage Scaling = VSCALE2

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

**Table 4.45. EUSART SPI Main Timing, Voltage Scaling = VSCALE2**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCLK period[1 2 3] | $t_{SCLK}$ | | $t_{CLK}$ | — | — | ns |
| CS to MOSI[1 2] | $t_{CS_MO}$ | | -10 | — | 8 | ns |
| SCLK to MOSI[1 2] | $t_{SCLK_MO}$ | | -3 | — | 8 | ns |
| MISO setup time[1 2] | $t_{SU_MI}$ | | 7 | — | — | ns |
| MISO hold time[1 2] | $t_{H_MI}$ | | 3 | — | — | ns |

**Note:**

1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 15 pF output loading at 10% and 90% of $V_{DD}$.
3. $t_{CLK}$ is one period of the selected peripheral clock: EM01GRPCCLK for EUSART1/2, EUSART0CLK for EUSART0.

### 4.22.2 EUSART SPI Main Timing, Voltage Scaling = VSCALE1

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

**Table 4.46. EUSART SPI Main Timing, Voltage Scaling = VSCALE1**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCLK period[1 2 3] | $t_{SCLK}$ | | $t_{CLK}$ | — | — | ns |
| CS to MOSI[1 2] | $t_{CS_MO}$ | | -18 | — | 15 | ns |
| SCLK to MOSI[1 2] | $t_{SCLK_MO}$ | | -4 | — | 13 | ns |
| MISO setup time[1 2] | $t_{SU_MI}$ | | 12 | — | — | ns |
| MISO hold time[1 2] | $t_{H_MI}$ | | 3 | — | — | ns |

**Note:**

1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 15 pF output loading at 10% and 90% of $V_{DD}$.
3. $t_{CLK}$ is one period of the selected peripheral clock: EM01GRPCCLK for EUSART1/2, EUSART0CLK for EUSART0.

## 4.23 EUSART SPI Secondary Timing

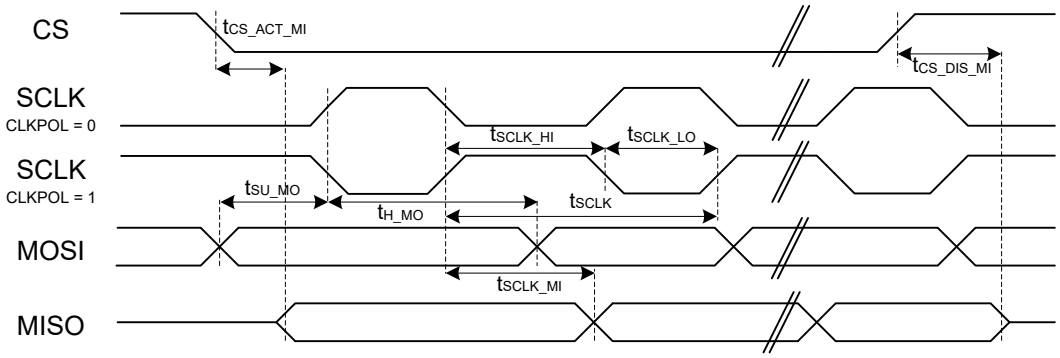


**Figure 4.6. SPI Secondary Timing**

### 4.23.1 EUSART SPI Secondary Timing, Voltage Scaling = VSCALE2

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

**Table 4.47. EUSART SPI Secondary Timing, Voltage Scaling = VSCALE2**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCLK high time[1] [2] | $t_{SCLK_HI}$ | | 50 | — | — | ns |
| SCLK low time[1] [2] | $t_{SCLK_LO}$ | | 50 | — | — | ns |
| CS active to MISO[1] [2] | $t_{CS_ACT_MI}$ | | 5 | — | 50 | ns |
| CS disable to MISO[1] [2] | $t_{CS_DIS_MI}$ | | 7 | — | 40 | ns |
| MOSI setup time[1] [2] | $t_{SU_MO}$ | | 5 | — | — | ns |
| MOSI hold time[1] [2] | $t_{H_MO}$ | | 6 | — | — | ns |
| SCLK to MISO[1] [2] | $t_{SCLK_MI}$ | IOVDD = 1.8 V | 9 | — | 40 | ns |
| | | IOVDD = 3.3 V | 9 | — | 30 | ns |

**Note:**
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 15 pF output loading at 10% and 90% of $V_{DD}$ (figure shows 50% of $V_{DD}$).

### 4.23.2 EUSART SPI Secondary Timing, Voltage Scaling = VSCALE1

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

**Table 4.48. EUSART SPI Secondary Timing, Voltage Scaling = VSCALE1**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCLK high time[1] [2] | $t_{SCLK_HI}$ | | 50 | — | — | ns |
| SCLK low time[1] [2] | $t_{SCLK_LO}$ | | 50 | — | — | ns |
| CS active to MISO[1] [2] | $t_{CS_ACT_MI}$ | | 6 | — | 75 | ns |
| CS disable to MISO[1] [2] | $t_{CS_DIS_MI}$ | | 6 | — | 60 | ns |
| MOSI setup time[1] [2] | $t_{SU_MO}$ | | 8 | — | — | ns |
| MOSI hold time[1] [2] | $t_{H_MO}$ | | 11 | — | — | ns |
| SCLK to MISO[1] [2] | $t_{SCLK_MI}$ | IOVDD = 1.8 V | 10 | — | 50 | ns |
| | | IOVDD = 3.3 V | 10 | — | 42 | ns |

**Note:**
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 15 pF output loading at 10% and 90% of $V_{DD}$ (figure shows 50% of $V_{DD}$).

### 4.23.3 EUSART SPI Secondary Timing, Voltage Scaling = VSCALE0

Timing specifications at VSCALE0 apply to EUSART0 only, routed to DBUSAB on consecutive pins. All GPIO set to slew rate = 6.

**Table 4.49. EUSART SPI Secondary Timing, Voltage Scaling = VSCALE0**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCLK high time[1] [2] | $t_{SCLK_HI}$ | | 100 | — | — | ns |
| SCLK low time[1] [2] | $t_{SCLK_LO}$ | | 100 | — | — | ns |
| CS active to MISO[1] [2] | $t_{CS_ACT_MI}$ | | 8 | — | 112 | ns |
| CS disable to MISO[1] [2] | $t_{CS_DIS_MI}$ | | 8 | — | 82 | ns |
| MOSI setup time[1] [2] | $t_{SU_MO}$ | | 12 | — | — | ns |
| MOSI hold time[1] [2] | $t_{H_MO}$ | | 32 | — | — | ns |
| SCLK to MISO[1] [2] | $t_{SCLK_MI}$ | IOVDD = 1.8 V | 12 | — | 92 | ns |
| | | IOVDD = 3.3 V | 12 | — | 82 | ns |

**Note:**
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 15 pF output loading at 10% and 90% of $V_{DD}$ (figure shows 50% of $V_{DD}$).

## 4.24 I2C Electrical Specifications

### 4.24.1 I2C Standard-mode (Sm)

CLHR set to 0 in the I2Cn_CTRL register.

**Table 4.50. I2C Standard-mode (Sm)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCL clock frequency[1] | $f_{SCL}$ | | 0 | — | 100 | kHz |
| SCL clock low time | $t_{LOW}$ | | 4.7 | — | — | µs |
| SCL clock high time | $t_{HIGH}$ | | 4 | — | — | µs |
| SDA set-up time | $t_{SU_DAT}$ | | 250 | — | — | ns |
| SDA hold time | $t_{HD_DAT}$ | | 0 | — | — | ns |
| Repeated START condition set-up time | $t_{SU_STA}$ | | 4.7 | — | — | µs |
| Repeated START condition hold time | $t_{HD_STA}$ | | 4.0 | — | — | µs |
| STOP condition set-up time | $t_{SU_STO}$ | | 4.0 | — | — | µs |
| Bus free time between a STOP and START condition | $t_{BUF}$ | | 4.7 | — | — | µs |

**Note:**

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

### 4.24.2 I2C Fast-mode (Fm)

CLHR set to 1 in the I2Cn_CTRL register.

**Table 4.51. I2C Fast-mode (Fm)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCL clock frequency[1] | $f_{SCL}$ | | 0 | — | 400 | kHz |
| SCL clock low time | $t_{LOW}$ | | 1.3 | — | — | µs |
| SCL clock high time | $t_{HIGH}$ | | 0.6 | — | — | µs |
| SDA set-up time | $t_{SU_DAT}$ | | 100 | — | — | ns |
| SDA hold time | $t_{HD_DAT}$ | | 0 | — | — | ns |
| Repeated START condition set-up time | $t_{SU_STA}$ | | 0.6 | — | — | µs |
| Repeated START condition hold time | $t_{HD_STA}$ | | 0.6 | — | — | µs |
| STOP condition set-up time | $t_{SU_STO}$ | | 0.6 | — | — | µs |
| Bus free time between a STOP and START condition | $t_{BUF}$ | | 1.3 | — | — | µs |

**Note:**

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

### 4.24.3 I2C Fast-mode Plus (Fm+)

CLHR set to 1 in the I2Cn_CTRL register.

**Table 4.52. I2C Fast-mode Plus (Fm+)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCL clock frequency[1] | $f_{SCL}$ | | 0 | — | 1000 | kHz |
| SCL clock low time | $t_{LOW}$ | | 0.5 | — | — | µs |
| SCL clock high time | $t_{HIGH}$ | | 0.26 | — | — | µs |
| SDA set-up time | $t_{SU_DAT}$ | | 50 | — | — | ns |
| SDA hold time | $t_{HD_DAT}$ | | 0 | — | — | ns |
| Repeated START condition set-up time | $t_{SU_STA}$ | | 0.26 | — | — | µs |
| Repeated START condition hold time | $t_{HD_STA}$ | | 0.26 | — | — | µs |
| STOP condition set-up time | $t_{SU_STO}$ | | 0.26 | — | — | µs |
| Bus free time between a STOP and START condition | $t_{BUF}$ | | 0.5 | — | — | µs |

**Note:**

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

## 4.25 Boot Timing

Secure boot impacts the recovery time from all sources of device reset. In addition to the root code authentication process, which cannot be disabled or bypassed, the root code can authenticate a bootloader, and the bootloader can authenticate the application. In projects that include only an application and no bootloader, the root code can authenticate the application directly. The duration of each authentication operation depends on two factors: the computation of the associated image hash, which is proportional to the size of the image, and the verification of the image signature, which is independent of image size.

The duration for the root code to authenticate the bootloader will depend on the SE firmware version as well as on the size of the bootloader.

The duration for the bootloader to authenticate the application can depend on the size of the application.

The configurations below assume that the associated bootloader and application code images do not contain a bootloader certificate or an application certificate. Authenticating a bootloader certificate or an application certificate will extend the boot time by an additional 6 to 7 ms.

The table below provides the durations from the termination of reset until the completion of the secure boot process (start of main() function in the application image) under various conditions.

Conditions:

- SE firmware version: 2.1.4
- Gecko Bootloader size: 10.4 kB

Timing is expected to be similar for subsequent SE firmware versions. Refer to SE firmware release notes for any significant changes.

**Table 4.53. Boot Timing**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Boot time | $t_{BOOT}$ | Secure boot application check disabled, no bootloader | — | 34.3 | — | ms |
| | | Secure boot application check disabled, second stage bootloader check enabled[1], 50 kB application size | — | 46.4 | — | ms |
| | | Secure boot application check enabled, second stage bootloader check enabled[1], 50 kB application size | — | 57.2 | — | ms |
| | | Secure boot application check enabled, second stage bootloader check enabled[1], 150 kB application size | — | 59.9 | — | ms |
| | | Secure boot application check enabled, second stage bootloader check enabled[1], 350 kB application size | — | 65.2 | — | ms |

**Note:**

1. Timing is measured with the specified bootloader size. Actual bootloader size will impact the boot timing slightly, with a similar µs / kB ratio as application size.

### 4.26 Crypto Operation Timing for SE Manager API

Values in this table represent timing from SE Manager API call to return. The Cortex-M33 HCLK frequency is 39.0 MHz. The timing specifications below are measured at the SE Manager function call API. Each duration in the table contains some portion that is influenced by SE Manager build compilation and Cortex-M33 operating frequency and some portion that is influenced by the Hardware Secure Engine's firmware version and its operating speed (typically 80 MHz). The contributions of the Cortex-M33 properties to the overall specification timing are most pronounced for the shorter operations such as AES and hash when operating on small payloads. The overhead of command processing at the mailbox interface can also dominate the timing for shorter operations.

Conditions:

- SE firmware version: 2.1.4
- GSDK version: 3.2.2

Timing is expected to be similar for subsequent SE firmware versions. Refer to SE firmware release notes for any significant changes.

**Table 4.54. Crypto Operation Timing for SE Manager API**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| AES-128 timing | $t_{AES128}$ | AES-128 CCM encryption, PT 1 kB | — | 548 | — | µs |
| | | AES-128 CCM encryption, PT 32 kB | — | 1737 | — | µs |
| | | AES-128 CTR encryption, PT 1 kB | — | 439 | — | µs |
| | | AES-128 CTR encryption, PT 32 kB | — | 1006 | — | µs |
| | | AES-128 GCM encryption, PT 1 kB | — | 492 | — | µs |
| | | AES-128 GCM encryption, PT 32 kB | — | 1061 | — | µs |
| AES-256 timing | $t_{AES256}$ | AES-256 CCM encryption, PT 1 kB | — | 563 | — | µs |
| | | AES-256 CCM encryption, PT 32 kB | — | 2161 | — | µs |
| | | AES-256 CTR encryption, PT 1 kB | — | 446 | — | µs |
| | | AES-256 CTR encryption, PT 32 kB | — | 1220 | — | µs |
| | | AES-256 GCM encryption, PT 1 kB | — | 500 | — | µs |
| | | AES-256 GCM encryption, PT 32 kB | — | 1274 | — | µs |
| ECC P-256 timing | $t_{ECC_P256}$ | ECC key generation, P-256 | — | 5.5 | — | ms |
| | | ECC signing, P-256 | — | 5.9 | — | ms |
| | | ECC verification, P-256 | — | 6.1 | — | ms |
| ECC P-521 timing[1] | $t_{ECC_P521}$ | ECC key generation, P-521 | — | 30.3 | — | ms |
| | | ECC signing, P-521 | — | 31 | — | ms |
| | | ECC verification, P-521 | — | 36.1 | — | ms |
| ECC P-25519 timing[2] | $t_{ECC_P25519}$ | ECC key generation, P-25519 | — | 4.5 | — | ms |
| | | ECC signing, P-25519 | — | 8.9 | — | ms |
| | | ECC verification, P-25519 | — | 6.3 | — | ms |
| ECDH compute secret timing | $t_{ECDH}$ | ECDH compute secret, P-521[1] | — | 30.3 | — | ms |
| | | ECDH compute secret, P-25519[2] | — | 4.4 | — | ms |
| | | ECDH compute secret, P-256 | — | 5.7 | — | ms |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ECJPAKE client timing | $t_{ECJPAKE_C}$ | ECJPAKE client write round one | — | 21.5 | — | ms |
| | | ECJPAKE client read round one | — | 11.7 | — | ms |
| | | ECJPAKE client write round two | — | 15.2 | — | ms |
| | | ECJPAKE client read round two | — | 6.4 | — | ms |
| | | ECJPAKE client derive secret | — | 8.7 | — | ms |
| ECJPAKE server timing | $t_{ECJPAKE_S}$ | ECJPAKE server write round one | — | 21.5 | — | ms |
| | | ECJPAKE server read round one | — | 11.7 | — | ms |
| | | ECJPAKE server write round two | — | 15.2 | — | ms |
| | | ECJPAKE server read round two | — | 6.4 | — | ms |
| | | ECJPAKE server derive secret | — | 8.8 | — | ms |
| POLY-1305 timing[1] | $t_{POLY1305}$ | POLY-1305, PT 1 kB | — | 478 | — | µs |
| | | POLY-1305, PT 32 kB | — | 1140 | — | µs |
| SHA-256 timing | $t_{SHA256}$ | SHA-256, PT 1 kB | — | 263 | — | µs |
| | | SHA-256, PT 32 kB | — | 685 | — | µs |
| SHA-512 timing[1] | $t_{SHA512}$ | SHA-512, PT 1 kB | — | 260 | — | µs |
| | | SHA-512, PT 32 kB | — | 573 | — | µs |

**Note:**

1. Option is only available on OPNs with Secure Vault High feature set.
2. Option is not available on Secure Vault Mid devices with SE firmware earlier than v2.1.7.

### 4.27 Crypto Operation Average Current for SE Manager API

Values in this table represent current consumed by security core during the operation, and represent additions to the current consumed by the Cortex-M33 application CPU due to the Hardware Secure Engine CPU and its associated crypto accelerators. The current measurements below represent the average value of the current for the duration of the crypto operation. Instantaneous peak currents may be higher.

Conditions:

- SE firmware version: 2.1.4
- GSDK version: 3.2.2

Current consumption is expected to be similar for subsequent SE firmware versions. Refer to SE firmware release notes for any significant changes.

**Table 4.55. Crypto Operation Average Current for SE Manager API**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| AES-128 current | $I_{AES128}$ | AES-128 CCM encryption, PT 1 kB | — | 1.7 | — | mA |
| | | AES-128 CCM encryption, PT 32 kB | — | 4.7 | — | mA |
| | | AES-128 CTR encryption, PT 1 kB | — | 1.6 | — | mA |
| | | AES-128 CTR encryption, PT 32 kB | — | 4.6 | — | mA |
| | | AES-128 GCM encryption, PT 1 kB | — | 1.6 | — | mA |
| | | AES-128 GCM encryption, PT 32 kB | — | 4.6 | — | mA |
| AES-256 current | $I_{AES256}$ | AES-256 CCM encryption, PT 1 kB | — | 1.8 | — | mA |
| | | AES-256 CCM encryption, PT 32 kB | — | 4.8 | — | mA |
| | | AES-256 CTR encryption, PT 1 kB | — | 1.7 | — | mA |
| | | AES-256 CTR encryption, PT 32 kB | — | 4.7 | — | mA |
| | | AES-256 GCM encryption, PT 1 kB | — | 1.7 | — | mA |
| | | AES-256 GCM encryption, PT 32 kB | — | 4.7 | — | mA |
| ECC P-256 current | $I_{ECCP256}$ | ECC key generation, P-256 | — | 2.4 | — | mA |
| | | ECC signing, P-256 | — | 2.4 | — | mA |
| | | ECC verification, P-256 | — | 2.4 | — | mA |
| ECC P-521 current[1] | $I_{ECCP521}$ | ECC key generation, P-521 | — | 2.6 | — | mA |
| | | ECC signing, P-521 | — | 2.6 | — | mA |
| | | ECC verification, P-521 | — | 2.6 | — | mA |
| ECC P-25519 current[2] | $I_{ECCP25519}$ | ECC key generation, P-25519 | — | 2.4 | — | mA |
| | | ECC signing, P-25519 | — | 2.4 | — | mA |
| | | ECC verification, P-25519 | — | 2.4 | — | mA |
| ECDH compute secret current | $I_{ECDH}$ | ECDH compute secret, P-521[1] | — | 2.6 | — | mA |
| | | ECDH compute secret, P-25519[2] | — | 2.3 | — | mA |
| | | ECDH compute secret, P-256 | — | 2.4 | — | mA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ECJPAKE client current | $I_{ECJPAKE_C}$ | ECJPAKE client write round one | — | 2.5 | — | mA |
| | | ECJPAKE client read round one | — | 2.5 | — | mA |
| | | ECJPAKE client write round two | — | 2.5 | — | mA |
| | | ECJPAKE client read round two | — | 2.4 | — | mA |
| | | ECJPAKE client derive secret | — | 2.5 | — | mA |
| ECJPAKE server current | $I_{ECJPAKE_S}$ | ECJPAKE server write round one | — | 2.5 | — | mA |
| | | ECJPAKE server read round one | — | 2.5 | — | mA |
| | | ECJPAKE server write round two | — | 2.5 | — | mA |
| | | ECJPAKE server read round two | — | 2.4 | — | mA |
| | | ECJPAKE server derive secret | — | 2.5 | — | mA |
| POLY-1305 current[1] | $I_{POLY1305}$ | POLY-1305, PT 1 kB | — | 1.5 | — | mA |
| | | POLY-1305, PT 32 kB | — | 2.4 | — | mA |
| SHA-256 current | $I_{SHA256}$ | SHA-256, PT 1 kB | — | 1.5 | — | mA |
| | | SHA-256, PT 32 kB | — | 3.1 | — | mA |
| SHA-512 current[1] | $I_{SHA512}$ | SHA-512, PT 1 kB | — | 1.5 | — | mA |
| | | SHA-512, PT 32 kB | — | 2.7 | — | mA |

**Note:**
1. Option is only available on OPNs with Secure Vault High feature set.
2. Option is not available on Secure Vault Mid devices with SE firmware earlier than v2.1.7.

### 4.28 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

### 4.28.1 Supply Current

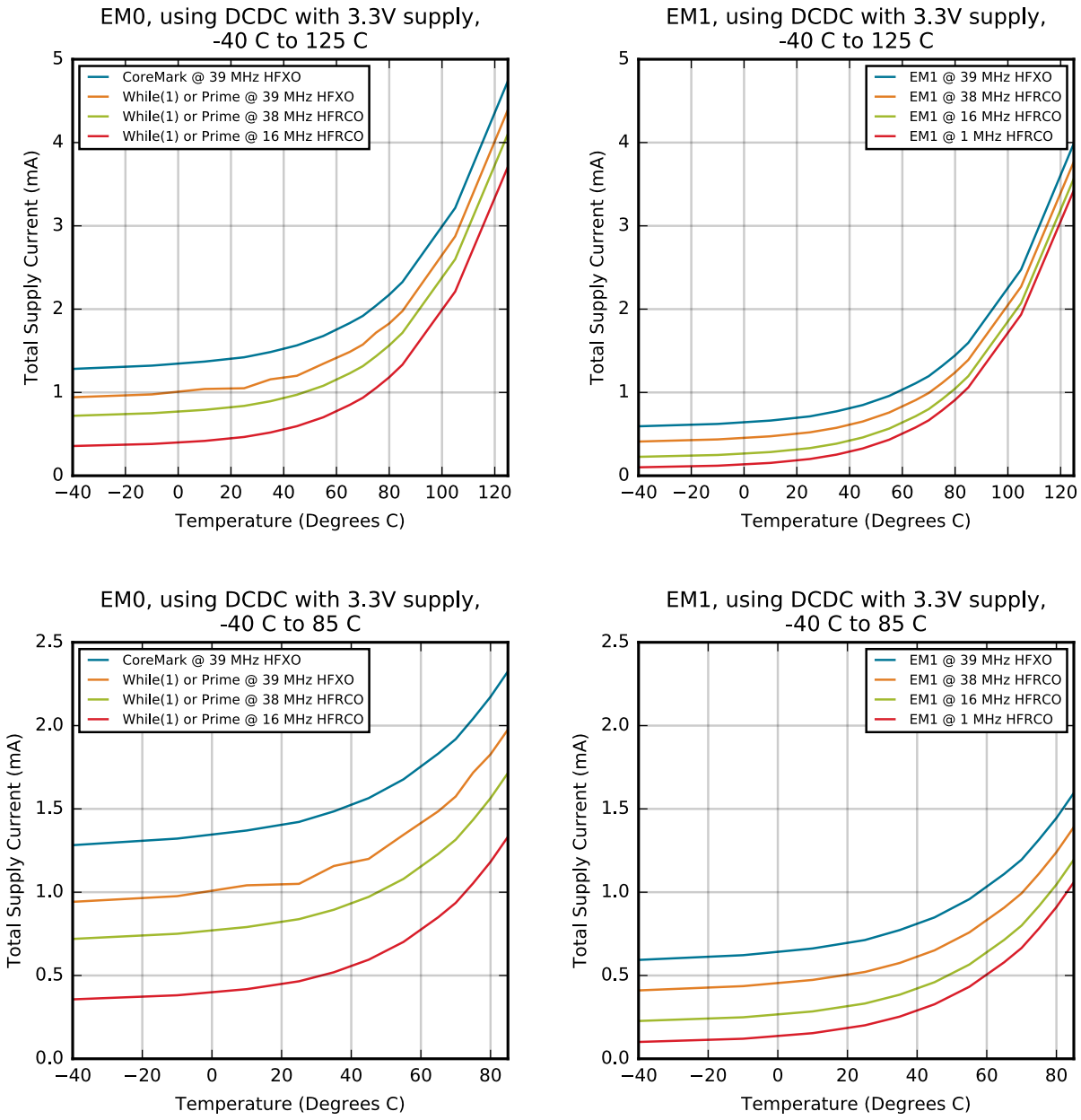


**Figure 4.7. EM0 and EM1 Typical Supply Current vs. Temperature**

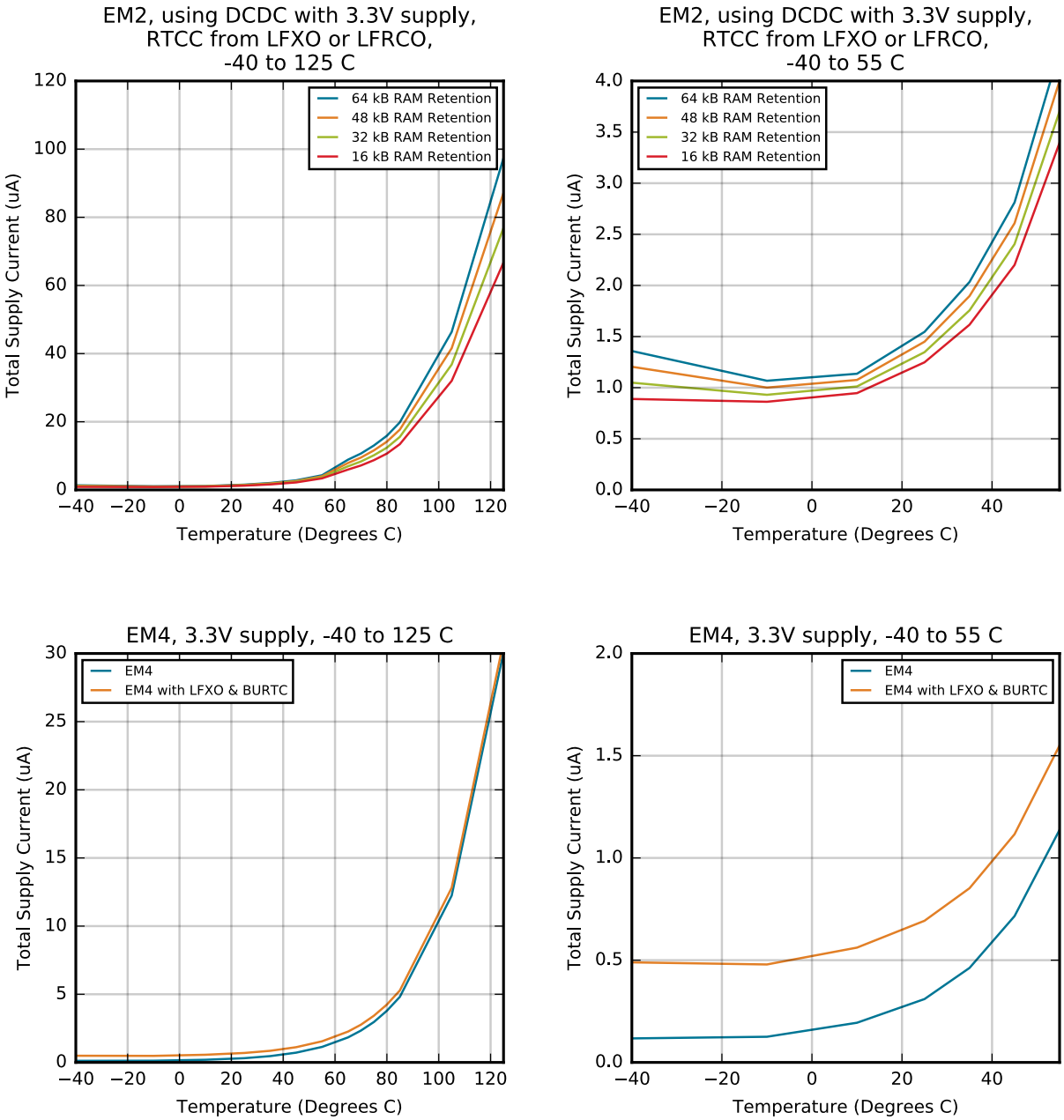


**Figure 4.8. EM2 and EM4 Typical Supply Current vs. Temperature**

### 4.28.2 RF Characteristics

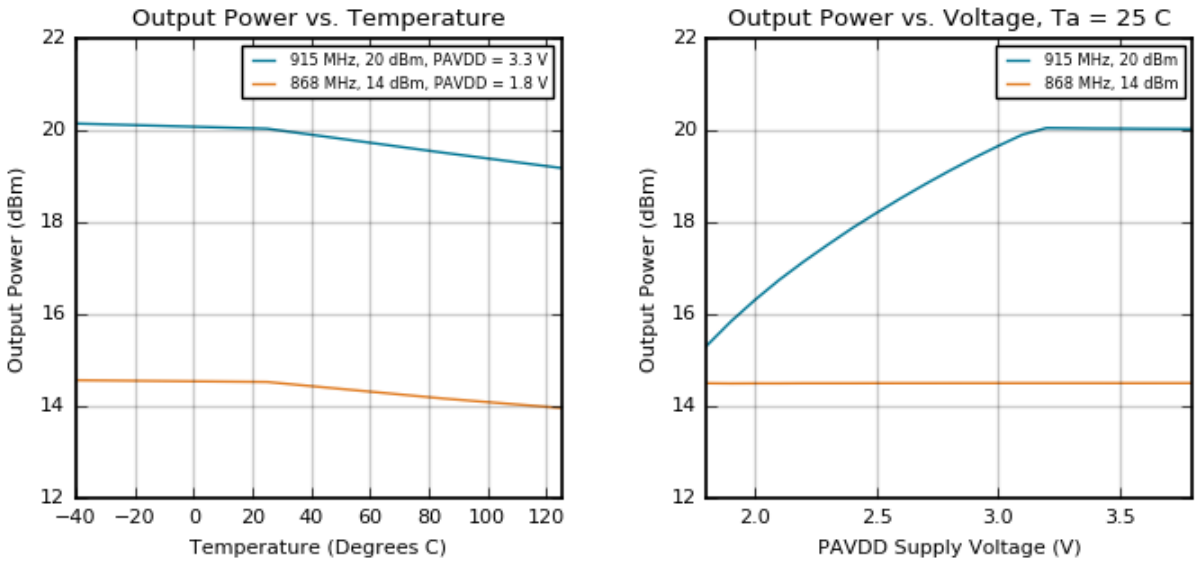


**Figure 4.9. Transmitter Output Power**

### 4.28.3 DC-DC Converter

Performance characterized with Samsung CIG22H2R2MNE ($L_{DCDC}$ = 2.2 uH ) and Samsung CL10B475KQ8NQNC ($C_{DCDC}$ = 4.7 uF)

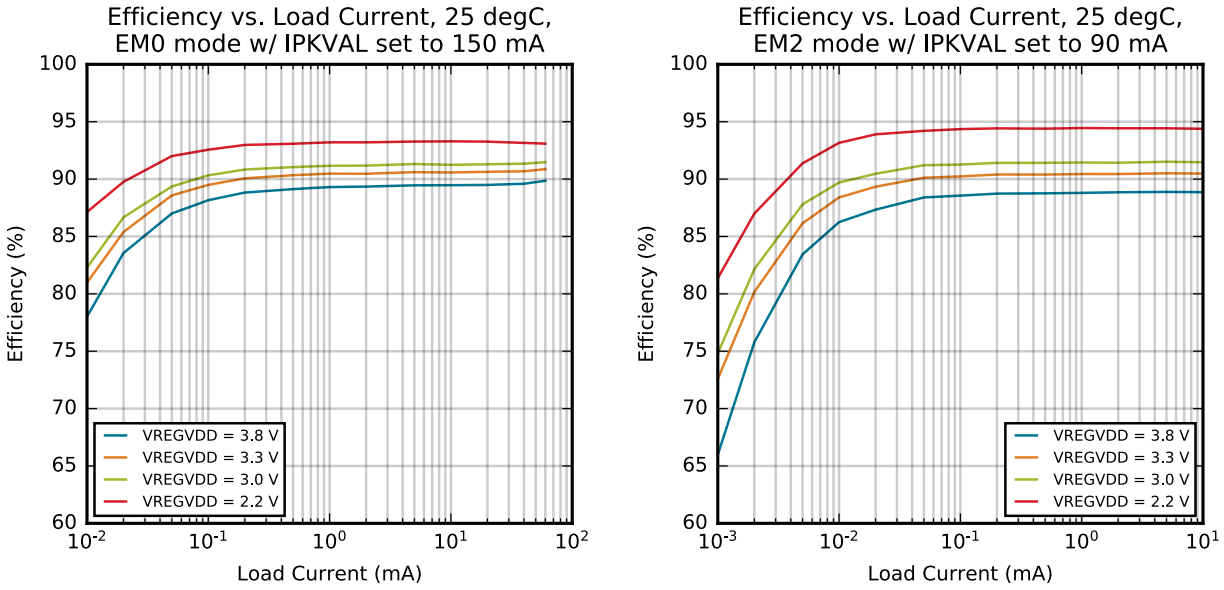


**Figure 4.10. DC-DC Efficiency**

### 4.28.4 IADC

Typical performance is shown using 10 MHz ADC clock for fastest sampling speed and adjusting oversampling ratio (OSR).

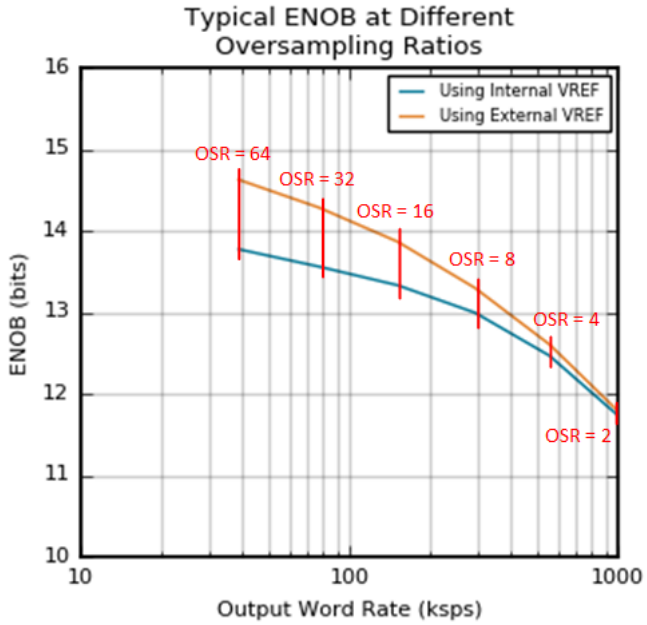


**Figure 4.11. Typical ENOB vs. Oversampling Ratio**

### 4.28.5 GPIO

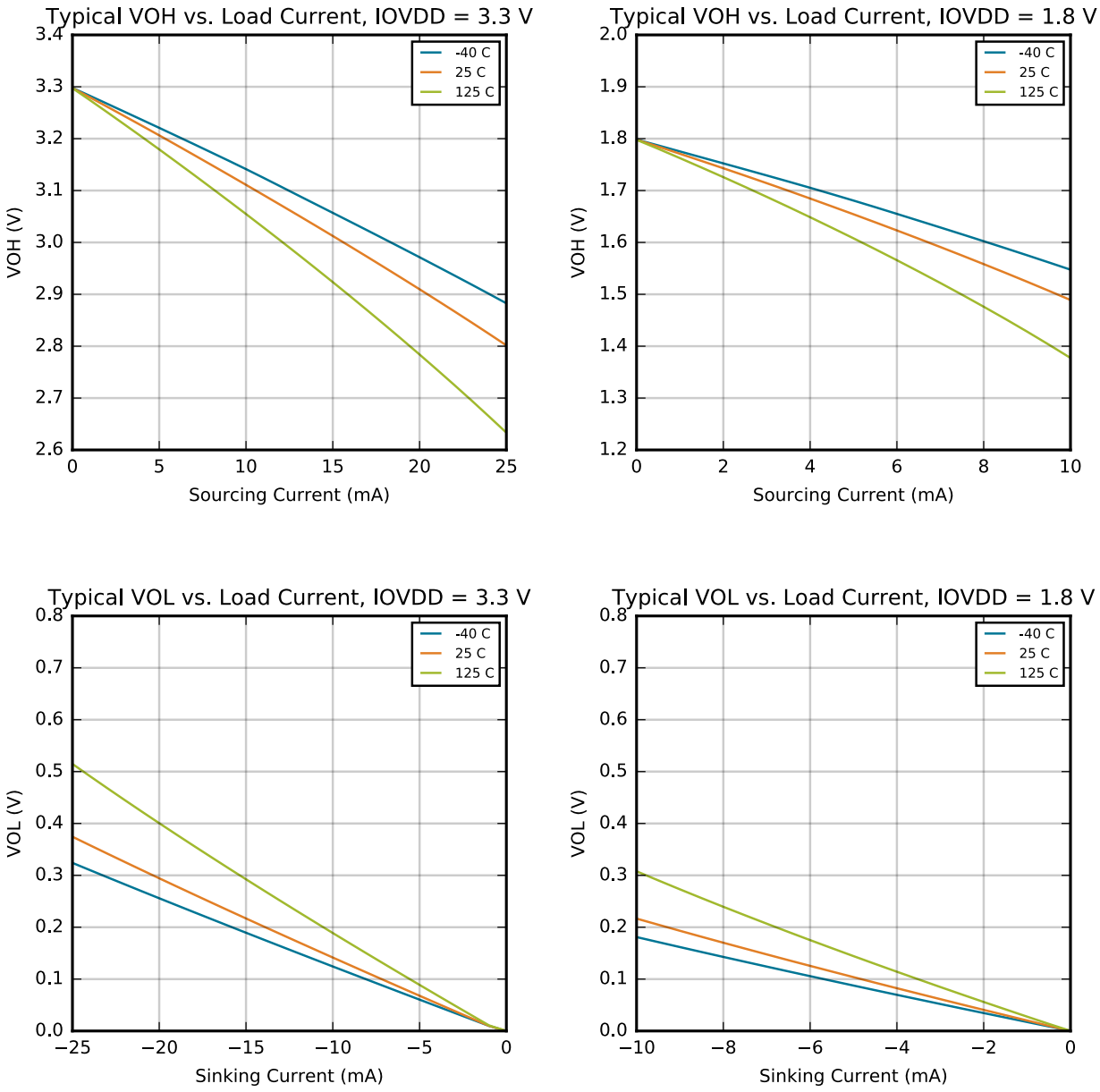


**Figure 4.12. VOH and VOL vs. Load Current**

# 5. Typical Connection Diagrams

## 5.1 Power

Typical power supply connections are shown in the following figures.

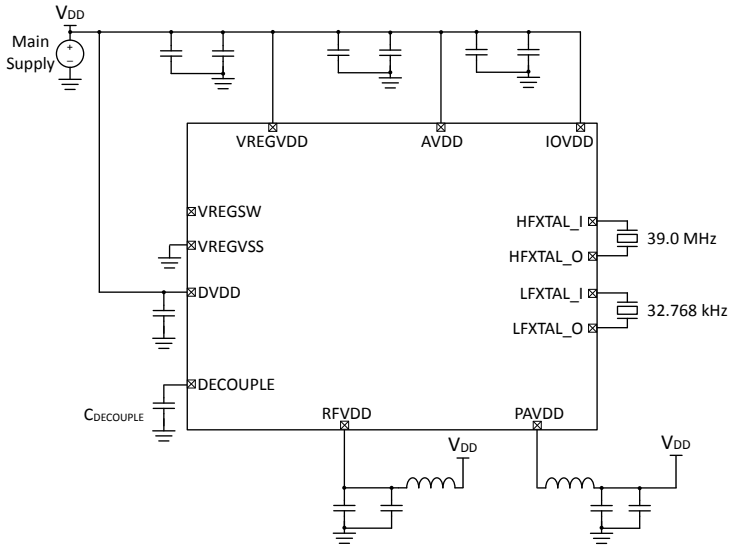


**Figure 5.1. EFR32ZG23 Typical Application Circuit: Direct Supply Configuration without DCDC**

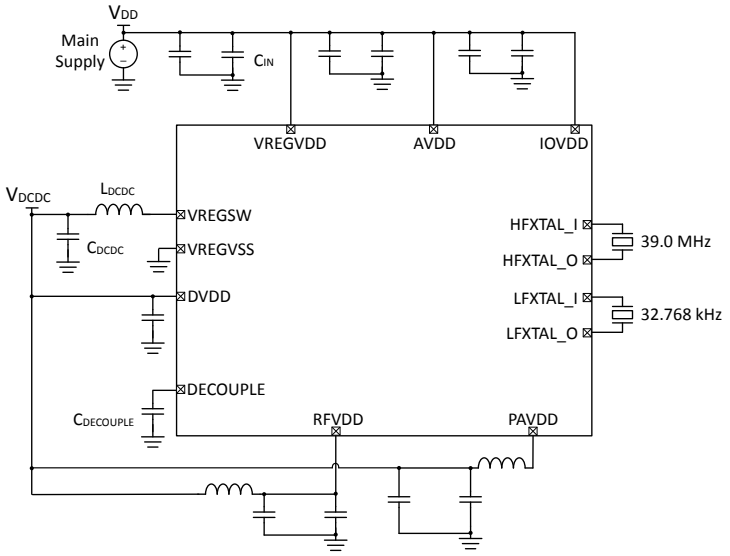


**Figure 5.2. EFR32ZG23 Typical Application Circuit: DCDC Configuration**

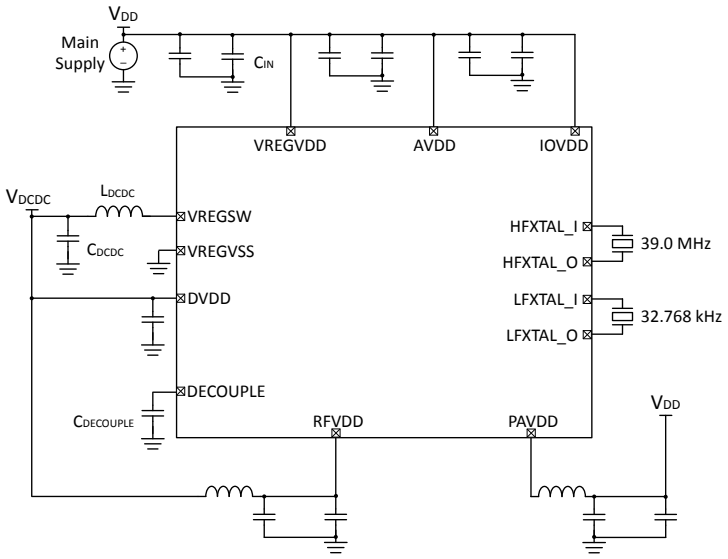


**Figure 5.3. EFR32ZG23 Typical Application Circuit: DCDC Configuration, PAVDD Powered Separately**

## 5.2 RF Matching Networks

### 5.2.1 Matching Networks for 868 MHz, 915 MHz, and 920 MHz Bands

The recommended RF matching network circuit diagram for the 868 MHz, 915 MHz, and 920 MHz bands at up to +14 dBm TX output power is shown in Figure 5.4 Typical 868/915/920 MHz RF impedance-matching network circuit, +14 dBm on page 103. This supports all frequencies from 868 to 930 MHz. Typical component values are shown in Table 5.1 868/915/920 MHz Component Values, +14 dBm on page 103. Please refer to the development board Bill of Materials for specific part recommendation including tolerance, component size, reccomended manufacturer, and recommended part number.

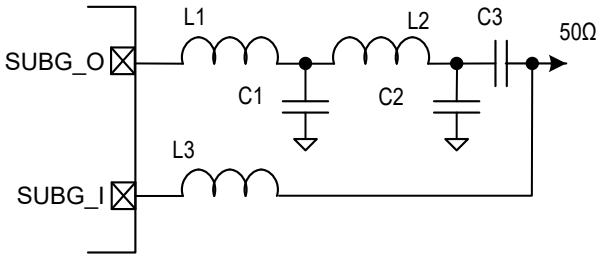


**Figure 5.4. Typical 868/915/920 MHz RF impedance-matching network circuit, +14 dBm**

**Table 5.1. 868/915/920 MHz Component Values, +14 dBm**

| Designator | Component Values |
|---|---|
| L1 | 4.2 nH |
| C1 | 5.9 pF |
| L2 | 16 nH |
| C2 | 2.1 pF |
| C3 | 220 pF |
| L3 | 18 nH |

The recommended RF matching network circuit diagram for the 868 MHz, 915 MHz, and 920 MHz bands at up to +20 dBm TX output power is shown in . This supports all frequencies from 868 to 930 MHz. Typical component values are shown in . Please refer to the development board Bill of Materials for specific part recommendation including tolerance, component size, reccomended manufacturer, and recommended part number.

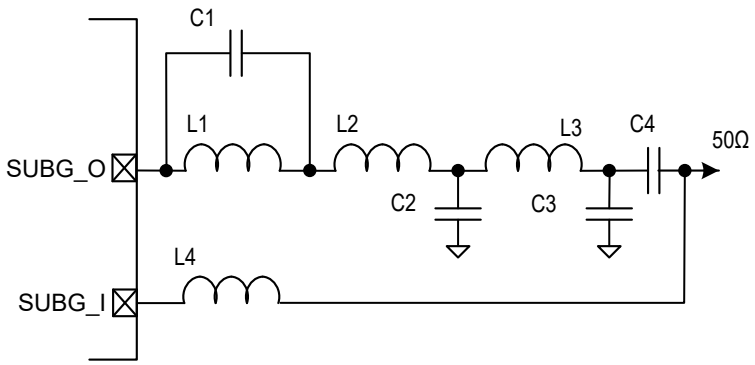


**Figure 5.5. Typical 868/915/920 MHz RF impedance-matching network circuit, +20 dBm**

**Table 5.2. 868/915/920 MHz Component Values, +20 dBm**

| Designator | Component Value |
|---|---|
| L1 | 1.5 nH |
| C1 | 1.9 pF |
| L2 | 1.3 nH |
| C2 | 7.2 pF |
| L3 | 13 nH |
| C3 | 1.3 pF |
| C4 | 220 pF |
| L4 | 18 nH |

### 5.2.2 Matching Network for 433 MHz Band

The recommended RF matching network circuit diagram for 433 MHz Band applications is shown in Figure 5.6 Typical 433 MHz Band RF impedance-matching network circuit on page 105. Typical component values optimizedfor different power levels are shown in Table 5.3 433 MHz Band Component Values on page 105. Please refer to the develoment board Bill of Materials for specific part recommendation including tolerance, component size, reccomended manufacturer, and reccomended part number.

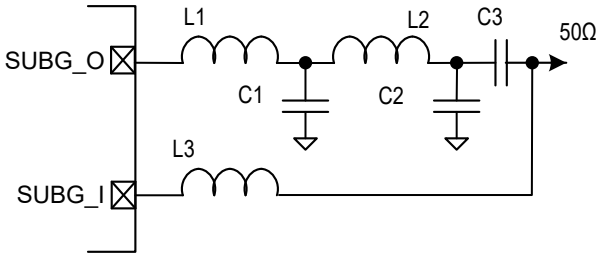


**Figure 5.6. Typical 433 MHz Band RF impedance-matching network circuit**

**Table 5.3. 433 MHz Band Component Values**

| Designator | Component Value |
|---|---|
| | +10 dBm |
| L1 | 20 nH |
| C1 | 8.5 pF |
| L2 | 39 nH |
| C2 | 4.6 pF |
| C3 | 220 pF |
| L3 | 82 nH |

## 5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN0002.2: "EFM32 and EFR32 Wireless Gecko Series 2 Hardware Design Considerations" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/32bit-appnotes).

# 6. Pin Definitions

## 6.1 QFN48 Device Pinout

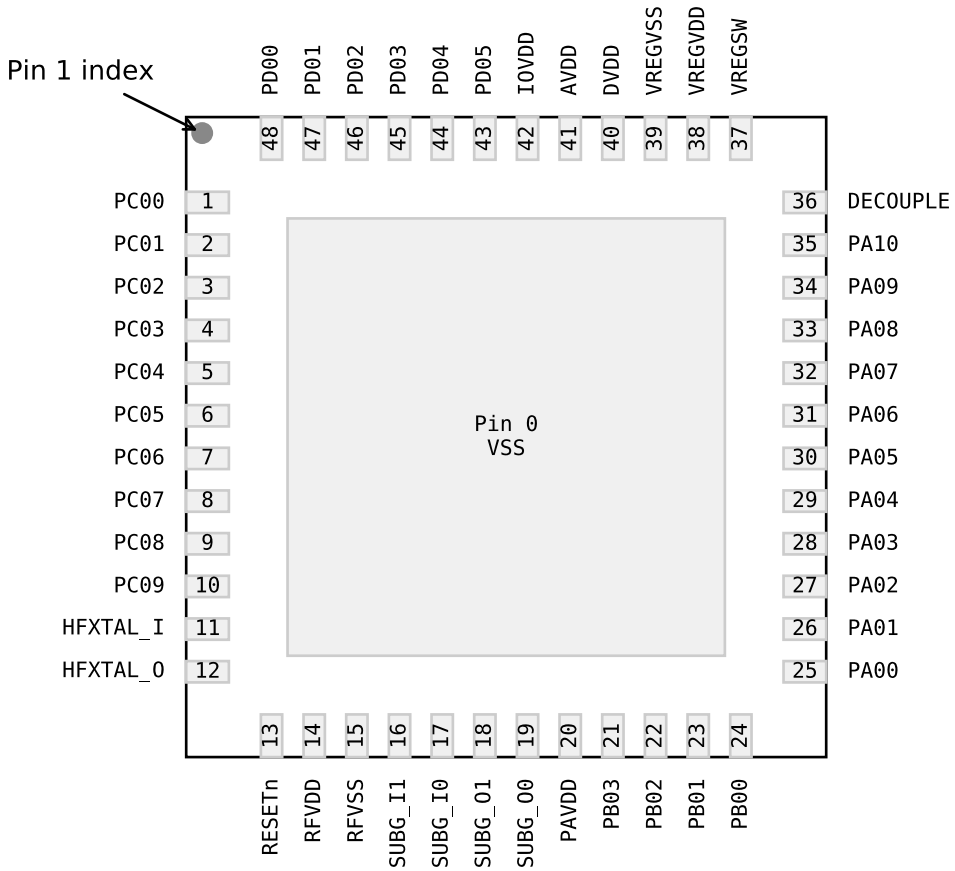


**Figure 6.1. QFN48 Device Pinout**

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.4 Alternate Function Table, 6.5 Analog Peripheral Connectivity, and 6.6 Digital Peripheral Connectivity.

Note that GPIO and Peripheral capabilities may differ by part number or be limited by the API or software stack.

**Table 6.1. QFN48 Device Pinout**

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| PC00 | 1 | GPIO | PC01 | 2 | GPIO |
| PC02 | 3 | GPIO | PC03 | 4 | GPIO |
| PC04 | 5 | GPIO | PC05 | 6 | GPIO |
| PC06 | 7 | GPIO | PC07 | 8 | GPIO |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| PC08 | 9 | GPIO | PC09 | 10 | GPIO |
| HFXTAL_I | 11 | High Frequency XTAL input pin | HFXTAL_O | 12 | High Frequency XTAL output pin |
| RESETn | 13 | Reset pin (active low) | RFVDD | 14 | RF VDD supply pin |
| RFVSS | 15 | RF VSS ground pin | SUBG_I1 | 16 | Sub-GHz Input 1 |
| SUBG_I0 | 17 | Sub-GHz Input 0 | SUBG_O1 | 18 | Sub-GHz Output 1 |
| SUBG_O0 | 19 | Sub-GHz Output 0 | PAVDD | 20 | PA VDD supply pin |
| PB03 | 21 | GPIO | PB02 | 22 | GPIO |
| PB01 | 23 | GPIO | PB00 | 24 | GPIO |
| PA00 | 25 | GPIO | PA01 | 26 | GPIO |
| PA02 | 27 | GPIO | PA03 | 28 | GPIO |
| PA04 | 29 | GPIO | PA05 | 30 | GPIO |
| PA06 | 31 | GPIO | PA07 | 32 | GPIO |
| PA08 | 33 | GPIO | PA09 | 34 | GPIO |
| PA10 | 35 | GPIO | DECOUPLE | 36 | Decoupling Capacitor pin |
| VREGSW | 37 | DCDC output (Inductor) pin | VREGVDD | 38 | DCDC input supply pin |
| VREGVSS | 39 | DCDC ground pin | DVDD | 40 | Digital VDD supply pin |
| AVDD | 41 | Analog VDD supply pin | IOVDD | 42 | IO VDD supply pin |
| PD05 | 43 | GPIO | PD04 | 44 | GPIO |
| PD03 | 45 | GPIO | PD02 | 46 | GPIO |
| PD01 | 47 | GPIO | PD00 | 48 | GPIO |

### 6.2 QFN40 Device Pinout

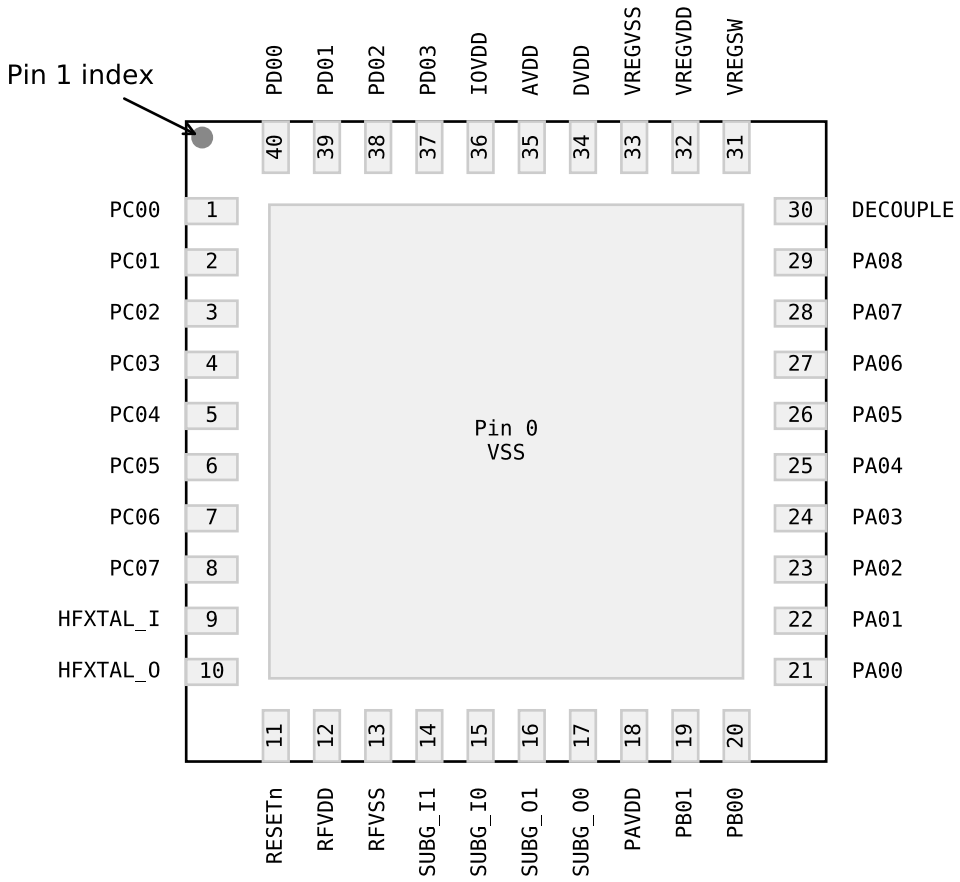


**Figure 6.2. QFN40 Device Pinout**

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.4 Alternate Function Table, 6.5 Analog Peripheral Connectivity, and 6.6 Digital Peripheral Connectivity.

Note that GPIO and Peripheral capabilities may differ by part number or be limited by the API or software stack.

**Table 6.2. QFN40 Device Pinout**

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| PC00 | 1 | GPIO | PC01 | 2 | GPIO |
| PC02 | 3 | GPIO | PC03 | 4 | GPIO |
| PC04 | 5 | GPIO | PC05 | 6 | GPIO |
| PC06 | 7 | GPIO | PC07 | 8 | GPIO |
| HFXTAL_I | 9 | High Frequency XTAL input pin | HFXTAL_O | 10 | High Frequency XTAL output pin |
| RESETn | 11 | Reset pin (active low) | RFVDD | 12 | RF VDD supply pin |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| RFVSS | 13 | RF VSS ground pin | SUBG_I1 | 14 | Sub-GHz Input 1 |
| SUBG_I0 | 15 | Sub-GHz Input 0 | SUBG_O1 | 16 | Sub-GHz Output 1 |
| SUBG_O0 | 17 | Sub-GHz Output 0 | PAVDD | 18 | PA VDD supply pin |
| PB01 | 19 | GPIO | PB00 | 20 | GPIO |
| PA00 | 21 | GPIO | PA01 | 22 | GPIO |
| PA02 | 23 | GPIO | PA03 | 24 | GPIO |
| PA04 | 25 | GPIO | PA05 | 26 | GPIO |
| PA06 | 27 | GPIO | PA07 | 28 | GPIO |
| PA08 | 29 | GPIO | DECOUPLE | 30 | Decoupling Capacitor pin |
| VREGSW | 31 | DCDC output (Inductor) pin | VREGVDD | 32 | DCDC input supply pin |
| VREGVSS | 33 | DCDC ground pin | DVDD | 34 | Digital VDD supply pin |
| AVDD | 35 | Analog VDD supply pin | IOVDD | 36 | IO VDD supply pin |
| PD03 | 37 | GPIO | PD02 | 38 | GPIO |
| PD01 | 39 | GPIO | PD00 | 40 | GPIO |

### 6.3 QFN40 with HFCLKOUT Device Pinout

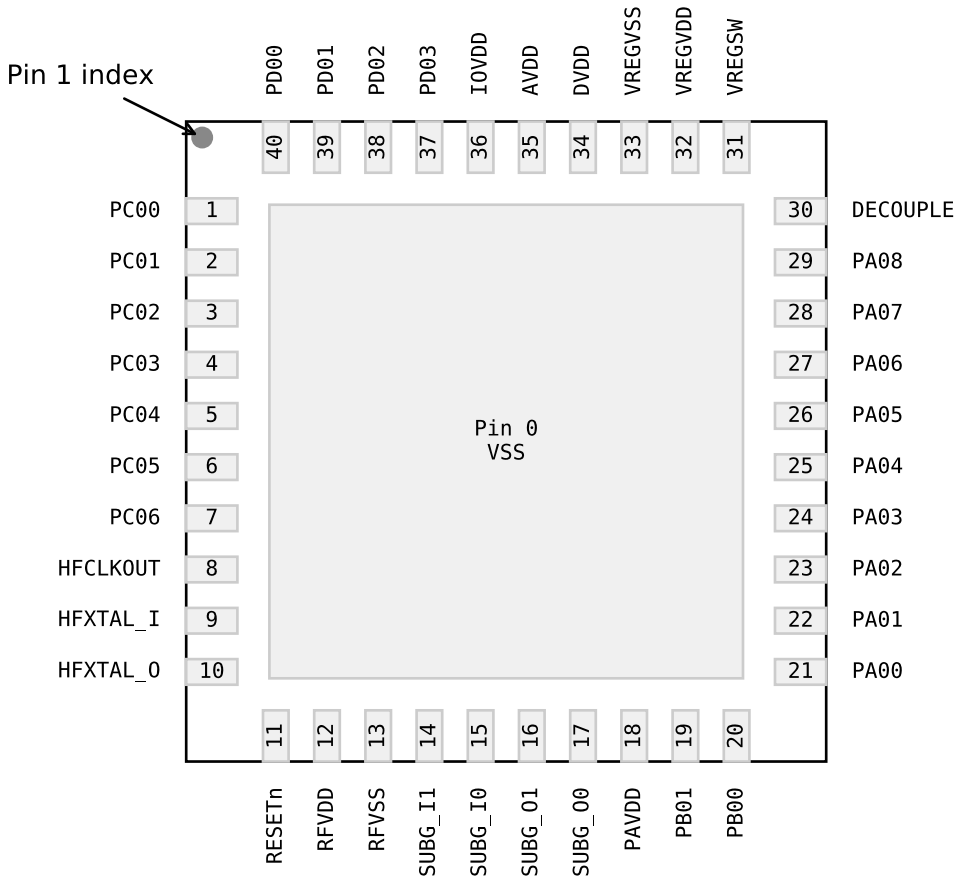


**Figure 6.3. QFN40 with HFCLKOUT Device Pinout**

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.4 Alternate Function Table, 6.5 Analog Peripheral Connectivity, and 6.6 Digital Peripheral Connectivity.

Note that GPIO and Peripheral capabilities may differ by part number or be limited by the API or software stack.

**Table 6.3. QFN40 with HFCLKOUT Device Pinout**

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| PC00 | 1 | GPIO | PC01 | 2 | GPIO |
| PC02 | 3 | GPIO | PC03 | 4 | GPIO |
| PC04 | 5 | GPIO | PC05 | 6 | GPIO |
| PC06 | 7 | GPIO | HFCLKOUT | 8 | High Frequency clock out pin |
| HFXTAL_I | 9 | High Frequency XTAL input pin | HFXTAL_O | 10 | High Frequency XTAL output pin |
| RESETn | 11 | Reset pin (active low) | RFVDD | 12 | RF VDD supply pin |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| RFVSS | 13 | RF VSS ground pin | SUBG_I1 | 14 | Sub-GHz Input 1 |
| SUBG_I0 | 15 | Sub-GHz Input 0 | SUBG_O1 | 16 | Sub-GHz Output 1 |
| SUBG_O0 | 17 | Sub-GHz Output 0 | PAVDD | 18 | PA VDD supply pin |
| PB01 | 19 | GPIO | PB00 | 20 | GPIO |
| PA00 | 21 | GPIO | PA01 | 22 | GPIO |
| PA02 | 23 | GPIO | PA03 | 24 | GPIO |
| PA04 | 25 | GPIO | PA05 | 26 | GPIO |
| PA06 | 27 | GPIO | PA07 | 28 | GPIO |
| PA08 | 29 | GPIO | DECOUPLE | 30 | Decoupling Capacitor pin |
| VREGSW | 31 | DCDC output (Inductor) pin | VREGVDD | 32 | DCDC input supply pin |
| VREGVSS | 33 | DCDC ground pin | DVDD | 34 | Digital VDD supply pin |
| AVDD | 35 | Analog VDD supply pin | IOVDD | 36 | IO VDD supply pin |
| PD03 | 37 | GPIO | PD02 | 38 | GPIO |
| PD01 | 39 | GPIO | PD00 | 40 | GPIO |

### 6.4 Alternate Function Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows GPIO pins with support for dedicated functions across the different package options.

**Table 6.4. GPIO Alternate Function Table**

| GPIO | Alternate Functions | QFN48 Package[1] | QFN40 Package[2] | QFN40 with HFCLKOUT Package[3] |
|---|---|---|---|---|
| PA00 | IADC0.VREFP | Yes | Yes | Yes |
| | LCD.SEG8 | Yes | | |
| PA01 | GPIO.SWCLK | Yes | Yes | Yes |
| | LCD.SEG9 | Yes | | |
| PA02 | GPIO.SWDIO | Yes | Yes | Yes |
| PA03 | GPIO.SWV | Yes | Yes | Yes |
| | GPIO.TDO | Yes | Yes | Yes |
| | GPIO.TRACEDATA0 | Yes | Yes | Yes |
| | LESENSE.EN_0 | Yes | Yes | Yes |
| PA04 | GPIO.TDI | Yes | Yes | Yes |
| | GPIO.TRACECLK | Yes | Yes | Yes |
| | LESENSE.EN_1 | Yes | Yes | Yes |
| | LCD.SEG10 | Yes | | |
| PA05 | GPIO.TRACEDATA1 | Yes | Yes | Yes |
| | GPIO.EM4WU0 | Yes | Yes | Yes |
| | LESENSE.EN_2 | Yes | Yes | Yes |
| | LCD.SEG11 | Yes | | |
| PA06 | GPIO.TRACEDATA2 | Yes | Yes | Yes |
| | LCD.LCD_CP | Yes | | |
| PA07 | GPIO.TRACEDATA3 | Yes | Yes | Yes |
| | LCD.SEG12 | Yes | | |
| PA08 | LCD.SEG13 | Yes | | |
| PB00 | VDAC0.CH0_MAIN_OUT | Yes | Yes | Yes |
| | LCD.SEG14 | Yes | | |
| PB01 | GPIO.EM4WU3 | Yes | Yes | Yes |
| | VDAC0.CH1_MAIN_OUT | Yes | Yes | Yes |
| | LCD.SEG15 | Yes | | |
| PB02 | LCD.SEG16 | Yes | | |
| PB03 | GPIO.EM4WU4 | Yes | | |
| | LCD.SEG17 | Yes | | |
| PC00 | GPIO.EM4WU6 | Yes | Yes | Yes |
| | LCD.SEG0 | Yes | | |

| GPIO | Alternate Functions | QFN48 Package[1] | QFN40 Package[2] | QFN40 with HFCLKOUT Package[3] |
|---|---|---|---|---|
| PC01 | LCD.SEG1 | Yes | | |
| PC02 | LCD.SEG2 | Yes | | |
| PC03 | LCD.SEG3 | Yes | | |
| PC04 | LCD.SEG4 | Yes | | |
| PC05 | GPIO.EM4WU7 | Yes | Yes | Yes |
| | LCD.SEG5 | Yes | | |
| PC06 | LCD.SEG6 | Yes | | |
| | GPIO.THMSW_EN | | | Yes |
| PC07 | GPIO.EM4WU8 | Yes | Yes | |
| | GPIO.THMSW_EN | | Yes | |
| | LCD.SEG7 | Yes | | |
| PC08 | LCD.SEG18 | Yes | | |
| PC09 | GPIO.THMSW_EN | Yes | | |
| | LCD.SEG19 | Yes | | |
| PD00 | LFXO.LFXTAL_O | Yes | Yes | Yes |
| PD01 | LFXO.LFXTAL_I | Yes | Yes | Yes |
| | LFXO.LF_EXTCLK | Yes | Yes | Yes |
| PD02 | GPIO.EM4WU9 | Yes | Yes | Yes |
| | LCD.COM0 | Yes | | |
| PD03 | LCD.COM1 | Yes | | |
| PD04 | LCD.COM2 | Yes | | |
| PD05 | GPIO.EM4WU10 | Yes | | |
| | LCD.COM3 | Yes | | |

**Note:**

1. QFN48 Package includes OPNs EFR32ZG23A010F512GM48-C, EFR32ZG23A020F512GM48-C, EFR32ZG23B010F512IM48-C, and EFR32ZG23B020F512IM48-C
2. QFN40 Package includes OPNs EFR32ZG23A010F512GM40-C, EFR32ZG23A020F512GM40-C, EFR32ZG23B010F512IM40-C, and EFR32ZG23B020F512IM40-C
3. QFN40 with HFCLKOUT Package includes OPNs EFR32ZG23B011F512IM40-C and EFR32ZG23B021F512IM40-C

### 6.5 Analog Peripheral Connectivity

Many analog resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port. When a differential connection is being used Positive inputs are restricted to the EVEN pins and Negative inputs are restricted to the ODD pins. When a single ended connection is being used positive input is available on all pins. See the device Reference Manual for more details on the ABUS and analog peripherals. Note that some functions may not be available on all device variants.

**Table 6.5. ABUS Routing Table**

| Peripheral | Signal | PA | | PB | | PC | | PD | |
|---|---|---|---|---|---|---|---|---|---|
| | | EVEN | ODD | EVEN | ODD | EVEN | ODD | EVEN | ODD |
| ACMP0 | ANA_NEG | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| | ANA_POS | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| ACMP1 | ANA_NEG | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| | ANA_POS | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| IADC0 | ANA_NEG | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| | ANA_POS | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| VDAC0 | CH0_ABUS_OUT | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| | CH1_ABUS_OUT | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |

### 6.6 Digital Peripheral Connectivity

Many digital resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port. Note that some functions may not be available on all device variants.

**Table 6.6. DBUS Routing Table**

| Peripheral.Resource | PORT | | | |
|---|---|---|---|---|
| | PA | PB | PC | PD |
| ACMP0.DIGOUT | Available | Available | Available | Available |
| ACMP1.DIGOUT | Available | Available | Available | Available |
| CMU.CLKIN0 | | | Available | Available |
| CMU.CLKOUT0 | | | Available | Available |
| CMU.CLKOUT1 | | | Available | Available |
| CMU.CLKOUT2 | Available | Available | | |
| EUSART0.CS | Available | Available | | |
| EUSART0.CTS | Available | Available | | |
| EUSART0.RTS | Available | Available | | |
| EUSART0.RX | Available | Available | | |
| EUSART0.SCLK | Available | Available | | |
| EUSART0.TX | Available | Available | | |
| EUSART1.CS | Available | Available | Available | Available |
| EUSART1.CTS | Available | Available | Available | Available |
| EUSART1.RTS | Available | Available | Available | Available |
| EUSART1.RX | Available | Available | Available | Available |
| EUSART1.SCLK | Available | Available | Available | Available |
| EUSART1.TX | Available | Available | Available | Available |
| EUSART2.CS | | | Available | Available |
| EUSART2.CTS | | | Available | Available |
| EUSART2.RTS | | | Available | Available |
| EUSART2.RX | | | Available | Available |
| EUSART2.SCLK | | | Available | Available |
| EUSART2.TX | | | Available | Available |
| FRC.DCLK | | | Available | Available |
| FRC.DFRAME | | | Available | Available |
| FRC.DOUT | | | Available | Available |
| HFXO0.BUFOUT_REQ_IN_ASYNC | Available | Available | | |
| I2C0.SCL | Available | Available | Available | Available |
| I2C0.SDA | Available | Available | Available | Available |
| I2C1.SCL | | | Available | Available |

| Peripheral.Resource | PORT | | | |
|---|---|---|---|---|
| | PA | PB | PC | PD |
| I2C1.SDA | | | Available | Available |
| KEYSCAN.COL_OUT_0 | Available | Available | Available | Available |
| KEYSCAN.COL_OUT_1 | Available | Available | Available | Available |
| KEYSCAN.COL_OUT_2 | Available | Available | Available | Available |
| KEYSCAN.COL_OUT_3 | Available | Available | Available | Available |
| KEYSCAN.COL_OUT_4 | Available | Available | Available | Available |
| KEYSCAN.COL_OUT_5 | Available | Available | Available | Available |
| KEYSCAN.COL_OUT_6 | Available | Available | Available | Available |
| KEYSCAN.COL_OUT_7 | Available | Available | Available | Available |
| KEYSCAN.ROW_SENSE_0 | Available | Available | | |
| KEYSCAN.ROW_SENSE_1 | Available | Available | | |
| KEYSCAN.ROW_SENSE_2 | Available | Available | | |
| KEYSCAN.ROW_SENSE_3 | Available | Available | | |
| KEYSCAN.ROW_SENSE_4 | Available | Available | | |
| KEYSCAN.ROW_SENSE_5 | Available | Available | | |
| LESENSE.CH0OUT | Available | Available | | |
| LESENSE.CH1OUT | Available | Available | | |
| LESENSE.CH2OUT | Available | Available | | |
| LESENSE.CH3OUT | Available | Available | | |
| LESENSE.CH4OUT | Available | Available | | |
| LESENSE.CH5OUT | Available | Available | | |
| LESENSE.CH6OUT | Available | Available | | |
| LESENSE.CH7OUT | Available | Available | | |
| LESENSE.CH8OUT | Available | Available | | |
| LESENSE.CH9OUT | Available | Available | | |
| LESENSE.CH10OUT | Available | Available | | |
| LESENSE.CH11OUT | Available | Available | | |
| LESENSE.CH12OUT | Available | Available | | |
| LESENSE.CH13OUT | Available | Available | | |
| LESENSE.CH14OUT | Available | Available | | |
| LESENSE.CH15OUT | Available | Available | | |
| LETIMER0.OUT0 | Available | Available | | |
| LETIMER0.OUT1 | Available | Available | | |
| MODEM.ANT0 | Available | Available | Available | Available |
| MODEM.ANT1 | Available | Available | Available | Available |
| MODEM.ANT_ROLL_OVER | | | Available | Available |

| Peripheral.Resource | PORT | | | |
|---|---|---|---|---|
| | PA | PB | PC | PD |
| MODEM.ANT_RR0 | | | Available | Available |
| MODEM.ANT_RR1 | | | Available | Available |
| MODEM.ANT_RR2 | | | Available | Available |
| MODEM.ANT_RR3 | | | Available | Available |
| MODEM.ANT_RR4 | | | Available | Available |
| MODEM.ANT_RR5 | | | Available | Available |
| MODEM.ANT_SW_EN | | | Available | Available |
| MODEM.ANT_SW_US | | | Available | Available |
| MODEM.ANT_TRIG | | | Available | Available |
| MODEM.ANT_TRIG_STOP | | | Available | Available |
| MODEM.DCLK | Available | Available | | |
| MODEM.DIN | Available | Available | | |
| MODEM.DOUT | Available | Available | | |
| PCNT0.S0IN | Available | Available | | |
| PCNT0.S1IN | Available | Available | | |
| PRS.ASYNCH0 | Available | Available | | |
| PRS.ASYNCH1 | Available | Available | | |
| PRS.ASYNCH2 | Available | Available | | |
| PRS.ASYNCH3 | Available | Available | | |
| PRS.ASYNCH4 | Available | Available | | |
| PRS.ASYNCH5 | Available | Available | | |
| PRS.ASYNCH6 | | | Available | Available |
| PRS.ASYNCH7 | | | Available | Available |
| PRS.ASYNCH8 | | | Available | Available |
| PRS.ASYNCH9 | | | Available | Available |
| PRS.ASYNCH10 | | | Available | Available |
| PRS.ASYNCH11 | | | Available | Available |
| PRS.SYNCH0 | Available | Available | Available | Available |
| PRS.SYNCH1 | Available | Available | Available | Available |
| PRS.SYNCH2 | Available | Available | Available | Available |
| PRS.SYNCH3 | Available | Available | Available | Available |
| TIMER0.CC0 | Available | Available | Available | Available |
| TIMER0.CC1 | Available | Available | Available | Available |
| TIMER0.CC2 | Available | Available | Available | Available |
| TIMER0.CDTI0 | Available | Available | Available | Available |
| TIMER0.CDTI1 | Available | Available | Available | Available |

| Peripheral.Resource | PORT | | | |
|---|---|---|---|---|
| | PA | PB | PC | PD |
| TIMER0.CDTI2 | Available | Available | Available | Available |
| TIMER1.CC0 | Available | Available | Available | Available |
| TIMER1.CC1 | Available | Available | Available | Available |
| TIMER1.CC2 | Available | Available | Available | Available |
| TIMER1.CDTI0 | Available | Available | Available | Available |
| TIMER1.CDTI1 | Available | Available | Available | Available |
| TIMER1.CDTI2 | Available | Available | Available | Available |
| TIMER2.CC0 | Available | Available | | |
| TIMER2.CC1 | Available | Available | | |
| TIMER2.CC2 | Available | Available | | |
| TIMER2.CDTI0 | Available | Available | | |
| TIMER2.CDTI1 | Available | Available | | |
| TIMER2.CDTI2 | Available | Available | | |
| TIMER3.CC0 | | | Available | Available |
| TIMER3.CC1 | | | Available | Available |
| TIMER3.CC2 | | | Available | Available |
| TIMER3.CDTI0 | | | Available | Available |
| TIMER3.CDTI1 | | | Available | Available |
| TIMER3.CDTI2 | | | Available | Available |
| TIMER4.CC0 | Available | Available | | |
| TIMER4.CC1 | Available | Available | | |
| TIMER4.CC2 | Available | Available | | |
| TIMER4.CDTI0 | Available | Available | | |
| TIMER4.CDTI1 | Available | Available | | |
| TIMER4.CDTI2 | Available | Available | | |
| USART0.CLK | Available | Available | Available | Available |
| USART0.CS | Available | Available | Available | Available |
| USART0.CTS | Available | Available | Available | Available |
| USART0.RTS | Available | Available | Available | Available |
| USART0.RX | Available | Available | Available | Available |
| USART0.TX | Available | Available | Available | Available |

# 7. QFN40 Package Specifications

## 7.1 QFN40 Package Dimensions

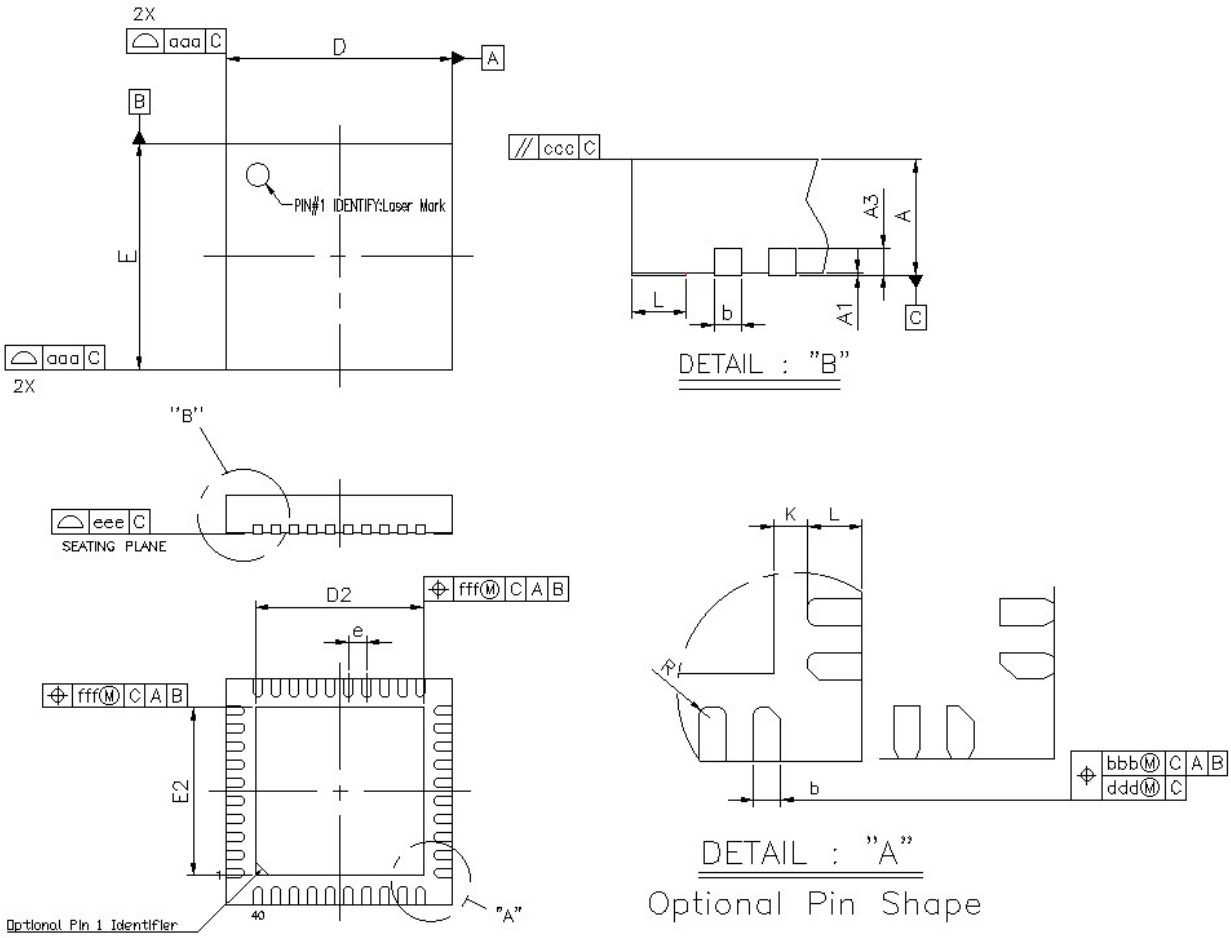


**Figure 7.1. QFN40 Package Drawing**

**Table 7.1. QFN40 Package Dimensions**

| Dimension | Min | Typ | Max |
|---|---|---|---|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.20 REF | |
| b | 0.15 | 0.20 | 0.25 |
| D | 4.90 | 5.00 | 5.10 |
| E | 4.90 | 5.00 | 5.10 |
| D2 | 3.55 | 3.70 | 3.85 |
| E2 | 3.55 | 3.70 | 3.85 |
| e | | 0.40 BSC | |
| L | 0.30 | 0.40 | 0.50 |
| K | 0.20 | — | — |
| R | 0.075 | — | — |
| aaa | | 0.10 | |
| bbb | | 0.07 | |
| ccc | | 0.10 | |
| ddd | | 0.05 | |
| eee | | 0.08 | |
| fff | | 0.10 | |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
5. Package external pad (epad) may have pin one chamfer.

### 7.2 QFN40 PCB Land Pattern

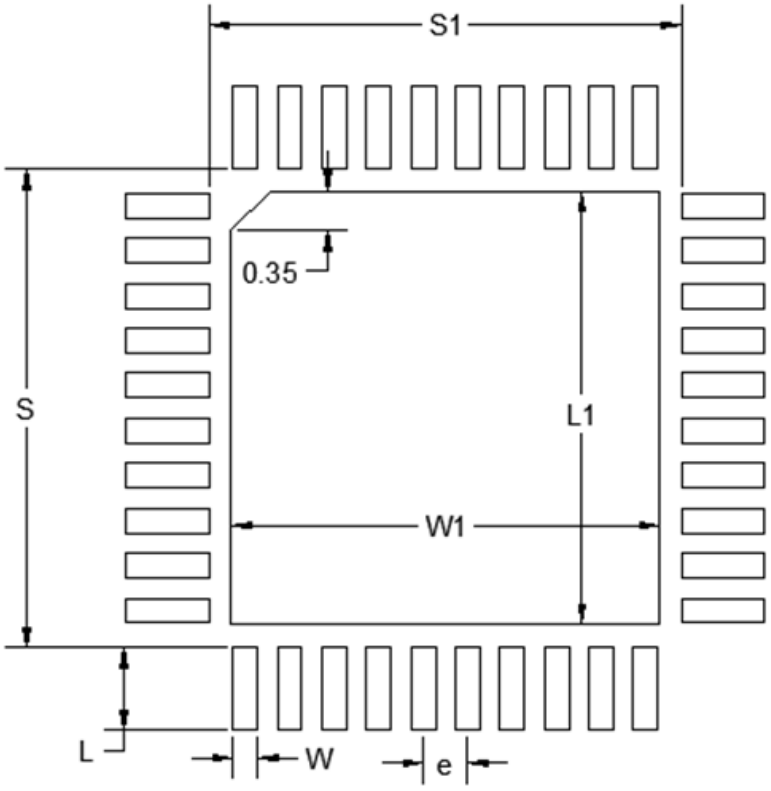


**Figure 7.2. QFN40 PCB Land Pattern Drawing**

**Table 7.2. QFN40 PCB Land Pattern Dimensions**

| Dimension | Typ |
|---|---|
| S1 | 4.25 |
| S | 4.25 |
| L1 | 3.85 |
| W1 | 3.85 |
| e | 0.40 |
| W | 0.22 |
| L | 0.74 |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
4. The stencil thickness should be 0.101 mm (4 mils).
5. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
6. A 3x3 array of 0.90 mm square openings on a 1.20 mm pitch can be used for the center ground pad.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
9. ***Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.***

### 7.3 QFN40 Package Marking

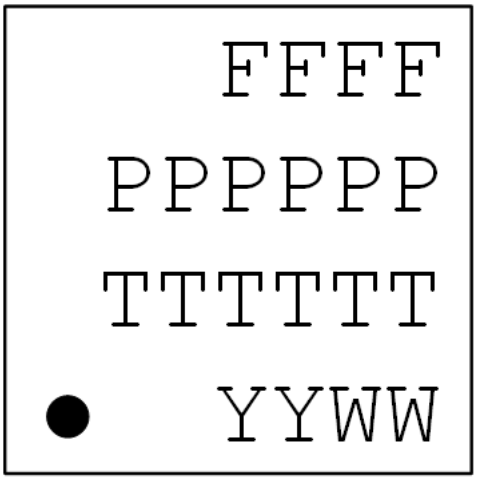


**Figure 7.3. QFN40 Package Marking**

The package marking consists of:

- FFFF – The product family codes.
  1. Family Code ( F | Z )
  2. G (Gecko)
  3. Series (2)
  4. Device Configuration (3)
- PPPPPP – The product option codes.
  - 1. Security ( A = Secure Vault Mid | B = Secure Vault High )
  - 2-4. Product Feature Codes
  - 5. Flash ( H = 512k | G = 256k | F = 128k )
  - 6. Temperature grade (G = -40 to 85 °C | I = -40 to 125 °C )
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

# 8. QFN48 Package Specifications

## 8.1 QFN48 Package Dimensions

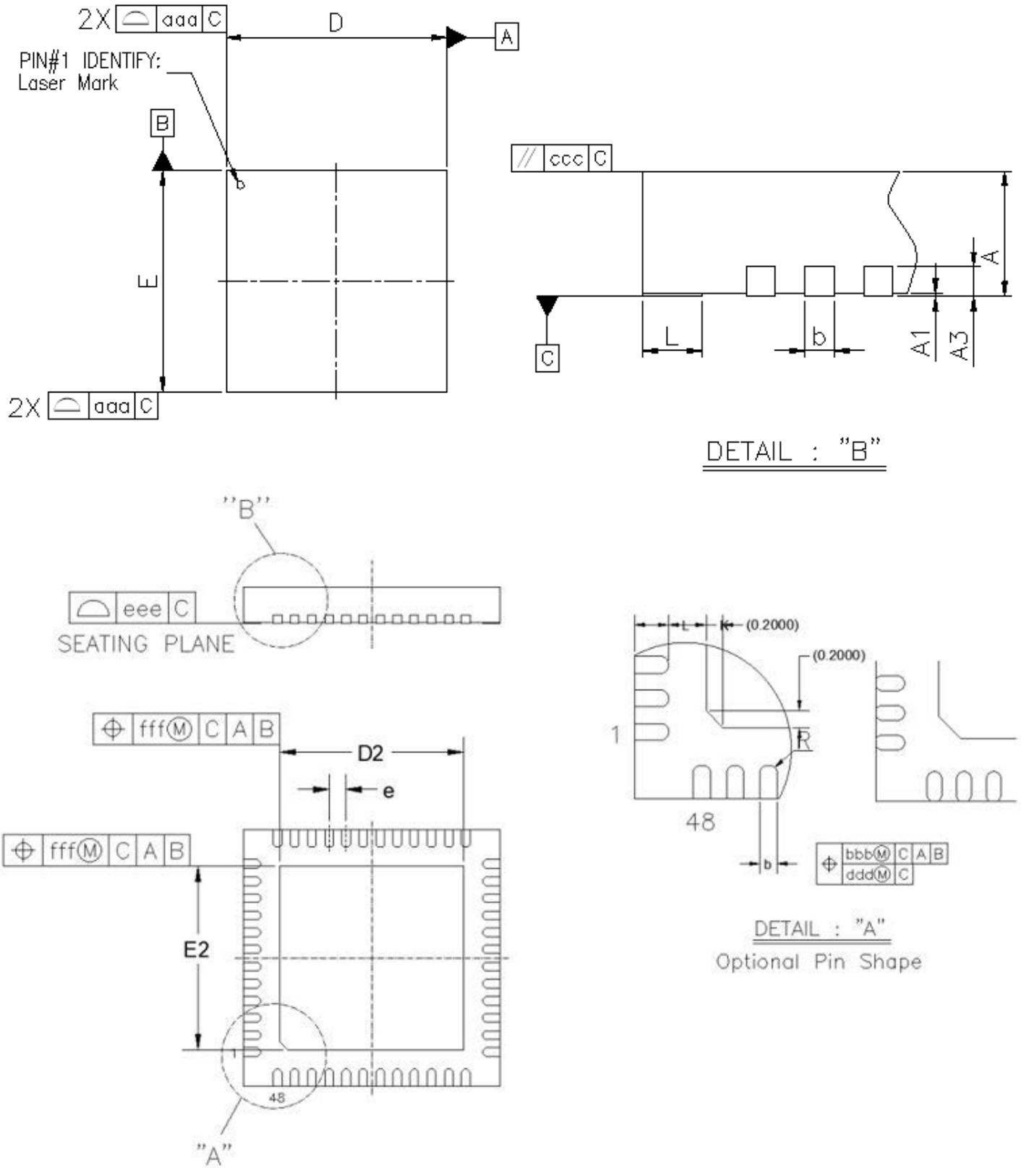


**Figure 8.1. QFN48 Package Drawing**

**Table 8.1. QFN48 Package Dimensions**

| Dimension | Min | Typ | Max |
|---|---|---|---|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.20 REF | |
| b | 0.15 | 0.2 | 0.25 |
| D | 5.90 | 6.00 | 6.10 |
| E | 5.90 | 6.00 | 6.10 |
| e | | 0.40 BSC | |
| D2 | 4.15 | 4.30 | 4.45 |
| E2 | 4.15 | 4.30 | 4.45 |
| L | 0.30 | 0.4 | 0.50 |
| K | 0.20 | — | — |
| R | 0.075 | — | — |
| aaa | | 0.10 | |
| bbb | | 0.07 | |
| ccc | | 0.10 | |
| ddd | | 0.05 | |
| eee | | 0.08 | |
| fff | | 0.10 | |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Outline MS-013, Variation AA.
4. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

### 8.2 QFN48 PCB Land Pattern

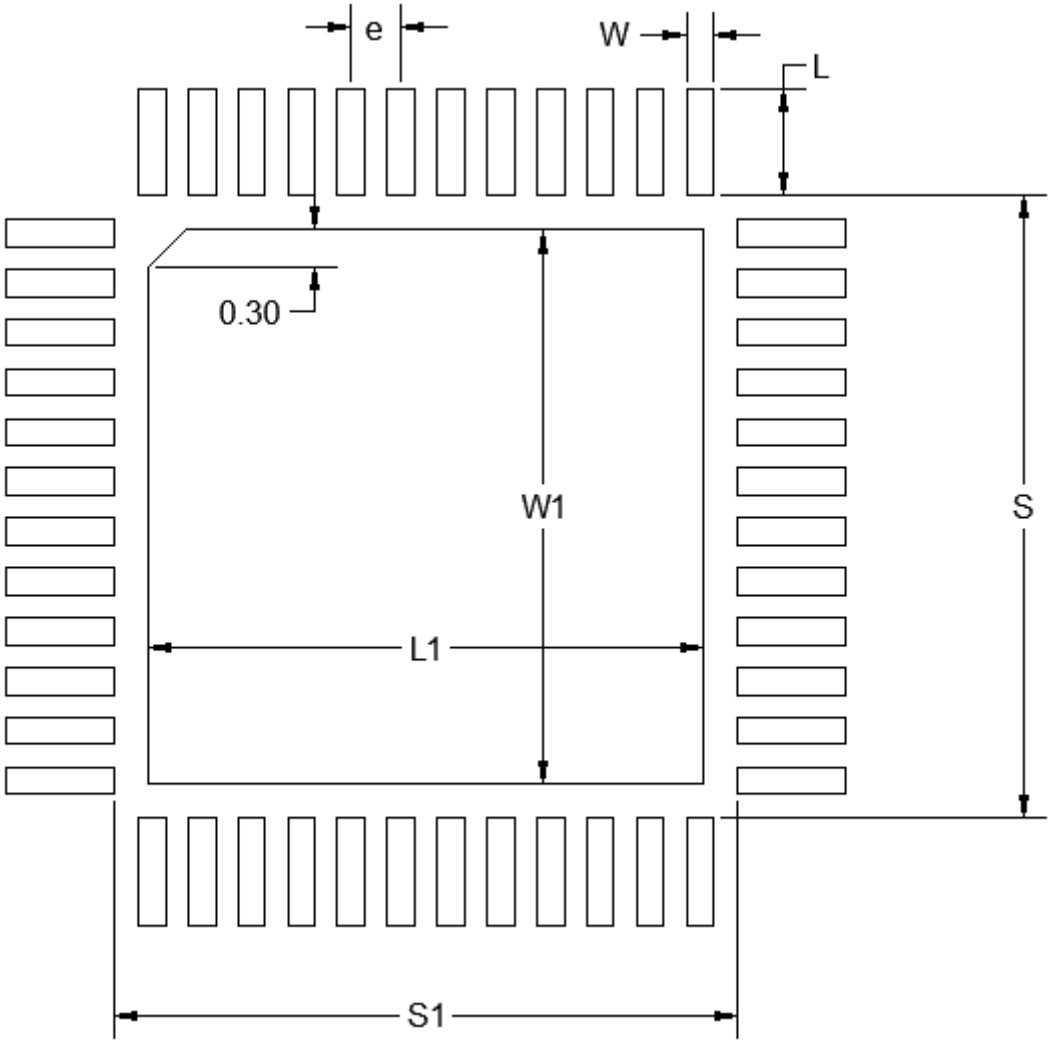


**Figure 8.2. QFN48 PCB Land Pattern Drawing**

**Table 8.2. QFN48 PCB Land Pattern Dimensions**

| Dimension | Typ |
|---|---|
| L | 0.86 |
| W | 0.22 |
| e | 0.40 |
| S | 5.01 |
| S1 | 5.01 |
| L1 | 4.45 |
| W1 | 4.45 |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.101 mm (4 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
7. A 3x3 array of 1.10mm x 1.10mm openings on 1.30mm pitch should be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
10. ***Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.***

### 8.3 QFN48 Package Marking

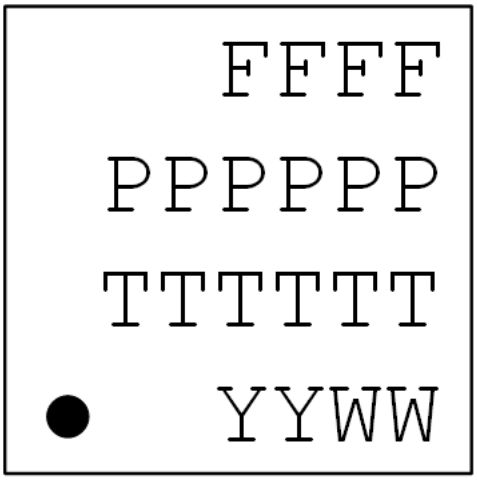


**Figure 8.3. QFN48 Package Marking**

The package marking consists of:

- FFFF – The product family codes.
  1. Family Code ( F | Z )
  2. G (Gecko)
  3. Series (2)
  4. Device Configuration (3)
- PPPPPP – The product option codes.
  - 1. Security ( A = Secure Vault Mid | B = Secure Vault High )
  - 2-4. Product Feature Codes
  - 5. Flash ( H = 512k | G = 256k | F = 128k )
  - 6. Temperature grade (G = -40 to 85 °C | I = -40 to 125 °C )
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

# 9. Revision History

### Revision 1.3

March, 2025

- Update INL specifications for Table 4.34 VDAC on page 75

### Revision 1.2

April, 2023

- Updated Table 3.1 Secure Vault Features on page 14 table to show that "Curve25519 (ECDH)" and "Ed25519 (EdDSA)" are available for Public Key Encryption for Secure Vault Mid if using SE firmware v2.1.7 or higher.
- Clarified that Secure Debug is supported for both Secure Vault Mid and High in 3.8.4 Secure Debug with Lock/Unlock section.
- 4.3 General Operating Conditions table changes:
  - Added HCLK and SYSCLK frequency specification for "VSCALE1, WS1" test condition.
  - Corrected HCLK and SYSCLK frequency MAX value for "VSCALE1, WS0" test condition.
  - Corrected test condition for External Clock input specifications to add "IOVDD >= 2.7V".
- 4.9.2.1 916 MHz Band RF Receiver Characteristics for Z-Wave table changes:
  - Minor updates to the parameters and symbols.
- 4.9.2.2 915 MHz Band RF Receiver Characteristics table changes:
  - Minor updates to the parameters, symbols and test conditions.
  - Added footnote 9.
- 4.9.2.3 868 MHz Band RF Receiver Characteristics for Z-Wave table changes:
  - Updated test condition for $SPUR_{RX}$ from "1 GHz to 12 GHz" to "1 GHz to 6 GHz"
  - Minor updates to the parameters and symbols.
- 4.9.2.4 868 MHz Band RF Receiver Characteristics table changes:
  - Minor updates to the parameters, symbols and test conditions.
  - Added footnote 8.
- 4.9.2.5 433 MHz Band RF Receiver Characteristics table changes:
  - Minor updates to the parameters and symbols.
- 4.11.3 High Frequency RC Oscillator (HFRCO) table changes:
  - Added Band Frequency Limit specification for "FREQRANGE =5".
- 4.13 Analog to Digital Converter (IADC) table changes:
  - Corrected test conditions for Gain Error specifications to add $f_{ADC_CLK}$ when using External VREF.
- 4.15 Digital to Analog Converter (VDAC) table changes:
  - Corrected $I_{DAC_2_STAT}$ MAX specification from 340 µA to 400 µA for High power mode.
  - Corrected $I_{DAC_2_STAT}$ MAX specification from 65 µA to 90 µA for Low power mode.
- Corrected Gecko Bootloader size from 24 kB to 10.4 kB in 4.25 Boot Timing section.
- 4.25 Boot Timing table changes:
  - Added condition "Second stage bootloader check enabled" for all specifications
  - Added specification for "Secure boot application check disable, no bootloader"

**Revision 1.1**

June, 2022

- 2. Ordering Information: Updated all OPNs to revision C.
- Corrected number of EUSART instances shown in Feature List'
- Table 4.3 DC-DC Converter on page 26: Added missing efficiency specification line for EM0/EM1.
- Table 4.12 Flash Characteristics on page 40: Specified timing for write/erase across full temperature (In version 1.0 showed timing at condition $T_A$ = 25 °C)'
- Table 4.25 High Frequency Crystal Oscillator on page 63: Corrected naming convention from "HFXOUT" to "HFCLKOUT", and $C_{HFXO_LC}$ to $C_{L_HFXO}$'
- Table 4.26 Low Frequency Crystal Oscillator on page 64: Corrected naming convention from $C_{LFXO_CL}$ to $C_{L_LFXO}$.
- Table 4.32 Analog to Digital Converter (IADC) on page 70:
  - Added $C_S$ specification for Analog Gain = 3x condition.
  - Added $f_S$ specification.
  - Updated naming from $f_{CLK}$ to $f_{ADC_CLK}$ to match mentions in reference manual and other literature.
  - Updated OFFSET units to LSB12 for clarity (was LSB).
- Table 4.33 Analog Comparator (ACMP) on page 73: Updated supply current specification numbers to revision C characterization results.
- Table 4.35 LCD on page 77: $V_{LCD}$ Max specifications changed to include supply limiting, numbers now show expected range for all conditions instead of potential range for any condition.
- Replaced "StdCmd" with more descriptive "Crypto Operation" text.

**Revision 1.0**

March, 2022

- Added section: 3.2.8 Preamble Sense Mode.
- 3.10.4 Power Domains: Extended description of available power domains.
- 4.1 Electrical Characteristics:
  - Populated min/max final test limits throughout electrical specification tables.
  - Added RF specification tables for general 915, 868, and 433 MHz operation.
  - Added HFCLKOUT specifications to High Frequency Crystal Oscillator table.
  - Added RF TX power output characteristic plots.
- 6.4 Alternate Function Table: Changed formatting of section to show signals available on each package option and include footnote to detail OPNs.

**Revision 0.5**

September, 2021

- 4.1 Electrical Characteristics: Updated specification tables with latest characterization and production test parameters.
- 5.1 Power: Corrected typical power supply connections to show proper ferrite placement on PAVDD.
- Table 5.2 868/915/920 MHz Component Values, +20 dBm on page 104: Corrected value L4 to 18 nH.
- Package marking specifications updated.

**Revision 0.2**

June, 2021

Initial release.

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