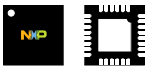
KW47

KW47 Product Family

Rev. 4 — 18 December 2025 Product data sheet

KW47B42ZBxAFTBx
KW47B42Z9xAFTBx
KW47B42Z8xAFTBx
KW47Z420BxAFTBx
KW47Z4209xAFTBx
KW47Z4208xAFTBx



48 HVQFN
7 x 7 x 0.85 mm
Pitch 0.5 mm
Wettable Flanks

Features

- The KW47 product family is a low-power, highly secure, single-chip wireless MCU that integrates a high performance Bluetooth Low Energy version 6.0 radio and CAN FD for Automotive and Industrial applications.
- The family integrates a state-of-the-art, scalable security architecture including Arm® TrustZone®-M, a resource domain controller, and an isolated EdgeLock™ Secure Enclave supporting hardware cryptographic accelerators, random number generators and key generation, storage and management and secure debug. Flash memory contents can optionally be stored as encrypted data and then decrypted on-the-fly enabling protection of sensitive data and algorithms.
- For automotive applications, two integrated FlexCAN supporting CAN and CAN FD compliant with the ISO 11898-1 standard. The on-chip, low-power UARTs have LIN capabilities. The family is AEC-Q100 Grade 2 automotive qualified, with an extended ambient operating temperature range up to +105 °C.
- The family integrates a Localization Compute Engine (LCE) featuring a digital signal processing (DSP) unit with a 64-bit SIMD data path for accelerating advanced Bluetooth® Channel Sounding algorithms via a high-performance vector and matrix operation library, including FFT, Eigenvalue Decomposition (EVD), and Hermitian matrix inverse.

Application core

- Up to 96 MHz Arm Cortex®-M33 core
- Up to 2 MB flash memory
- 264 KB SRAM
- TrustZone-M, IEEE 754 FPU, DSP, MPU, NVIC, SysTick
- 16 KB Code Cache to improve performance and efficiency
- Secure Boot ROM

Low-power consumption (DCDC 3.3 V, 25 ºC)

- Transceiver current
  - Typical RX: 5.2 mA
  - Typical TX at 0 dBm: 5.38 mA and 15.75 mA at 10 dBm
- Less than 4 µA in power-down mode with real-time clock (RTC) active and 48 KB SRAM retention
- Less than 1.5 µA in Deep Power-Down mode with RTC active
- Multiple power-down modes supporting currents as low as 300 nA
- Ultra-low leakage Smart Power Switch with less than 130 nA sleep current with exit from internal timer or GPIO.

Input supply voltage options:

- Integrated DCDC regulator 1.86–3.6 V providing power to Core_LDO regulator, SYS_LDO regulators, and Radio
- Integrated Core_LDO regulator 1.25 V–3.6 V powering the core digital domain
- Integrated SYS_LDO regulator 1.86 V to 3.6 V powering the SYS domain

Human Machine Interface modules

- 29 General-purpose input/output (GPIO)

Operating characteristics

- Temperature range (ambient): –40 °C to 105 °C
- Temperature range (junction): –40 °C to 125 °C
- DC/DC voltage range: 1.86 V to 3.6 V
- LDO mode voltage range: 1.86 V to 3.6 V
- Qualification: AEC-Q100 Grade 2

EdgeLock Secure Enclave

- Secure boot and debug
- Trusted Resource Domain Controller (TRDC) providing programmable control mechanisms for independent processing domains including embedded memory and peripherals
  - Privilege/user
  - Data only
  - Execute only
  - Read-only access
  - Secure/Non-secure

  Advanced flash access protection
  - Write/Erase protection, Execute only, Data only access control
  - Optional encryption and on-the-fly decryption using a PRINCE XEX block cipher mode
- Hardware encryption and decryption
  - Symmetric Key Encryption
    - AES-128/192/256
    - ECB, CBC, CTR, GCM, CMAC, and CCM Modes
  - Asymmetric Key Encryption
    - ECC NIST P–192/224/256/384/521
    - Curve25519
  - Key Exchange Algorithms
    - ECDH(E)
    - SPAKE2+
    - JPAKE
  - Digital Signature Algorithms
    - ECDSA
    - Ed25519

  - Hash Algorithms
    - SHA2-224/256/384/512
    - Poly1305
- Secure key generation, storage, and management
- Pseudo (PRNG) and True Random Number Generator (TRNG) with 512-bits entropy supporting NIST SP 800-90A and SP 800-90B
- Support for secure over-the-air (OTA) firmware updates
- Four digital tamper pins with optional interrupt and seconds timestamp upon trigger
- Universally Unique ID (UUID) programmed by NXP during factory programming
- Factory Root of Trust programming

Communication interfaces

- Two FlexCAN with CAN and CAN FD supporting the full implementation of the CAN Specification Version 2.0, Part B. FD Support.
- Two Low Power UART (LPUART) modules with LIN support
- Two Low Power SPI modules and one MIPI-I3C module
- Two Low Power I2C (LPI2C) modules supporting the System Management Bus (SMBus) Specification, version 2
- One programmable FlexIO module supporting emulation of UART, I2C, SPI, Camera IF, LCD RGB, PWM/Waveform generation

Clocks

- 32 MHz RF crystal oscillator
- 32.768 kHz crystal oscillator
- Internal 192 MHz high frequency free running oscillator providing 48/64/96 MHz clock
- Internal low power free running oscillator providing 32 kHz clock

System peripherals

- DC/DC converter supporting buck and bypass operating modes
- Asynchronous DMA controller with per channel access permissions (secure/non-secure)
- Two internal and one external watchdog monitors
- Nested vectored interrupt controller
- Wake-up unit for power-down modes

Timers

- Two 6-channel 32-bit timers (TPM) with PWM capability and DMA support
- Three 32-bit low-power timers (LPTMR) or pulse counters with compare features
- 4-channel 32-bit low-power periodic interrupt timer (LPIT) with DMA support
- 32-bit seconds real time counter (RTC) with 32-bit alarm and independent power supply
- Signal frequency analyzer (SFA) provides facilities for measurement of clock period/frequency as well as time between triggers

Safety

- Memory Protection Unit (MPU)
- Register write protection

- Illegal memory access
- Flash area protection
- SRAM Error Correction Code (ECC)
- Clock Frequency Accuracy Measurement Circuit (CAC) using Signal Frequency Analyzer (SFA) module
- Cyclic Redundancy Check (CRC) calculator
- Two internal, independent and one external watchdog timer
- Clock loss detection
- Main oscillator stop detection (Loss of lock detection)
- Low voltage / high voltage detection

Bluetooth Low Energy radio core

- Factory-programmed IEEE MAC address
- Dedicated CM33 core running at up to 64 MHz
- 512 kB Flash supporting upgradable software radio
- 171 KB SRAM optimized for link layer support
- Up to 24 simultaneous connections
- –106 dBm 125 kbps Long Range Receive Sensitivity
- –102 dBm 500 kbps Long Range Receive Sensitivity
- –97.5 dBm 1 Mbps Receive Sensitivity
- –95 dBm 2 Mbps Receiver Sensitivity
- Programmable Transmit Output Power up to +10 dBm
- Data Rates: 125 kbps, 500 kbps, 1 Mbps, and 2 Mbps
- Modulation Types: 2 Level FSK, GFSK, MSK, GMSK
- Integrated memories in radio containing Bluetooth LE Controller Stack and radio drivers
- On-chip balun with single ended bidirectional RF port
- Low external component counts for low cost, small form-factor designs

Channel Sounding capabilities

- CS Step for time and frequency synchronization – Mode 0 - supported
- RTT packet exchange – Mode 1 - supported
- Tone exchange (Phase Based Ranging) – Mode 2 - supported
- RTT and tone exchange – Mode 3 - supported
- Number of antenna paths - N_AP - 1, 2, 4
- Antenna Configurations - 1x1, 1x2, 1x4, 2x1, 4x1, 2x2
- Channel map specifies which channels are used or excluded - Channel_Map - supported
- Channel Sounding Initiator - CS Initiator - supported
- Channel Sounding Reflector - CS Reflector - supported
- Modulation supported in mode 0, mode 1 and mode 3 packets 1 Mbps, 2 Mbps - CS SYNC PHY - supported
- CS SYNC packet payload (HW support) – RTT_TYPE - Access Address only Random Sequence 32, 64, 96 and 128 bit

- RTT_AA_Only_N, RTT_Random_Payload_N - 10 ns time-of-flight precision requirement - RTT_Capability - supported Channel Sounding security up to level 4
- Channel selection algorithm for mode 0 steps - #3A
- Channel selection algorithm for non-mode 0 steps - #3B, #3C
- Tone quality indicator – TQI – low and high supported
- Normalized Attack Detection Metric (phase-based) – NADM - supported
- Bluetooth LE specification allows repeating the procedure multiple times in a controlled way - Procedure Repeat - supported
- Frequency Actuation Error bit indicates whether the device supports mode-0 FAE tables - No_FAE - supported
- Time allocated to swap channel – T_FCS – 50, 80, 150 µs
- Interlude time allocated between RTT packets from initiator device and reflector device – T_IP1 - 40, 80, 145 µs
- Interlude time allocated between tone TX from initiator device and reflector device – T_IP2 - 40, 80, 145 µs
- Phase measurement time – T_PM – 20, 40 µs
- Time allocated for Power Amplifier ramp-down – T_RD – 5 µs
- Guard time between tone and packet transmission, in mode 0 and mode 3 steps – T_GD – 10 µs
- Antenna switching time – T_SW – 2, 4, 10 µs
- Frequency measurement time in mode 0 step – T_FM – 80 µs
- CS SYNC packet (Access Address) duration – T_SY - 44 µs(1M CS SYNC PHY), 26 µs(2M CS SYNC PHY)

Analog modules

- 16-bit single ended SAR Analog-to-Digital Converter (ADC) up to 2 Msps
- Two high-speed Analog Comparators (CMP) with 8-bit Digital-to-Analog Converter (DAC)
- 1.0 V to 2.1 V Voltage Reference (Vref)

Target applications

- Automotive
  - Secure Car Access
  - Keyless Entry
  - Passive Entry/Passive Start (PEPS) Systems
  - Wireless Battery Management Systems (WBMS)
- Industrial/IoT
  - Positioning/Localization
  - Building Control and Monitoring
  - Process/Factory Automation
  - Access Control

Table 1. Ordering information of radio parts [1],[2]

Part number	Radio Protocol	FLASH (KB)	SRAM (KB)	LCE	Package/Pin Count	CAN	Qualification	Packaging Type
KW47B42ZB7AFTBT	Bluetooth 6.0	2 MB + 512 KB	264 KB + 171 KB	Yes	7x7 48-pin HVQFN "Wettable"	Yes	AEC-Q100 Grade 2	Tray
KW47B42ZB7AFTBR	Bluetooth 6.0	2 MB + 512 KB	264 KB + 171 KB	Yes	7x7 48-pin HVQFN "Wettable"	Yes	AEC-Q100 Grade 2	Tape and Reel
KW47B42ZB6AFTBT	Bluetooth 6.0	2 MB + 512 KB	264 KB + 171 KB	Yes	7x7 48-pin HVQFN "Wettable"	No	AEC-Q100 Grade 2	Tray
KW47B42ZB6AFTBR	Bluetooth 6.0	2 MB + 512 KB	264 KB + 171 KB	Yes	7x7 48-pin HVQFN "Wettable"	No	AEC-Q100 Grade 2	Tape and Reel
KW47B42Z97AFTBT	Bluetooth 6.0	1 MB + 512 KB	264 KB + 171 KB	Yes	7x7 48-pin HVQFN "Wettable"	Yes	AEC-Q100 Grade 2	Tray
KW47B42Z97AFTBR	Bluetooth 6.0	1 MB + 512 KB	264 KB + 171 KB	Yes	7x7 48-pin HVQFN "Wettable"	Yes	AEC-Q100 Grade 2	Tape and Reel
KW47B42Z96AFTBT	Bluetooth 6.0	1 MB + 512 KB	264 KB + 171 KB	Yes	7x7 48-pin HVQFN "Wettable"	No	AEC-Q100 Grade 2	Tray
KW47B42Z96AFTBR	Bluetooth 6.0	1 MB + 512 KB	264 KB + 171 KB	Yes	7x7 48-pin HVQFN "Wettable"	No	AEC-Q100 Grade 2	Tape and Reel
KW47B42ZB3AFTBT	Bluetooth 6.0	2 MB + 512 KB	264 KB + 171 KB	No	7x7 48-pin HVQFN "Wettable"	Yes	AEC-Q100 Grade 2	Tray
KW47B42ZB3AFTBR	Bluetooth 6.0	2 MB + 512 KB	264 KB + 171 KB	No	7x7 48-pin HVQFN "Wettable"	Yes	AEC-Q100 Grade 2	Tape and Reel
KW47B42ZB2AFTBT	Bluetooth 6.0	2 MB + 512 KB	264 KB + 171 KB	No	7x7 48-pin HVQFN "Wettable"	No	AEC-Q100 Grade 2	Tray
KW47B42ZB2AFTBR	Bluetooth 6.0	2 MB + 512 KB	264 KB + 171 KB	No	7x7 48-pin HVQFN "Wettable"	No	AEC-Q100 Grade 2	Tape and Reel
KW47B42Z83AFTBT	Bluetooth 6.0	1 MB + 512 KB	136 KB + 171 KB	No	7x7 48-pin HVQFN "Wettable"	Yes	AEC-Q100 Grade 2	Tray
KW47B42Z83AFTBR	Bluetooth 6.0	1 MB + 512 KB	136 KB + 171 KB	No	7x7 48-pin HVQFN "Wettable"	Yes	AEC-Q100 Grade 2	Tape and Reel

[1] To confirm current availability of orderable part numbers, go to http://www.nxp.com and perform a part number search.

[2] Devices with prefix "P" are pre-qualification devices. Fully qualified general market flow devices will not include this "P" prefix.

Table 2. Ordering information of non-radio parts [1],[2]

Part number	FLASH (KB)	SRAM (KB)	LCE	Package/Pin Count	CAN	Qualification	Packaging Type
KW47Z420B3AFTBR	2 MB + 512 KB	264 KB + 171 KB	No	7x7 48-pin HVQFN "Wettable"	Yes	AEC-Q100 Grade 2	Tape and Reel
KW47Z420B3AFTBT	2 MB + 512 KB	264 KB + 171 KB	No	7x7 48-pin HVQFN "Wettable"	Yes	AEC-Q100 Grade 2	Tray
KW47Z420B2AFTBR	2 MB + 512 KB	264 KB + 171 KB	No	7x7 48-pin HVQFN "Wettable"	No	AEC-Q100 Grade 2	Tape and Reel
KW47Z420B2AFTBT	2 MB + 512 KB	264 KB + 171 KB	No	7x7 48-pin HVQFN "Wettable"	No	AEC-Q100 Grade 2	Tray
KW47Z42092AFTBR	1 MB + 512 KB	264 KB + 171 KB	No	7x7 48-pin HVQFN "Wettable"	No	AEC-Q100 Grade 2	Tape and Reel
KW47Z42092AFTBT	1 MB + 512 KB	264 KB + 171 KB	No	7x7 48-pin HVQFN "Wettable"	No	AEC-Q100 Grade 2	Tray
KW47Z42082AFTBR	1 MB + 512 KB	136 KB + 171 KB	No	7x7 48-pin HVQFN "Wettable"	No	AEC-Q100 Grade 2	Tape and Reel
KW47Z42082AFTBT	1 MB + 512 KB	136 KB + 171 KB	No	7x7 48-pin HVQFN "Wettable"	No	AEC-Q100 Grade 2	Tray

[1] To confirm current availability of orderable part numbers, go to http://www.nxp.com and perform a part number search.
[2] Devices with prefix "P" are pre-qualification devices. Fully qualified general market flow devices will not include this "P" prefix.

Note:

- *In case of Tray 7x7 48-pin HVQFN "Wettable" - Minimum Package Quantity is 260 pcs*
- *In case of Tape and Reel 7x7 48-pin HVQFN "Wettable" - Minimum Package Quantity is 2 kpcs*

Table 3. Device revision number

Device Mask Set Number	SIM_SDID[REVID]
3P57K	2b'11

Table 4. Related resources

Type	Description	Resource
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KW47RM
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	KW47
Security Reference Manual	The Security Reference Manual contains a comprehensive description of the security architecture and function of a device.	KW47SRM
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KW47_3P57K

Table continues on the next page...

Table 4. Related resources *...continued*

Type	Description	Resource
Package drawing	Package dimensions are provided in package drawings.	48 HVQFN:SOT619-17(DD)

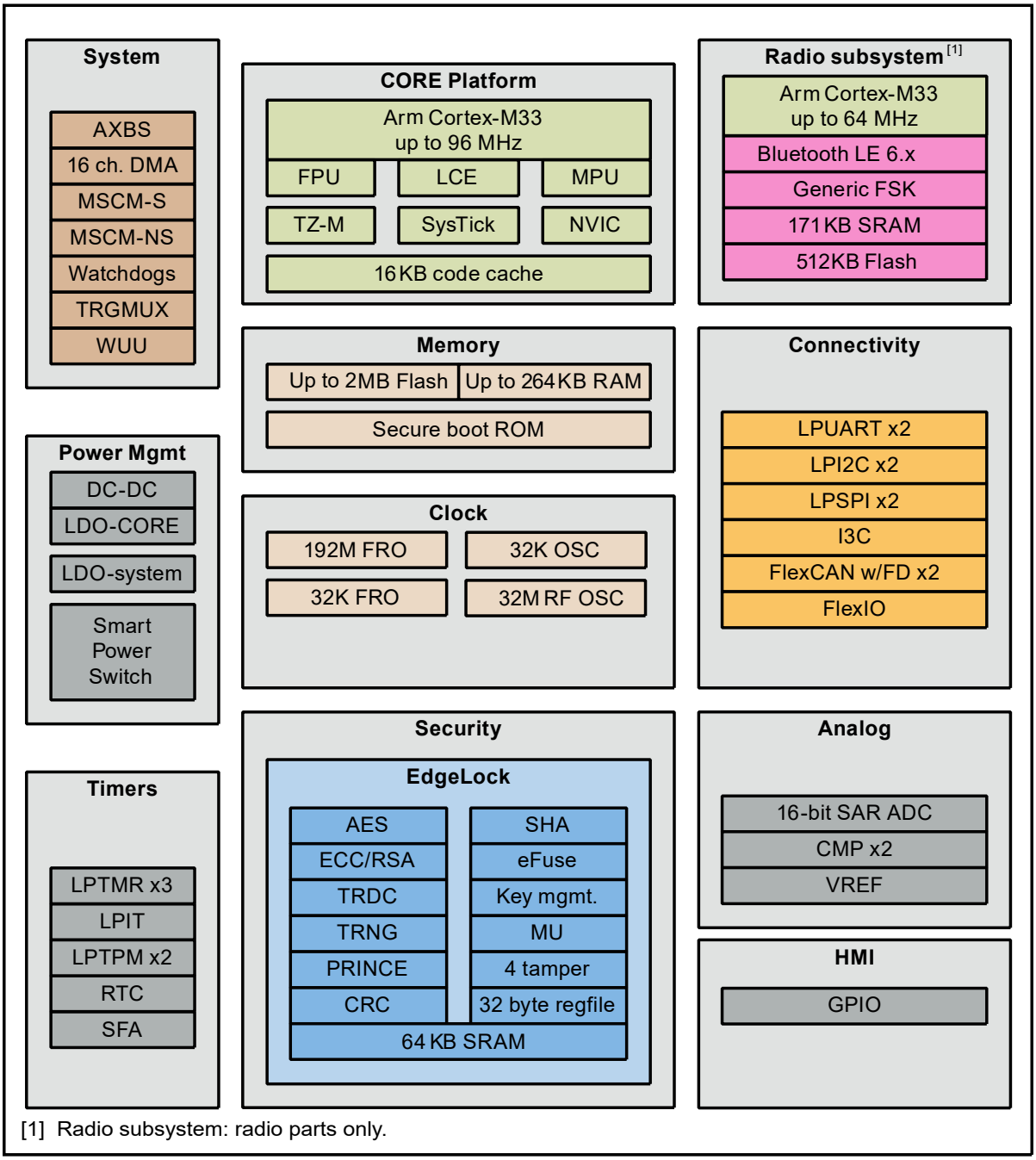


Figure 1. KW47 block diagram

1 Ratings

1.1 Thermal handling ratings

Table 5. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	-55	150	°C	[1]
T_{SDR}	Solder temperature, lead-free	—	260	°C	[2]

[1] Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
[2] Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Table 6. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	[1]

[1] Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD and Latch-Up ratings

Table 7. ESD and Latch-Up ratings

Description	Rating	Notes
Electrostatic discharge voltage, human body model	±2000 V	[1]
Electrostatic discharge voltage, charged-device model	±500 V	[2]
Latch-up immunity level (Class II at 125 °C junction temperature)	Immunity Level A	[3]

[1] Determined according to JEDEC Standard JS-001-2023, *For Electrostatic Discharge (ESD) Sensitivity Testing, Human Body Model (HBM) - Component Level*.
[2] Determined according to JEDEC Standard JS-002-2022, *For Electrostatic Discharge (ESD) Sensitivity Testing, Charged-Device Model (CDM) - Device Level* .
[3] Determined according to JEDEC Standard JESD78F, *IC Latch-Up Test*.

1.4 Voltage and current maximum ratings

Table 8. Voltage and current maximum ratings

Symbol	Description	Min.	Max.	Unit
VDD_CORE	Supply voltage for most digital domains	-0.3	1.26	V
VDD_SYS	Supply voltage for PMC, EFUSE, SRTC, and FROs	-0.3	1.98 [1]	V
VDD_DCDC	Supply voltage for DCDC regulator	-0.3	3.63	V
VDD_IO_D	Supply voltage for LDO_SYS regulator, and PortD	-0.3	3.63	V
VDD_LDO_CORE	Supply voltage for LDO_CORE regulator	-0.3	3.63	V
VDD_RF	Supply voltage for OSC and radio analog	-0.3	3.6	V

Table continues on the next page...

Table 8. Voltage and current maximum ratings...*continued*

Symbol	Description	Min.	Max.	Unit
VPA_2P4GHZ	Supply voltage for 2.4 GHz radio power amplifier	-0.3	2.8	V
VDD_IO_ABC	Supply voltage for Port A, Port B, Port C, Flash and CMP0/1	-0.3	3.63	V
VDD_ANA	Supply voltage for ADC, DAC, and VREF	-0.3	3.63	V
V_{IN}	Port input voltage	-0.3	3.63 [2]	V
I_D	Maximum current single pin limit (digital output pins)	-25	25	mA
VOUT_SWITCH	Smart power switch output voltage	1.78 [3]	3.6[3]	V

[1] The part supports 2.75 V for up to 20 s over lifetime to allow fuse programming.
[2] The Max. of the V_{IN} cannot be greater than the voltage applied to the VDD_IO_*x*.
[3] Current loading is less than 40 mA.

1.5 Required Power-On-Reset (POR) sequencing

When VDD_CORE is supplied by one of the internal regulators, VDD supply inputs can be powered up in any order. VDD supply inputs on power-up must not exceed VDD voltage maximums.

When powering VDD_CORE with an external supply, VDD_CORE must not be enabled until VDD_IO_ABC ≥ 1.65 V, as shown below.

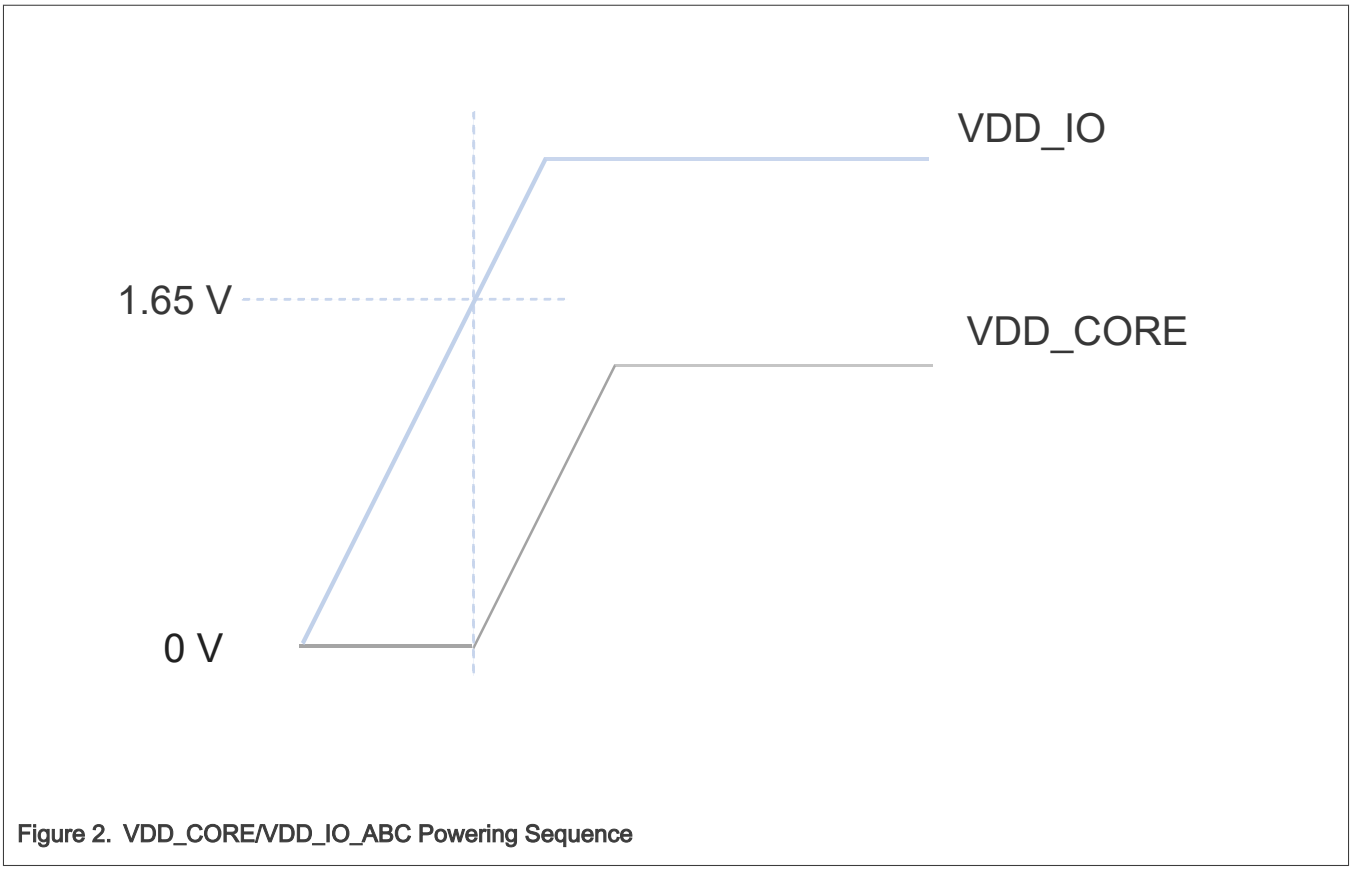


Figure 2. VDD_CORE/VDD_IO_ABC Powering Sequence

1.6 Power sequence

Table 9. Power sequence

Symbol	Description	Order in sequence	Notes
VDD_SWITCH	Smart Power Switch input	1	[1]
VDD_DCDC/ VDD_IO_D	DCDC / PORT D / LDO_SYS regulator input	2	[1]
VDD_IO_ABC	Ports A, B, and C power rail input	2	[1]
VDD_ANA	Analog source input	2	[1]
VDD_LDO_CORE	Core power rail input	2	[1]
VDD_RF	RF power rail input	3	[1]
VPA_2P4GHz	RF PA voltage input	4	[1]

[1] All domains can be powered at the same time. If external sources are used, make sure they start at the same time or they follow the order in the sequence.

2 General

2.1 AC electrical characteristics

Unless specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

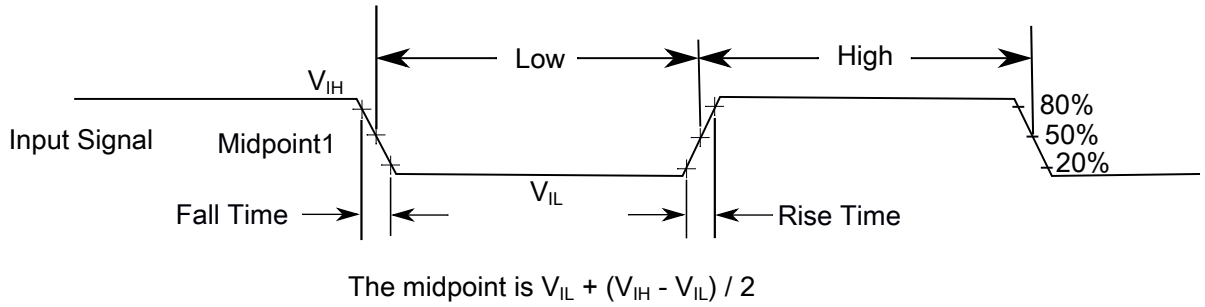


Figure 3. Input signal measurement reference

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 10. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
VDD_CORE	VDD_CORE input supply voltage			V	—
	Mid Drive (1.05 V) Operation	1.0	1.1		
	Normal Drive (1.1 V) Operation	1.045	1.15		

Table continues on the next page...

Table 10. Voltage and current operating requirements...*continued*

Symbol	Description	Min.	Max.	Unit	Notes
VDD_SYS	Supply voltage for System Voltage Domain • Normal mode • Fuse Programming	1.71 2.25	1.98 2.75	V	—
VDD_DCDC	Supply voltage DCDC regulator	1.86	3.6	V	—
VDD_IO_D	Supply voltage for LDO_SYS regulator, PortD	1.86	3.6	V	—
VDD_LDO_CORE	Supply voltage for LDO_CORE regulator	1.25	3.6	V	—
VDD_RF	Supply voltage for OSC and radio analog	1.187	3.6	V	—
VPA_2P4GHz	Supply voltage for 2.4 GHz radio power amplifier	0.9	2.4	V	—
VDD_IO_ABC	Supply voltage for PortA, PortB, Port C, and CMPs	1.71	3.6	V	[1]
VDD_ANA	Supply voltage for ADC, DAC, and VREF	1.71	3.6	V	—
VSS - VSS_ANA	VSS-to-VSS_ANA differential voltage	–0.1	0.1	V	—
V_{IH}	Input high voltage • 1.71 V ≤ VDD_IO_ABC ≤ 3.6 V • 1.86 V ≤ VDD_IO_D ≤ 3.6 V	0.7 × VDD_IO_ABC 0.7 × VDD_IO_D	— —	V	[2]
V_{IL}	Input low voltage • 1.71 V ≤ VDD_IO_ABC ≤ 3.6 V • 1.86 V ≤ VDD_IO_D ≤ 3.6 V	— —	0.3 × VDD_IO_ABC 0.3 × VDD_IO_D	V	[2]
V_{HYS}	Input hysteresis	0.1 × VDD_IO_*X*	—	V	—
I_{ICIO}	IO pin DC injection current — single pin • V_{IN} < VSS – 0.3 V (negative current injection) • V_{IN} > VDD + 0.3 V (positive current injection)	0 —	— 0	mA	[3], [4]
V_{ODPU}	Open drain pullup voltage level	VDD_IO_*X*	VDD_IO_*X*	V	[5]

[1] If none of the PortA, PortB, and PortC pins are being used, then the VDD_IO_ABC can be left floating.
[2] VIH and VIL for PTD0 are based of VDD_SYS instead of VDD_IO_D.
[3] All I/O pins are internally clamped to VSS and VDD_IO_*x* through an ESD protection diode. If V_{IN} is greater than VDD_IO_x_MIN(= VSS – 0.3 V) or is less than VDD_IO_x_MAX(= VDD + 0.3 V), then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed, then a current limiting resistor is required.
[4] This device does not allow pin injection current. User must ensure that VIN is kept within the Voltage Maximum Ratings.
[5] Open drain outputs must be pulled to whichever supply voltage corresponds to that IO, VDD_IO_*X* as appropriate.

2.2.2 HVD, LVD, and POR operating requirements

The device includes Low-Voltage Detection (LVD) and High-Voltage Detection (HVD) power supervisor circuits for following power supplies:

- VDD_IO_ABC
- VDD_CORE
- VDD_SYS

For VDD_SYS, it has Power-On-Reset (POR) power supervisor circuits.

Table 11. VDD_IO_ABC supply HVD, LVD, and POR Operating Ratings

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{HVDH\_IO\_ABC}$	VDD_IO_ABC Rising high-voltage detect threshold	3.730	3.810	3.890	V	—
$V_{HVDH\_HYS\_IO\_ABC}$	VDD_IO_ABC High-voltage inhibit reset/recover hysteresis	—	38	—	mV	—
$V_{LVDH\_IO\_ABC}$	VDD_IO_ABC Falling low-voltage detect threshold - high range	2.567	2.619	2.673	V	—
$V_{LVDH\_HYS\_IO\_ABC}$	VDD_IO_ABC Low-voltage inhibit reset/recover hysteresis - high range	—	27	—	mV	—
$V_{LVDL\_IO\_ABC}$	VDD_IO_ABC Falling low-voltage detect threshold - low range	1.618	1.651	1.684	V	—
$V_{LVDV\_HYS\_IO\_ABC}$	VDD_IO_ABC Low-voltage inhibit reset/recover hysteresis - low range	—	20	—	mV	—

Table 12. VDD_CORE supply HVD and LVD Operating Ratings

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{HVD_CORE}	VDD_CORE Rising high-voltage detect threshold (HVD assertion) Target VDD_CORE = 1.05 V Target VDD_CORE = 1.1 V	 1.230 1.230	 1.257 1.257	 1.285 1.285	V	[1]
$V_{HVD\_HYS\_CORE}$	VDD_CORE High-voltage inhibit reset/recover hysteresis Target VDD_CORE = 1.05 V Target VDD_CORE = 1.1 V	 — —	 14 14	 — —	mV	[1]
V_{LVD_CORE}	VDD_CORE Falling low-voltage detect threshold (LVD assertion) Target VDD_CORE = 1.05 V Target VDD_CORE = 1.1 V	 0.944 0.989	 0.963 1.009	 0.983 1.029	V	—
$V_{LVD\_HYS\_CORE}$	VDD_CORE Low-voltage inhibit reset/ recover hysteresis				mV	—

Table continues on the next page...

Table 12. VDD_CORE supply HVD and LVD Operating Ratings...*continued*

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Target VDD_CORE = 1.05 V	—	14	—		
	Target VDD_CORE = 1.1 V	—	14	—		

[1] Same value applies to all conditions.

Table 13. VDD_SYS supply HVD and LVD Operating Ratings

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{HVD_SYS}	VDD_SYS Rising high-voltage detect threshold (HVD assertion) Target VDD_SYS = 1.8 V	2.035	2.077	2.120	V	[1]
$V_{HVD\_HYS\_SYS}$	VDD_SYS High-voltage inhibit reset/recover hysteresis	—	22	—	mV	—
V_{POR_SYS}	Falling VDD_SYS POR detect voltage (POR assertion)	0.8	1.0	1.5	V	—
V_{LVD_SYS}	VDD_SYS Falling low-voltage detect threshold (LVD assertion) Target VDD_SYS = 1.8 V	1.616	1.649	1.683	V	—
$V_{LVD\_HYS\_SYS}$	VDD_SYS Low-voltage inhibit reset/recover hysteresis	—	19	—	mV	—
V_{BG}	Bandgap voltage reference voltage	—	1.0	—	V	—

[1] When fuses are being programmed VDD_SYS is raised to 2.5 V nominal. This is outside the HVD bounds, so HVD detection for VDD_SYS must be disabled when programming fuses.

2.2.3 Voltage and current operating behaviors

Table 14. Voltage and current operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive strength • 2.7 V ≤ VDD_IO_*X* ≤ 3.6 V, I_{OH} = 3.5 mA • 1.71 V ≤ VDD_IO_ABC < 2.7 V, I_{OH} = 2 mA • 1.86 V ≤ VDD_IO_D < 2.7 V, I_{OH} = 2 mA	VDD_IO_*X* – 0.5 VDD_IO_*X* – 0.5 VDD_IO_*X* – 0.5	— — —	— — —	V	[1]
V_{OH}	Output high voltage — High drive strength • 2.7 V ≤ VDD_IO_*X* ≤ 3.6 V, I_{OH} = 5.5 mA • 1.71 V ≤ VDD_IO_ABC < 2.7 V, I_{OH} = 3.25 mA • 1.86 V ≤ VDD_IO_D < 2.7 V, I_{OH} = 3.25 mA	VDD_IO_*X* – 0.5 VDD_IO_*X* – 0.5	— — —	— — —	V	[1],[2]

Table continues on the next page...

Table 14. Voltage and current operating behaviors...*continued*

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
		VDD_IO_*X* – 0.5				
I_{OHT}	Output high current total for all ports	—	—	100	mA	—
V_{OL}	Output low voltage — Normal drive strength • 2.7 V ≤ VDD_IO_*X* ≤ 3.6 V, I_{OL} = 4 mA • 1.71 V ≤ VDD_IO_ABC < 2.7 V, I_{OL} = 2.5 mA • 1.86 V ≤ VDD_IO_D < 2.7 V, I_{OL} = 2.5 mA	— — —	— — —	0.5 0.5 0.5	V	[1],[3]
V_{OL}	Output low voltage — High drive strength • 2.7 V ≤ VDD_IO_*X* ≤ 3.6 V, I_{OL} = 6 mA • 1.71 V ≤ VDD_IO_ABC < 2.7 V, I_{OL} = 3.75 mA • 1.86 V ≤ VDD_IO_D < 2.7 V, I_{OL} = 3.75 mA	— — —	— — —	0.5 0.5 0.5	V	[1],[3],[2]
I_{OLT}	Output low current total for all ports	—	—	100	mA	—
I_{IN}	Input leakage current (per pin) for full temperature range	—	—	1	µA	[4]
I_{IN}	Input leakage current (per pin) at 25 °C	—	—	0.025	µA	[4]
I_{IN}	Input leakage current (total all pins) for full temperature range	—	—	41	µA	[4]
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	—	1	µA	—
R_{PU}	Internal pullup resistors	33	50	75	kΩ	—
R_{PU} (I3C)	Internal pullup resistors	1.1	2	2.833	kΩ	[5]
R_{PD}	Internal pulldown resistors	33	50	75	kΩ	—
R_{HPU}	High-resistance pullup option (PORTx_PCRy[PV] = 1)	0.67	—	1.5	MΩ	[6]
R_{HPD}	High-resistance pulldown option (PORTx_PCRy[PV] = 1)	0.67	—	1.5	MΩ	[6]

[1] When setting DSE1=1, the same VOH / VOL is met with IOH / IOL at 4x.
[2] RTC signals are always configured in high drive mode.
[3] Open drain outputs must be pulled to VDD_IO_*X*.
[4] Measured at VDD_IO_*X* = 3.6 V.
[5] Only I3C pins support this option.
[6] Only Port D pins support this option.

2.2.4 On-chip regulator electrical specifications

2.2.4.1 DCDC converter specifications

Table 15. DCDC Converter Specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD_DCDC}	DCDC input voltage	1.86	—	3.6	V	
V_{OUT_DCDC}	DCDC output voltage					[1], [2]
	1.25 V	1.1875	1.25	1.3125	V	
	1.35 V	1.2825	1.35	1.475	V	
	1.5 V	1.425	1.5	1.575	V	
	1.8 V	1.71	1.8	1.89	V	
	2.5 V	2.375	2.5	2.625	V	
I_{LOAD}	DCDC load current • Normal drive strength • Low drive strength • SPC_DCD_CFG[FREQ_CNTRL_ON]=1	 — — —	 — — —	 105 15 45	 mA mA mA	[1], [3]
LX	DCDC inductor value	0.8	1,1.5,2.2	2.65	µH	[4]
ESR	External inductor equivalent series resistance	—	110	—	mΩ	[5]
C_{OUT}	DCDC capacitance value	6	22	30	µF	[6], [7]
V_{RIPPLE}	DCDC voltage ripple • In normal drive strength • In low drive strength	 — —	 1 25	 — —	 % mV	—
f_{burst}	DCDC burst frequency	3	5	8	MHz	[8]
f_{burst_acc}	DCDC burst frequency accuracy	—	10	—	%	[8]

[1] The system DCDC converter generates 1.8 V at DCDC_LX by default. The DCDC can be used to power VDD_RF, VDD_LDO_CORE, and external components as long as the max I_{LOAD} is not exceeded.
[2] The VDD_DCDC input supply to DCDC must be at least 500 mV higher than the desired output at DCDC_LX.
[3] The maximum load current during boot up shall not exceed 60 mA.
[4] Recommended inductor value is 1 µH to 1.5 µH. If the inductor is < 1 µH, the DCDC efficiency is not guaranteed.
[5] The maximum recommended ESR is 250 mΩ (not a hard limit).
[6] The variation in capacitance of the capacitor at DCDC_LX due to aging, temperature, and voltage degradation must not exceed the Min./Max. values.
[7] Cout DCDC capacitance value parameter represents the total capacitance reflected on the DCDC low pass filter. In some configurations, the DCDC output supplies other power rails like VDD_RF, VDD_LDO_CORE and external components. The sum of all parallel capacitances of power rails, external components, and the DCDC low pass filter capacitor itself are included as part of Cout specification.
[8] FREQ_CNTRL_ON = 1.

2.2.4.2 LDO_SYS electrical specifications

Table 16. LDO_SYS electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VDD_IO_D	LDO_SYS input supply voltage				V	[1]

Table continues on the next page...

Table 16. LDO_SYS electrical specifications*...continued*

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• LDO_SYS input supply voltage (Regulation mode) • LDO_SYS input supply voltage (Bypass mode) • Fuse programming mode	1.86 1.8 2.75	— — —	3.6 1.98 3.6		
VOUT_SYS	LDO_SYS regulator output voltage • Normal drive mode • Fuse Programming mode	 1.71 2.25	 1.8 2.5	 1.98 2.75	V	[2],[3],[4],[5]
I_{LOAD}	LDO_SYS maximum load current • Normal drive mode • Low drive mode • Fuse programming mode	 — — —	 — — —	 50 2 40	 mA mA mA	—
I_{DD}	LDO_SYS power consumption • Normal drive mode • Low drive mode	 — —	 100 70	 — —	 µA nA	[6]
C_{OUT}	External output capacitor	—	1.5	10	µF	—
C_{DEC}	External output decoupling capacitor	—	0.1	—	µF	—
ESR	External output capacitor equivalent series resistance	—	30	—	mΩ	—
I_{INRUSH}	LDO_SYS inrush current	—	—	120	mA	[7]

[1] Regulator will automatically switch to passthrough (means the regulator driver is fully ON) with the supply is below 1.95 V.
[2] The LDO_SYS converter generates 1.8 V by default at VOUT_SYS. VOUT_SYS can be used to power VDD_SYS, VDD_RF, VDD_IO_*X*, VDD_ANA, and external components as long as the max I_{LOAD} is not exceeded.
[3] VOUT_SYS and VDD_SYS are connected together.
[4] VDD_IO_D must be at least 150 mV higher than the desired VOUT_SYS.
[5] LDO_SYS can be used to program efuse and in this configuration the output voltage can range between 2.25 V and 2.75 V.
[6] In normal drive strength, LDO_SYS draws ~100 µA for every 20 mA of load current.
[7] This is for 1.5 µF external output capacitor. If the capacitor has 10 µF value, this value should be 300 mA instead.

2.2.4.3 LDO_CORE electrical specifications

Table 17. LDO_CORE electrical specifications

Symbol	Description	Conditions	Min	Typ	Max	unit	Notes
VDD_LDO_CORE	LDO_CORE input supply voltage	—	1.25	—	3.6	V	[1]
VOUT_CORE	LDO_CORE regulator output voltage	—	—	—	—	—	[2]
	Normal drive strength	—	—	—		—	

Table continues on the next page...

Table 17. LDO_CORE electrical specifications*...continued*

Symbol	Description	Conditions	Min	Typ	Max	unit	Notes
	• Mid voltage	1.0	1.05	1.1		V	
	• Normal voltage	1.045	1.1	1.15		V	
	Low drive strength	—	—	—		—	
	• Mid Voltage	1.0	1.05	1.1		V	
	• Normal Voltage	1.045	1.1	1.15		V	
VDROP_OUT	Drop out voltage	Tj = 25C	—	0.20	—	V	[3]
ILOAD	**LDO_CORE max load current**	—	—	—			—
	• Normal drive strength	0.20 V < VDROP_OUT < 0.4 V			40	mA	
		VDROP_OUT > 0.4 V			60	mA	
	• Low drive strength	0.20 V < VDROP_OUT < 0.4 V			18	mA	
		VDROP_OUT > 0.4 V			28	mA	
IINRUSH	—	—	—	—	500	mA	[4]

[1] To bypass LDO_CORE, tie VDD_LDO_CORE to VDD_CORE.
[2] VOUT_CORE and VDD_CORE are connected together in package .
[3] V_{DROP_OUT} is the difference between the minimum LDO input supply VDD_LDO_CORE that can be applied and output VOUT_CORE before regulator stops regulating .
[4] This value is for 4.7 uF external output capacitor. This value would increase with higher load capacitor.

Table 18. LDO_CORE external device electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
C_{OUT}	External output capacitor	3.7	4.7	10	µF	—
C_{DEC}	External output decoupling capacitor	—	0.1	—	µF	—
ESR	External output capacitor equivalent series resistance	—	10	—	mΩ	—

2.2.5 Smart power switch

Note: *SWITCH_WAKEUP_B pad is internally pulled up to the switch input through a resistor, it can be pulled down to wake up the smart power switch. To generate a valid internal wake-up signal successfully, maximum value of SWITCH_WAKEUP_B pulldown voltage is 0.7 V, duration time should be larger than 1 µs.*

Table 19. Smart power switch

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{supply}	Input voltage (VDD_SWITCH)	1.9	—	3.6	V	—
R_{ON}	Switch resistor at 'ON' state	—	—	3	Ω	—
I_{load}	Load current	—	—	40	mA	—
$I_{leakage1}$	Typical leakage current when Vsupply = 2.7 V, 25 °C	—	4	—	nA	—
$I_{leakage2}$	Maximum leakage current when Vsupply = 3.3 V	—	—	1	µA	—

Note: *If battery (with peak current limitation) is used to power VDD_SWITCH which power rest of chip supplies, it is not recommended to go to deep-power-down mode constantly. Because DCDC startup will introduce big peak current when wakeup.*

2.2.6 Power mode transition operating behaviors

All specifications in the following table assume that the default clock configuration will be 96 MHz CPU_CLK/BUS_CLK and 24 MHz slow clock.

Table 20. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time to execution of the first instruction (measured from the point where VDD and VDD_SYS reach 1.8 V) across the operating temperature range of the chip.	—	4.75	—	ms	[1],[2] ,[3]
t_{SLEEP}	SLEEP → ACTIVE	—	7.72	—	µs	[2],[4]
t_{DSLEEP}	DEEP SLEEP → ACTIVE	—	8.73	—	µs	[2],[4]
t_{PWDN}	POWER DOWN → ACTIVE	—	158.20	—	µs	[2],[4],[3]
t_{DPWDN}	Deep Power DOWN → ACTIVE	—	707.47	—	µs	[2],[4],[3]

[1] Boot Configuration at 96 Mhz.
[2] Based on characterization. Not tested in production.
[3] ROM configured for low power wake up path.
[4] WFE used for low power entry.

2.2.7 Power consumption operating behaviors

The KW47B42Z device has multiple power supplies that can be connected in different configurations, where the total current consumption of the device is the accumulative result of each individual power supply's current consumption. When in LDO mode, the device is supplied with a power supply of 3.3 V. The power supply is connected to VDD_IO_ABC, VDD_IO_D/VDD_DCDC, VDD_RF, VDD_ANA, VDD_LDO_CORE and VDD_SWITCH. When in DCDC mode, the device is supplied with a power supply of 3.3 V. The power supply is connected to VDD_IO_ABC, VDD_IO_D/VDD_DCDC, VDD_ANA, and VDD_SWITCH. The DCDC output is connected to VDD_LDO_CORE and VDD_RF power rails.

When calculating the total MCU current consumption, the following considerations should be made:

- Specifications below only include power for the MCU itself
- On top of the device’s IDD current consumption, external loads applied to pins of the device need to be considered
- Efficiency of regulators (on-chip or off-chip) used to generate supply voltages should be considered

2.2.7.1 Power consumption operating behaviors

Table 21. LDO mode configuration power consumption table

LDO mode configuration power consumption table					
Symbol	Description	Temperature (°C),Tj	Typ[1]	Unit	Notes
IDD_ACT_CM1	CoreMark executing on Main Core and NBU Core from Flash, LCE executing matrix multiplication; Cache enabled. Main core clocked at 96 MHz and NBU Core clocked at 64 MHz. All peripheral clocks enabled.	25 105 125	40 50 56.3	mA	[2]
IDD_ACT_CM2	CoreMark executing on Main Core and NBU Core from Flash; Cache enabled. Main core clocked at 48 MHz and NBU Core clocked at 32 MHz. All peripheral clocks disabled.	25 105 125	9.2 16.7 22.5	mA	[2]
IDD_ACT_CM_DS1	CoreMark executing on Main Core from Flash; Cache enabled. Main core clocked at 96 MHz. NBU Core in Deep Sleep mode, no RAM retained. All peripheral clocks disabled.	25 105 125	11.1 17.7 22.7	mA	[2]
IDD_ACT_CM_DS2	CoreMark executing on Main Core from Flash; Cache enabled. Main core clocked at 48 MHz. NBU Core in Deep Sleep mode, no RAM retained. All peripheral clocks disabled.	25 105 125	6.1 12 16.5	mA	[2]
IDD_ACT_DS_CM1	CoreMark executing on NBU Core from Flash; Cache enabled. NBU core clocked at 64 MHz. Main Core in Deep Sleep mode, no RAM retained. All peripheral clocks disabled.	25 105 125	6.2 8 9.4	mA	[2]
IDD_ACT_DS_CM2	CoreMark executing on NBU Core from Flash; Cache enabled. NBU core clocked at 32 MHz. Main Core in Deep Sleep mode, all RAM retained. All peripheral clocks disabled.	25 105 125	3 4.9 6.2	mA	[2]
IDD_SLEEP	Core_Main in Sleep, Core_Wake in Sleep, Core_Radio in Deep Sleep. All RAM retained. Core voltage at 1.0 V. Main core clocked at 96 MHz.	25 105 125	302 5.6 10.1	µA mA mA	—
IDD_DS1	Core_Main in Deep Sleep, Core_Wake in Sleep, Core_Radio in Deep Sleep. All RAM retained. Core voltage at 1.0 V.	25 105 125	16.1 342 718	µA	—

Table continues on the next page...

Table 21. LDO mode configuration power consumption table...*continued*

LDO mode configuration power consumption table					
Symbol	Description	Temperature (°C),Tj	Typ[1]	Unit	Notes
IDD_DS2	Core_Main in Deep Sleep, Core_Wake in Deep Sleep, Core_Radio in Deep Sleep. All RAM retained. Core voltage at 1.0 V.	25 105 125	8.2 202 463	µA	—
IDD_PD_DS1	Core_Main in Power Down, Core_Wake in Power Down, Core_Radio in Deep Sleep. No RAM retained. Core voltage at 1.0 V.	25 105 125	2.8 29 67	µA	—
IDD_PD_DS2	Core_Main in Power Down, Core_Wake in Sleep, Core_Radio in Deep Sleep. 48 kB RAM retained. Core voltage at 1.0 V.	25 105 125	12.4 237 478	µA	—
IDD_DPD1	Core_Main in Deep Power Down, Core_Wake in Deep Power Down, Core_Radio in Deep Power Down. No RAM retained. Core voltage at 1.0 V.	25 105 125	1.1 11.1 26	µA	—

[1] Based on characterization of typical units. Not tested in production.
[2] In order to reach App Core frequency of 96 MHz, CORELDO_VDD_LVL must be programmed to 1.1 V. Otherwise, CORELDO_VDD_LVL is 1.05 V.

Note: *Refer to Thermal specifications for formula to calculate Ta from Tj.*

Table 22. DCDC mode configuration power consumption table

DCDC Mode Configuration Power Consumption Table					
Symbol	Description	Temperature (°C),Tj	Typ[1]	Unit	Notes
IDD_ACT_CM1	CoreMark executing on Main Core and NBU Core from Flash, LCE executing matrix multiplication; Cache enabled. Main core clocked at 96MHz and NBU Core clocked at 64 MHz. All peripheral clocks enabled.	25 105 125	26.3 31.5 35.7	mA	[2],[3]
IDD_ACT_CM2	CoreMark executing on Main Core and NBU Core from Flash; Cache enabled. Main core clocked at 48MHz and NBU Core clocked at 32 MHz. All peripheral clocks disabled.	25 105 125	5 7.9 10.6	mA	[2],[4]
IDD_ACT_CM_DS1	CoreMark executing on Main Core from Flash; Cache enabled. Main core clocked at 96 MHz. NBU Core in Deep Sleep mode, no RAM retained. All peripheral clocks disabled.	25 105 125	7.5 11.3 14.5	mA	[2],[3]
IDD_ACT_CM_DS2	CoreMark executing on Main Core from Flash; Cache enabled. Main core clocked	25 105	3.5 5.8	mA	[2],[4]

Table continues on the next page...

Table 22. DCDC mode configuration power consumption table...*continued*

DCDC Mode Configuration Power Consumption Table					
Symbol	Description	Temperature (°C),Tj	Typ[1]	Unit	Notes
	at 48 MHz. NBU Core in Deep Sleep mode, no RAM retained. All peripheral clocks disabled.	125	7.9		
IDD_ACT_DS_CM1	CoreMark executing on NBU Core from Flash; Cache enabled. NBU core clocked at 64 MHz. Main Core in Deep Sleep mode, no RAM retained. All peripheral clocks disabled.	25 105 125	4.4 5.4 6.2	mA	[2],[3]
IDD_ACT_DS_CM2	CoreMark executing on NBU Core from Flash; Cache enabled. NBU core clocked at 32 MHz. Main Core in Deep Sleep mode, all RAM retained. All peripheral clocks disabled.	25 105 125	2 2.7 3.3	mA	[2],[4]
IDD_SLEEP	Core_Main in Sleep, Core_Wake in Sleep, Core_Radio in Deep Sleep. All RAM retained. Core voltage at 1.0 V. Main core clocked at 96 MHz.	25 105 125	146 2.3 4.2	µA mA mA	—
IDD_DS1	Core_Main in Deep Sleep, Core_Wake in Sleep, Core_Radio in Deep Sleep. All RAM retained. Core voltage at 1.0 V.	25 105 125	8.3 137 291.5	µA	—
IDD_DS2	Core_Main in Deep Sleep, Core_Wake in Deep Sleep, Core_Radio in Deep Sleep. All RAM retained. Core voltage at 1.0 V.	25 105 125	4.7 81.2 186.3	µA	—
IDD_PD_DS1	Core_Main in Power Down, Core_Wake in Power Down, Core_Radio in Deep Sleep. No RAM retained. Core voltage at 1.0 V.	25 105 125	2.2 15.7 36.2	µA	—
IDD_PD_DS2	Core_Main in Power Down, Core_Wake in Sleep, Core_Radio in Deep Sleep. 48 kB RAM retained. Core voltage at 1.0 V.	25 105 125	6.8 98 200.4	µA	—
IDD_DPD1	Core_Main in Deep Power Down, Core_Wake in Deep Power Down, Core_Radio in Deep Power Down. No RAM retained. Core voltage at 1.0 V.	25 105 125	0.9 8.3 19.6	µA	—

[1] Based on characterization of typical units. Not tested in production.
[2] In order to reach App Core frequency of 96 MHz, CORELDO_VDD_LVL must be programmed to 1.1 V. Otherwise, CORELDO_VDD_LVL is 1.05 V.
[3] DCDC output configured at 1.8 V
[4] DCDC output configured at 1.25 V.

Note: *Refer to Thermal specifications for formula to calculate T_a from T_j.*

Table 23. Smart power switch

Symbol	Description	Temperature(°C),Tj	Typ [1]	Unit	Notes
IDD_SPS	Smart power switch with 8K SPS RAM retained	25 105 125	273 2.6 5.7	nA µA µA	—

[1] Based on characterization of typical units. Not tested in production.

Note: *Refer to Thermal specifications for formula to calculate T_a from T_j.*

2.2.8 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

2.2.9 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to https://www.nxp.com/.
2. Perform a keyword search for “EMC design”.

2.2.10 Capacitance attributes

Table 24. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 25. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
VDD_CORE = 1.1 V					
f_{CPU}	CPU clock (CPU_CLK)	—	96	MHz	—
f_{BUS}	Bus clock (BUS_CLK)	—	96	MHz	—
f_{SLOW}	Slow clock (SLOW_CLK)	—	24	MHz	—
VDD_CORE = 1.05 V					
f_{CPU}	CPU clock (CPU_CLK)	—	48	MHz	—
f_{BUS}	Bus clock (BUS_CLK)	—	48	MHz	—
f_{SLOW}	Slow clock (SLOW_CLK)	—	24	MHz	—

Note: *By default, VDD_CORE = 1.0 V, f_{CPU_CLK}/f_{BUS_CLK} = 32 MHz, f_{SLOW_CLK} = 16 MHz.*

2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO, LPUART, LPTMR, TPM, CAN, LPI2C, LPI3C, LPSPI, or FlexIO functions.

Table 26. General switching specifications

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (passive filter enabled) — Synchronous path	Largest of 1.5 and 150		AHB clock cycles	[1],[2]
GPIO pin interrupt pulse width (passive filter disabled) — Synchronous path	1.5		AHB clock cycles	[1], [2]
GPIO pin interrupt pulse width (passive filter enabled) — Asynchronous path	150		ns	[1], [3]
GPIO pin interrupt pulse width(passive filter disabled) — Asynchronous path	50		ns	[1], [3]
AON pins and I2C/I3C Pins interrupt pulse width (passive filter enabled) — Asynchronous path	330		ns	[1],[4]
AON pins and I2C/I3C Pins interrupt pulse width (passive filter disabled) — Asynchronous path	10		ns	[1]
Port rise/fall time				
Slow I/O and I2C/I3C pins • 2.7 ≤ VDD_IO_*x* ≤ 3.6 V — Fast slew rate (SRE = 0; DSE = 0) — Slow slew rate (SRE = 1; DSE = 0) • 1.71 ≤ VDD_IO_*x* < 2.7 V — Fast slew rate (SRE = 0; DSE = 1) — Slow slew rate (SRE = 1; DSE = 1)	 2.5 4.6 1.6 4.3	 7 15 7 20	 ns ns ns ns	[5],[6]
Fast I/O pins • 2.7 ≤ VDD_IO_*x* ≤ 3.6 V — Normal drive, fast slew rate (SRE = 0; DSE = 0) — Normal drive, slow slew rate (SRE = 1; DSE = 0) • 1.71 ≤ VDD_IO_*x* < 2.7 V — Normal drive, fast slew rate (SRE = 0; DSE = 1) — Normal drive, slow slew rate (SRE = 1; DSE = 1)	 0.8 0.9 0.5 0.6	 2 2.5 2 2.5	 ns ns ns ns	[7], [8]
AOI pins • 2.7 ≤ VDD_IO_*x* ≤ 3.6 V • 1.71 ≤ VDD_IO_*x* < 2.7 V	 3 3.6	 8 20	ns ns	[6]

[1] This is the shortest pulse that is guaranteed to be recognized.
[2] Synchronous path is used in active and sleep mode for pin functions other than WUU. Pins configured as WUU use asynchronous path in all power modes.
[3] Asynchronous path is used deep sleep, power down, and deep power down modes
[4] Passive filter is always enabled for RESET_PIN

[5] Load is 25 pF for DSE=0 or DSE=1. Load is 50 pF for DSE=2 or DSE=3. Drive strength and slew rate are configured using PORTx_PCRn[DSE1], PORTx_PCRn[DSE], and PORTx_PCRn[SRE].
[6] Load is 25 pF.
[7] Assumes default values in CALIB1 and CALIB0.
[8] Load is 15 pF.

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 27. Thermal operating requirements

Symbol	Description	Min.	Typical	Max.	Unit	Notes
T_A	Ambient temperature	-40	25	105	°C	[1]
T_J	Die junction temperature maximum	–	–	125	°C	[2],[3], [4],[5]

[1] The device may operate at maximum T_A rating as long as T_J maximum of 125 °C is not exceeded. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times$ chip power dissipation.
[2] The device operating specification is not guaranteed beyond 125 °C T_J.
[3] The maximum operating requirement applies to all chapters unless otherwise specifically stated.
[4] Operating at maximum conditions for extended periods may affect device reliability.
[5] The radio performances are guaranteed up to 105 °C. Above this temperature, parameters will gradually change.

2.4.2 Thermal attributes

Table 28. Thermal attributes

Rating	Board type[1]	Symbol	48 HVQFN	Unit
Junction to Ambient Thermal Resistance [2]	JESD51-7, 2s2p	$R_{\theta JA}$	30	°C/W
Junction-to-Top of Package Thermal Characterization Parameter [2]	JESD51-7, 2s2p	Ψ_{JT}	8.1	°C/W
Junction to Case Bottom Thermal Resistance [3]	NA	$R_{\theta JC}$	7.1	°C/W

[1] Thermal test board meets JEDEC specification for this package (JESD51-7).
[2] Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air).*
[3] Junction-to-Case thermal resistance determined using an isothermal cold plate. For QFN package, case temperature refers to the exposed pad surface temperature at the package bottom side dead centre.

3 Peripheral operating requirements and behaviors

3.1 Localization Compute Engine (LCE)

LCE is a localization processing engine with a generic DSP core. It features a 64-bit Single Instruction, Multiple Data (SIMD) data path optimized for high-throughput integer and floating-point operations, with native support for complex number arithmetic. The LCE operates independently from the application CPU during API execution. The DSP core sustains fast parallel operations, making LCE ideal for the advanced mathematical computations required for high-performance Bluetooth® Channel Sounding (CS) algorithms. By offloading these complex computations, the LCE significantly optimizes the overall system timing and power consumption for CS applications.

The LCE is supported by a high-bandwidth, 64-bit AXBS64 bus fabric connected to three memory banks, providing its vector processing unit with a dedicated, flexible data path that ensures minimal contention with the main system bus. This enables efficient management of large data sets simultaneous operations. The platform integrates a smart cache (SC) to maintain a local working set and includes a Messaging Unit (MU) block for streamlined communication and software abstraction with the application CPU.

The KW47 SDK includes a comprehensive vector math library and APIs that leverage the LCE's hardware capabilities. These libraries provide optimized functions for key operations of advanced Channel Sounding algorithms such as Fast Fourier Transform

(FFT), Eigenvalue Decomposition (EVD), and Hermitian matrix inverse. The user application on CPU manages the LCE RAM buffers and orchestrates the execution of these LCE APIs to perform the complete Channel Sounding processing chain.

3.2 Core modules

3.2.1 SWD electricals

Table 29. SWD timing

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	SWD_CLK frequency of operation	—	25	MHz
S2	SWD_CLK cycle period	1/S1	—	ns
S3	SWD_CLK clock pulse width	20	—	ns
S4	SWD_CLK rise and fall times	—	3	ns
S5	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
S6	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
S7	SWD_CLK high to SWD_DIO data valid	—	25	ns
S8	SWD_CLK high to SWD_DIO high-Z	5	—	ns

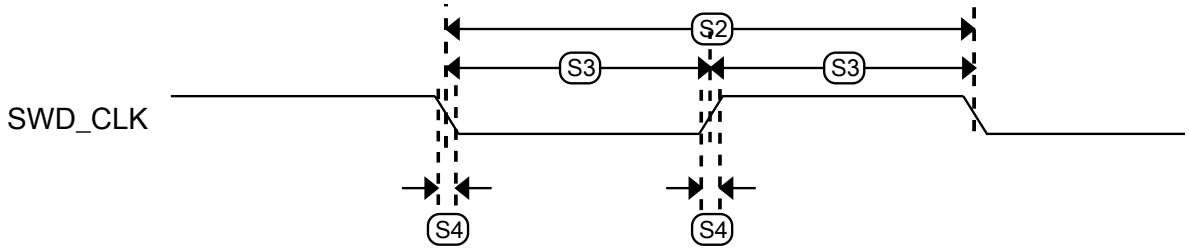


Figure 4. Serial wire clock input timing

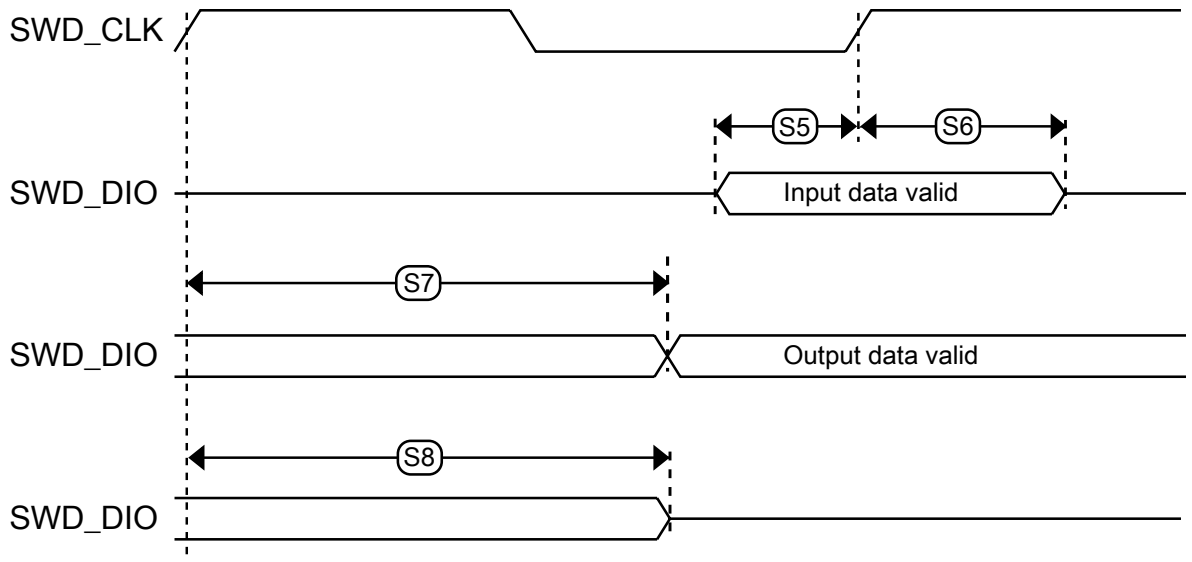


Figure 5. Serial wire data timing

3.3 Clock modules

3.3.1 Reference oscillator specification

This chip is designed to meet targeted specifications with a ±50 ppm frequency error over the life of the part, which includes the temperature, mechanical, and aging excursions.

The table below shows typical specifications for the Crystal Oscillator.

Table 30. Reference Crystal Specification

Symbol	Description	F0 = 32.0 MHz			Unit	Footnotes
		Min	Typ	Max		
T_A	Operating Temperature	-40	—	125	°C	[1]
	Crystal frequency tolerance over Aging and Temperature	-33	—	30	ppm	[2],[3]
	Oscillator variation	-17	—	20	ppm	[4]
	Total reference oscillator tolerance	-50	—	50	ppm	[5]
C_L	Load capacitance	—	6	—	pF	[2],[6]
C_0	Shunt capacitance	0.378	0.54	0.702	pF	[2],[6]
Cm1	Motional capacitance	0.819	1.17	1.521	fF	[2], [6]
Lm1	Motional inductance	14.77	21.1	27.43	mH	[2],[6]

Table continues on the next page...

Table 30. Reference Crystal Specification...*continued*

Symbol	Description	F0 = 32.0 MHz			Unit	Footnotes
		Min	Typ	Max		
ESR	Equivalent series resistance	—	—	60	Ohms	[2], [7]
P_d	Maximum crystal drive	—	—	200	µW	[2]
T_S	Trim sensitivity	9.94	14.2	18.64	ppm/pF	[2],[6]
T_{OSC}	Oscillator Startup Time	—	500	—	µs	[8]

[1] Full temperature range of this device. A reduced range can be chosen to meet application needs.
[2] Recommended crystal specification.
[3] Combination of frequency stability variation over desired temperature range and frequency variation due to aging over desired lifetime of system.
[4] Variation due to temperature, process, and aging of MCU.
[5] Sum of crystal initial frequency tolerance, crystal frequency stability and aging, oscillator variation, and PCB manufacturing variation must not exceed this value.
[6] Typical is target. 30% tolerances shown.
[7] ESR = Rm1 * (1 + [C_0/C_L])^2.
[8] Time from oscillator enables to clock ready. Dependent on the complete hardware configuration of the oscillator.

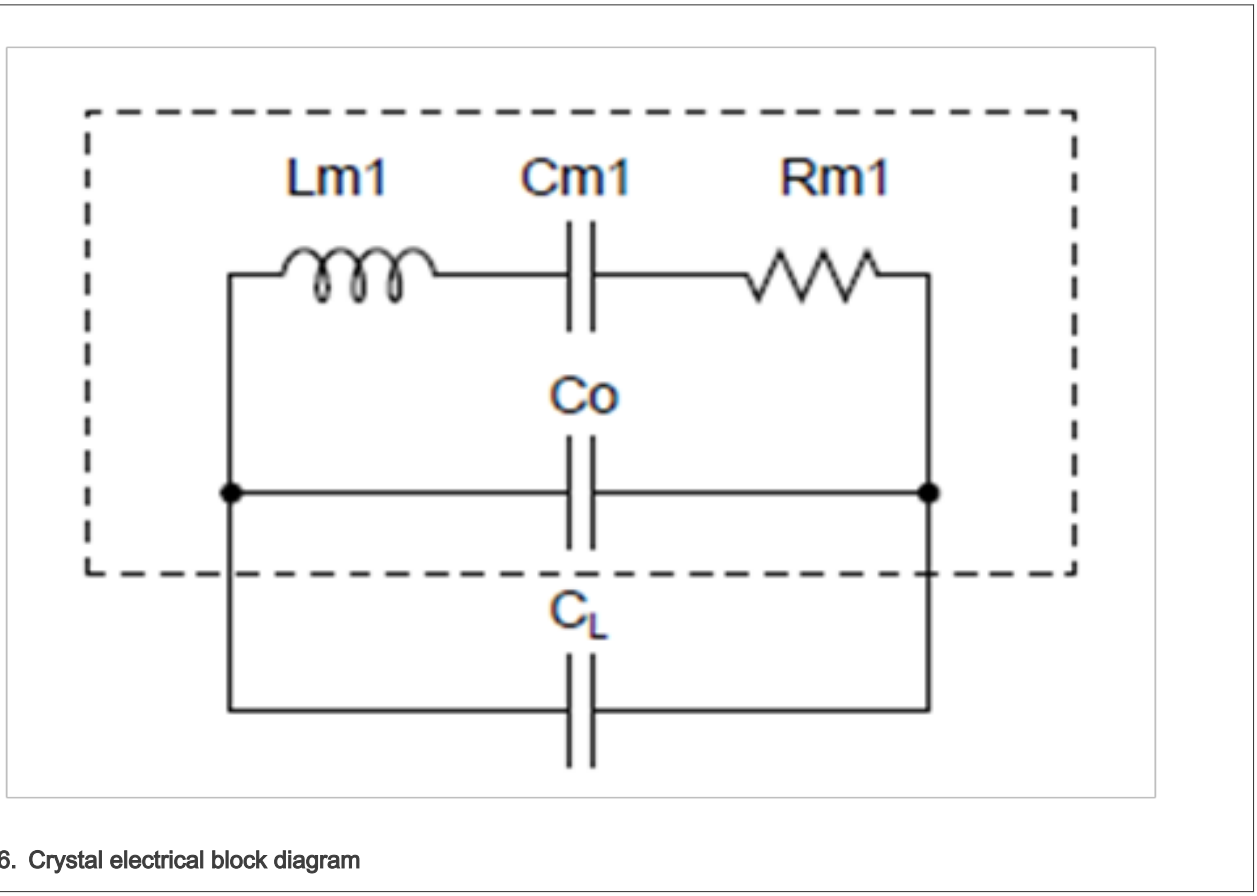


Figure 6. Crystal electrical block diagram

3.3.2 32 kHz oscillator electrical specifications

Table 31. 32 kHz oscillator electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_32k}	Crystal frequency	—	32.768	—	kHz	—
Tol	Frequency tolerance • Normal/Start up mode • Low power mode	—	±100 ±150	—	ppm	—
Jit_{osc}	Jitter • Period jitter (RMS) • Accumulated jitter over 1 ms (RMS)	— —	12000 8000	— —	ns	—
ESR	Crystal equivalent series resistance • Normal mode • Low power mode	— —	— —	100 50	kΩ	[1]
C_{para}	Parasitic capacitance of EXTAL32 and XTAL32	—	2.5	—	pF	—
t_{start}	Crystal start-up time • Normal/Start up mode • Low power mode	— —	1000 8000	— —	ms	[2]
I_{OSC_32k}	Current consumption • ON mode — Normal mode — Low power mode • OFF mode	 — — —	 220 110 0.5	 — — —	 nA	—
V_{pp}	Peak-to-peak amplitude of oscillation • Normal mode • Low power mode	— —	0.2 0.1	— —	V	[3]
$f_{ec\_extal32}$	Externally provided input clock frequency	—	32.768	—	kHz	[4]
$v_{ec\_extal32}$	Externally provided input clock amplitude	Refer to Voltage and Current operating requirements for V_{IH} and V_{IL} levels			mV	[4], [5]
$C_{extal/xtal}$	EXTAL, XTAL Load Capacitance	0	—	30	pF	[6]

[1] Maximum value is 80 kΩhms for parasitic capacitances higher than 1 pF, and 150 kOhms for parasitic capacitances around 1 pF.
[2] Proper PC board layout procedures must be followed to achieve specifications.
[3] When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.
[4] This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
[5] The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to $V_{DD\_IO\_D}$.
[6] With 2 pF steps.

Note: *It is recommended that the oscillator margin be measured on the actual application PCB with the target crystal.*

3.3.3 Free-running oscillator FRO-192M specifications

Table 32. FRO-192M specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
$f_{fro192m}$	FRO-192M frequency (nominal)		96/192		MHz	—
$\Delta f_{fro192m}$	Frequency deviation (–40 °C – 125 °C) • Open loop • Closed loop (using accurate clock source as reference)	 — —	 — —	 ±3 ±0.25	 % %	—
$t_{startup}$	Start-up time • Oscillation time with initial accuracy of ±20 % to ±2 % of enable signal assertion • Oscillation time within ±2 % from enable signal assertion	 — —	 2 10	 — —	 µs µs	—
f_{os}	Frequency overshoot during startup	—	—	2	%	—
jit_{per}	• Period jitter RMS [1] • Accumulated jitter over 1 µs	— —	50 375	— —	ps	—
jit_{cyc}	Cycle to Cycle jitter RMS	—	60	—	ps	—
$I_{fro192m}$	Current consumption	—	40	100	µA	—

[1] Reference clock = 192 MHz.

3.3.4 Free-running oscillator FRO-32K specifications

Table 33. FRO-32K specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
f_{fro32k}	FRO-32K frequency (nominal)	—	32.768	—	kHz	—
Δf_{fro32k}	Frequency deviation(– 40 °C –125 °C) • open loop	—	—	±2	%	—
$TRIM_{step}$	Trimming step	—	0.05	—	%	—
$t_{startup}$	Start-up time	—	—	50	µs	—
f_{os}	Frequency overshoot during startup • Trimmed	—	—	—	%	—
I_{fro32k}	Current consumption	—	220	—	nA	—

3.3.5 Free-running oscillator FRO-16K specifications

Table 34. FRO-16K specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
V_{BAT}	Supply voltage operating range	1.9	2.7	3.6	V	[1]

Table continues on the next page...

Table 34. FRO-16K specifications*...continued*

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Temp	Temperature range	–40	25	125	°C	—
f_{fro16K}	FRO-16K frequency (nominal)	—	16.384	—	kHz	—
Δf_{fro16K}	Frequency deviation • Over –40 °C~125 °C temperature range	—	—	±6	%	—
TRIMstep	Frequency trimming step	—	1.5	—	%	—
I_{fro16k}	Current consumption	—	50	—	nA	[2]
I_{por}	Current consumption	—	26	—	nA	—

[1] FRO-16K is in Power Switch block, which is powered by min 1.9 V VDD_SWITCH
[2] The Typical value (50 nA) of current consumption includes 26 nA POR current consumption in stable running period.

3.4 Memories and memory interfaces

3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.4.1.1 Flash timing specifications

The following command times assume a flash bus clock frequency of 24 MHz.This clock come from SLOW_CLK. Command times will be increased by up to 10 µs at 24 MHz if the module is exiting sleep mode when the command is launched. The time to abort a command is not included in the following table.

Table 35. Flash command time specifications

Symbol	Description	Typ.	Max.	Unit	Notes
$t_{rd1all2048k}$	Read 1s All execution time (2048 KB)	—	12400	µs	—
$t_{rd1blk2048k}$	Read 1s Block execution time (2048 KB)	—	12000	µs	—
t_{rd1scr}	Read 1s Sector execution time	—	50	µs	[1]
t_{rd1pg}	Read 1s Page execution time	—	4.4	µs	[1]
$t_{rd1pglv}$	Read 1s Page at low voltage execution time	—	5.8	µs	[1]
$t_{rd1phrlv}$	Read 1s Phrase at low voltage execution time	—	4.8	µs	[1]
$t_{rd1ipglv}$	Read 1s IFR Page at low voltage execution time	—	5.8	µs	[1]
$t_{rd1iphrlv}$	Read 1s IFR Phrase at low voltage execution time	—	4.8	µs	[1]
t_{rd1phr}	Read 1s Phrase execution time	—	3.8	µs	[1]
$t_{rdmisr8k}$	Read into MISR (8 KB)	—	50	µs	[1]
$t_{rdmisr2048k}$	Read into MISR (2048 KB)	—	12000	µs	[1]
$t_{rd1iscr}$	Read 1s IFR Sector execution time	—	50	µs	[1]
t_{rd1ipg}	Read 1s IFR Page execution time	—	4.4	us	[1]
$t_{rd1iphr}$	Read 1s IFR Phrase execution time	—	3.8	µs	[1]

Table continues on the next page...

Table 35. Flash command time specifications...*continued*

Symbol	Description	Typ.	Max.	Unit	Notes
$t_{rdimisr8k}$	Read IFR into MISR (8 KB)	—	50	µs	[1]
$t_{rdimisr32k}$	Read IFR into MISR (32 KB)	—	190	µs	[1]
t_{pgmpg}	Program Page execution time(Initial)	450	600	µs	[2]
t_{pgmpg}	Program Page execution time(Lifetime)	450	750	µs	[2]
t_{pgmphr}	Program Phrase execution time(Initial)	135	180	µs	[2]
t_{pgmphr}	Program Phrase execution time(Lifetime)	135	225	µs	[2]
$t_{ersall2048k}$	Erase All execution time (2048KB)	—	5800	ms	—
$t_{masers2048k}$	Mass Erase execution time (2048 KB)	—	5800	ms	—
t_{ersscr}	Erase Sector execution time	2	22	ms	[2]

[1] Time to abort the command may significantly impact the time to execute the command.
[2] Measured from the time PERDY is cleared.

3.4.1.2 Flash high voltage current behavior

Table 36. Flash high voltage current behavior

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DD\_IO\_PGM}$	Average current adder to VDD_IO_x during flash programming operation	—	—	6	mA	[1]
$I_{DD\_IO\_ERS}$	Average current adder to VDD_IO_x during flash erase operation	—	—	4	mA	[1]

[1] See the Power Management chapter in the reference manual for the specific VDD_IO_x voltage supply powering the flash array.

3.4.1.3 Flash reliability specifications

Table 37. Flash reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	10	50	—	years	—
$n_{nvmcycscr}$	Sector cycling endurance	10 K	500 K	—	cycles	[2]
$T_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$T_{nvmretp100k}$	Data retention after up to 100 K cycles	5	50	—	years	—
$N_{nvmcyc256k}$	Sector cycling endurance for 256 KB per array block	100 K	500 K	—	cycles	[3]

[1] Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile.
[2] Sector cycling endurance represents the number of Program/Erase cycles on a single sector at -40 °C ≤ T_j ≤ 125 °C.
[3] For devices with a single flash block, sectors must be located within the last 256 KB of the flash main memory. For devices with two flash blocks, sectors must be located within the last 256 KB of each flash main memory.

3.5 Radio modules

3.5.1 2.4 GHz radio transceiver electrical specification

Table 38. 2.4 GHz radio transceiver specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
VDD_RF	RF supply voltage	1.187	1.2	3.6	V	—
VPA_2P4GHZ	Supply voltage for 2.4 GHz radio power amplifier	0.9	—	2.4	V	[1], [2]
f_{in}	Input RF frequency	2.360	—	2.487	GHz	—
f_c	Output RF frequency	2.360	—	2.487	GHz	—
P_{max}	RF input power	—	—	10	dBm	—
f_{ref}	Crystal reference oscillator frequency	—	32	—	MHz	—
f_{tol}	Frequency tolerance	—	±50	—	ppm	—
T_{rx_tx}	Rx - Tx turnaround time	—	150	—	µs	[3]

[1] Voltage required at this rail depends on the desired output power. See Transmit and PLL feature summary for the required voltages.
[2] VPA_2P4GHZ is internally connected to the VDD_RF pin. When not powered externally, VPA_2P4GHZ = VDD_RF - 0.275 V. An internal regulator prevents VPA_2P4GHZ from going above 2.4 V when powered through the VDD_RF pin.
[3] Bluetooth LE. Other modes have different requirements

3.5.2 Receiver feature summary

Table 39. Top-level receiver specifications (T_A = 25 °C, nominal process unless otherwise noted)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
Receiver Active Power Consumption					
Supply current Rx On with DC-DC converter enable (Buck; VDD_DCDC =3.3 V, VDD_RF=VDD_LDO_CORE = 1.25 V) [2]	I_{Rxon}	—	5.20	—	mA
Supply current Rx On with DC-DC converter disabled (Bypass, VDD_RF = VDD_LDO_CORE = 3.3. V) [2]	I_{Rxonb}	—	8.61	—	mA
Receiver General Specifications					
Input RF Frequency	F_{in}	2.360	—	2.487	GHz
GFSK Rx Sensitivity(250 kbps GFSK-BT = 0.5, h = 0.5)[3]	$SENS_{GFSK}$	—	–103	—	dBm
Max RX RF Input Signal Level	RF_{inMax}	—	—	10	dBm
Noise Figure for maximum gain mode at typical sensitivity[4]	NF_{HG}	—	6.5	—	dB
Receiver Signal Strength Indicator Range[5]	$RSSI_{Range}$	-100	—	0[6]	dBm
Receiver Signal Strength Indicator Resolution	$RSSI_{Res}$	—	1	—	dB
Typical RSSI variation over frequency		–2	—	2	dB
Typical RSSI variation over temperature		–2	—	2	dB
Narrowband RSSI accuracy[7]	$RSSI_{Acc}$	–3	—	3	dB

Table continues on the next page...

Table 39. Top-level receiver specifications (T_A = 25 °C, nominal process unless otherwise noted)*...continued*

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
Spurious Emission < 1.6 MHz offset (Measured with 100 kHz resolution and average detector. Device transmit on RF channel with center frequency fc and spurious power measured in 1 MHz at RF frequency f), where |f-fc| < 1.6 MHz	—	—	–54	—	dBc
Spurious Emission > 2.5 MHz offset (Measured with 100 kHz resolution and average detector. Device transmit on RF channel with center frequency fc and spurious power measured in 1 MHz at RF frequency f), where |f-fc| > 2.5 MHz[8]	—	—	–70	—	dBc
Bluetooth LE coded 125 kbps (Long Range, 8x Spreading)					
Bluetooth LE LR 125 kbps Sensitivity[9],[3]	$SENS_{BLELR125}$	—	–106	—	dBm
Bluetooth LE LR 125 kbps Co-channel Interference (Wanted signal at –79 dBm, BER < 0.1 %).[10]	$COSEL_{BLELR125}$		–2		dB
Adjacent/Alternate Channel Selectivity Performance [11]					
Bluetooth LE LR 125 kbps Adjacent ±1 MHz Interference offset (Wanted signal at –79 dBm, BER < 0.1 %)[10]	$SEL_{BLELR125,\ 1\ MHz}$	—	8	—	dB
Bluetooth LE LR 125 kbps Adjacent ± 2 MHz Interference offset (Wanted signal at –79 dBm, BER < 0.1 %)[10]	$SEL_{BLELR125,\ 2\ MHz}$	—	50/35	—	dB
Bluetooth LE LR 125 kbps Alternate ±3 MHz Interference offset (Wanted signal at –79 dBm, BER < 0.1 %)[10]	$SEL_{BLELR125,\ 3\ MHz}$	—	55/45	—	dB
Bluetooth LE LR 125 kbps Alternate ≥ ±4 MHz Interference offset (Wanted signal at –79 dBm, BER < 0.1 %)[12],[10]	$SEL_{BLELR125,\ 4+\ MHz}$	—	55	—	dB
Bluetooth LE coded 500 kbps (Long Range, 2x Spreading)					
Bluetooth LE LR 500 kbps Sensitivity[9],[3]	$SENS_{BLELR500}$	—	–102	—	dBm
Bluetooth LE LR 500 kbps Co-channel Interference (Wanted signal at –72 dBm, BER < 0.1 %).[10]	$COSEL_{BLELR500}$		–3		dB
Adjacent/Alternate Channel Selectivity Performance [11]					
Bluetooth LE LR 500 kbps Adjacent ±1 MHz Interference offset (Wanted signal at –72 dBm, BER < 0.1 %.)[10]	$SEL_{BLELR500,\ 1\ MHz}$	—	8	—	dB
Bluetooth LE LR 500 kbps Adjacent ±2 MHz Interference offset (Wanted signal at –72 dBm, BER < 0.1 %.)[10]	$SEL_{BLELR500,\ 2\ MHz}$	—	50/35	—	dB
Bluetooth LE LR 500 kbps Alternate ±3 MHz Interference offset (Wanted signal at –72 dBm, BER < 0.1 %.)[10]	$SEL_{BLELR500,\ 3\ MHz}$	—	55/45	—	dB
Bluetooth LE LR 500 kbps Alternate ≥ ±4 MHz Interference offset (Wanted signal at –72 dBm, BER < 0.1 %.)[12],[10]	$SEL_{BLELR500,\ 4+\ MHz}$	—	52	—	dB
Bluetooth LE un-coded 1 Mbps					

Table continues on the next page...

Table 39. Top-level receiver specifications (T_A = 25 °C, nominal process unless otherwise noted)*...continued*

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
Bluetooth LE 1 Mbps Sensitivity[9],[3]	$SENS_{BLE1M}$	—	–97.5	—	dBm
Bluetooth LE 1 Mbps Co-channel Interference (Wanted signal at –67 dBm, BER < 0.1 %.).[10]	$COSEL_{BLE1M}$		–6		dB
Adjacent/Alternate Channel Selectivity Performance [11]					
Bluetooth LE 1 Mbps Selectivity ±1 MHz Interference offset (Wanted signal at –67 dBm, BER < 0.1 %.)[10]	$SEL_{BLE1M, 1 MHz}$	—	0	—	dB
Bluetooth LE 1 Mbps Adjacent ±2 MHz Interference offset (Wanted signal at –67 dBm, BER < 0.1 %.)[10]	$SEL_{BLE1M, 2 MHz}$	—	45/35	—	dB
Bluetooth LE 1 Mbps Selectivity ±3 MHz Interference offset (Wanted signal at –67 dBm, BER < 0.1 %.)[10]	$SEL_{BLE1M, 3 MHz}$	—	53/45	—	dB
Bluetooth LE 1 Mbps Alternate ≥ ±4 MHz Interference offset (Wanted signal at –67 dBm, BER < 0.1 %.)[12],[10]	$SEL_{BLE1M, 4+ MHz}$	—	52	—	dB
Intermodulation Performance					
Bluetooth LE 1 Mbps Intermodulation with continuous wave interferer at ±3 MHz (or ±4 MHz) and modulated interferer is at ±6 MHz (or ±8 MHz) – Wanted signal at –64 dBm, BER < 0.1 %.	$IM3\text{-}6_{BLE1M}$ $IM4\text{-}8_{BLE1M}$	—	–27	—	dBm
Bluetooth LE 1 Mbps Intermodulation with continuous wave interferer at ±5 MHz and modulated interferer is at ±10 MHz – Wanted signal at –64 dBm, BER < 0.1 %.	$IM5\text{-}10_{BLE1M}$	—	–28	—	dBm
Blocking Performance					
Bluetooth LE 1 Mbps Out of band blocking from 30 MHz to 1000 MHz and 4000 MHz to 5000 MHz (Wanted signal at –67 dBm, BER < 0.1 %. Interferer continuous wave signal.)[13]	—	–2	—	—	dBm
Bluetooth LE 1 Mbps Out of band blocking from 1000 MHz to 2000 MHz and 3000 MHz to 4000 MHz (Wanted signal at –67 dBm, BER < 0.1 %. Interferer continuous wave signal.)	—	–10	—	—	dBm
Bluetooth LE 1 Mbps Out of band blocking from 2001 MHz to 2339 MHz and 2484 MHz to 2999 MHz (Wanted signal at –67 dBm, BER < 0.1 %. Interferer continuous wave signal.)[14]	—	–10	—	—	dBm
Bluetooth LE 1 Mbps Out of band blocking from 5000 MHz to 12750 MHz (Wanted signal at –67 dBm, BER < 0. 1 %. Interferer continuous wave signal.)[14]	—	2	10	—	dBm
Bluetooth LE un-coded 2 Mbps (High Speed)					
Bluetooth LE 2 Mbps Sensitivity[9],[3]	$SENS_{BLE2M}$	—	–95	—	dBm
Bluetooth LE 2 Mbps Co-channel Interference (Wanted signal at –67 dBm, BER < 0.1 %).[10]	$COSEL_{BLE2M}$		–7		dB

Table continues on the next page...

Table 39. Top-level receiver specifications (T_A = 25 °C, nominal process unless otherwise noted)*...continued*

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
Adjacent/Alternate Channel Performance [11]					
Bluetooth LE 2 Mbps Adjacent ±2 MHz Interference offset (Wanted signal at –67 dBm, BER < 0.1 %) [10]	$SEL_{BLE2M, 2 MHz}$	—	5	—	dB
Bluetooth LE 2 Mbps Alternate ±4 MHz Interference offset (Wanted signal at –67 dBm, BER < 0.1 %.)[10]	$SEL_{BLE2M, 4 MHz}$	—	42/30	—	dB
Bluetooth LE 2 Mbps Selectivity ±6 MHz Interference offset (Wanted signal at –67 dBm, BER < 0.1 %.)[10]	$SEL_{BLE2M, 6 MHz}$	—	50	—	dB
Bluetooth LE 2 Mbps Selectivity ≥±8 MHz Interference offset (Wanted signal at –67 dBm, BER < 0.1 %.)[12],[10]	$SEL_{BLE2M, 8+ MHz}$	—	52	—	dB
Intermodulation Performance					
Bluetooth LE 2 Mbps Intermodulation with continuous wave interferer at ±6 MHz and modulated interferer is at ±12 MHz -- Wanted signal at –64 dBm, BER < 0.1 %.	$IM6\text{-}12_{BLE2M}$	—	–28	—	dBm
Bluetooth LE 2 Mbps Intermodulation with continuous wave interferer at ±8 MHz (or ±10 MHz) and modulated interferer is at ±16 MHz (or ±20 MHz) – Wanted signal at –64 dBm, BER < 0.1 %.)	$IM8\text{-}10_{BLE2M}$ $IM16\text{-}20_{BLE2M}$	—	–32	—	dBm
Blocking Performance					
Bluetooth LE 2 Mbps Out of band blocking from 30 MHz to 1000 MHz and 4000 MHz to 5000 MHz (Wanted signal at –67 dBm, BER < 0.1 %. Interferer continuous wave signal.)[13]	—	–4	—	—	dBm
Bluetooth LE 2 Mbps Out of band blocking from 1000 MHz to 2000 MHz and 3000 MHz to 4000 MHz (Wanted signal at –67 dBm, BER < 0.1 %. Interferer continuous wave signal.)	—	–10	—	—	dBm
Bluetooth LE 2 Mbps Out of band blocking from 2001 MHz to 2339 MHz and 2484 MHz to 2999 MHz (Wanted signal at –67 dBm, BER < 0.1 %. Interferer continuous wave signal.)[14]	—	–10	—	—	dBm
Bluetooth LE 2 Mbps Out of band blocking from 5000 MHz to 12750 MHz (Wanted signal at –67 dBm, BER < 0.1 %. Interferer continuous wave signal.)[14]	—	2	10	—	dBm

[1] All the RX parameters are measured at the RF pin.
[2] Transceiver power consumption.
[3] Variation across temperature (-40 °C to 125 °C) is up to 3 dB.
[4] Receiver noise Figure is computed from RF pin to composite (I+jQ) ADC output
[5] Narrow-band RSSI mode.
[6] With RSSI_CTRL_0.RSSI_ADJ field calibrated to account for antenna to RF input losses.
[7] With one point calibration over frequency and temperature.
[8] Exceptions allowed for twice the reference clock frequency(fref) multiples.
[9] Measured at 0.1 % BER using 37 bytes payload long packets in maximum gain mode and nominal conditions.
[10] Selectivity values expressed as Interferer over Carrier relative level (I/C)
[11] Bluetooth LE adjacent and alternate selectivity performance is measured with modulated interference signals.
[12] Exceptions allowed for multiple of XTAL frequency
[13] Exceptions allowed for carrier frequency sub harmonics.
[14] Exceptions allowed for carrier frequency harmonics.

Table 40. Receiver Specifications with Generic FSK Modulations

				Adjacent/Alternate channel selectivity (dB)[1] [2]					
Modulation type	Data rate (kb/s)	Channel BW (kHz)	Typical sensitivity (dBm)[3]	Desired signal level (dBm)	Interferer at ±1* channel BW offset	Interferer at ±2* channel BW offset	Interferer at ±3* channel BW offset	Interferer at ±4* channel BW offset	Co-channel
GFSK BT = 0.5, h = 0.5	2000	4000	-95	-67	5	45/35	52	55	7
	1000	2000	-98	-67	0	42/32	52/42	55	7
	500	1000	-101	-85	40	50/35	55	55	6
	250	500	-106	-85	38	48	52	55/35	6

[1] Selectivity measured with an unmodulated blocker.
[2] Selectivity values expressed as Interferer over Carrier relative level (I/C)
[3] Variation across temperature (-40 °C to 125 °C) is up to 3 dB.

3.5.3 Channel sounding summary

Channel sounding mode capabilities

Table 41. Channel sounding mode capabilities

Description	Parameter	Qualified Value	Unit
Time allocated to swap channel	T_FCS	50 80 150	µs
Interlude time allocated between RTT packets from initiator device and reflector device	T_IP1	40 80 145	µs
Interlude time allocated between tone TX from initiator device and reflector device	T_IP2	40 80 145	µs
Phase measurement time	T_PM	20 40	µs
Time allocated for Power Amplifier ramp-down (fixed value in the core specification)	T_RD	5	µs
Guard time between tone and packet transmission, in mode 0 and mode 3 steps (fixed value in the core specification)	T_GD	10	µs
Antenna switching time	T_SW	2 4 10	µs
Frequency measurement time in mode 0 step (fixed value in the core specification)	T_FM	80	µs

Table continues on the next page...

Table 41. Channel sounding mode capabilities*...continued*

Description	Parameter	Qualified Value	Unit
CS SYNC packet (Access Address) duration (fixed value in the core specification)	T_SY	44 26	µs

Table 42. Channel sounding supported capabilities

Description	Parameter	Supported
Modulation supported in mode 0, mode 1 and mode 3 packets 1 Mbps, 2 Mbps	CS SYNC PHY	YES
CS SYNC packet payload (HW support).Access Address Random Sequence 32, 64, 96 & 128 bit	RTT_TYPE	YES
RTT_AA_Only_N, RTT_Random_Payload_N - 10 ns time-of-flight precision requirement for Channel Sounding security up to level 4	RTT_Capability	YES
Channel Sounding Initiator support	CS Initiator	YES
Channel Sounding Reflector support	CS Reflector	YES
CS Step for time and frequency synchronization	MODE 0	YES
RTT packet exchange	MODE 1	YES
Tone exchange (Phase Based Ranging)	MODE 2	YES
RTT & tone exchange	MODE 3	YES
Number of antenna paths1, 2, 4	N_AP	YES
1x1, 1x2, 1x4, 2x1, 4x1, 2x2	Antenna Configurations	YES
Specifies which channels are used or excluded0xXXXX XXXX XXXX XXXX XXXX	Channel_Map	YES
Channel selection algorithm for mode 0 steps	Channel selection #3A	YES
Channel selection algorithm for non-mode 0 steps	Channel selection #3B, #3C	YES
CS Tone Quality Indicator 2 levels (low & high)	TQI	YES
Normalized Attack Detection Metric (phase-based)	NADM	YES
Bluetooth LE specification allows repeating the procedure multiple times in a controlled way	Procedure Repeat	YES
Frequency Actuation Error bit indicates whether the device supports mode-0 FAE tables	No_FAE	YES

3.5.4 Transmit and PLL feature summary

- Supports constant envelope modulation of 2.4 GHz ISM frequency band.
- Fast PLL Lock time: < 25 µs
- Reference Frequency:
  - 32 MHz crystals supported for Bluetooth LE and Generic FSK modes

Table 43. Top-level transmitter specifications (T_A = 25 °C, nominal process unless otherwise noted)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
Transmitter Active Power Consumption					
Supply current Tx On with P_{RF} = 0 dBm and DC-DC converter enabled (Buck; VDD_DCDC = 3.3 V, VDD_RF = VDD_LDO_CORE = 1.25 V,VDD_LDO_ANT_OUT = 1.12 V) [2]	I_{TX0dBm}	—	5.38	—	mA
Supply current Tx On with P_{RF} = 0 dBm and DC-DC converter disabled (Bypass, VDD_RF = VDD_LDO_CORE = 3.3 V,VDD_LDO_ANT_OUT = 1.12 V) [2]	$I_{TX0dBmb}$	—	8.95	—	mA
Supply current Tx On with P_{RF} = +4 dBm and DC-DC converter enabled (Buck; VDD_DCDC = 3.3 V, VDD_RF = VDD_LDO_CORE = 1.8 V, VDD_LDO_ANT_OUT = 1.69 V) [2]	I_{TX4dBm}	—	7.96	—	mA
Supply current Tx On with P_{RF} = 4 dBm and DC-DC converter disabled (Bypass, VDD_RF = VDD_LDO_CORE = 3.3 V,VDD_LDO_ANT_OUT = 1.69 V) [2]	$I_{TX4dBmb}$	—	11.28	—	mA
Supply current Tx On with P_{RF} = +7 dBm and DC-DC converter enabled (Buck; VDD_DCDC = 3.3 V, VDD_RF = VDD_LDO_CORE = 1.8 V, VDD_LDO_ANT_OUT = 1.67 V) [2]	I_{TX7dBm}	—	9.86	—	mA
Supply current Tx On with P_{RF} = 7 dBm and DC-DC converter disabled (Bypass, VDD_RF = VDD_LDO_CORE = 3.3 V, VDD_LDO_ANT_OUT = 1.67 V)[2]	$I_{TX7dBmb}$	—	14.72	—	mA
Supply current Tx On with P_{RF} = +10 dBm and DC-DC converter enabled (Buck; VDD_DCDC = 3.3 V, VDD_RF = VDD_LDO_CORE = 2.4 V,VDD_LDO_ANT_OUT = 2.32 V)[2]	$I_{TX10dBm}$	—	15.75	—	mA
Supply current Tx On with P_{RF} = 10 dBm and DC-DC converter disabled (Bypass, VDD_RF = VDD_LDO_CORE = 3.3 V, VDD_LDO_ANT_OUT = 2.32 V)[2]	$I_{TX10dBmb}$	—	18.99	—	mA
Transmitter General Specifications					
Output RF Frequency	f_{RFout}	2.360	—	2.487	GHz
Maximum RF Output Power; 10 dBm configuration [3],[4]	$P_{RF,maxV}$	—	10	—	dBm
Minimum RF Output power [5],[4]	$P_{RF,minn}$	—	-30	—	dBm
RF Output power control range (nominal power supply)	P_{RFCR}	—	32	—	dB
Bluetooth LE Maximum Deviation of the Carrier Frequency[6]	$F_{cdev,BLE}$	—	±3	—	kHz
Bluetooth LE Frequency Hopping Support			YES		

Table continues on the next page...

Table 43. Top-level transmitter specifications (T_A = 25 °C, nominal process unless otherwise noted)*...continued*

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
2nd Harmonic of Transmit Carrier Frequency (P_{out} = $P_{RF,max}$)[7],[8]	TXH2	—	–53	—	dBm/MHz
3rd Harmonic of Transmit Carrier Frequency (P_{out} = $P_{RF,max}$)[8]	TXH3	—	–50	—	dBm/MHz
Bluetooth LE un-coded 1 Mbps/coded 125 kbps/coded 500 kbps					
Bluetooth LE 1 Mbps TX Output Spectrum 20 dB BW	$TXBW_{BLE1M}$	1.0		—	MHz
Bluetooth LE 1 Mbps average frequency deviation using a 00001111 modulation sequence	$\Delta f1_{avg,BLE1M}$	—	250	—	kHz
Bluetooth LE 1 Mbps average frequency deviation using a 01010101 modulation sequence	$\Delta f2_{avg,BLE1M}$	—	220	—	kHz
Bluetooth LE 1 Mbps RMS FSK Error	$FSK_{err,BLE1M}$	—	3%	—	
Bluetooth LE 1 Mbps Adjacent Channel Transmit Power at 2 MHz offset[8]	$P_{RF2MHz,BLE1M}$	—	—	-55	dBc
Bluetooth LE 1 Mbps Adjacent Channel Transmit Power at ≥ 3 MHz offset[8]	$P_{RF3MHz,BLE1M}$	—	—	-59	dBc
Bluetooth LE un-coded 2 Mbps					
Bluetooth LE 2 Mbps TX Output Spectrum 20 dB BW	$TXBW_{BLE2M}$	2.0	—	—	MHz
Bluetooth LE 2 Mbps average frequency deviation using a 00001111 modulation sequence	$\Delta f1_{avg,BLE2M}$	—	500	—	kHz
Bluetooth LE 2 Mbps average frequency deviation using a 01010101 modulation sequence	$\Delta f2_{avg,BLE2M}$	—	440	—	kHz
Bluetooth LE 2 Mbps RMS FSK Error	$FSK_{err,BLE2M}$	—	4%	—	
Bluetooth LE 2 Mbps Adjacent Channel Transmit Power at 4 MHz offset[8]	$P_{RF4MHz,BLE2M}$	—	—	-55	dBc
Bluetooth LE 2 Mbps Adjacent Channel Transmit Power at ≥ 6 MHz offset[8]	$P_{RF6MHz,BLE2M}$	—	—	-60	dBc

[1] All the TX parameters are measured at test hardware SMA connector.
[2] Transceiver power consumption. NBU running at 16 MHz.
[3] Measured at RF pins, with V_{PA_2P4GHz} = 2.4 V.
[4] Variation across temperature (-40 °C to 125 °C) is up to 3 dB.
[5] Measured at the RF pins single supply configuration VDD_RF = VDD_LDO_CORE = 1.25 V
[6] Maximum drift of carrier frequency of the PLL during a Bluetooth LE packet with a nominal 32 MHz reference crystal.
[7] Harmonic levels based on recommended 2 component match for TX output power ≤ 5 dBm. Transmit harmonic levels depend on the quality of matching components. Additional harmonic margin using a 3rd matching component (1x shunt capacitor) is possible.
[8] Measured at P_{out} > 5 dBm and recommended high-power TX match.

3.6 Analog

3.6.1 ADC electrical specifications

3.6.1.1 16-bit ADC operating conditions

Table 44. 16-bit ADC operating conditions

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
V_{DD_ANA}	Supply voltage	1.71	—	3.6	V	—
ΔV_{DD_ANA}	Supply voltage delta to V_{DD} ($V_{DD} - V_{DD\_ANA}$)	–0.1	0	+0.1	mV	[2]
ΔV_{SS_ANA}	Ground voltage delta to V_{SS} ($V_{SS} - V_{SS\_ANA}$)	–0.1	0	+0.1	mV	[2]
V_{REFH}	ADC reference voltage high	0.99	V_{DD_ANA}	V_{DD_ANA}	V	—
V_{REFL}	ADC reference voltage low	V_{SS_ANA}	V_{SS_ANA}	V_{SS_ANA}	V	[3]
V_{ADIN}	Input voltage	V_{REFL}	—	V_{REFH}	V	[3], [4],[5]
f_{ADCK}	ADC input clock frequency					—
	• Low-power mode (PWRSEL=00)	6	—	20	MHz	
	• High-speed 16b mode (PWRSEL = 10)	6	—	48	MHz	
	• High-speed 12b mode (PWRSEL = 10)	6	—	60	MHz	
C_{ADIN}	Input capacitance	—	3.7	4.63	pF	—
C_p	Parasitic Cap of pad /package	—	2	3	pF	—
R_{AS}	Analog source resistance (external)	—	—	5	kΩ	[6]
R_{ADIN}	• High-speed dedicated input channel (CH0:3)				kΩ	[7],[8]
	— $V_{DD\_ANA} \geq 1.71$ V	—	0.95	1.7		
	— $V_{DD\_ANA} \geq 2.1$ V	—	0.95	1.6		
	— $V_{DD\_ANA} \geq 2.5$ V	—	0.95	1.4		
	• Standard external input channel (Ch4:7)					
	— $V_{DD\_ANA} \geq 1.71$ V	—	1.35	3.25		
	— $V_{DD\_ANA} \geq 2.1$ V	—	1.35	2.15		
	— $V_{DD\_ANA} \geq 2.5$ V	—	1.35	1.75		
	• Standard muxed input channel (Ch4:11)					
	— $V_{DD\_ANA} \geq 1.71$ V	—	1.65	7.25		
	— $V_{DD\_ANA} \geq 2.1$ V	—	1.65	3.05		
	— $V_{DD\_ANA} \geq 2.5$ V	—	1.65	2.35		

[1] Typical values assume V_{DD_ANA}= 3.0 V, Temp = 25 °C, f_{ADCK} = 24 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
[2] DC potential difference.
[3] For devices that do not have a dedicated VREFL and VSS_ANA pins, VREFL and VSS_ANA are tied to VSS internally.
[4] If V_{REFH} is less than V_{DD_ANA}, then voltage inputs greater than V_{REFH} but less than V_{DD_ANA} are allowed but result in a full scale conversion result
[5] ADC selected inputs and unselected dedicated inputs must not exceed V_{DD_ANA} during an ADC conversion. Unselected muxed inputs may exceed V_{DD_ANA} but must not exceed the IO supply associated with the inputs (VDD_IO_X) when a conversion is in progress. If an ADC input may exceed these levels, then a minimum of 1 K series resistance must be used between the source and the ADC input pin.
[6] This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible.
[7] There are several types of ADC inputs. To see which channels correspond to which type of ADC inputs, see channel index map in reference manual
[8] If the input come through a mux in the IO pad, add the IO Mux Resistance Adder value to the resistance for the channel type

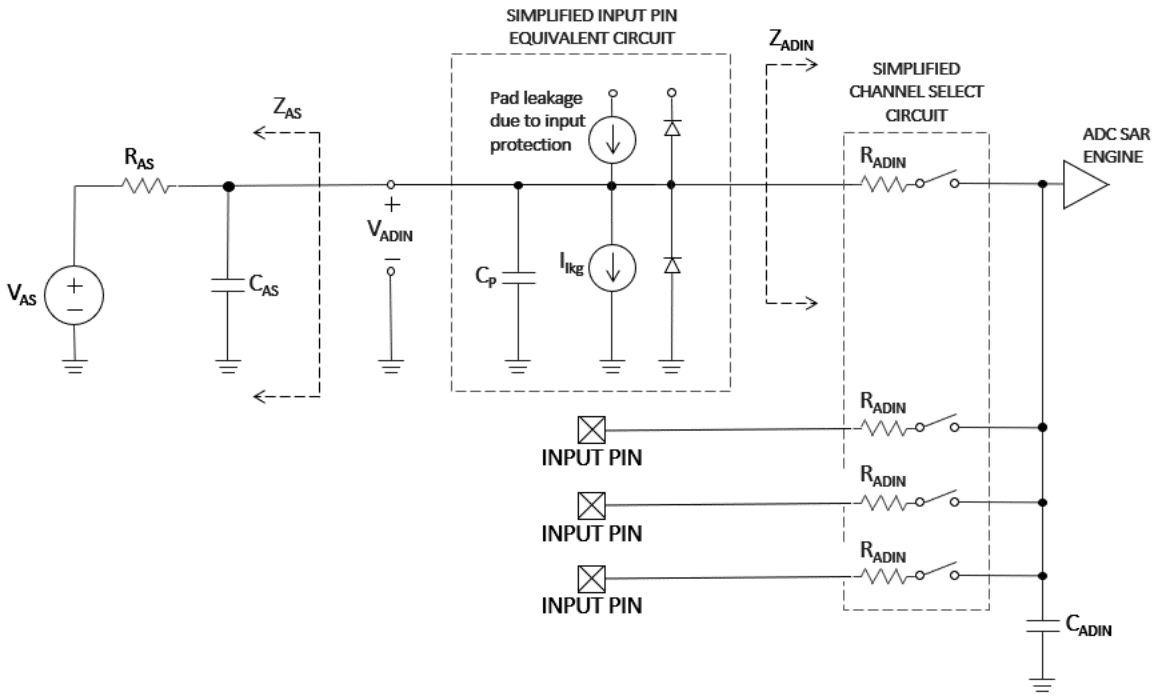


Figure 7. ADC input impedance equivalency diagram

3.6.1.2 16-bit ADC electrical characteristics

Table 45. 16-bit ADC characteristics (VREFH = VDD_ANA, VREFL = VSS_ANA)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
I_{DDA}	Supply current					[2]
	• PWREN=0, Conversions triggered at 1 kS/s	—	2.2	—	µA	
	• PWREN=1, No Conversions	—	160	215	µA	
	• Low-power, single-ended mode, 6 MHz	—	340	440	µA	
	• Low-power, or dual-SE mode, 6 MHz	—	500	640	µA	
	• Low-power, single-ended mode, 24 MHz	—	415	530	µA	
	• Low-power, or dual-SE mode, 24 MHz	—	580	750	µA	
	• High-speed, single-ended mode, 48 MHz	—	940	1200	µA	
	• High-speed, or dual-SE mode, 48 MHz	—	1500	1950	µA	
I_{TS}	Temp Sensor Current Adder	—	40	50	µA	—
C_{SMP}	ADC Sample cycles	3.5	—	131.5	cycles	[3]
C_{CONV}	ADC conversion cycles	24	—	152	cycles	—
C_{RATE}	ADC conversion rate	—	—	0.857	MS/s	[4]

Table continues on the next page...

Table 45. 16-bit ADC characteristics (VREFH = VDD_ANA, VREFL = VSS_ANA)*...continued*

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
	• Low-power mode • High-speed mode (16-bits) • High-speed mode (12-bits)	— —	— —	2 3.16		
T_{SMP_REQ}	Required Sample Time	See equation	—	—	ns	[5]
T_{AZ_REQ}	Required Auto-zero Time • Low-power mode • High-power mode (16-bits) • High-power mode (12-bits)	291.7 72.9 58.3	— — —	— — —	ns	[5]
T_{SMP}	Sample Time External inputs	See equation	—	—	ns	[5]
T_{SMP_INT}	Internal channel sample time	1.5	—	—	µs	[6]
DNL	Differential non-linearity	—	±0.7	+1.4/–0.95	LSB[7]	[8]
INL	Integral non-linearity	—	±2.0	+4.0/–2.0	LSB[7]	[8]
Z_{SE}	Zero-scale error (V_{ADIN} = V_{REFL})	—	±1.0	±2.0	LSB[7]	[8]
F_{SE}	Full-scale error (V_{ADIN}=V_{REFH})	—	±2.0	+2.0/–8.0	LSB[7]	[8]
TUE	Total unadjusted error	—	±4.0	±10.0	LSB[7]	[8]
ENOB	Effective number of bits • Differential mode — 0.5 MS/s — 2 MS/s • Single-ended mode — 0.5 MS/s — 2 MS/s	 12.7 12.0 12.4 11.5	 13.5 12.7 13.1 12.2	 — — — —	bits	[8],[9]
SINAD	Signal-to-noise plus distortion • Differential mode — 0.5 MS/s — 2 MS/s • Single-ended mode — 0.5 MS/s — 2 MS/s	 80 75 77 71	 86 79 81 75	 — — — —	dB	[8],[9]
THD	Total harmonic distortion	85	92	—	dB	[8],[10]
SFDR	Spurious free dynamic range	86	94	—	dB	[8],[10]

Table continues on the next page...

Table 45. 16-bit ADC characteristics (VREFH = VDD_ANA, VREFL = VSS_ANA)*...continued*

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
T_{SU}	ADC/VREF start-up time	5	—	—	µs	[11]
E_{IL}	Input leakage error	—	$I_{lkg} \times R_{AS}$	—	mV	[12]
E_{TS}	Temperature sensor error • T=–40 °C to 105 °C • T=–40 °C to 125 °C	— —	±1 ±1.5	±3 ±4	°C	[13]

[1] Typical values assume V_{DD_ANA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 24 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
[2] The ADC supply current depends on the ADC conversion clock speed, conversion rate and power mode. Typical value show is at 6 MHz, 24 MHz, and 48 MHz. For lowest power operation, PWRSEL should be set to 00.
[3] Must meet minimum TSMP requirement.
[4] Maximum conversion rate for high-speed mode is with F_{ADCK} = 48 MHz. Maximum conversion rate for low-power mode is F_{ADCK} = 24 MHz and 7.5 sample cycles (to meet the minimum auto-zero time requirement).
[5] Required sample time is dictated by external components R_{AS}, C_{AS}, internal components R_{ADIN}, C_{ADIN}, C_P, and desired sample accuracy in bits. Calculated it with formula: $T_{SMP\_REQ} = B*IN(2)*[R_{AS}*(C_{AS}*C_P)+ (R_{AS} + R_{ADIN})* C_{ADIN(typ)}$. Required auto-zero time is for ADC comparator offset cancellation. The chosen sample time should be no less than maximum of the two: $T_{SMP} = max(T_{SMP\_REQ}, T_{AZ\_REQ})$.
[6] Internal channel inputs are those that do not come from external source (temperature sensor, bandgap).
[7] 1 LSB = $(V_{REFH} - V_{REFL})/2^N$ (N=14 bits), for 16-bit specifications, multiply by 4.
[8] All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DD_ANA} and using a high-speed dedicated input channel.
[9] Dynamic results assume F_{in} = 1 kHz sinewave, AVGS = 0 for 2 MS/s, AVGS = 4 for 0.5 MS/s.
[10] Dynamic results assume F_{in} = 1 kHz sinewave, no averaging.
[11] Set the power up delay (PUDLY) according to the ADC start-up time if PWREN=0.
[12] I_{lkg} = leakage current (Refer to pin leakage specification in the packaged device's voltage and current operating ratings).
[13] The temperature sensor can be calibrated to a ± 0.5% precision after board assembly by using a 3 temperature calibration flow with accurate ± 0.15 % temperature chamber.

3.6.2 CMP and 8-bit DAC electrical specifications

Table 46. Comparator and 8-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VDD_IO_ABC	Supply voltage	1.71	—	3.6	V	—
VREFH	8-bit DAC reference voltage high	0.97	—	VDD_IO_ABC	V	—
I_{DD_CMP}	Supply current • High-speed mode (EN=1, HPMD=1, NPMD=0) • Normal mode (EN=1, HPMD=0, NPMD=0) • Nano mode (EN=1, HPMD=0, NPMD=1)	— — —	200 10 400	— — —	µA µA nA	—
V_{AIN}	Analog input voltage	VSS_ANA	—	VDD_ANA	V	[1]
V_{AIO}	Analog input offset voltage • High-speed mode • Normal mode • Nano mode	— — —	— — —	20 20 40	mV mV mV	—
V_H	Analog comparator hysteresis	—	0	—	mV	[2]

Table continues on the next page...

Table 46. Comparator and 8-bit DAC electrical specifications...*continued*

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• CR0[HYSTCTR] = 00	—	10	—	mV	
	• CR0[HYSTCTR] = 01	—	20	—	mV	
	• CR0[HYSTCTR] = 10	—	30	—	mV	
	• CR0[HYSTCTR] = 11					
t_D	Propagation delay					[3]
	• High-speed mode, 100 mV overdrive, power > 1.71 V	—	—	25	ns	
	• High-speed mode, 30 mV overdrive, power > 1.71 V	—	—	50	ns	
	• Normal mode, 30 mV overdrive, power > 1.71 V	—	—	600	ns	
	• Nano mode, 30 mV overdrive, power > 1.71 V	—	—	5	µs	
t_{init}	Analog comparator initialization delay	—	—	40	µs	[4]
I_{DAC8b}	8-bit DAC current adder (enabled)					—
	• High-power mode (EN=1, PMODE=1)	—	10	—	µA	
	• Low-power mode (EN=1, PMODE=0)	—	1	—	µA	
INL	8-bit DAC integral non-linearity				LSB	[5]
	• Low/High power mode, supply power > 1.71 V	−1.0	—	+1.0		
DNL	8-bit DAC differential non-linearity				LSB	[5]
	• Low/High power mode, power > 1.71 V	−1.0	—	+1.0		

[1] For devices that do not have a dedicated VSS_ANA pin, VSS_ANA is tied to VSS internally.
[2] Typical hysteresis is measured with input voltage range limited to 0.6 to VDD_ANA–0.6 V.
[3] Overdrive does not include input offset voltage or hysteresis.
[4] Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]), and the comparator output settling to a stable level.
[5] 1 LSB = $V_{reference}/256$.

Typical hysteresis

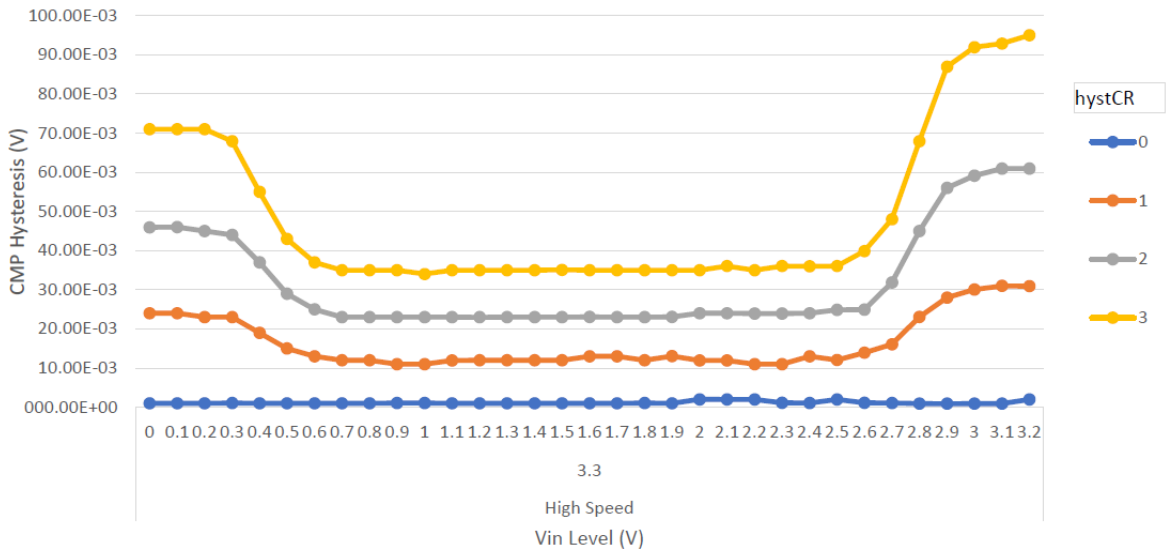


Figure 8. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 1, NMPD = 0)

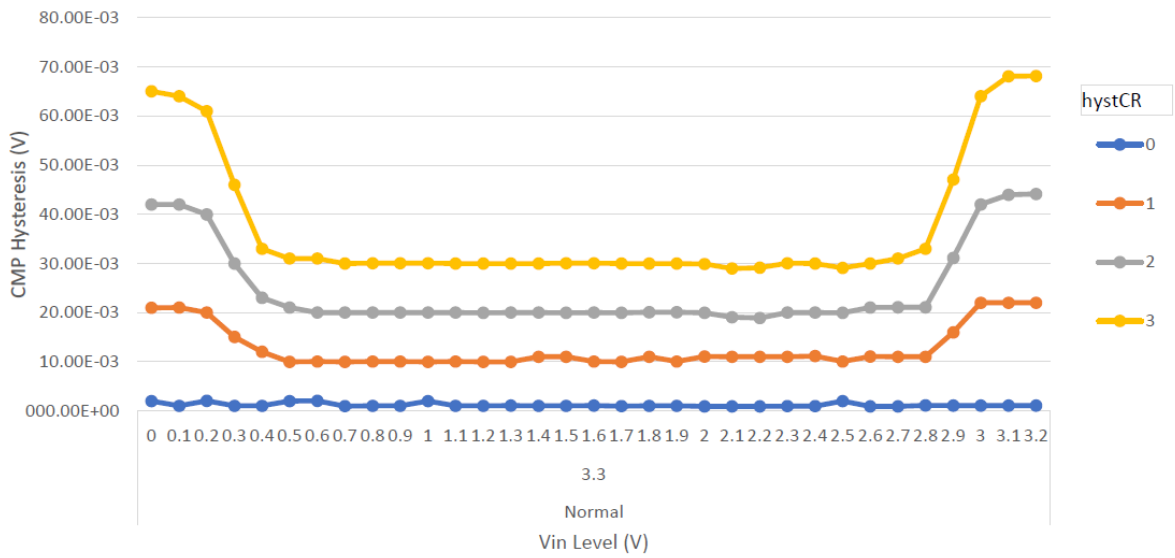


Figure 9. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 0, NPMD = 0)

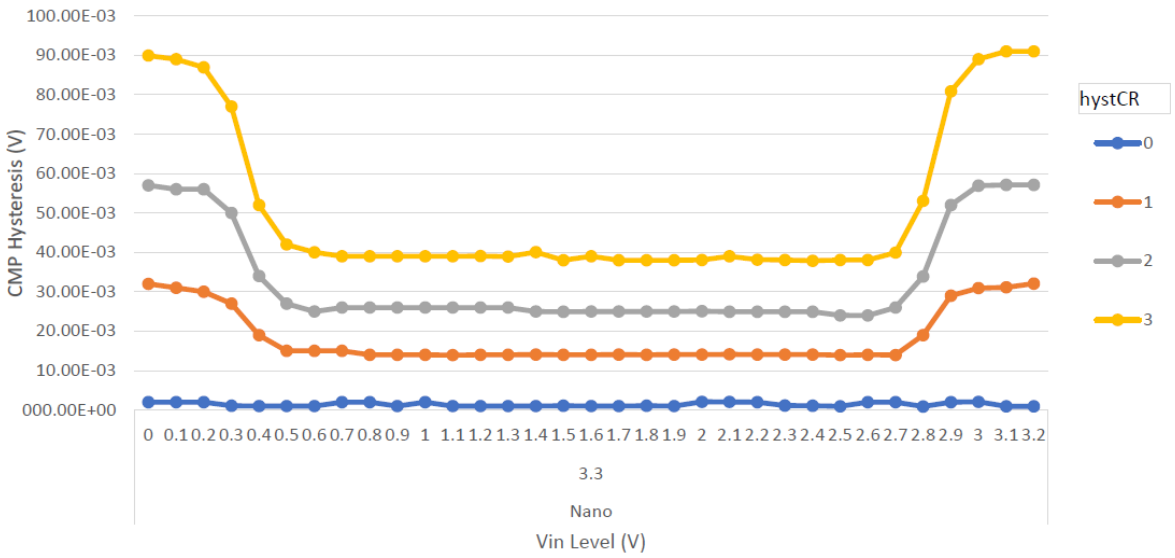


Figure 10. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 0, NPMD = 1)

3.6.3 Voltage reference electrical specifications

Table 47. VREF operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VDD_ANA	Supply voltage	1.71	3.0	3.6	V	[1]
C_L	Output load capacitance	130	220	470	nF	[2], [3]

[1] VDD_ANA must be at least 600 mV greater than the selected VREFO output voltage.
[2] C_L must be connected to VREFO if the VREFO functionality is being used for either an internal or external reference.
[3] The minimum CL capacitance must take into account the variation in capacitance of the chosen capacitor due to voltage, temperature and aging.

Table 48. VREF operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
1.0 V low-power reference voltage						
V_{vrefo_lpbg}	Voltage reference output 1.0 V - LP bandgap		1.0		V	[1]
I_{q_lpbg}	Quiescent current - LP bandgap	—	19	—	µA	—
I_{ptat}	Output current reference (PTAT) - LP bandgap (room temp)	—	1	—	µA	—
I_{ztc}	Output current (ZTC) - LP bandgap	—	1	—	µA	—
t_{st_lpbg}	Start-up time - LP bandgap	—	—	20	µs	—
$\Delta V / V_{refo\_lpbg}$	Voltage variation - LP bandgap	—	±5	—	%	—
High precision reference voltage						

Table continues on the next page...

Table 48. VREF operating behaviors...*continued*

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{vrefo}	Voltage reference output 2.0 V	1.0	—	2.1	V	[2][1]
V_{step}	Fine trim step	—	0.5 x V_{refo}	—	mV	—
I_q	Quiescent current	—	750	—	µA	—
I_{out}	Output current	±1	—	—	mA	—
t_{st_lpbg}	Start-up time	—	—	400	µs	—
ΔV_{LOAD}	Load regulation	—	100	200	µV/mA	[3]
V_{acc}	Absolute voltage accuracy (room temp)	—	±1.5	±6.5	mV	—
V_{dev}	Voltage deviation over temperature	—	15	—	ppm/°C	—

[1] See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
[2] V_{vrefo} max is also ≤ VDD_ANA - 600 mV.
[3] Load regulation voltage is the difference between the VREFO voltage with no load vs. voltage with defined load.

3.7 Timers

See General switching specifications.

3.8 Communication interfaces

3.8.1 LPUART

See General switching specifications.

3.8.2 LPSPI switching specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with controller and peripheral operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes.

Table 49. LPSPI controller mode timing

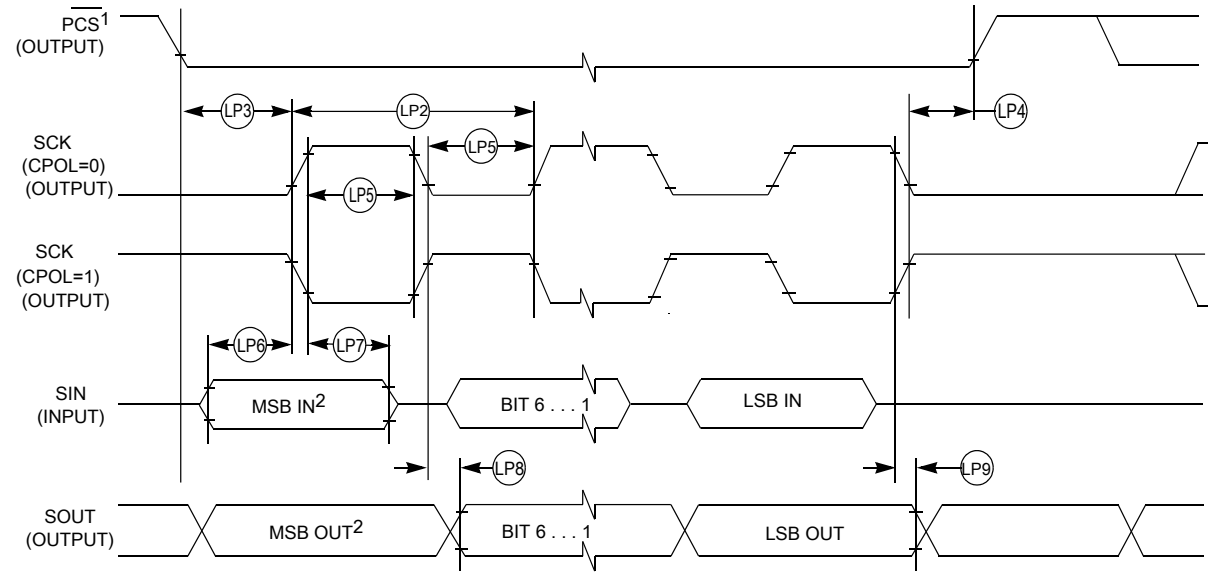
Symbol	Description	Min.	Max.	Unit	Notes
LP1	Frequency of operation • LPSPI0 • LPSPI1	— —	24 48	MHz MHz	[1][2]
LP2	SCK period	2 x t_{periph}	2048 x t_{periph}	ns	[3]
LP3	Enable lead time	1/2	—	t_{periph}	[3]
LP4	Enable lag time	1/2	—	t_{periph}	[3]
LP5	Clock (SCK) high or low time	t_{SCK}/2 - 3	t_{SCK}/2	ns	—
LP6	Data setup time (inputs) • LPSPI0, LPSPI1 at 24 MHz • LPSPI1 at 48 MHz	14.4 7.2	—	ns	—
LP7	Data hold time (inputs)	0	—	ns	—

Table continues on the next page...

Table 49. LPSPI controller mode timing...*continued*

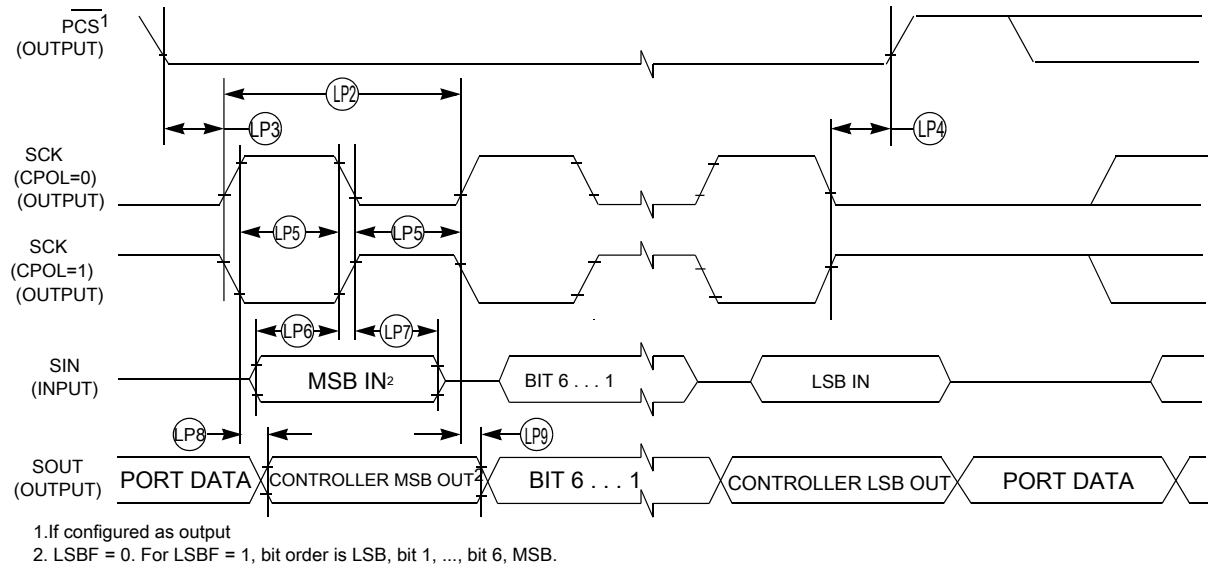
Symbol	Description	Min.	Max.	Unit	Notes
LP8	Data valid (after SCK edge) • LPSPI0, LPSPI1 at 24 MHz • LPSPI1 at 48 MHz	—	14.4 7.2	ns	—
LP9	Data hold time (outputs)	-1	—	ns	—

[1] The frequency of operation is also limited to a minimum of $f_{periph}/2048$ and a max of $f_{periph}/2$, where f_{periph} is the LPSPI peripheral functional clock.
[2] 48 MHz is only possible for PTB port. If PTC port is used, maximum allowed is 12 MHz.
[3] $t_{periph} = 1/f_{periph}$.



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 11. LPSPI controller mode timing (CPHA = 0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 12. LPSPI controller mode timing (CPHA = 1)

Table 50. LPSPI target mode timing

Symbol	Description	Min.	Max.	Unit	Notes
LP1	Frequency of operation • target TX in SD mode — LPSPI0 — LPSPI1 on PTB — LPSPI1 (not PTB pins) • target RX in SD mode — LPSPI0 — LPSPI1 on PTB — LPSPI1 (not PTB pins)	—	 12 24 12 24 48 24	MHz	[1]
LP2	SCK period	2 x t_{periph}	2048 x t_{periph}	ns	[2]
LP3	Enable lead time	1	—	t_{periph}	[2]
LP4	Enable lag time	1	—	t_{periph}	[2]
LP5	Clock (SCK) high or low time	t_{SCK}/2 - 5	t_{SCK}/2	ns	—
LP6	Data setup time (inputs) • LPSPI0, LPSPI1 at 24 MHz • LPSPI1 at 48 MHz	 14.4 3.6	—	ns	[3]
LP7	Data hold time (inputs)	0	—	ns	—
LP8	target access time	—	t_{periph}	ns	[2][4],[3]

Table continues on the next page...

Table 50. LPSPI target mode timing...*continued*

Symbol	Description	Min.	Max.	Unit	Notes
LP9	target MISO disable time	—	t_{periph}	ns	[2][5]
LP10	Data valid (after SCK edge) • LPSPI0, LPSPI1 at 12 MHz • LPSPI1 at 24 MHz	—	31.2 16.25	ns	[2]
LP11	Data hold time (outputs)	2	—	ns	—

[1] The frequency of operation is also limited to a minimum of $f_{periph}/2048$ and a max of $f_{periph}/2$, where f_{periph} is the LPSPI peripheral functional clock.
[2] $t_{periph} = 1/f_{periph}$.
[3] 48 MHz is only possible for PTB port in normal voltage (VDD_CORE=1.1 V) with SAMPLE=1. If PTC port is used, maximum allowed is 24 MHz.
[4] Time to data active from high-impedance stat.
[5] Hold time to high-impedance state.

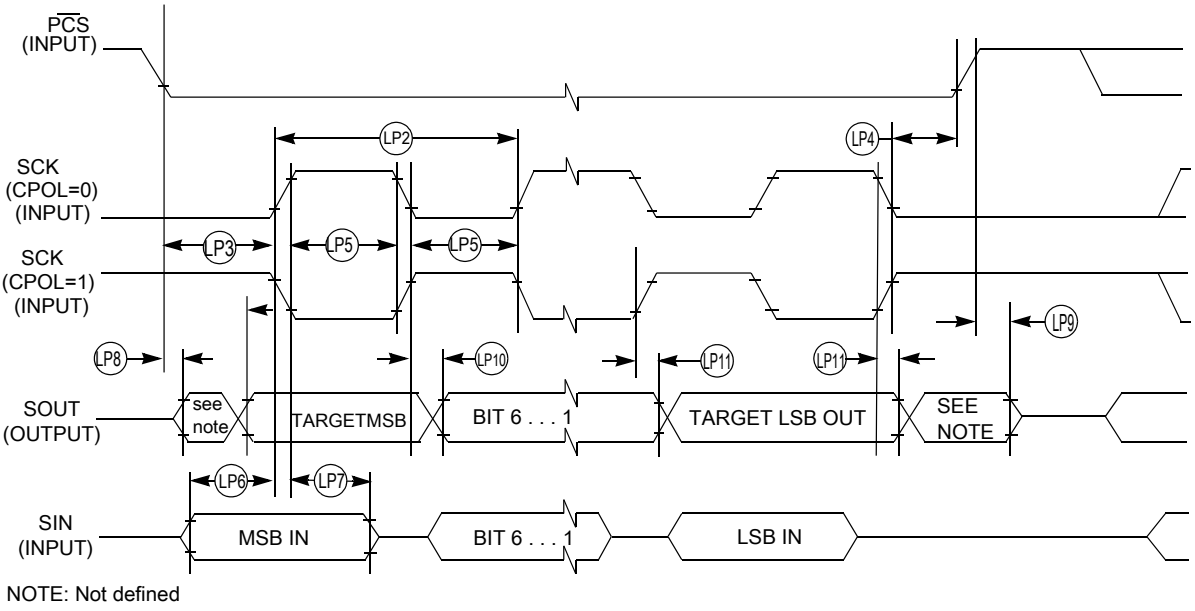


Figure 13. LPSPI target mode timing (CPHA = 0)

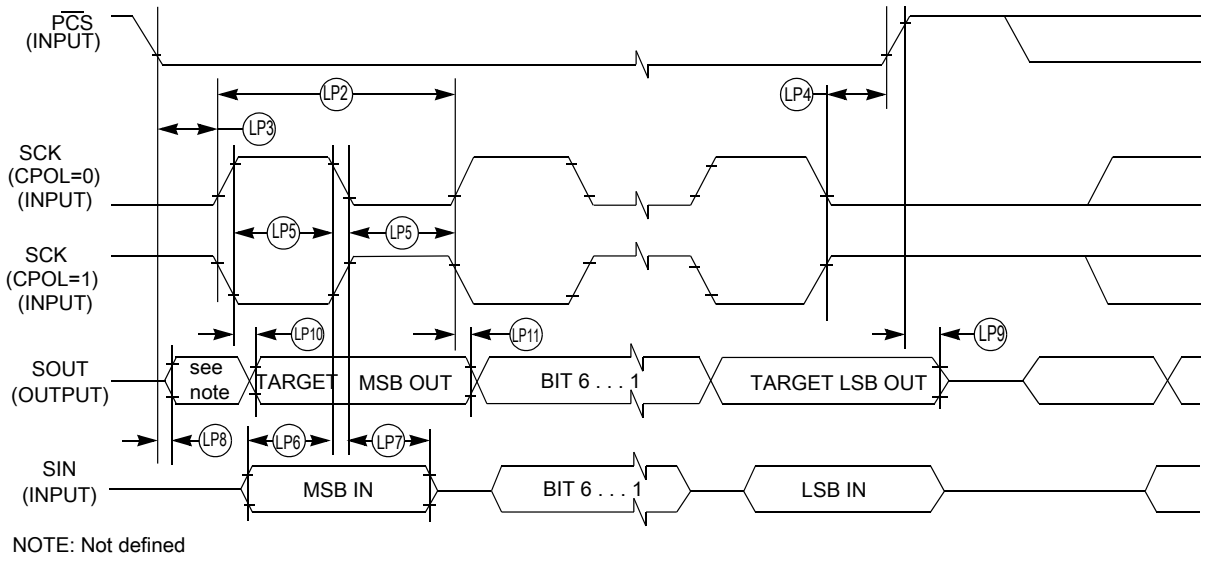


Figure 14. LPSPI target mode timing (CPHA = 1)

3.8.3 Inter-Integrated circuit interface (I2C) specifications

Table 51. I ^{2}C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.25	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I2C bus devices	t_{HD}; DAT	0[1],[2]	3.45[3]	0[4],[2]	0.9[1]	µs
Data set-up time	t_{SU}; DAT	250[5]	—	100[3][6]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[7]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[6]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

[1] The controller mode I2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no targets acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
[2] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the VIH(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
[3] The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.

[4] Input signal Slew = 10 ns and Output Load = 50 pF
[5] Set-up time in target-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
[6] A Fast mode I2C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode I2C bus specification) before the SCL line is released.
[7] C_b = total capacitance of the one bus line in pF.

Table 52. I²C 1 Mbps timing

Characteristic	Symbol	Min.	Max.	Unit
SCL Clock Frequency	f_{SCL}	0	1	MHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	0.26	—	µs
LOW period of the SCL clock	t_{LOW}	0.5	—	µs
HIGH period of the SCL clock	t_{HIGH}	0.26	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	0.26	—	µs
Data hold time for I2C bus devices	t_{HD}; DAT	0	—	µs
Data set-up time	t_{SU}; DAT	50	—	ns
Rise time of SDA and SCL signals	t_r	20 +0.1C_b [1]	120	ns
Fall time of SDA and SCL signals	t_f	20 +0.1C_b[1]	120	ns
Set-up time for STOP condition	t_{SU}; STO	0.26	—	µs
Bus free time between STOP and START condition	t_{BUF}	0.5	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	0	50	ns

[1] C_b = total capacitance of the one bus line in pF. The max C_b value is 50 pF.

Table 53. I2C HS mode timing[1]

Parameter	Symbol	Min	Max	Units
SCL Clock Frequency	f_{SCL}	0	3.4	MHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	0.26	–	µs
LOW period of the SCL clock	t_{LOW}	0.5	–	µs
High period of the SCL clock	t_{HIGH}	0.26	–	µs
Set-up time for a repeated START condition	t_{SU}; STA	0.26	–	µs
Data hold time for I2C bus devices	t_{HD}; DAT	0[2]	–	µs
Data setup time	t_{SU}; DAT	34	_	ns
Rise time of SDA and SCL signals	t_r	20 +0.1Cb[3]	120	ns
Fall time of SDA and SCL signals	t_f	20 +0.1Cb[3]	120	ns
Setup time for STOP condition	t_{SU}; STO	0.26	_	µs
Bus free time between STOP and START condition	t_{BUF}	0.5	_	µs

Table continues on the next page...

Table 53. I2C HS mode timing[1]*...continued*

Pulse width of spikes that must be suppressed by the input filter	t_{SP}	0	50	ns

[1] Only PTB4/5, PTA18/19, PTC0/1, PTC4/5 pin can support Fast+ (3 MHz) mode.
[2] A device must internally provide a data hold time to bridge the undefined part between VIH and VIL of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time.
[3] C_b = total capacitance of the one bus line in pF. The max C_b value is 50 pF.

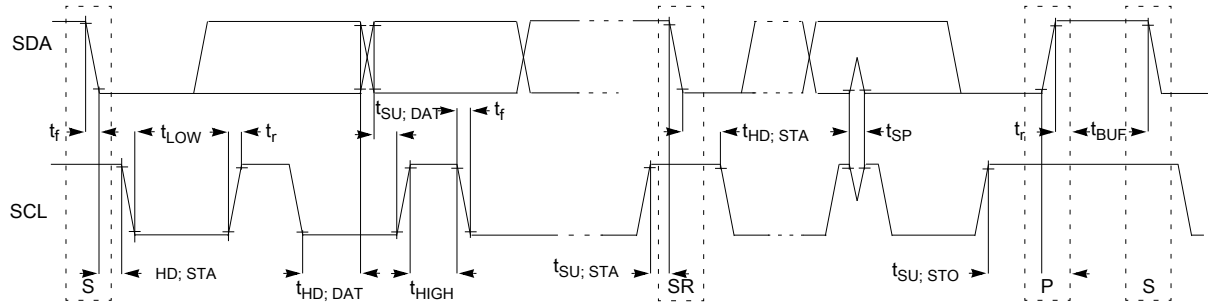


Figure 15. Timing definition for devices on the I2C bus

3.8.4 Improved Inter-Integrated Circuit Interface (MIPI-I3C) specifications

Unless otherwise specified, MIPI-I3C specifications are timed to/from the V_{IH} and/or V_{IL} signal points.

Table 54. MIPI-I3C specifications when communicating with legacy I2C devices

Symbol	Characteristic	400 kHz/Fast mode		1 MHz/ Fast+ mode		Unit
		Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	0	0.4	0	1.0	MHz
t_{SU_STA}	Set-up time for a repeated START condition	600	—	260	—	ns
t_{HD_STA}	Hold time (repeated START condition)	600	—	260	—	ns
t_{LOW}	LOW period of the SCL clock	1300	—	500	—	ns
t_{HIGH}	HIGH period of the SCL clock	600	—	260	—	ns
t_{SU_DAT}	Data set-up time	100	—	50	—	ns
t_{HD_DAT}	Data hold time for I2C bus devices	0	—	0	—	ns
t_f	Fall time of SDA and SCL signals	20 + $0.1C_b$[1]	300	20 + $0.1C_b$[1]	120	ns
t_r	Rise time of SDA and SCL signals	20 + $0.1C_b$[1]	300	20 + $0.1C_b$[1]	120	ns
t_{SU_STO}	Set-up time for STOP condition	600	—	260	—	ns
t_{BUF}	Bus free time between STOP and START condition	1.3	—	0.5	—	µs
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	0	50	0	50	ns

[1] C_b = total capacitance of the one bus line in pF.

Table 55. MIPI-I3C open drain mode specifications

Symbol	Characteristic	Min.	Max.	Unit	Notes
t_{LOW_OD}	LOW period of the SCL clock	200	—	ns	—
$t_{DIG\_OD\_L}$		t_{LOW_OD} + t_{fDA_OD} (min)	—	ns	—
t_{HIGH}	HIGH period of the SCL clock	t_{CF}	12	ns	—
t_{fDA_OD}	Fall time of SDA signal	20 +0.1C_b	120	ns	[1]
t_{SU_OD}	Data set-up time during open drain mode	3	—	ns	—
t_{CAS}	Clock after START (S) Condition • ENTAS0 • ENTAS1 • ENTAS2 • ENTAS3	 38.4 n 38.4 n 38.4 n 38.4 n	 1 µ 100 µ 2 m 50 m	 s s s s	—
t_{CBP}	Clock before STOP (P) condition	t_{CAS}(min)/2	—	ns	—
$t_{MMOverlap}$	Current controller to secondary controller overlap time during handoff	$t_{DIG\_OD\_L}$	—	ns	—
t_{AVAL}	Bus available condition	1	—	µs	—
t_{IDLE}	Bus idle condition	1	—	ms	—
t_{MMLock}	Time internal where new controller not driving SDA low	t_{AVAL}	—	µs	—

[1] C_b = total capacitance of the one bus line in pF.

Table 56. MIPI-I3C push-pull specifications for SDR and HDR-DDR modes

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
f_{SCL}	SCL Clock Frequency	0.01	—	12.5	MHz	—
t_{LOW}	LOW period of the SCL clock	24	—	—	ns	—
t_{DIG_L}		32	—	—	ns	—
t_{HIGH_MIXED}	HIGH period of the SCL clock for a mixed bus	24	—	—	ns	—
$t_{DIG\_H\_MIXED}$		32	—	45	ns	[1]
t_{HIGH}	HIGH period of the SCL clock	24	—	—	ns	—
t_{DIG_H}		32	—	—	ns	—
tSCO	Clock in to data out for target					—
	Load capacitance = 50 pF	—	—	38	ns	—
	Load capacitance = 25 pF	—	—	36	ns	—

Table continues on the next page...

Table 56. MIPI-I3C push-pull specifications for SDR and HDR-DDR modes*...continued*

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
	Load capacitance = 15 pF	—	—	35	ns	—
	Load capacitance = 1 pF	—	—	33	ns	—
t_{CR}	SCL clock rise time	—	—	150 x 1/ f_{SCL} (capped at 60)	ns	—
t_{CF}	SCL clock fall time	—	—	150 x 1/ f_{SCL} (capped at 60)	ns	—
t_{HD_PP}	SDA signal data hold • controller mode • target mode	t_{CR} + 3 and t_{CF} + 3 0	— —	— —	ns	—
t_{SU_PP}	SDA signal setup	3	—	—	ns	—
t_{CASr}	Clock after repeated START (Sr)	t_{CAS} (min)	—	—	ns	—
t_{CBSr}	Clock before repeated START (Sr)	t_{CAS} (min)/2	—	—	ns	—
C_b	Capacitive load per bus line	—	—	50	pF	—

[1] When communicating with an I3C Device on a mixed Bus, the $t_{DIG\_H\_MIXED}$ period must be constrained in order to make sure that I2C devices do not interpret I3C signaling as valid I2C signaling.

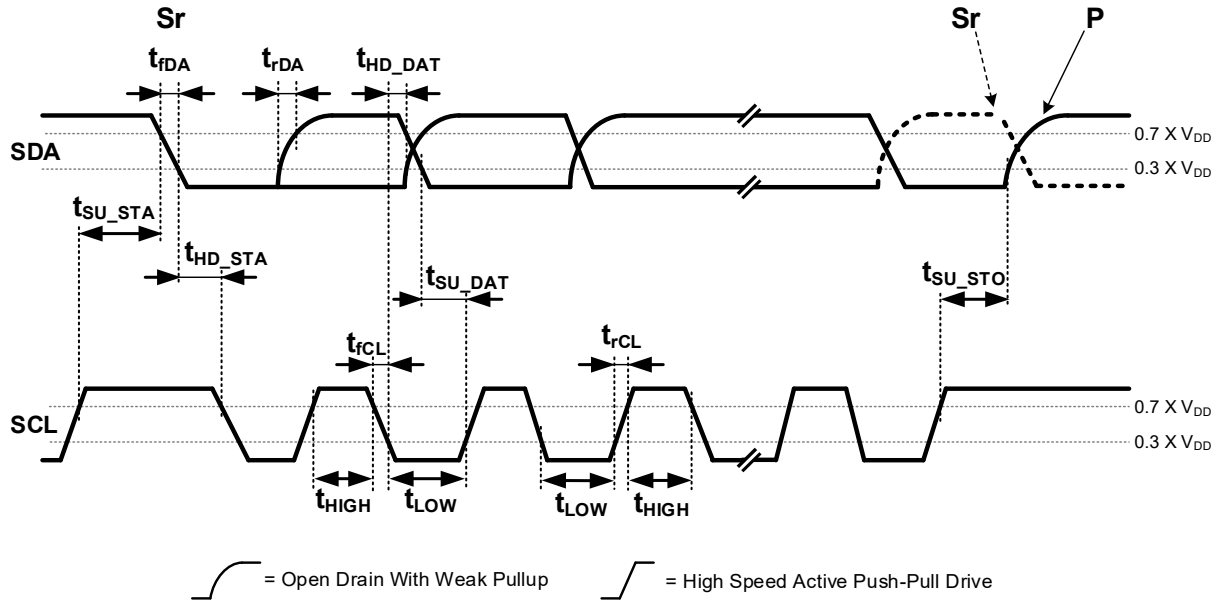


Figure 16. I3C legacy mode timing

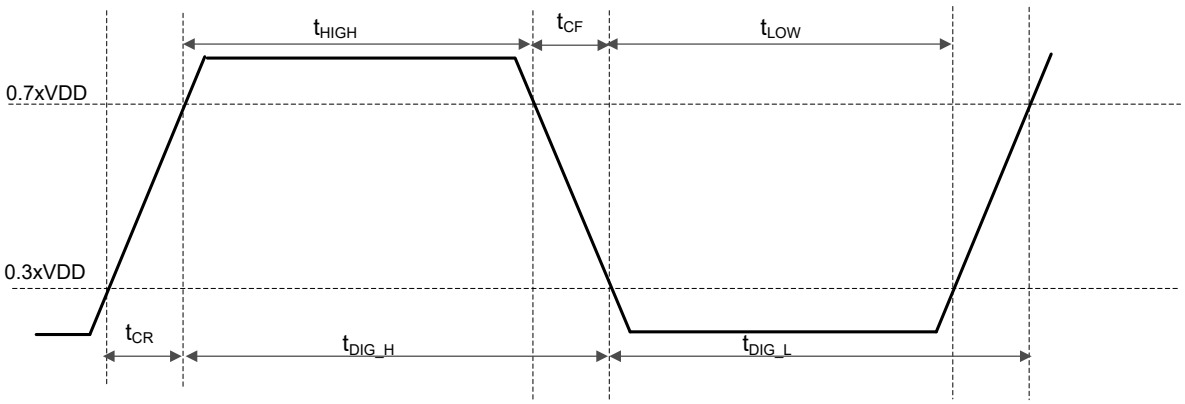


Figure 17. t_{DIG_H} and t_{DIG_L}

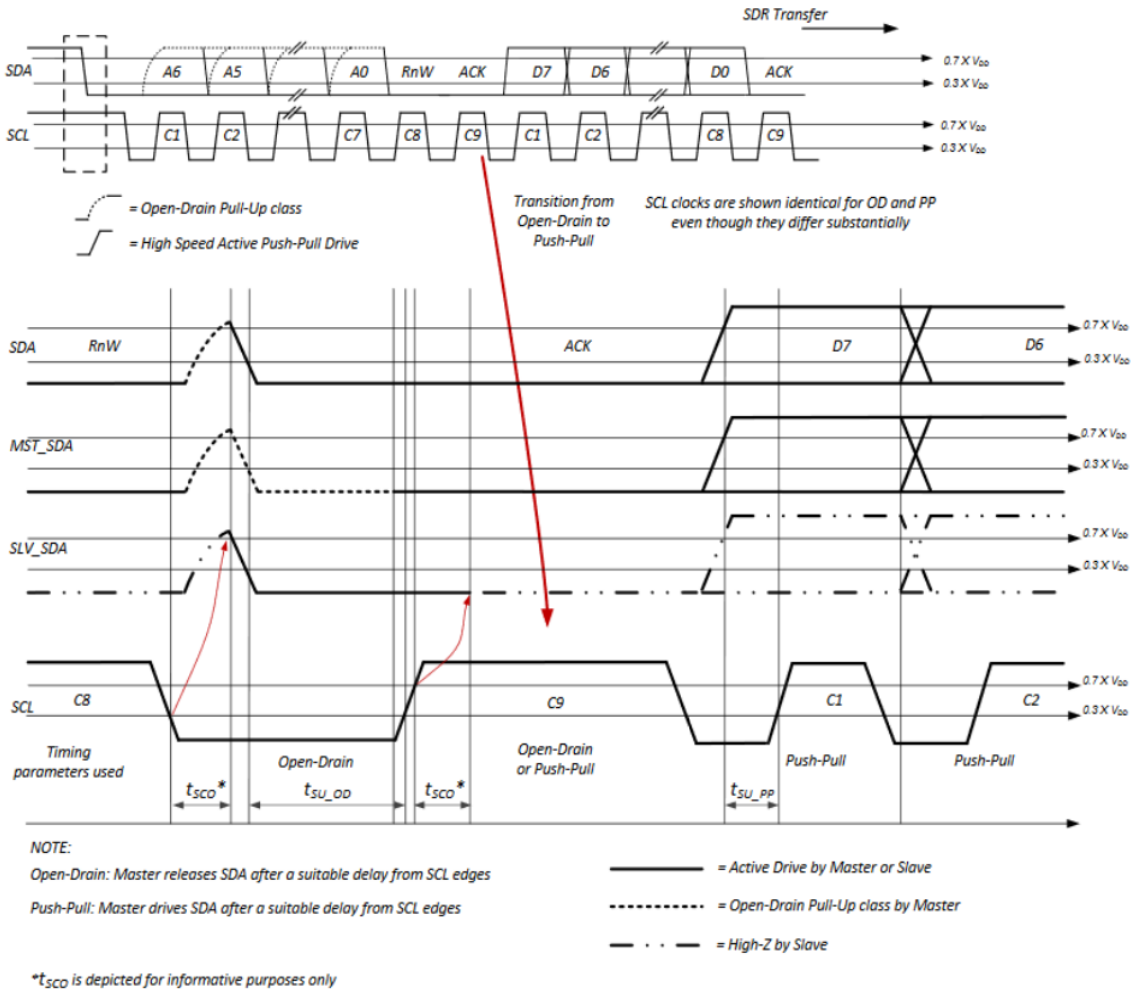


Figure 18. Timing definition for devices on the I3C bus

3.8.5 CAN switching specifications

See General switching specifications.

3.9 Human Machine Interface (HMI) modules

3.9.1 General Purpose Input/Output (GPIO)

See General switching specifications.

3.9.2 Flexible IO controller (FlexIO)

Table 57. FlexIO timing specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
t_{ODS}	Output delay skew between any two FlexIO_Dx pins configured as outputs that toggle on same internal clock cycle	0	—	10	ns	[1]
t_{IDS}	Input delay skew between any two FlexIO_Dx pins configured as inputs that are sampled on the same internal clock cycle	0	—	10	ns	[1]

[1] Assumes pins muxed on same VDD_IO domain with same load

4 Package dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
48-pin QFN	SOT619-17(DD)

5 Pinout

5.1 Pinout table

Table 58. KW47 Package pinout

Pin Name	KW47 48QFN	Pinmux Assignment	Pad Settings	Alternate Functions
PTB3	1	**ALT0** - ADC0_B13 **ALT1** - PTB3 **ALT2** - LPSPI1_SOUT **ALT3** - LPUART1_RX **ALT5** - TPM1_CH3 **ALT9** - FLEXIO0_D29	**IO Supply** - VDD_IO_ABC **Pad type** - 50 MHZ **Default** - ADC0_B13	**VDD SYS** - WUU0_P14

Table continues on the next page...

Table 58. KW47 Package pinout*...continued*

Pin Name	KW47 48QFN	Pinmux Assignment	Pad Settings	Alternate Functions
PTB4	2	**ALT1** - PTB4 **ALT2** - LPSPI1_PCS3 **ALT3** - LPUART1_CTS_b **ALT4** - LPI2C1_SDA **ALT5** - I3C0_SDA **ALT6** - TRGMUX0_IN0 **ALT9** - FLEXIO0_D30	**IO Supply** - VDD_IO_ABC **Pad type** - 50 MHZ + I3C + RXF **Default** - DISABLED	**VDD SYS** - WUU0_P15
PTB5	3	**ALT1** - PTB5 **ALT2** - LPSPI1_PCS2 **ALT3** - LPUART1_RTS_b **ALT4** - LPI2C1_SCL **ALT5** - I3C0_SCL **ALT6** - TRGMUX0_OUT0 **ALT9** - FLEXIO0_D31	**IO Supply** - VDD_IO_ABC **Pad type** - 50 MHZ + RXF **Default** - DISABLED	—
VDD_IO_ABC	4	**ALT0** - VDD_IO_ABC	**IO Supply** - VDD_IO_ABC **Default** - VDD_IO_ABC	—
SWITCH_WAKEUP_B	5	**ALT0** - SWITCH_WAKEUP_B	**IO Supply** - VDD_SWI **Default** - SWITCH_WAKEUP_B	—
VDD_SWITCH	6	**ALT0** - VDD_SWITCH	**IO Supply** - VDD_SWI **Default** - VDD_SWITCH	—
VOUT_SWITCH	7	**ALT0** - VOUT_SWITCH	**IO Supply** - VDD_SWI **Default** - VOUT_SWITCH	—
PTA0	8	**ALT1** - PTA0 **ALT2** - CMP0_OUT **ALT3** - LPUART0_CTS_b **ALT4** - RF_GPO_11 **ALT5** - TPM0_CH4 **ALT6** - FLEXIO0_D0 **ALT7** - SWD_DIO	**IO Supply** - VDD_IO_ABC **Pad type** - 25 MHZ **Default** - SWD_DIO	**VDD SYS** - WUU0_P0
PTA1	9	**ALT1** - PTA1 **ALT2** - CMP1_OUT	**IO Supply** - VDD_IO_ABC **Pad type** - 25 MHZ	—

Table continues on the next page...

Table 58. KW47 Package pinout*...continued*

Pin Name	KW47 48QFN	Pinmux Assignment	Pad Settings	Alternate Functions
		ALT3 - LPUART0_RTS_b **ALT4** - RF_GPO_10 **ALT5** - TPM0_CH5 **ALT6** - FLEXIO0_D1 **ALT7** - SWD_CLK	**Default** - SWD_CLK	
PTA4	10	**ALT0** - ADC0_A10/CMP0_IN0 **ALT1** - PTA4 **ALT3** - RF_GPO_9 **ALT4** - TPM0_CLKIN **ALT5** - TRACE_SWO **ALT6** - FLEXIO0_D4 **ALT7** - BOOT_CONFIG	**IO Supply** - VDD_IO_ABC **Pad type** - 25 MHZ **Default** - BOOT_CONFIG	**VDD SYS** - WUU0_P2/ RF_XTAL_OUT_ENABLE
PTA16	11	**ALT0** - ADC0_A12 **ALT1** - PTA16 **ALT2** - LPSPI0_PCS0 **ALT3** - EWM0_OUT_b **ALT4** - LPI2C0_SCLS **ALT5** - TPM0_CH4 **ALT6** - LPUART0_RX **ALT7** - RF_GPO_8 **ALT9** - FLEXIO0_D5	**IO Supply** - VDD_IO_ABC **Pad type** - 25 MHZ **Default** - ADC0_A12	**VDD SYS** - WUU0_P19/ RF_NOT_ALLOWED
PTA17	12	**ALT0** - ADC0_A13 **ALT1** - PTA17 **ALT2** - LPSPI0_SIN **ALT3** - EWM0_IN **ALT4** - LPI2C0_SDAS **ALT5** - TPM0_CH5 **ALT6** - LPUART0_TX **ALT7** - RF_GPO_7 **ALT8** - RF_GPO_8 **ALT9** - FLEXIO0_D6	**IO Supply** - VDD_IO_ABC **Pad type** - 25 MHZ **Default** - ADC0_A13	**VDD SYS** - WUU0_P3/ RF_NOT_ALLOWED

Table continues on the next page...

Table 58. KW47 Package pinout*...continued*

Pin Name	KW47 48QFN	Pinmux Assignment	Pad Settings	Alternate Functions
		ALT11 - RF_EXT_XTAL_REQUEST/RF_GPO_7		
PTA18	13	**ALT0** - CMP1_IN1 **ALT1** - PTA18 **ALT2** - LPSPI0_SOUT **ALT3** - LPUART0_CTS_b **ALT4** - LPI2C0_SDA **ALT5** - TPM0_CH3 **ALT6** - RF_GPO_0 **ALT10** - LPUART0_RX **ALT11** - SPC0_LPREQ	**IO Supply** - VDD_IO_ABC **Pad type** - I2CFP **Default** - CMP1_IN1	**VDD SYS** - WUU0_P20
PTA19	14	**ALT0** - CMP1_IN0 **ALT1** - PTA19 **ALT2** - LPSPI0_SCK **ALT3** - LPUART0_RTS_b **ALT4** - LPI2C0_SCL **ALT5** - TPM0_CH2 **ALT6** - RF_GPO_1	**IO Supply** - VDD_IO_ABC **Pad type** - I2CFP **Default** - CMP1_IN0	**VDD SYS** - WUU0_P4
VDD_LDO_CORE	15	**ALT0** - VDD_LDO_CORE	**IO Supply** - VDD_IO_ABC **Default** - VDD_LDO_CORE	—
VDD_CORE	16	**ALT0** - VOUT_CORE	**IO Supply** - VDD_IO_ABC **Default** - VOUT_CORE	—
PTA20	17	**ALT0** - ADC0_A14/CMP0_IN3 **ALT1** - PTA20 **ALT2** - LPSPI0_PCS2 **ALT3** - LPUART0_TX **ALT4** - EWM0_IN **ALT5** - TPM0_CH1 **ALT6** - RF_GPO_2 **ALT8** - FLEXIO0_D7	**IO Supply** - VDD_IO_ABC **Pad type** - 25 MHZ **Default** - ADC0_A14/CMP0_IN3	—

Table continues on the next page...

Table 58. KW47 Package pinout*...continued*

Pin Name	KW47 48QFN	Pinmux Assignment	Pad Settings	Alternate Functions
		ALT11 - LPUART0_RTS_b		
PTA21	18	**ALT0** - ADC0_A15/CMP0_IN2 **ALT1** - PTA21 **ALT2** - LPSPI0_PCS3 **ALT3** - LPUART0_RX **ALT4** - EWM0_OUT_b **ALT5** - TPM0_CH0 **ALT6** - RF_GPO_3 **ALT7** - RF_GPO_7 **ALT8** - FLEXIO0_D8 **ALT9** - RF_GPO_10 **ALT11** - LPUART0_CTS_b	**IO Supply** - VDD_IO_ABC **Pad type** - 25 MHZ **Default** - ADC0_A15/CMP0_IN2	**VDD SYS** - WUU0_P5
VSS_DCDC	19	**ALT0** - VSS_DCDC	**IO Supply** - VDD_DCDC **Default** - VSS_DCDC	—
DCDC_LX	20	**ALT0** - DCDC_LX	**IO Supply** - VDD_DCDC **Default** - DCDC_LX	—
VDD_IO_D	21	**ALT0** - VDD_IO_D	**IO Supply** - VDD_IO_D **Default** - VDD_IO_D	—
VOUT_SYS/ VDD_SYS	22	**ALT0** - VOUT_SYS/VDD_SYS	**IO Supply** - VDD_IO_D **Default** - VOUT_SYS/VDD_SYS	—
PTD0	23	**ALT0** - ADC0_A5 **ALT1** - PTD0 **ALT3** - RESET_b	**IO Supply** - VDD_IO_D **Pad type** - RST **Default** - RESET_b	—
PTD1	24	**ALT0** - ADC0_B5 **ALT1** - PTD1 **ALT2** - SPC0_LPREQ **ALT3** - NMI_b **ALT4** - RF_GPO_4 **ALT5** - RF_GPO_7	**IO Supply** - VDD_IO_D **Pad type** - AON **Default** - ADC0_B5	—

Table continues on the next page...

Table 58. KW47 Package pinout*...continued*

Pin Name	KW47 48QFN	Pinmux Assignment	Pad Settings	Alternate Functions
		ALT7 - LPTMR2_TRIG_OUT_b		
PTD2	25	**ALT0** - ADC0_A6 **ALT1** - PTD2 **ALT2** - LPTMR0_ALT3 **ALT3** - TAMPER0 **ALT4** - RF_GPO_5 **ALT5** - TPM2_CH0 **ALT7** - LPTMR1_TRIG_OUT_b	**IO Supply** - VDD_IO_D **Pad type** - AON **Default** - ADC0_A6	—
PTD3	26	**ALT0** - ADC0_B6 **ALT1** - PTD3 **ALT2** - LPTMR1_ALT3 **ALT3** - TAMPER1 **ALT4** - RF_GPO_6 **ALT5** - TPM2_CH1 **ALT6** - TRGMUX0_IN2 **ALT7** - LPTMR0_TRIG_OUT_b	**IO Supply** - VDD_IO_D **Pad type** - AON **Default** - ADC0_B6	—
PTD4	27	**ALT0** - XTAL32K **ALT1** - PTD4 **ALT2** - LPTMR0_ALT2 **ALT3** - TAMPER2	**IO Supply** - VDD_IO_D **Pad type** - AON **Default** - XTAL32K	—
PTD5	28	**ALT0** - EXTAL32K **ALT1** - PTD5 **ALT2** - LPTMR1_ALT2	**IO Supply** - VDD_IO_D **Pad type** - AON **Default** - EXTAL32K	—
VDD_ANA	29	**ALT0** - VDD_ANA	**IO Supply** - VDD_ANA **Default** - VDD_ANA	—
VREF_OUT	30	**ALT0** - VREFO	**IO Supply** - VDD_ANA **Default** - VREF_OUT	—
VSS	49	**ALT0** - VSS	**IO Supply** - VDD_ANA **Default** - VSS	—

Table continues on the next page...

Table 58. KW47 Package pinout...*continued*

Pin Name	KW47 48QFN	Pinmux Assignment	Pad Settings	Alternate Functions
XTAL_OUT	31	**ALT0** - XTAL_OUT	**IO Supply** - VDD_RF **Default** - XTAL_OUT	—
XTAL	32	**ALT0** - XTAL	**IO Supply** - VDD_RF **Default** - XTAL	—
EXTAL	33	**ALT0** - EXTAL	**IO Supply** - VDD_RF **Default** - EXTAL	—
VDD_RF	34	**ALT0** - VDD_RF	**IO Supply** - VDD_RF **Default** - VDD_RF	—
ANT_2P4GHZ	35	**ALT0** - ANT_2P4GHZ	**IO Supply** - VDD_RF **Default** - ANT_2P4GHZ	—
VPA_2P4GHZ	36	**ALT0** - VPA_2P4GHZ	**IO Supply** - VDD_RF **Default** - VPA_2P4GHZ	—
PTC0	37	**ALT1** - PTC0 **ALT2** - LPSPI1_PCS2 **ALT3** - CAN0_TX [1] **ALT4** - I3C0_SDA **ALT5** - TPM1_CH0 **ALT7** - LPI2C1_SCL **ALT9** - FLEXIO0_D16	**IO Supply** - VDD_IO_ABC **Pad type** - I2CFP + I3C **Default** - DISABLED	**VDD SYS** - WUU0_P7
PTC1	38	**ALT1** - PTC1 **ALT2** - LPSPI1_PCS3 **ALT3** - CAN0_RX [1] **ALT4** - I3C0_SCL **ALT5** - TPM1_CH1 **ALT7** - LPI2C1_SDA **ALT9** - FLEXIO0_D17	**IO Supply** - VDD_IO_ABC **Pad type** - I2CFP **Default** - DISABLED	**VDD SYS** - WUU0_P8
PTC2	39	**ALT1** - PTC2 **ALT2** - LPSPI1_SOUT **ALT3** - LPUART1_RX **ALT4** - LPI2C1_SCLS	**IO Supply** - VDD_IO_ABC **Pad type** - 25 MHZ **Default** - DISABLED	**VDD SYS** - WUU0_P9

Table continues on the next page...

Table 58. KW47 Package pinout...*continued*

Pin Name	KW47 48QFN	Pinmux Assignment	Pad Settings	Alternate Functions
		ALT5 - TPM1_CH2 **ALT7** - I3C0_PUR **ALT9** - FLEXIO0_D18 **ALT11** - CAN1_RX [1]		
PTC3	40	**ALT1** - PTC3 **ALT2** - LPSPI1_SCK **ALT3** - LPUART1_TX **ALT4** - LPI2C1_SDAS **ALT5** - TPM1_CH3 **ALT9** - FLEXIO0_D19 **ALT11** - CAN1_TX [1]	**IO Supply** - VDD_IO_ABC **Pad type** - 25 MHZ **Default** - DISABLED	—
VDD_CORE	41	**ALT0** - VDD_CORE	**IO Supply** - VDD_IO_ABC **Default** - VDD_CORE	—
PTC4	42	**ALT1** - PTC4 **ALT2** - LPSPI1_SIN **ALT3** - CAN0_TX [1] **ALT4** - LPI2C1_SCL **ALT6** - TPM2_CH0 **ALT9** - FLEXIO0_D20	**IO Supply** - VDD_IO_ABC **Pad type** - I2CFP **Default** - DISABLED	**VDD SYS** - WUU0_P10
PTC5	43	**ALT1** - PTC5 **ALT2** - LPSPI1_PCS0 **ALT3** - CAN0_RX [1] **ALT4** - LPI2C1_SDA **ALT5** - TPM1_CH4 **ALT6** - TPM2_CH1 **ALT9** - FLEXIO0_D21	**IO Supply** - VDD_IO_ABC **Pad type** - I2CFP **Default** - DISABLED	**VDD SYS** - WUU0_P22
PTC6	44	**ALT0** - ADC0_A8 **ALT1** - PTC6 **ALT2** - LPSPI1_PCS1 **ALT5** - TPM1_CH5	**IO Supply** - VDD_IO_ABC **Pad type** - 25 MHZ **Default** - ADC0_A8	**VDD SYS** - WUU0_P11

Table continues on the next page...

Table 58. KW47 Package pinout...*continued*

Pin Name	KW47 48QFN	Pinmux Assignment	Pad Settings	Alternate Functions
		ALT9 - FLEXIO0_D22 **ALT11** - CAN1_RX [1]		
PTC7	45	**ALT0** - DISABLED **ALT1** - PTC7 **ALT2** - TRGMUX0_IN3 **ALT3** - TRGMUX0_OUT3 **ALT4** - SFA0_CLK **ALT5** - TPM1_CLKIN **ALT6** - TPM2_CLKIN **ALT7** - CLKOUT **ALT9** - FLEXIO0_D23 **ALT10** - NMI_b **ALT11** - CAN1_TX [1]	**IO Supply** - VDD_IO_ABC **Pad type** - 100 MHz **Default** - DISABLED	**VDD SYS** - WUU0_P12/ NMI_b/ RF_NOT_ALLOWED
PTB0	46	**ALT0** - ADC0_B10 **ALT1** - PTB0 **ALT2** - LPSPI1_PCS0 **ALT3** - CAN1_RX [1] **ALT5** - TPM1_CH0 **ALT9** - FLEXIO0_D26	**IO Supply** - VDD_IO_ABC **Pad type** - 50 MHZ **Default** - ADC0_B10	**VDD SYS** - WUU0_P13
PTB1	47	**ALT0** - ADC0_B11 **ALT1** - PTB1 **ALT2** - LPSPI1_SIN **ALT3** - CAN1_TX [1] **ALT5** - TPM1_CH1 **ALT9** - FLEXIO0_D27	**IO Supply** - VDD_IO_ABC **Pad type** - 50 MHZ **Default** - ADC0_B11	—
PTB2	48	**ALT0** - ADC0_B12 **ALT1** - PTB2 **ALT2** - LPSPI1_SCK **ALT3** - LPUART1_TX **ALT5** - TPM1_CH2 **ALT9** - FLEXIO0_D28	**IO Supply** - VDD_IO_ABC **Pad type** - 50 MHZ **Default** - ADC0_B12	—

[1] This signal is not available for the parts without CAN module.

5.2 Recommended connection for unused analog and digital pins

Table 59 shows the recommended connections for pins if those pins are not used in the application of customer

Table 59. Recommended connection for unused interfaces

Pin Type	Pin function	Recommendation	Comments
Power	VDD_LDO_CORE	Connect to VOUT_CORE and VSS	When LDO_CORE is not used, the VDD_LDO_CORE and VDD_CORE need to be shorted together and supplied at the VDD_CORE voltage level. The LDO-CORE can be disabled in software.
Power	VOUT_CORE	Connect to VDD_LDO_CORE and VSS	When the LDO is not used, the input and output should be connected together and tied to ground through a 10 kΩ resistor. The regulator should also be disabled in software.
Power	VOUT_SYS	1.5 µF - 10 µF Capacitor	Connect a capacitor between range 1.5 µF and 10 µF as specified in the LDO_SYS electrical specifications table. External capacitors are needed for output stability
Power	VDD_DCDC	Ground	When the DCDC is not used, the input should be tied to VSS through a 10 kΩ resistor.
Power	DCDC_LX	Float	—
Power	VDD_IO_D	Must be powered	VDD_IO_D is used to power parts of the system power controller (SPC) and must be powered to use the chip. If LDO_SYS is not being used, then tie VDD_IO_D to VOUT_SYS and supply power from an external source. The regulator should also be disabled in software.
Power	VDD_SWITCH	Must be powered	Powers FRO16 and a portion of RAM.
Power	VOUT_SWITCH	Float	—
Power	VDD_IO_ABC	Must be powered	VDD_IO_ABC powers the mux logic for PORTA, PORTB and PORTC. It must be powered during POR. The recommendation is to keep it powered, but it can be connected to the output of the Smart Power Switch and be left floating in shelf storage mode.
Power	VPA_2P4GHz	Float/Connect to ANT_2P4GHZ	**Float**.The pin must be left floating when the radio is not used in the application. **Connect to ANT_2P4GHz**The pin shall be connected to the ANT pin in applications that use the radio.
Power	VDD_ANA	Float	—
Power	VREFH	Always connect to VDD_ANA potential	Always connect to VDD_ANA potential

Table continues on the next page...

Table 59. Recommended connection for unused interfaces...*continued*

Pin Type	Pin function	Recommendation	Comments
Power	VREFL	Always connect to VSS potential	Always connect to VSS potential
Power	VSS_ANA	Always connect to VSS potential	Always connect to VSS potential
Power	VREFO	220 nF capacitor	220 nF capacitor if VREF is used otherwise Float
Power	VSS_DCDC	Always connect to VSS potential	Always connect to VSS potential
Power	VSS_RF	Always connect to VSS potential	Always connect to VSS potential
Analog/non-GPIO	ADC*n_x*	Float	—
Analog/non-GPIO	VREFO	Float	Analog output - Float
Analog/non-GPIO	TAMPERx	Float	—
Analog/non-GPIO	RTC_WAKEUP_B	Float	—
Analog/non-GPIO	RTC_RTCCLKOUT	Float	—
Analog/non-GPIO	EXTAL32K	Float	—
Analog/non-GPIO	XTAL32K	Float	Analog output - Float
Analog/non-GPIO	EXTAL_32M	Float	—
Analog/non-GPIO	XTAL_32M	Float	Analog output - Float
GPIO/Analog	PTx/CMP*n*_IN*x*	Float	Float (default is analog input)
GPIO/Digital	PTD1/NMI_b	10kΩ pullup or disable and float	Pull high or disable in PCR & FOPT and float
GPIO/Digital	PTx	Float	Float (default is disabled)
Digital/non-GPIO	SWITCH_WAKEUP_B	Float	Enable internal pull-up

5.3 Pinouts diagram

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

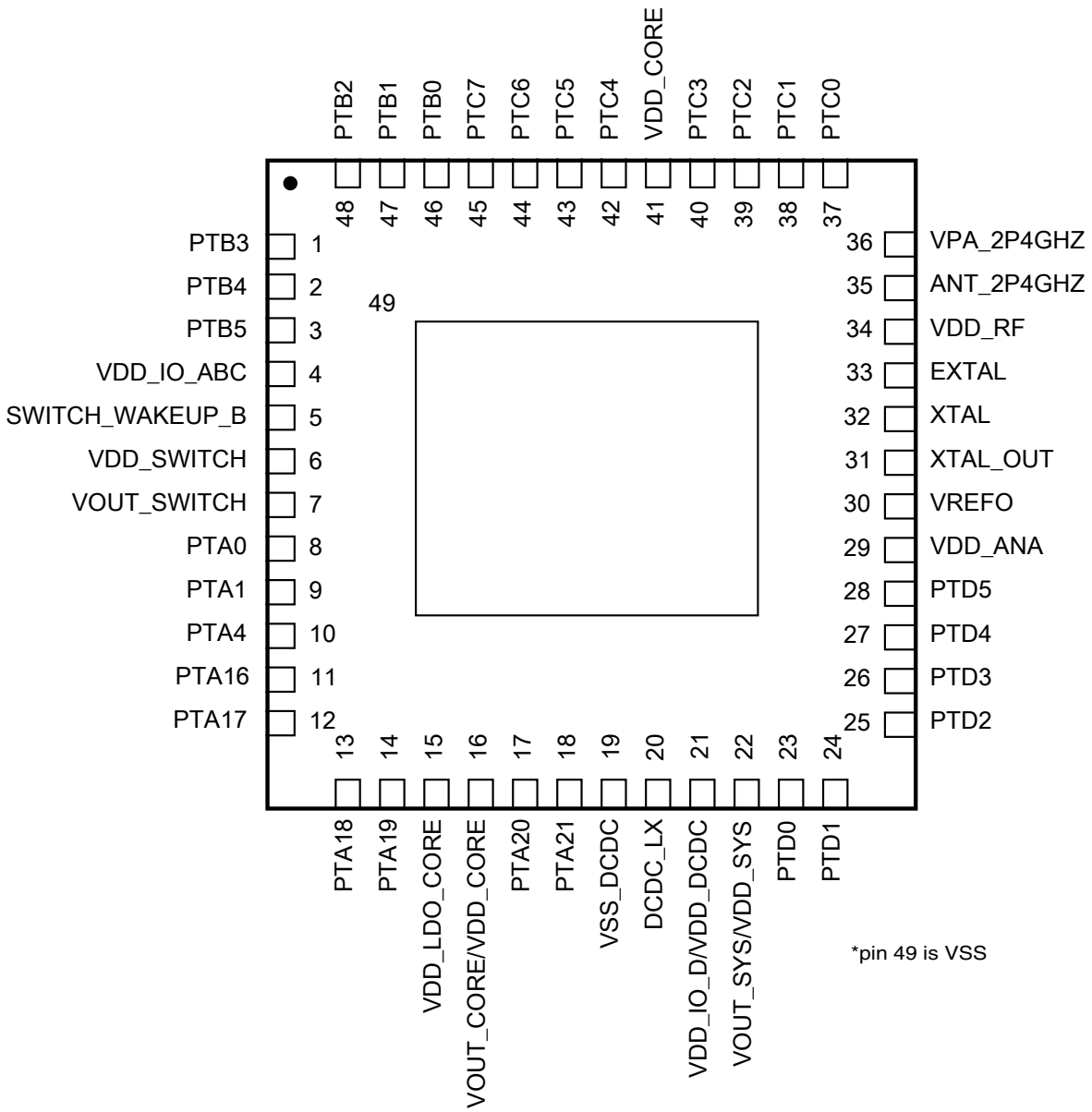


Figure 19. 48-pin HVQFN package pinout diagram

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to nxp.com and perform a part number search for the following device numbers: KW47

7 Part identification

Part numbers for the device have fields that identify the specific part. Use the values of these fields to determine the specific part.

7.1 Part number format

Part numbers for this device have the following format:

B R PF RV FS SF T PG SR PT

Table 60. Part number fields descriptions

Field	Description	Values
B	Brand	• KW47
R	Radio	• B = Bluetooth LE • Z = No Radio
PF	Product Family	• 42
RV	Radio Version	• Z = Upgradable • 0 = Not Applicable (No Radio)
FS	Flash Size /SRAM	• 8 = 1 MB + 512 KB/136 KB + 171 KB • 9 = 1 MB + 512 KB/264 KB + 171 KB • B = 2 MB + 512 KB/264 KB + 171 KB
SF	Sub Feature	• 2 = Secure Enclave • 3 = Secure Enclave and CAN • 6 = Secure Enclave and LCE • 7 = Secure Enclave, CAN and LCE
T	Temperature	• A = Automotive, -40 ºC to + 105 ºC (Ta), -40 ºC to + 125 ºC (Tj)
PG	Package	• FT = 48 HVQFN “Wettable”, 7 mm x 7 mm, 0.5p
SR	Silicon Revision	• A = Initial Mask Set • B = Production Release Mask Set
PT	Packaging Type	• R = Tape and Reel • T = Tray

7.2 Example

This is an example part number:

KW47B42ZB7AFTBT

7.3 Package marking information

The KW47 package has the following top-side marking:

- First line: aaaaaaa
- Second line: aaaaaa
- Third line: mmmmm

- Fourth line: xxxywwxx

Table 61. Package marking

Identifier	Description
a	Reduced part number code, refer to Part Number Format table
m	Mask set
y	Year
w	Work week
x	NXP internal use

8 Terminology and guidelines

8.1 Definitions

Key terms are defined in the following table:

Table 62. Definitions

Term	Definition
Rating	A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure: • *Operating ratings* apply during operation of the chip. • *Handling ratings* apply when the chip is not powered. ***Note:*** *The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.*
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that: • Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions ***Note:*** *Typical values are provided as design guidelines and are neither tested nor guaranteed.*

8.2 Examples

Operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

Operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

Operating behavior that includes a *typical value*:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

Figure 20. Examples

8.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Table 63. Typical-value conditions

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	Supply voltage	3.3	V

8.4 Relationship between ratings and operating requirements

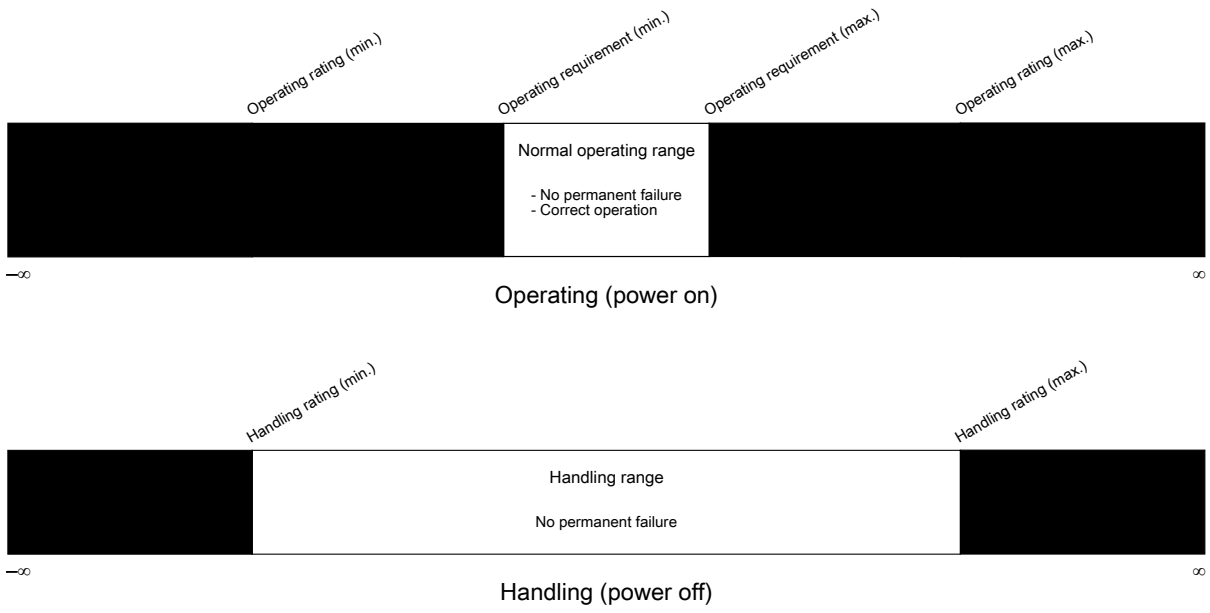


Figure 21. Relationship between ratings and operating requirements

8.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

9 Abbreviations and acronyms

The following table provides the list of abbreviations and acronyms their definitions.

Table 64. Abbreviations and acronyms and their definition

Abbreviations and acronyms	Definitions
ADC	Analog-to-Digital Converter
AXBS	Crossbar Switch
CMC	Core Mode Controller
CRC	Cyclic Redundancy Check
CTI	Cross Trigger Interface
DAP	Debug Access Port
DMA	Direct Memory Access
DSP	Digital Signal Processing

Table continues on the next page...

Table 64. Abbreviations and acronyms and their definition...*continued*

Abbreviations and acronyms	Definitions
DWT	Data Watchpoint and Trace
EWM	External Watchdog Monitor
FRO	Free Running Oscillator
FMC	Flash Memory Controller
FPU	Floating Point Unit
GPIO	General-purpose Input and Output
I3C	Improved Inter-Integrated Circuit
ITM	Instruction Trace Macrocell
LPCMP	Low Power Comparator
LPI2C	Low Power Inter-Integrated Circuit
LPIT	Low Power Periodic Interrupt Timer
LPSPI	Low Power Serial Peripheral Interface
LPTMR	Low-Power Timer
LPUART	Low Power Universal Asynchronous Receiver/ Transmitter
MPU	Memory Protection Unit
MRCC	Module Reset and Clock Control
MSCM	Miscellaneous System Control Module
MU	Messaging Unit
NBU	Narrowband Unit
NPX	FMC with NVM PRINCE Encryption and Decryption
NVIC	Nested Vectored Interrupt Controller
NVM	Non-Volatile Memory
OSC	Oscillator
RFMC	Radio Mode Controller
RTC	Real Time Clock
SEMA42	Semaphore Module
SCG	System Clock Generator
SFA	Signal Frequency Analyzer
SMSCM	Secure Miscellaneous System Control Module
SPC	System Power Controller
SWD	Serial Wire Debug
TPIU	Trace Port Interface Unit

Table continues on the next page...

Table 64. Abbreviations and acronyms and their definition...*continued*

Abbreviations and acronyms	Definitions
TPM	Timer/PWM Module
TRDC	Trusted Resource Domain Controller
TRNG	True Random Number Generator
TRGMUX	Trigger Multiplexer
VREF	Voltage Reference
WDOG	Watchdog
WUU	Wake-Up Unit
LCE	Localization Compute Engine

10 Revision history

The following table provides a revision history for this document.

Table 65. Revision History

Rev. No.	Date	Substantial Changes
KW47 v4.0	December 18th 2025	Initial public release

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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