Atmel SAM R21E / SAM R21G

SMART ARM-Based Wireless Microcontroller

PRELIMINARY DATASHEET SUMMARY

Description

The Atmel® | SMART™ SAM R21 is a series of low-power microcontrollers using the 32-bit ARM® Cortex®-M0+ processor and an integrated ultra-low power 2.4GHz ISM band transceiver. SAM R21 devices are available in 32- and 48-pin packages with up to 256KB Flash, 32KB of SRAM and are operating at a maximum frequency of 48MHz and reach 2.14 Coremark/MHz. They are designed for simple and intuitive migration with identical peripheral modules, hex compatible code, identical linear address map and pin compatible migration paths between all devices in the product series. All devices include intelligent and flexible peripherals, Atmel Event System for inter-peripheral signaling, and support for capacitive touch button, slider and wheel user interfaces.

The Atmel SAM R21 devices provide the following features: In-system programmable Flash, 12-channel direct memory access (DMA) controller, 12-channel Event System, programmable interrupt controller, up to 28 programmable I/O pins, ultra-low power 2.4GHz ISM band transceiver with a data rate of 250kB/s, 32-bit real-time clock and calendar, three 16-bit Timer/Counters (TC) and three 16-bit Timer/Counters for Control (TCC), where each TC can be configured to perform frequency and waveform generation, accurate program execution timing or input capture with time and frequency measurement of digital signals. The TCs can operate in 8- or 16-bit mode, selected TCs can be cascaded to form a 32-bit TC, and the three Timer/Counters for Control have extended functions optimized for motor, lighting and other control applications. The series provide one full-speed USB 2.0 embedded host and device interface; up to five Serial Communication Modules (SERCOM) that each can be configured to act as an USART, UART, SPI, I2C up 3.4MHz and LIN slave; up to eight channel 350ksps 12-bit ADC with programmable gain and optional oversampling and decimation supporting up to 16-bit resolution, two analog comparators with window mode, Peripheral Touch Controller supporting up to 48 buttons, sliders, wheels and proximity sensing; programmable Watchdog Timer, brown-out detector and power-on reset and two-pin Serial Wire Debug (SWD) program and debug interface.

All devices have accurate and low-power external and internal oscillators. All oscillators can be used as a source for the system clock. Different clock domains can be independently configured to run at different frequencies, enabling power saving by running each peripheral at its optimal clock frequency, and thus maintaining a high CPU frequency while reducing power consumption.

The SAM R21 devices have two software-selectable sleep modes, idle and standby. In idle mode the CPU is stopped while all other functions can be kept running. In standby all clocks and functions are stopped expect those selected to continue running. The device supports SleepWalking, which is the module's ability to wake itself up and wake up its own clock, and hence perform predefined tasks without waking up the CPU. The CPU can then be only woken on a need basis, e.g. a threshold is crossed or a result is ready. The Event System supports synchronous and asynchronous events, allowing peripherals to receive, react to and send events even in standby mode.

The Flash program memory can be reprogrammed in-system through the SWD interface. The same interface can be used for non-intrusive on-chip debug of application code. A boot loader running in the device can use any communication interface to download and upgrade the application program in the Flash memory.

The SAM R21 devices are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers and evaluation kits.

Features

- Processor
  - ARM Cortex-M0+ CPU running at up to 48MHz
    - Single-cycle hardware multiplier
    - Micro Trace Buffer (MTB)
- Memories
  - 256/128/64KB in-system self-programmable Flash
  - 32/16/8KB SRAM
- System
  - Power-on reset (POR) and brown-out detection (BOD)
  - Internal and external clock options with 48MHz Digital Frequency Locked Loop (DFLL48M) and 48MHz to 96MHz Fractional Digital Phase Locked Loop (FDPLL96M)
  - External Interrupt Controller (EIC)
  - Up to 15 external interrupts
  - One non-maskable interrupt
  - Two-pin Serial Wire Debug (SWD) programming, test and debugging interface
- Low Power
  - Idle and standby sleep modes
  - SleepWalking peripherals
- Peripherals
  - 12-channel Direct Memory Access Controller (DMAC)
  - 12-channel Event System
  - Integrated Ultra Low Power Transceiver for 2.4GHz ISM Band
    - 250kB/s data rate
    - -99dBm RX Sensitivity; TX Output Power up to +4dBm
    - Hardware Assisted MAC (Auto-Acknowledge, Auto-Retry)
    - SFD-Detection; Spreading; De-Spreading; Framing; CRC-16 Computation
    - Antenna Diversity and TX/RX Control
    - 128 Byte TX/RX Frame Buffer
    - Integrated 16MHz Crystal Oscillator (external crystal needed)
    - PLL synthesizer with 5 MHz and 500 kHz channel spacing for 2.4GHz ISM band
    - Hardware Security (AES, True Random Generator)
  - Three 16-bit Timer/Counters (TC), configurable as either:
    - One 16-bit TC with compare/capture channels
    - One 8-bit TC with compare/capture channels
    - One 32-bit TC with compare/capture channels, by using two TCs
  - Three 16-bit Timer/Counters for Control (TCC), with extended functions:
    - Up to four compare channels with optional complementary output
    - Generation of synchronized pulse width modulation (PWM) pattern across port pins
    - Deterministic fault protection, fast decay and configurable dead-time between complementary output
    - Dithering that increase resolution with up to 5 bit and reduce quantization error
  - 32-bit Real Time Counter (RTC) with clock/calendar function
  - Watchdog Timer (WDT)
  - CRC-32 generator
  - One full-speed (12Mbps) Universal Serial Bus (USB) 2.0 interface
    - Embedded host and device function
    - Eight endpoints
  - Up to five Serial Communication Interfaces (SERCOM), each configurable to operate as either:
    - USART with full-duplex and single-wire half-duplex configuration
    - I^2C up to 3.4MHz
    - SPI
    - LIN slave
  - One 12-bit, 350ksps Analog-to-Digital Converter (ADC) with up to eight external channels
    - Differential and single-ended input
    - 1/2x to 16x programmable gain stage
    - Automatic offset and gain error compensation
    - Oversampling and decimation in hardware to support 13-, 14-, 15- or 16-bit resolution
  - Two Analog Comparators (AC) with window compare function
  - Peripheral Touch Controller (PTC)
    - 48-channel capacitive touch and proximity sensing
- I/O and Package
  - 16/28 programmable I/O pins
  - 32-pin and 48-pin QFN

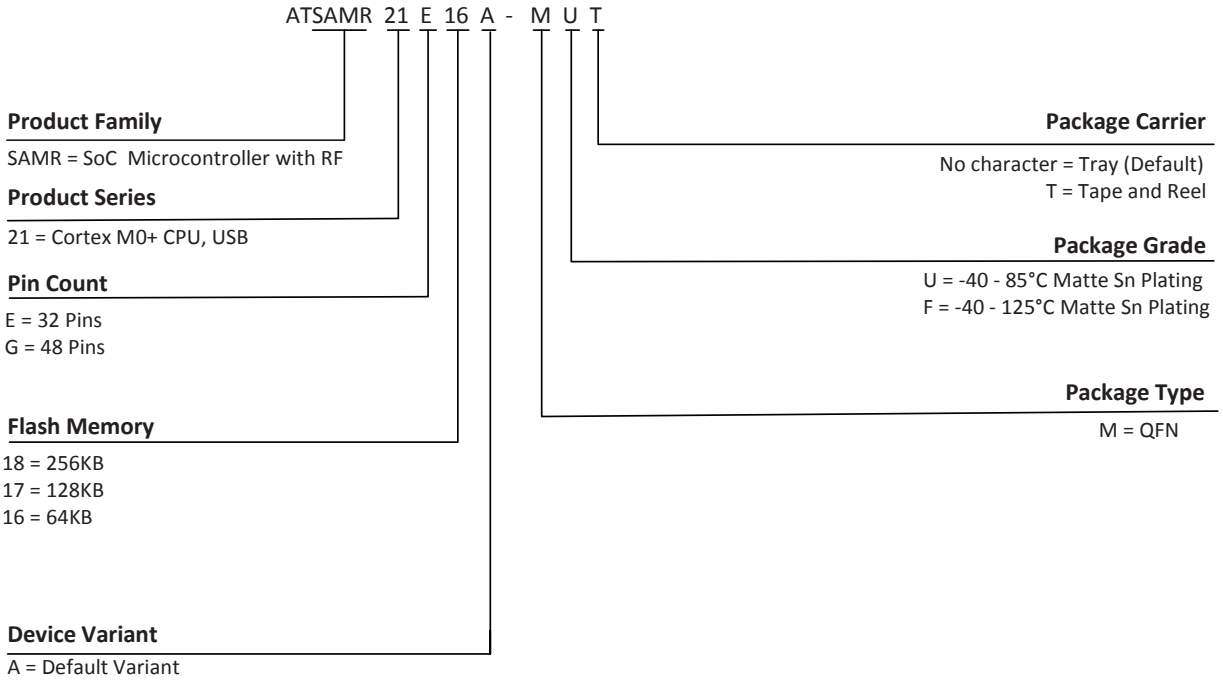
- Operating Voltage
  - 1.8V – 3.6V
- Temperature Range
  - -40°C to 85°C Industrial
  - -40°C to 125°C Industrial

1. Configuration Summary

	SAM R21G	SAM R21E
Pins	48	32
General Purpose I/O-pins (GPIOs)	28	16
Flash	256/128/64KB	256/128/64KB
SRAM	32/16/8KB	32/16/8KB
Timer Counter (TC) instances	3	3
Waveform output channels per TC instance	2	2
Timer Counter for Control (TCC) instances	3	3
Waveform output channels per TCC	4/4/2	4/4/2
DMA channels	12	12
USB interface	1	1
Serial Communication Interface (SERCOM) instances	5+1(1)	4+1(1)
Inter-IC Sound (I^2S) interface	No	No
Analog-to-Digital Converter (ADC) channels	8	4
Analog Comparators (AC)	2	2
Digital-to-Analog Converter (DAC) channels	No	No
Real-Time Counter (RTC)	Yes	Yes
RTC alarms	1	1
RTC compare values	1 32-bit value or 2 16-bit values	1 32-bit value or 2 16-bit values
External Interrupt lines	15	14
Peripheral Touch Controller (PTC) X and Y lines	8x6	6x2
Maximum CPU frequency	48MHz	
Packages	QFN	QFN
32.768kHz crystal oscillator (XOSC32K)	Yes	No
Oscillators	16MHz crystal oscillator for 2.4GHz TRX (XOSCRF) 0.4-32MHz crystal oscillator (XOSC) 32.768kHz internal oscillator (OSC32K) 32kHz ultra-low-power internal oscillator (OSCULP32K) 8MHz high-accuracy internal oscillator (OSC8M) 48MHz Digital Frequency Locked Loop (DFLL48M) 96MHz Fractional Digital Phased Locked Loop (FDPLL96M)	
Event System channels	12	12
SW Debug Interface	Yes	Yes
Watchdog Timer (WDT)	Yes	Yes

Note: 1. SERCOM4 is internally connected to the AT86RF233.

2. Ordering Information



2.1 SAM R21E

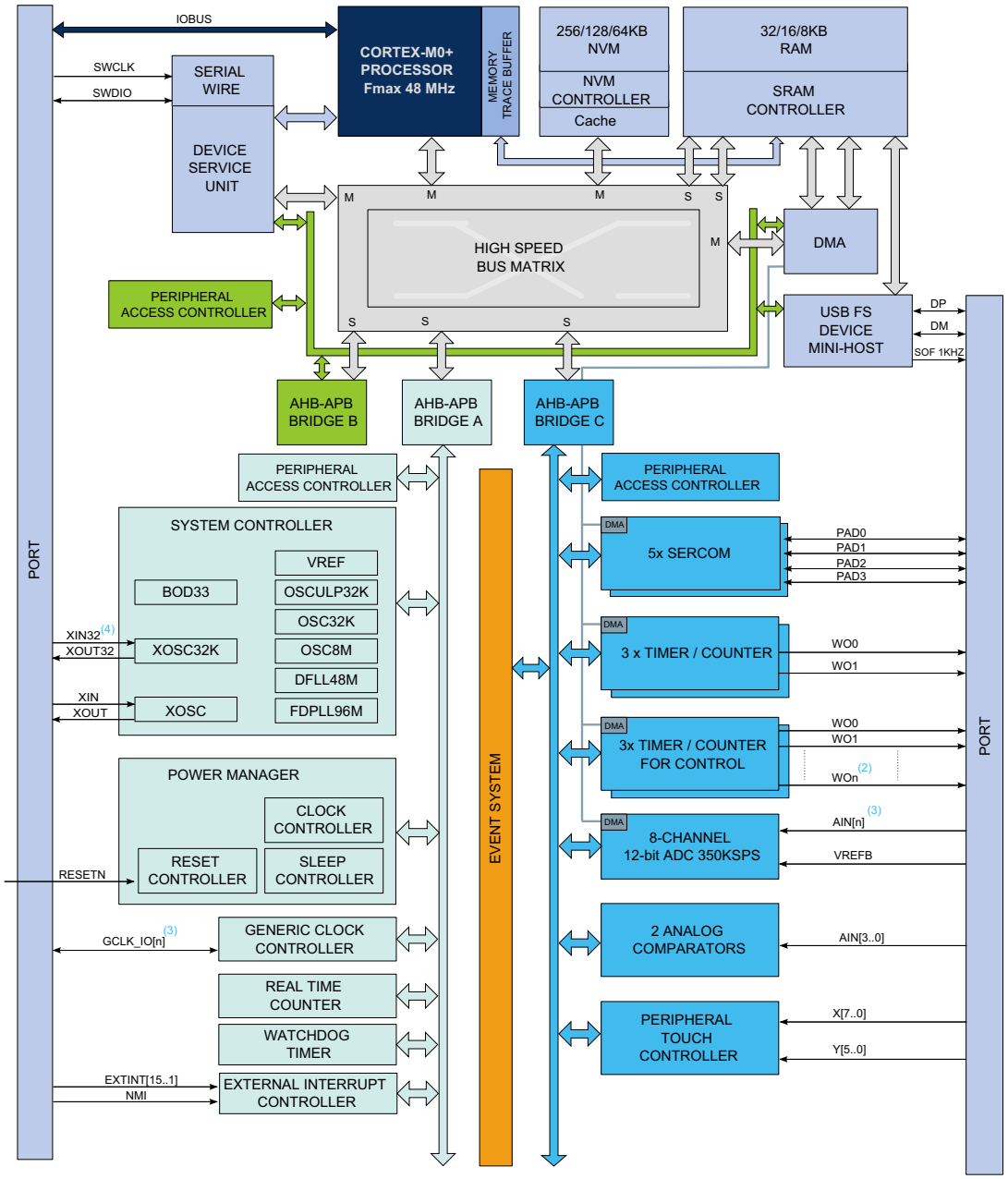
Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMR21E16A-MF	64K	8K	QFN32	Tray
ATSAMR21E16A-MFT				Tape & Reel
ATSAMR21E16A-MU				Tray
ATSAMR21E16A-MUT				Tape & Reel
ATSAMR21E17A-MF	128K	16K	QFN32	Tray
ATSAMR21E17A-MFT				Tape & Reel
ATSAMR21E17A-MU				Tray
ATSAMR21E17A-MUT				Tape & Reel
ATSAMR21E18A-MF	256K	32K	QFN32	Tray
ATSAMR21E18A-MFT				Tape & Reel
ATSAMR21E18A-MU				Tray
ATSAMR21E18A-MUT				Tape & Reel

2.2 SAM R21G

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMR21G16A-MF	64K	8K	QFN48	Tray
ATSAMR21G16A-MFT				Tape & Reel
ATSAMR21G16A-MU				Tray
ATSAMR21G16A-MUT				Tape & Reel
ATSAMR21G17A-MF	128K	16K	QFN48	Tray
ATSAMR21G17A-MFT				Tape & Reel
ATSAMR21G17A-MU				Tray
ATSAMR21G17A-MUT				Tape & Reel
ATSAMR21G18A-MF	256K	32K	QFN48	Tray
ATSAMR21G18A-MFT				Tape & Reel
ATSAMR21G18A-MU				Tray
ATSAMR21G18A-MUT				Tape & Reel

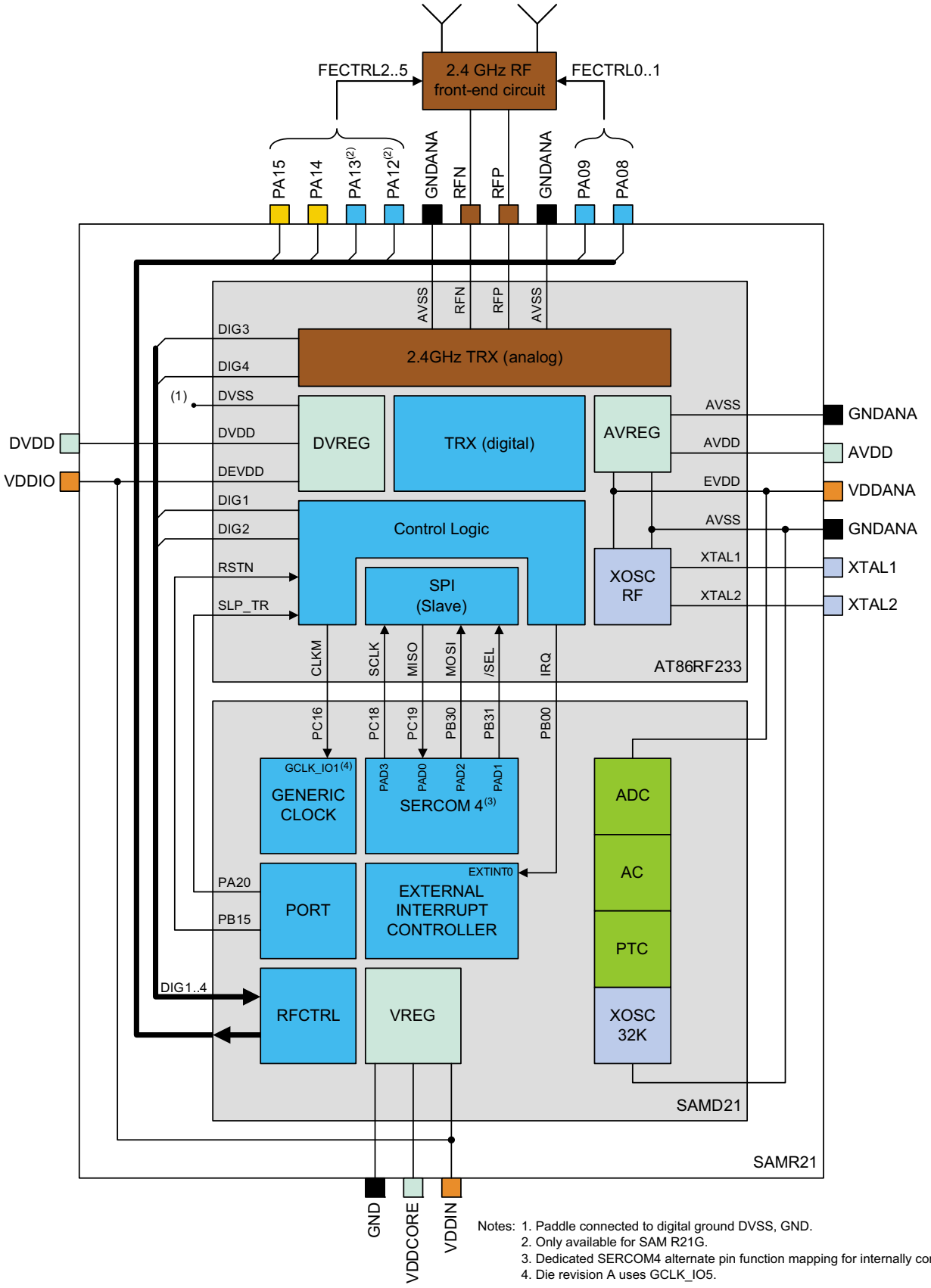
3. Block Diagrams

3.1 MCU Block Diagram



Notes:
1. Some products have different number of SERCOM instances, Timer/Counter instances, PTC signals and ADC signals. Refer to “Ordering Information” on page 6 for details.
2. The three TCC instances have different configurations, including the number of Waveform Output (WO) lines.
3. Refer to the PORT Function Multiplexing Table 5-1 for details about the available GCLK_IO and ADC signals.
4. Only available for SAM R21G.

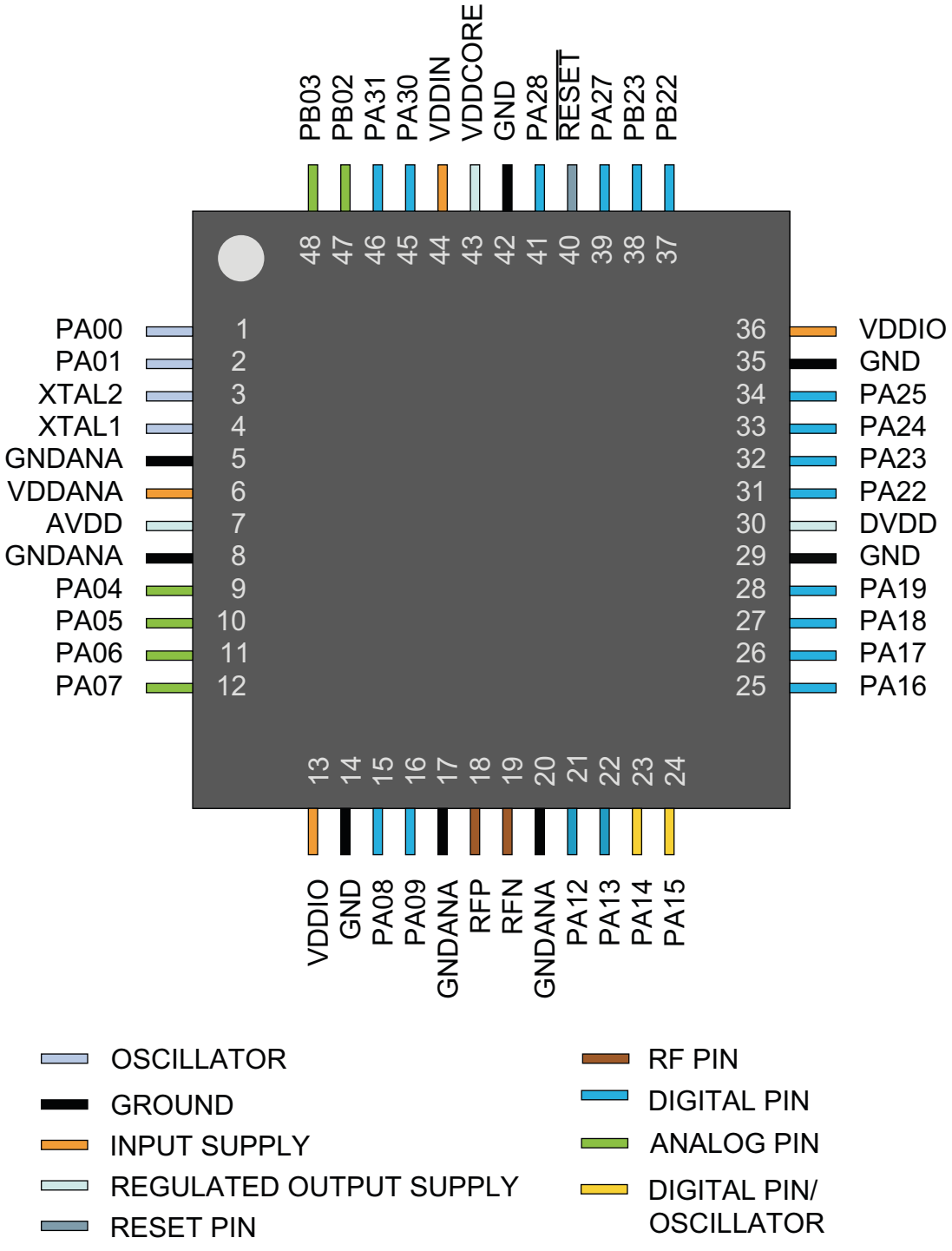
3.2 SAM R21 Interconnection



Notes: 1. Paddle connected to digital ground DVSS, GND.
2. Only available for SAM R21G.
3. Dedicated SERCOM4 alternate pin function mapping for internally connected AT86RF233.
4. Die revision A uses GCLK_IO5.

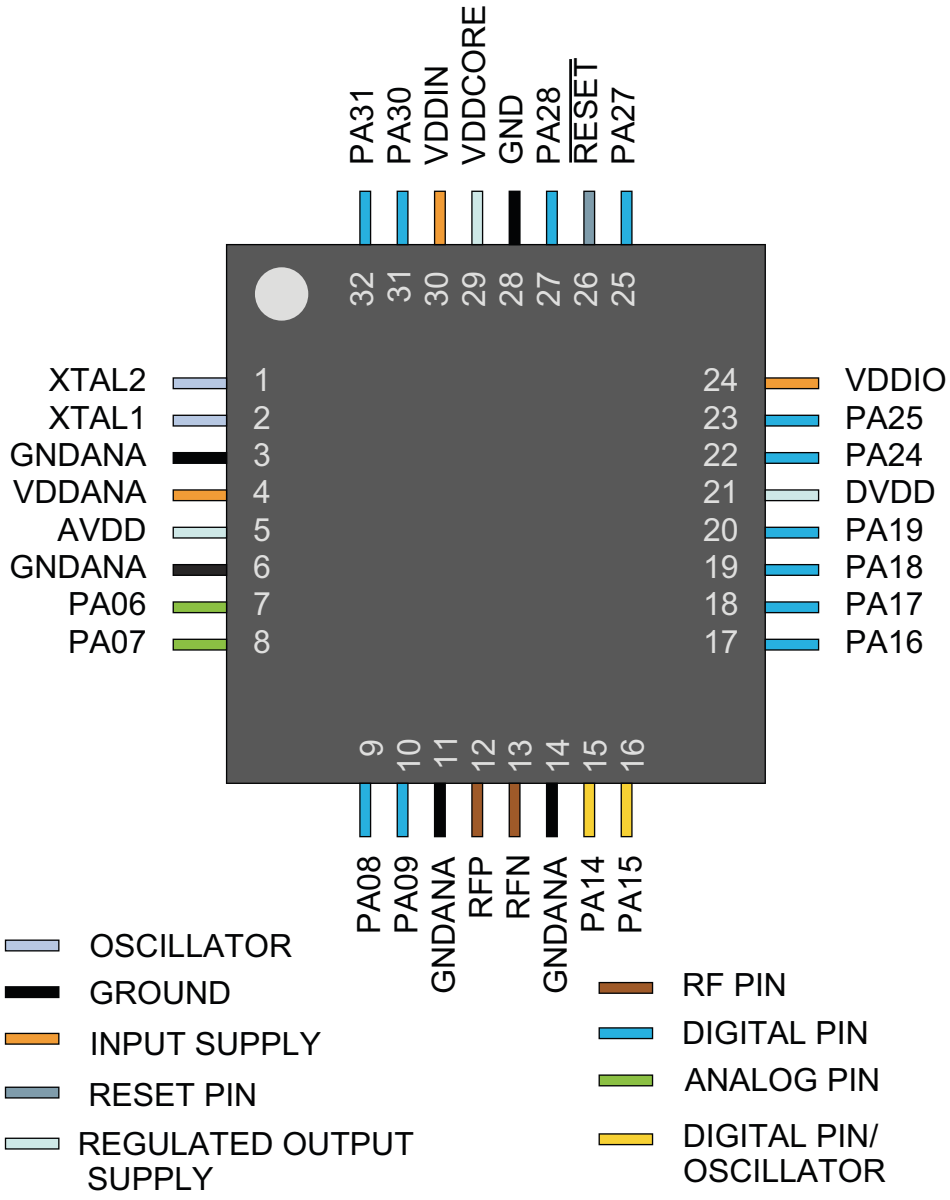
4. Pinout

4.1 SAM R21G - QFN48



Note: The large center pad underneath the QFN package is made of metal and internally connected to GND. It should be soldered and connected to the digital ground on the board to ensure good mechanical stability. It is not recommended to use the exposed paddle as a replacement of the regular GND pin.

4.2 SAM R21E - QFN32



Note: The large center pad underneath the QFN package is made of metal and internally connected to GND. It should be soldered and connected to the digital ground on the board to ensure good mechanical stability. It is not recommended to use the exposed paddle as a replacement of the regular GND pin.

5. I/O Multiplexing and Considerations

5.1 Multiplexed Signals

Each pin is by default controlled by the PORT as a general purpose I/O and alternatively it can be assigned to one of the peripheral functions A, B, C, D, E, F, G or H. To enable a peripheral function on a pin, the Peripheral Multiplexer Enable bit in the Pin Configuration register corresponding to that pin (PINCFGn.PMUXEN, n = 0..31) in the PORT must be written to one. The selection of peripheral function A to H is done by writing to the Peripheral Multiplexing Odd and Even bits in the Peripheral Multiplexing register (PMUXn.PMUXE/O) in the PORT.

Table 5-1 describes the peripheral signals multiplexed to the PORT I/O pins.

Table 5-1. PORT Function Multiplexing

Pin					A	B[1][2]				C	D	E	F	G	H
SAMR21E	SAMR21G	I/O Pin	Supply	Type	EIC	REF	ADC	AC	PTC	SERCOM[1][2]	SERCOM-ALT	TC TCC	FECTRL TCC SERCOM	COM	AC/ GCLK
	1	PA00	VDDANA								SERCOM1/ PAD[0]	TCC2/WO[0]			
	2	PA01	VDDANA		EXTINT[1]						SERCOM1/ PAD[1]	TCC2/WO[1]			
	9	PA04	VDDANA		EXTINT[4]	ADC/ VREFB	AIN[4]	AIN[0]	Y[2]		SERCOM0/ PAD[0]	TCC0/WO[0]			
	10	PA05	VDDANA		EXTINT[5]		AIN[5]	AIN[1]	Y[3]		SERCOM0/ PAD[1]	TCC0/WO[1]			
7	11	PA06	VDDANA		EXTINT[6]		AIN[6]	AIN[2]	Y[4]		SERCOM0/ PAD[2]	TCC1/WO[0]			
8	12	PA07	VDDANA		EXTINT[7]		AIN[7]	AIN[3]	Y[5]		SERCOM0/ PAD[3]	TCC1/WO[1]			
9	15	PA08	VDDIO	I^2C	NMI		AIN[16]		X[0]	SERCOM0/ PAD[0]	SERCOM2/ PAD[0]	TCC0/WO[0]	FECTRL[0]		
10	16	PA09	VDDIO	I^2C	EXTINT[9]		AIN[17]		X[1]	SERCOM0/ PAD[1]	SERCOM2/ PAD[1]	TCC0/WO[1]	FECTRL[1]		
	21	PA12	VDDIO	I^2C	EXTINT[12]					SERCOM2/ PAD[0]		TCC2/WO[0]	FECTRL[2]		AC/ CMP[0]
	22	PA13	VDDIO	I^2C	EXTINT[13]					SERCOM2/ PAD[1]		TCC2/WO[1]	FECTRL[3]		AC/ CMP[1]
15	23	PA14	VDDIO		EXTINT[14]					SERCOM2/ PAD[2]		TC3/WO[0]	FECTRL[4]		GCLK_IO[0]
16	24	PA15	VDDIO		EXTINT[15]					SERCOM2/ PAD[3]		TC3/WO[1]	FECTRL[5]		GCLK_IO[1]
17	25	PA16	VDDIO	I^2C					X[4]	SERCOM1/ PAD[0]	SERCOM3/ PAD[0]	TCC2/WO[0]	TCC0/ WO[0]		GCLK_IO[2]
18	26	PA17	VDDIO	I^2C	EXTINT[1]				X[5]	SERCOM1/ PAD[1]	SERCOM3/ PAD[1]	TCC2/WO[1]	TCC0/ WO[1]		GCLK_IO[3]
19	27	PA18	VDDIO		EXTINT[2]				X[6]	SERCOM1/ PAD[2]	SERCOM3/ PAD[2]	TC3/WO[0]	TCC0/ WO[2]		AC/ CMP[0]
20	28	PA19	VDDIO		EXTINT[3]				X[7]	SERCOM1/ PAD[3]	SERCOM3/ PAD[3]	TC3/WO[1]	TCC0/ WO[3]		AC/ CMP[1]
	31	PA22	VDDIO	I^2C	EXTINT[6]				X[10]	SERCOM3/ PAD[0]	SERCOM5/ PAD[0]	TC4/WO[0]	TCC0/ WO[4]		GCLK_IO[6]
	32	PA23	VDDIO	I^2C	EXTINT[7]				X[11]	SERCOM3/ PAD[1]	SERCOM5/ PAD[1]	TC4/WO[1]	TCC0/ WO[5]		GCLK_IO[7]
22	33	PA24	VDDIO		EXTINT[12]					SERCOM3/ PAD[2]	SERCOM5/ PAD[2]	TC5/WO[0]	TCC1/ WO[2]	USB_DM	
23	34	PA25	VDDIO		EXTINT[13]					SERCOM3/ PAD[3]	SERCOM5/ PAD[3]	TC5/WO[1]	TCC1/ WO[3]	USB_DP	

Table 5-1. PORT Function Multiplexing (Continued)

Pin		I/O Pin	Supply	Type	A	B[1][2]				C	D	E	F	G	H
SAMR21E	SAMR21G				EIC	REF	ADC	AC	PTC	SERCOM[1][2]	SERCOM-ALT	TC TCC	FECTRL TCC SERCOM	COM	AC/ GCLK
	37	PB22	VDDIO		EXTINT[6]						SERCOM5/ PAD[2]				GCLK_IO[0]
	38	PB23	VDDIO		EXTINT[7]						SERCOM5/ PAD[3]				GCLK_IO[1]
25	39	PA27	VDDIO		EXTINT[15]								SERCOM3/ PAD[0]		GCLK_IO[0]
27	41	PA28	VDDIO		EXTINT[8]								SERCOM3/ PAD[1]		GCLK_IO[0]
31	45	PA30	VDDIO		EXTINT[10]						SERCOM1/ PAD[2]	TCC1/WO[0]		SWCLK	GCLK_IO[0]
32	46	PA31	VDDIO		EXTINT[11]						SERCOM1/ PAD[3]	TCC1/WO[1]			
	47	PB02	VDDANA		EXTINT[2]		AIN[10]		Y[8]		SERCOM5/ PAD[0]				
	48	PB03	VDDANA		EXTINT[3]		AIN[11]		Y[9]		SERCOM5/ PAD[1]				

Notes:
1. All analog pin functions are on peripheral function B. Peripheral function B must be selected to disable the digital control of the pin.
2. Only some pins can be used in SERCOM I^2C mode. See the Type column for using a SERCOM pin in I^2C mode. Refer to !!!CRs_ElChar_Top!!! for details on the I^2C pin characteristics.

5.2 Internal Multiplexed Signals

PA20, PB00, PB15, PB30, PB31, PC16, PC18 and PC19 are by default controlled by the PORT as a general purpose I/O and alternatively it can be assigned to one of the peripheral functions A, B, C, D, E, F, G or H. To enable a peripheral function on a pin, the Peripheral Multiplexer Enable bit in the Pin Configuration register corresponding to that pin (PINCFGn.PMUXEN, n = 0-31) in the PORT must be written to one. The selection of peripheral function A to H is done by writing to the Peripheral Multiplexing Odd and Even bits in the Peripheral Multiplexing register (PMUXn.PMUXE/O) in the PORT.

PA10, PA11, PB16 and PB17 cannot be configured as output ports. These ports are always connected to the RFCTRL inputs.

Internal Signal	I/O Pin	Supply	Type	A	B				C	D	E	F	G	H
				EIC	REF	ADC	AC	PTC	SERCOM	SERCOM-ALT	TC	FECTRL TCC SERCOM	COM	AC/ GCLK
DIG3	PA10	VDDIO	Input	EXTINT[10]										
DIG4	PA11	VDDIO	Input	EXTINT[11]										
SLP_TR	PA20	VDDIO	I/O											
IRQ	PB00	VDDANA	I/O	EXTINT[0]										
RSTN	PB15	VDDIO	I/O											
DIG1	PB16	VDDIO	Input	EXTINT[0]										
DIG2	PB17	VDDIO	Input	EXTINT[1]										
MOSI	PB30	VDDIO	I/O									SERCOM4/ PAD[2]		
SEL	PB31	VDDIO	I/O									SERCOM4/ PAD[1]		

Internal Signal	I/O Pin	Supply	Type	A	B				C	D	E	F	G	H
				EIC	REF	ADC	AC	PTC	SERCOM	SERCOM-ALT	TC	FECTRL TCC SERCOM	COM	AC/ GCLK
CLKM	PC16	VDDIO	I/O									GCLK/ IO[1](1)		
SCLK	PC18	VDDIO	I/O									SERCOM4/ PAD[3]		
MISO	PC19	VDDIO	I/O									SERCOM4/ PAD[0]		

Note: 1. Die revision A uses GCLK/IO[5].

5.3 Other Functions

5.3.1 Oscillator Pinout

The oscillators are not mapped to the normal PORT functions and their multiplexing are controlled by registers in the System Controller (SYSCTRL).

Oscillator	Supply	Signal	I/O Pin
XOSC	VDDIO	XIN	PA14
		XOUT	PA15
XOSC32K	VDDANA	XIN32	PA00
		XOUT32	PA01

The integrated AT86RF233 16 MHz crystal oscillator is directly connected to pins and has no multiplexing functionality.

Oscillator	Supply	Signal	I/O Pin
XOSCRF	EVDD/VDDANA	XTAL1	XTAL1
		XTAL2	XTAL2

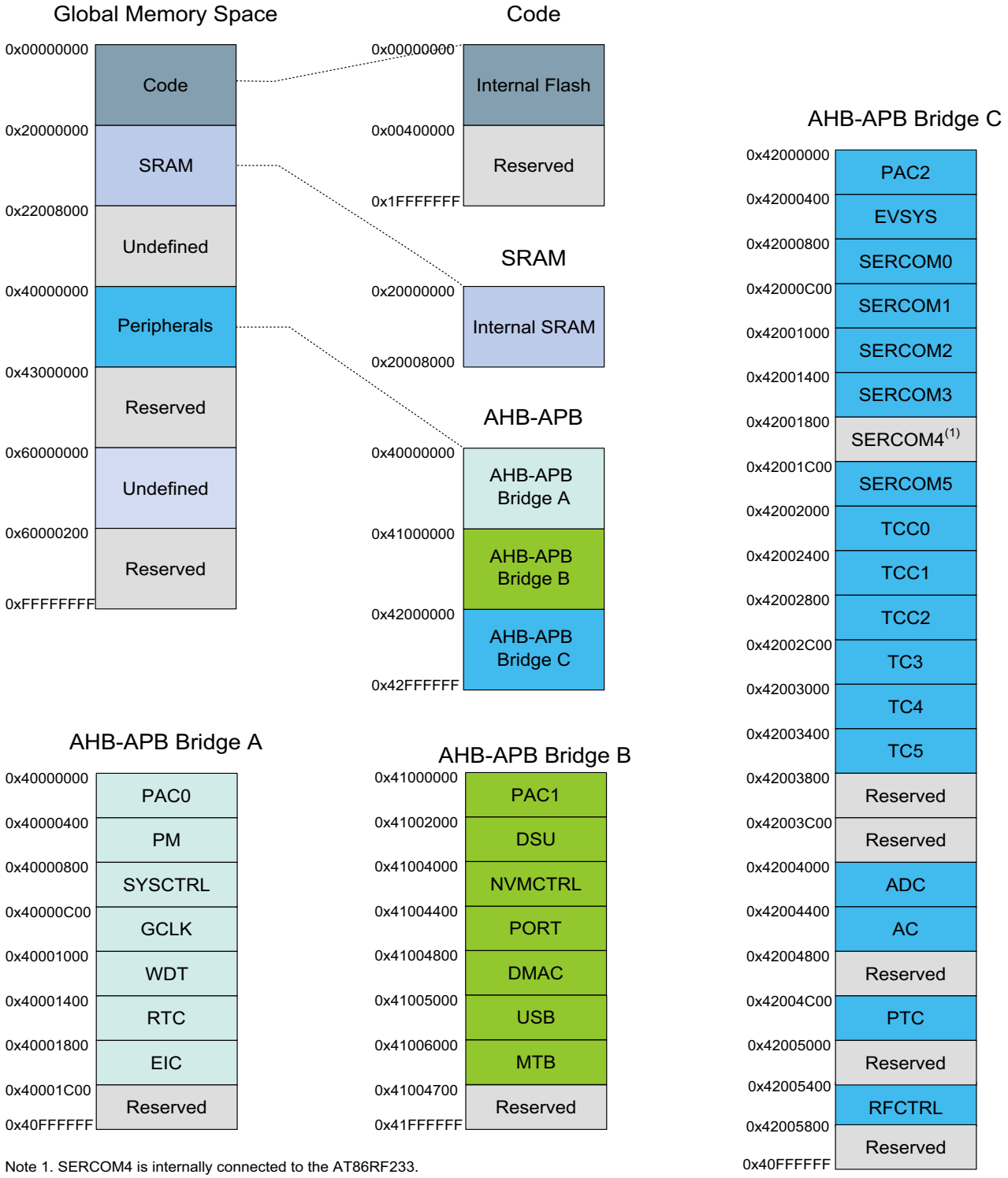
5.3.2 Serial Wire Debug Interface Pinout

Only the SWCLK pin is mapped to the normal PORT functions. A debugger cold-plugging or hot-plugging detection will automatically switch the SWDIO port to the SWDIO function.

Signal	Supply	I/O Pin
SWCLK	VDDIO	PA30
SWDIO	VDDIO	PA31

6. Product Mapping

Figure 6-1. Atmel | SMART SAM R21 Product Mapping



Note 1. SERCOM4 is internally connected to the AT86RF233.

This figure represents the full configuration of the Atmel | SMART SAM R21 with maximum Flash and SRAM capabilities and a full set of peripherals. Refer to the "Configuration Summary" on page 4 for details.

7. Processor And Architecture

7.1 Cortex M0+ Processor

The Atmel | SMART SAM R21 implements the ARM® Cortex™-M0+ processor, which is based on the ARMv6 Architecture and Thumb®-2 ISA. The Cortex M0+ is 100% instruction set compatible with its predecessor, the Cortex-M0 processor, and upward compatible to Cortex-M3 and M4 processors.

For more information refer to www.arm.com.

7.1.1 Cortex M0+ Configuration

Features	Configuration option	Atmel | SMART SAM R21 configuration
Interrupts	External interrupts 0-32	32
Data endianness	Little-endian or big-endian	Little-endian
SysTick timer	Present or absent	Present
Number of watchpoint comparators	0, 1, 2	2
Number of breakpoint comparators	0, 1, 2, 3, 4	4
Halting debug support	Present or absent	Present
Multiplier	Fast or small	Fast (single cycle)
Single-cycle I/O port	Present or absent	Present
Wake-up interrupt controller	Supported or not supported	Not supported
Vector Table Offset Register	Present or absent	Present
Unprivileged/Privileged support	Present or absent	Absent(1)
Memory Protection Unit	Not present or 8-region	Not present
Reset all registers	Present or absent	Absent
Instruction fetch width	16-bit only or mostly 32-bit	32-bit

Note: 1. All software run in privileged mode only

The ARM Cortex-M0+ core has two bus interfaces:

- Single 32-bit AMBA®-3 AHB-Lite™ system interface that provides connections to peripherals and all system memory, including flash and RAM
- Single 32-bit I/O port bus interfacing to the PORT with one-cycle loads and stores

8. Packaging Information

8.1 Thermal Considerations

8.1.1 Thermal Resistance Data

Table 8-1 summarizes the thermal resistance data depending on the package.

Table 8-1. Thermal Resistance Data

Package Type	θ_{JA}	θ_{JC}
32-pin QFN	37.2 °C/W	3.1 °C/W
48-pin QFN	33 °C/W	11.4 °C/W

8.1.2 Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

1. $T_D = T_A + (P_D \times \theta_{JA})$
2. $T_D = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

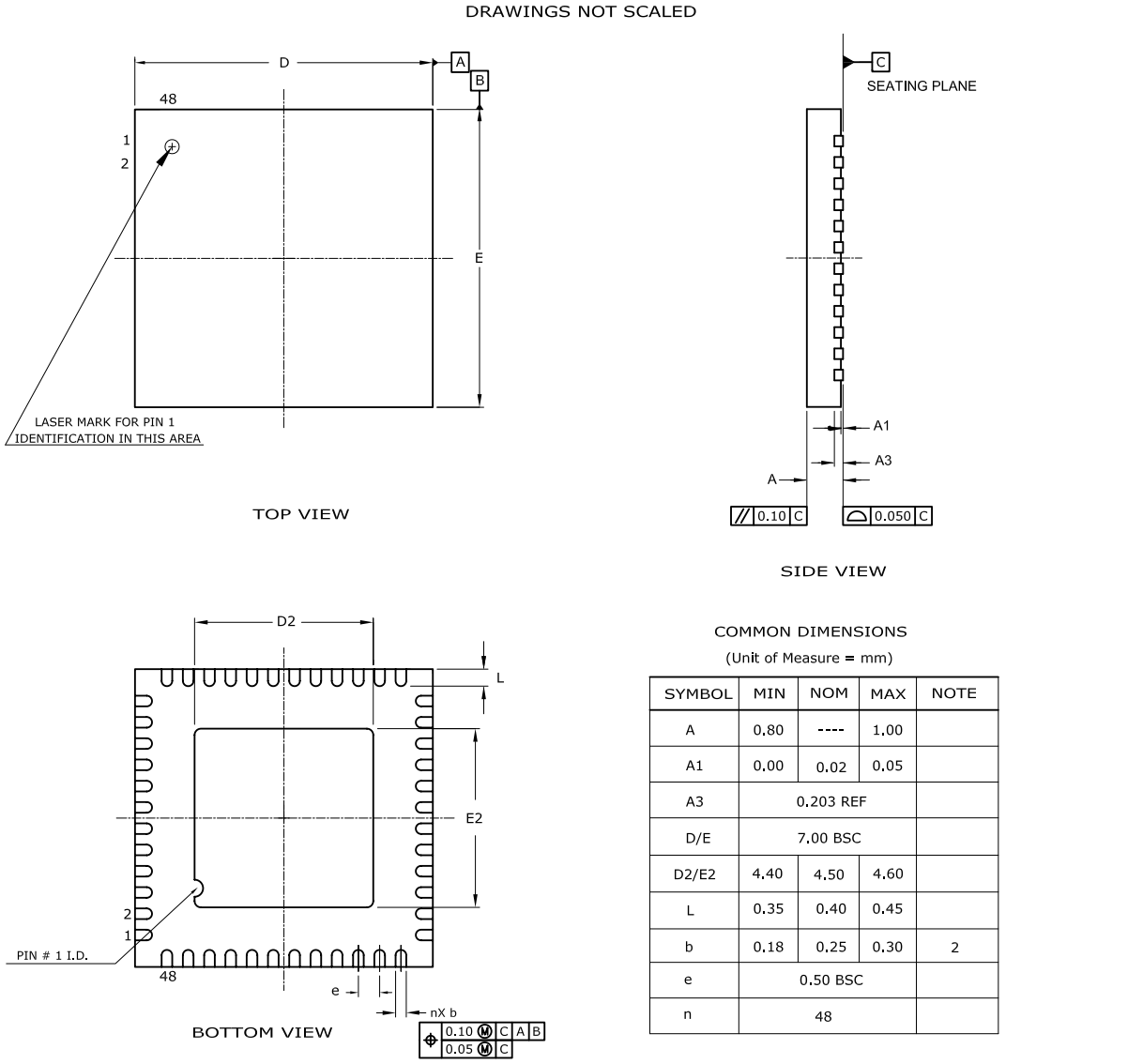
where:

- θ_{JA} = package thermal resistance, Junction-to-ambient (°C/W), provided in Table 8-1.
- θ_{JC} = package thermal resistance, Junction-to-case thermal resistance (°C/W), provided in Table 8-1.
- $\theta_{HEATSINK}$ = cooling device thermal resistance (°C/W), provided in the device datasheet.
- P_D = device power consumption (W).
- T_A = ambient temperature (°C).

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

8.2 Package Drawings

8.2.1 48-pin QFN



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	----	1.00	
A1	0.00	0.02	0.05	
A3		0.203 REF		
D/E		7.00 BSC		
D2/E2	4.40	4.50	4.60	
L	0.35	0.40	0.45	
b	0.18	0.25	0.30	2
e		0.50 BSC		
n		48		

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VKKD-4, for proper dimensions, tolerances, datums, etc. (Excepted D2/E2).
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

Table 8-2. Device and Package Maximum Weight

100	mg

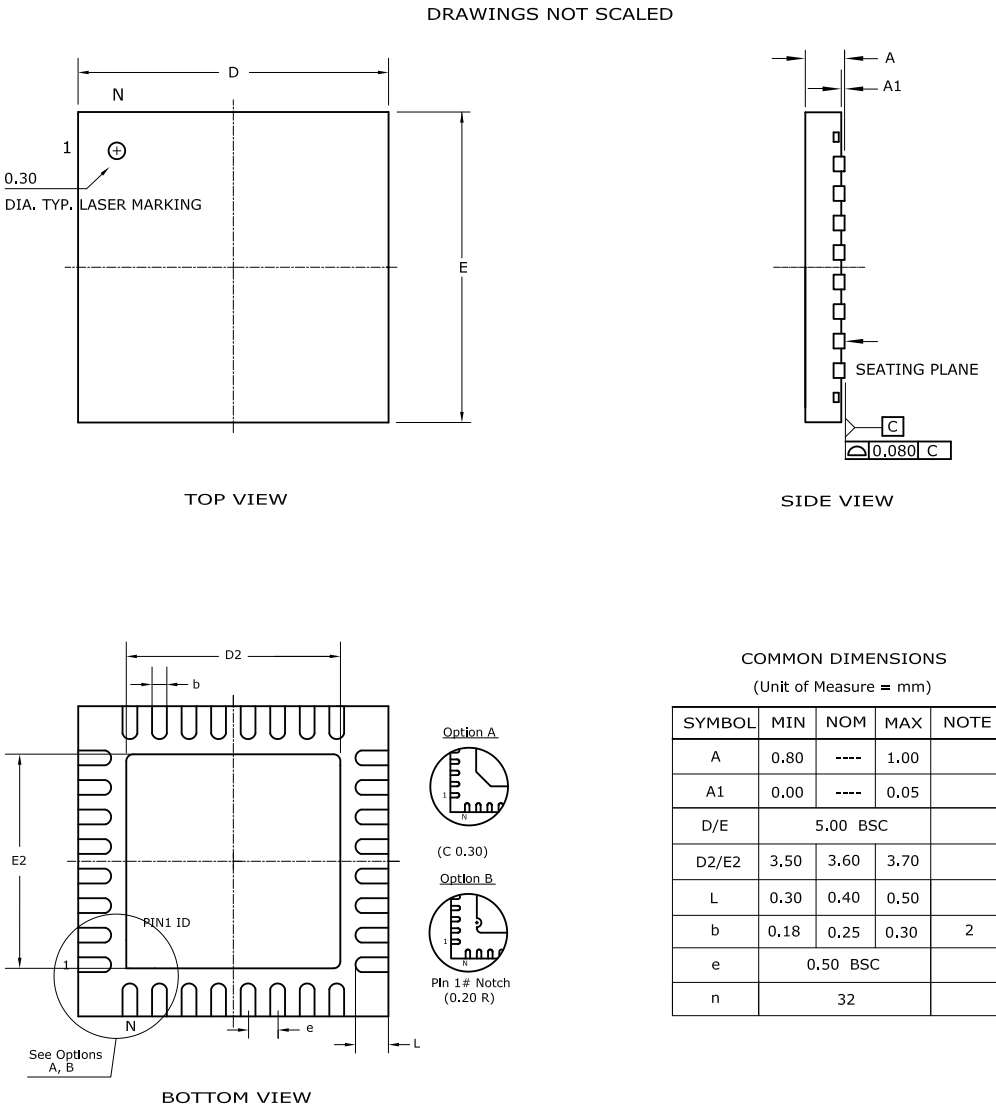
Table 8-3. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 8-4. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

8.2.2 32-pin QFN



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	----	1.00	
A1	0.00	----	0.05	
D/E		5.00 BSC		
D2/E2	3.50	3.60	3.70	
L	0.30	0.40	0.50	
b	0.18	0.25	0.30	2
e		0.50 BSC		
n		32		

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VHHD-2, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

Table 8-5. Device and Package Maximum Weight

90	mg

Table 8-6. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 8-7. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

8.3 Soldering Profile

The following table gives the recommended soldering profile from J-STD-20.

Profile Feature	Green Package
Average Ramp-up Rate (217°C to peak)	3°C/s max
Preheat Temperature 175°C +/-25°C	150-200°C
Time Maintained Above 217°C	60-150s
Time within 5°C of Actual Peak Temperature	30s
Peak Temperature Range	260°C
Ramp-down Rate	6°C/s max
Time 25°C to Peak Temperature	8 minutes max

A maximum of three reflow passes is allowed per component.

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