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ADVANCE

CYW43570

Single-Chip 5G WiFi IEEE 802.11ac 2×2 MAC/Baseband/Radio with Integrated Bluetooth 4.1 and EDR

The Cypress CYW4343W1 is a complete dual-band (2.4 GHz and 5 GHz) 5G WiFi 2 × 2 MIMO MAC/PHY/Radio System-on-a-Chip. This WiFi single-chip device provides a high level of integration with a dual-stream IEEE 802.11ac MAC/baseband/radio and Bluetooth 4.1 + enhanced data rate (EDR). In IEEE 802.11ac mode, the WLAN operation supports rates of MCS0–MCS9 (up to 256 QAM) in 20 MHz, 40 MHz, and 80 MHz channels for data rates up to 867 Mbps. In addition, all the IEEE 802.11a/b/g/n rates are supported. Included on-chip are 2.4 GHz and 5 GHz transmitter power amplifiers and receiver low noise amplifiers.

The CYW4343W1 integrates several peripheral interfaces including USB 2.0 (Bluetooth), PCIe (Wi-Fi), and serial flash. For the Bluetooth section, the host interface options are a high-speed 4-wire UART and USB 2.0 full-speed (12 Mbps).

The CYW4343W1 uses advanced design techniques and process technology to reduce active and idle power, and includes an embedded power management unit that simplifies the system power topology.

The CYW4343W1 implements highly sophisticated enhanced collaborative coexistence hardware mechanisms and algorithms that ensure that WLAN and Bluetooth collaboration is optimized for maximum performance.

This datasheet provides details on the functional, operational, and electrical characteristics for the Cypress CYW4343W1. It is intended for hardware design, application, and OEM engineers.

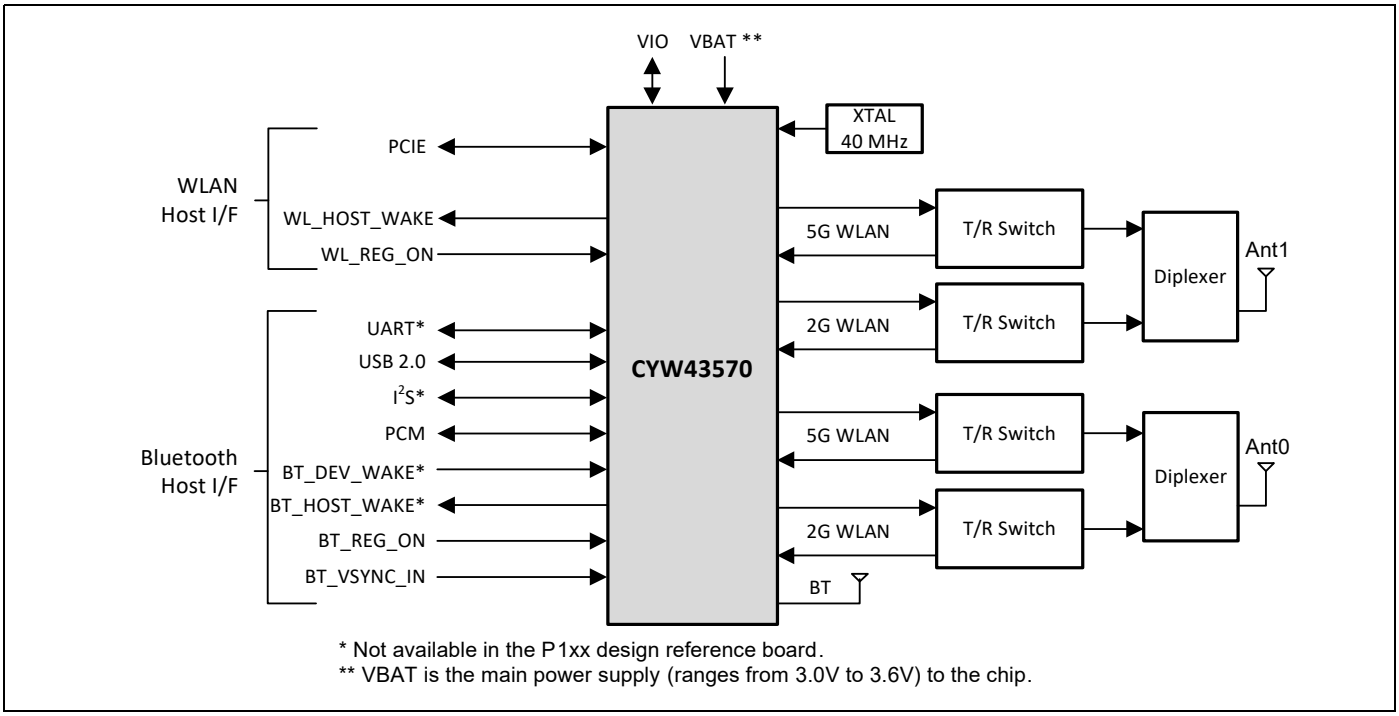
Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM43570	CYW43570
BCM43570KFFBG	CYW43570KFFBG

Figure 1. Functional Block Diagram for PCIe (WLAN) and BT (USB 2.0) Interfaces



* Not available in the P1xx design reference board.
** VBAT is the main power supply (ranges from 3.0V to 3.6V) to the chip.

Features

IEEE 802.11X Key Features

- IEEE 802.11ac Draft compliant.
- Dual-stream spatial multiplexing up to 867 Mbps data rate.
- Supports 20, 40, and 80 MHz channels with optional SGI (256 QAM modulation).
- Full IEEE 802.11a/b/g/n legacy compatibility with enhanced performance.
- Tx and Rx low-density parity check (LDPC) support for improved range and power efficiency.
- Supports IEEE 802.11ac/n beamforming.
- On-chip power amplifiers and low-noise amplifiers for both bands.
- Supports various RF front-end architectures including:
  - Three antennas design: two separate antennas (Core0 and Core1 to WLAN) and a separate antenna to Bluetooth.
  - Optional support: two antennas with WLAN diversity and a shared Bluetooth antenna.
- Internal fractional nPLL allows support for a wide range of reference clock frequencies.
- Supports PCIe Gen2 interface but up to Gen1 transfer speed.
- OneDriver™ software architecture for easy migration from existing embedded WLAN and Bluetooth devices as well as future devices.

Bluetooth Key Features

- Complies with Bluetooth Core Specification Version 4.1 + EDR with provisions for supporting future specifications.
- Bluetooth Class 1 or Class 2 transmitter operation.
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.
- Host controller interface (HCI) using a USB or high-speed UART interface and PCM for audio data. HCI/UART interface capable but not currently supported.
- USB 2.0 full-speed (12 Mbps) supported for Bluetooth.
- Low-power mode helps power consumption of the media devices.
- Supports multiple simultaneous advanced audio distribution profiles (A2DP) for stereo sound.
- Automatic frequency detection for standard crystal and TCXO values.
- Supports serial flash interfaces.

General Features

- Supports 3.3V power supplies with internal switching regulator.
- Programmable dynamic power management
- 484 bytes of user-accessible OTP for storing board parameters
- GPIOs supported: 16
- Package: 254-ball FCBGA (10 mm × 10 mm, 0.4 mm pitch)
- Security:
  - WPA and WPA2 (personal) support for powerful encryption and authentication
  - AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility
  - Reference WLAN subsystem provides Cisco Compatible Extensions (CCX, CCX 2.0, CCX 3.0, CCX 4.0, CCX 5.0)
  - Reference WLAN subsystem provides Wi-Fi protected setup (WPS)
- Worldwide regulatory support: Global products supported with worldwide homologated design.

Contents

1. Overview 5
1.1 Overview 5
1.3 Standards Compliance 7
2. Power Supplies and Power Management 9
2.1 Power Supply Topology 9
2.2 CYW43570 PMU Features 9
2.3 WLAN Power Management 11
2.4 PMU Sequencing 11
2.5 Power-Off Shutdown 12
2.6 Power-Up/Power-Down/Reset Circuits 12
3. Frequency References 13
3.1 Crystal Interface and Clock Generation 13
3.2 External Frequency Reference 14
4. Bluetooth Overview 15
4.1 Features 15
4.2 Bluetooth Radio 16
5. Bluetooth Baseband Core 18
5.1 Bluetooth 4.1 Features 18
5.2 Bluetooth Low Energy 18
5.3 Link Control Layer 18
5.4 Test Mode Support 19
5.5 Bluetooth Power Management Unit 19
5.6 Adaptive Frequency Hopping 22
5.7 Advanced Bluetooth/WLAN Coexistence 22
5.8 Fast Connection (Interlaced Page and Inquiry Scans) 22
6. Microprocessor and Memory Unit for Bluetooth 23
6.1 RAM, ROM, and Patch Memory 23
6.2 Reset 23
7. Bluetooth Peripheral Transport Unit 24
7.1 SPI/UART Transport Detection 24
7.2 PCM Interface 24
7.3 USB Interface 31
7.4 UART Interface 32
7.5 I^2S Interface 34
8. WLAN Global Functions 37
8.1 WLAN CPU and Memory Subsystem 37
8.2 One-Time Programmable Memory 37
9. PCI Express Interface 39
9.1 Transaction Layer Interface 39
9.2 Data Link Layer 39
9.3 Physical Layer 40
9.4 Logical Subblock 40
9.5 Scrambler/Descrambler 40
9.6 8B/10B Encoder/Decoder 40
9.7 Elastic FIFO 40
9.8 Electrical Subblock 40
9.9 Configuration Space 40
10. WLAN MAC and PHY 41
10.1 IEEE 802.11ac Draft MAC 41
10.2 IEEE 802.11ac Draft PHY 44
11. WLAN Radio Subsystem 45
11.1 Receiver Path 45
11.2 Transmitter Path 45
11.3 Calibration 45
12. Pin Diagram and Signal Descriptions 46
12.1 Ball Maps 46
12.2 Pin List 48
12.3 Signal Descriptions 51
12.4 WLAN/BT GPIO Signals and Strapping Options 56
13. DC Characteristics 57
13.1 Absolute Maximum Ratings 57
13.3 Recommended Operating Conditions and DC Characteristics 58
14. Bluetooth RF Specifications 59
15. WLAN RF Specifications 62
15.1 Introduction 62
15.2 2.4 GHz Band General RF Specifications 62
15.3 WLAN 2.4 GHz Receiver Performance Specifications 63
15.4 WLAN 2.4 GHz Transmitter Performance Specifications 67
15.5 WLAN 5 GHz Receiver Performance Specifications 68
15.6 WLAN 5 GHz Transmitter Performance Specifications 73
16. Internal Regulator Electrical Specifications. 74
16.1 Core Buck Switching Regulator 74
16.2 2.5V LDO (BTLDO2P5) 75
16.3 CLDO 76
16.4 LNLDO 77

17. System Power Consumption 78
17.1 WLAN Current Consumption 78
17.2 Bluetooth Current Consumption 80
18. Interface Timing and AC Characteristics..... 81
18.1 PCI Express Interface Parameters 81
19. Power-Up Sequence and Timing 83
19.1 Sequencing of Reset and Regulator Control Signals 83
20. Package Information..... 88
20.1 Package Thermal Characteristics 88
20.2 Junction Temperature Estimation and PSI_{JT} Versus $Theta_{JC}$ 88
20.3 Environmental Characteristics 88
21. Mechanical Information..... 89
22. Ordering Information..... 90
23. Additional Information 90
23.1 Acronyms and Abbreviations 90
23.2 References 90
24. IoT Resources 90
Document History..... 91
Sales, Solutions, and Legal Information 93

1. Overview

1.1 Overview

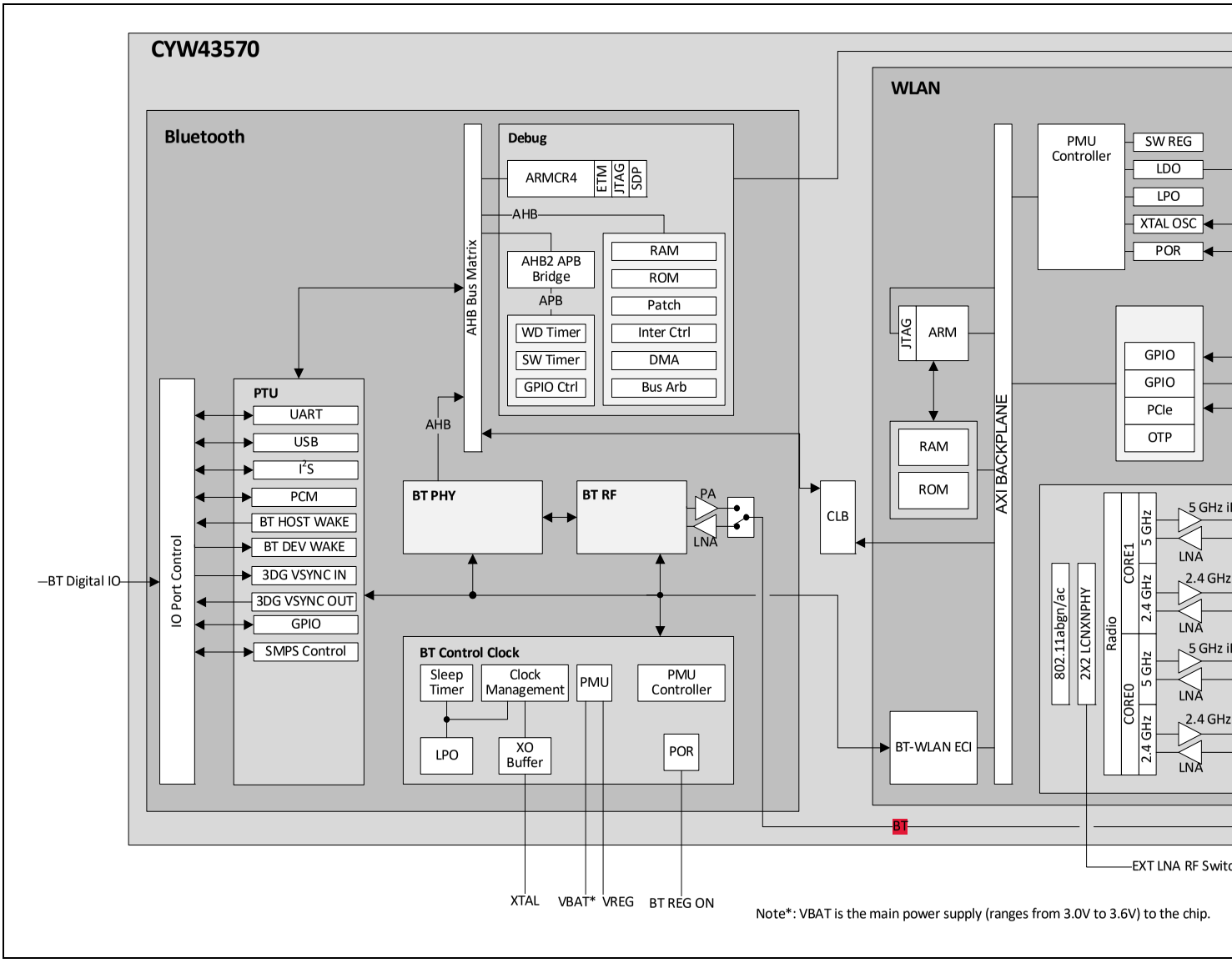
The Cypress CYW43570 single-chip device provides the highest level of integration for a mobile or handheld wireless system, with integrated IEEE 802.11 a/b/g/n/ac MAC/baseband/radio and Bluetooth 4.1 + EDR. It provides a small form-factor solution with minimal external components to drive down cost for mass volumes and allows for handheld device flexibility in size, form, and function. Comprehensive power management circuitry and software ensure the system can meet the needs of highly mobile devices that require minimal power consumption and reliable operation.

Figure 2 shows the interconnect of all the major physical blocks in the CYW43570 and their associated external interfaces, which are described in greater detail in the following sections.

Table 2. Device Interface Support

Feature	Interface Capability	Currently Supported Interfaces
BT GPIO (Bluetooth)	Yes	Yes
GPIO	16	No
GPIO (Wi-Fi)	Yes	Yes
I^2S	Yes	No
I^2S (Bluetooth)	Yes	No
JTAG (Wi-Fi)	Yes	No
PCIe (Wi-Fi)	Yes	Yes
PCM	Yes	No
PCM (Bluetooth)	Yes	No
SPI	Yes	No
UART (Bluetooth)	Yes	No
UART (Wi-Fi)	Yes	No
USB 2.0 (Bluetooth)	Yes	Yes

Figure 2. CYW43570 Block Diagram



1.2 Features

The CYW43570 supports the following features:

- IEEE 802.11a/b/g/n/ac dual-band 2x2 MIMO radio with virtual-simultaneous dual-band operation
- Bluetooth v4.1 + EDR with integrated Class 1 PA
- Concurrent Bluetooth and WLAN operation
- On-chip WLAN driver execution capable of supporting IEEE 802.11 functionality
- WLAN host interface, PCIe 2.0 (Wi-Fi), is compatible with Gen2 but the interface speed is up to Gen1 only.
- BT host digital interface (can be used concurrently with above interfaces):
  - UART (up to 4 Mbps)
- BT supports full-speed USB 2.0-compliant interface
- Enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives
- HCI high-speed UART (H4, H4+, and H5) transport (interface capable, but not currently supported)
- Wideband speech support (16 bit linear data, MSB first, left justified at 4K samples/s for transparent air coding, both through I^2S and PCM interface). (Interface capable, but not currently supported)
- Bluetooth SmartAudio technology improves voice and music quality to headsets
- Bluetooth low power inquiry and page scan
- Bluetooth low energy (BLE) support
- Bluetooth packet loss concealment (PLC)
- Bluetooth wideband speech (WBS)

1.3 Standards Compliance

The CYW43570 supports the following standards:

- Bluetooth 2.1 + EDR
- Bluetooth 3.0 + HS
- Bluetooth 4.1 + EDR
- IEEE802.11ac mandatory and optional requirements for 20 MHz, 40 MHz, and 80 MHz channels
- IEEE 802.11n (Handheld Device Class, Section 11)
- IEEE 802.11a
- IEEE 802.11b
- IEEE 802.11g
- IEEE 802.11d
- IEEE 802.11h
- IEEE 802.11i

- Security:
  - WEP
  - WPA Personal
  - WPA2 Personal
  - WMM
  - WMM-PS (U-APSD)
  - WMM-SA
  - AES (hardware accelerator)
  - TKIP (hardware accelerator)
  - CKIP (software support)
- Proprietary protocols:
  - CCXv2
  - CCXv3
  - CCXv4
  - CCXv5

The CYW43570 will support the following future drafts/standards:

- IEEE 802.11r (fast roaming between APs)
- IEEE 802.11w (secure management frames)
- IEEE 802.11 extensions:
  - IEEE 802.11e QoS enhancements (In accordance with the WMM specification, QoS is already supported.)
  - IEEE 802.11h 5 GHz extensions
  - IEEE 802.11i MAC enhancements
  - IEEE 802.11k radio resource measurement

2. Power Supplies and Power Management

2.1 Power Supply Topology

One Buck regulator, multiple LDO regulators, and a power management unit (PMU) are integrated into the CYW43570. All regulators are programmable via the PMU. These blocks simplify power supply design for Bluetooth and WLAN functions in embedded designs.

A single VBAT[1] (3.0V to 3.6V maximum) and VIO supply (1.8V to 3.3V) can be used, with all additional voltages being provided by the regulators in the CYW43570.

Two control signals, BT_REG_ON and WL_REG_ON, are used to power-up the regulators and take the respective section out of reset. The CBUCK CLDO and LNLDO power up when any of the reset signals are deasserted. All regulators are powered down only when both BT_REG_ON and WL_REG_ON are deasserted. The CLDO and LNLDO may be turned off/on based on the dynamic demands of the digital baseband.

The CYW43570 allows for an extremely low power-consumption mode by completely shutting down the CBUCK, CLDO, and LNLDO regulators. When in this state, LPLDO1 and LPLDO2 (which are low-power linear regulators that are supplied by the system VIO supply) provide the CYW43570 with all the voltages it requires, further reducing leakage currents.

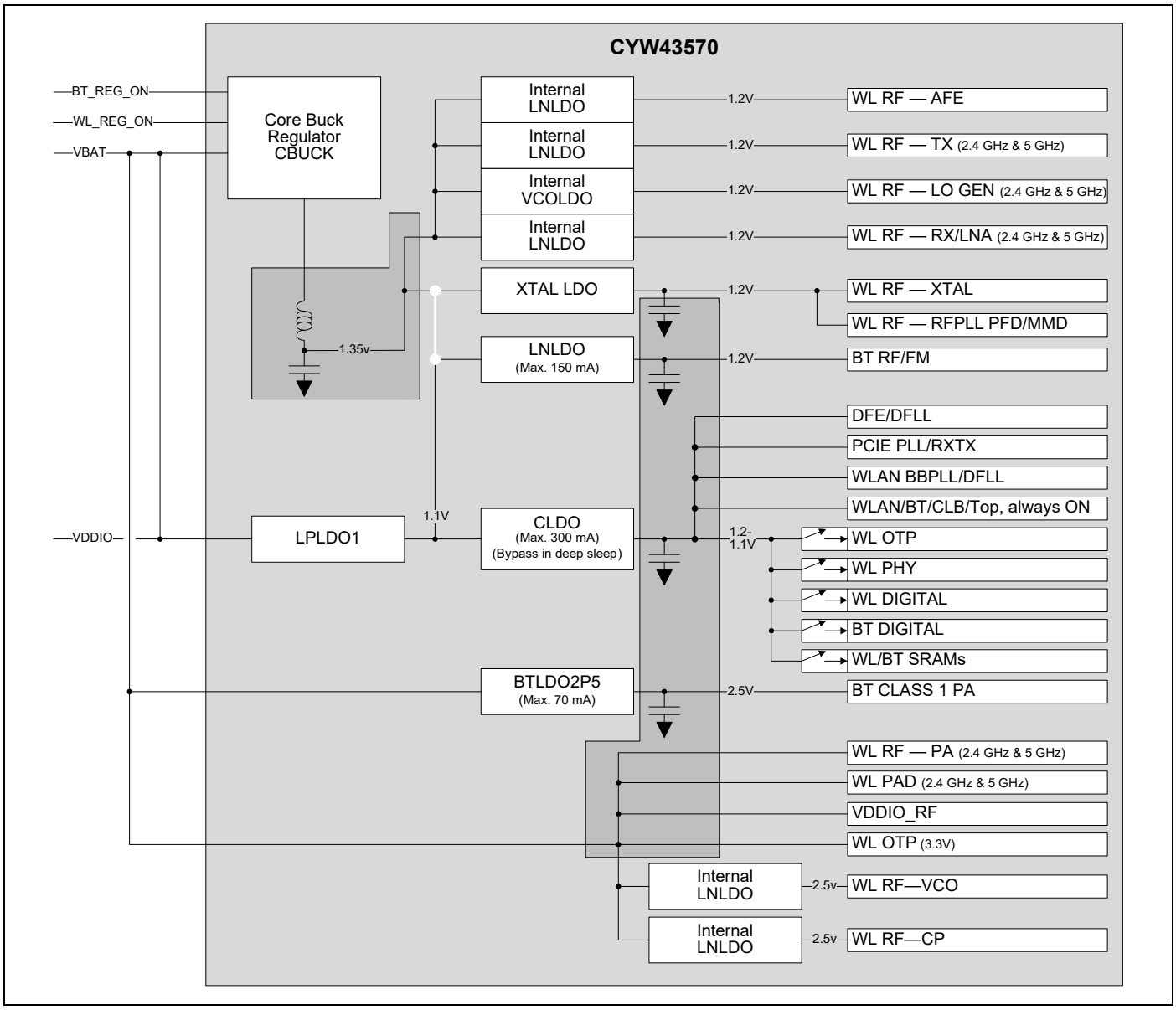
Figure 3 shows a typical power topology.

2.2 CYW43570 PMU Features

- VBAT to 1.35Vout (550 mA nominal, 870 mA maximum) Core-Buck (CBUCK) switching regulator
- VBAT to 2.5V out (15 mA nominal, 70 mA maximum) BTLDO2P5
- 1.35V to 1.2Vout (100 mA nominal, 150 mA maximum) LNLDO
- 1.35V to 1.2Vout (350 mA nominal, 500 mA maximum) CLDO with bypass mode for deep-sleep
- Additional internal LDOs (not externally accessible)

1. VBAT is the main power supply (ranges from 3.0V to 3.6V) to the chip.

Figure 3. Power Topology (Typical)



2.3 WLAN Power Management

The CYW43570 has been designed with the stringent power consumption requirements of mobile devices in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the CYW43570 integrated RAM is a high Vt memory with dynamic clock control. The dominant supply current consumed by the RAM is leakage current only. Additionally, the CYW43570 includes an advanced WLAN power management unit (PMU) sequencer. The PMU sequencer provides significant power savings by putting the CYW43570 into various power management states appropriate to the current environment and activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power up sequences are fully programmable. Configurable, free-running counters (running at 32.768 kHz LPO clock) in the PMU sequencer are used to turn on/turn off individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible.

The CYW43570 WLAN power states are described as follows:

- Active mode—All WLAN blocks in the CYW43570 are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- Doze mode—The radio, analog domains, and most of the linear regulators are powered down. The rest of the CYW43570 remains powered up in an IDLE state. All main clocks (PLL, crystal oscillator, or TCXO) are shut down to reduce active power to the minimum. The 32.768 kHz LPO clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake up the chip and transition to Active mode. In Doze mode, the primary power consumed is due to leakage current.
- Deep-sleep mode—Most of the chip including both analog and digital domains and most of the regulators are powered off. Logic states in the digital core are saved and preserved into a retention memory in the always-ON domain before the digital core is powered off. Upon a wake-up event triggered by the PMU timers, an external interrupt or a host resume through logic states in the digital core are restored to their pre-deep-sleep settings to avoid lengthy HW reinitialization.
- Power-down mode—The CYW43570 is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic re-enabling the internal regulators.

2.4 PMU Sequencing

The PMU sequencer is responsible for minimizing system power consumption. It enables and disables various system resources based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them.

Resource requests may come from several sources: clock requests from cores, the minimum resources defined in the ResourceMin register, and the resources requested by any active resource request timers. The PMU sequencer maps clock requests into a set of resources required to produce the requested clocks.

Each resource is in one of four states: enabled, disabled, transition_on, and transition_off and has a timer that contains 0 when the resource is enabled or disabled and a non-zero value in the transition states. The timer is loaded with the time_on or time_off value of the resource when the PMU determines that the resource must be enabled or disabled. That timer decrements on each 32.768 kHz PMU clock. When it reaches 0, the state changes from transition_off to disabled or transition_on to enabled. If the time_on value is 0, the resource can go immediately from disabled to enabled. Similarly, a time_off value of 0 indicates that the resource can go immediately from enabled to disabled. The terms enable sequence and disable sequence refer to either the immediate transition or the timer load-decrement sequence.

During each clock cycle, the PMU sequencer performs the following actions:

- Computes the required resource set based on requests and the resource dependency table.
- Decrements all timers whose values are non zero. If a timer reaches 0, the PMU clears the ResourcePending bit for the resource and inverts the ResourceState bit.
- Compares the request with the current resource status and determines which resources must be enabled or disabled.
- Initiates a disable sequence for each resource that is enabled, no longer being requested, and has no powered up dependents.
- Initiates an enable sequence for each resource that is disabled, is being requested, and has all of its dependencies enabled.

2.5 Power-Off Shutdown

The CYW43570 provides a low-power shutdown feature that allows the device to be turned off while the host, and any other devices in the system, remain operational. When the CYW43570 is not needed in the system, VDDIO_RF and VDDC are shut down while VDDIO remains powered. This allows the CYW43570 to be effectively off while keeping the I/O pins powered so that they do not draw extra current from any other devices connected to the I/O.

During a low-power shut-down state, provided VDDIO remains applied to the CYW43570, all outputs are tristated, and most inputs signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system, and enables the CYW43570 to be fully integrated in an embedded device and take full advantage of the lowest power-savings modes.

When the CYW43570 is powered on from this state, it is the same as a normal power-up and the device does not retain any information about its state from before it was powered down.

2.6 Power-Up/Power-Down/Reset Circuits

The CYW43570 has two signals (see Table 3) that enable or disable the Bluetooth and WLAN circuits and the internal regulator blocks, allowing the host to control power consumption. For timing diagrams of these signals and the required power-up sequences, see Section 19. Power-Up Sequence and Timing.

Table 3. Power-Up/Power-Down/Reset Control Signals

Signal	Description
WL_REG_ON	This signal is used by the PMU (with BT_REG_ON) to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal CYW43570 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If BT_REG_ON and WL_REG_ON are both low, the regulators are disabled. This pin has an internal 200 kW pull-down resistor that is enabled by default. It can be disabled through programming.
BT_REG_ON	This signal is used by the PMU (with WL_REG_ON) to decide whether or not to power down the internal CYW43570 regulators. If BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. This pin has an internal 200 kW pull-down resistor that is enabled by default. It can be disabled through programming.

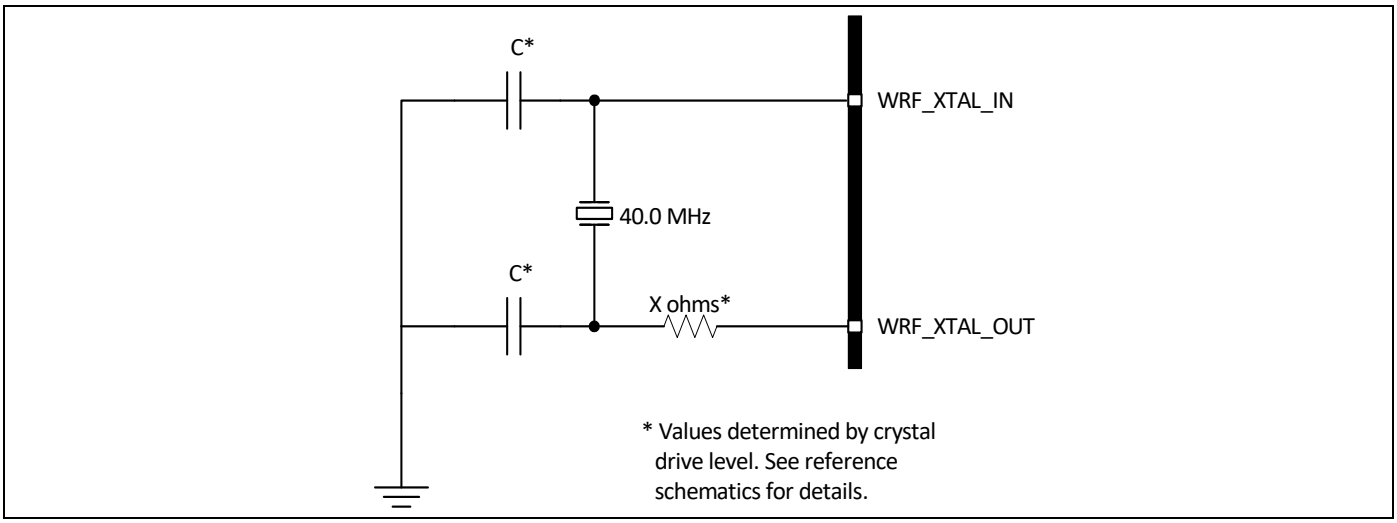
3. Frequency References

An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference may be used. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

3.1 Crystal Interface and Clock Generation

The CYW43570 can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in Figure 4. Consult the reference schematics for the latest configuration.

Figure 4. Recommended Oscillator Configuration



A fractional-N synthesizer in the CYW43570 generates the radio frequencies, clocks, and data/packet timing, enabling it to operate using a wide selection of frequency references.

The recommended default frequency reference is a 40.0 MHz crystal. The signal characteristics for the crystal interface are listed in Table 4.

Note: Although the fractional-N synthesizer can support alternative reference frequencies, frequencies other than the default require support to be added in the driver, plus additional extensive system testing. Contact Cypress for further details.

3.2 External Frequency Reference

Table 4. Crystal Oscillator and External Clock—Requirements and Performance

Parameter	Conditions/Notes	Crystal[a]			External Frequency Reference[b c]			
		Min	Typ	Max	Min	Typ	Max	Units
Frequency	2.4G and 5G bands: IEEE 802.11ac operation	–	40	–	–	–	–	MHz
Frequency tolerance over the lifetime of the equipment, including temperature[d]	Without trimming	–20	–	20	–20	–	20	ppm
Crystal load capacitance	–	–	12	–	–	–	–	pF
ESR	–	–	–	60	–	–	–	Ω
Drive level	External crystal must be able to tolerate this drive level.	200	–	–	–	–	–	µW
Input impedance (WRF_XTAL_IN)	Resistive	–	–	–	30	100	–	kΩ
	Capacitive	–	–	7.5	–	–	7.5	pF
WRF_XTAL_IN Input low level	DC-coupled digital signal	–	–	–	0	–	0.2	V
WRF_XTAL_IN Input high level	DC-coupled digital signal	–	–	–	1.0	–	1.26	V
WRF_XTAL_IN input voltage	AC-coupled analog signal	–	–	–	400	–	1200	mV_{p-p}
Duty cycle	40 MHz clock	–	–	–	40	50	60	%
Phase Noise[e] (IEEE 802.11b/g)	40 MHz clock at 10 kHz offset	–	–	–	–	–	–129	dBc/ Hz
	40 MHz clock at 100 kHz offset	–	–	–	–	–	–136	dBc/ Hz
Phase Noise[e] (IEEE 802.11a)	40 MHz clock at 10 kHz offset	–	–	–	–	–	–137	dBc/ Hz
	40 MHz clock at 100 kHz offset	–	–	–	–	–	–144	dBc/ Hz
Phase Noise[e] (IEEE 802.11n, 2.4 GHz)	40 MHz clock at 10 kHz offset	–	–	–	–	–	–134	dBc/ Hz
	40 MHz clock at 100 kHz offset	–	–	–	–	–	–141	dBc/ Hz
Phase Noise[e] (IEEE 802.11n, 5 GHz)	40 MHz clock at 10 kHz offset	–	–	–	–	–	–142	dBc/ Hz
	40 MHz clock at 100 kHz offset	–	–	–	–	–	–149	dBc/ Hz
Phase Noise[e] (IEEE 802.11ac, 5 GHz)	40 MHz clock at 10 kHz offset	–	–	–	–	–	–150	dBc/ Hz
	40 MHz clock at 100 kHz offset	–	–	–	–	–	–157	dBc/ Hz

a. (Crystal) Use WRF_XTAL_IN and WRF_XTAL_OUT.
b. See 3.2 External Frequency Reference for alternative connection methods.
c. For a clock reference other than 40 MHz, 20 × log10(f/40) dB should be added to the limits, where f = the reference clock frequency in MHz.
d. It is the responsibility of the equipment designer to select oscillator components that comply with these specifications.
e. Assumes that the external clock has a flat phase noise response above 100 kHz.

4. Bluetooth Overview

The CYW43570 is a Bluetooth 4.1 + EDR-compliant, baseband processor/2.4 GHz transceiver. It features the highest level of integration and eliminates all critical external components, thus minimizing the footprint, power consumption, and system cost of a Bluetooth radio solution.

The CYW43570 is the optimal solution for any Bluetooth voice and/or data application. The Bluetooth subsystem presents a standard host controller interface (HCI) via a high-speed UART and PCM for audio. The CYW43570 incorporates all Bluetooth 4.1 + EDR features including secure simple pairing, sniff subrating, and encryption pause and resume.

The CYW43570 Bluetooth radio transceiver provides enhanced radio performance to meet the most stringent mobile phone temperature applications and the tightest integration into mobile handsets and portable devices. It is fully compatible with any of the standard TCXO frequencies and provides full radio compatibility to operate simultaneously with GPS, WLAN, and cellular radios.

The Bluetooth transmitter also features a Class 1 power amplifier with Class 2 capability.

4.1 Features

Major Bluetooth features of the CYW43570 include:

- Supports key features of upcoming Bluetooth standards
- Fully supports Bluetooth Core Specification version 4.1 + EDR features:
  - Adaptive frequency hopping (AFH)
  - Quality of service (QoS)
  - Extended synchronous connections (eSCO)—voice connections
  - Fast connect (interlaced page and inquiry scans)
  - Secure simple pairing (SSP)
  - Sniff subrating (SSR)
  - Encryption pause resume (EPR)
  - Extended inquiry response (EIR)
  - Link supervision timeout (LST)
- UART baud rates up to 4 Mbps
- Supports all Bluetooth 4.1 + EDR packet types
- Maximum Bluetooth data rates over HCI UART (interface capable but not currently supported in the software driver)
- BT supports full-speed USB 2.0-compliant interface
- Multipoint operation with up to seven active slaves
  - Maximum of seven simultaneous active ACL links
  - Maximum of three simultaneous active SCO and eSCO connections with scatternet support
- Trigger Broadcom fast connect (TBFC)
- Narrowband and wideband packet loss concealment
- Scatternet operation with up to four active piconets with background scan and support for scatter mode
- High-speed HCI UART transport support with low-power out-of-band BT_DEV_WAKE and BT_HOST_WAKE signaling (see Host Controller Power Management)
- Channel quality driven data rate and packet type selection
- Standard Bluetooth test modes
- Extended radio and production test mode features

- Full support for power savings modes
  - Bluetooth clock request
  - Bluetooth standard sniff
  - Deep-sleep modes and software regulator shutdown
- TCXO input and auto-detection of all standard handset clock frequencies. Also supports a low-power crystal, which can be used during power save mode for better timing accuracy.
- Improved audio interface capabilities with full-featured bidirectional PCM and I^2S
- I^2S can be master or slave

4.2 Bluetooth Radio

The CYW43570 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with the Bluetooth Radio Specification and EDR specification and meets or exceeds the requirements to provide the highest communication link quality of service. An integrated T/R switch combines Bluetooth transmit and receive paths, and connects directly to a dedicated Bluetooth antenna.

4.2.1 Transmit

The CYW43570 features a fully integrated zero-IF transmitter. The baseband transmit data is GFSK-modulated in the modem block and upconverted to the 2.4 GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q upconversion, output power amplifier, and RF filtering. The transmitter path also incorporates π/4-DQPSK for 2 Mbps and 8-DPSK for 3 Mbps to support EDR. The transmitter section is compatible to the Bluetooth Low Energy specification. The transmitter PA bias can also be adjusted to provide Bluetooth class 1 or class 2 operation.

4.2.2 Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK, π/4-DQPSK, and 8-DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

4.2.3 Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit-synchronization algorithm.

4.2.4 Power Amplifier

The fully integrated PA supports Class 1 or Class 2 output using a highly linearized, temperature-compensated design. This provides greater flexibility in front-end matching and filtering. Due to the linear nature of the PA combined with some integrated filtering, external filtering is required to meet the Bluetooth and regulatory harmonic and spurious requirements. For integrated mobile handset applications in which Bluetooth is integrated next to the cellular radio, external filtering can be applied to achieve near thermal noise levels for spurious and radiated noise emissions. The transmitter features a sophisticated on-chip transmit signal strength indicator (TSSI) block to keep the absolute output power variation within a tight range across process, voltage, and temperature.

4.2.5 Receiver

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology with built-in out-of-band attenuation enables the CYW43570 to be used in most applications with minimal off-chip filtering. For integrated handset operation, in which the Bluetooth function is integrated close to the cellular transmitter, external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

4.2.6 Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

4.2.7 Receiver Signal Strength Indicator

The radio portion of the CYW43570 provides a receiver signal strength indicator (RSSI) signal to the baseband, so that the controller can take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

4.2.8 Local Oscillator Generation

A local oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation subblock employs an architecture for high immunity to LO pulling during PA operation. The CYW43570 uses an internal RF and IF loop filter.

4.2.9 Calibration

The CYW43570 radio transceiver features an automated calibration scheme that is fully self contained in the radio. No user interaction is required during normal operation or during manufacturing to provide the optimal performance. Calibration optimizes the performance of all the major blocks within the radio to within 2% of optimal conditions, including gain and phase characteristics of filters, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. Calibration occurs transparently during normal operation during the settling time of the hops and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

5. Bluetooth Baseband Core

The Bluetooth baseband core (BBC) implements all of the time critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewhitening in the receiver.
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

5.1 Bluetooth 4.1 Features

The BBC supports all Bluetooth 4.1 features with the following benefits:

- Dual-mode Bluetooth low energy (BT and BLE operation)
- Extended inquiry response (EIR): Shortens the time to retrieve the device name, specific profile, and operating mode.
- Encryption pause resume (EPR): Enables the use of Bluetooth technology in a much more secure environment.
- Sniff subrating (SSR): Optimizes power consumption for low duty cycle asymmetric data flow, which subsequently extends battery life.
- Secure simple pairing (SSP): Reduces the number of steps for connecting two devices, with minimal or no user interaction required.
- Link supervision time out (LSTO): Additional commands added to HCI and link management protocol (LMP) for improved link time-out supervision.
- QoS enhancements: Changes to data traffic control, which results in better link performance. Audio, human interface device (HID), bulk traffic, SCO, and enhanced SCO (eSCO) are improved with the erroneous data (ED) and packet boundary flag (PBF) enhancements.

5.2 Bluetooth Low Energy

The CYW43570 supports the Bluetooth Low Energy operating mode.

5.3 Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller, to perform the link control tasks. Each task performs a different state in the Bluetooth link controller.

- Major states:
  - Standby
  - Connection
- Substates:
  - Page
  - Page Scan
  - Inquiry
  - Inquiry Scan
  - Sniff

5.4 Test Mode Support

The CYW43570 fully supports Bluetooth Test mode as described in Part I:1 of the Specification of the Bluetooth System Version 3.0. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth Test Mode, the CYW43570 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - Eight-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

5.5 Bluetooth Power Management Unit

The Bluetooth power management unit (PMU) provides power management features that can be invoked by either software through power management registers or packet handling in the baseband core. The power management functions provided by the CYW43570 are:

- RF Power Management
- Host Controller Power Management
- BBC Power Management

5.5.1 RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver. The transceiver then processes the power-down functions accordingly.

5.5.2 Host Controller Power Management

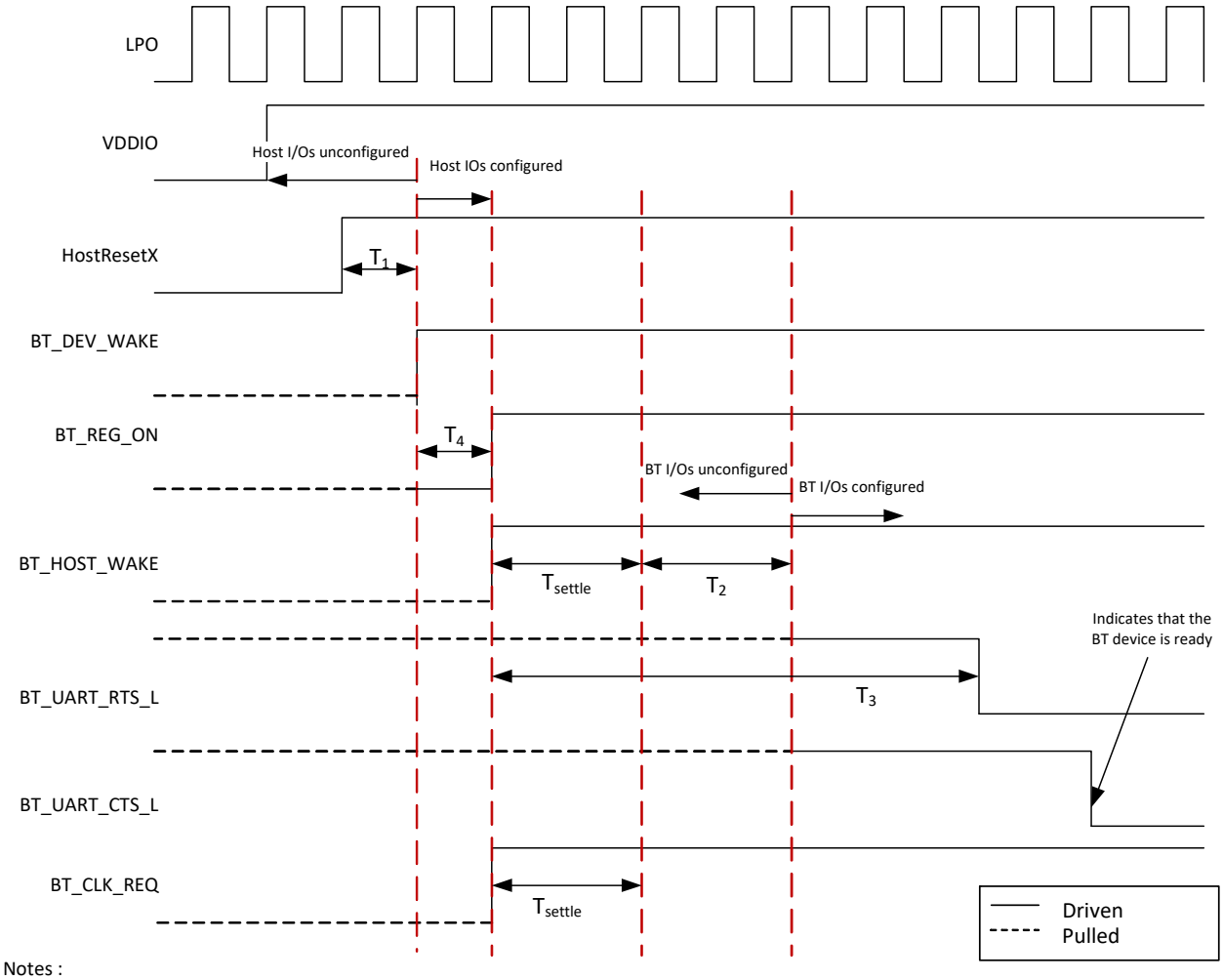
When running in UART mode, the CYW43570 can be configured so that dedicated signals are used for power management handshaking between it and the host. The basic power-saving functions supported by those hand-shaking signals include the standard Bluetooth defined power savings modes and standby modes of operation.

Table 5 describes the power-control hand-shake signals used with the UART interface.

Table 5. Power Control Pin Description

Signal	Mapped to Pin	Type	Description
BT_DEV_WAKE	J1	I	Bluetooth device wake-up: Signal from the host to the CYW43570 indicating that the host requires attention. ■ Asserted: The Bluetooth device must wake-up or remain awake. ■ Deasserted: The Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
BT_HOST_WAKE	J2	O	Host wake up. Signal from the CYW43570 to the host indicating that the CYW43570 requires attention. ■ Asserted: host device must wake-up or remain awake. ■ Deasserted: host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low. This is an active-low signal that require external pull-up resistor 10k for operation.
BT_CLK_REQ	J5	O	The CYW43570 asserts BT_CLK_REQ when Bluetooth or WLAN wants the host to turn on the reference clock. The BT_CLK_REQ polarity is active-high. Add an external 100 kΩ pull-down resistor to ensure the signal is deasserted when the CYW43570 powers up or resets when VDDIO is present.
Note: Pad function Control Register is set to 0 for these pins (see Section 13. DC Characteristics).			

Figure 5. Startup Signaling Sequence



Notes :

T_1 is the time for host to settle its IOs after a reset.

T_2 is the time for the BTH device to settle its IOs after a reset and reference clockk settling time elapsed.

T_3 is the time for the BT device to complete initialization and drive BT_UART_RTS_L low.

T_4 is the setup time for BT_DEV_WAKE prior to driving BT_REG_ON high; BT_DEV_WAKE must be high prior to BT_REG_ON being released. BT_DEV_WAKE should not be driven low until after the host has completed configuration.

T_{settle} is the time for the reference clock signal from the host to be guaranteed to have settled.

5.5.3 BBC Power Management

The following are low-power operations for the BBC:

- Physical layer packet-handling turns the RF on and off dynamically within transmit/receive packets.
- Bluetooth-specified low-power connection modes: sniff, hold, and park. While in these modes, the CYW43570 runs on the low-power oscillator and wakes up after a predefined time period.
- A low-power shutdown feature allows the device to be turned off while the host and any other devices in the system remain operational. When the CYW43570 is not needed in the system, the RF and core supplies are shut down while the I/O remains powered. This allows the CYW43570 to effectively be off while keeping the I/O pins powered so they do not draw extra current from any other devices connected to the I/O.

  During the low-power shut-down state, provided VDDIO remains applied to the CYW43570, all outputs are tristated, and most input signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system and enables the CYW43570 to be fully integrated in an embedded device to take full advantage of the lowest power-saving modes.

  Two CYW43570 input signals are designed to be high-impedance inputs that do not load the driving signal even if the chip does not have VDDIO power supplied to it: the frequency reference input (WRF_TCXO_IN) and the 32.768 kHz input (LPO). When the CYW43570 is powered on from this state, it is the same as a normal power-up, and the device does not contain any information about its state from the time before it was powered down.

5.5.4 Wideband Speech

The CYW43570 provides support for wideband speech (WBS) using on-chip SmartAudio technology. The CYW43570 can perform subband codec (SBC), as well as mSBC, encoding, and decoding of linear 16 bits at 16 kHz (256 kbps rate) transferred over the PCM bus.

5.5.5 Packet Loss Concealment

Packet loss concealment (PLC) improves apparent audio quality for systems with marginal link performance. Bluetooth messages are sent in packets. When a packet is lost, it creates a gap in the received audio bit-stream. Packet loss can be mitigated in several ways:

- Fill in zeros.
- Ramp down the output audio signal toward zero (this is the method used in current Bluetooth headsets).
- Repeat the last frame (or packet) of the received bit-stream and decode it as usual (frame repeat).

These techniques cause distortion and popping in the audio stream. The CYW43570 uses a proprietary waveform extension algorithm to provide dramatic improvement in the audio quality. Figure 6 and Figure 7 show audio waveforms with and without Packet Loss Concealment. Cypress PLC/BEC algorithms also support wideband speech.

Figure 6. CVSD Decoder Output Waveform Without PLC

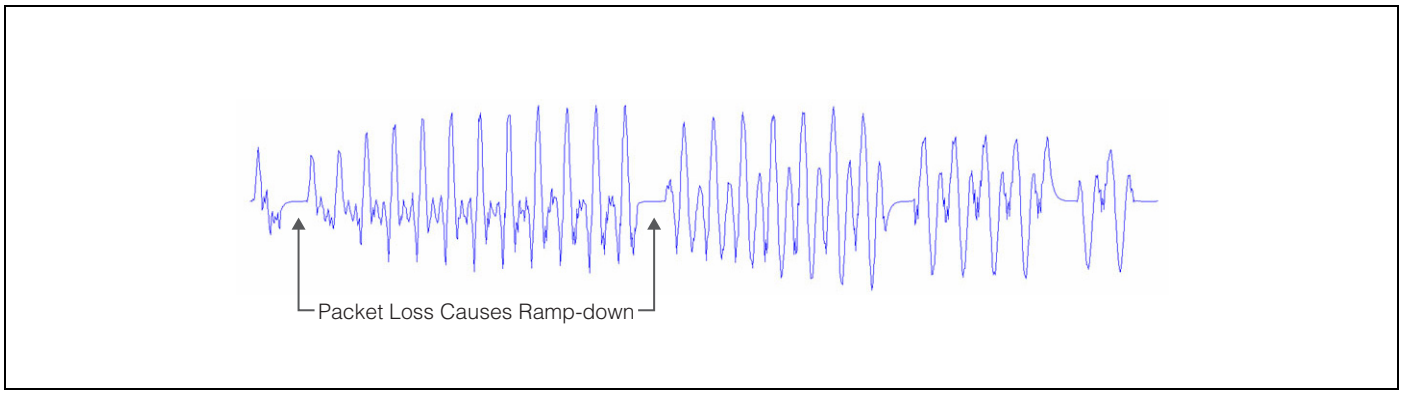
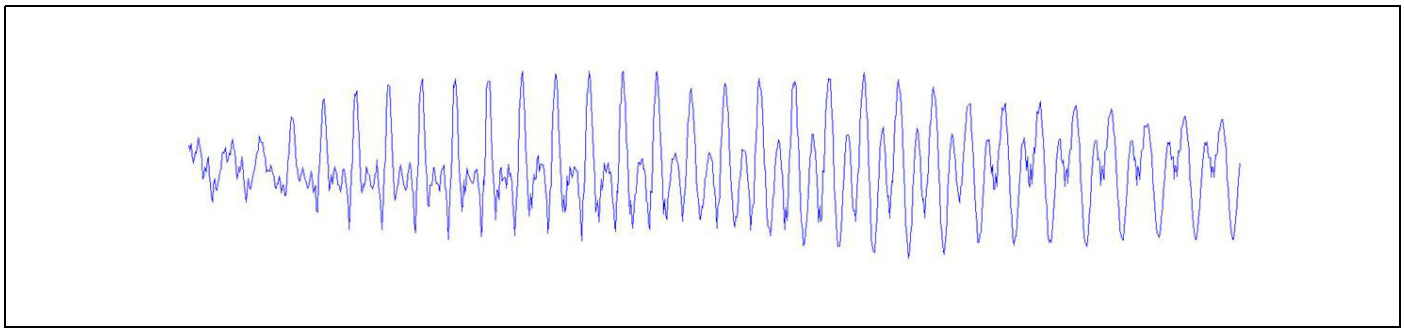


Figure 7. CVSD Decoder Output Waveform After Applying PLC



5.5.6 Audio Rate-Matching Algorithms

The CYW43570 has an enhanced rate-matching algorithm that uses interpolation algorithms to reduce audio stream jitter that may be present when the rate of audio data coming from the host is not the same as the Bluetooth audio data rates.

5.5.7 Codec Encoding

The CYW43570 can support SBC and mSBC encoding and decoding for wideband speech.

5.5.8 Multiple Simultaneous A2DP Audio Stream

The CYW43570 has the ability to take a single audio stream and output it to multiple Bluetooth devices simultaneously. This allows a user to share his or her music (or any audio stream) with a friend.

5.5.9 Burst Buffer Operation

The CYW43570 has a data buffer that can buffer data being sent over the HCI and audio transports, then send the data at an increased rate. This mode of operation allows the host to sleep for the maximum amount of time, dramatically reducing system current consumption.

5.6 Adaptive Frequency Hopping

The CYW43570 gathers link quality statistics on a channel by channel basis to facilitate channel assessment and channel map selection. The link quality is determined using both RF and baseband signal processing to provide a more accurate frequency-hop map.

5.7 Advanced Bluetooth/WLAN Coexistence

The CYW43570 includes advanced coexistence technologies that are only possible with a Bluetooth/WLAN integrated die solution. These coexistence technologies are targeted at small form-factor platforms, such as smart TVs, over-the-top (OTT) boxes, set-top boxes, and wireless speakers, including applications such as VoWLAN + SCO and video-over-WLAN + high-fidelity BT stereo.

The CYW43570 integrated solution enables MAC-layer signaling (firmware) and a greater degree of sharing via an enhanced coexistence interface. Information is exchanged between the Bluetooth and WLAN cores without host processor involvement.

The CYW43570 also supports Transmit Power Control on the STA together with standard Bluetooth TPC to limit mutual interference and receiver desensitization. Preemption mechanisms are utilized to prevent AP transmissions from colliding with Bluetooth frames. Improved channel classification techniques have been implemented in Bluetooth for faster and more accurate detection and elimination of interferers (including non-WLAN 2.4 GHz interference).

The Bluetooth AFH classification is also enhanced by the WLAN core’s channel information.

5.8 Fast Connection (Interlaced Page and Inquiry Scans)

The CYW43570 supports page scan and inquiry scan modes that significantly reduce the average inquiry response and connection times. These scanning modes are compatible with the Bluetooth version 2.1 page and inquiry procedures.

6. Microprocessor and Memory Unit for Bluetooth

The Bluetooth microprocessor core is based on the ARM Cortex-M3 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. It runs software from the link control (LC) layer, up to the host controller interface (HCI).

The ARM core is paired with a memory unit that contains 668 KB of ROM memory for program storage and boot ROM, 200 KB of RAM for data scratchpad and patch RAM code. The internal ROM allows for flexibility during power-on reset to enable the same device to be used in various configurations. At power-up, the lower-layer protocol stack is executed from the internal ROM memory.

External patches may be applied to the ROM-based firmware to provide flexibility for bug fixes or features additions. These patches may be downloaded from the host to the CYW43570 through the UART transports.

6.1 RAM, ROM, and Patch Memory

The CYW43570 Bluetooth core has 200 KB of internal RAM which is mapped between general purpose scratch pad memory and patch memory and 668 KB of ROM used for the lower-layer protocol stack, test mode software, and boot ROM. The patch memory capability enables the addition of code changes for purposes of feature additions and bug fixes to the ROM memory.

6.2 Reset

The CYW43570 has an integrated power-on reset circuit that resets all circuits to a known power-on state. The BT power-on reset (POR) circuit is out of reset after BT_REG_ON goes high. If BT_REG_ON is low, then the POR circuit is held in reset.

7. Bluetooth Peripheral Transport Unit

7.1 SPI/UART Transport Detection

The BT_HOST_WAKE pin is also used for BT transport detection. The transport detection occurs during the power-up sequence. It selects either UART or SPI transport operation based on the following pin states:

- If the BT_HOST_WAKE pin is pulled low by an external pull-down during power-up, it selects the SPI transport interface.
- If the BT_HOST_WAKE pin is not pulled low externally during power-up, then the default internal pull-up is detected as a high and it selects the UART transport interface.

7.2 PCM Interface

The CYW43570 supports two independent PCM interfaces that share pins with the serial flash interfaces.

Table 6 shows PCM signal mapping used in this data sheet:

Table 6. PCM-to-Serial Flash Interface Mapping

PCM Interface Pins	Serial Flash Interface Pins
BT_PCM_CLK	BT_SF_CLK
BT_PCM_IN	BT_SF_MISO
BT_PCM_OUT	BT_SF_MOSI
BT_PCM_SYNC	BT_SF_CS_L

The PCM Interface on the CYW43570 can connect to linear PCM Codec devices in master or slave mode. In master mode, the CYW43570 generates the BT_PCM_CLK and BT_PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the CYW43570.

The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

7.2.1 Slot Mapping

The CYW43570 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate of 128 kHz, 512 kHz, or 1024 kHz. The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

7.2.2 Frame Synchronization

The CYW43570 supports both short- and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

7.2.3 Data Formatting

The CYW43570 may be configured to generate and accept several different data formats. For conventional narrow band speech mode, the CYW43570 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2’s complement data, left justified, and clocked MSB first.

7.2.4 Wideband Speech Support

When the host encodes wideband speech (WBS) packets in transparent mode, the encoded packets are transferred over the PCM bus for an eSCO voice connection. In this mode, the PCM bus is typically configured in master mode for a 4 kHz sync rate with 16-bit samples, resulting in a 64 kbps bit rate. The CYW43570 also supports slave transparent mode using a proprietary rate-matching scheme. In SBC-code mode, linear 16-bit data at 16 kHz (256 kbps rate) is transferred over the PCM bus.

7.2.5 Burst PCM Mode

In this mode of operation, the PCM bus runs at a significantly higher rate of operation to allow the host to duty cycle its operation and save current. In this mode of operation, the PCM bus can operate at a rate of up to 24 MHz. This mode of operation is initiated with an HCI command from the host.

7.2.6 PCM Interface Timing

Short Frame Sync, Master Mode

Figure 8. PCM Timing Diagram (Short Frame Sync, Master Mode)

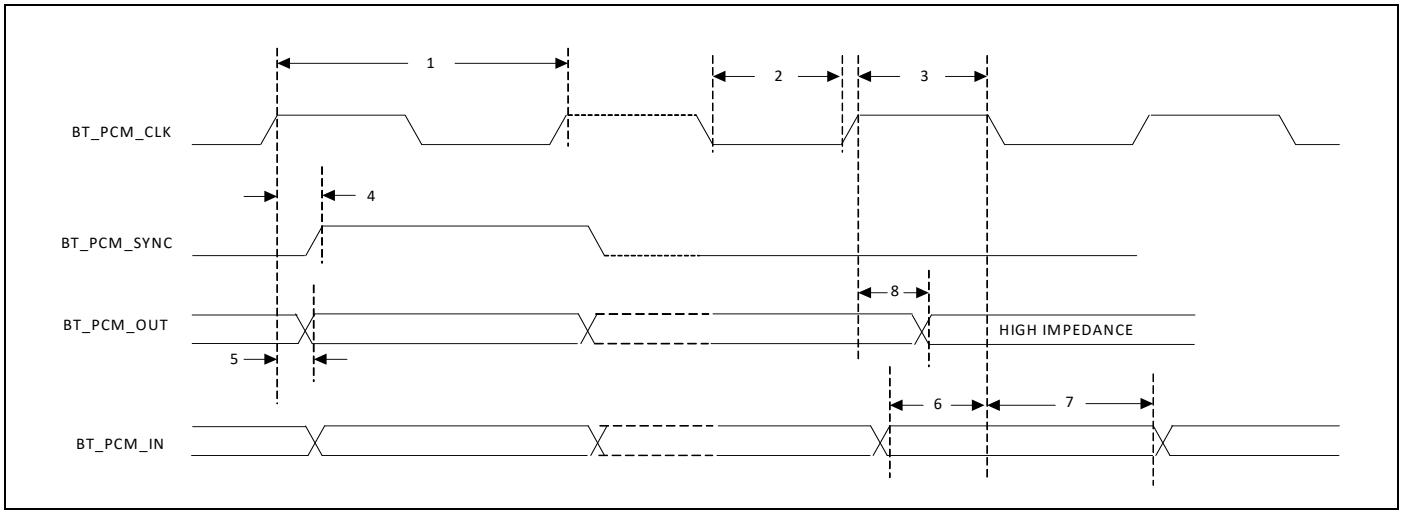


Table 7. PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	BT_PCM_SYNC delay	0	–	25	ns
5	BT_PCM_OUT delay	0	–	25	ns
6	BT_PCM_IN setup	8	–	–	ns
7	BT_PCM_IN hold	8	–	–	ns
8	Delay from rising edge of BT_PCM_BCLK during last bit period to BT_PCM_OUT becoming high impedance.	0	–	25	ns

Short Frame Sync, Slave Mode

Figure 9. PCM Timing Diagram (Short Frame Sync, Slave Mode)

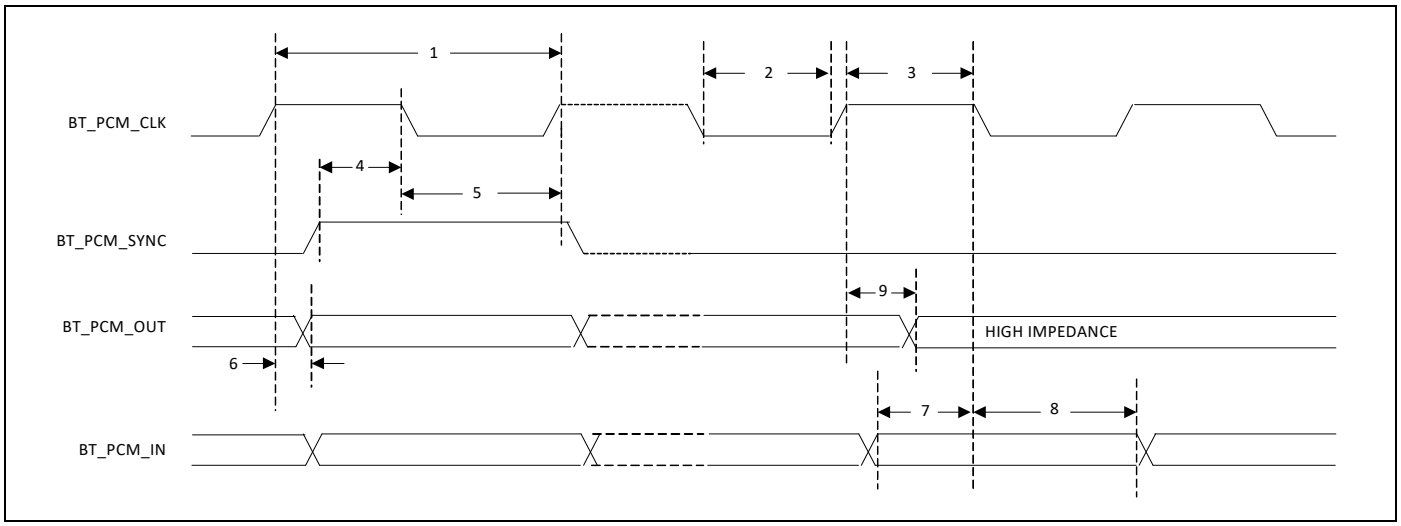


Table 8. PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	BT_PCM_SYNC setup	8	–	–	ns
5	BT_PCM_SYNC hold	8	–	–	ns
6	BT_PCM_OUT delay	0	–	25	ns
7	BT_PCM_IN setup	8	–	–	ns
8	BT_PCM_IN hold	8	–	–	ns
9	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance.	0	–	25	ns

Long Frame Sync, Master Mode

Figure 10. PCM Timing Diagram (Long Frame Sync, Master Mode)

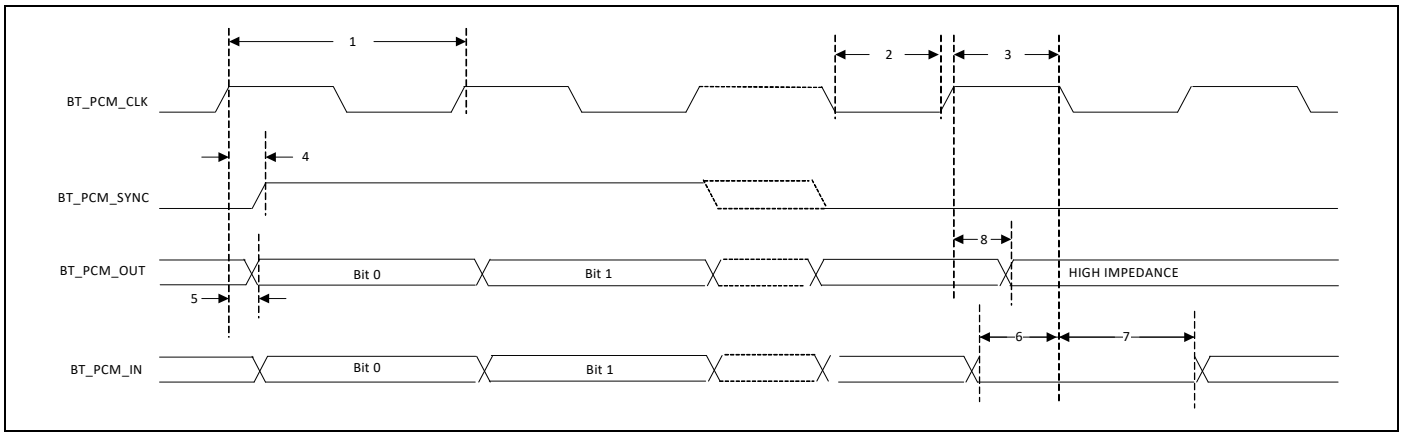


Table 9. PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	BT_PCM_SYNC delay	0	–	25	ns
5	BT_PCM_OUT delay	0	–	25	ns
6	BT_PCM_IN setup	8	–	–	ns
7	BT_PCM_IN hold	8	–	–	ns
8	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance.	0	–	25	ns

Long Frame Sync, Slave Mode

Figure 11. PCM Timing Diagram (Long Frame Sync, Slave Mode)

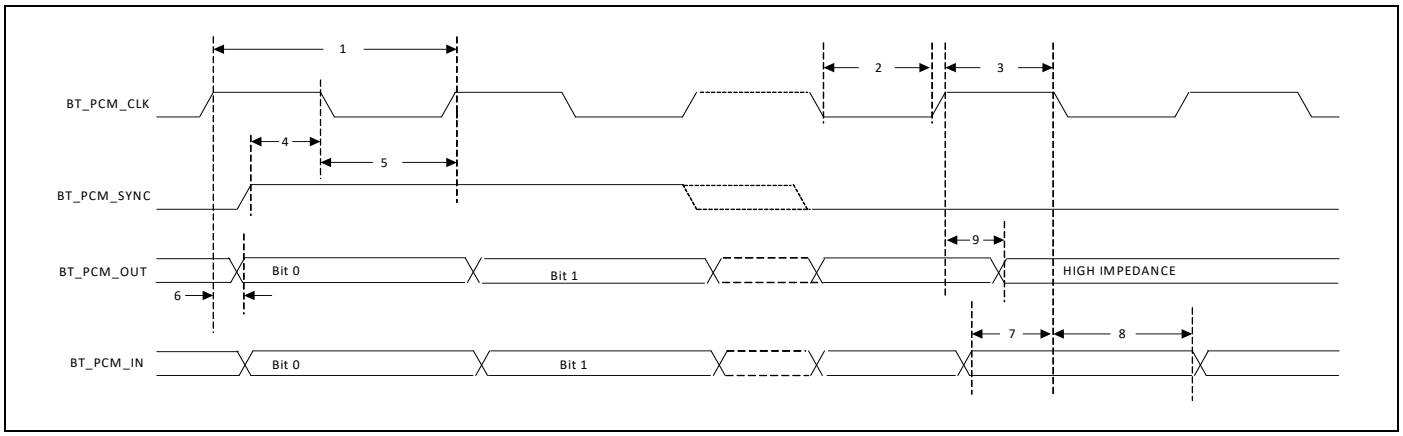


Table 10. PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
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4	BT_PCM_SYNC setup	8	–	–	ns
5	BT_PCM_SYNC hold	8	–	–	ns
6	BT_PCM_OUT delay	0	–	25	ns
7	BT_PCM_IN setup	8	–	–	ns
8	BT_PCM_IN hold	8	–	–	ns
9	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance.	0	–	25	ns

Short Frame Sync, Burst Mode

Figure 12. PCM Burst Mode Timing (Receive Only, Short Frame Sync)

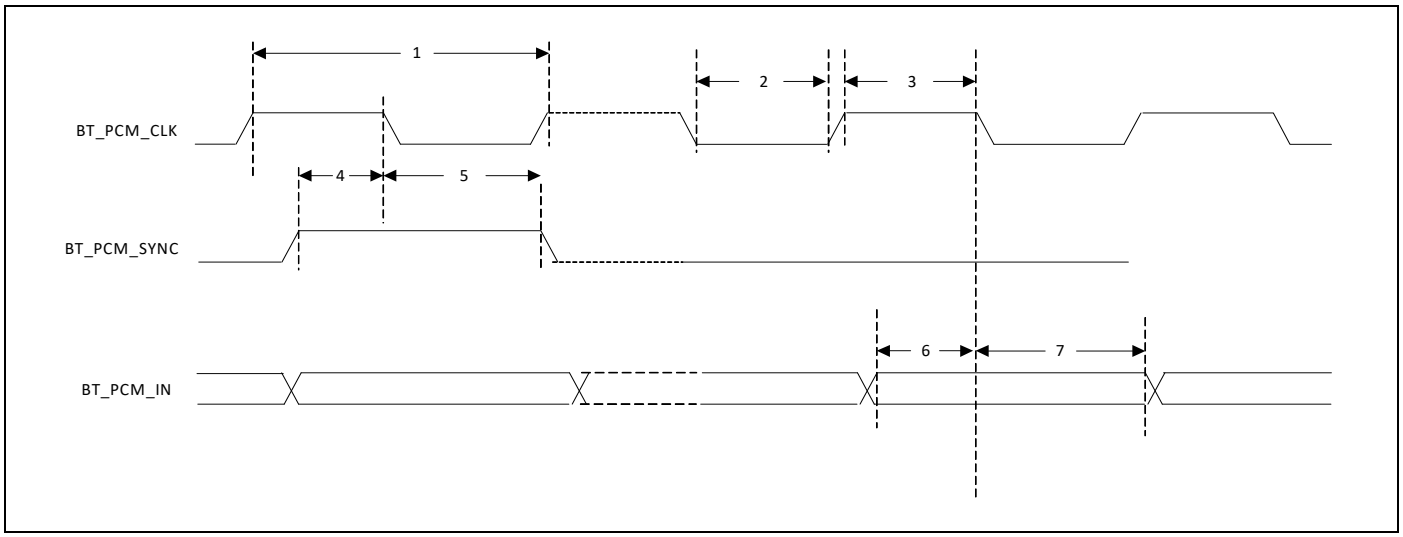


Table 11. PCM Burst Mode (Receive Only, Short Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock LOW	20.8	–	–	ns
3	PCM bit clock HIGH	20.8	–	–	ns
4	BT_PCM_SYNC setup	8	–	–	ns
5	BT_PCM_SYNC hold	8	–	–	ns
6	BT_PCM_IN setup	8	–	–	ns
7	BT_PCM_IN hold	8	–	–	ns

Long Frame Sync, Burst Mode

Figure 13. PCM Burst Mode Timing (Receive Only, Long Frame Sync)

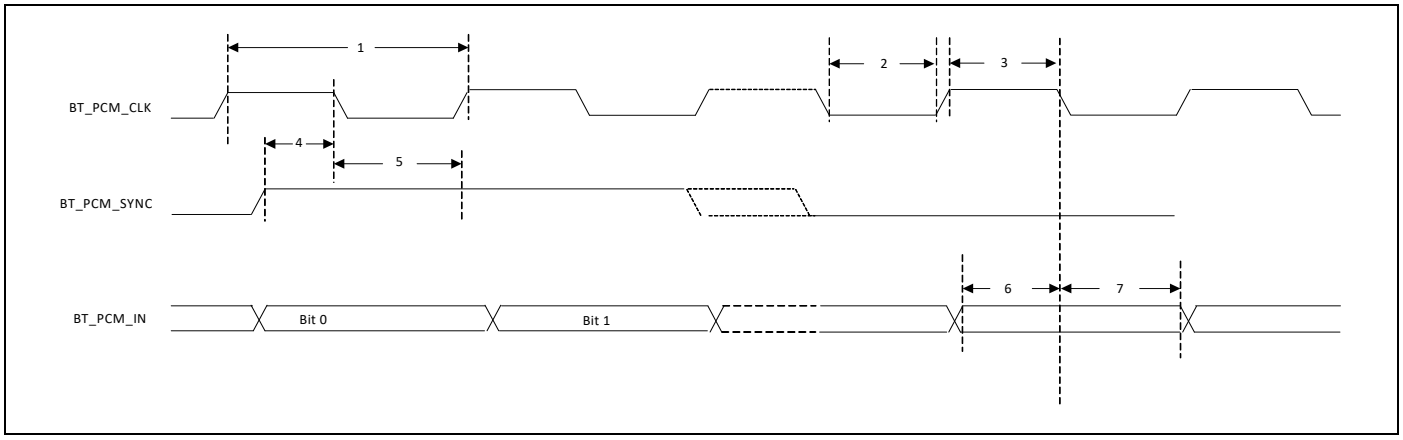


Table 12. PCM Burst Mode (Receive Only, Long Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock LOW	20.8	–	–	ns
3	PCM bit clock HIGH	20.8	–	–	ns
4	BT_PCM_SYNC setup	8	–	–	ns
5	BT_PCM_SYNC hold	8	–	–	ns
6	BT_PCM_IN setup	8	–	–	ns
7	BT_PCM_IN hold	8	–	–	ns

7.3 USB Interface

7.3.1 Features

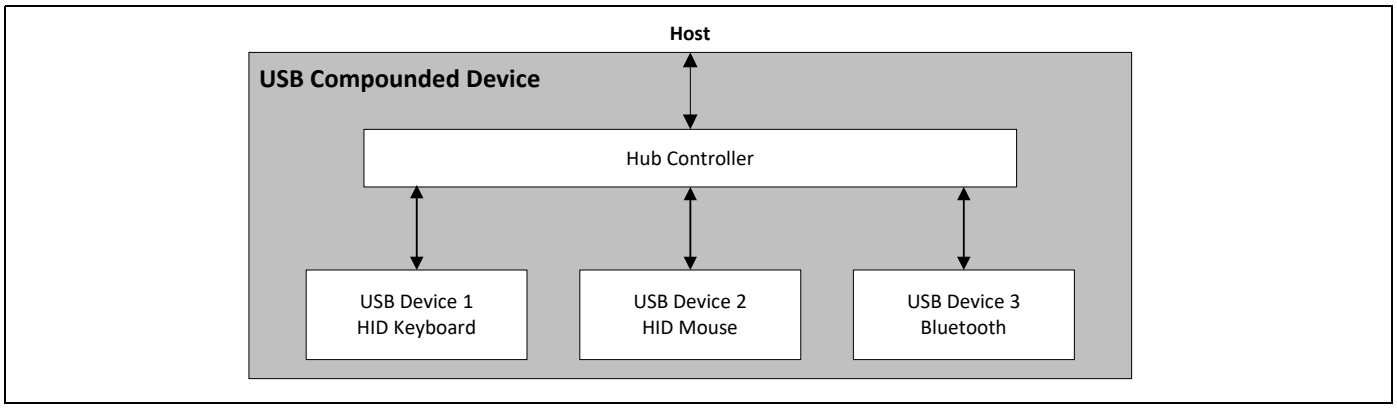
The following USB interface features are supported:

- USB Protocol, Revision 2.0, full-speed (12 Mbps) compliant including the hub
- Optional hub compound device with up to three device cores internal to device
- Bus or self-power, dynamic configuration for the hub
- Global and selective suspend and resume with remote wakeup
- Bluetooth HCI
- HID and DFU
- Integrated detach resistor

7.3.2 Operation

The CYW43570 can be configured to boot up as either a single USB peripheral or a USB hub with several USB peripherals attached. As a single peripheral, the host detects a single USB Bluetooth device. In hub mode, the host detects a hub with one to three of the ports already connected to USB devices (see Figure 14).

Figure 14. USB Compounded Device Configuration



Depending on the desired hub mode configuration, the CYW43570 can boot up showing the three ports connected to logical USB devices internal to the CYW43570: a generic Bluetooth device, a mouse, and a keyboard. In this mode, the mouse and keyboard are emulated devices, since they connect to real HID devices via a Bluetooth link. The Bluetooth link to these HID devices is hidden from the USB host. To the host, the mouse and/or keyboard appear to be directly connected to the USB port.

The USB device, configuration, and string descriptors are fully programmable, allowing manufacturers to customize the descriptors, including vendor and product IDs, the CYW43570 uses to identify itself on the USB port. To make custom USB descriptor information available at boot time, stored it in external NVRAM.

Despite the mode of operation (single peripheral or hub), the Bluetooth device is configured to include the following interfaces:

Interface 0	Contains a Control endpoint (Endpoint 0x00) for HCI commands, a Bulk In Endpoint (Endpoint 0x82) for receiving ACL data, a Bulk Out Endpoint (Endpoint 0x02) for transmitting ACL data, and an Interrupt Endpoint (Endpoint 0x81) for HCI events.
Interface 1	Contains Isochronous In and Out endpoints (Endpoints 0x83 and 0x03) for SCO traffic. Several alternate Interface 1 settings are available for reserving the proper bandwidth of isochronous data (depending on the application).
Interface 2	Contains Bulk In and Bulk Out endpoints (Endpoints 0x84 and 0x04) used for proprietary testing and debugging purposes. These endpoints can be ignored during normal operation.

The CYW43570 supports the USB hub and device model (USB, Revision 2.0, full-speed compliant).

When the hub is enabled, the CYW43570 handles all standard USB functions for the following devices:

- HID keyboard
- HID mouse
- Bluetooth

All hub and device descriptors are firmware-programmable. This USB compound device configuration (see Figure 14) supports up to three downstream ports. This configuration can also be programmed to a single USB device core. The device automatically detects activity on the USB interface when connected. Therefore, no special configuration is needed to select HCI as the transport.

The hub's downstream port definition is as follows:

- Port 1 USB lite device core (for HID applications)
- Port 2 USB lite device core (for HID applications)
- Port 3 USB full device core (for Bluetooth applications)

When operating in hub mode, all three internal devices do not have to be enabled. Each internal USB device can be optionally enabled. The configuration record in NVRAM determines which devices are present.

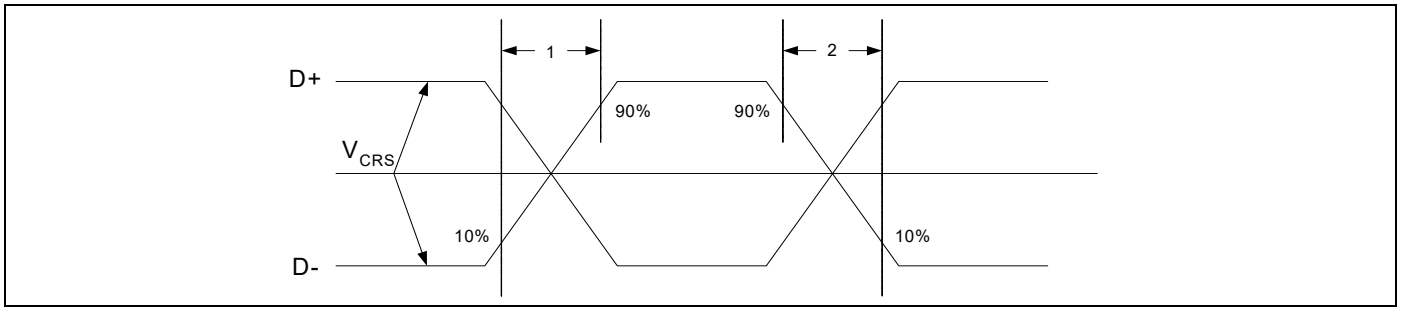
7.3.3 USB Full-Speed Timing

Table 13 shows timing specifications for the VDD_USB = 3.3V, V_{SS} = 0V, and T_A = 0°C to 85°C operating temperature range.

Table 13. USB Full-Speed Timing Specifications

Reference	Characteristics	Minimum	Maximum	Unit
1	Transition rise time	4	20	ns
2	Transition fall time	4	20	ns
3	Rise/fall timing matching	90	111	%
4	Full-speed data rate	12 – 0.25%	12 + 0.25%	Mbps

Figure 15. USB Full-Speed Timing



7.4 UART Interface

The CYW43570 has a UART host interface for Bluetooth. The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

The UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 4.1 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (*Three-wire UART Transport Layer*). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The CYW43570 UART can perform XON/XOFF flow control and includes hardware support for the serial line input protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The CYW43570 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

Table 14. Example of Common Baud Rates

Desired Rate	Actual Rate	Error (%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

Figure 16. UART Timing

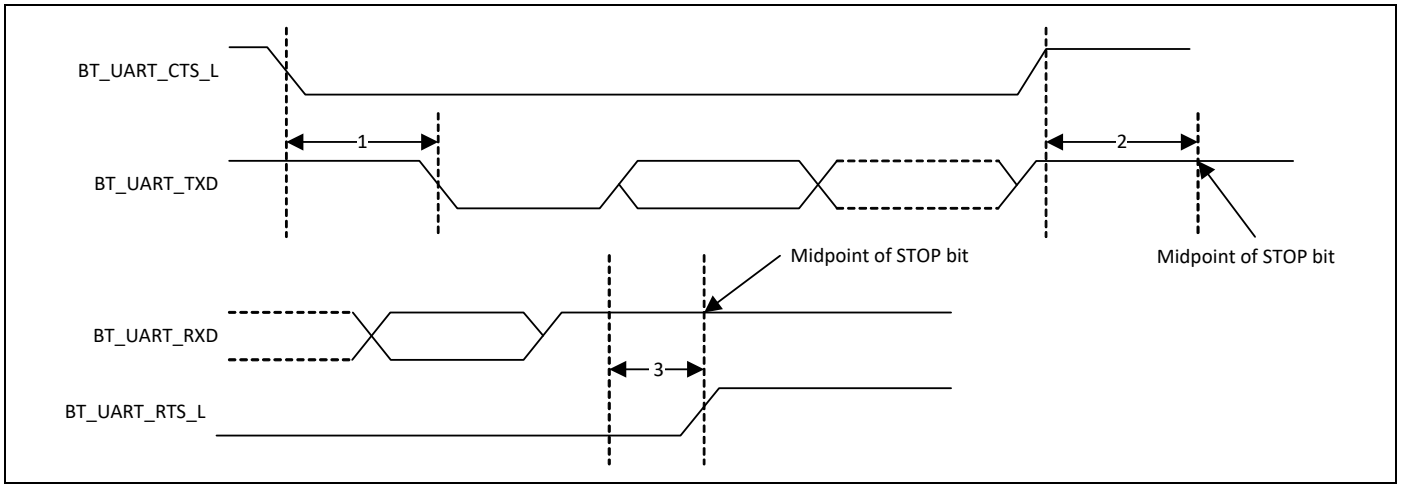


Table 15. UART Timing Specifications

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	Delay time, BT_UART_CTS_L low to BT_UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, BT_UART_CTS_L high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_L high	–	–	0.5	Bit periods

7.5 I²S Interface

The CYW43570 supports an I²S digital audio port for Bluetooth audio. The I²S interface supports both master and slave modes. The I²S signals are:

- I²S clock: BT_I2S_CLK
- I²S Word Select: BT_I2S_WS
- I²S Data Out: BT_I2S_DO
- I²S Data In: BT_I2S_DI

BT_I2S_CLK and BT_I2S_WS become outputs in master mode and inputs in slave mode, whereas BT_I2S_DO always stays as an output. The channel word length is 16 bits, and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I²S bus, in accord with the I²S specification. The MSB of each data word is transmitted one bit clock cycle after the BT_I2S_WS transition, synchronous with the falling edge of the bit clock. Left-channel data is transmitted when IBT_I2S_WS is low, and right-channel data is transmitted when BT_I2S_WS is high. Data bits sent by the CYW43570 are synchronized with the falling edge of BT_I2S_CLK and should be sampled by the receiver on the rising edge of BT_I2S_CLK.

The clock rate in master mode is either of the following:

- 48 kHz x 32 bits per frame = 1.536 MHz
- 48 kHz x 50 bits per frame = 2.400 MHz

The master clock is generated from the input reference clock using a N/M clock divider.

In the slave mode, any clock rate is supported to a maximum of 3.072 MHz.

7.5.1 I^2S Timing

Note: Timing values specified in Table 16 are relative to high and low threshold levels.

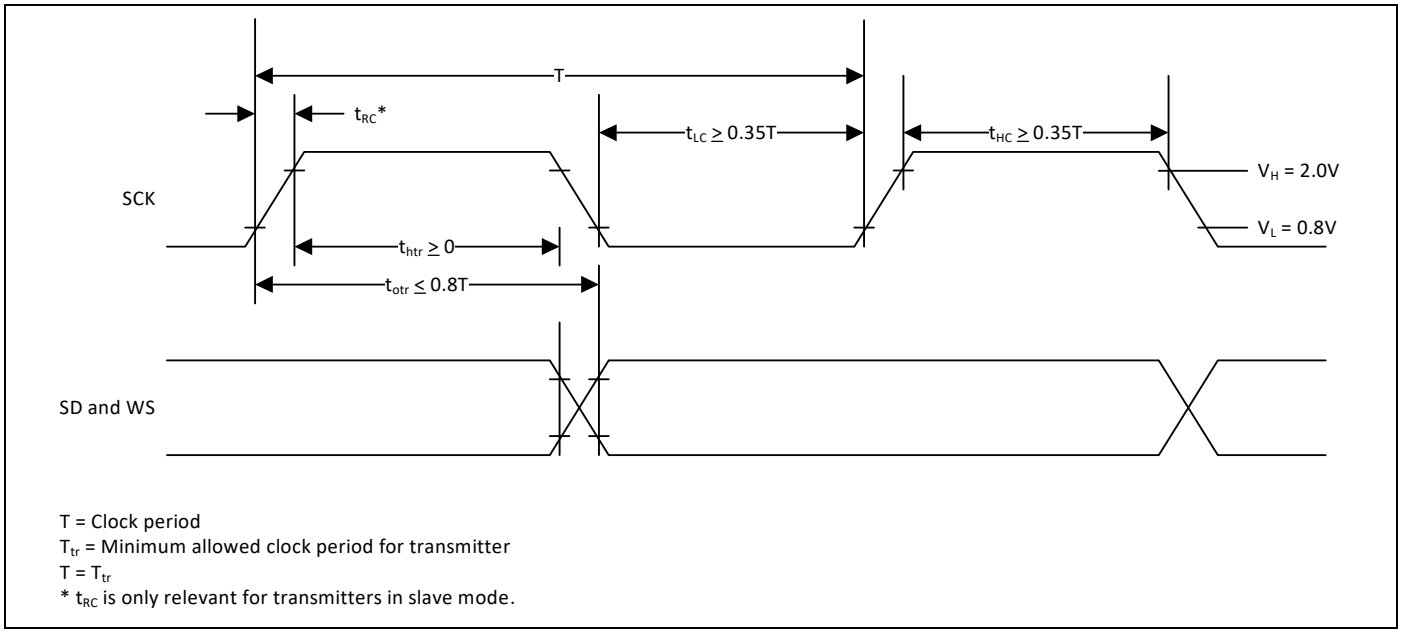
Table 16. Timing for I^2S Transmitters and Receivers

	Transmitter				Receiver				
	Lower LImit		Upper Limit		Lower Limit		Upper Limit		
	Min	Max	Min	Max	Min	Max	Min	Max	Notes
Clock Period T	T_{tr}	–	–	–	T_r	–	–	–	a
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	b
LOWt_{LC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	b
Slave Mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	c
LOW t_{LC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	c
Rise time t_{RC}	–	–	$0.15T_{tr}$	–	–	–	–	–	d
Transmitter									
Delay t_{dtr}	–	–	–	0.8T	–	–	–	–	e
Hold time t_{htr}	0	–	–	–	–	–	–	–	d
Receiver									
Setup time t_{sr}	–	–	–	–	–	$0.2T_r$	–	–	f
Hold time t_{hr}	–	–	–	–	–	0	–	–	f

a. The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
b. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.
c. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used.
d. Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{tr}$.
e. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
f. The data setup and hold time must not be less than the specified receiver setup and hold time.

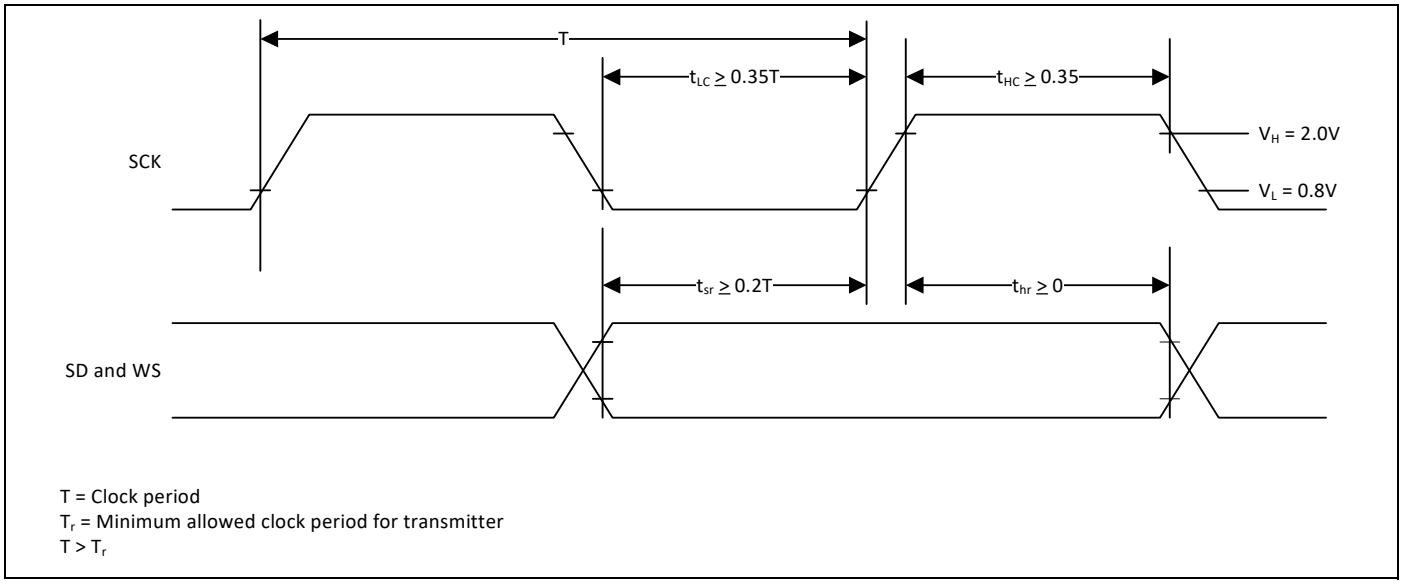
Note: The time periods specified in Figure 17 and Figure 18 are defined by the transmitter speed. The receiver specifications must match transmitter performance.

Figure 17. I²S Transmitter Timing



T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
T = T_{tr}
* t_{RC} is only relevant for transmitters in slave mode.

Figure 18. I²S Receiver Timing



T = Clock period
T_r = Minimum allowed clock period for transmitter
T > T_r

8. WLAN Global Functions

8.1 WLAN CPU and Memory Subsystem

The CYW43570 WLAN section includes an integrated ARM Cortex-R4 32-bit processor with internal RAM and ROM. The ARM Cortex-R4 is a low-power processor that features low gate count, low interrupt latency, and low-cost debug capabilities. It is intended for deeply embedded applications that require fast interrupt response features. Delivering more than 30% performance gain over ARM7TDMI, the ARM Cortex-R4 implements the ARM v7-R architecture with support for the Thumb-2 instruction set.

At 0.19 µW/MHz, the Cortex-R4 is the most power efficient general-purpose microprocessor available, outperforming 8- and 16-bit devices on MIPS/µW. It supports integrated sleep modes.

Using multiple technologies to reduce cost, the ARM Cortex-R4 offers improved memory utilization, reduced pin overhead, and reduced silicon area. It supports independent buses for Code and Data access (ICode/DCode and System buses), and extensive debug features including real time trace of program execution.

On-chip memory for the CPU includes 768 KB SRAM and 640 KB ROM.

8.2 One-Time Programmable Memory

Various hardware configuration parameters may be stored in an internal one-time programmable (OTP) memory, which is read by the system software after device reset. In addition, customer-specific parameters, including the system vendor ID and the MAC address can be stored, depending on the specific board design. Up to 484 bytes of user-accessible OTP are available.

The initial state of all bits in an unprogrammed OTP device is 0. After any bit is programmed to a 1, it cannot be reprogrammed to 0. The entire OTP array can be programmed in a single write cycle using a utility provided with the Cypress WLAN manufacturing test tools. Alternatively, multiple write cycles can be used to selectively program specific bytes, but only bits which are still in the 0 state can be altered during each programming cycle.

Prior to OTP programming, all values should be verified using the appropriate editable nvram.txt file, which is provided with the reference board design package.

8.3 GPIO Interface

The WLAN section of the CYW43570 supports 16 GPIOs.

Upon power up and reset, these pins become tristated. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. In addition, the GPIO pins can be assigned to various other functions.

Table 17. Strapping Options PCIe

<table>
<tr><th>PAD Names</th><th>FCBGA</th><th>Strapping Options</th><th>Default Chip Internal Pulls</th><th>Description</th></tr>
<tr><td>GPIO_0</td><td>Y</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>GPIO_1</td><td>Y</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>GPIO_2</td><td>Y</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>GPIO_3</td><td>Y</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>GPIO_4</td><td>Y</td><td>sprom_present/</td><td>0</td><td>1: SPROM is present
0: SPROM is absent (default is 0)
Applicable in PCIe host mode.</td></tr>
<tr><td>GPIO_5</td><td>Y</td><td>sflash_present</td><td>0</td><td>1: SFLASH is present
0: SFLASH is absent (default is 0)</td></tr>
<tr><td>GPIO_6</td><td>Y</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>GPIO_7</td><td>Y</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>GPIO_[8:10]</td><td>Y</td><td>strap_host_ifc_1</td><td>1</td><td>Together strap_host_ifc [3], [2], and [1] is used to select interfaces:
<table>
<tr><th>GPIO10</th><th>GPIO9</th><th>GPIO8</th><th>WLAN Host selected Bluetooth interprets</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>PCIe (default only for B0, B1, C0 PKG_OPT1/FCBGA-PCIe) BTUART or BTUSB (11D+11PHY) //BT tPorts stand alone.</td></tr>
</table></td></tr>
<tr><td>GPIO_11</td><td>Y</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>GPIO_12</td><td>Y</td><td>Default</td><td>0</td><td>Resource Mode Init in ALP clock mode only.</td></tr>
<tr><td>GPIO_13</td><td>Y</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>GPIO_14</td><td>Y</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>GPIO_15</td><td>Y</td><td>–</td><td>–</td><td>–</td></tr>
</table>

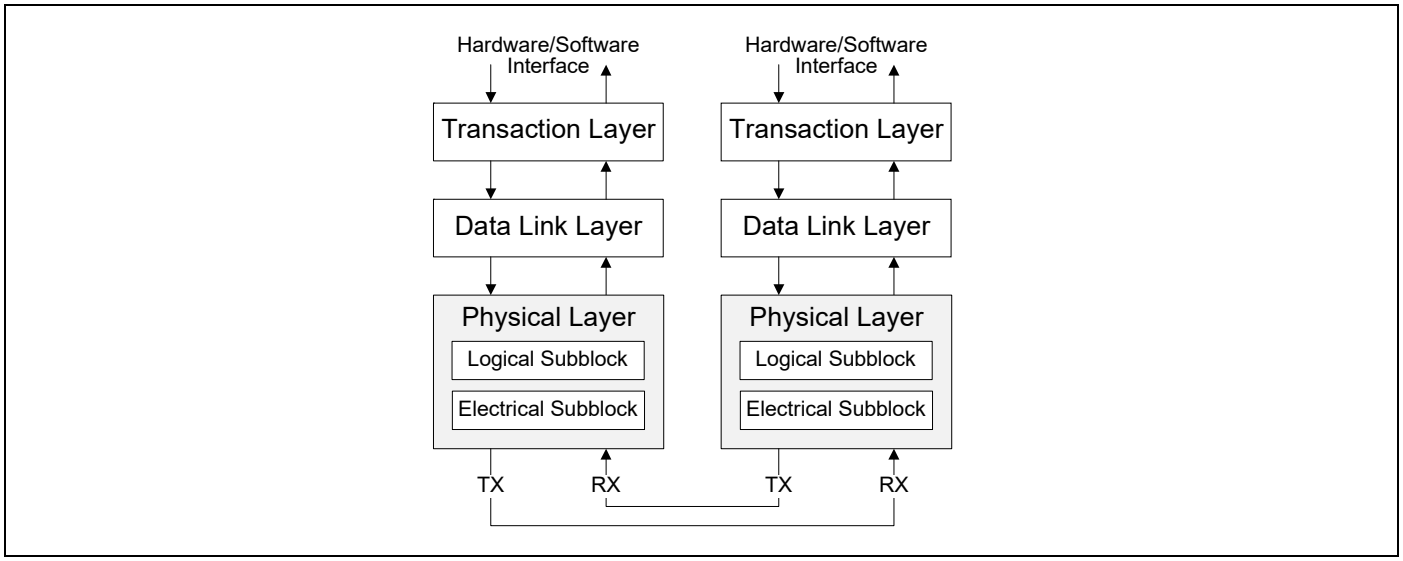
9. PCI Express Interface

The PCI Express (PCIe) core on the CYW43570 is a high-performance serial I/O interconnect that is protocol compliant and electrically compatible with the *PCI Express Base Specification v2.0*. This core contains all the necessary blocks, including logical and electrical functional subblocks to perform PCIe functionality and maintain high-speed links, using existing PCI system configuration software implementations without modification.

Organization of the PCIe core is in logical layers: Transaction Layer, Data Link Layer, and Physical Layer, as shown in Figure 19. A configuration or link management block is provided for enumerating the PCIe configuration space and supporting generation and reception of System Management Messages by communicating with PCIe layers.

Each layer is partitioned into dedicated transmit and receive units that allow point-to-point communication between the host and CYW43570 device. The transmit side processes outbound packets whereas the receive side processes inbound packets. Packets are formed and generated in the Transaction and Data Link Layer for transmission onto the high-speed links and onto the receiving device. A header is added at the beginning to indicate the packet type and any other optional fields.

Figure 19. PCI Express Layer Model



9.1 Transaction Layer Interface

The PCIe core employs a packet-based protocol to transfer data between the host and CYW43570 device, delivering new levels of performance and features. The upper layer of the PCIe is the Transaction Layer. The Transaction layer is primarily responsible for assembly and disassembly of transaction layer packets (TLPs). TLP structure contains header, data payload, and end-to-end CRC (ECRC) fields, which are used to communicate transactions, such as read and write requests and other events.

A pipelined full split-transaction protocol is implemented in this layer to maximize efficient communication between devices with credit-based flow control of TLP, which eliminates wasted link bandwidth due to retries.

9.2 Data Link Layer

The data link layer serves as an intermediate stage between the transaction layer and the physical layer. Its primary responsibility is to provide reliable, efficient mechanism for the exchange of TLPs between two directly connected components on the link. Services provided by the data link layer include data exchange, initialization, error detection and correction, and retry services.

The data link layer packets (DLLPs) are generated and consumed by the data link layer. DLLPs are the mechanism used to transfer link management information between data link layers of the two directly connected components on the link, including TLP acknowledgement, power management, and flow control.

9.3 Physical Layer

The physical layer of the PCIe provides a handshake mechanism between the data link layer and the high-speed signaling used for Link data interchange. This layer is divided into the logical and electrical functional subblocks. Both subblocks have dedicated transmit and receive units that allow for point-to-point communication between the host and CYW43570 device. The transmit section prepares outgoing information passed from the data link layer for transmission, and the receiver section identifies and prepares received information before passing it to the data link layer. This process involves link initialization, configuration, scrambler, and data conversion into a specific format.

9.4 Logical Subblock

The logical sub block primary functions are to prepare outgoing data from the data link layer for transmission and identify received data before passing it to the data link layer.

9.5 Scrambler/Descrambler

This PCIe PHY component generates pseudo-random sequence for scrambling of data bytes and the idle sequence. On the transmit side, scrambling is applied to characters prior to the 8b/10b encoding. On the receive side, descrambling is applied to characters after 8b/10b decoding. Scrambling may be disabled in polling and recovery for testing and debugging purposes.

9.6 8B/10B Encoder/Decoder

The PCIe core on the CYW43570 uses an 8b/10b encoder/decoder scheme to provide DC balancing, synchronizing clock and data recovery, and error detection. The transmission code is specified in the ANSI X3.230-1994, clause 11 and in IEEE 802.3z, 36.2.4.

Using this scheme, 8-bit data characters are treated as 3 bits and 5 bits mapped onto a 4-bit code group and a 6-bit code group, respectively. The control bit in conjunction with the data character is used to identify when to encode one of the twelve Special Symbols included in the 8b/10b transmission code. These code groups are concatenated to form a 10-bit symbol, which is then transmitted serially. Special Symbols are used for link management, frame TLPs, and DLLPs, allowing these packets to be quickly identified and easily distinguished.

9.7 Elastic FIFO

An elastic FIFO is implemented in the receiver side to compensate for the differences between the transmit clock domain and the receive clock domain, with worse case clock frequency specified at 600 ppm tolerance. As a result, the transmit and receive clocks can shift one clock every 1666 clocks. In addition, the FIFO adaptively adjusts the elastic level based on the relative frequency difference of the write and read clock. This technique reduces the elastic FIFO size and the average receiver latency by half.

9.8 Electrical Subblock

The high-speed signals utilize the common mode logic (CML) signaling interface with on-chip termination and de-emphasis for best-in-class signal integrity. A de-emphasis technique is employed to reduce the effects of intersymbol interference (ISI) due to the interconnect by optimizing voltage and timing margins for worst case channel loss. This results in a maximally open “eye” at the detection point, thereby allowing the receiver to receive data with acceptable bit-error rate (BER).

To further minimize ISI, multiple bits of the same polarity that are output in succession are de-emphasized. Subsequent same bits are reduced by a factor of 3.5 dB in power. This amount is specified by PCIe to allow for maximum interoperability while minimizing the complexity of controlling the de-emphasis values. The high-speed interface requires AC coupling on the transmit side to eliminate the DC common mode voltage from the receiver. The range of AC capacitance allowed is 75 nF to 200 nF.

9.9 Configuration Space

The PCIe function in the CYW43570 implements the configuration space as defined in the *PCI Express Base Specification v2.0*.

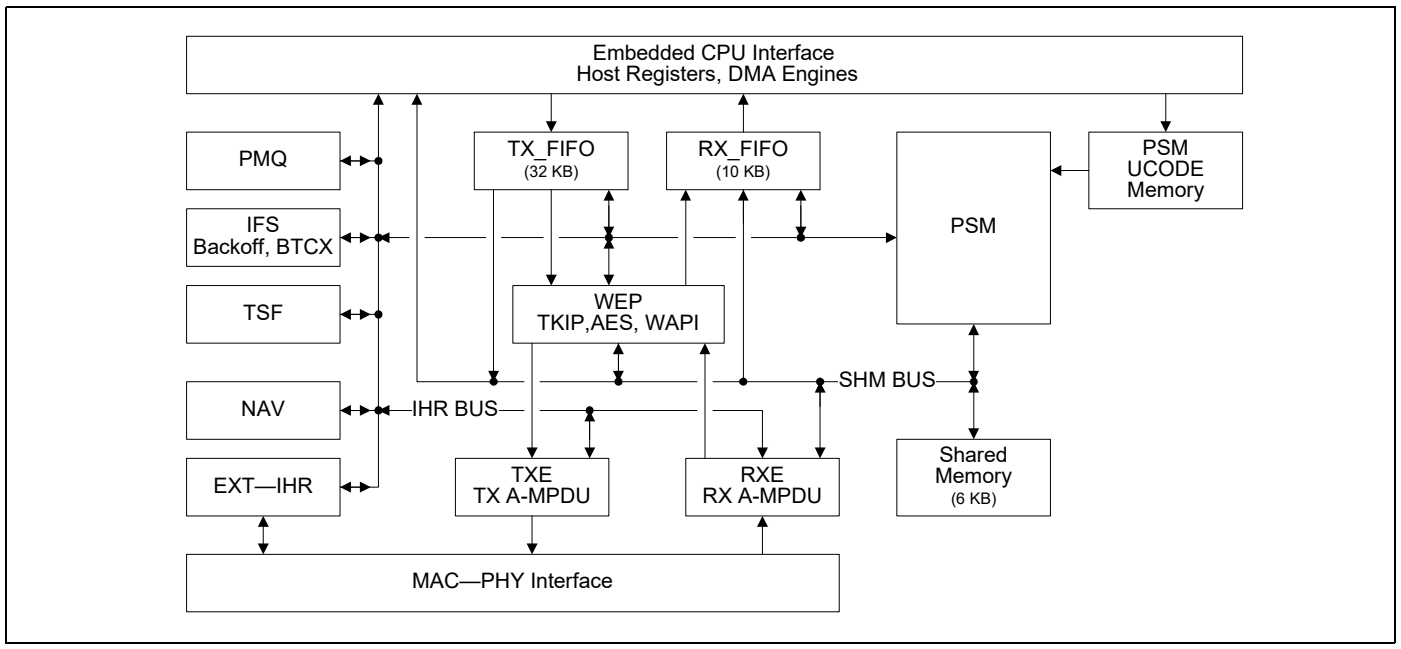
10. WLAN MAC and PHY

10.1 IEEE 802.11ac Draft MAC

The CYW43570 WLAN MAC is designed to support high-throughput operation with low-power consumption. It does so without compromising the Bluetooth coexistence policies, thereby enabling optimal performance over both networks. In addition, several power saving modes have been implemented that allow the MAC to consume very little power while maintaining network-wide timing synchronization. The architecture diagram of the MAC is shown in Figure 20.

The following sections provide an overview of the important modules in the MAC.

Figure 20. WLAN MAC Architecture



The CYW43570 WLAN media access controller (MAC) supports features specified in the IEEE 802.11 base standard, and amended by IEEE 802.11n. The key MAC features include:

- Enhanced MAC for supporting IEEE 802.11ac Draft features
- Transmission and reception of aggregated MPDUs (A-MPDU) for high throughput (HT)
- Support for power management schemes, including WMM power-save, power-save multi-poll (PSMP) and multiphase PSMP operation
- Support for immediate ACK and Block-ACK policies
- Interframe space timing support, including RIFS
- Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges
- Back-off counters in hardware for supporting multiple priorities as specified in the WMM specification
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware
- Hardware offload for AES-CCMP, legacy WPA TKIP, legacy WEP ciphers, WAPI, and support for key management
- Support for coexistence with Bluetooth and other external radios
- Programmable independent basic service set (IBSS) or infrastructure basic service set functionality
- Statistics counters for MIB support

10.1.1 PSM

The programmable state machine (PSM) is a micro-coded engine, which provides most of the low-level control to the hardware, to implement the IEEE 802.11 specification. It is a microcontroller that is highly optimized for flow control operations, which are predominant in implementations of communication protocols. The instruction set and fundamental operations are simple and general, which allows algorithms to be optimized until very late in the design process. It also allows for changes to the algorithms to track evolving IEEE 802.11 specifications.

The PSM fetches instructions from the microcode memory. It uses the shared memory to obtain operands for instructions, as a data store, and to exchange data between both the host and the MAC data pipeline (via the SHM bus). The PSM also uses a scratchpad memory (similar to a register bank) to store frequently accessed and temporary variables.

The PSM exercises fine-grained control over the hardware engines, by programming internal hardware registers (IHR). These IHRs are co-located with the hardware functions they control, and are accessed by the PSM via the IHR bus.

The PSM fetches instructions from the microcode memory using an address determined by the program counter, instruction literal, or a program stack. For ALU operations the operands are obtained from shared memory, scratchpad, IHRs, or instruction literals, and the results are written into the shared memory, scratchpad, or IHRs.

There are two basic branch instructions: conditional branches and ALU based branches. To better support the many decision points in the IEEE 802.11 algorithms, branches can depend on either a readily available signals from the hardware modules (branch condition signals are available to the PSM without polling the IHRs), or on the results of ALU operations.

10.1.2 WEP

The wired equivalent privacy (WEP) engine encapsulates all the hardware accelerators to perform the encryption and decryption, and MIC computation and verification. The accelerators implement the following cipher algorithms: legacy WEP, WPA TKIP, WPA2 AES-CCMP.

The PSM determines, based on the frame type and association information, the appropriate cipher algorithm to be used. It supplies the keys to the hardware engines from an on-chip key table. The WEP interfaces with the TXE to encrypt and compute the MIC on transmit frames, and the RXE to decrypt and verify the MIC on receive frames.

10.1.3 TXE

The transmit engine (TXE) constitutes the transmit data path of the MAC. It coordinates the DMA engines to store the transmit frames in the TXFIFO. It interfaces with WEP module to encrypt frames, and transfers the frames across the MAC-PHY interface at the appropriate time determined by the channel access mechanisms.

The data received from the DMA engines are stored in transmit FIFOs. The MAC supports multiple logical queues to support traffic streams that have different QoS priority requirements. The PSM uses the channel access information from the IFS module to schedule a queue from which the next frame is transmitted. Once the frame is scheduled, the TXE hardware transmits the frame based on a precise timing trigger received from the IFS module.

The TXE module also contains the hardware that allows the rapid assembly of MPDUs into an A-MPDU for transmission. The hardware module aggregates the encrypted MPDUs by adding appropriate headers and pad delimiters as needed.

10.1.4 RXE

The receive engine (RXE) constitutes the receive data path of the MAC. It interfaces with the DMA engine to drain the received frames from the RXFIFO. It transfers bytes across the MAC-PHY interface and interfaces with the WEP module to decrypt frames. The decrypted data is stored in the RXFIFO.

The RXE module contains programmable filters that are programmed by the PSM to accept or filter frames based on several criteria such as receiver address, BSSID, and certain frame types.

The RXE module also contains the hardware required to detect A-MPDUs, parse the headers of the containers, and disaggregate them into component MPDUS.

10.1.5 IFS

The IFS module contains the timers required to determine interframe space timing including RIFS timing. It also contains multiple backoff engines required to support prioritized access to the medium as specified by WMM.

The interframe spacing timers are triggered by the cessation of channel activity on the medium, as indicated by the PHY. These timers provide precise timing to the TXE to begin frame transmission. The TXE uses this information to send response frames or perform transmit frame-bursting (RIFS or SIFS separated, as within a TXOP).

The backoff engines (for each access category) monitor channel activity, in each slot duration, to determine whether to continue or pause the backoff counters. When the backoff counters reach 0, the TXE gets notified, so that it may commence frame transmission. In the event of multiple backoff counters decrementing to 0 at the same time, the hardware resolves the conflict based on policies provided by the PSM.

The IFS module also incorporates hardware that allows the MAC to enter a low-power state when operating under the IEEE power save mode. In this mode, the MAC is in a suspended state with its clock turned off. A sleep timer, whose count value is initialized by the PSM, runs on a slow clock and determines the duration over which the MAC remains in this suspended state. Once the timer expires the MAC is restored to its functional state. The PSM updates the TSF timer based on the sleep duration ensuring that the TSF is synchronized to the network. The IFS module also contains the PTA hardware that assists the PSM in Bluetooth coexistence functions.

10.1.6 TSF

The timing synchronization function (TSF) module maintains the TSF timer of the MAC. It also maintains the target beacon transmission time (TBTT). The TSF timer hardware, under the control of the PSM, is capable of adopting timestamps received from beacon and probe response frames in order to maintain synchronization with the network.

The TSF module also generates trigger signals for events that are specified as offsets from the TSF timer, such as uplink and downlink transmission times used in PSMP.

10.1.7 NAV

The network allocation vector (NAV) timer module is responsible for maintaining the NAV information conveyed through the duration field of MAC frames. This ensures that the MAC complies with the protection mechanisms specified in the standard.

The hardware, under the control of the PSM, maintains the NAV timer and updates the timer appropriately based on received frames. This timing information is provided to the IFS module, which uses it as a virtual carrier-sense indication.

10.1.8 MAC-PHY Interface

The MAC-PHY interface consists of a data path interface to exchange RX/TX data from/to the PHY. In addition, there is an programming interface, which can be controlled either by the host or the PSM to configure and control the PHY.

10.2 IEEE 802.11ac Draft PHY

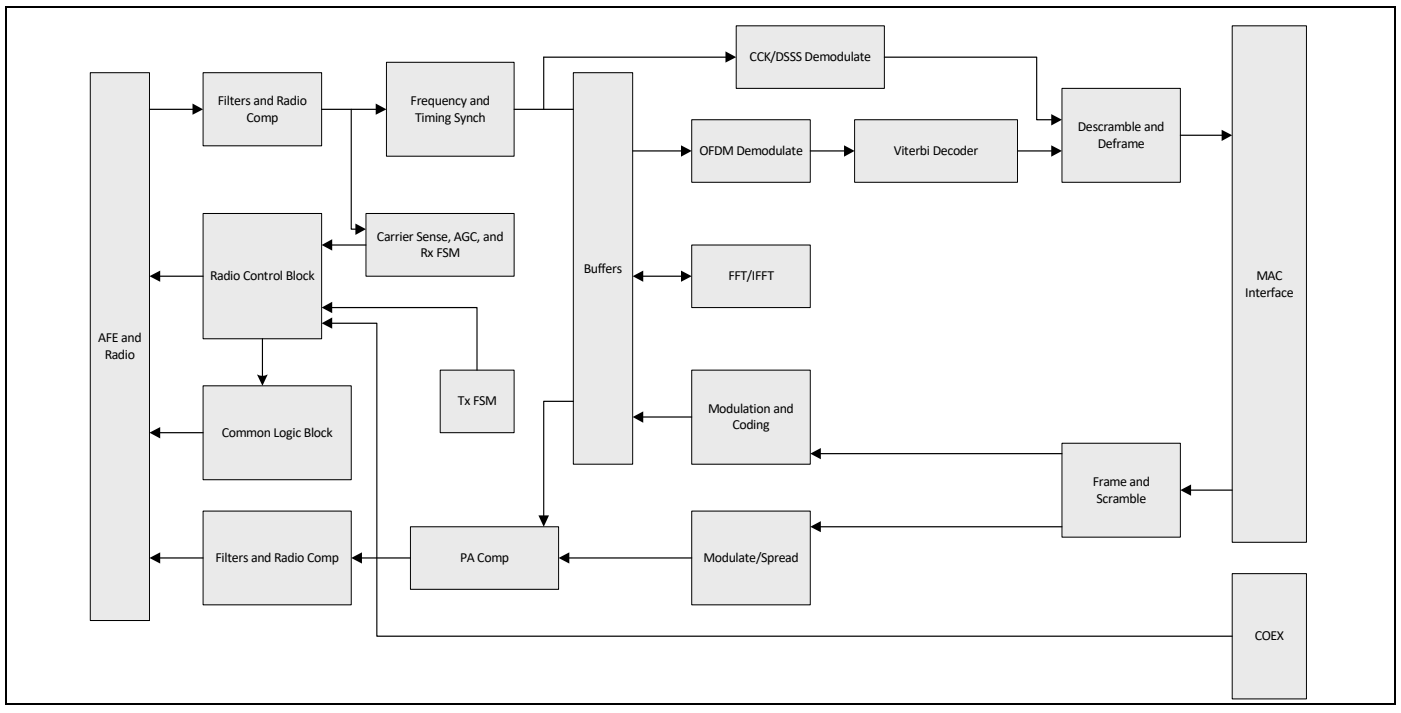
The CYW43570 WLAN Digital PHY is designed to comply with IEEE 802.11ac Draft and IEEE 802.11a/b/g/n dual-stream specifications to provide wireless LAN connectivity supporting data rates from 1 Mbps to 866.7 Mbps for low-power, high-performance handheld applications.

The PHY has been designed to work in the presence of interference, radio nonlinearity, and various other impairments. It incorporates optimized implementations of the filters, FFT and Viterbi decoder algorithms. Efficient algorithms have been designed to achieve maximum throughput and reliability, including algorithms for carrier sense/rejection, frequency/phase/timing acquisition and tracking, channel estimation and tracking. The PHY receiver also contains a robust IEEE 802.11b demodulator. The PHY carrier sense has been tuned to provide high throughput for IEEE 802.11g/11b hybrid networks with Bluetooth coexistence.

The key PHY features include:

- Programmable data rates from MCS0–15 in 20 MHz, 40 MHz, and 80 MHz channels, as specified in IEEE 802.11ac Draft
- Supports Optional Short GI and Green Field modes in Tx and Rx
- Tx and Rx LDPC for improved range and power efficiency
- Beamforming support
- All scrambling, encoding, forward error correction, and modulation in the transmit direction and inverse operations in the receive direction.
- Supports IEEE 802.11h/k for worldwide operation
- Advanced algorithms for low power, enhanced sensitivity, range, and reliability
- Algorithms to improve performance in presence of Bluetooth
- Closed loop transmit power control
- Digital RF chip calibration algorithms to handle CMOS RF chip non-idealities
- On-the-fly channel frequency and transmit power selection
- Supports per packet Rx antenna diversity
- Available per-packet channel quality and signal strength measurements
- Designed to meet FCC and other worldwide regulatory requirements

Figure 21. WLAN PHY Block Diagram



11. WLAN Radio Subsystem

The CYW43570 includes an integrated dual-band WLAN RF transceiver that has been optimized for use in 2.4 GHz and 5 GHz Wireless LAN systems. It has been designed to provide low-power, low-cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM or 5 GHz U-NII bands. The transmit and receive sections include all on-chip filtering, mixing, and gain control functions.

Sixteen RF control signals are available (eight per core) to drive external RF switches and support optional external power amplifiers and low-noise amplifiers for each band. See the reference board schematics for further details.

11.1 Receiver Path

The CYW43570 has a wide dynamic range, direct conversion receiver that employs high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band or the entire 5 GHz U-NII band. Control signals are available that can support the use of optional LNAs for each band, which can increase the receive sensitivity by several decibels.

11.2 Transmitter Path

Baseband data is modulated and upconverted to the 2.4 GHz ISM or 5-GHz U-NII bands, respectively. Linear on-chip power amplifiers are included, which are capable of delivering high output powers while meeting IEEE 802.11ac and IEEE 802.11a/b/g/n specifications without the need for external PAs. When using the internal PAs, closed-loop output power control is completely integrated.

11.3 Calibration

The CYW43570 features dynamic and automatic on-chip calibration to continually compensate for temperature and process variations across components. These calibration routines are performed periodically in the course of normal radio operation. Examples of some of the automatic calibration algorithms are baseband filter calibration for optimum transmit and receive performance, and LOFT calibration for carrier leakage reduction. In addition, I/Q Calibration, R Calibration, and VCO Calibration are performed on-chip. No per-board calibration is required in manufacturing test, which helps to minimize the test time and cost in large volume production.

12. Pin Diagram and Signal Descriptions

12.1 Ball Maps

Figure 22 and Figure 23 show the FCBGA ball map.

Figure 22. FCBGA Ball Map, 10 mm × 10 mm Array, 242 Balls (Top View, 1 of 2)

	1	2	3	4	5	6	7	8	9	10	11	12
A	VSSC	GPIO_5		PCIE_TESTP	PCIE_TESTN	PCIE_RXTX_AVDD1P2	PCIE_RDP0	PCIE_RDN0	PCIE_TDP0	PCIE_TDN0	PCIE_REFCLKP	PCIE_REFCLKN
B	BT_USB_DN	VSSC	GPIO_6	GPIO_2					PCIE_AVSS			PCIE_AVSS
C	BT_USB_DP	BT_SF_CLK										
D		BT_SF_CS_L										
E	BT_UART_RXD	BT_UART_CTS_L			BT_I2S_WS	OTP_VDD33	LPO_IN				VSSC	VSSC
F		BT_UART_TXD			BT_SF_MISO							
G	BT_I2S_CLK	GPIO_4			BT_GPIO_4							
H					BT_SF_MOSI			BT_I2S_DO		BT_I2S_DI		VSSC
J	BT_DEV_WAKE	BT_HOST_WAKE			BT_CLK_REQ							VSSC
K	BT_IFVDD1P2	BT_VCOVDD1P2			BTRGND			BTRGND		AVDD_BBPLL		VDDC
L	BT_LNAVDD1P2	BT_PLLVDD1P2						BTRGND	AVSS_BBPLL		VDDC	
M		BTRGND			BTRGND			BT_VDDO		BT_VDDC		
N	BT_RF				BTRGND			BTRGND		BT_VDDC		
P	BT_PAVDD2P5				BTRGND			BTRGND		BTRGND	VDDC	VDDC
R	BTRGND	BTRGND			BTRGND		BTRGND		BTRGND		VSSC	VSSC
T	WRF_RFIN_2G_CORE0	RGND			RGND		RGND			RGND		
U	RGND	RGND			RGND							
V	WRF_RFOUT_2G_CORE0	RGND			RGND	RGND	RGND	RGND	RGND			
W	RGND				RGND	RGND	WRF_TSSI_A_CORE0	RGND	WRF_GPIO_OUT_CORE0	WRF_PFD_GND1P2	WRF_CP_GND1P2	WRF_MMD_GND1P2
Y	WRF_PA2G_VBAT_VDD3P3_CORE0	RGND										
AA	WRF_PADRV_VBAT_VDD3P3_CORE0	RGND										
AB	WRF_PA5G_VBAT_VDD3P3_CORE0	RGND		RGND	RGND		RGND	RGND	RGND	RGND	RGND	
AC	RGND	WRF_RFOUT_5G_CORE0	RGND	WRF_RFIN_5G_CORE0	RGND	WRF_BUCK_VDD1P5_CORE0	WRF_PFD_VDD1P2	WRF_MMD_VDD1P2	WRF_SYNTH_VBAT_VDD3P3	RGND	WRF_RFIN_2G_CORE1	RGND
	1	2	3	4	5	6	7	8	9	10	11	12

Figure 23. FCBGA Ball Map, 10 mm × 10 mm Array, 242 Balls (Top View, 2 of 2)

12	13	14	15	16	17	18	19	20	21	22	23	
PCIE_REFCLKN	PCIE_PLL_AVDD1P2	PCIE_PERST_L	BT_UART_RTS_L	GPIO_1				SR_VLX	SR_VLX	SR_PVSS	SR_PVSS	A
PCIE_AVSS		PCIE_CLKREQ_L		PCIE_PME_L	GPIO_0						SR_VDDBATA5V	B
										SR_VDDBATP5V	SR_VDDBATP5V	C
										LDO_VDD1P5	LDO_VDD1P5	D
VSSC	JTAG_SEL	GPIO_3		VSSC	PMU_AVSS	WL_REG_ON				VOUT_LDO3P3_B	VOUT_LDO3P3_B	E
							VOUT_3P3_SENSE			VOUT_3P3	VOUT_3P3	F
										LDO_VDDBAT5V	LDO_VDDBAT5V	G
VSSC	VSSC		BT_REG_ON	VSSC			GPIO_15			GPIO_14	VOUT_CLDO	H
VSSC		VSSC		VDDIO_PMU			GPIO_12			GPIO_13	VOUT_BTLDO2P5	J
VDDC		VDDC		VDDIO			GPIO_9	GPIO_11		GPIO_10	VOUT_LNLDO	K
		VDDC	VDDC	VDDIO_RF			RF_SW_CTRL_15			GPIO_7	GPIO_8	L
							RF_SW_CTRL_13			RF_SW_CTRL_14	RF_SW_CTRL_12	M
			VDDC				RF_SW_CTRL_6			RF_SW_CTRL_11	RF_SW_CTRL_9	N
VDDC		VDDC	VDDC	VSSC			RF_SW_CTRL_7			RF_SW_CTRL_10		P
VSSC	VSSC	VSSC	VSSC	VSSC	VSSC		RF_SW_CTRL_5			RF_SW_CTRL_8	RF_SW_CTRL_4	R
	VSSC		VSSC	VSSC			RF_SW_CTRL_3					T
	RGND			RGND	RGND		RF_SW_CTRL_0			WRF_XTAL_GND1P2	WRF_XTAL_OUT	U
	WRF_LOGENG_GND1P2			RGND	RGND	RGND	RF_SW_CTRL_2			WRF_XTAL_GND1P2	WRF_XTAL_IN	V
WRF_MMD_GND1P2	WRF_VCO_GND1P2	WRF_GPIO_OUT_CORE1	RGND	WRF_TSSI_A_CORE1	RGND	RGND	RF_SW_CTRL_1			WRF_XTAL_GND1P2	WRF_XTAL_VDD1P2	W
										WRF_XTAL_GND1P2	WRF_XTAL_VDD1P5	Y
										RGND	WRF_BUCK_VDD1P5_CORE1	AA
	RGND		RGND	RGND		RGND	RGND	RGND	RGND	RGND	RGND	AB
RGND	WRF_RFOUT_2G_CORE1	RGND	WRF_PA2G_VBAT_VDD3P3_CORE1	WRF_PADRV_VBAT_VDD3P3_CORE1	WRF_PA5G_VBAT_VDD3P3_CORE1	RGND	RGND	WRF_RFOUT_5G_CORE1	RGND	WRF_RFIN_5G_CORE1	RGND	AC
12	13	14	15	16	17	18	19	20	21	22	23	

12.2 Pin List

Table 18. Pin List

Ball	PKG Net Name
A1	VSSC
A2	GPIO_5
A4	PCIE_TESTP
A5	PCIE_TESTN
A6	PCIE_RXTX_AVDD1P2
A7	PCIE_RDP0
A8	PCIE_RDN0
A9	PCIE_TDP0
A10	PCIE_TDN0
A11	PCIE_REFCLKP
A12	PCIE_REFCLKN
A13	PCIE_PLL_AVDD1P2
A14	PCIE_PERST_L
A15	BT_UART_RTS_L
A16	GPIO_1
A20	SR_VLX
A21	SR_VLX
A22	SR_PVSS
A23	SR_PVSS
B1	BT_USB_DN
B2	VSSC
B3	GPIO_6
B4	GPIO_2
B9	PCIE_AVSS
B12	PCIE_AVSS
B14	PCIE_CLKREQ_L
B16	PCIE_PME_L
B17	GPIO_0
B23	SR_VDDBATA5V
C1	BT_USB_DP
C2	BT_SF_CLK
C22	SR_VDDBATP5V
C23	SR_VDDBATP5V
D2	BT_SF_CS_L
D22	LDO_VDD1P5
D23	LDO_VDD1P5
E1	BT_UART_RXD
E2	BT_UART_CTS_L
E5	BT_I2S_WS
E6	OTP_VDD33
E7	LPO_IN
E11	VSSC

Table 18. Pin List (Cont.)

Ball	PKG Net Name
E12	VSSC
E13	JTAG_SEL
E14	GPIO_3
E16	VSSC
E17	PMU_AVSS
E18	WL_REG_ON
E22	VOUT_LDO3P3_B
E23	VOUT_LDO3P3_B
F2	BT_UART_TXD
F5	BT_SF_MISO
F19	VOUT_3P3_SENSE
F22	VOUT_3P3
F23	VOUT_3P3
G1	BT_I2S_CLK
G2	GPIO_4
G5	BT_GPIO_4
G22	LDO_VDDBAT5V
G23	LDO_VDDBAT5V
H5	BT_SF_MOSI
H8	BT_I2S_DO
H10	BT_I2S_DI
H12	VSSC
H13	VSSC
H15	BT_REG_ON
H16	VSSC
H19	GPIO_15
H22	GPIO_14
H23	VOUT_CLDO
J1	BT_DEV_WAKE
J2	BT_HOST_WAKE
J5	BT_CLK_REQ
J12	VSSC
J14	VSSC
J16	VDDIO_PMU
J19	GPIO_12
J22	GPIO_13
J23	VOUT_BTLDO2P5
K1	BT_IFVDD1P2
K2	BT_VCOVDD1P2
K5	BTRGND
K8	BTRGND
K10	AVDD_BBPLL

Table 18. Pin List (Cont.)

Ball	PKG Net Name
K12	VDDC
K14	VDDC
K16	VDDIO
K19	GPIO_9
K20	GPIO_11
K22	GPIO_10
K23	VOUT_LNLDO
L1	BT_LNAVDD1P2
L2	BT_PLLVDD1P2
L8	BTRGND
L9	AVSS_BBPLL
L11	VDDC
L14	VDDC
L15	VDDC
L16	VDDIO_RF
L19	RF_SW_CTRL_15
L22	GPIO_7
L23	GPIO_8
M2	BTRGND
M5	BTRGND
M8	BT_VDDO
M10	BT_VDDC
M19	RF_SW_CTRL_13
M22	RF_SW_CTRL_14
M23	RF_SW_CTRL_12
N1	BT_RF
N5	BTRGND
N8	BTRGND
N10	BT_VDDC
N15	VDDC
N19	RF_SW_CTRL_6
N22	RF_SW_CTRL_11
N23	RF_SW_CTRL_9
P1	BT_PAVDD2P5
P5	BTRGND
P8	BTRGND
P10	BTRGND
P11	VDDC
P12	VDDC
P14	VDDC
P15	VDDC
P16	VSSC

Table 18. Pin List (Cont.)

Ball	PKG Net Name
P19	RF_SW_CTRL_7
P22	RF_SW_CTRL_10
R1	BTRGND
R2	BTRGND
R5	BTRGND
R7	BTRGND
R9	BTRGND
R11	VSSC
R12	VSSC
R13	VSSC
R14	VSSC
R15	VSSC
R16	VSSC
R17	VSSC
R19	RF_SW_CTRL_5
R22	RF_SW_CTRL_8
R23	RF_SW_CTRL_4
T1	WRF_RFIN_2G_CORE0
T2	RGND
T5	RGND
T7	RGND
T10	RGND
T13	VSSC
T15	VSSC
T16	VSSC
T19	RF_SW_CTRL_3
U1	RGND
U2	RGND
U5	RGND
U13	RGND
U16	RGND
U17	RGND
U19	RF_SW_CTRL_0
U22	WRF_XTAL_GND1P2
U23	WRF_XTAL_OUT
V1	WRF_RFOUT_2G_CORE0
V2	RGND
V5	RGND
V6	RGND
V7	RGND
V8	RGND
V9	RGND

Table 18. Pin List (Cont.)

Ball	PKG Net Name
V13	WRF_LOGENG_GND1P2
V16	RGND
V17	RGND
V18	RGND
V19	RF_SW_CTRL_2
V22	WRF_XTAL_GND1P2
V23	WRF_XTAL_IN
W1	RGND
W5	RGND
W6	RGND
W7	WRF_TSSI_A_CORE0
W8	RGND
W9	WRF_GPIO_OUT_CORE0
W10	WRF_PFD_GND1P2
W11	WRF_CP_GND1P2
W12	WRF_MMD_GND1P2
W13	WRF_VCO_GND1P2
W14	WRF_GPIO_OUT_CORE1
W15	RGND
W16	WRF_TSSI_A_CORE1
W17	RGND
W18	RGND
W19	RF_SW_CTRL_1
W22	WRF_XTAL_GND1P2
W23	WRF_XTAL_VDD1P2
Y1	WRF_PA2G_VBAT_VDD3P3_CORE0
Y2	RGND
Y22	WRF_XTAL_GND1P2
Y23	WRF_XTAL_VDD1P5
AA1	WRF_PADRV_VBAT_VDD3P3_CORE0
AA2	RGND
AA22	RGND
AA23	WRF_BUCK_VDD1P5_CORE1
AB1	WRF_PA5G_VBAT_VDD3P3_CORE0
AB2	RGND
AB4	RGND
AB5	RGND
AB7	RGND
AB8	RGND
AB9	RGND
AB10	RGND
AB11	RGND

Table 18. Pin List (Cont.)

Ball	PKG Net Name
AB13	RGND
AB15	RGND
AB16	RGND
AB18	RGND
AB19	RGND
AB20	RGND
AB21	RGND
AB22	RGND
AB23	RGND
AC1	RGND
AC2	WRF_RFOUT_5G_CORE0
AC3	RGND
AC4	WRF_RFIN_5G_CORE0
AC5	RGND
AC6	WRF_BUCK_VDD1P5_CORE0
AC7	WRF_PFD_VDD1P2
AC8	WRF_MMD_VDD1P2
AC9	WRF_SYNTH_VBAT_VDD3P3
AC10	RGND
AC11	WRF_RFIN_2G_CORE1
AC12	RGND
AC13	WRF_RFOUT_2G_CORE1
AC14	RGND
AC15	WRF_PA2G_VBAT_VDD3P3_CORE1
AC16	WRF_PADRV_VBAT_VDD3P3_CORE1
AC17	WRF_PA5G_VBAT_VDD3P3_CORE1
AC18	RGND
AC19	RGND
AC20	WRF_RFOUT_5G_CORE1
AC21	RGND
AC22	WRF_RFIN_5G_CORE1
AC23	RGND

12.3 Signal Descriptions

The signal name, type, and description of each pin in the CYW43570 is listed in Table 19. The symbols shown under Type indicate pin directions (I/O = bidirectional, I = input, O = output) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any.

Table 19. Signal Descriptions

Ball	Signal Name	Type	Description
WLAN Receive RF Signal Interface			
T1	WRF_RFIN_2G_CORE0	I	2.4 GHz WLAN CORE0 receiver input.
AC11	WRF_RFIN_2G_CORE1	I	2.4 GHz WLAN CORE1 receiver input.
AC4	WRF_RFIN_5G_CORE0	I	5 GHz WLAN CORE0 receiver input.
AC22	WRF_RFIN_5G_CORE1	I	5 GHz WLAN CORE1 receiver input.
V1	WRF_RFOUT_2G_CORE0	O	2.4 GHz WLAN CORE0 PA output.
AC13	WRF_RFOUT_2G_CORE1	O	2.4 GHz WLAN CORE1 PA output.
AC2	WRF_RFOUT_5G_CORE0	O	5 GHz WLAN CORE0 PA output.
AC20	WRF_RFOUT_5G_CORE1	O	5 GHz WLAN CORE1 PA output.
W7	WRF_TSSI_A_CORE0	I	5 GHz TSSI CORE0 input from an optional external power amplifier/power detector.
W16	WRF_TSSI_A_CORE1	I	5 GHz TSSI CORE1 input from an optional external power amplifier/power detector.
W9	WRF_GPIO_OUT_CORE0	I/O	GPIO or 2.4 GHz TSSI CORE0 input from an optional external power amplifier/power detector.
W14	WRF_GPIO_OUT_CORE1	I/O	GPIO or 2.4 GHz TSSI CORE1 input from an optional external power amplifier/power detector.
RF Switch Control Lines			
U19	RF_SW_CTRL_0	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
W19	RF_SW_CTRL_1	O	
V19	RF_SW_CTRL_2	O	
T19	RF_SW_CTRL_3	O	
R23	RF_SW_CTRL_4	O	
R19	RF_SW_CTRL_5	O	
N19	RF_SW_CTRL_6	O	
P19	RF_SW_CTRL_7	O	
R22	RF_SW_CTRL_8	O	
N23	RF_SW_CTRL_9	O	
P22	RF_SW_CTRL_10	O	
N22	RF_SW_CTRL_11	O	
M23	RF_SW_CTRL_12	O	
M19	RF_SW_CTRL_13	O	
M22	RF_SW_CTRL_14	O	
L19	RF_SW_CTRL_15	O	
PCIe Interface			
A11	PCIE_REFCLKP	I/O	100Ω diff pair clock signal positive.
A12	PCIE_REFCLKN	I/O	100Ω diff pair clock signal negative.
A10	PCIE_TDN0	I/O	100Ω diff pair Tx data signal negative.
A9	PCIE_TDP0	I/O	100Ω diff pair Tx data signal positive.
A7	PCIE_RDP0	I/O	100Ω diff pair Rx data signal positive.

Table 19. Signal Descriptions (Cont.)

Ball	Signal Name	Type	Description
A8	PCIE_RDN0	I/O	100Ω diff pair Rx data signal negative.
B14	PCIE_CLKREQ_L	I/O	PCIE clock request signal.
A14	PCIE_PERST_L	I/O	PCIE preset signal.
A4	PCIE_TESTP	I/O	100Ω diff pair.
A5	PCIE_TESTN	I/O	100Ω diff pair.
WLAN GPIO Interface **Note:** The GPIO signals can be multiplexed via software and the JTAG_SEL pin to support other functions. See Table 17 for additional details.			
B17	GPIO_0	I/O	Programmable GPIO pins.
A16	GPIO_1	I/O	
B4	GPIO_2	I/O	
E14	GPIO_3	I/O	
G2	GPIO_4	I/O	
A2	GPIO_5	I/O	
B3	GPIO_6	I/O	
L22	GPIO_7	I/O	
L23	GPIO_8	I/O	
K19	GPIO_9	I/O	
K22	GPIO_10	I/O	
K20	GPIO_11	I/O	
J19	GPIO_12	I/O	
J22	GPIO_13	I/O	
H22	GPIO_14	I/O	
H19	GPIO_15	I/O	
JTAG Interface			
E13	JTAG_SEL	I/O	JTAG select. This pin must be connected to ground if the JTAG interface is not used.
Clocks			
E7	LPO_IN	I	External sleep clock input (32.768 kHz).
J5	BT_CLK_REQ	O	Asserts when WLAN wants the host to turn on the reference clock.
U23	WRF_XTAL_OUT	O	XTAL oscillator output.
V23	WRF_XTAL_IN	I	XTAL oscillator input.
Bluetooth Transceiver			
N1	BT_RF	O	Bluetooth RF input/output.
C2	BT_SF_CLK	I	SFLASH_CLK.
D2	BT_SF_CS_L	I/O	SFLASH_CSN.
F5	BT_SF_MISO	I/O	SFLASH master input, slave output.
H5	BT_SF_MOSI	I/O	SFLASH master output, slave input.
Bluetooth USB Interface			
B1	BT_USB_DN	I/O	USB (Host) data negative. Negative terminal of the USB transceiver.
C1	BT_USB_DP	I/O	USB (Host) data positive. Positive terminal of the USB transceiver.

Table 19. Signal Descriptions (Cont.)

Ball	Signal Name	Type	Description
Bluetooth UART			
E2	BT_UART_CTS_L	I	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.
A15	BT_UART_RTS_L	O	UART request-to-send. Active-low request-to-send signal for the HCI UART interface. BT LED control pin.
E1	BT_UART_RXD	I	UART serial input. Serial data input for the HCI UART interface.
F2	BT_UART_TXD	O	UART serial output. Serial data output for the HCI UART interface.
Bluetooth I^2S			
G1	BT_I2S_CLK	I/O	I^2S clock, can be master (output) or slave (input).
H8	BT_I2S_DO	I/O	I^2S data output.
H10	BT_I2S_DI	I/O	I^2S data input.
E5	BT_I2S_WS	I/O	I^2S WS; can be master (output) or slave (input).
Bluetooth GPIO			
G5	BT_GPIO_4	I/O	Bluetooth general-purpose I/O.
Miscellaneous			
E18	WL_REG_ON	I	Used by PMU to power up or power down the internal CYW43570 regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
H15	BT_REG_ON	I	Used by PMU to power up or power down the internal CYW43570 regulators used by the Bluetooth section. Also, when deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
J1	BT_DEV_WAKE	I/O	Bluetooth DEV_WAKE.
J2	BT_HOST_WAKE	I/O	Bluetooth HOST_WAKE.
Integrated Voltage Regulators			
B23	SR_VDDBATA5V	I	Quiet VBAT.
C22, C23	SR_VDDBATP5V	I	Power VBAT.
A20, A21	SR_VLX	O	CBUCK switching regulator output. Refer to Table 33 on page 74 for details of the inductor and capacitor required on this output.
D22, D23	LDO_VDD1P5	I	LNLDO input.
G22, G23	LDO_VDDBAT5V	I	LDO VBAT.
Y23	WRF_XTAL_VDD1P5	I	XTAL LDO input (1.35V).
W23	WRF_XTAL_VDD1P2	O	XTAL LDO output (1.2V).
K23	VOUT_LNLDO	O	Output of LNLDO.
H23	VOUT_CLDO	O	Output of core LDO.
J23	VOUT_LDO2P5	O	2.5V LDO. Connects to a 2.2 µF bypass capacitor to GND.
E22, E23	VOUT_LDO3P3_B	O	3.3V LDO.
F22, F23	VOUT_3P3	O	LDO 3.3V output.
F19	VOUT_3P3_SENSE	O	Voltage sense pin for LDO 3.3V output.
Bluetooth Supplies			
P1	BT_PAVDD2P5	PWR	Bluetooth PA power supply.
L1	BT_LNAVDD1P2	PWR	Bluetooth LNA power supply.

Table 19. Signal Descriptions (Cont.)

Ball	Signal Name	Type	Description
K1	BT_IFVDD1P2	PWR	Bluetooth IF block power supply.
L2	BT_PLLVDD1P2	PWR	Bluetooth RF PLL power supply.
K2	BT_VCOVDD1P2	PWR	Bluetooth RF power supply.
M8	BT_VDDO	PWR	Core supply.
M10, N10	BT_VDDC	PWR	1.2V core supply for BT.
WLAN Supplies			
AC6	WRF_BUCK_VDD1P5_CORE0	PWR	Internal capacitor-less CORE0 LDO supply.
AA23	WRF_BUCK_VDD1P5_CORE1	PWR	Internal capacitor-less CORE1 LDO supply.
AC9	WRF_SYNTH_VBAT_VDD3P3	PWR	Synth VDD 3.3V supply.
AA1	WRF_PADRV_VBAT_VDD3P3_CORE0	PWR	CORE0 PA Driver VBAT supply.
AC16	WRF_PADRV_VBAT_VDD3P3_CORE1	PWR	CORE1 PA Driver VBAT supply.
AB1	WRF_PA5G_VBAT_VDD3P3_CORE0	PWR	5 GHz CORE0 PA 3.3V VBAT supply.
AC17	WRF_PA5G_VBAT_VDD3P3_CORE1	PWR	5 GHz CORE1 PA 3.3V VBAT supply.
Y1	WRF_PA2G_VBAT_VDD3P3_CORE0	PWR	2 GHz CORE0 PA 3.3V VBAT supply.
AC15	WRF_PA2G_VBAT_VDD3P3_CORE1	PWR	2 GHz CORE1 PA 3.3V VBAT supply.
AC8	WRF_MMD_VDD1P2	PWR	1.2V supply.
AC7	WRF_PFD_VDD1P2	PWR	1.2V supply.
Miscellaneous Supplies			
E6	OTP_VDD33	PWR	OTP 3.3V supply.
K12, K14, L11, L14, L15, N15, P11, P12, P14, P15	VDDC	PWR	1.2V core supply for WLAN.
K16	VDDIO	PWR	1.8V–3.3V supply for WLAN. Must be directly connected to PMU_VDDIO on the PCB.
M10, N10	BT_VDDC	PWR	1.2V core supply for BT.
K10	AVDD_BBPLL	PWR	Baseband PLL supply
J16	VDDIO_PMU	PWR	1.8V–3.3V supply for PMU controls. Must be directly connected to VDDIO on the PCB.
L16	VDDIO_RF	PWR	IO supply for RF switch control pads (3.3V).
A13	PCIE_PLL_AVDD1P2	PWR	1.2V supply for PCIe PLL.
A6	PCIE_RXTX_AVDD1P2	PWR	1.2V supply for PCIe TX and RX.
B16	PCIE_PME_L	OD	PCI power management event output. Used to request a change in the device or system power state. The assertion and deassertion of this signal is asynchronous to the PCIe reference clock. This signal has an open-drain output structure, as per the *PCI Bus Local Bus Specification, revision 2.3*.
Ground			
U22, V22, W22, Y22	WRF_XTAL_GND1P2	GND	XTAL ground.
V13	WRF_LOGENG_GND1P2	GND	LOGEN ground.

Table 19. Signal Descriptions (Cont.)

Ball	Signal Name	Type	Description
W13	WRF_VCO_GND1P2	GND	VCO ground.
W12	WRF_MMD_GND1P2	GND	Ground.
W11	WRF_CP_GND1P2	GND	Ground.
W10	WRF_PFD_GND1P2	GND	Ground.
A1, B2, E11, E12, E16, H12, H13, H16, J12, J14, P16, R11–R17, T13, T15, T16	VSSC	GND	Core ground for WLAN.
A22, A23	SR_PVSS	GND	Power ground.
E17	PMU_AVSS	GND	Quiet ground.
L9	AVSS_BBPLL	GND	Baseband PLL ground.
T2, T5, T7, T10, U1, U2, U5, U13, U16, U17, V2, V5–V9, V16–V18, W1, W5, W6, W8, W15, W17, W18, Y2, AA2, AA22, AB2, AB4, AB5, AB7–AB11, AB13, AB15, AB16, AB18–AB23, AC1, AC3, AC5, AC10, AC12, AC14, AC18, AC19, AC21, AC23	RGND	GND	Ground.
K5, K8, L8, M2, M5, N5, N8, P5, P8, P10, R1, R2, R5, R7, R9	BTRGND	GND	Ground.
B9,B12	PCIE_AVSS	GND	PCIe ground.

12.4 WLAN/BT GPIO Signals and Strapping Options

The pins listed in Table 20 are sampled at power-on reset (POR) to determine the various operating modes. Sampling occurs a few milliseconds after an internal POR or deassertion of the external POR. After the POR, each pin assumes the GPIO or alternative function specified in the signal descriptions table. Each strapping option pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to GND, using a 10 kΩ resistor or less.

Note: Refer to the reference board schematics for more information.

Table 20. BT GPIO Functions and Strapping Options[a]

Pin Name	Default Function	Description
BT_GPIO4	0	1: BT Serial Flash is present. 0: BT Serial Flash is absent (default).

a. Currently, Bluetooth headless is only supported with BT_Sflash onboard.

13. DC Characteristics

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

13.1 Absolute Maximum Ratings

Caution! The absolute maximum ratings in Table 21 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 21. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
DC supply for VBAT[a] and PA driver supply[b]	VBAT	–0.5 to +6.0	V
DC supply voltage for digital I/O	VDDIO	–0.5 to 3.9	V
DC supply voltage for RF switch I/Os	VDDIO_RF	–0.5 to 3.9	V
DC input supply voltage for CLDO and LNLDO	–	–0.5 to 1.575	V
DC supply voltage for RF analog	VDDRF	–0.5 to 1.32	V
DC supply voltage for core	VDDC	–0.5 to 1.32	V
WRF_TCXO_VDD	–	–0.5 to 3.63	V
Maximum undershoot voltage for I/O[c]	$V_{undershoot}$	–0.5	V
Maximum overshoot voltage for I/O[c]	$V_{overshoot}$	VDDIO + 0.5	V
Maximum junction temperature	T_j	125	°C

a. VBAT is the main power supply of the chip.
b. Voltage transients up to 6.0V for up to 10 seconds, cumulative duration over the lifetime of the device, are allowed. Voltage transients as high as 5.5V for up to 250 seconds, cumulative duration over the lifetime of the device, are allowed.
c. Duration not to exceed 25% of the duty cycle.

13.2 Environmental Ratings

The environmental ratings are shown in Table 22.

Table 22. Environmental Ratings

Characteristic	Value	Units	Conditions/Comments
Ambient temperature (T_A)	0 to +60	°C	Functional operation[a]
Storage temperature	–40 to +125	°C	–
Relative humidity	Less than 60	%	Storage
	Less than 85	%	Operation

a. Functionality is guaranteed but specifications require derating at extreme temperatures; see the specification tables for details.

13.3 Recommended Operating Conditions and DC Characteristics

Note: Functional operation is not guaranteed outside of the limits shown in Table 23, and operation outside these limits for extended periods can adversely affect long-term reliability of the device.

Table 23. Recommended Operating Conditions and DC Characteristics

Parameter	Symbol	Value			Unit
		Minimum	Typical	Maximum	
DC supply voltage for VBAT	VBAT[a]	3.0[b]	–	3.6	V
DC supply voltage for core	VDD	1.14	1.2	1.26	V
DC supply voltage for RF blocks in chip	VDDRF	1.14	1.2	1.26	V
DC supply voltage for TCXO input buffer	WRF_TCX-O_VDD	1.62	1.8	1.98	V
DC supply voltage for digital I/O	VDDIO, VDDIO_SD	1.71	–	3.63	V
DC supply voltage for RF switch I/Os	VDDIO_RF	3.0	3.3	3.6	V
External TSSI input	TSSI	0.15	–	0.95	V
Internal POR threshold	Vth_POR	0.4	–	0.7	V
Other Digital I/O Pins					
For VDDIO = 1.8V:					
Input high voltage	VIH	0.65 × VDDIO	–	–	V
Input low voltage	VIL	–	–	0.35 × VDDIO	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.45	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.45	V
For VDDIO = 3.3V:					
Input high voltage	VIH	2.00	–	–	V
Input low voltage	VIL	–	–	0.80	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output low Voltage @ 2 mA	VOL	–	–	0.40	V
RF Switch Control Output Pins[c]					
For VDDIO_RF = 3.3V:					
Output high voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.40	V
Input capacitance	C_{IN}	–	–	5	pF

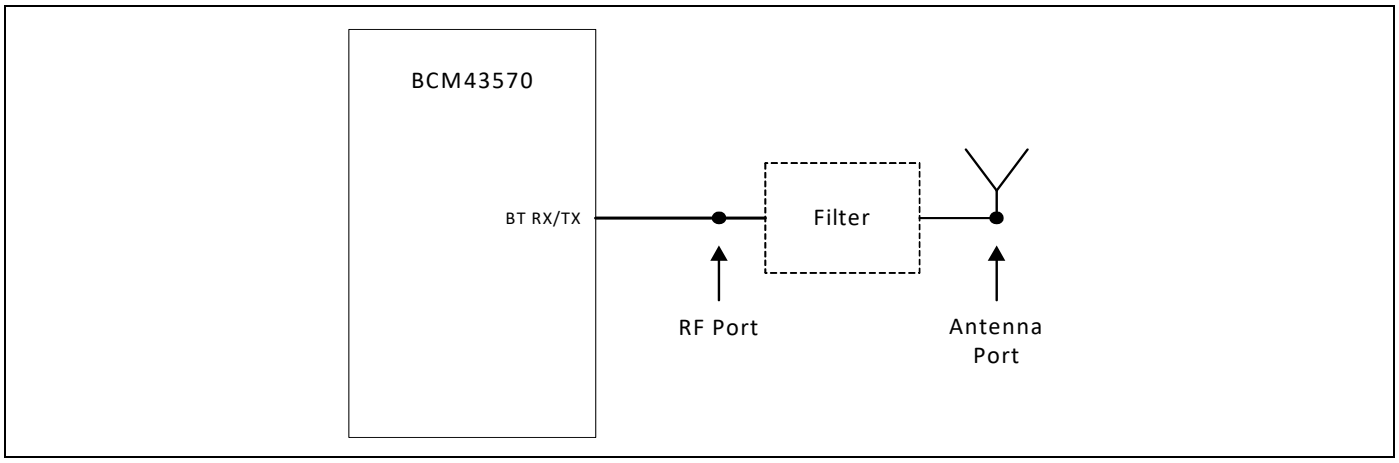
a. VBAT is the main power supply of the chip.
b. The CYW43570 is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3.13V < VBAT < 3.6V.
c. Programmable 2 mA to 16 mA drive strength. Default is 10 mA.

14. Bluetooth RF Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, limit values apply for the conditions specified in Table 22 and Table 23. Typical values apply for an ambient temperature of +25°C.

Figure 24. RF Port Location for Bluetooth Testing



Note: All Bluetooth specifications are measured at the chip port unless otherwise specified.

Table 24. Bluetooth Receiver RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Note: The specifications in this table are measured at the chip port output unless otherwise specified.					
General					
Frequency range	–	2402	–	2480	MHz
RX sensitivity	GFSK, 0.1% BER, 1 Mbps	–	–92	–	dBm
	π/4–DQPSK, 0.01% BER, 2 Mbps	–	–94	–	dBm
	8–DPSK, 0.01% BER, 3 Mbps	–	–88	–	dBm
Input IP3	–	–	–16	–	dBm
Maximum input at antenna	–	–	–20	–	dBm
Rx LO Leakage					
2.4 GHz band	–	–	–93	–80.0	dBm
Interference Performance[a]					
C/I co-channel	GFSK, 0.1% BER	–	8	11	dB
C/I 1 MHz adjacent channel	GFSK, 0.1% BER	–	–7	0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1% BER	–	–38	–30	dB
C/I ≥ 3 MHz adjacent channel	GFSK, 0.1% BER	–	–56	–40	dB
C/I image channel	GFSK, 0.1% BER	–	–31	–9	dB
C/I 1 MHz adjacent to image channel	GFSK, 0.1% BER	–	–46	–20	dB
C/I co-channel	π/4–DQPSK, 0.1% BER	–	9	13	dB
C/I 1 MHz adjacent channel	π/4–DQPSK, 0.1% BER	–	–11	0	dB
C/I 2 MHz adjacent channel	π/4–DQPSK, 0.1% BER	–	–39	–30	dB
C/I ≥ 3 MHz adjacent channel	π/4–DQPSK, 0.1% BER	–	–55	–40	dB
C/I image channel	π/4–DQPSK, 0.1% BER	–	–23	–7	dB

Table 24. Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
C/I 1 MHz adjacent to image channel	π/4–DQPSK, 0.1% BER	–	–43	–20	dB
C/I co-channel	8–DPSK, 0.1% BER	–	17	21	dB
C/I 1 MHz adjacent channel	8–DPSK, 0.1% BER	–	–4	5	dB
C/I 2 MHz adjacent channel	8–DPSK, 0.1% BER	–	–37	–25	dB
C/I ≥ 3 MHz adjacent channel	8–DPSK, 0.1% BER	–	–53	–33	dB
C/I Image channel	8–DPSK, 0.1% BER	–	–16	0	dB
C/I 1 MHz adjacent to image channel	8–DPSK, 0.1% BER	–	–37	–13	dB

a. The maximum value represents the actual Bluetooth specification required for Bluetooth qualification as defined in the version 4.1 specification.

Table 25. Bluetooth Transmitter RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Note: The specifications in this table are measured at the Chip port output unless otherwise specified.					
General					
Frequency range		2402	–	2480	MHz
Basic rate (GFSK) Tx power at Bluetooth		–	12.0	–	dBm
QPSK Tx power at Bluetooth		–	9.0	–	dBm
8PSK Tx power at Bluetooth		–	9.0	–	dBm
Power control step	–	–	4	8	dB
Note: Output power is with TCA and TSSI enabled.					
GFSK In-Band Spurious Emissions					
–20 dBc BW	–	–	0.93	1	MHz
EDR In-Band Spurious Emissions					
1.0 MHz < |M – N| < 1.5 MHz	M – N = the frequency range for which the spurious emission is measured relative to the transmit center frequency.	–	–38	–26.0	dBc
1.5 MHz < |M – N| < 2.5 MHz		–	–31	–20.0	dBm
|M – N| ≥ 2.5 MHz[a]		–	–43	–40.0	dBm
Out-of-Band Spurious Emissions					
30 MHz to 1 GHz	–	–	–	–36.0 [b, c]	dBm
1 GHz to 12.75 GHz	–	–	–	–30.0 [b, d, e]	dBm
1.8 GHz to 1.9 GHz	–	–	–	–47.0	dBm
5.15 GHz to 5.3 GHz	–	–	–	–47.0	dBm
GPS Band Spurious Emissions					
Spurious emissions	–	–	–103	–	dBm

a. The typical number is measured at ± 3 MHz offset.
b. The maximum value represents the value required for Bluetooth qualification as defined in the v4.1 specification.
c. The spurious emissions during Idle mode are the same as specified in Table 25.
d. Specified at the Bluetooth Antenna port.
e. Meets this specification using a front-end band-pass filter.

Table 26. Local Oscillator Performance

Parameter	Minimum	Typical	Maximum	Unit
LO Performance				
Lock time	–	72	–	µs
Initial carrier frequency tolerance	–	±25	±75	kHz
Frequency Drift				
DH1 packet	–	±8	±25	kHz
DH3 packet	–	±8	±40	kHz
DH5 packet	–	±8	±40	kHz
Drift rate	–	5	20	kHz/50 µs
Frequency Deviation				
00001111 sequence in payload[a]	140	155	175	kHz
10101010 sequence in payload[b]	115	140	–	kHz
Channel spacing	–	1	–	MHz

a. This pattern represents an average deviation in payload.
b. Pattern represents the maximum deviation in payload for 99.9% of all frequency deviations.

Table 27. BLE RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Frequency range	–	2402	–	2480	MHz
Rx sense[a]	GFSK, 0.1% BER, 1 Mbps	–	–94	–	dBm
Tx power[b]	–	–	8.5	–	dBm
Mod Char: delta F1 average	–	225	255	275	kHz
Mod Char: delta F2 max[c]	–	–	99.9	–	%
Mod Char: ratio	–	0.8	0.95	–	%

a. Dirty Tx is On.
b. BLE Tx power can be increased to compensate for front-end losses such as BPF, diplexer, switch, etc.). The output is capped at 12 dBm out. The BLE Tx power at the antenna port cannot exceed the 10 dBm specification limit.
c. At least 99.9% of all delta F2 max frequency values recorded over 10 packets must be greater than 185 kHz.

15. WLAN RF Specifications

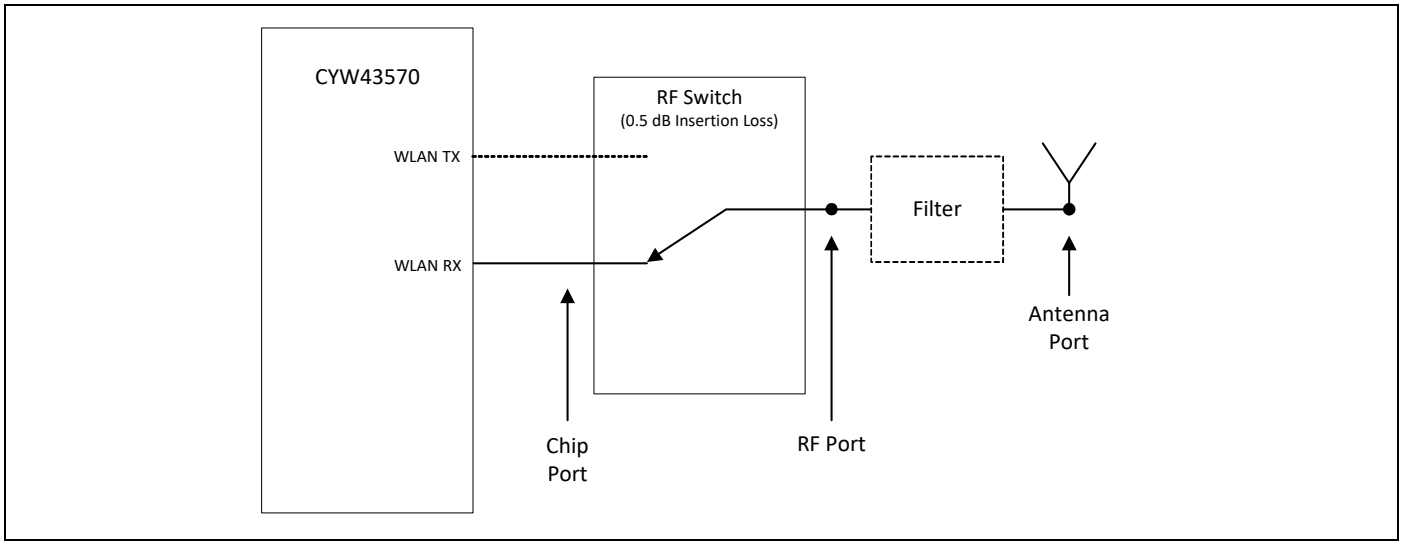
15.1 Introduction

The CYW43570 includes an integrated dual-band direct conversion radio that supports the 2.4 GHz and the 5 GHz bands. This section describes the RF characteristics of the 2.4 GHz and 5 GHz radios.

Note: Values in this section of the data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, limit values apply for the conditions specified in Table 22 and Table 23. Typical values apply for an ambient temperature +25°C.

Figure 25. Port Locations (Applies to 2.4 GHz and 5 GHz)



15.2 2.4 GHz Band General RF Specifications

Table 28. 2.4 GHz Band General RF Specifications

Item	Condition	Min.	Typ.	Max.	Unit
Tx/Rx switch time	Including TX ramp down	–	–	5	µs
Rx/Tx switch time	Including TX ramp up	–	–	2	µs
Power-up and power-down ramp time	DSSS/CCK modulations	–	–	< 2	µs

15.3 WLAN 2.4 GHz Receiver Performance Specifications

Note: The specifications in Table 29 are specified at the RF port unless otherwise specified. Results with FEMs that are not on the Cypress AVL are not guaranteed.

Table 29. WLAN 2.4 GHz Receiver Performance Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency range	–	2400	–	2500	MHz
RX sensitivity IEEE 802.11b[a]	1 Mbps DSSS	–	–98.5	–	dBm
	2 Mbps DSSS	–	–95.4	–	dBm
	5.5 Mbps DSSS	–	–93.4	–	dBm
	11 Mbps DSSS	–	–90.4	–	dBm
SISO RX sensitivity IEEE 802.11g (10% PER for 1024 octet PSDU)[a]	6 Mbps OFDM	–	–94.4	–	dBm
	9 Mbps OFDM	–	–93.4	–	dBm
	12 Mbps OFDM	–	–91.5	–	dBm
	18 Mbps OFDM	–	–89.3	–	dBm
	24 Mbps OFDM	–	–86.0	–	dBm
	36 Mbps OFDM	–	–82.8	–	dBm
	48 Mbps OFDM	–	–78.4	–	dBm
	54 Mbps OFDM	–	–77.0	–	dBm
MIMO RX sensitivity IEEE 802.11g (10% PER for 1024 octet PSDU)[a]	6 Mbps OFDM	–	–95.6	–	dBm/core
	9 Mbps OFDM	–	–95.4	–	dBm/core
	12 Mbps OFDM	–	–94.3	–	dBm/core
	18 Mbps OFDM	–	–92.4	–	dBm/core
	24 Mbps OFDM	–	–88.9	–	dBm/core
	36 Mbps OFDM	–	–85.8	–	dBm/core
	48 Mbps OFDM	–	–81.4	–	dBm/core
	54 Mbps OFDM	–	–80.0	–	dBm/core
SISO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU)[a, b] Defined for default parameters: GT, 800 ns GI, LDPC coding, and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS0	–	–93.6	–	dBm
	MCS1	–	–91.0	–	dBm
	MCS2	–	–88.7	–	dBm
	MCS3	–	–86.2	–	dBm
	MCS4	–	–82.7	–	dBm
	MCS5	–	–78.6	–	dBm
	MCS6	–	–77.2	–	dBm
	MCS7	–	–75.4	–	dBm

Table 29. WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
MIMO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU)[a, b] Defined for default parameters: GT, 800 ns GI, LDPC coding, and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS0	–	–94.8	–	dBm/core
	MCS1	–	–93.7	–	dBm/core
	MCS2	–	–91.6	–	dBm/core
	MCS3	–	–88.9	–	dBm/core
	MCS4	–	–85.6	–	dBm/core
	MCS5	–	–81.5	–	dBm/core
	MCS6	–	–80.3	–	dBm/core
	MCS7	–	–78.4	–	dBm/core
	MCS8	–	–94.5	–	dBm/core
	MCS15	–	–76.2	–	dBm/core
SISO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU)[a, b] Defined for default parameters: GT, 800 ns GI, LDPC coding, and non-STBC.	40 MHz channel spacing for all MCS rates				
	MCS0	–	–91.1	–	dBm
	MCS1	–	–88.5	–	dBm
	MCS2	–	–86.0	–	dBm
	MCS3	–	–83.5	–	dBm
	MCS4	–	–80.1	–	dBm
	MCS5	–	–76.3	–	dBm
	MCS6	–	–74.4	–	dBm
	MCS7	–	–73.1	–	dBm
MIMO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU)[a, b] Defined for default parameters: GT, 800 ns GI, LDPC coding, and non-STBC.	40 MHz channel spacing for all MCS rates				
	MCS0	–	–93.3	–	dBm/core
	MCS1	–	–91.3	–	dBm/core
	MCS2	–	–88.9	–	dBm/core
	MCS3	–	–86.2	–	dBm/core
	MCS4	–	–83.2	–	dBm/core
	MCS5	–	–79.2	–	dBm/core
	MCS6	–	–77.4	–	dBm/core
	MCS7	–	–76.5	–	dBm/core
	MCS8	–	–91.7	–	dBm/core
	MCS15	–	–73.4	–	dBm/core
SISO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU)[a, b] Defined for default parameters: 800 ns GI and non-STBC	20 MHz channel spacing for all MCS rates				
	MCS0, Nss 1	–	–93.8	–	dBm
	MCS1, Nss 1	–	–91.1	–	dBm
	MCS2, Nss 1	–	–89.9	–	dBm
	MCS3, Nss 1	–	–87.4	–	dBm
	MCS4, Nss 1	–	–83.6	–	dBm
	MCS5, Nss 1	–	–79.8	–	dBm
	MCS6, Nss 1	–	–78.4	–	dBm
	MCS7, Nss 1	–	–77.1	–	dBm
	MCS8, Nss 1	–	–72.9	–	dBm
	MCS9, Nss 1	–	–71.4	–	dBm

Table 29. WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
MIMO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU)[a, b] Defined for default parameters: 800 ns GI and non-STBC	20 MHz channel spacing for all MCS rates				
	MCS0, Nss 1	–	–95.6	–	dBm/core
	MCS1, Nss 1	–	–93.9	–	dBm/core
	MCS2, Nss 1	–	–92.6	–	dBm/core
	MCS3, Nss 1	–	–90.3	–	dBm/core
	MCS4, Nss 1	–	–87.0	–	dBm/core
	MCS5, Nss 1	–	–82.7	–	dBm/core
	MCS6, Nss 1	–	–81.3	–	dBm/core
	MCS7, Nss 1	–	–80.2	–	dBm/core
	MCS8, Nss 1	–	–76.3	–	dBm/core
	MCS9, Nss 1	–	–74.5	–	dBm/core
	MCS9, Nss 2	–	–71.1	–	dBm/core
SISO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU)[a, b] Defined for default parameters: 800 ns GI and non-STBC.	40 MHz channel spacing for all MCS rates				
	MCS0, Nss 1	–	–91.5	–	dBm
	MCS1, Nss 1	–	–88.5	–	dBm
	MCS2, Nss 1	–	–87.1	–	dBm
	MCS3, Nss 1	–	–84.7	–	dBm
	MCS4, Nss 1	–	–81.4	–	dBm
	MCS5, Nss 1	–	–77.2	–	dBm
	MCS6, Nss 1	–	–75.8	–	dBm
	MCS7, Nss 1	–	–74.4	–	dBm
	MCS8, Nss 1	–	–70.4	–	dBm
	MCS9, Nss 1	–	–68.7	–	dBm
MIMO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU)[a, b] Defined for default parameters: 800 ns GI and non-STBC.	40 MHz channel spacing for all MCS rates				
	MCS0, Nss 1	–	–93.1	–	dBm/core
	MCS1, Nss 1	–	–91.3	–	dBm/core
	MCS2, Nss 1	–	–89.7	–	dBm/core
	MCS3, Nss 1	–	–87.8	–	dBm/core
	MCS4, Nss 1	–	–84.3	–	dBm/core
	MCS5, Nss 1	–	–80.2	–	dBm/core
	MCS6, Nss 1	–	–78.6	–	dBm/core
	MCS7, Nss 1	–	–77.3	–	dBm/core
	MCS8, Nss 1	–	–73.6	–	dBm/core
	MCS9, Nss 1	–	–71.6	–	dBm/core
	MCS0, Nss 2	–	–91.7	–	dBm/core
	MCS9, Nss 2	–	–67.7	–	dBm/core
In-band static CW jammer immunity (fc – 8 MHz < fcw < + 8 MHz)	RX PER < 1%, 54 Mbps OFDM, 1000 octet PSDU for: (RxSens + 23 dB < Rxlevel < max input level)	–80	–	–	dBm
Input in–band IP3	Maximum LNA gain	–	–15.5	–	dBm
	Minimum LNA gain	–	–1.5	–	dBm

Table 29. WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Min.	Typ.	Max.	Unit
Maximum receive level @ 2.4 GHz	@ 1, 2 Mbps (8% PER, 1024 octets)		–	–3.5	–	dBm
	@ 5.5, 11 Mbps (8% PER, 1024 octets)		–	–9.5	–	dBm
	@ 6–54 Mbps (10% PER, 1024 octets)		–	–9.5	–	dBm
	@ MCS0–MCS7 rates (10% PER, 4095 octets)		–	–9.5	–	dBm
	@ MCS8–MCS9 rates (10% PER, 4095 octets)		–	–11.5	–	dBm
LPF 3 dB bandwidth	–		9	–	36	MHz
Adjacent channel rejection-DSSS (Difference between interfering and desired signal at 8% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	Desired and interfering signal 30 MHz apart					
	1 Mbps DSSS	–74 dBm	35	–	–	dB
	2 Mbps DSSS	–74 dBm	35	–	–	dB
	Desired and interfering signal 25 MHz apart					
	5.5 Mbps DSSS	–70 dBm	35	–	–	dB
	11 Mbps DSSS	–70 dBm	35	–	–	dB
Adjacent channel rejection-OFDM (difference between interfering and desired signal (25 MHz apart) at 10% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
Adjacent channel rejection MCS0–9 (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/Notes)	MCS0	–79 dBm	16	–	–	dB
	MCS1	–76 dBm	13	–	–	dB
	MCS2	–74 dBm	11	–	–	dB
	MCS3	–71 dBm	8	–	–	dB
	MCS4	–67 dBm	4	–	–	dB
	MCS5	–63 dBm	0	–	–	dB
	MCS6	–62 dBm	–1	–	–	dB
	MCS7	–61 dBm	–2	–	–	dB
	MCS8	–59 dBm	–4	–	–	dB
	MCS9	–57 dBm	–6	–	–	dB
Maximum receiver gain	–	–	–	95	–	dB
Gain control step	–	–	–	3	–	dB
RSSI accuracy[c]	Range –90 dBm to –30 dBm		–5	–	5	dB
	Range above –30 dBm		–8	–	8	dB
Return loss	Zo = 50Ω, across the dynamic range		10	11.5	13	dB
Receiver cascaded noise figure	At maximum gain		–	4.5	–	dB

a. Derate by 1.5 dB over the operating temperature range and for voltages from 3.0V to 3.13V.
b. Sensitivity degradations for alternate settings in MCS modes. MM: 0.5 dB drop, and SGI: 2 dB drop.
c. The minimum and maximum values shown have a 95% confidence level.

15.4 WLAN 2.4 GHz Transmitter Performance Specifications

Note: The specifications in Table 30 are specified at the RF port unless otherwise specified. Results with FEMs that are not on the Cypress AVL are not guaranteed.

Table 30. WLAN 2.4 GHz Transmitter Performance Specifications

Parameter	Condition/Notes		Min.	Typ.	Max.	Unit
Frequency range	–		2400	–	2500	MHz
EVM Does Not Exceed						
TX power at RF port for highest power level setting at 25°C with spectral mask and EVM compliance[a]	802.11b (DSSS/CCK)	–9 dB	18.5	20	–	dBm
	OFDM, BPSK	–8 dB	18	19	–	dBm
	OFDM, QPSK	–13 dB	18	19	–	dBm
	OFDM, 16-QAM	–19 dB	16.5	18	–	dBm
	OFDM, 64-QAM (R = 3/4)	–25 dB	16.5	18	–	dBm
	OFDM, 64-QAM (R = 5/6)	–28 dB	16.5	18	–	dBm
	OFDM, 256-QAM (R = 3/4)	–30 dB	15.5	17	–	dBm
	OFDM, 256-QAM (R = 5/6)	–32 dB	14.5	16	–	dBm
Phase noise	40 MHz crystal, integrated from 10 kHz to 10 MHz		–	0.45	–	Degrees
TX power control dynamic range	–		10	–	–	dB
Closed-loop TX power variation at highest power level setting	Across full temperature and voltage range. Applies across 10 dBm to 20 dBm output power range.		–	–	±1.5	dB
Carrier suppression	–		15	–	–	dBc
Gain control step	–		–	0.25	–	dB
Return loss at chip port TX	Zo = 50Ω		–	6	–	dB

a. Derate by 1.5 dB over the operating temperature range and for voltages from 3.0V to 3.13V.

15.5 WLAN 5 GHz Receiver Performance Specifications

Note: The specifications in Table 31 are specified at the RF port unless otherwise specified. Results with FEMs that are not on the Cypress AVL are not guaranteed.

Table 31. WLAN 5 GHz Receiver Performance Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency range	–	4900	–	5845	MHz
SISO RX sensitivity IEEE 802.11a (10% PER for 1000 octet PSDU)[a]	6 Mbps OFDM	–	–94.5	–	dBm
	9 Mbps OFDM	–	–93.2	–	dBm
	12 Mbps OFDM	–	–91.3	–	dBm
	18 Mbps OFDM	–	–89.1	–	dBm
	24 Mbps OFDM	–	–85.7	–	dBm
	36 Mbps OFDM	–	–82.4	–	dBm
	48 Mbps OFDM	–	–78.0	–	dBm
	54 Mbps OFDM	–	–76.6	–	dBm
MIMO RX sensitivity IEEE 802.11a (10% PER for 1024 octet PSDU)[a]	6 Mbps OFDM	–	–95.7	–	dBm/core
	9 Mbps OFDM	–	–95.6	–	dBm/core
	12 Mbps OFDM	–	–94.1	–	dBm/core
	18 Mbps OFDM	–	–92.1	–	dBm/core
	24 Mbps OFDM	–	–89.0	–	dBm/core
	36 Mbps OFDM	–	–85.7	–	dBm/core
	48 Mbps OFDM	–	–81.2	–	dBm/core
	54 Mbps OFDM	–	–79.9	–	dBm/core
SISO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU)[a] Defined for default parameters: GF, 800 ns GI, LDPC coding, and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS0	–	–93.3	–	dBm
	MCS1	–	–90.9	–	dBm
	MCS2	–	–88.7	–	dBm
	MCS3	–	–86.1	–	dBm
	MCS4	–	–82.5	–	dBm
	MCS5	–	–78.4	–	dBm
	MCS6	–	–76.9	–	dBm
	MCS7	–	–75.1	–	dBm
MIMO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU)[a] Defined for default parameters: GF, 800 ns GI, LDPC coding, and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS0	–	–95.8	–	dBm/core
	MCS1	–	–93.8	–	dBm/core
	MCS2	–	–91.4	–	dBm/core
	MCS3	–	–88.7	–	dBm/core
	MCS4	–	–85.6	–	dBm/core
	MCS5	–	–81.4	–	dBm/core
	MCS6	–	–79.8	–	dBm/core
	MCS7	–	–78.3	–	dBm/core
	MCS8	–	–75.6	–	dBm/core
	MCS15	–	–72.7	–	dBm/core

Table 31. WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
SISO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU)[a] Defined for default parameters: GF, 800 ns GI, LDPC coding, and non-STBC.	40 MHz channel spacing for all MCS rates				
	MCS0	–	–91.1	–	dBm
	MCS1	–	–88.5	–	dBm
	MCS2	–	–86.0	–	dBm
	MCS3	–	–83.5	–	dBm
	MCS4	–	–80.1	–	dBm
	MCS5	–	–76.3	–	dBm
	MCS6	–	–74.3	–	dBm
	MCS7	–	–72.9	–	dBm
MIMO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU)[a] Defined for default parameters: GF, 800 ns GI, LDPC coding, and non-STBC.	40 MHz channel spacing for all MCS rates				
	MCS0	–	–92.9	–	dBm/core
	MCS1	–	–91.1	–	dBm/core
	MCS2	–	–88.7	–	dBm/core
	MCS3	–	–86.2	–	dBm/core
	MCS4	–	–83.0	–	dBm/core
	MCS5	–	–79.2	–	dBm/core
	MCS6	–	–77.4	–	dBm/core
	MCS7	–	–76.4	–	dBm/core
	MCS8	–	–91.9	–	dBm/core
	MCS15	–	–73.3	–	dBm/core
SISO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU)[a] Defined for default parameters: 800 ns GI, LDPC coding, and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS0, Nss 1	–	–93.4	–	dBm
	MCS1, Nss 1	–	–91.0	–	dBm
	MCS2, Nss 1	–	–89.7	–	dBm
	MCS3, Nss 1	–	–87.2	–	dBm
	MCS4, Nss 1	–	–83.1	–	dBm
	MCS5, Nss 1	–	–79.5	–	dBm
	MCS6, Nss 1	–	–78.0	–	dBm
	MCS7, Nss 1	–	–76.8	–	dBm
	MCS8, Nss 1	–	–72.3	–	dBm
	MCS9, Nss 1	–	–70.7	–	dBm

Table 31. WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
MIMO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU)[a] Defined for default parameters: 800 ns GI, LDPC coding, and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS0, Nss 1	–	–95.7	–	dBm/core
	MCS1, Nss 1	–	–93.9	–	dBm/core
	MCS2, Nss 1	–	–92.7	–	dBm/core
	MCS3, Nss 1	–	–90.3	–	dBm/core
	MCS4, Nss 1	–	–86.8	–	dBm/core
	MCS5, Nss 1	–	–82.7	–	dBm/core
	MCS6, Nss 1	–	–81.4	–	dBm/core
	MCS7, Nss 1	–	–79.9	–	dBm/core
	MCS8, Nss 1	–	–75.6	–	dBm/core
	MCS0, Nss 2	–	–91	–	dBm/core
	MCS8, Nss 2	–	–67.1	–	dBm/core
	MCS9, Nss 2	–	–74.1	–	dBm/core
SISO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU)[a] Defined for default parameters: 800 ns GI, LDPC coding, and non-STBC.	40 MHz channel spacing for all MCS rates				
	MCS0, Nss 1	–	–91.5	–	dBm
	MCS1, Nss 1	–	–88.5	–	dBm
	MCS2, Nss 1	–	–87.2	–	dBm
	MCS3, Nss 1	–	–84.6	–	dBm
	MCS4, Nss 1	–	–81.2	–	dBm
	MCS5, Nss 1	–	–77.1	–	dBm
	MCS6, Nss 1	–	–75.6	–	dBm
	MCS7, Nss 1	–	–74.2	–	dBm
	MCS8, Nss 1	–	–70.0	–	dBm
	MCS9, Nss 1	–	–68.2	–	dBm
MIMO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU)[a] Defined for default parameters: 800 ns GI, LDPC coding, and non-STBC.	40 MHz channel spacing for all MCS rates				
	MCS0, Nss 1	–	–93.0	–	dBm/core
	MCS1, Nss 1	–	–91.2	–	dBm/core
	MCS2, Nss 1	–	–89.8	–	dBm/core
	MCS3, Nss 1	–	–87.6	–	dBm/core
	MCS4, Nss 1	–	–84.1	–	dBm/core
	MCS5, Nss 1	–	–80.1	–	dBm/core
	MCS6, Nss 1	–	–78.6	–	dBm/core
	MCS7, Nss 1	–	–77.3	–	dBm/core
	MCS8, Nss 1	–	–73.1	–	dBm/core
	MCS9, Nss 1	–	–71.4	–	dBm/core
	MCS0, Nss 2	–	–91.8	–	dBm/core
	MCS9, Nss 2	–	–67.1	–	dBm/core

Table 31. WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Min.	Typ.	Max.	Unit
SISO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU)[a] Defined for default parameters: 800 ns GI, LDPC coding, and non-STBC.	80 MHz channel spacing for all MCS rates					
	MCS0, Nss 1		–	–88.7	–	dBm
	MCS1, Nss 1		–	–85.2	–	dBm
	MCS2, Nss 1		–	–83.8	–	dBm
	MCS3, Nss 1		–	–81.2	–	dBm
	MCS4, Nss 1		–	–77.8	–	dBm
	MCS5, Nss 1		–	–73.5	–	dBm
	MCS6, Nss 1		–	–72.2	–	dBm
	MCS7, Nss 1		–	–70.5	–	dBm
	MCS8, Nss 1		–	–66.4	–	dBm
	MCS9, Nss 1		–	–64.1	–	dBm
MIMO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU)[a] Defined for default parameters: 800 ns GI, LDPC coding, and non-STBC.	80 MHz channel spacing for all MCS rates					
	MCS0, Nss 1		–	–90.2	–	dBm/core
	MCS1, Nss 1		–	–88.0	–	dBm/core
	MCS2, Nss 1		–	–86.5	–	dBm/core
	MCS3, Nss 1		–	–84.2	–	dBm/core
	MCS4, Nss 1		–	–80.7	–	dBm/core
	MCS5, Nss 1		–	–76.6	–	dBm/core
	MCS6, Nss 1		–	–75.0	–	dBm/core
	MCS7, Nss 1		–	–73.4	–	dBm/core
	MCS8, Nss 1		–	–69.4	–	dBm/core
	MCS9, Nss 1		–	–67.2	–	dBm/core
	MCS0, Nss 2		–	–88.2	–	dBm/core
	MCS9, Nss 2		–	–62.2	–	dBm/core
Input in-band IP3	Maximum LNA gain		–	–15.5	–	dBm
	Minimum LNA gain		–	–1.5	–	dBm
Maximum receive level @ 5.24 GHz	@ 6, 9, 12 Mbps		–	–9.5	–	dBm
	@ 18, 24, 36, 48, 54 Mbps		–	–14.5	–	dBm
LPF 3 dB bandwidth	–		9	–	36	MHz
Adjacent channel rejection (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 1000 octet PSDU with desired signal level as specified in Condition/ Notes)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
	65 Mbps OFDM	–61 dBm	–2	–	–	dB

Table 31. WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Min.	Typ.	Max.	Unit
(Difference between interfering and desired signal (40 MHz apart) at 10% PER for 1000[b] octet PSDU with desired signal level as specified in Condition/ Notes)	6 Mbps OFDM	–78.5 dBm	32	–	–	dB
	9 Mbps OFDM	–77.5 dBm	31	–	–	dB
	12 Mbps OFDM	–75.5 dBm	29	–	–	dB
	18 Mbps OFDM	–73.5 dBm	27	–	–	dB
	24 Mbps OFDM	–70.5 dBm	24	–	–	dB
	36 Mbps OFDM	–66.5 dBm	20	–	–	dB
	48 Mbps OFDM	–62.5 dBm	16	–	–	dB
	54 Mbps OFDM	–61.5 dBm	15	–	–	dB
	65 Mbps OFDM	–60.5 dBm	14	–	–	dB
Maximum receiver gain	–		–	95	–	dB
Gain control step	–		–	3	–	dB
RSSI accuracy[c]	Range –90 dBm to –30 dBm		–5	–	5	dB
	Range above –30 dBm		–8	–	8	dB
Return loss	Zo = 50Ω, across the dynamic range		10	–	13	dB
Receiver cascaded noise figure	At maximum gain		–	5	–	dB

a. Derate by 1.5 dB over the operating temperature range and for voltages from 3.0V to 3.13V.
b. For 65 Mbps, the size is 4096.
c. The minimum and maximum values shown have a 95% confidence level.

15.6 WLAN 5 GHz Transmitter Performance Specifications

Note: The specifications in Table 32 are specified at the RF port unless otherwise specified. Results with FEMs that are not on the Cypress AVL are not guaranteed.

Table 32. WLAN 5 GHz Transmitter Performance Specifications

Parameter	Condition/Notes		Min.	Typ.	Max.	Unit
Frequency range	–		4900	–	5845	MHz
TX power at RF port for highest power level setting at 25°C with spectral mask and EVM compliance[a]	OFDM, QPSK	–13 dB	17.5	18.5	–	dBm
	OFDM, 16-QAM	–19 dB	16	17.5	–	dBm
	OFDM, 64-QAM (R = 3/4)	–25 dB	16	17.5	–	dBm
	OFDM, 64-QAM (R = 5/6)	–28 dB	16	17.5	–	dBm
	OFDM, 256-QAM (R = 3/4, VHT)	–30 dB	14	15.5	–	dBm
	OFDM, 256-QAM (R = 5/6, VHT)	–32 dB	13	14.5	–	dBm
Phase noise	40 MHz crystal, integrated from 10 kHz to 10 MHz		–	0.5	–	Degrees
TX power control dynamic range	–		10	–	–	dB
Closed loop TX power variation at highest power level setting	Across full-temperature and voltage range. Applies across 10 to 20 dBm output power range.		–	–	±2.0	dB
Carrier suppression	–		15	–	–	dBc
Gain control step	–		–	0.25	–	dB
Return loss	Zo = 50Ω		–	6	–	dB

a. Derate by 1.5 dB over the operating temperature range and for voltages from 3.0V to 3.13V.

16. Internal Regulator Electrical Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization. Functional operation is not guaranteed outside of the specification limits provided in this section.

16.1 Core Buck Switching Regulator

Table 33. Core Buck Switching Regulator (CBUCK) Specifications

Specification	Notes	Min	Typ	Max	Units
Input supply voltage (DC)	DC voltage range inclusive of disturbances.	3.0	3.3	3.6[a]	V
PWM mode switching frequency	CCM, Load > 100 mA VBAT = 3.6V	2.8	4	5.2	MHz
PWM output current	–	–	–	600	mA
Output current limit	–	–	1400	–	mA
Output voltage range	Programmable, 30 mV steps Default = 1.35V	1.2	1.35	1.5	V
PWM output voltage DC accuracy	Includes load and line regulation. Forced PWM mode	–4	–	4	%
PWM ripple voltage, static	Measure with 20 MHz bandwidth limit. Static Load. Max Ripple based on VBAT = 3.6V, Vout = 1.35V, Fsw = 4 MHz, 2.2 µH inductor L > 1.05 µH, Cap + Board total-ESR < 20 mΩ, C_{out} > 1.9 µF, ESL<200pH	–	7	20	mVpp
PWM mode peak efficiency	Peak Efficiency at 200 mA load	78	86	–	%
PFM mode efficiency	10 mA load current	70	81	–	%
Start-up time from power down	VIO already ON and steady. Time from REG_ON rising edge to CLDO reaching 1.2V	–	–	850	µs
External inductor	0806 size, ± 30%, 0.11 ± 25% Ohms	–	2.2	–	µH
External output capacitor	Ceramic, X5R, 0402, ESR <30 mΩ at 4 MHz, ± 20%, 6.3V	2.0[b]	4.7	10[c]	µF
External input capacitor	For SR_VDDBATP5V pin, ceramic, X5R, 0603, ESR < 30 mΩ at 4 MHz, ± 20%, 6.3V, 4.7 µF	0.67[b]	4.7	–	µF
Input supply voltage ramp-up time	0V to 3.3V	40	–	–	µs

a. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.5V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
b. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.
c. Total capacitance includes those connected at the far end of the active load.

16.2 2.5V LDO (BTLDO2P5)

Table 34. BTLDO2P5 Specifications

Specification	Notes	Min	Typ	Max	Units
Input supply voltage	Min = 2.5V + 0.2V = 2.7V. Dropout voltage requirement must be met under maximum load for performance specifications.	3.0	3.3	3.6[a]	V
Nominal output voltage	Default = 2.5V.	–	2.5	–	V
Output voltage programmability	Range	2.2	2.5	2.8	V
	Accuracy at any step (including line/load regulation), load > 0.1 mA.	–5	–	5	%
Dropout voltage	At maximum load.	–	–	200	mV
Output current	–	0.1	–	70	mA
Quiescent current	No load.	–	8	16	µA
	Maximum load at 70 mA.	–	660	700	µA
Leakage current	Power-down mode.	–	1.5	5	µA
Line regulation	V_{in} from (V_o + 0.2V) to 3.6V, maximum load.	–	–	3.5	mV/V
Load regulation	Load from 1 mA to 70 mA, V_{in} = 3.6V.	–	–	0.3	mV/mA
PSRR	$V_{in} \geq V_o$ + 0.2V, V_o = 2.5V, C_o = 2.2 µF, maximum load, 100 Hz to 100 kHz.	20	–	–	dB
LDO turn-on time	Chip already powered up.	–	–	150	µs
In-rush current	$V_{in} = V_o$ + 0.15V to 3.6V, C_o = 2.2 µF, No load.	–	–	250	mA
External output capacitor, C_o	Ceramic, X5R, 0402, (ESR: 5–240 mΩ), ±10%, 10V	0.7[b]	2.2	2.64	µF
External input capacitor	For SR_VDDBATA5V pin (shared with Bandgap) ceramic, X5R, 0402, (ESR: 30–200 mΩ), ±10%, 10V. Not needed if sharing VBAT 4.7 µF capacitor with SR_VDDBATP5V.	–	4.7	–	µF

a. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.5V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
b. The minimum value refers to the residual capacitor value after taking into account part-to-part tolerance, DC-bias, temperature, and aging.

16.3 CLDO

Table 35. CLDO Specifications

Specification	Notes	Min	Typ	Max	Units
Input supply voltage, V_{in}	Min = 1.2 + 0.15V = 1.35V dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output current	–	0.2	–	300	mA
Output voltage, V_o	Programmable in 25 mV steps. Default = 1.2.V	1.1	1.2	1.275	V
Dropout voltage	At max load	–	–	150	mV
Output voltage DC accuracy	Includes line/load regulation	–4	–	+4	%
Quiescent current	No load	–	24	–	µA
	300 mA load	–	2.1	–	mA
Line Regulation	V_{in} from (V_o + 0.15V) to 1.5V, maximum load	–	–	5	mV/V
Load Regulation	Load from 1 mA to 300 mA	–	0.02	0.05	mV/mA
Leakage Current	Power down	–	–	20	µA
	Bypass mode	–	1	3	µA
PSRR	@1 kHz, Vin ≥ 1.35V, C_o = 4.7 µF	20	–	–	dB
Start-up Time of PMU	VIO up and steady. Time from the REG_ON rising edge to the CLDO reaching 1.2V.	–	–	700	µs
LDO Turn-on Time	LDO turn-on time when rest of the chip is up	–	140	180	µs
External Output Capacitor, C_o	Total ESR: 5–240 mΩ	1.32[a]	4.7	–	µF
External Input Capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output.	–	1	2.2	µF

a. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

16.4 LNLDO

Table 36. LNLDO Specifications

Specification	Notes	Min	Typ	Max	Units
Input supply voltage, Vin	Min = $1.2V_o$ + 0.15V = 1.35V dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output Current	–	0.1	–	150	mA
Output Voltage, V_o	Programmable in 25 mV steps. Default = 1.2V	1.1	1.2	1.275	V
Dropout Voltage	At maximum load	–	–	150	mV
Output Voltage DC Accuracy	Includes line/load regulation	–4	–	+4	%
Quiescent current	No load	–	44	–	µA
	Max load	–	970	990	µA
Line Regulation	V_{in} from (V_o + 0.1V) to 1.5V, max load	–	–	5	mV/V
Load Regulation	Load from 1 mA to 150 mA	–	0.02	0.05	mV/mA
Leakage Current	Power-down	–	–	10	µA
Output Noise	@30 kHz, 60–150 mA load C_o = 2.2 µF @100 kHz, 60–150 mA load C_o = 2.2 µF	–	–	60 35	nV/rt Hz nV/rt Hz
PSRR	@ 1kHz, Input > 1.35V, C_o= 2.2 µF, V_o = 1.2V	20	–	–	dB
LDO Turn-on Time	LDO turn-on time when rest of chip is up	–	140	180	µs
External Output Capacitor, C_o	Total ESR (trace/capacitor): 5–240 mΩ	0.5[a]	2.2	4.7	µF
External Input Capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output. Total ESR (trace/capacitor): 30–200 mΩ	–	1	2.2	µF

a. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

17. System Power Consumption

17.1 WLAN Current Consumption

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization. Unless otherwise stated, these values apply for the conditions specified in Table 23.

The WLAN current consumption measurements are shown in Table 37. All values in Table 37 are with the Bluetooth core in reset.

Table 37. Typical WLAN Power Consumption

Mode	Bandwidth (MHz)	Band (GHz)	V_{BAT} = V_{IO} = 3.3V (mA)
OFF[a]	**–**	**–**	**0.07**
Sleep[b]	**–**	**–**	**0.3**
IEEE power save, WoWL mode, DTIM 1 1 RX core[c]	20	2.4	3.87
IEEE power save, WoWL mode, DTIM 3 1 RX core[c]	20	2.4	1.42
IEEE power save, WoWL mode, DTIM 1 1 RX core[c]	20	5	2.34
IEEE power save, WoWL mode, DTIM 3 1 RX core[c]	20	5	0.98
IEEE power save, WoWL mode, DTIM 1 1 RX core[c]	40	5	2.65
IEEE power save, WoWL mode, DTIM 3 1 RX core[c]	40	5	1.07
IEEE power save, WoWL mode, DTIM 1 1 RX core[c]	80	5	3.13
IEEE power save, WoWL mode, DTIM 3 1 RX core[c]	80	5	1.14
IEEE power save, DTIM 1 1 RX core[c, d]	20	2.4	8
IEEE power save, DTIM 3 1 RX core[c, d]	20	2.4	6.1
IEEE power save, DTIM 1 1 RX core[c, d]	20	5	7
IEEE power save, DTIM 3 1 RX core[c, d]	20	5	5.7
IEEE power save, DTIM 1 1 RX core[c, d]	40	5	7.2
IEEE power save, DTIM 3 1 RX core[c, d]	40	5	5.8
IEEE power save, DTIM 1 1 RX core[c, d]	80	5	7.3
IEEE power save, DTIM 3 1 RX core[c, d]	80	5	5.8
Active Modes			
Transmit			
Rate 11 (at measured power/core = 18.5 dBm)	20	2.4	358
MCS8, NSS 1 (at measured power/core = 14 dBm)	20	2.4	250
MCS8, NSS 2 (at measured power/core = 14 dBm)	20	2.4	470
MCS7, SGI (at measured power/core = 15 dBm)	20	5	302
MCS15, SGI (at measured power/core = 15 dBm)	20	5	543
MCS7 (at measured power/core = 17 dBm)	40	5	332
MCS9, NSS 1 (at measured power/core = 14.5 dBm)	40	5	322
MCS9, NSS 2 (at measured power/core = 14.5 dBm)	40	5	590
MCS9, NSS 1 (at measured power/core = 13 dBm)	80	5	350
MCS9, NSS 2 (at measured power/core = 13 dBm)	80	5	620
Receive			
1 Mbps, 1 RX core	20	2.4	79
1 Mbps, 2 RX cores	20	2.4	97
MCS7, HT20 1 RX core[e]	20	2.4	80
MCS7, HT20 2 RX cores[e]	20	2.4	99
MCS15, HT20[e]	20	2.4	110

Table 37. Typical WLAN Power Consumption (Cont.)

Mode	Bandwidth (MHz)	Band (GHz)	V_{BAT} = V_{IO} = 3.3V (mA)
CRS 1 RX core[f]	20	2.4	75
CRS 2 RX cores[f]	20	2.4	93
Receive MCS7, SGI 1 RX core[e]	20	5	89
Receive MCS7, SGI 2 RX cores[e]	20	5	112
Receiver MCS15, SGI[e]	20	5	125
CRS 1 RX core[f]	20	5	80
CRS 2 RX cores[f]	20	5	102
Receive MCS 7, SGI 1 RX core[e]	40	5	110
Receive MCS 7, SGI 2 RX cores[e]	40	5	143
Receive MCS 15, SGI[e]	40	5	170
CRS 1 RX core[f]	40	5	94
CRS 2 RX cores[f]	40	5	125
Receive MCS9, NSS 1, SGI[e]	80	5	150
Receive MCS9, NSS 1, SGI 2 RX cores[e]	80	5	202
Receive MCS9, NSS 2, SGI[e]	80	5	220
CRS 1 RX core[f]	80	5	115
CRS 2 RX cores[f]	80	5	165

a. WL_REG_ON, BT_REG_ON low, no VDDIO.
b. Idle, not associated, or inter-beacon.
c. Beacon Interval = 102.4 ms. Beacon duration = 1 ms @1 Mbps. Average current over three DTIM intervals.
d. Measurements were done on the Broadcom Brix Platform.
e. Duty cycle is 100%. Carrier sense (CS) detect/packet receive.
f. Carrier sense (CCA) when no carrier is present.

17.2 Bluetooth Current Consumption

The Bluetooth current consumption measurements are listed in Table 38.

Note:

- The WLAN core is in reset (WL_REG_ON = low) for all measurements provided in Table 38.
- The BT current consumption numbers are measured based on:
  - TGFSK TX output power = 12 dBm.
  - VBAT at 3.3V
  - VIO at 3.3V

Table 38. Bluetooth Current Consumption

Operating Mode	VBAT = VIO = 3.3V (mA)
Sleep with external LPOs	1.0
Standard 1.28s inquiry scan	1.2
Standard R1 page and 1.28s inquiry scan	1.3
500 ms sniff att = 4 master	1.2
500 ms sniff att = 4 slave	1.2
DM1/DH1 master TX/RX	25.5
DM3/DH3 master TX/RX	30.9
DM5/DH5 master TX/RX	31.8
3DH1 master TX/RX	23.2
3DH5 master TX/RX	29.5
3DH5 slave TX/RX	29.3
HV3 master (500 ms sniff)	11.7
2EV3 master (500 ms sniff)	8.4
HV3 slave R1 page and 2.56s inquiry scan	11.9
Transmit 100% on maximum OP BDR	49.8
Receive 100% on	17.4
Passive scan 1.28s	1.2
Adv unconnectable 1.00s	1.1
Adv connectable undirected 1.00s	1.1
Connected 1.00s interval master	1.1

18. Interface Timing and AC Characteristics

18.1 PCI Express Interface Parameters

Table 39. PCI Express Interface Parameters

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
General						
Baud rate	BPS	–	–	5	–	Gbaud
Reference clock amplitude	Vref	LVPECL, AC coupled	1	–	–	V
Receiver						
Differential termination	ZRX-DIFF-DC	Differential termination	80	100	120	Ω
DC impedance	ZRX-DC	DC common-mode impedance	40	50	60	Ω
Powered down termination (POS)	ZRX-HIGH-IMP-DC-POS	Power-down or RESET high impedance	100k	–	–	Ω
Powered down termination (NEG)	ZRX-HIGH-IMP-DC-NEG	Power-down or RESET high impedance	1k	–	–	Ω
Input voltage	VRX-DIFFp-p	AC coupled, differential p-p	175	–	–	mV
Jitter tolerance	TRX-EYE	Minimum receiver eye width	0.4	–	–	UI
Differential return loss	RLRX-DIFF	Differential return loss	10	–	–	dB
Common-mode return loss	RLRX-CM	Common-mode return loss	6	–	–	dB
Unexpected electrical idle enter detect threshold integration time	TRX-IDEL-DET-DIFF-ENTERTIME	An unexpected electrical idle must be recognized no longer than this time to signal an unexpected idle condition.	–	–	10	ms
Signal detect threshold	VRX-IDLE-DET-DIFFp-p	Electrical idle detect threshold	65	–	175	mV
Transmitter						
Output voltage	VTX-DIFFp-p	Differential p-p, programmable in 16 steps	0.8	–	1200	mV
Output voltage rise time	VTX-RISE	20% to 80%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	–	–	UI
Output voltage fall time	VTX-FALL	80% to 20%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	–	–	UI
RX detection voltage swing	VTX-RCV-DETECT	The amount of voltage change allowed during receiver detection.	–	–	600	mV
TX AC peak common-mode voltage (5 GT/s)	VTX-CM-AC-PP	TX AC common mode voltage (5 GT/s)	–	–	100	mV
TX AC peak common-mode voltage (2.5 GT/s)	VTX-CM-AC-P	TX AC common mode voltage (2.5 GT/s)	–	–	20	mV
Absolute delta of DC common-model voltage during L0 and electrical idle	VTX-CM-DC-ACTIVE-IDLE-DELTA	Absolute delta of DC common-model voltage during L0 and electrical idle.	0	–	100	mV

Table 39. PCI Express Interface Parameters (Cont.)

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
Absolute delta of DC common-model voltage between D+ and D-	VTX-CM-DC-LINE-DELTA	DC offset between D+ and D-	0	–	25	mV
Electrical idle differential peak output voltage	VTX-IDLE-DIFF-AC-p	Peak-to-peak voltage	0	–	20	mV
TX short circuit current	ITX-SHORT	Current limit when TX output is shorted to ground.	–	–	90	mA
DC differential TX termination	ZTX-DIFF-DC	Low impedance defined during signaling (parameter is captured for 5.0 GHz by RLTX-DIFF)	80	–	120	Ω
Differential return loss	RLTX-DIFF	Differential return loss	10 (min) for 0.05: 1.25 GHz	–	–	dB
Common-mode return loss	RLTX-CM	Common-mode return loss	6	–	–	dB
TX eye width	TTX-EYE	Minimum TX eye width	0.75	–	–	UI

19. Power-Up Sequence and Timing

19.1 Sequencing of Reset and Regulator Control Signals

The CYW43570 has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states (see Figure 26, Figure 27, Figure 28 and Figure 29). The timing values indicated are minimum required values; longer delays are also acceptable.

19.1.1 Description of Control Signals

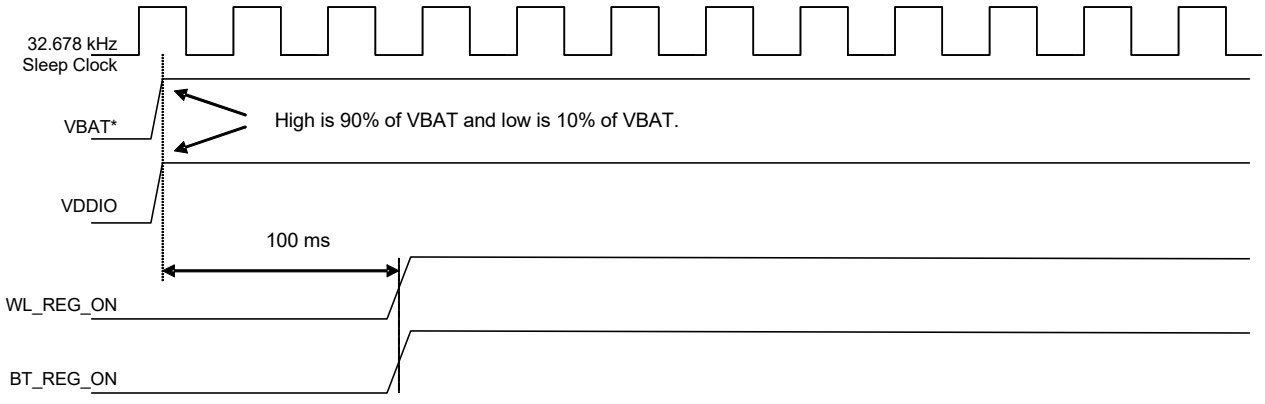
- **WL_REG_ON**: Used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal CYW43570 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.
- **BT_REG_ON**: Used by the PMU (OR-gated with WL_REG_ON) to power up the internal CYW43570 regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset.

Note:

- For both the WL_REG_ON and BT_REG_ON pins, there should be at least a 10 ms time delay between consecutive toggles (where both signals have been driven low). This is to allow time for the CBUCK regulator to discharge. If this delay is not followed, then there may be a VDDIO in-rush current on the order of 36 mA during the next PMU cold start.
- The CYW43570 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold.
- VBAT should not rise 10%–90% faster than 40 microseconds. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

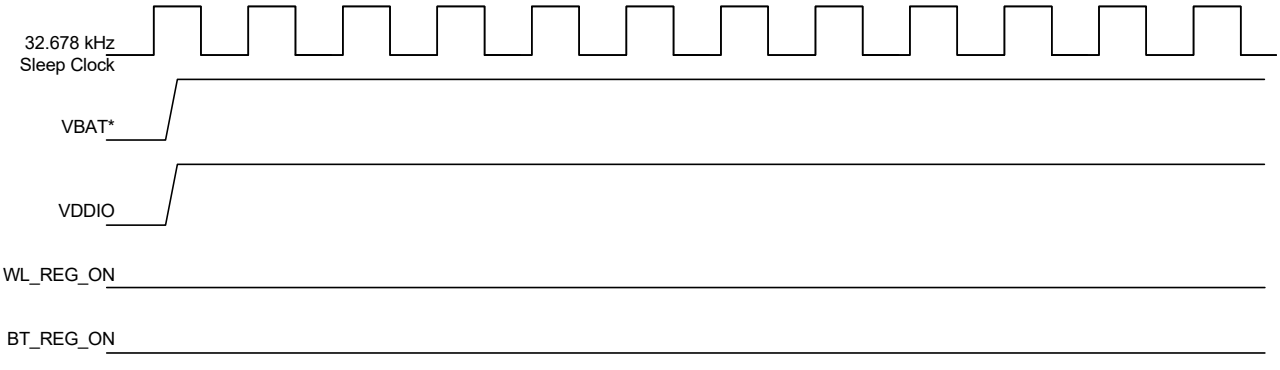
19.1.2 Control Signal Timing Diagrams

Figure 26. WLAN = ON, Bluetooth = ON



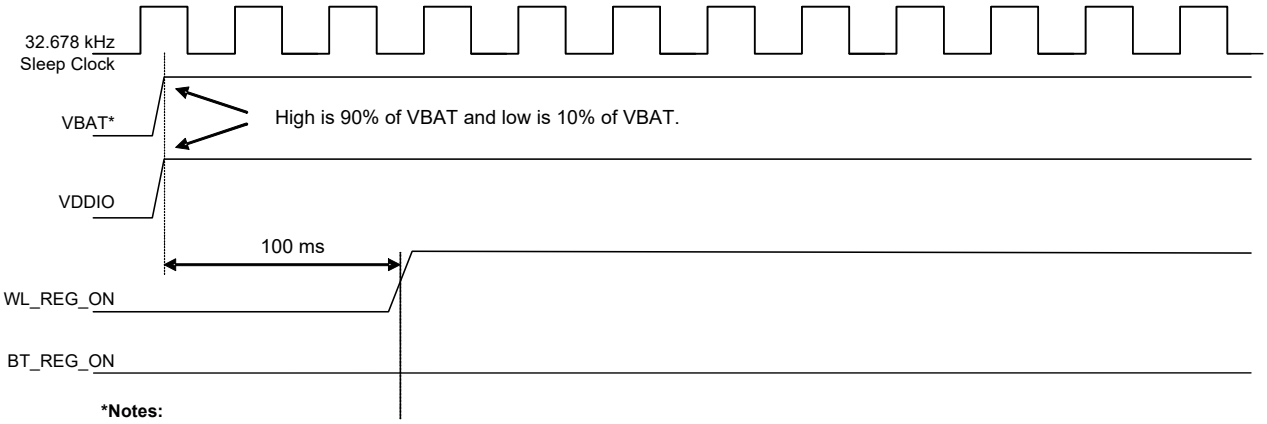
***Notes:**
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.
3. Reset control signal timing for warm boot (high/low/high on REG_ON) is 100 ms and for cold power-on (low/high) is 10 ms.

Figure 27. WLAN = OFF, Bluetooth = OFF



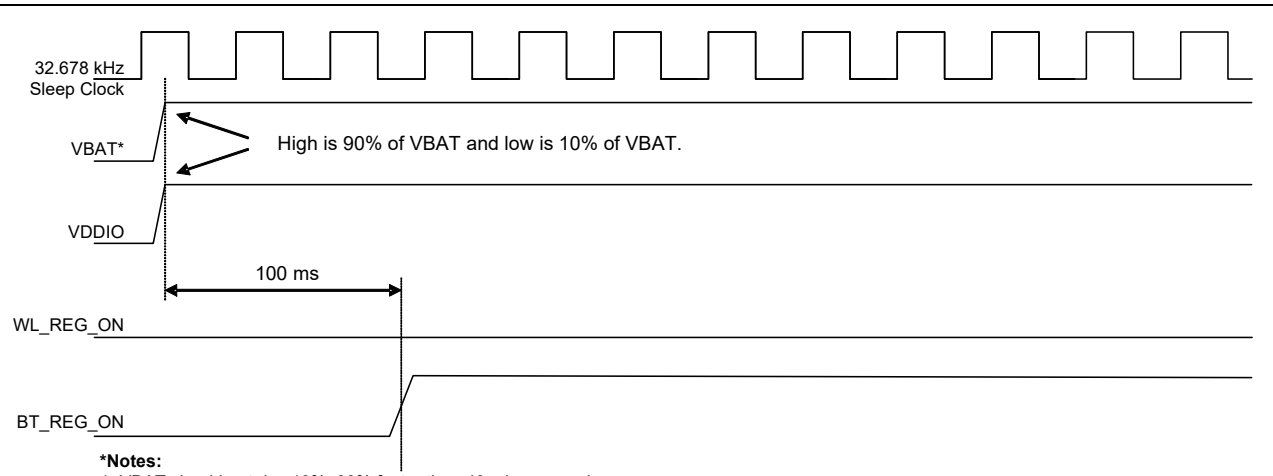
***Notes:**
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 28. WLAN = ON, Bluetooth = OFF



***Notes:**
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.
3. Reset control signal timing for warm boot (high/low/high on REG_ON) is 100 ms and for cold power-on (low/high) is 10 ms.

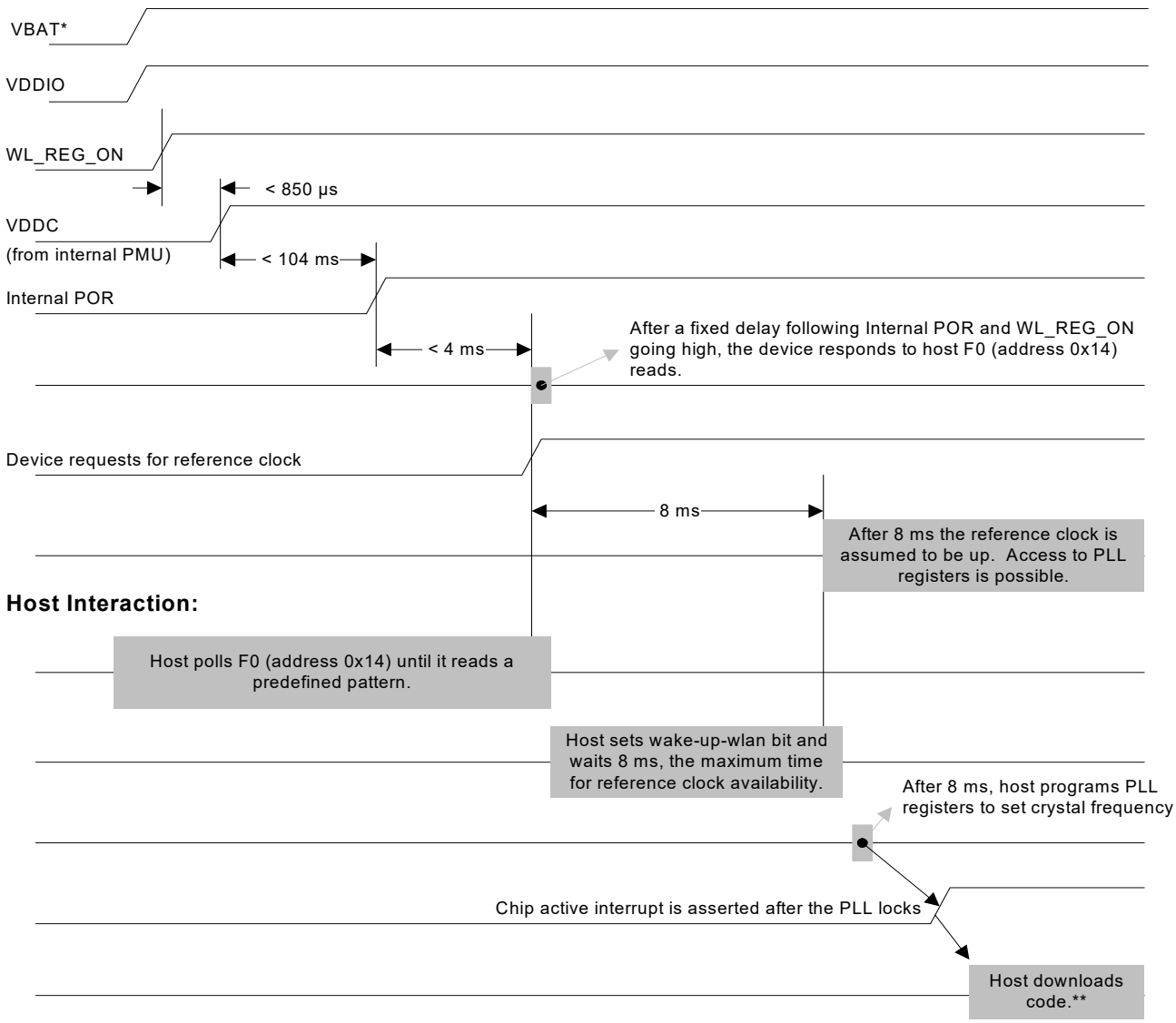
Figure 29. WLAN = OFF, Bluetooth = ON



***Notes:**
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.
3. Reset control signal timing for warm boot (high/low/high on REG_ON) is 100 ms and for cold power-on (low/high) is 10 ms.

Figure 30 shows the WLAN boot sequence from power-up to firmware download.

Figure 30. WLAN Boot Sequence

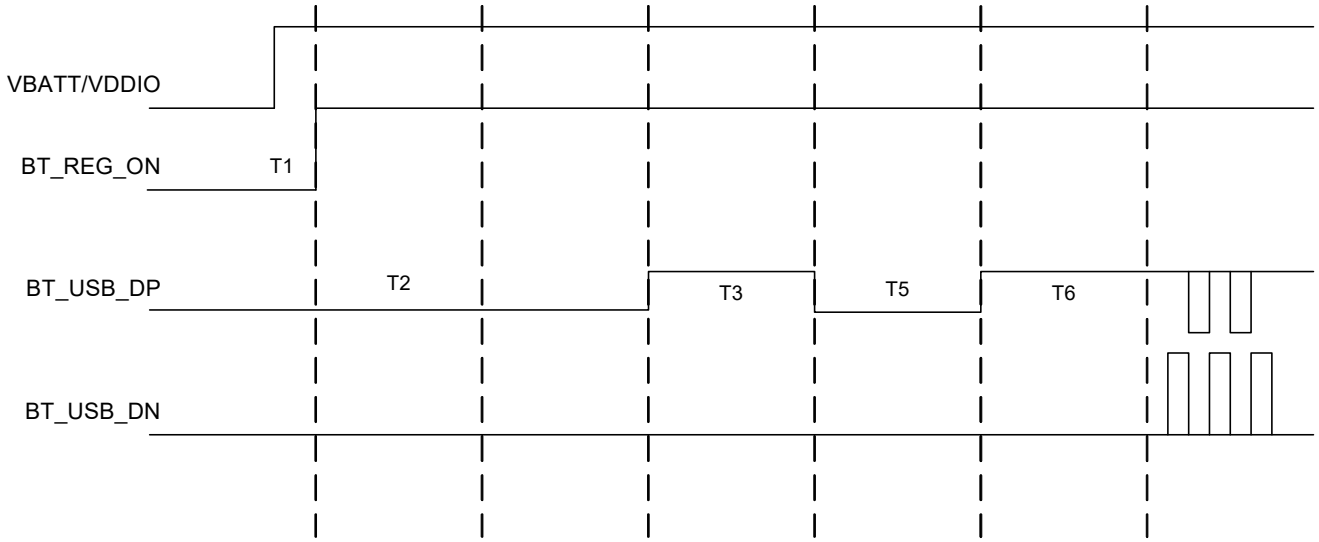


***Notes:**
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.
3. For timing information of the host interaction (after asserting WL_REG_ON) to be ready for firmware download is typically 124 ms, including POR.
4. Wi-Fi FW download depends on the system performance and memory available. Typically, the firmware download on a FC19 Linux PC is 102 ms.

****Note:**
1. Host download code is typically ~102 ms, but it also depends on the size of the firmware. After the firmware download is complete, it is recommended to wait an additional 250 ms before host can issue control commands to a dongle.

Figure 31 shows the Bluetooth boot-up sequence from power-up to firmware download.

Figure 31. Bluetooth Boot-Up Sequence



Notes:
T1: Reset control signal timing ~100 ms.
T2: BT POR and FW ROM boot time, before BT enables USB D+ pull-up to connect the device to the host, ranges from 100 ms (ROM boot) to 250 ms (depends on the size of FW download, based on Broadcom qualified BT Sflash).
T3: > 100 ms USB connection de-bounce time on the host side.
T5: > 10 ms Host drives USB reset.
T6: > 10 ms Host sends USB SOF packet.
After T6: Device is ready to communicate with the host.

20. Package Information

20.1 Package Thermal Characteristics

Table 40. Package Thermal Characteristics[a]

Characteristic	Value
θ_{JA} (°C/W) (value in still air)	26.38
θ_{JB} (°C/W)	8.37
θ_{JC} (°C/W)	9.94
Ψ_{JT} (°C/W)	6.12
Ψ_{JB} (°C/W)	12.62
Maximum Junction Temperature T_j (°C)	125
Maximum Power Dissipation (W)	2.46

a. No heat sink, TA = 70°C. This is an estimate, based on a 4-layer PCB that conforms to EIA/JESD51–7 (101.6 mm × 101.6 mm × 1.6 mm) and P = 1.53W continuous dissipation.

20.2 Junction Temperature Estimation and PSI_{JT} Versus $Theta_{JC}$

The package thermal characterization parameter PSI_{JT} (Ψ_{JT}) yields a better estimation of actual junction temperature (T_J) than using the junction-to-case thermal resistance parameter $Theta_{JC}$ (θ_{JC}). The reason for this is that θ_{JC} is based on the assumption that all the power is dissipated through the top surface of the package case. In actual applications, however, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account the power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is:

$$T_J = T_T + P \times \Psi_{JT}$$

Where:

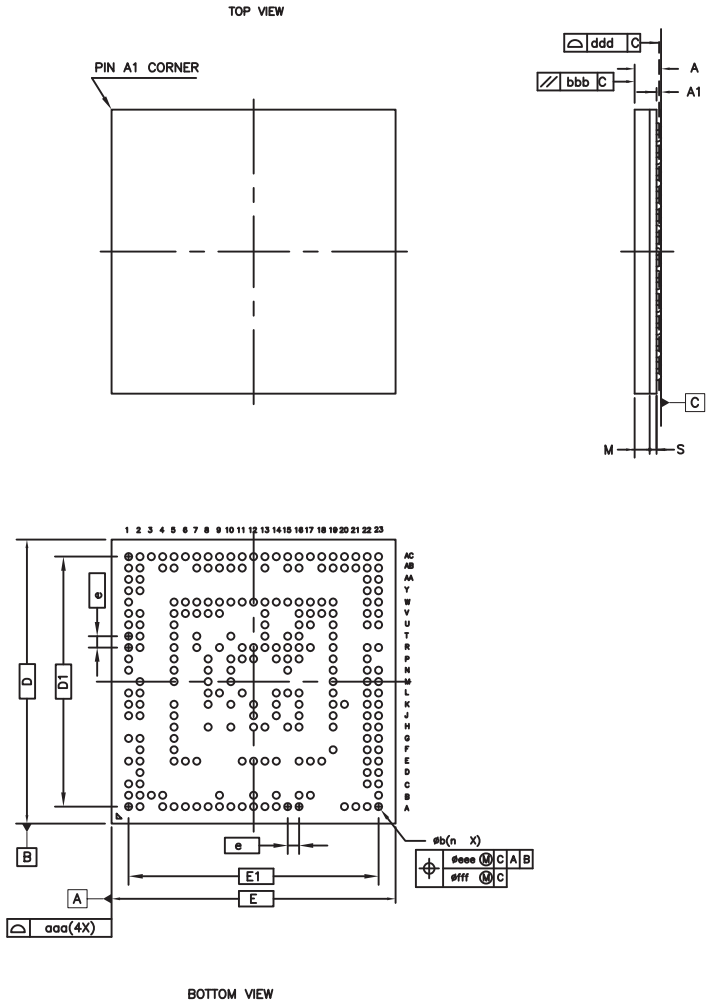
- T_J = Junction temperature at steady-state condition (°C)
- T_T = Package case top center temperature at steady-state condition (°C)
- P = Device power dissipation (Watts)
- Ψ_{JT} = Package thermal characteristics; no airflow (°C/W)

20.3 Environmental Characteristics

For environmental characteristics data, see Table 22.

21. Mechanical Information

Figure 32. 242-Ball Package Mechanical Information



		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :				MFC TFBGA	
Body Size:	X	E		10.000	
	Y	D		10.000	
Ball Pitch :		e		0.400	
Total Thickness :		A			1.05
Mold Thickness :		M		0.530 Ref.	
Substrate Thickness :		S		0.240 Ref.	
Ball Diameter :				0.250	
Stand Off :		A1	0.110	–	0.210
Ball Width :		b	0.200	–	0.300
Package Edge Tolerance :		aaa		0.100	
Mold Parallelism :		bbb		0.100	
Coplanarity:		ddd		0.080	
Ball Offset (Package) :		eee		0.150	
Ball Offset (Ball) :		fff		0.080	
Ball Count :		n		242	
Edge Ball Center to Center :	X	E1		8.800	
	Y	D1		8.800	

22. Ordering Information

Part Number[a]	Package	Description	Operating Ambient Temperature
BCM43570KFFBG	242-ball FCBGA (10 mm × 10 mm, 0.4 mm pitch)	Dual-band 2.4 GHz and 5 GHz WLAN + Bluetooth 4.1 + EDR	0°C to +60°C (32°F to 140°F)

a. Add “T” at the end of the part number to specify “Tape and Reel”.

23. Additional Information

23.1 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

For a comprehensive list of acronyms and other terms used in Cypress documents, go to: http://www.cypress.com/glossary

23.2 References

The references in this section may be used in conjunction with this document.

Note: Cypress provides customer access to technical documentation and software through its Cypress Developer Community and Downloads and Support site (see IoT Resources).

For Cypress documents, replace the “xx” in the document number with the largest number available in the repository to ensure that you have the most current version of the document.

Document (or Item) Name	Number	Source
Bluetooth MWS Coexistence 2.wire Transport Interface Specification	–	www.bluetooth.com
PCI Express Base Specification v2.0.	–	www.pcisig.com

24. IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

Document History

Document Title: CYW43570 Single-Chip 5G WiFi IEEE 802.11ac 2×2 MAC/Baseband/Radio with Integrated Bluetooth 4.1 and EDR Document Number: 002-15054				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	04/02/2014	43570-DS100-R Initial release
*A	–	–	04/14/2014	43570-DS101-R **Updated:** • Section 22. Ordering Information
*B	–	–	07/02/2014	43570-DS102-R **Updated:** • Table 18. Pin List • Table 19. Signal Descriptions
*C	–	–	07/11/2014	43570-DS103-R **Updated:** • Table 37. Typical WLAN Power Consumption • Table 38. Bluetooth BLE and FM Current Consumption
*D	–	–	07/29/2014	43570-DS104-R **Updated:** • Table 5. Power Control Pin Description • Figure 5. Startup Signaling Sequence • Table 6. SPI-to-UART Signal Mapping • Figure 32. 242-Ball Package Mechanical Information • PCM Interface Timing • Table 15. UART Timing Specifications • Figure 16. UART Timing • Figure 32. 242-Ball Package Mechanical Information **Added:** • Table 6. PCM-to-Serial Flash Interface Mapping
*E	–	–	08/03/2015	43570-DS105-R **Updated:** • General Description and Features • Figure 1. Functional Block Diagram for PCIe (WLAN) and BT (USB 2.0) Interfaces • Table 2. Device Interface Support • Figure 2. CYW43570/E Block Diagram • CYW43570/E PMU Features • UART/USB Transport Detection • USB Interface • Table 17. Strapping Options PCIe • Table 20. BT GPIO Functions and Strapping Options • Table 24. Bluetooth Receiver RF Specifications • Table 28. 2.4 GHz Band General RF Specifications • Table 29. WLAN 2.4 GHz Receiver Performance Specifications through Table 32. WLAN 5 GHz Transmitter Performance Specifications • Table 37. Typical WLAN Power Consumption • Table 38. Bluetooth Current Consumption • Bluetooth Current Consumption • Figure 26. WLAN = ON, Bluetooth = ON • Figure 27. WLAN = OFF, Bluetooth = OFF • Figure 28. WLAN = ON, Bluetooth = OFF • Figure 29. WLAN = OFF, Bluetooth = ON • Figure 30. WLAN Boot Sequence • Table 40. Package Thermal Characteristics **Added:** • Figure 31. Bluetooth Boot-Up Sequence • Note: VBAT is the main power supply (ranges from 3.0V to 3.6V) to the chip.
*F	–	–	01/05/2016	43570-DS106-R **Updated:** • Figure 1. Functional Block Diagram for PCIe (WLAN) and BT (USB 2.0) Interfaces • SPI/UART Transport Detection

Document Title: CYW43570 Single-Chip 5G WiFi IEEE 802.11ac 2×2 MAC/Baseband/Radio with Integrated Bluetooth 4.1 and EDR Document Number: 002-15054				
*G	–	–	02/19/2016	43570-DS107-R **Updated:** • Table 21. Absolute Maximum Ratings • Table 23. Recommended Operating Conditions and DC Characteristics • Table 33. Core Buck Switching Regulator (CBUCK) Specifications • Table “LDO3P3 Specifications” • Table 34. BTLDO2P5 Specifications
*H	–	–	03/10/2016	43570-DS108-R **Updated:** • Section 13. DC Characteristics • Table 33. Core Buck Switching Regulator (CBUCK) Specifications • Table 34. BTLDO2P5 Specifications **Removed:** • Table “LDO3P3 Specifications”
*I	5491700	UTSV	10/27/2016	Updated to Cypress Template. Added Cypress Part Numbering Scheme.
*J	5968648	AESATP12	11/16/2017	Updated logo and copyright.
*K	6346984	KRIS	10/12/2018	Added a footnote: Add “T” at the end of the part number to specify “Tape and Reel” in Ordering Information section.

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