Mighty Gecko Wireless SoC
EFR32MG1X232 Data Sheet

The Mighty Gecko family of wireless solutions combines an energy-friendly MCU with a highly integrated radio transceiver supporting Bluetooth Smart®, wireless mesh, and proprietary short range wireless protocols.

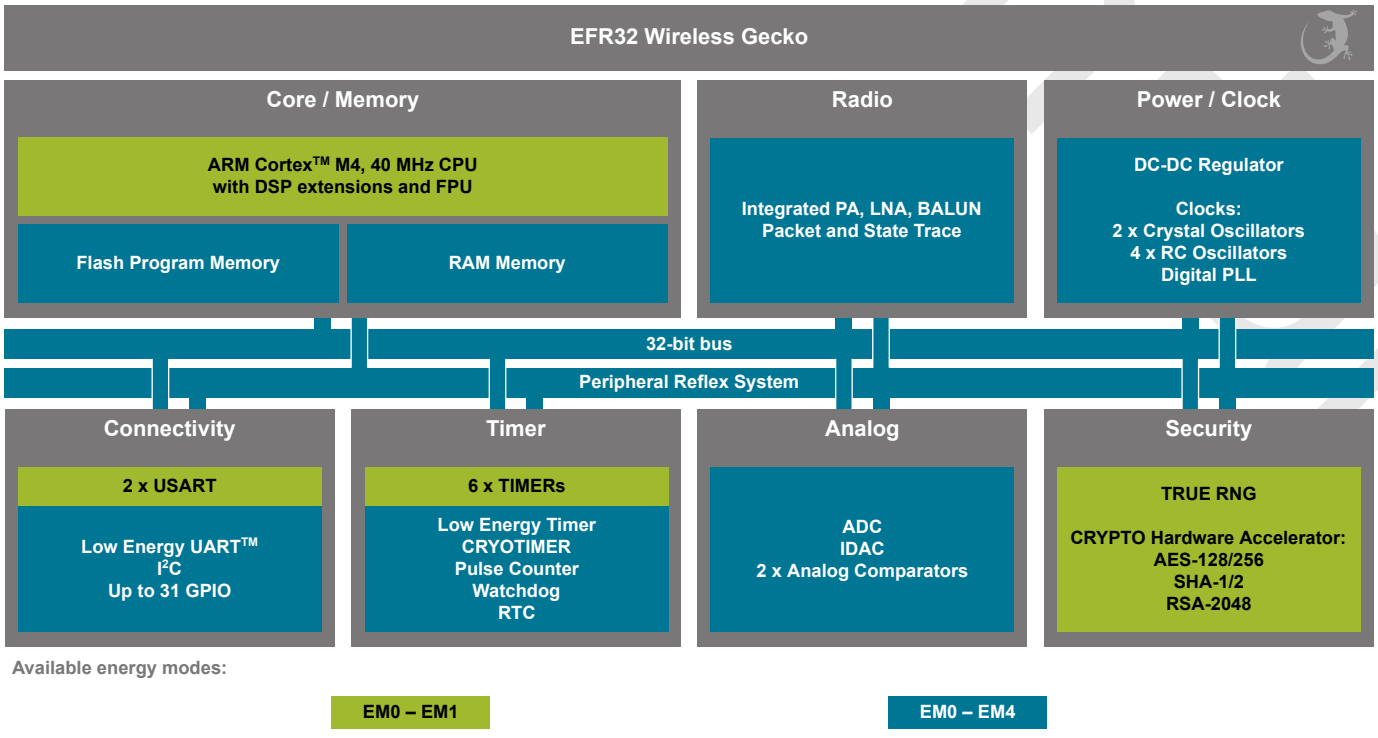
The IoT System-On-Chip provides industry-leading energy efficiency, ultra-fast wakeup times, a scalable power amplifier, an integrated balun and no-compromise MCU features.

Mighty Gecko applications include

- Connected Home
- Lighting
- Sports and Fitness
- Metering
- Building Automation

KEY FEATURES

- 32-bit ARM® Cortex®-M4 core with 40 MHz maximum operating frequency
- Low energy active and sleep currents
- Scalable Memory and Radio configuration options available in several footprint compatible QFN packages
- 12-channel Peripheral Reflex System enabling autonomous interaction of MCU peripherals
- Autonomous Hardware Crypto Accelerator and True Random Number Generator



1. Features

- **Low Power Wireless System-on-Chip**.
  - High Performance 32-bit 40 MHz ARM Cortex-M4 with DSP instruction and floating-point unit for efficient signal processing
  - Up to 256 kB flash program memory
  - Up to 32 kB RAM data memory
  - 2.4 GHz radio operation
  - TX power up to 19.5 dBm
- **Low Energy Consumption**
  - 8.6 mA RX current at 2.4 GHz (1 Mbps GFSK)
  - 9.1 mA RX current at 2.4 GHz (250 kbps O-QPSK DSSS)
  - 8.2 mA TX current @ 0 dBm output power at 2.4 GHz
  - 60 µA/MHz in Energy Mode 0 (EM0)
  - 1.35 µA EM2 DeepSleep current (full RAM retention and RTCC running from LFXO)
  - 1 µA EM3 Stop current (State/RAM retention)
  - Wake on Radio with signal strength detection, preamble pattern detection, frame detection and timeout
- **High Receiver Performance**
  - -94 dBm sensitivity at 1 Mbps GFSK
  - -99.4 dBm sensitivity at 250 kbps O-QPSK DSSS
- **Modulation Format(s) Supported**
  - 2-FSK / 4-FSK with fully configurable shaping
  - Shaped OQPSK / (G)MSK
- **Supported Protocol(s)**
  - Bluetooth Smart
  - ZigBee®
  - Thread
  - 2.4 GHz Proprietary Protocols
- **Wide selection of MCU peripherals**
  - 12-bit 1 Msamples/s SAR Analog to Digital Converter
  - 2× Analog Comparator
  - Digital to Analog Current Converter (IDAC)
  - Up to 31 pins connected to analog channels (APORT) shared between Analog Comparators, ADC, and IDAC
  - 31 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller
  - 12 Channel Peripheral Reflex System (PRS)
  - Hardware Crypto Acceleration with public key support
  - 2×16-bit Timer/Counter
    - 3 + 4 Compare/Capture/PWM channels
  - 32-bit Real Time Counter and Calendar
  - 16-bit Low Energy Timer for waveform generation
  - 32-bit Ultra Low Energy Timer/Counter for periodic wake-up from any Energy Mode
  - 16-bit Pulse Counter with asynchronous operation
  - Watchdog Timer with dedicated RC oscillator @ 50 nA
  - 2×Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/I^2S)
  - Low Energy UART (LEUART™)
  - I^2C interface with SMBus support and address recognition in EM3 Stop
- **Wide Operating Range**
  - 1.62 V to 3.8 V single power supply
  - -40 °C to 85 °C
- **QFN48 7x7 mm Package**

2. Ordering Information

Ordering Code	Frequency Band	Core	Flash (kB)	RAM (kB)	Protocol Stack	Encryption	Max TX Power (dBm)
EFR32MG1P232F256GM48-A0	2.4 GHz	M4	256	32	• Bluetooth Smart • ZigBee/Thread • ZigBee RC • Proprietary	Full	19.5
EFR32MG1P232F256GM48-B0	2.4 GHz	M4	256	32	• Bluetooth Smart • ZigBee/Thread • ZigBee RC • Proprietary	Full	19.5
EFR32MG1B232F256GM48-B0	2.4 GHz	M4	256	32	• ZigBee/Thread • ZigBee RC	Full	19.5

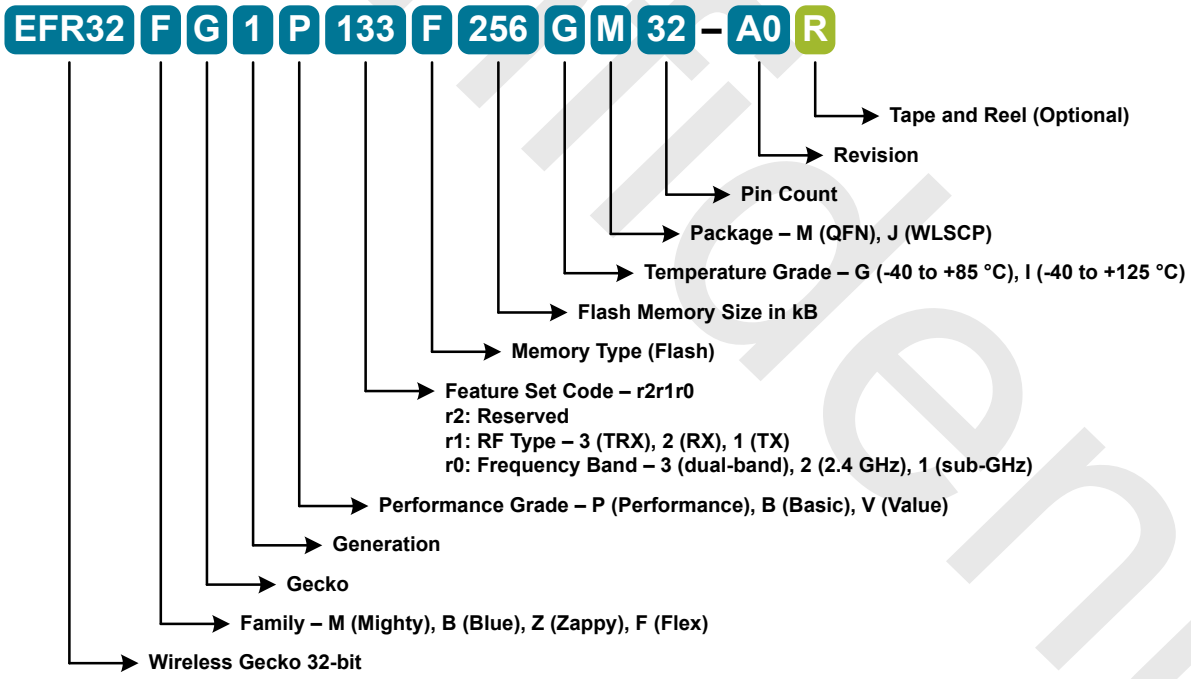


Figure 2.1. OPN Decoder

3. System Overview

3.1 Introduction

The EFR32 product family features the world's most energy friendly System-on-Chip radios. The devices are well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the full radio and MCU system. The detailed functional description can be found in the EFR32 Reference Manual.

3.2 Block Diagram

A block diagram of the EFR32MG1X232 is shown in Figure 3.1 Block Diagram on page 3.

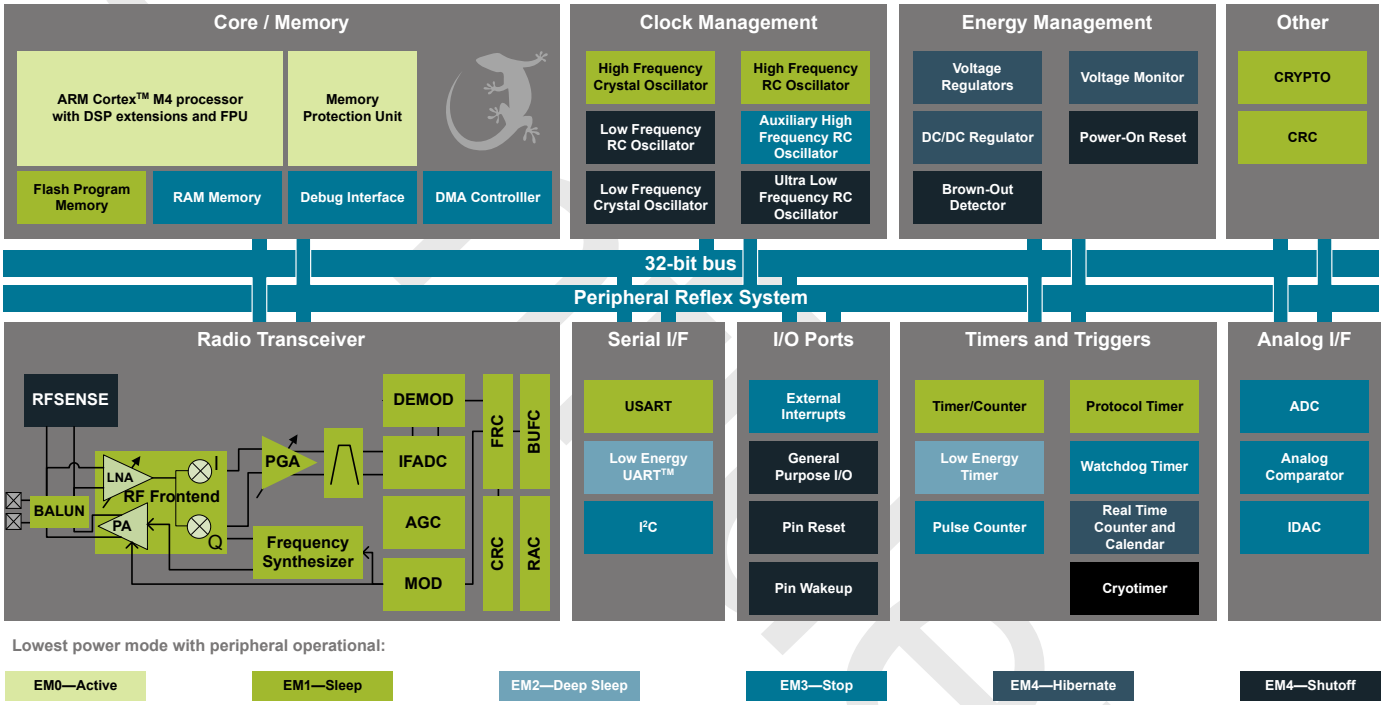


Figure 3.1. Block Diagram

3.3 System Description

3.3.1 Antenna interface

The 2.4 GHz antenna interface consists of two pins (2GRF_IOP and 2GRF_ION) that interface directly to the on-chip BALUN. The 2GRF_ION pin should be grounded externally.

The external components and power supply connections for the antenna interface in a typical application are shown in Section 5. Application Circuits.

3.3.2 Integrated Oscillators

The EFR32MG1X232 supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the radio and MCU. Crystal frequencies in the range from 38 to 40 MHz are supported. Silicon Laboratories reference designs employ a crystal frequency of 38.4 MHz. An external clock source such as a TCXO can also be applied to the HFXO input for improved accuracy over temperature.
- An optional 32.768 kHz crystal oscillator (LFXO) can be used as an accurate timing reference in low energy modes.
- A 32.768 kHz crystal oscillator (LFXO) should be used as an accurate timing reference in Bluetooth Smart low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range.
- An integrated auxilliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire debug port with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.3.3 Fractional-N Frequency Synthesizer

The EFR32MG1X232 contains a high performance, low phase noise, fully integrated fractional-N frequency synthesizer. The synthesizer is used in receive mode to generate the LO frequency used by the down-conversion mixer. It is also used in transmit mode to directly generate the modulated RF carrier.

The fractional-N architecture provides excellent phase noise performance combined with frequency resolution better than 100 Hz, with low energy consumption. The synthesizer has fast frequency settling which allows very short receiver and transmitter wake up times to optimize system energy consumption.

3.3.4 Receiver Architecture

The EFR32MG1X232 uses a low-IF receiver architecture, consisting of a Low-Noise Amplifier (LNA) followed by an I/Q down-conversion mixer, emplying a 38.4 MHz crystal reference. The I/Q signals are further filtered and amplified before being sampled by the IF analog-to-digital converter (IFADC).

The IF frequency is configurable from 150 kHz to 1371 kHz. The IF can further be configured for high-side or low-side injection, providing flexibility with respect to known interferers at the image frequency.

The Automatic Gain Control (AGC) module adjusts the receiver gain to optimize performance and avoid saturation for excellent selectivity and blocking performance.

Demodulation is performed in the digital domain. The demodulator performs configurable decimation and channel filtering to allow receive bandwidths ranging from 0.1 to 2530 kHz. High carrier frequency and baud rate offsets are tolerated by active estimation and compensation. Advanced features supporting high quality communication under adverse conditions include forward error correction by block and convolutional coding as well as Direct Sequence Spread Spectrum (DSSS).

A Received Signal Strength Indicator (RSSI) is available for signal quality metrics, for level-based proximity detection, and for RF channel access by Collision Avoidance (CA) or Listen Before Talk (LBT) algorithms. An RSSI capture value with dB resolution is associated with each received frame and the dynamic RSSI measurement can be monitored throughout reception.

The EFR32MG1X232 features integrated support for antenna diversity to improve link budget, using complementary control outputs to an external switch. Internal configurable hardware controls automatic switching between antennae during RF receive detection operations.

In typical applications, the demodulator output is stored in internal buffer memory for access by the MCU. Direct mode supports direct serial output of demodulated data on configured GPIO pins.

3.3.5 Transmitter Architecture

The EFR32MG1X232 uses a direct-conversion transmitter architecture. For constant envelope modulation formats, the modulator controls phase and frequency modulation in the frequency synthesizer. Transmit symbols or chips are optionally shaped by a digital shaping filter. The shaping filter is fully configurable, including the BT product, and can be used to implement Gaussian or Raised Cosine shaping.

Automated PA up and down ramping is applied to each transmitted frame, in order to ensure the Adjacent Channel Power (ACP) meets regulatory requirements.

Carrier Sense Multiple Access - Collision Avoidance (CSMA-CA) or Listen Before Talk (LBT) algorithms can be automatically timed by the EFR32MG1X232. These algorithms are typically defined by regulatory standards to improve inter-operability in a given bandwidth between devices that otherwise lack synchronized RF channel access.

3.3.6 Wake on Radio

The Wake on Radio feature allows flexible, autonomous RF sensing, qualification, and demodulation without required MCU activity, using a subsystem of the EFR32MG1X232 including the Radio Controller (RAC), Peripheral Reflex System (PRS), and Low Energy peripherals. Wake on Radio implementation may typically include the following functionality:

- Periodic trigger to start RF evaluation from the RTCC, GPIO or other low energy peripherals
- Received Signal Strength Indicator (RSSI) qualification
- Preamble and frame sync qualification
- Frame header qualification, including address filtering
- Autonomous packet demodulation and buffering
- Optional transfer of RSSI values to RAM via DMA
- Timeout to disable the receiver through the PRS in case of false alarm

3.3.7 RFSENSE

The RFSENSE module generates a system wakeup interrupt upon detection of wideband RF energy at the antenna interface, providing true RF wakeup capabilities from low energy modes including EM2, EM3 and EM4.

RFSENSE triggers on a relatively strong RF signal and is available in the lowest energy modes, allowing exceptionally low energy consumption. RFSENSE does not demodulate or otherwise qualify the received signal, but software may respond to the wakeup event by enabling normal RF reception.

Various strategies for optimizing power consumption and system response time in presence of false alarms may be employed using available timer peripherals.

3.3.8 Flexible Frame Handling

EFR32MG1X232 has an extensive and flexible frame handling support for easy implementation of even complex communication protocols. The Frame Controller (FRC) supports all low level and timing critical tasks together with the Radio Controller and Modulator/Demodulator:

- Highly adjustable preamble length
- Up to 2 simultaneous synchronization words, each up to 32 bits and providing separate interrupts
- Frame disassembly and address matching (filtering) to accept or reject frames
- Automatic ACK frame assembly and transmission
- Fully flexible CRC generation and verification:
  - Multiple CRC values can be embedded in a single frame
  - 8, 16, 24 or 32-bit CRC value
  - Configurable CRC bit and byte ordering
- Selectable bit-ordering (least significant or most significant bit first)
- Optional data whitening
- Optional Forward Error Correction (FEC), including convolutional encoding / decoding and block encoding / decoding
- Half rate convolutional encoder and decoder with constraint lengths from 2 to 7 and optional puncturing
- Fully configurable block codes for sub-GHz protocols, supporting both linear codes and table based lookup (e.g. Wireless M-bus 3-out-of-6 coding)
- Optional symbol interleaving, typically used in combination with FEC
- Symbol coding, such as Manchester or DSSS, supported in the MODEM, or biphase space encoding using FEC hardware
- UART encoding over air, with start and stop bit insertion / removal
- Test mode support, such as modulated or unmodulated carrier output
- Received frame timestamping

3.3.9 Packet and State Trace

The EFR32MG1X232 Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data and state information
- Data observability on a single-pin UART data output, or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data and state / meta information in a single serial data stream

3.3.10 Data Buffering

The EFR32MG1X232 features an advanced buffer controller (BUFC) capable of handling up to 4 buffers of adjustable size from 64 bytes to 4096 bytes. Each buffer can be used for RX, TX or both. The buffer data is located in RAM, enabling zero-copy operations.

3.3.11 Radio Controller (RAC)

The Radio Controller controls the top level state of the radio subsystem in the EFR32MG1X232. It performs the following tasks:

- Precisely-timed control of enabling and disabling of the receiver and transmitter circuitry
- Run-time calibration of receiver, transmitter and frequency synthesizer
- Detailed frame transmission timing, including optional LBT or CSMA-CA

3.3.12 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. EFR32 devices support various levels of hardware-accelerated encryption, depending on the part. Section 2. Ordering Information specifies whether this part has **full** or **AES-only** crypto support. AES-only devices support AES encryption and decryption with 128- or 256-bit keys. Full crypto support adds RSA-2048, ECC over both GF(P) and GF(2^m), SHA-1 and SHA-2.

Supported modes of operation for AES includes ECB, CTR, CBC, PCBC, CFB, OFB, CBC-MAC, GMAC, CCM and GCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO is tightly linked to the BUFC enabling fast and efficient autonomous cipher operations on data buffer content. It allows fast processing of ECC, RSA and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

3.3.13 True Random Number Generator

The Frame Controller (FRC) implements a true random number generator that extracts noise from the RF receive chain. Data can be read from a register 32 bits at a time, or larger blocks of random data can be written directly to RAM.

Output from the random number generator can be used either directly or as a seed or entropy source for software based random number generator algorithms such as Fortuna.

3.3.14 System Processor

The ARM Cortex-M processor subsystem integrates the following features and tasks in the system:

- 32-bit ARM Cortex-M RISC processor achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- Up to 256 kB flash program memory
- Up to 32 kB RAM data memory
- Advanced and flexible protocol support, in cooperation with the Frame Controller
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface, which can be disabled

The Cortex-M4 is equipped with DSP instruction support and a floating-point unit (FPU).

3.3.15 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active/EM1 Sleep.

3.3.16 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller features 8 channels capable of performing memory operations independently of software. This reduces both energy consumption and software workload.

3.3.17 Integrated Voltage Regulators

The EFR32MG1X232 generates internal supply voltages from integrated regulators. This means that only a single external supply voltage is required, from which all internal voltages are created. An optional integrated DC-DC buck regulator, further detailed in section 3.3.37 Integrated DC-DC Converter (DC-DC), can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

3.3.18 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFR32MG1X232. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset and watchdog reset.

3.3.19 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available. The EMU can also be used to turn off the power to unused RAM blocks. The EMU also contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has 4 channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.3.20 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFR32MG1X232. Individual enabling and disabling of clocks to all peripheral modules is perfomed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.3.21 Watchdog (WDOG)

The watchdog timer with window monitoring capabilities can monitor the Peripheral Reflex System and generate a reset in case of a system failure to improve application reliability.

3.3.22 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality can be applied by the PRS. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

3.3.23 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I^2S

3.3.24 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

3.3.25 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I^2C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

3.3.26 Protocol Timer (PROTIMER)

The PROTIMER is perfectly suited for radio protocol time-keeping, featuring support for time-slotted and random backoff LBT/CSMA radio access mechanisms. The PROTIMER includes a capture/compare functionality, including several capture registers, configurable to capture counter or RTCC values upon trigger events selected from Peripheral Reflex System events or radio events. The capture register values may be used for received frame timestamping. The compare feature produces output events upon match of captured values to programmed comparison values, which can be used to enable or disable the RF receiver without MCU intervention.

3.3.27 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. Please refer to Section 3.4 Configuration Summary for available TIMER units and features in the EFR32MG1X232

The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.3.28 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators (Section 3.3.2 Integrated Oscillators) with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. When receiving frames, the RTCC value can be used for timestamping. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes.

3.3.29 Low Energy Timer (LETIMER™)

The unique LETIMER, is a 16-bit timer that is available in energy mode EM2 DeepSleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.3.30 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO) or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

3.3.31 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The module may operate in energy mode EM0 Active, EM1 Sleep, EM2 DeepSleep and EM3 Stop.

3.3.32 General Purpose Input/Output (GPIO)

EFR32MG1X232 has 31 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.3.33 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to analog modules ADC, ACMP, and IDAC on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs. See 6.4 Analog Port (APORT) for an illustration of the APORT connections.

3.3.34 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software.

The ACMP can also be used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold.

3.3.35 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 MSamples/s. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples.

The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of source, including pins configurable as either single-ended or differential.

3.3.36 Digital to Analog Current Converter (IDAC)

The Digital to Analog Current Converter can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The current is programmable between 0.05 µA and 64 µA with several ranges with various step sizes.

3.3.37 Integrated DC-DC Converter (DC-DC)

The DC-DC buck converter covers a wide range of load currents and provides high efficiency in energy modes EM0, EM1, EM2 and EM3. Patent-pending RF noise mitigation allows operation of the DC-DC converter without degrading radio sensitivity. The converter has three modes: low noise (LN), low power (LP), and bypass. Each operating mode transition is initiated by firmware and executed by an integrated hardware state machine, providing well-controlled transitions. Bypass mode may be entered when the input voltage is too low for efficient operation of the DC-DC converter. In Bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to avoid dipping the input supply due to excessive current transients.

Key Features:

- Wide load range from sub-µA to 200 mA
- High efficiency up to 90%
- Low Noise (LN), Low Power (LP) and Bypass operating modes for high performance and low energy applications
  - Fast wakeup from LP to LN to support quick EM2 to EM0 transition
  - Low 50 nA quiescent current in LP mode to support micro-ampere range load currents
- Optimized for integration with the on-board radio
  - Switching frequency programmable from 3 MHz to 8 MHz
  - RF noise mitigation mechanism
- Supports wide range of passive part selection
  - External capacitor range from 1 µF to 10 µF with external 4.7 µH inductor
- Protection features
  - Programmable sourcing and sinking current limits
  - Output short-circuit protection
  - Dead-time protection

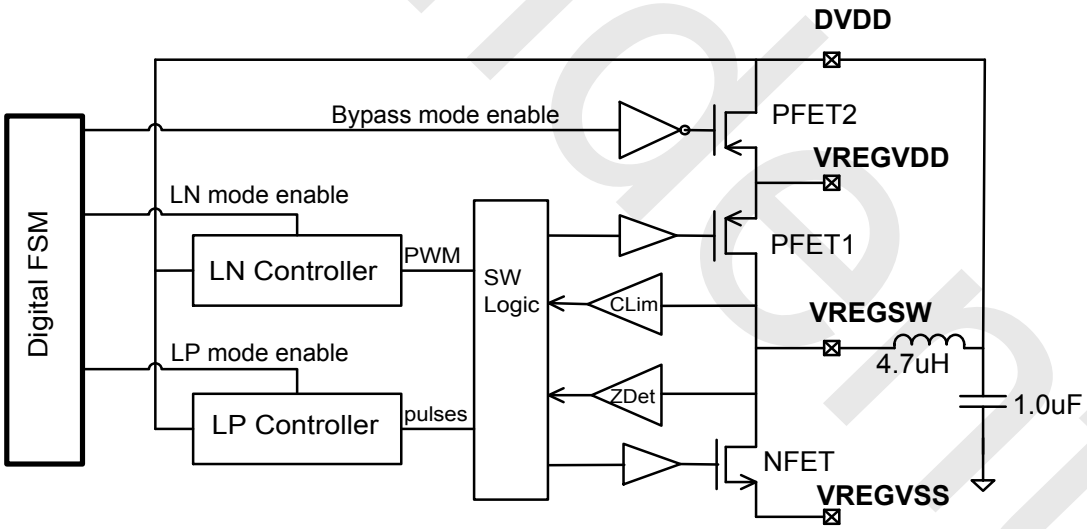


Figure 3.2. Functional Diagram of the DC-DC Converter

3.3.37.1 DC-DC Converter Powertrain

The powertrain consists of low-resistance P-channel (PFET1) and N-channel (NFET) switches, combined with a current limiter and zero-crossing detector. The power switches provide programmable drive strength by selection of a number of slices for each switch. The switching logic takes either a PWM signal from a low-noise controller or pulses from a low-power controller and drives PFET1 and NFET switches using proper dead-time control. The powertrain can switch in both forced Continuous Conduction Mode (CCM) mode and load-adaptive Continuous Conduction/Discontinuous Conduction (CCM/DCM) mode. Load-adaptive CCM/DCM mode has superior efficiency in light load conditions, whereas forced CCM mode provides the best transient response and noise control when the radio is on.

The DC-DC converter includes a current limiter to protect PFET1 from large transient currents. Whenever a current overload is detected, the switching logic advances the transition from PFET1 to NFET and optionally sends an interrupt signal to the processor.

A zero-voltage detector is included to prevent reverse current in DCM mode. When NFET is on and zero voltage is detected across NFET, the switching logic will turn NFET off to prevent reverse current. The zero-voltage detector can be disabled to enable forced CCM mode. It can also be configured as a programmable reverse current limiter.

3.3.37.2 DC-DC Converter Low Noise (LN) Controller

The LN controller consists of an active-RC type-III compensator, a ramp generator and a PWM comparator. The compensator generates an error voltage from on-chip feedback, which is compared against a ramp voltage by the PWM comparator. The resulting PWM signal is duty-cycle limited between 3% and 96%, with circuitry to avoid control-loop lockout. The PWM frequency can be generated from the ramp generator's oscillator or from an external clock from the radio's RF synthesizer. Noise mitigation hardware post-processes the PWM signal to avoid in-band noise coupling into the radio system.

3.3.37.3 DC-DC Converter Low Power (LP) Controller

The LP controller consists of a continuous-time comparator with hysteresis and a constant frequency pulse generator. When the output voltage is lower than the low threshold of the comparator, the pulse generator is enabled to activate the powertrain. The powertrain switches at a constant-frequency with a fixed duty cycle of about 90%. When the DC-DC output exceeds the comparator's high threshold, the pulse generator is disabled until the cycle starts over again on the next low-threshold crossing. The comparator has four programmable response-time settings. The lowest setting consumes only approximately 50nA, providing high-efficiency regulation of current loads down to the micro-ampere range.

3.4 Configuration Summary

The features of the EFR32MG1X232 is a subset of the feature set described in the EFR32 Reference Manual. Table 3.1 Configuration Summary on page 11 describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.1. Configuration Summary

Module	Configuration	Pin Connections
USART0	IrDA I^2S SmartCard	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	IrDA I^2S SmartCard	US1_TX, US1_RX, US1_CLK, US1_CS
TIMER0	with DTI.	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1		TIM1_CC[3:0]

3.5 Memory Map

The **EFR32MG1X232** memory map is shown in the figure below. RAM and flash sizes are for the largest memory configuration.

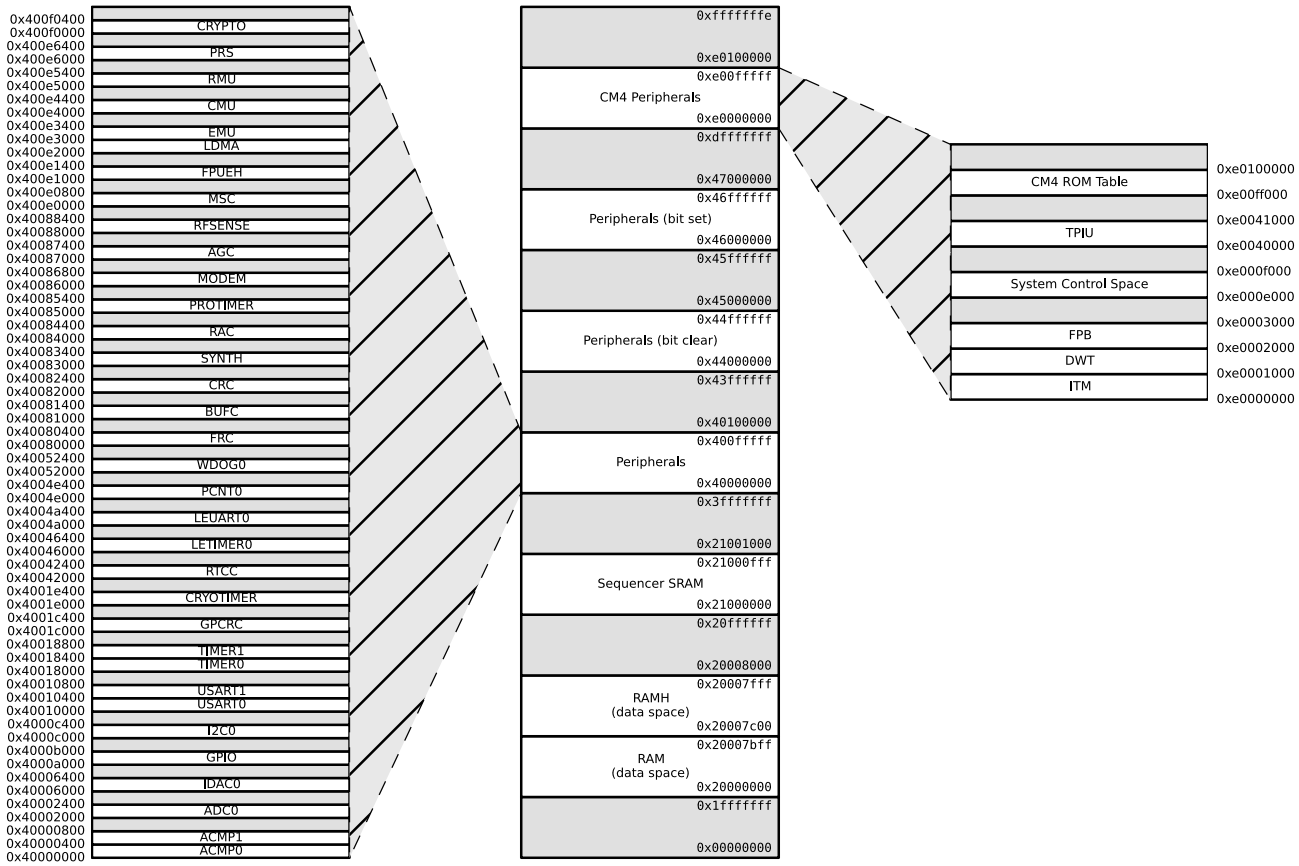


Figure 3.3. EFR32MG1X232 Memory Map

4. Electrical Characteristics

4.1 Test Conditions

4.1.1 Typical Values

Typical values are based on T_{AMB}=25 °C and V_{DD}=3.3 V, as defined in 4.3.1 General Operating Conditions, by production test and/or technology characterization unless otherwise specified.

Radio performance numbers are measured in conducted mode, based on Silicon Labs reference designs using output power-specific external RF impedance-matching networks, further identified in Section 5. Application Circuits, for interfacing to a 50 Ω antenna.

4.1.2 Minimum and Maximum Values

Minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in 4.3.1 General Operating Conditions.

4.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions is not guaranteed. Stress beyond the limits specified in may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in 4.3.1 General Operating Conditions.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-50	-	150	°C
External main supply voltage	V_{DDMAX}		0	-	3.8	V
External main supply voltage ramp rate	$V_{DDRAMPMAX}$		-	-	1	V / µs
Voltage on any 5V tolerant GPIO pin[1]	V_{DIGPIN}		-0.3	-	Min of 5.25 and IOVDD +2	V
Voltage on non-5V tolerant GPIO pins			-0.3	-	IOVDD+0.3	V
Voltage on HFXO pins	$V_{HFXOPIN}$		-0.3	-	1.4	V
Voltage on RF pins 2G4RF_IOP and 2G4RF_ION	V_{MAX2G4}		TBD	-	TBD	V
Total current into V_{SS} ground lines (sink)	I_{VSSMAX}		-	-	TBD	mA
Current per I/O pin (sink)	I_{IOMAX}		-	-	50	mA
Current per I/O pin (source)			-	-	50	mA
Current for all I/O pins (sink)	$I_{IOALLMAX}$		-	-	TBD	mA
Current for all I/O pins (source)			-	-	TBD	mA
Voltage difference between AVDD and VREGVDD	ΔV_{DD}		-	-	0.3	V

Note:
1. When a GPIO pin is routed to the analog module through the APORT, the maximum voltage = IOVDD.

4.3 Operating Conditions

When assigning supply sources, the following requirements must be observed:

- VREGVDD must be the highet voltage in the system
- VREGVDD ≥ AVDD
- VREGVDD ≥ DVDD
- DVDD ≥ PAVDD
- DVDD ≥ DECOUPLE
- AVDD ≥ IOVDD

4.3.1 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient temperature range	T_{AMB}		-40	25	85	°C
VREGVDD Operating supply voltage	$V_{VREGVDD}$		1.62	3.3	3.8	V
RFVDD Operating supply voltage	V_{RFVDD}		1.62	-	V(VREGVDD)	V
AVDD Operating supply voltage	V_{AVDD}	AVDD must be tied to VREGVDD	V(VREGVDD)	-	V(VREGVDD)	V
DVDD Operating supply voltage	V_{DVDD}		1.62	-	V(VREGVDD)	V
PAVDD Operating supply voltage	V_{PAVDD}		1.62	-	3.8	V
IOVDD Operating supply voltage	V_{IOVDD}		1.62	-	V(VREGVDD)	V
DECOUPLE Operating supply voltage	$V_{DECOUPLE}$		1.08	1.2	1.32	V
Difference between AVDD and VREGVDD, ABS(AVDD-VREGVDD)	dV_{DD}		-	-	0.1	V
HFCLK frequency	f_{CORE}	0 wait-states (MODE = WS0) [1]	-	-	26	MHz
		1 wait-states (MODE = WS1) [1]	-	38.4	40	MHz

Note:
1. in MSC_READCTRL register

4.4 DC-DC Converter

Test conditions: L_{DCDC}=4.7 µH, C_{DCDC}=1.0 µF, V_{DCDC_I}=3.3 V, V_{DCDC_O}=1.8 V, I_{DCDC_LOAD}=50 mA, Heavy Drive configuration, F_{DCDC_LN}=8 MHz, unless otherwise indicated.

Table 4.3. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{DCDC_I}	Bypass mode	TBD	-	3.8	V
		Low noise (LN) or low power (LP) mode, 1.8 V output, 200 mA load current	2.4	-	3.8	V
Output voltage range	V_{DCDC_O}	1.8V configuration	1.8	-	-	V
Steady-state output ripple	V_R	ESR=50 Ω, ESL=2 nH on 1 µF filter cap. Radio disabled	-	3	-	mVpp
		ESR=50 Ω, ESL=2 nH on 1 µF filter cap. Radio enabled	-	TBD	-	mVpp
Output voltage under/overshoot	V_{OV}	CCM Mode (LNFORCECCM[1] = 1), Load changes between 0 mA and 100 mA	-	100	-	mV
		DCM Mode (LNFORCECCM[1] = 0), Load changes between 0 mA and 10 mA	-	150	-	mV
DC line regulation	V_{REG}	Input changes between 3.8 V and 2.4 V	-	0.1	-	%
DC load regulation	I_{REG}	Load changes between 0 mA and 100 mA in CCM mode	-	0.1	-	%
Quiescent current	I_{DCDC_Q}	Low power (LP) mode, lowest bias setting (LPCMPBIAS[1] = BIAS0)	-	50	-	nA
		Low noise (LN) mode, DCM configuration (LNFORCECCM[1] = 0)	-	0.3	-	mA
		Low noise (LN) mode, CCM configuration (LNFORCECCM[1] = 1)	-	0.8	-	mA
Max load current	I_{LOAD_MAX}	Low noise (LN) mode	-		200	mA
		Low power (LP) mode	-		10	mA
Capacitance of DCDC output capacitor	C_{DCDC}		1	-	10	µF
Inductance of DCDC output inductor	L_{DCDC}		-	4.7	-	µH
Resistance in Bypass mode	R_{BYP}		-	0.8	-	Ω
Peak current limit range	I_{IPK}		20	-	640	mA
Peak current limit step	I_{PK_STEP}	Light drive[2]	-	20	-	mA
		Medium Drive[2]	-	40	-	mA
		Heavy Drive[2]	-	80	-	mA
Switching frequency	F_{LN}	Low noise (LN) mode	3		8	MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. In MU_DCDCMISCCTRL register
2. Drive levels are defined by configuration of the P/NSLICESEL register. Light Drive: P/NSLICESEL=3; Medium Drive: P/NSLICESEL=7; Heavy Drive: P/NSLICESEL=15.

4.4.1 DC-DC Converter Typical Performance Characteristics

Default test conditions: CCM mode, L_{DCDC}=4.7 µH, C_{DCDC}=1.0 µF, V_{DCDC_I}=3.3 V, V_{DCDC_O}=1.8 V, F_{DCDC_LN}=8 MHz

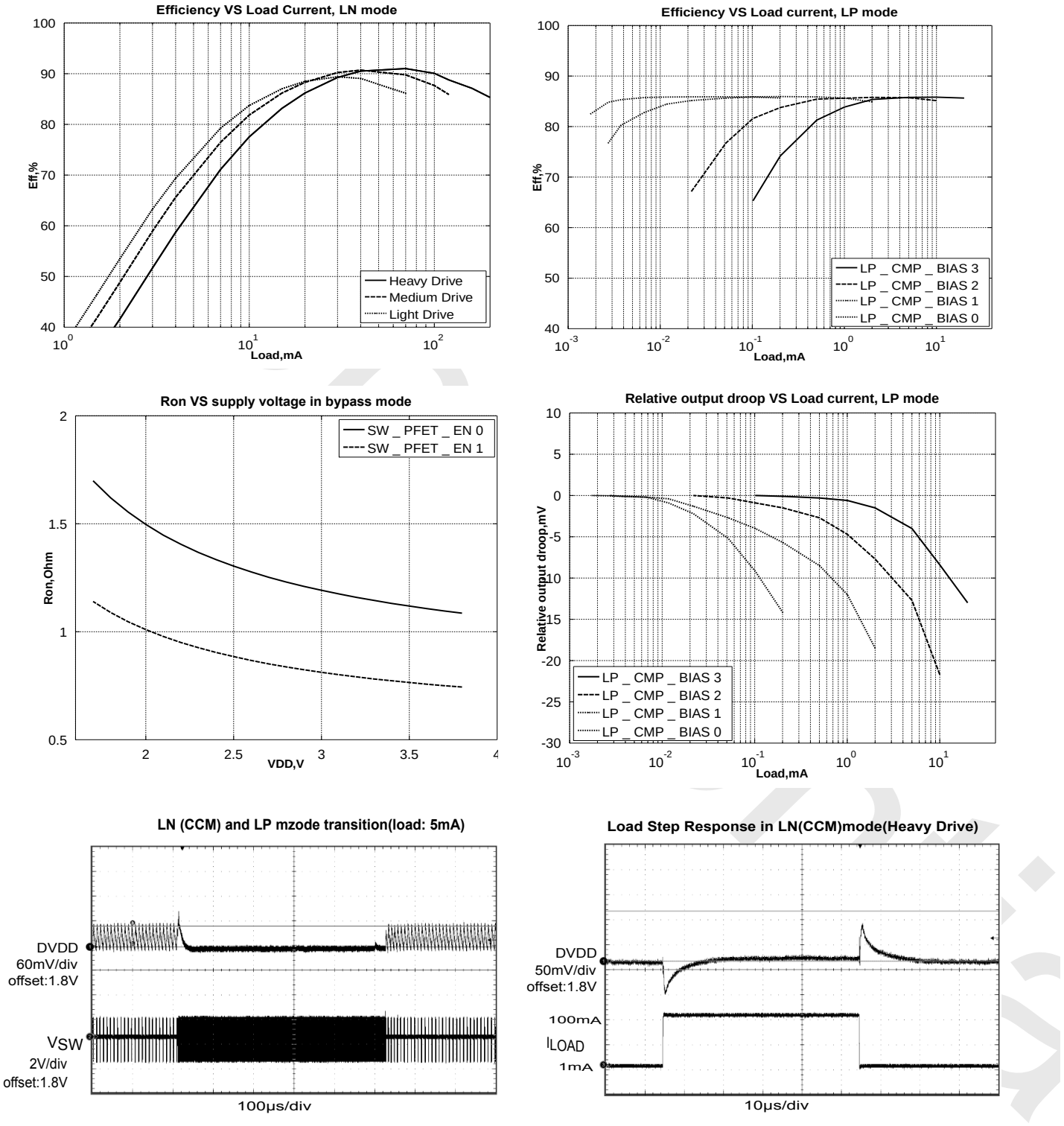


Figure 4.1. DC-DC Electrical Characteristics

4.5 Current Consumption

4.5.1 Current Consumption 1.8 V without DC-DC Converter

Unless otherwise indicated VREGVDD = AVDD = DVDD = RFVDD = PAVDD= 1.8 V. EMU_PWRCFG_PWRCG=NODCDC. EMU_DCDCCTRL_DCDCMODE=BYPASS. See Figure 5.1 EFR32MG1X232 Typical Application Circuit: Direct Supply Configuration without DC-DC converter on page 44.

Table 4.4. Current Consumption 1.8V without DC/DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 Active mode with radio disabled, All peripherals disabled	I_{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash	-	TBD	-	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	-	TBD	-	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	-	TBD	-	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	-	TBD	-	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	-	TBD	-	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	-	TBD	-	µA/MHz
Current consumption in EM1 Sleep mode with radio disabled. All peripherals disabled	I_{IDLE}	38.4 MHz crystal	-	TBD	-	µA/MHz
		38 MHz HFRCO	-	TBD	-	µA/MHz
		26 MHz HFRCO	-	TBD	-	µA/MHz
		1 MHz HFRCO	-	TBD	-	µA/MHz
Current consumption in EM2 DeepSleep mode.	I_{EM2}	Full RAM retention and RTCC running from LFXO	-	TBD	-	µA
Current consumption in EM3 Stop mode	I_{EM3}	Full RAM retention and CRYOTIMER running from ULFRCO	-	TBD	-	µA
Current consumption in EM4 Hibernate mode	I_{EM4}	128 byte RAM retention, RTCC running from LFXO	-	TBD	-	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	-	TBD	-	µA
		128 byte RAM retention, no RTCC	-	TBD	-	µA
Current consumption in EM4 Shutoff mode	I_{EM4S}	No RAM retention, no RTCC	-	TBD	-	µA

4.5.2 Current Consumption 3.3 V without DC-DC Converter

Unless otherwise indicated VREGVDD = AVDD = DVDD = RFVDD = PAVDD= 3.3 V. EMU_PWRCFG_PWRCG=NODCDC. EMU_DCDCCTRL_DCDCMODE=BYPASS. See Figure 5.1 EFR32MG1X232 Typical Application Circuit: Direct Supply Configuration without DC-DC converter on page 44.

Table 4.5. Current Consumption 3.3V without DC/DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 Active mode with radio disabled, All peripherals disabled	I_{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash	-	124	-	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	-	85	-	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	-	99	-	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	-	TBD	-	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	-	100	-	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	-	TBD	-	µA/MHz
Current consumption in EM1 Sleep mode with radio disabled. All peripherals disabled	I_{IDLE}	38.4 MHz crystal	-	45	-	µA/MHz
		38 MHz HFRCO	-	27	-	µA/MHz
		26 MHz HFRCO	-	28	-	µA/MHz
		1 MHz HFRCO	-	TBD	-	µA/MHz
Current consumption in EM2 DeepSleep mode.	I_{EM2}	Full RAM retention and RTCC running from LFXO	-	2.92	-	µA
Current consumption in EM3 Stop mode	I_{EM3}	Full RAM retention and CRYOTIMER running from ULFRCO	-	TBD	-	µA
Current consumption in EM4 Hibernate mode	I_{EM4}	128 byte RAM retention, RTCC running from LFXO	-	TBD	-	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	-	TBD	-	µA
		128 byte RAM retention, no RTCC	-	TBD	-	µA
Current consumption in EM4 Shutoff mode	I_{EM4S}	no RAM retention, no RTCC	-	TBD	-	µA

4.5.3 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD= 1.8 V DC-DC output. See Figure 5.2 EFR32MG1X232 Typical Application Circuit: Configuration with DC-DC Coverter (PAVDD from VDCDC) on page 44 or Figure 5.3 EFR32MG1X232 Typical Application Circuit: Configuration with DC-DC Coverter (PAVDD from VDD) on page 45.

Table 4.6. Current Consumption 3.3V with DC/DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 Active mode with radio disabled. All peripherals disabled, DCDC in LowNoise mode	I_{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash.	-	94	-	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	-	60	-	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	-	69	-	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	-	TBD	-	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	-	75	-	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	-	TBD	-	µA/MHz
Current consumption in EM1 Sleep mode with radio disabled. All peripherals disabled, DCDC in LowPower mode.	I_{IDLE}	38.4 MHz crystal	-	39	-	µA/MHz
		38 MHz HFRCO	-	20	-	µA/MHz
		26 MHz HFRCO	-	21	-	µA/MHz
		1 MHz HFRCO	-	TBD	-	µA/MHz
Current consumption in EM2 DeepSleep mode.	I_{EM2}	Full RAM retention and RTCC running from LFXO[1]	-	1.35	-	µA
Current consumption in EM3 Stop mode	I_{EM3}	Full RAM retention and CRYOTIMER running from ULFRCO[2]	-	1	-	µA
Current consumption in EM4 Hibernate mode	I_{EM4}	128 byte RAM retention, RTCC running from LFXO	-	0.7	-	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	-	0.5	-	µA
		128 byte RAM retention, no RTCC	-	0.3	-	µA
Current consumption in EM4 Shutoff mode	I_{EM4S}	no RAM retention, no RTCC	-	0.2	-	µA

Note:
1. Target for planned revision. Current silicon performance is 2.3 µA
2. Target for planned revision.

4.5.4 Current Consumption Using Radio

Unless otherwise indicated VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. See Figure 5.2 EFR32MG1X232 Typical Application Circuit: Configuration with DC-DC Coverter (PAVDD from VDCDC) on page 44. or Figure 5.3 EFR32MG1X232 Typical Application Circuit: Configuration with DC-DC Coverter (PAVDD from VDD) on page 45.

Table 4.7. Current Consumption Using Radio 3.3 V with DC-DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled)	I_{RX}	1 Mbit/s, 2GFSK, F = 2.4 GHz	-	8.6	-	mA
		802.15.4 receiving frame, F = 2.4 GHz	-	9.1	-	mA
Current consumption in polled RX mode (radio active for 200 µs every second to check for traffic)	I_{RX_POLL}	1 Mbit/s, 2GFSK, F = 2.4 GHz	-	4	-	µA
Current consumption in transmit mode (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled)	I_{TX}	CW, 0 dBm, F = 2.4 GHz	-	8.2	-	mA
		CW, 3 dBm, F = 2.4 GHz	-	16.4	-	mA
		CW, 8 dBm, F = 2.4 GHz	-	25.5	-	mA
		CW, 10.5 dBm, F = 2.4 GHz	-	34.5	-	mA
		CW, 16.5 dBm, F = 2.4 GHz, PAVDD connected directly to external 3.3V supply	-	88	-	mA
		CW, 19.5 dBm, F = 2.4 GHz, PAVDD connected directly to external 3.3V supply	-	133	-	mA

4.6 Wake up times

Table 4.8. Wake up times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wake up from EM2 Deep-Sleep	t_{EM2_WU}	Code execution from RAM	-	2.8	3.4	µs
		Code execution from FLASH	-	7.8	10.4	µs
Wakeup time from idle, executing from flash	t_{IDLE}	Executing from flash	-	TBD	-	AHB Clocks
		Executing from RAM	-	TBD	-	AHB Clocks
Wake up from EM3 Stop	t_{EM3_WU}	Executing from flash	-	2.8	3.4	µs
		Executing from RAM	-	TBD	-	µs
Wake up from EM4 Hibernate [1]	t_{EM4H_WU}	Executing from flash	-	TBD	-	µs
		Executing from RAM	-	TBD	-	µs
Wake up from EM4 Shutoff[1]	t_{EM4S_WU}	Executing from flash	-	TBD	-	µs
		Executing from RAM	-	TBD	-	µs

Note:
1. Time from wakeup request till first instruction is executed. Wakeup results in device reset.

4.7 Brown Out Detector

Table 4.9. Brown Out Detector

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DECOUPLE BOD threshold	$V_{DECOUPLEBOD}$		TBD	TBD	TBD	V
DECOUPLE BOD hysteresis	$V_{DECOUPLE\_HYST}$		-	TBD	-	V
DECOUPLE response time	$t_{DECOUPLE\_DELAY}$	Supply drops at 1V/µs rate	-	TBD	-	nS
DVDDBOD threshold	$V_{DVDDBOD}$	DVDD rising	TBD	TBD	TBD	V
		DVDD falling	TBD	TBD	TBD	V
DVDD BOD hysteresis	$V_{DVDDBOD\_HYST}$		-	TBD	-	mV
DVDD response time	$t_{DVDDBOD\_DELAY}$	Supply drops at 1V/µs rate	-	TBD	-	nS
AVDD BOD threshold	$V_{AVDDBOD}$	AVDD rising	TBD	TBD	TBD	V
		AVDD falling	TBD	TBD	TBD	V
AVDD BOD hysteresis	$V_{AVDDBOD\_HYST}$		-	TBD	-	mV
AVDD response time	$t_{AVDDBOD\_DELAY}$	Supply drops at 1V/µs rate	-	TBD	-	nS
EM4 BOD threshold	$V_{EM4DBOD}$	AVDD rising	TBD	TBD	TBD	V
		AVDD falling	TBD	TBD	TBD	V
EM4 BOD hysteresis	V_{EM4BOD_HYST}		-	TBD	-	mV
EM4 response time	t_{EM4BOD_DELAY}	Supply drops at 1V/µs rate	-	TBD	-	nS

4.8 Frequency Synthesizer Characteristics

Table 4.10. Frequency Synthesizer Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF Synthesizer Frequency range	F_{RANGE_2400}	2.4 GHz frequency range	2400	-	2485	MHz
LO tuning frequency resolution with 38.4 MHz crystal	F_{RES_2400}	2400 - 2485 MHz	-	-	73	Hz
Maximum frequency deviation with 38.4 MHz crystal	ΔF_{MAX_2400}		-	-	1677	kHz

4.9 2.4 GHz RF Transceiver Characteristics

4.9.1 RF Transmitter General Characteristics for the 2.4 GHz Band

Unless otherwise indicated T=25C,VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4MHz. RF center frequency 2.440 GHz. Test circuit according to Figure 5.2 EFR32MG1X232 Typical Application Circuit: Configuration with DC-DC Coverter (PAVDD from VDCDC) on page 44 and Figure 5.4 Typical 2.4 GHz RF impedance-matching network circuits on page 45.

Table 4.11. RF Transmitter General Characteristics for 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum TX power[1]	$POUT_{MAX}$	0 dBm-rated part numbers	-	0	-	dBm
Minimum active TX Power	$POUT_{MIN}$			-62	-	dBm
Output power step size	$POUT_{STEP}$	-5 dBm< Output power < 0 dBm	-	1	-	dB
Output power variation vs supply at $POUT_{MAX}$	$POUT_{VAR\_V}$	1.8 V < V(VREGVDD) < 3.3 V without DC-DC converter	-	6	-	dB
		1.8 V < V(VREGVDD < 3.3 V using DC-DC converter	-	2	-	dB
Output power variation vs temperature at $POUT_{MAX}$	$POUT_{VAR\_T}$	From -40 to +85° C	-	2	-	dB
Output power variation vs RF frequency at $POUT_{MAX}$	$POUT_{VAR\_F}$	Over RF tuning frequency range	-	1	-	dB
RF tuning frequency range	F_{RANGE}		2400	-	2483.5	MHz

Note:
1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of 2. Ordering Information

4.9.2 RF Receiver General Characteristics for the 2.4 GHz Band

Unless otherwise indicated T=25C,VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4MHz. RF center frequency 2.440 GHz. Test circuit according to Figure 5.2 EFR32MG1X232 Typical Application Circuit: Configuration with DC-DC Coverter (PAVDD from VDCDC) on page 44 and Figure 5.4 Typical 2.4 GHz RF impedance-matching network circuits on page 45.

Table 4.12. RF Receiver General Characteristics for 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2400	-	2483.5	MHz
Receive mode maximum spurious emission	$SPUR_{RX}$	30 MHz to 1 GHz	-	-57	-	dBm
		1 GHz to 12 GHz	-	-47	-	dBm
Level above which RFSENSE will trigger	$RFSENSE_{TRIG}$	CW at 2.45 GHz	-	-17	-	dBm
Level below which RFSENSE wil not trigger	$RFSENSE_{THRES}$		-	-50	-	dBm

4.9.3 RF Transmitter Characteristics for Bluetooth Smart in the 2.4 GHz Band

Unless otherwise indicated T=25C,VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4MHz. RF center frequency 2.440 GHz. Test circuit according to Figure 5.2 EFR32MG1X232 Typical Application Circuit: Configuration with DC-DC Coverter (PAVDD from VDCDC) on page 44 and Figure 5.4 Typical 2.4 GHz RF impedance-matching network circuits on page 45.

Table 4.13. RF Transmitter Characteristics for Bluetooth Smart in the 2.4GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6dB bandwidth	TXBW		-	TBD	-	kHz
Power spectral density limit	PSD_{LIMIT}	Per FCC part 15.247	-	TBD	-	dBm/ kHz
		Per ETSI 300.328	-	TBD	-	dBm/ MHz
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	99% BW at highest and lowest channels in band	-	TBD	-	MHz
In-band spurious emissions, with allowed exceptions[1]	$SPUR_{INB}$	At ±2 MHz	-	-35	-	dBm
		At ±3 MHz	-	-36	-	dBm
Emissions of harmonics out-of-band, per FCC part 15.247	$SPUR_{HRM\_FCC}$	2nd,3rd, 5, 6, 8, 9,10 harmonics; continuous transmission of modulated carrier	-	TBD	-	dBm
Spurious emissions out-of-band, per FCC part 15.247, excluding harmonics captured in $SPUR_{HARM,FCC}$	$SPUR_{OOB\_FCC}$	Above 2.483 GHz or below 2.4 GHz; continuous transmission of modulated carrier	-	TBD	-	dBc
Spurious emissions out-of-band; per ETSI 300.328	$SPUR_{ETSI328}$	[2400-BW to 2400] MHz, [2483.5 to 2483.5+BW] MHz	-	TBD	-	dBm
		[2400-2BW to 2400-BW] MHz, [2483.5+BW to 2483.5+2BW] MHz per ETSI 300.328	-	TBD	-	dBm
Spurious emissions per ETSI EN300.440	$SPUR_{ETSI440}$	47-74 MHz,87.5-108 MHz, 174-230 MHz, 470-862 MHz	-	TBD	-	nW
		25-1000 MHz	-	TBD	-	nW
		1-24 GHz	-	TBD	-	nW

Note:

1. Per Bluetooth Core_4.2, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.

4.9.4 RF Receiver Characteristics for Bluetooth Smart in the 2.4 GHz Band

Unless otherwise indicated T=25C,VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4MHz. RF center frequency 2.440 GHz. Test circuit according to Figure 5.2 EFR32MG1X232 Typical Application Circuit: Configuration with DC-DC Coverter (PAVDD from VDCDC) on page 44 and Figure 5.4 Typical 2.4 GHz RF impedance-matching network circuits on page 45.

Table 4.14. RF Receiver Characteristics for Bluetooth Smart in the 2.4GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level, 0.1% BER	SAT	Signal is reference signal[1]. Packet length is 20 bytes.	-	10	-	dBm
Sensitivity, 0.1% BER	SENS	Signal is reference signal. Using DC-DC converter[2]	-	-94	-	dBm
		With dirty transmitter as defined in Core_4.1	-	-91.4	-	dBm
Signal to co-channel interferer, 0.1% BER	C/I_{CC}	Desired signal 3 dB above reference sensitivity	-	9	-	dB
N+1 adjacent channel (1 MHz) selectivity, 0.1% BER, with allowable exceptions[3]. Desired is reference signal at 3 dB above reference sensitivity level	C/I_{1+}	Interferer is reference signal at +1 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	-	-2	-	dB
N-1 adjacent channel (1 MHz) selectivity, 0.1% BER, with allowable exceptions[3]. Desired is reference signal at 3 dB above reference sensitivity level	C/I_{1-}	Interferer is reference signal at -1 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	-	0	-	dB
Alternate (2 MHz) selectivity, 0.1% BER, with allowable exceptions[3]. Desired is reference signal at 3 dB above reference sensitivity level	C/I_2	Interferer is reference signal at ± 2 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	-	-43	-	dB
Alternate (3 MHz) selectivity, 0.1% BER, with allowable exceptions[3]. Desired is reference signal at 3 dB above reference sensitivity level	C/I_3	Interferer is reference signal at ±3 MHz offset. Desired frequency 2404 MHz ≤ Fc ≤ 2480 MHz	-	-48	-	dB
Selectivity to image frequency, 0.1% BER. Desired is reference signal at 3 dB above reference sensitivity level	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision	-	-40	-	dB
Selectivity to image frequency +1 MHz, 0.1% BER.[4] Desired is reference signal at 3 dB above reference sensitivity level	C/I_{IM+1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision	-	-48	-	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Blocking, 0.1% BER, Desired is reference signal at 3 dB above reference sensitivity level. Interferer is CW in OOB range.	$BLOCK_{OOB}$	Interferer frequency 30 MHz ≤ f ≤ 2000 MHz	-	-30	-	dBm
		Interferer frequency 2003 MHz ≤ f ≤ 2399 MHz	-	-35	-	dBm
		Interferer frequency 2484 MHz ≤ f ≤ 2997 MHz	-	-35	-	dBm
		Interferer frequency 3 GHz ≤ f ≤ 12.75 GHz	-	-30	-	dBm
Intermodulation performance per Core_4.1, Vol 6 Section 4.4 (n = 3 alternative), 0.1% BER.	IM	Desired is reference signal at 6dB above reference sensitivity level. Interferer 1 is CW at level IM_{BLE}. Interferer 2 is reference signal at IM_{BLE}.	-	-33	-	dBm
Upper limit of input power range over which RSSI resolution is maintained	$RSSI_{MAX}$		TBD	-	-	dBm
Lower limit of input power range over which RSSI resolution is maintained	$RSSI_{MIN}$		-	-	TBD	dBm
RSSI resolution	$RSSI_{RES}$	Over $RSSI_{MIN}$ to $RSSI_{MAX}$	-	-	TBD	dB

Note:

1. Reference signal is defined in Core_4.2, Vol 6, Section 4.6. 2GFSK, Modulation index = 0.5, BT = 0.5, Bit rate = 1 Mbps, desired data = PRBS9; interferer data = PRBS15; frequency accuracy better than 1 ppm
2. Target for planned revision. Current silicon performance is -92.1 dBm
3. Allowable exceptions for spurious response RF channels, as specified in Core_4.2, Vol 6, Section 4.2 "Interference Performance". Where there is conflict of specifications regarding interference at image frequencies, the less stringent specification applies.
4. Selectivity to image frequency -1 MHz corresponds to C/I_{1+} N+1 adjacent hannel selectivity

4.9.5 RF Transmitter Characteristics for 802.15.4 O-QPSK DSSS in the 2.4 GHz Band

Unless otherwise indicated T=25C,VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4MHz. RF center frequency 2.445 GHz. Test circuit according to Figure 5.2 EFR32MG1X232 Typical Application Circuit: Configuration with DC-DC Coverter (PAVDD from VDCDC) on page 44 and Figure 5.4 Typical 2.4 GHz RF impedance-matching network circuits on page 45.

Table 4.15. RF Transmitter Characteristics for 802.15.4 DSSS-OQPSK in the 2.4GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Error vector magnitude (offset EVM), per 802.15.4-2011	EVM	Signal is DSSS-OQPSK reference packet[1]	-	5	-	% rms
Transmit center frequency error[2]	FERR		-40	-	40	ppm
Power spectral density limit	PSD_{LIMIT}	Relative, at carrier ±3.5 MHz	-	TBD	-	dBc
		Absolute, at carrier ±3.5 MHz	-	TBD	-	dBm
		Per FCC part 15.247	-	TBD	-	dBm/kHz
		Per ETSI 300.328	-	TBD	-	dBm/MHz
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	99% BW at highest and lowest channels in band	-	TBD	-	MHz
Emissions of harmonics out-of-band, per FCC part 15.247	$SPUR_{HRM\_FCC}$	2nd,3rd, 5, 6,8,9,10 harmonics; continuous transmission of modulated carrier	-	TBD	-	dBm
Spurious emissions out-of-band, per FCC part 15.247, excluding harmonics	$SPUR_{OOB\_FCC}$	Above 2.483 GHz or below 2.4 GHz; continuous transmission of modulated carrier	-	TBD	-	dBc
Spurious emissions out-of-band; per ETSI 300.328	$SPUR_{ETSI328}$	[2400-BW to 2400], [2483.5 to 2483.5+BW];	-	TBD	-	dBm
		[2400-2BW to 2400-BW], [2483.5+BW to 2483.5+2BW]; per ETSI 300.328	-	TBD	-	dBm
Spurious emissions per ETSI EN300.440	$SPUR_{ETSI440}$	47-74 MHz,87.5-108 MHz, 174-230 MHz, 470-862 MHz	-	TBD	-	nW
		25-1000 MHz,	-	TBD	-	nW
		1G-24G	-	TBD	-	nW

Note:

1. Reference packet is defined as TBD of packet length TBD, modulated according to 802.15.4-2011 DSSS-OQPSK in the 2.4GHz band, with pseudo-random packet data content
2. Frequency error measurements are referred to the high-frequency crystal reference of the device

4.9.6 RF Receiver Characteristics for 802.15.4 O-QPSK DSSS in the 2.4 GHz Band

Unless otherwise indicated T=25C,VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4MHz. RF center frequency 2.445 GHz. Test circuit according to Figure 5.2 EFR32MG1X232 Typical Application Circuit: Configuration with DC-DC Coverter (PAVDD from VDCDC) on page 44 and Figure 5.4 Typical 2.4 GHz RF impedance-matching network circuits on page 45.

Table 4.16. RF Receiver Characteristics for 801.15.4 DSSS-OQPSK in the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level, 1% PER	SAT	Signal is reference signal[1]. Packet length is 20 octets.	-	10	-	dBm
Sensitivity, 1% PER	SENS	Signal is reference signal. Packet length is 20 octets. Using DC-DC converter.	-	-99.1	-	dBm
		Signal is reference signal. Packet length is 20 octets. Without DC-DC converter.	-	-99.4	-	dBm
Co-channel interferer rejection, 1% PER	CCR	Desired signal 10 dB above sensitivity limit	-	-2.2	-	dB
High-side adjacent channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level[2]	ACR_{+1}	Interferer is reference signal at +1 channel-spacing.	-	34.1	-	dB
		Interferer is filtered reference signal[3] at +1 channel-spacing.	-	51	-	dB
		Interferer is CW at +1 channel-spacing.[4]	-	58.7	-	dB
Low-side adjacent channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level[2]	ACR_{-1}	Interferer is reference signal at -1 channel-spacing.	-	35.5	-	dB
		Interferer is filtered reference signal[3] at -1 channel-spacing.	-	54	-	dB
		Interferer is CW at -1 channel-spacing.	-	60.6	-	dB
Alternate channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level[2]	ACR_2	Interferer is reference signal at ±2 channel-spacing	-	45.6	-	dB
		Interferer is filtered reference signal[3] at ±2 channel-spacing	-	59.5	-	dB
		Interferer is CW at ±2 channel-spacing	-	66	-	dB
Image rejection , 1% PER, Desired is reference signal at 3dB above reference sensitivity level[2]	IR	Interferer is CW in image band[4]	-	50.2	-	dB
Blocking rejection of all other channels. 1% PER, Desired is reference signal at 3dB above reference sensitivity level[2]. Interferer is reference signal.	BLOCK	Interferer frequency < Desired frequency - 3 channel-spacing	-	58.8	-	dB
		Interferer frequency > Desired frequency + 3 channel-spacing	-	57.7	-	dB
Blocking rejection of 802.11g signal centered at +12MHz or -13MHz	$BLOCK_{80211G}$	Desired is reference signal at 6dB above reference sensitivity level[2]	-	50.6	-	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Upper limit of input power range over which RSSI resolution is maintained	$RSSI_{MAX}$		5	-	-	dBm
Lower limit of input power range over which RSSI resolution is maintained	$RSSI_{MIN}$		-	-	-98	dBm
RSSI resolution	$RSSI_{RES}$	over $RSSI_{MIN}$ to $RSSI_{MAX}$	-	0.25	-	dB
RSSI linearity as defined by 802.15.4-2003	$RSSI_{LIN}$		-	TBD	-	dB

Note:

1. Reference signal is defined as TBD
2. Reference sensitivity level is -85 dBm
3. Filter is characterized as a symmetric bandpass centered on the adjacent channel having a 3dB bandwidth of 4.6 MHz and stop-band rejection better than 26 dB beyond 3.15MHz from the adjacent carrier.
4. Due to low-IF frequency, there is some overlap of adjacent channel and image channel bands. Adjacent channel CW blocker tests place the Interferer center frequency at the Desired frequency ±5 MHz on the channel raster, whereas the image rejection test places the CW interferer near the image frequency of the Desired signal carrier, regardless of the channel raster.

4.10 RFSENSE

Table 4.17. RFSENSE

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RFSENSE current consumption	$I_{RFSENSE}$		-	TBD	TBD	nA

4.11 Modem Features

Table 4.18. Modem Features

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Receive Bandwidth	$RX_{Bandwidth}$	Configurable range with 38.4 MHz crystal	0.1	-	2530	kHz
IF Frequency	IF_{Freq}	Configurable range with 38.4 MHz crystal. Selected steps available.	150	-	1371	kHz
DSSS symbol length	$DSSS_{Range}$	Configurable in steps of 1 chip	2	-	32	chips
DSSS Bits per symbol	$DSSS_{BitPerSym}$	Configurable	1	-	4	bits/ symbol

4.12 Oscillators

4.12.1 LFXO

Table 4.19. LFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{LFXO}		-	32.768	-	kHz
Supported crystal equivalent series resistance (ESR)	ESR_{LFXO}		-	-	70	kΩ
Supported range of crystal load capacitance [1]	C_{LFXO_CL}		6	-	18	pF
On-chip tuning cap range [2]	C_{LFXO_T}	On each of LFXTAL_N and LFXTAL_P pins	8	-	40	pF
On-chip tuning cap step size	SS_{LFXO}		-	0.25	-	pF
LFXO current consumption on AVDD [3] after startup	I_{LFXO_ANA}	ESR = 30 kΩ, C_L=12.5 pF, GAIN[4] = 3, AGC[4] = 1	-	TBD	-	nA
LFXO current consumption on DVDD after startup	I_{LFXO_DIG}	ESR = 30 kΩ, C_L=12.5 pF, GAIN[4] = 1	-	TBD	-	nA
Start- up time	t_{LFXO}	ESR=30 kΩ, C_L=12.5 pF, GAIN[4] =2	-	200	-	ms

Note:

1. Total load capacitance as seen by the crystal
2. The effective load capacitance seen by the crystal will be C_{LFXO_T} /2. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.
3. Current consumption on DVDD instead if ANASW=1 in EMU_PWRCTRL register
4. In CMU_LFXOCTRL register

4.12.2 HFXO

Table 4.20. HFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	f_{HFXO}		38	38.4	40	MHz
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO}	Crystal frequency 38.4 MHz	-	-	60	Ω
Supported range of crystal load capacitance [1]	C_{HFXO_CL}		6	-	12	pF
On-chip tuning cap range [2]	C_{HFXO_T}	On each of HFXTAL_N and HFXTAL_P pins	0	20	25	pF
On-chip tuning capacitance step	SS_{HFXO}		-	0.04	-	pF
Current consumption on DVDD for HFXO after startup	$I_{HFXODIG}$	38.4 MHz: ESR = 50 Ω, C_L = 10 pF, BOOST[3] = 2	-	TBD	-	µA
Current consumption on AVDD for HFXO after startup	$I_{HFXOANA}$	38.4 MHz: ESR = 50 Ω, C_L = 10 pF, BOOST[3] = 2	-	TBD	-	µA
Startup time	t_{HFXO}	38.4 MHz: ESR=50 Ω, C_L = 10 pF, BOOST[3] = 2	-	300	-	µs
Frequency Tolerance for the crystal	FT_{HFXO}	38.4 MHz, ESR = 50 Ω, CL = 10 pF	-40	-	40	ppm

Note:
1. Total load capacitance as seen by the crystal
2. The effective load capacitance seen by the crystal will be C_{HFXO_T} /2. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.
3. In CMU_HFXOCTRL register

4.12.3 LFRCO

Table 4.21. LFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{LFRCO}		TBD	32.768	TBD	kHz
Startup time	t_{LFRCO}		-	500	-	µs
Current consumption on DVDD	$I_{LFRCODIG}$		-	TBD	-	nA
Current consumption on AVDD [1]	$I_{LFRCOANA}$		-	TBD	-	nA

Note:
1. Current consumption on DVDD instead if ANASW=1 in EMU_PWRCTRL register

4.12.4 HFRCO and AUXHFRCO

Table 4.22. HFRCO and AUXHFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{HFRCO}	38 MHz frequency band	TBD	38	TBD	MHz
		32 MHz frequency band	TBD	32	TBD	MHz
		26 MHz frequency band	TBD	26	TBD	MHz
		19 MHz frequency band	TBD	19	TBD	MHz
		16 MHz frequency band	TBD	16	TBD	MHz
		13 MHz frequency band	TBD	13	TBD	MHz
		7 MHz frequency band	TBD	7	TBD	MHz
		4 MHz frequency band	TBD	4	TBD	MHz
		2 MHz frequency band	TBD	2	TBD	MHz
		1 MHz frequency band	TBD	1	TBD	MHz
Start-up time	t_{HFRCO}	$f_{HFRCO} \geq 19$ MHz	-	300	-	ns
		$4 < f_{HFRCO} < 19$ MHz	-	1	-	µs
		$f_{HFRCO} \leq 4$ MHz	-	2.5	-	µs
Current consumption on DVDD	$I_{HFRCODIG}$	f_{HFRCO} = 38 MHz	-	TBD	-	µA
		f_{HFRCO} = 32 MHz	-	TBD	-	µA
		f_{HFRCO} = 26 MHz	-	TBD	-	µA
		f_{HFRCO} = 19 MHz	-	TBD	TBD	µA
		f_{HFRCO} = 16 MHz	-	TBD	-	µA
		f_{HFRCO} = 13 MHz	-	TBD	-	µA
		f_{HFRCO} = 7 MHz	-	TBD	-	µA
		f_{HFRCO} = 4 MHz	-	TBD	-	µA
		f_{HFRCO} = 2 MHz	-	TBD	-	µA
		f_{HFRCO} = 1 MHz	-	TBD	-	µA
Current consumption on AVDD [1]	$I_{HFRCOANA}$	f_{HFRCO} = 38 MHz	-	TBD	-	µA
		f_{HFRCO} = 32 MHz	-	TBD	-	µA
		f_{HFRCO} = 26 MHz	-	TBD	-	µA
		f_{HFRCO} = 19 MHz	-	TBD	TBD	µA
		f_{HFRCO} = 16 MHz	-	TBD	-	µA
		f_{HFRCO} = 13 MHz	-	TBD	-	µA
		f_{HFRCO} = 7 MHz	-	TBD	-	µA
		f_{HFRCO} = 4 MHz	-	TBD	-	µA
		f_{HFRCO} = 2 MHz	-	TBD	-	µA
		f_{HFRCO} = 1 MHz	-	TBD	-	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Step size	SS_{HFRCO}	Coarse (% of period)	-	0.8	-	%
		Fine (% of period)	-	0.1	-	%
Duty cycle	DC_{HFRCO}		47.5	-	52.5	%
Period Jitter	PJ_{HFRCO}		-	0.2	-	% RMS

Note:
1. Current consumption on DVDD instead if ANASW=1 in EMU_PWRCTRL register

4.12.5 ULFRCO

Table 4.23. ULFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{ULFRCO}		TBD	1	TBD	kHz

4.13 GPIO

Table 4.24. GPIO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IOIL}		-	-	IOVDD*0.3	V
Input high voltage	V_{IOIH}		IOVDD*0.7	-	-	V
Output high voltage relative to IOVDD	V_{IOOH}	Sourcing 3 mA, V_{DD} ≥ 3 V, DRIVESTRENGTH[1] = WEAK	IOVDD*0.8	-	-	V
		Sourcing 1.2 mA, V_{DD} ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK	IOVDD*0.6	-	-	V
		Sourcing 20 mA, V_{DD} ≥ 3 V, DRIVESTRENGTH[1] = STRONG	IOVDD*0.8	-	-	V
		Sourcing 8 mA, V_{DD} ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG	IOVDD*0.6	-	-	V
Output low voltage relative to IOVDD	V_{IOOL}	Sinking 3 mA, V_{DD} ≥ 3 V, DRIVESTRENGTH[1] = WEAK	-	-	IOVDD*0.2	V
		Sinking 1.2 mA, V_{DD} ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK	-	-	IOVDD*0.4	V
		Sinking 20 mA, V_{DD} ≥ 3 V, DRIVESTRENGTH[1] = STRONG	-	-	IOVDD*0.2	V
		Sinking 8 mA, V_{DD} ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG	-	-	IOVDD*0.4	V
Input leakage current	I_{IOLEAK}	GPIO ≤ IOVDD	-	0.1	TBD	nA
Input leakage current on 5VTOL pads above IOVDD	$I_{5VTOLLEAK}$	IOVDD < GPIO ≤ IOVDD + 2 V	-	3.3	15	µA
I/O pin pull-up resistor	R_{PU}		TBD	40	TBD	kΩ
I/O pin pull-down resistor	R_{PD}		TBD	40	TBD	kΩ
Pulse width of pulses removed by the glitch suppression filter	$t_{IOGLITCH}$		TBD	25	TBD	ns
Output fall time, From 70% to 30% of V_{IO}	t_{IOOF}	C_L = 50pF, DRIVESTRENGTH[1] = STRONG, SLEWRATE[1] = 0x6	-	TBD	-	ns
		C_L = 50pF, DRIVESTRENGTH[1] = WEAK, SLEWRATE[1] = 0x6	-	TBD	-	ns
Output rise time, From 30% to 70% of V_{IO}	t_{IOOR}	C_L = 50pF, DRIVESTRENGTH[1] = STRONG, SLEWRATE = 0x6[1]	-	TBD	-	ns
		C_L = 50pF, DRIVESTRENGTH[1] = WEAK, SLEWRATE[1] = 0x6	-	TBD	-	ns

Note:
1. In GPIO_Pn_CTRL register

4.14 VMON

Table 4.25. VMON

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VMON Supply Current in EM0 or EM1	I_{VMON}	In EM0 or EM1, 1 supply monitored	-	5.8	-	µA
		In EM0 or EM1, 4 supplies monitored	-	11.8	-	µA
		In EM2, EM3 or EM4, 1 supplies monitored	-	68	-	nA
		In EM2, EM3 or EM4, 4 supplies monitored	-	115	-	nA
VMON Loading of Monitored Supply	I_{SENSE}	In EM0 or EM1	-	2	-	µA
		In EM2, EM3 or EM4	-	2	-	nA
Threshold range	V_{VMON_RANGE}		TBD	-	TBD	V
Threshold step size	N_{VMON_STESP}	Coarse	-	200	-	mV
		Fine	-	20	-	mV
Response time	t_{VMON_RES}	Supply drops at 1V/µs rate	-	500	-	ns
Hysteresis	V_{VMON_HYST}		-	TBD	-	mV

4.15 ADC

Table 4.26. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	$V_{RESOLUTION}$		6	-	12	Bits
Input voltage range	V_{ADCIN}	Single ended	0	-	$2*V_{REF}$	V
		Differential	$-V_{REF}$	-	V_{REF}	V
Input range of external reference voltage, single ended and differential	$V_{ADCREFIN\_P}$		1	-	V_{AVDD}	V
Power supply rejection	$PSRR_{ADC}$	At DC	-	80	-	dB
Analog input common mode rejection ratio	$CMRR_{ADC}$	At DC	-	80	-	dB
Current on DVDD, using internal reference buffer. Continous operation. WARMUPMODE[1] = KEEPADCWARM	$I_{ADCDIG\_CONTINOUS}$	1 Msps / 16 MHz ADCCLK, BIASPROG[2] = 0	-	TBD	-	µA
		250 ksps / 4 MHz ADCCLK, BIASPROG[2] = 6	-	TBD	-	µA
		62.5 Msps / 1 MHz ADCCLK, BIASPROG[2] = 15	-	TBD	-	µA
Current on DVDD, using internal reference buffer. Duty-cycled operation. WARMUPMODE[1] = NORMAL	I_{ADCDIG_NORMAL}	50 ksps / 16 MHz ADCCLK, BIASPROG[2] = 0	-	TBD	-	µA
		5 ksps / 16 MHz ADCCLK BIASPROG[2] = 0	-	TBD	-	µA
Current on DVDD, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[1] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADCDIG\_STANDBY}$	125 ksps / 16 MHz ADCCLK, BIASPROG[2] = 0	-	TBD	-	µA
		5 ksps / 16 MHz ADCCLK, BIASPROG[2] = 0	-	TBD	-	µA
Current on AVDD[3], using internal reference buffer. Continous operation. WARMUPMODE[1] = KEEPADCWARM	$I_{ADCANA\_CONTINOUS}$	1 Msps / 16 MHz ADCCLK, BIASPROG[2] = 0	-	TBD	-	µA
		250 ksps / 4 MHz ADCCLK, BIASPROG[2] = 6	-	TBD	-	µA
		62.5 Msps / 1 MHz ADCCLK, BIASPROG[2] = 15	-	TBD	-	µA
Current on AVDD[3] , using internal reference buffer. Duty-cycled operation. WARMUPMODE[1] = NORMAL	I_{ADCANA_NORMAL}	50 Ksps / 16 MHz ADCCLK, BIASPROG[2] = 0	-	TBD	-	µA
		5 Ksps / 16 MHz ADCCLK, BIASPROG[2] = 0	-	TBD	-	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current on AVDD[3], using internal reference buffer. Duty-cycled operation. WARMUPMODE[1] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADCANA\_STANDBY}$	125 Ksps / 16 MHz ADCCLK, BIASPROG[2] = 0	-	TBD	-	µA
		5 Ksps / 16 MHz ADCCLK, BIASPROG[2] = 0	-	TBD	-	µA
ADC Clock Frequency	f_{ADCCLK}		-	-	16	MHz
Throughput rate	$f_{ADCRATE}$		-	-	1	Msps
Conversion time	$t_{ADCCONV}$	6 bit	-	7	-	ADCCLK Cycles
		10 bit	-	11	-	ADCCLK Cycles
		12 bit	-	13	-	ADCCLK Cycles
Startup time of reference generator and ADC core in NORMAL mode	$t_{ADCSTART}$	WARMUPMODE[1] = NORMAL	-	-	5	µs
From standby mode		WARMUPMODE[1] = KEEPINSTANDBY or KEEPINSLOWACC	-	-	1	µs
SNDR at 1Msps and f_{in} = 10kHz	$SNDR_{ADC}$	Internal reference, 2.5 V full-scale, differential (-1.25, 1.25)	TBD	67	-	dB
		vrefp_in = 1.25 V direct mode with 2.5 V full-scale, differential	-	68	-	dB
Spurious-Free Dynamic Range (SFDR)	$SFDR_{ADC}$	1 MSamples/s, 10 kHz full-scale sine wave	-	75	-	dB
Input referred ADC noise, rms	V_{REF_NOISE}	Including quantization noise and distortion	-	380	-	µV
Offset Error	$V_{ADCOFFSETERR}$		TBD	1	TBD	LSB
Gain error in ADC	V_{ADC_GAIN}	Using internal reference	-	±0.1	TBD	%
		Using external reference	-	TBD	-	%
Differential non-linearity (DNL)	DNL_{ADC}	12 bit resolution	-1	-	TBD	LSB
Integral non-linearity (INL), End point method	INL_{ADC}	12 bit resolution	TBD	-	TBD	LSB

Note:

1. In ADCn_CNTL register
2. In ADCn_BIASPROG register
3. Current consumption on DVDD instead if ANASW=1 in EMU_PWRCTRL register

4.16 IDAC

Table 4.27. IDAC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Number of Ranges	N_{IDAC_RANGES}		-	4	-	-
Output Current	I_{IDAC_OUT}	RANGSEL[1] = RANGE0	0.05	-	1.6	µA
		RANGSEL[1] = RANGE1	1.6	-	4.7	µA
		RANGSEL[1] = RANGE2	0.5	-	16	µA
		RANGSEL[1] = RANGE3	2	-	64	µA
Linear steps within each range	N_{IDAC_STEPS}		-	32	-	
Step size	SS_{IDAC}	RANGSEL[1] = RANGE0	-	50	-	nA
		RANGSEL[1] = RANGE1	-	100	-	nA
		RANGSEL[1] = RANGE2	-	500	-	nA
		RANGSEL[1] = RANGE3	-	2	-	µA
Total Accuracy, STEPSEL[1] = 0x10	ACC_{IDAC}	Continuous mode, AVDD=3.3V, T = 25°C	TBD	-	TBD	%
		Continuous mode, AVDD=3.8V, across all temperature	TBD	-	TBD	%
		EM2 or EM3	TBD	-	TBD	%
Start up time	t_{IDAC_SU}	Output within 1% of steady state value	-	5	TBD	µs
Settling time, (output settled within 1% of steady state value)	t_{IDAC_SETTLE}	Range setting is changed	-	5	-	µs
		Step value is changed	-	1	-	µs
Current consumption on AVDD in continuous mode [2]	I_{IDAC}	Source mode, excluding output current	-	9.2	-	µA
		Sink mode, excluding output current	-	12.3	-	µA
Output voltage compliance in source mode, source current change relative to current sourced at 0 V	I_{COMP_SRC}	RANGESEL1=0, output voltage = max(V(IOVDD), V(AVDD)[3]-100 mv)	-	TBD	-	%
		RANGESEL1=1, output voltage = max(V(IOVDD), V(AVDD)[3]-100 mV)	-	TBD	-	%
		RANGESEL1=2, output voltage = max(V(IOVDD), V(AVDD)[3]-150 mV)	-	TBD	-	%
		RANGESEL1=3, output voltage = max(V(IOVDD), V(AVDD)[3]-250 mV)	-	TBD	-	%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output voltage compliance in source mode, sink current change relative to current sunk at IOVDD	I_{COMP_SINK}	RANGESEL1=0, output voltage = 100 mV	-	TBD	-	%
		RANGESEL1=1, output voltage = 100 mV	-	TBD	-	%
		RANGESEL1=2, output voltage = 150 mV	-	TBD	-	%
		RANGESEL1=3, output voltage = 250 mV	-	TBD	-	%

Note:

1. In IDAC_CURPROG register
2. Current consumption on DVDD instead if ANASW=1 in EMU_PWRCTRL register
3. Voltage reference AVDD switches to DVDD when ANASW=1 in EMU_PWRCTRL

4.17 Analog Comparator (ACMP)

Table 4.28. ACMP

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{ACMPIN}	CMPVDD = ACMPn_CTRL_PWRSEL [1]	0	-	CMPVDD	V
Active current not including voltage reference	I_{ACMP}	BIASPROG[2] = 1, FULLBIAS[2] = 0	-	50	-	nA
		BIASPROG[2] = 0x10, FULLBIAS[2] = 0	-	370	TBD	nA
		BIASPROG[2] = 0x20, FULLBIAS[2] = 1	-	65	TBD	µA
Current consumption of internal voltage reference,	$I_{ACMPREF}$	VLP selected as input using 2.5V Reference / 4 (0.625V)	-	50	-	nA
		VLP selected as input using VDD	-	20	-	nA
		VBDIV selected as input using 1.25 V reference / 1	-	3	-	µA
		VADIV selected as input using VDD/1	-	2	-	µA
Hysteresis	$V_{ACMPHYST}$	HYSTSEL[3] = HYST0	-	0	TBD	mV
		HYSTSEL[3] = HYST1	-	14	-	mV
		HYSTSEL[3] = HYST2	-	25	-	mV
		HYSTSEL[3] = HYST3	-	30	-	mV
		HYSTSEL[3] = HYST4	-	35	-	mV
		HYSTSEL[3] = HYST5	-	39	-	mV
		HYSTSEL[3] = HYST6	-	42	-	mV
		HYSTSEL[3] = HYST7	-	45	-	mV
Comparator delay	$t_{ACMPDELAY}$	BIASPROG[2] = 1, FULLBIAS[2] = 0 [4]	-	30	-	µs
		BIASPROG[2] = 0x10, FULLBIAS[2] = 0 [4]	-	3.7	-	µs
		BIASPROG[2] = 0x20, FULLBIAS[2] = 1 [4]	-	35	-	ns
Startup time of reference generator	$t_{ACMPREF}$	BIASPROG[2] =0x07, FULLBIAS[2] = 1 [4]	-	TBD		µs
Offset voltage	$V_{ACMPOFFSET}$		-	-	TBD	mV

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reference Voltage	$V_{ACMPREF}$	Single ended, internal 1.25 V reference	TBD	1.25	TBD	V
		Single ended, internal 2.5 V reference	TBD	2.5	TBD	V
		Differential, internal 1.25 V reference	TBD	1.25	TBD	V
		Differential, internal 2.5 V reference	TBD	2.5	TBD	V
Capacitive Sense Internal Resistance	R_{CSRES}	CSRESSEL[5] = 0	-	inf	-	kΩ
		CSRESSEL[5] = 1	-	12	-	kΩ
		CSRESSEL[5] = 2	-	24	-	kΩ
		CSRESSEL[5] = 3	-	36	-	kΩ
		CSRESSEL[5] = 4	-	48	-	kΩ
		CSRESSEL[5] = 5	-	92	-	kΩ
		CSRESSEL[5] = 6	-	148	-	kΩ
		CSRESSEL[5] = 7	-	215	-	kΩ

Note:

1. CMPVDD is a supply chosen by the setting in ACMPn_CTRL_PWRSEL and may be IOVDD, AVDD or DVDD
2. In ACMPn_CTRL register
3. In ACMPn_HYSTERESIS register
4. ± 100 mV differential
5. In ACMPn_INPUTSEL register

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given as:

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$$

$I_{ACMPREF}$ is zero if an external voltage reference is used.

5. Application Circuits

5.1 Power Supplies

Typical power supply connections for direct supply, without using the internal DC-DC converter, are shown in the following figure.

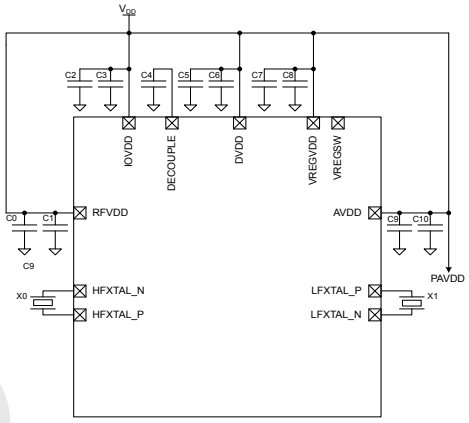


Figure 5.1. EFR32MG1X232 Typical Application Circuit: Direct Supply Configuration without DC-DC converter

Typical power supply circuits using the internal DC-DC converter are shown below. The MCU operates from the DC-DC converter supply. For low RF transmit power applications less than 13dBm, the RF PA may be supplied by the DC-DC converter. For OPNs supporting high power RF transmission, the RF PA must be directly supplied by VDD for RF transmit power greater than 13 dBm.

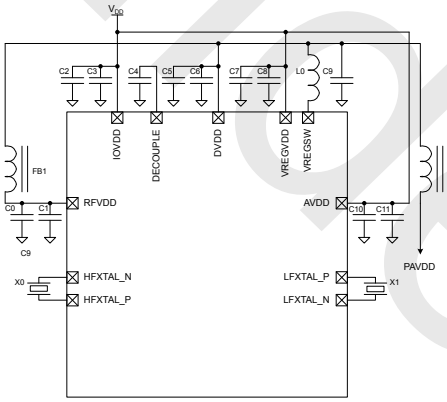


Figure 5.2. EFR32MG1X232 Typical Application Circuit: Configuration with DC-DC Coverter (PAVDD from VDCDC)

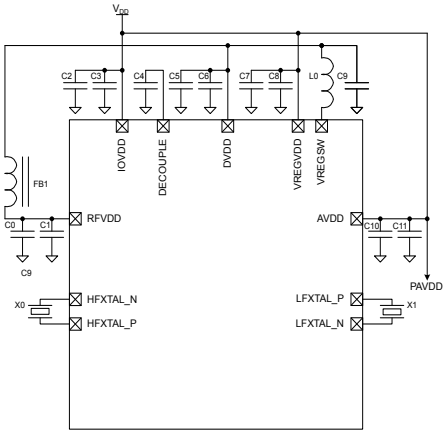


Figure 5.3. EFR32MG1X232 Typical Application Circuit: Configuration with DC-DC Coverter (PAVDD from VDD)

5.2 RF Matching Networks

Typical RF matching network circuit diagrams are shown in Figure 5.4 Typical 2.4 GHz RF impedance-matching network circuits on page 45 for applications in the 2.4GHz band. Application-specific component values can be found in the EFR32 Reference Manual. For low RF transmit power applications less than 13dBm, the two-element match is recommended. For OPNs supporting high power RF transmission, the four-element match is recommended for high RF transmit power (> 13dBm).

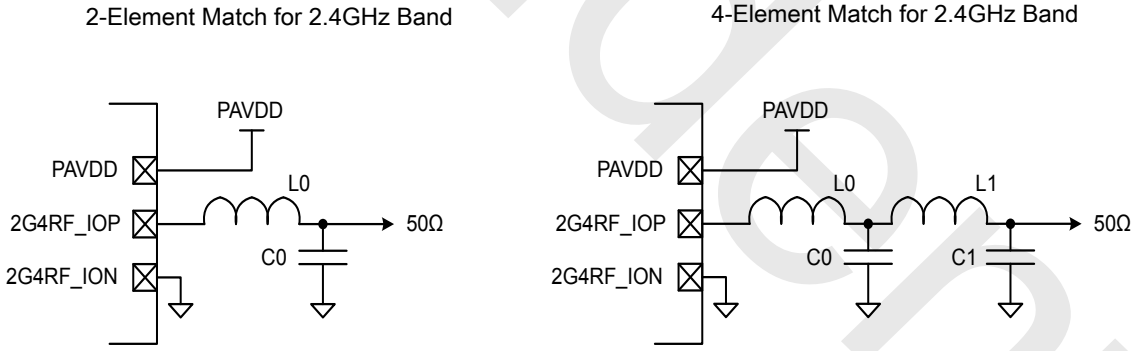


Figure 5.4. Typical 2.4 GHz RF impedance-matching network circuits

6. Pinout and Package

6.1 Pinout

The **EFR32MG1X232** pinout, including selected functionality, is shown in Figure 6.1 **EFR32MG1X232** Pinout (top view, not to scale) on page 46.

Figure 6.1. EFR32MG1X232 Pinout (top view, not to scale)

Table 6.1. Device Pinout

QFN48 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
0	VSSIO_0_0	GroundIO_0_0				
1	PF0	BUSBY BUSAX	TIM0_CC0 #24 TIM0_CC1 #23 TIM0_CC2 #22 TIM0_CDTI0 #21 TIM0_CDTI1 #20 TIM0_CDTI2 #19 TIM1_CC0 #24 TIM1_CC1 #23 TIM1_CC2 #22 TIM1_CC3 #21 LE- TIM0_OUT0 #24 LETIM0_OUT1 #23 PCNT0_S0IN #24 PCNT0_S1IN #23	US0_TX #24 US0_RX #23 US0_CLK #22 US0_CS #21 US0_CTS #20 US0_RTS #19 US1_TX #24 US1_RX #23 US1_CLK #22 US1_CS #21 US1_CTS #20 US1_RTS #19 LEU0_TX #24 LEU0_RX #23 I2C0_SDA #24 I2C0_SCL #23	FRC_DCLK #24 FRC_DOUT #23 FRC_DFRAME #22 MODEM_DCLK #24 MODEM_DIN #23 MODEM_DOUT #22 MODEM_ANT0 #21 MODEM_ANT1 #20	PRS_CH0 #0 PRS_CH1 #7 PRS_CH2 #6 PRS_CH3 #5 ACMP0_O #24 ACMP1_O #24 DBG_SWCLKTCK #0 BOOT_TX
2	PF1	BUSAY BUSBX	TIM0_CC0 #25 TIM0_CC1 #24 TIM0_CC2 #23 TIM0_CDTI0 #22 TIM0_CDTI1 #21 TIM0_CDTI2 #20 TIM1_CC0 #25 TIM1_CC1 #24 TIM1_CC2 #23 TIM1_CC3 #22 LE- TIM0_OUT0 #25 LETIM0_OUT1 #24 PCNT0_S0IN #25 PCNT0_S1IN #24	US0_TX #25 US0_RX #24 US0_CLK #23 US0_CS #22 US0_CTS #21 US0_RTS #20 US1_TX #25 US1_RX #24 US1_CLK #23 US1_CS #22 US1_CTS #21 US1_RTS #20 LEU0_TX #25 LEU0_RX #24 I2C0_SDA #25 I2C0_SCL #24	FRC_DCLK #25 FRC_DOUT #24 FRC_DFRAME #23 MODEM_DCLK #25 MODEM_DIN #24 MODEM_DOUT #23 MODEM_ANT0 #22 MODEM_ANT1 #21	PRS_CH0 #1 PRS_CH1 #0 PRS_CH2 #7 PRS_CH3 #6 ACMP0_O #25 ACMP1_O #25 DBG_SWDIOTMS #0 BOOT_RX

QFN48 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
3	PF2	BUSBY BUSAX	TIM0_CC0 #26 TIM0_CC1 #25 TIM0_CC2 #24 TIM0_CDTI0 #23 TIM0_CDTI1 #22 TIM0_CDTI2 #21 TIM1_CC0 #26 TIM1_CC1 #25 TIM1_CC2 #24 TIM1_CC3 #23 LE- TIM0_OUT0 #26 LETIM0_OUT1 #25 PCNT0_S0IN #26 PCNT0_S1IN #25	US0_TX #26 US0_RX #25 US0_CLK #24 US0_CS #23 US0_CTS #22 US0_RTS #21 US1_TX #26 US1_RX #25 US1_CLK #24 US1_CS #23 US1_CTS #22 US1_RTS #21 LEU0_TX #26 LEU0_RX #25 I2C0_SDA #26 I2C0_SCL #25	FRC_DCLK #26 FRC_DOUT #25 FRC_DFRAME #24 MODEM_DCLK #26 MODEM_DIN #25 MODEM_DOUT #24 MODEM_ANT0 #23 MODEM_ANT1 #22	CMU_CLK0 #6 PRS_CH0 #2 PRS_CH1 #1 PRS_CH2 #0 PRS_CH3 #7 ACMP0_O #26 ACMP1_O #26 DBG_TDO #0 DBG_SWO #0 GPIO_EM4WU0
4	PF3	BUSAY BUSBX	TIM0_CC0 #27 TIM0_CC1 #26 TIM0_CC2 #25 TIM0_CDTI0 #24 TIM0_CDTI1 #23 TIM0_CDTI2 #22 TIM1_CC0 #27 TIM1_CC1 #26 TIM1_CC2 #25 TIM1_CC3 #24 LE- TIM0_OUT0 #27 LETIM0_OUT1 #26 PCNT0_S0IN #27 PCNT0_S1IN #26	US0_TX #27 US0_RX #26 US0_CLK #25 US0_CS #24 US0_CTS #23 US0_RTS #22 US1_TX #27 US1_RX #26 US1_CLK #25 US1_CS #24 US1_CTS #23 US1_RTS #22 LEU0_TX #27 LEU0_RX #26 I2C0_SDA #27 I2C0_SCL #26	FRC_DCLK #27 FRC_DOUT #26 FRC_DFRAME #25 MODEM_DCLK #27 MODEM_DIN #26 MODEM_DOUT #25 MODEM_ANT0 #24 MODEM_ANT1 #23	CMU_CLK1 #6 PRS_CH0 #3 PRS_CH1 #2 PRS_CH2 #1 PRS_CH3 #0 ACMP0_O #27 ACMP1_O #27 DBG_TDI #0
5	PF4	BUSBY BUSAX	TIM0_CC0 #28 TIM0_CC1 #27 TIM0_CC2 #26 TIM0_CDTI0 #25 TIM0_CDTI1 #24 TIM0_CDTI2 #23 TIM1_CC0 #28 TIM1_CC1 #27 TIM1_CC2 #26 TIM1_CC3 #25 LE- TIM0_OUT0 #28 LETIM0_OUT1 #27 PCNT0_S0IN #28 PCNT0_S1IN #27	US0_TX #28 US0_RX #27 US0_CLK #26 US0_CS #25 US0_CTS #24 US0_RTS #23 US1_TX #28 US1_RX #27 US1_CLK #26 US1_CS #25 US1_CTS #24 US1_RTS #23 LEU0_TX #28 LEU0_RX #27 I2C0_SDA #28 I2C0_SCL #27	FRC_DCLK #28 FRC_DOUT #27 FRC_DFRAME #26 MODEM_DCLK #28 MODEM_DIN #27 MODEM_DOUT #26 MODEM_ANT0 #25 MODEM_ANT1 #24	PRS_CH0 #4 PRS_CH1 #3 PRS_CH2 #2 PRS_CH3 #1 ACMP0_O #28 ACMP1_O #28

QFN48 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
6	PF5	BUSAY BUSBX	TIM0_CC0 #29 TIM0_CC1 #28 TIM0_CC2 #27 TIM0_CDTI0 #26 TIM0_CDTI1 #25 TIM0_CDTI2 #24 TIM1_CC0 #29 TIM1_CC1 #28 TIM1_CC2 #27 TIM1_CC3 #26 LE- TIM0_OUT0 #29 LETIM0_OUT1 #28 PCNT0_S0IN #29 PCNT0_S1IN #28	US0_TX #29 US0_RX #28 US0_CLK #27 US0_CS #26 US0_CTS #25 US0_RTS #24 US1_TX #29 US1_RX #28 US1_CLK #27 US1_CS #26 US1_CTS #25 US1_RTS #24 LEU0_TX #29 LEU0_RX #28 I2C0_SDA #29 I2C0_SCL #28	FRC_DCLK #29 FRC_DOUT #28 FRC_DFRAME #27 MODEM_DCLK #29 MODEM_DIN #28 MODEM_DOUT #27 MODEM_ANT0 #26 MODEM_ANT1 #25	PRS_CH0 #5 PRS_CH1 #4 PRS_CH2 #3 PRS_CH3 #2 ACMP0_O #29 ACMP1_O #29
7	PF6	BUSBY BUSAX	TIM0_CC0 #30 TIM0_CC1 #29 TIM0_CC2 #28 TIM0_CDTI0 #27 TIM0_CDTI1 #26 TIM0_CDTI2 #25 TIM1_CC0 #30 TIM1_CC1 #29 TIM1_CC2 #28 TIM1_CC3 #27 LE- TIM0_OUT0 #30 LETIM0_OUT1 #29 PCNT0_S0IN #30 PCNT0_S1IN #29	US0_TX #30 US0_RX #29 US0_CLK #28 US0_CS #27 US0_CTS #26 US0_RTS #25 US1_TX #30 US1_RX #29 US1_CLK #28 US1_CS #27 US1_CTS #26 US1_RTS #25 LEU0_TX #30 LEU0_RX #29 I2C0_SDA #30 I2C0_SCL #29	FRC_DCLK #30 FRC_DOUT #29 FRC_DFRAME #28 MODEM_DCLK #30 MODEM_DIN #29 MODEM_DOUT #28 MODEM_ANT0 #27 MODEM_ANT1 #26	CMU_CLK1 #7 PRS_CH0 #6 PRS_CH1 #5 PRS_CH2 #4 PRS_CH3 #3 ACMP0_O #30 ACMP1_O #30
8	PF7	BUSAY BUSBX	TIM0_CC0 #31 TIM0_CC1 #30 TIM0_CC2 #29 TIM0_CDTI0 #28 TIM0_CDTI1 #27 TIM0_CDTI2 #26 TIM1_CC0 #31 TIM1_CC1 #30 TIM1_CC2 #29 TIM1_CC3 #28 LE- TIM0_OUT0 #31 LETIM0_OUT1 #30 PCNT0_S0IN #31 PCNT0_S1IN #30	US0_TX #31 US0_RX #30 US0_CLK #29 US0_CS #28 US0_CTS #27 US0_RTS #26 US1_TX #31 US1_RX #30 US1_CLK #29 US1_CS #28 US1_CTS #27 US1_RTS #26 LEU0_TX #31 LEU0_RX #30 I2C0_SDA #31 I2C0_SCL #30	FRC_DCLK #31 FRC_DOUT #30 FRC_DFRAME #29 MODEM_DCLK #31 MODEM_DIN #30 MODEM_DOUT #29 MODEM_ANT0 #28 MODEM_ANT1 #27	CMU_CLK0 #7 PRS_CH0 #7 PRS_CH1 #6 PRS_CH2 #5 PRS_CH3 #4 ACMP0_O #31 ACMP1_O #31 GPIO_EM4WU1
9	RFVDD	Radio power supply				
10	HFXTAL_N	High Frequency Crystal input pin.				
11	HFXTAL_P	High Frequency Crystal output pin.				
12	RESETn	Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.				
13	NC	No Connect.				

QFN48 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
14	RFVSS	Radio Ground				
15	PAVSS	Power Amplifier (PA) voltage regulator VSS				
16	2G4RF_ION	2.4 GHz Differential RF input/output, negative path.				
17	2G4RF_IOP	2.4 GHz Differential RF input/output, positive path.				
18	PAVDD	Power Amplifier (PA) voltage regulator VDD input				
19	PD10	BUSDY BUSCX	TIM0_CC0 #18 TIM0_CC1 #17 TIM0_CC2 #16 TIM0_CDTI0 #15 TIM0_CDTI1 #14 TIM0_CDTI2 #13 TIM1_CC0 #18 TIM1_CC1 #17 TIM1_CC2 #16 TIM1_CC3 #15 LE- TIM0_OUT0 #18 LETIM0_OUT1 #17 PCNT0_S0IN #18 PCNT0_S1IN #17	US0_TX #18 US0_RX #17 US0_CLK #16 US0_CS #15 US0_CTS #14 US0_RTS #13 US1_TX #18 US1_RX #17 US1_CLK #16 US1_CS #15 US1_CTS #14 US1_RTS #13 LEU0_TX #18 LEU0_RX #17 I2C0_SDA #18 I2C0_SCL #17	FRC_DCLK #18 FRC_DOUT #17 FRC_DFRAME #16 MODEM_DCLK #18 MODEM_DIN #17 MODEM_DOUT #16 MODEM_ANT0 #15 MODEM_ANT1 #14	CMU_CLK1 #4 PRS_CH3 #9 PRS_CH4 #1 PRS_CH5 #0 PRS_CH6 #12 ACMP0_O #18 ACMP1_O #18
20	PD11	BUSCY BUSDX	TIM0_CC0 #19 TIM0_CC1 #18 TIM0_CC2 #17 TIM0_CDTI0 #16 TIM0_CDTI1 #15 TIM0_CDTI2 #14 TIM1_CC0 #19 TIM1_CC1 #18 TIM1_CC2 #17 TIM1_CC3 #16 LE- TIM0_OUT0 #19 LETIM0_OUT1 #18 PCNT0_S0IN #19 PCNT0_S1IN #18	US0_TX #19 US0_RX #18 US0_CLK #17 US0_CS #16 US0_CTS #15 US0_RTS #14 US1_TX #19 US1_RX #18 US1_CLK #17 US1_CS #16 US1_CTS #15 US1_RTS #14 LEU0_TX #19 LEU0_RX #18 I2C0_SDA #19 I2C0_SCL #18	FRC_DCLK #19 FRC_DOUT #18 FRC_DFRAME #17 MODEM_DCLK #19 MODEM_DIN #18 MODEM_DOUT #17 MODEM_ANT0 #16 MODEM_ANT1 #15	PRS_CH3 #10 PRS_CH4 #2 PRS_CH5 #1 PRS_CH6 #13 ACMP0_O #19 ACMP1_O #19
21	PD12	BUSDY BUSCX	TIM0_CC0 #20 TIM0_CC1 #19 TIM0_CC2 #18 TIM0_CDTI0 #17 TIM0_CDTI1 #16 TIM0_CDTI2 #15 TIM1_CC0 #20 TIM1_CC1 #19 TIM1_CC2 #18 TIM1_CC3 #17 LE- TIM0_OUT0 #20 LETIM0_OUT1 #19 PCNT0_S0IN #20 PCNT0_S1IN #19	US0_TX #20 US0_RX #19 US0_CLK #18 US0_CS #17 US0_CTS #16 US0_RTS #15 US1_TX #20 US1_RX #19 US1_CLK #18 US1_CS #17 US1_CTS #16 US1_RTS #15 LEU0_TX #20 LEU0_RX #19 I2C0_SDA #20 I2C0_SCL #19	FRC_DCLK #20 FRC_DOUT #19 FRC_DFRAME #18 MODEM_DCLK #20 MODEM_DIN #19 MODEM_DOUT #18 MODEM_ANT0 #17 MODEM_ANT1 #16	PRS_CH3 #11 PRS_CH4 #3 PRS_CH5 #2 PRS_CH6 #14 ACMP0_O #20 ACMP1_O #20

QFN48 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
22	PD13	BUSCY BUSDX	TIM0_CC0 #21 TIM0_CC1 #20 TIM0_CC2 #19 TIM0_CDTI0 #18 TIM0_CDTI1 #17 TIM0_CDTI2 #16 TIM1_CC0 #21 TIM1_CC1 #20 TIM1_CC2 #19 TIM1_CC3 #18 LE- TIM0_OUT0 #21 LETIM0_OUT1 #20 PCNT0_S0IN #21 PCNT0_S1IN #20	US0_TX #21 US0_RX #20 US0_CLK #19 US0_CS #18 US0_CTS #17 US0_RTS #16 US1_TX #21 US1_RX #20 US1_CLK #19 US1_CS #18 US1_CTS #17 US1_RTS #16 LEU0_TX #21 LEU0_RX #20 I2C0_SDA #21 I2C0_SCL #20	FRC_DCLK #21 FRC_DOUT #20 FRC_DFRAME #19 MODEM_DCLK #21 MODEM_DIN #20 MODEM_DOUT #19 MODEM_ANT0 #18 MODEM_ANT1 #17	PRS_CH3 #12 PRS_CH4 #4 PRS_CH5 #3 PRS_CH6 #15 ACMP0_O #21 ACMP1_O #21
23	PD14	BUSDY BUSCX	TIM0_CC0 #22 TIM0_CC1 #21 TIM0_CC2 #20 TIM0_CDTI0 #19 TIM0_CDTI1 #18 TIM0_CDTI2 #17 TIM1_CC0 #22 TIM1_CC1 #21 TIM1_CC2 #20 TIM1_CC3 #19 LE- TIM0_OUT0 #22 LETIM0_OUT1 #21 PCNT0_S0IN #22 PCNT0_S1IN #21	US0_TX #22 US0_RX #21 US0_CLK #20 US0_CS #19 US0_CTS #18 US0_RTS #17 US1_TX #22 US1_RX #21 US1_CLK #20 US1_CS #19 US1_CTS #18 US1_RTS #17 LEU0_TX #22 LEU0_RX #21 I2C0_SDA #22 I2C0_SCL #21	FRC_DCLK #22 FRC_DOUT #21 FRC_DFRAME #20 MODEM_DCLK #22 MODEM_DIN #21 MODEM_DOUT #20 MODEM_ANT0 #19 MODEM_ANT1 #18	CMU_CLK0 #5 PRS_CH3 #13 PRS_CH4 #5 PRS_CH5 #4 PRS_CH6 #16 ACMP0_O #22 ACMP1_O #22 GPIO_EM4WU4
24	PD15	BUSCY BUSDX	TIM0_CC0 #23 TIM0_CC1 #22 TIM0_CC2 #21 TIM0_CDTI0 #20 TIM0_CDTI1 #19 TIM0_CDTI2 #18 TIM1_CC0 #23 TIM1_CC1 #22 TIM1_CC2 #21 TIM1_CC3 #20 LE- TIM0_OUT0 #23 LETIM0_OUT1 #22 PCNT0_S0IN #23 PCNT0_S1IN #22	US0_TX #23 US0_RX #22 US0_CLK #21 US0_CS #20 US0_CTS #19 US0_RTS #18 US1_TX #23 US1_RX #22 US1_CLK #21 US1_CS #20 US1_CTS #19 US1_RTS #18 LEU0_TX #23 LEU0_RX #22 I2C0_SDA #23 I2C0_SCL #22	FRC_DCLK #23 FRC_DOUT #22 FRC_DFRAME #21 MODEM_DCLK #23 MODEM_DIN #22 MODEM_DOUT #21 MODEM_ANT0 #20 MODEM_ANT1 #19	CMU_CLK1 #5 PRS_CH3 #14 PRS_CH4 #6 PRS_CH5 #5 PRS_CH6 #17 ACMP0_O #23 ACMP1_O #23 DBG_SWO #2

QFN48 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
25	PA0	BUSDY BUSCX ADC0_EXTN	TIM0_CC0 #0 TIM0_CC1 #31 TIM0_CC2 #30 TIM0_CDTI0 #29 TIM0_CDTI1 #28 TIM0_CDTI2 #27 TIM1_CC0 #0 TIM1_CC1 #31 TIM1_CC2 #30 TIM1_CC3 #29 LE-TIM0_OUT0 #0 LE-TIM0_OUT1 #31 PCNT0_S0IN #0 PCNT0_S1IN #31	US0_TX #0 US0_RX #31 US0_CLK #30 US0_CS #29 US0_CTS #28 US0_RTS #27 US1_TX #0 US1_RX #31 US1_CLK #30 US1_CS #29 US1_CTS #28 US1_RTS #27 LEU0_TX #0 LEU0_RX #31 I2C0_SDA #0 I2C0_SCL #31	FRC_DCLK #0 FRC_DOUT #31 FRC_DFRAME #30 MODEM_DCLK #0 MODEM_DIN #31 MODEM_DOUT #30 MODEM_ANT0 #29 MODEM_ANT1 #28	CMU_CLK1 #0 PRS_CH6 #0 PRS_CH7 #10 PRS_CH8 #9 PRS_CH9 #8 ACMP0_O #0 ACMP1_O #0
26	PA1	BUSCY BUSDX ADC0_EXTP	TIM0_CC0 #1 TIM0_CC1 #0 TIM0_CC2 #31 TIM0_CDTI0 #30 TIM0_CDTI1 #29 TIM0_CDTI2 #28 TIM1_CC0 #1 TIM1_CC1 #0 TIM1_CC2 #31 TIM1_CC3 #30 LE-TIM0_OUT0 #1 LE-TIM0_OUT1 #0 PCNT0_S0IN #1 PCNT0_S1IN #0	US0_TX #1 US0_RX #0 US0_CLK #31 US0_CS #30 US0_CTS #29 US0_RTS #28 US1_TX #1 US1_RX #0 US1_CLK #31 US1_CS #30 US1_CTS #29 US1_RTS #28 LEU0_TX #1 LEU0_RX #0 I2C0_SDA #1 I2C0_SCL #0	FRC_DCLK #1 FRC_DOUT #0 FRC_DFRAME #31 MODEM_DCLK #1 MODEM_DIN #0 MODEM_DOUT #31 MODEM_ANT0 #30 MODEM_ANT1 #29	CMU_CLK0 #0 PRS_CH6 #1 PRS_CH7 #0 PRS_CH8 #10 PRS_CH9 #9 ACMP0_O #1 ACMP1_O #1
27	PA2	BUSDY BUSCX	TIM0_CC0 #2 TIM0_CC1 #1 TIM0_CC2 #0 TIM0_CDTI0 #31 TIM0_CDTI1 #30 TIM0_CDTI2 #29 TIM1_CC0 #2 TIM1_CC1 #1 TIM1_CC2 #0 TIM1_CC3 #31 LE-TIM0_OUT0 #2 LE-TIM0_OUT1 #1 PCNT0_S0IN #2 PCNT0_S1IN #1	US0_TX #2 US0_RX #1 US0_CLK #0 US0_CS #31 US0_CTS #30 US0_RTS #29 US1_TX #2 US1_RX #1 US1_CLK #0 US1_CS #31 US1_CTS #30 US1_RTS #29 LEU0_TX #2 LEU0_RX #1 I2C0_SDA #2 I2C0_SCL #1	FRC_DCLK #2 FRC_DOUT #1 FRC_DFRAME #0 MODEM_DCLK #2 MODEM_DIN #1 MODEM_DOUT #0 MODEM_ANT0 #31 MODEM_ANT1 #30	PRS_CH6 #2 PRS_CH7 #1 PRS_CH8 #0 PRS_CH9 #10 ACMP0_O #2 ACMP1_O #2

QFN48 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
28	PA3	BUSCY BUSDX	TIM0_CC0 #3 TIM0_CC1 #2 TIM0_CC2 #1 TIM0_CDTI0 #0 TIM0_CDTI1 #31 TIM0_CDTI2 #30 TIM1_CC0 #3 TIM1_CC1 #2 TIM1_CC2 #1 TIM1_CC3 #0 LE- TIM0_OUT0 #3 LE- TIM0_OUT1 #2 PCNT0_S0IN #3 PCNT0_S1IN #2	US0_TX #3 US0_RX #2 US0_CLK #1 US0_CS #0 US0_CTS #31 US0_RTS #30 US1_TX #3 US1_RX #2 US1_CLK #1 US1_CS #0 US1_CTS #31 US1_RTS #30 LEU0_TX #3 LEU0_RX #2 I2C0_SDA #3 I2C0_SCL #2	FRC_DCLK #3 FRC_DOUT #2 FRC_DFRAME #1 MODEM_DCLK #3 MODEM_DIN #2 MODEM_DOUT #1 MODEM_ANT0 #0 MODEM_ANT1 #31	PRS_CH6 #3 PRS_CH7 #2 PRS_CH8 #1 PRS_CH9 #0 ACMP0_O #3 ACMP1_O #3 GPIO_EM4WU8
29	PA4	BUSDY BUSCX	TIM0_CC0 #4 TIM0_CC1 #3 TIM0_CC2 #2 TIM0_CDTI0 #1 TIM0_CDTI1 #0 TIM0_CDTI2 #31 TIM1_CC0 #4 TIM1_CC1 #3 TIM1_CC2 #2 TIM1_CC3 #1 LE- TIM0_OUT0 #4 LE- TIM0_OUT1 #3 PCNT0_S0IN #4 PCNT0_S1IN #3	US0_TX #4 US0_RX #3 US0_CLK #2 US0_CS #1 US0_CTS #0 US0_RTS #31 US1_TX #4 US1_RX #3 US1_CLK #2 US1_CS #1 US1_CTS #0 US1_RTS #31 LEU0_TX #4 LEU0_RX #3 I2C0_SDA #4 I2C0_SCL #3	FRC_DCLK #4 FRC_DOUT #3 FRC_DFRAME #2 MODEM_DCLK #4 MODEM_DIN #3 MODEM_DOUT #2 MODEM_ANT0 #1 MODEM_ANT1 #0	PRS_CH6 #4 PRS_CH7 #3 PRS_CH8 #2 PRS_CH9 #1 ACMP0_O #4 ACMP1_O #4
30	PA5	BUSCY BUSDX	TIM0_CC0 #5 TIM0_CC1 #4 TIM0_CC2 #3 TIM0_CDTI0 #2 TIM0_CDTI1 #1 TIM0_CDTI2 #0 TIM1_CC0 #5 TIM1_CC1 #4 TIM1_CC2 #3 TIM1_CC3 #2 LE- TIM0_OUT0 #5 LE- TIM0_OUT1 #4 PCNT0_S0IN #5 PCNT0_S1IN #4	US0_TX #5 US0_RX #4 US0_CLK #3 US0_CS #2 US0_CTS #1 US0_RTS #0 US1_TX #5 US1_RX #4 US1_CLK #3 US1_CS #2 US1_CTS #1 US1_RTS #0 LEU0_TX #5 LEU0_RX #4 I2C0_SDA #5 I2C0_SCL #4	FRC_DCLK #5 FRC_DOUT #4 FRC_DFRAME #3 MODEM_DCLK #5 MODEM_DIN #4 MODEM_DOUT #3 MODEM_ANT0 #2 MODEM_ANT1 #1	PRS_CH6 #5 PRS_CH7 #4 PRS_CH8 #3 PRS_CH9 #2 ACMP0_O #5 ACMP1_O #5

QFN48 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
31	PB11	BUSCY BUSDX	TIM0_CC0 #6 TIM0_CC1 #5 TIM0_CC2 #4 TIM0_CDTI0 #3 TIM0_CDTI1 #2 TIM0_CDTI2 #1 TIM1_CC0 #6 TIM1_CC1 #5 TIM1_CC2 #4 TIM1_CC3 #3 LE- TIM0_OUT0 #6 LE- TIM0_OUT1 #5 PCNT0_S0IN #6 PCNT0_S1IN #5	US0_TX #6 US0_RX #5 US0_CLK #4 US0_CS #3 US0_CTS #2 US0_RTS #1 US1_TX #6 US1_RX #5 US1_CLK #4 US1_CS #3 US1_CTS #2 US1_RTS #1 LEU0_TX #6 LEU0_RX #5 I2C0_SDA #6 I2C0_SCL #5	FRC_DCLK #6 FRC_DOUT #5 FRC_DFRAME #4 MODEM_DCLK #6 MODEM_DIN #5 MODEM_DOUT #4 MODEM_ANT0 #3 MODEM_ANT1 #2	PRS_CH6 #6 PRS_CH7 #5 PRS_CH8 #4 PRS_CH9 #3 ACMP0_O #6 ACMP1_O #6
32	PB12	BUSDY BUSCX	TIM0_CC0 #7 TIM0_CC1 #6 TIM0_CC2 #5 TIM0_CDTI0 #4 TIM0_CDTI1 #3 TIM0_CDTI2 #2 TIM1_CC0 #7 TIM1_CC1 #6 TIM1_CC2 #5 TIM1_CC3 #4 LE- TIM0_OUT0 #7 LE- TIM0_OUT1 #6 PCNT0_S0IN #7 PCNT0_S1IN #6	US0_TX #7 US0_RX #6 US0_CLK #5 US0_CS #4 US0_CTS #3 US0_RTS #2 US1_TX #7 US1_RX #6 US1_CLK #5 US1_CS #4 US1_CTS #3 US1_RTS #2 LEU0_TX #7 LEU0_RX #6 I2C0_SDA #7 I2C0_SCL #6	FRC_DCLK #7 FRC_DOUT #6 FRC_DFRAME #5 MODEM_DCLK #7 MODEM_DIN #6 MODEM_DOUT #5 MODEM_ANT0 #4 MODEM_ANT1 #3	PRS_CH6 #7 PRS_CH7 #6 PRS_CH8 #5 PRS_CH9 #4 ACMP0_O #7 ACMP1_O #7
33	PB13	BUSCY BUSDX	TIM0_CC0 #8 TIM0_CC1 #7 TIM0_CC2 #6 TIM0_CDTI0 #5 TIM0_CDTI1 #4 TIM0_CDTI2 #3 TIM1_CC0 #8 TIM1_CC1 #7 TIM1_CC2 #6 TIM1_CC3 #5 LE- TIM0_OUT0 #8 LE- TIM0_OUT1 #7 PCNT0_S0IN #8 PCNT0_S1IN #7	US0_TX #8 US0_RX #7 US0_CLK #6 US0_CS #5 US0_CTS #4 US0_RTS #3 US1_TX #8 US1_RX #7 US1_CLK #6 US1_CS #5 US1_CTS #4 US1_RTS #3 LEU0_TX #8 LEU0_RX #7 I2C0_SDA #8 I2C0_SCL #7	FRC_DCLK #8 FRC_DOUT #7 FRC_DFRAME #6 MODEM_DCLK #8 MODEM_DIN #7 MODEM_DOUT #6 MODEM_ANT0 #5 MODEM_ANT1 #4	PRS_CH6 #8 PRS_CH7 #7 PRS_CH8 #6 PRS_CH9 #5 ACMP0_O #8 ACMP1_O #8 DBG_SWO #1 GPIO_EM4WU9
34	AVDD	Analog power supply.				

QFN48 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
35	PB14	BUSDY BUSCX LFXTAL_N	TIM0_CC0 #9 TIM0_CC1 #8 TIM0_CC2 #7 TIM0_CDTI0 #6 TIM0_CDTI1 #5 TIM0_CDTI2 #4 TIM1_CC0 #9 TIM1_CC1 #8 TIM1_CC2 #7 TIM1_CC3 #6 LE-TIM0_OUT0 #9 LE-TIM0_OUT1 #8 PCNT0_S0IN #9 PCNT0_S1IN #8	US0_TX #9 US0_RX #8 US0_CLK #7 US0_CS #6 US0_CTS #5 US0_RTS #4 US1_TX #9 US1_RX #8 US1_CLK #7 US1_CS #6 US1_CTS #5 US1_RTS #4 LEU0_TX #9 LEU0_RX #8 I2C0_SDA #9 I2C0_SCL #8	FRC_DCLK #9 FRC_DOUT #8 FRC_DFRAME #7 MODEM_DCLK #9 MODEM_DIN #8 MODEM_DOUT #7 MODEM_ANT0 #6 MODEM_ANT1 #5	CMU_CLK1 #1 PRS_CH6 #9 PRS_CH7 #8 PRS_CH8 #7 PRS_CH9 #6 ACMP0_O #9 ACMP1_O #9
36	PB15	BUSCY BUSDX LFXTAL_P	TIM0_CC0 #10 TIM0_CC1 #9 TIM0_CC2 #8 TIM0_CDTI0 #7 TIM0_CDTI1 #6 TIM0_CDTI2 #5 TIM1_CC0 #10 TIM1_CC1 #9 TIM1_CC2 #8 TIM1_CC3 #7 LE-TIM0_OUT0 #10 LETIM0_OUT1 #9 PCNT0_S0IN #10 PCNT0_S1IN #9	US0_TX #10 US0_RX #9 US0_CLK #8 US0_CS #7 US0_CTS #6 US0_RTS #5 US1_TX #10 US1_RX #9 US1_CLK #8 US1_CS #7 US1_CTS #6 US1_RTS #5 LEU0_TX #10 LEU0_RX #9 I2C0_SDA #10 I2C0_SCL #9	FRC_DCLK #10 FRC_DOUT #9 FRC_DFRAME #8 MODEM_DCLK #10 MODEM_DIN #9 MODEM_DOUT #8 MODEM_ANT0 #7 MODEM_ANT1 #6	CMU_CLK0 #1 PRS_CH6 #10 PRS_CH7 #9 PRS_CH8 #8 PRS_CH9 #7 ACMP0_O #10 ACMP1_O #10
37	VREGVSS	Voltage regulator VSS				
38	VREGSW	DCDC regulator switching node				
39	VREGVDD	Voltage regulator VDD input				
40	DVDD	Digital power supply.				
41	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.				
42	IOVDD	Digital IO power supply.				

QFN48 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
43	PC6	BUSBY BUSAX	TIM0_CC0 #11 TIM0_CC1 #10 TIM0_CC2 #9 TIM0_CDTI0 #8 TIM0_CDTI1 #7 TIM0_CDTI2 #6 TIM1_CC0 #11 TIM1_CC1 #10 TIM1_CC2 #9 TIM1_CC3 #8 LE- TIM0_OUT0 #11 LE- TIM0_OUT1 #10 PCNT0_S0IN #11 PCNT0_S1IN #10	US0_TX #11 US0_RX #10 US0_CLK #9 US0_CS #8 US0_CTS #7 US0_RTS #6 US1_TX #11 US1_RX #10 US1_CLK #9 US1_CS #8 US1_CTS #7 US1_RTS #6 LEU0_TX #11 LEU0_RX #10 I2C0_SDA #11 I2C0_SCL #10	FRC_DCLK #11 FRC_DOUT #10 FRC_DFRAME #9 MODEM_DCLK #11 MODEM_DIN #10 MODEM_DOUT #9 MODEM_ANT0 #8 MODEM_ANT1 #7	CMU_CLK0 #2 PRS_CH0 #8 PRS_CH9 #11 PRS_CH10 #0 PRS_CH11 #5 ACMP0_O #11 ACMP1_O #11
44	PC7	BUSAY BUSBX	TIM0_CC0 #12 TIM0_CC1 #11 TIM0_CC2 #10 TIM0_CDTI0 #9 TIM0_CDTI1 #8 TIM0_CDTI2 #7 TIM1_CC0 #12 TIM1_CC1 #11 TIM1_CC2 #10 TIM1_CC3 #9 LE- TIM0_OUT0 #12 LETIM0_OUT1 #11 PCNT0_S0IN #12 PCNT0_S1IN #11	US0_TX #12 US0_RX #11 US0_CLK #10 US0_CS #9 US0_CTS #8 US0_RTS #7 US1_TX #12 US1_RX #11 US1_CLK #10 US1_CS #9 US1_CTS #8 US1_RTS #7 LEU0_TX #12 LEU0_RX #11 I2C0_SDA #12 I2C0_SCL #11	FRC_DCLK #12 FRC_DOUT #11 FRC_DFRAME #10 MODEM_DCLK #12 MODEM_DIN #11 MODEM_DOUT #10 MODEM_ANT0 #9 MODEM_ANT1 #8	CMU_CLK1 #2 PRS_CH0 #9 PRS_CH9 #12 PRS_CH10 #1 PRS_CH11 #0 ACMP0_O #12 ACMP1_O #12
45	PC8	BUSBY BUSAX	TIM0_CC0 #13 TIM0_CC1 #12 TIM0_CC2 #11 TIM0_CDTI0 #10 TIM0_CDTI1 #9 TIM0_CDTI2 #8 TIM1_CC0 #13 TIM1_CC1 #12 TIM1_CC2 #11 TIM1_CC3 #10 LE- TIM0_OUT0 #13 LETIM0_OUT1 #12 PCNT0_S0IN #13 PCNT0_S1IN #12	US0_TX #13 US0_RX #12 US0_CLK #11 US0_CS #10 US0_CTS #9 US0_RTS #8 US1_TX #13 US1_RX #12 US1_CLK #11 US1_CS #10 US1_CTS #9 US1_RTS #8 LEU0_TX #13 LEU0_RX #12 I2C0_SDA #13 I2C0_SCL #12	FRC_DCLK #13 FRC_DOUT #12 FRC_DFRAME #11 MODEM_DCLK #13 MODEM_DIN #12 MODEM_DOUT #11 MODEM_ANT0 #10 MODEM_ANT1 #9	PRS_CH0 #10 PRS_CH9 #13 PRS_CH10 #2 PRS_CH11 #1 ACMP0_O #13 ACMP1_O #13

QFN48 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
46	PC9	BUSAY BUSBX	TIM0_CC0 #14 TIM0_CC1 #13 TIM0_CC2 #12 TIM0_CDTI0 #11 TIM0_CDTI1 #10 TIM0_CDTI2 #9 TIM1_CC0 #14 TIM1_CC1 #13 TIM1_CC2 #12 TIM1_CC3 #11 LE- TIM0_OUT0 #14 LETIM0_OUT1 #13 PCNT0_S0IN #14 PCNT0_S1IN #13	US0_TX #14 US0_RX #13 US0_CLK #12 US0_CS #11 US0_CTS #10 US0_RTS #9 US1_TX #14 US1_RX #13 US1_CLK #12 US1_CS #11 US1_CTS #10 US1_RTS #9 LEU0_TX #14 LEU0_RX #13 I2C0_SDA #14 I2C0_SCL #13	FRC_DCLK #14 FRC_DOUT #13 FRC_DFRAME #12 MODEM_DCLK #14 MODEM_DIN #13 MODEM_DOUT #12 MODEM_ANT0 #11 MODEM_ANT1 #10	PRS_CH0 #11 PRS_CH9 #14 PRS_CH10 #3 PRS_CH11 #2 ACMP0_O #14 ACMP1_O #14
47	PC10	BUSBY BUSAX	TIM0_CC0 #15 TIM0_CC1 #14 TIM0_CC2 #13 TIM0_CDTI0 #12 TIM0_CDTI1 #11 TIM0_CDTI2 #10 TIM1_CC0 #15 TIM1_CC1 #14 TIM1_CC2 #13 TIM1_CC3 #12 LE- TIM0_OUT0 #15 LETIM0_OUT1 #14 PCNT0_S0IN #15 PCNT0_S1IN #14	US0_TX #15 US0_RX #14 US0_CLK #13 US0_CS #12 US0_CTS #11 US0_RTS #10 US1_TX #15 US1_RX #14 US1_CLK #13 US1_CS #12 US1_CTS #11 US1_RTS #10 LEU0_TX #15 LEU0_RX #14 I2C0_SDA #15 I2C0_SCL #14	FRC_DCLK #15 FRC_DOUT #14 FRC_DFRAME #13 MODEM_DCLK #15 MODEM_DIN #14 MODEM_DOUT #13 MODEM_ANT0 #12 MODEM_ANT1 #11	CMU_CLK1 #3 PRS_CH0 #12 PRS_CH9 #15 PRS_CH10 #4 PRS_CH11 #3 ACMP0_O #15 ACMP1_O #15 GPIO_EM4WU12
48	PC11	BUSAY BUSBX	TIM0_CC0 #16 TIM0_CC1 #15 TIM0_CC2 #14 TIM0_CDTI0 #13 TIM0_CDTI1 #12 TIM0_CDTI2 #11 TIM1_CC0 #16 TIM1_CC1 #15 TIM1_CC2 #14 TIM1_CC3 #13 LE- TIM0_OUT0 #16 LETIM0_OUT1 #15 PCNT0_S0IN #16 PCNT0_S1IN #15	US0_TX #16 US0_RX #15 US0_CLK #14 US0_CS #13 US0_CTS #12 US0_RTS #11 US1_TX #16 US1_RX #15 US1_CLK #14 US1_CS #13 US1_CTS #12 US1_RTS #11 LEU0_TX #16 LEU0_RX #15 I2C0_SDA #16 I2C0_SCL #15	FRC_DCLK #16 FRC_DOUT #15 FRC_DFRAME #14 MODEM_DCLK #16 MODEM_DIN #15 MODEM_DOUT #14 MODEM_ANT0 #13 MODEM_ANT1 #12	CMU_CLK0 #3 PRS_CH0 #13 PRS_CH9 #16 PRS_CH10 #5 PRS_CH11 #4 ACMP0_O #16 ACMP1_O #16 DBG_SWO #3

6.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 6.2. Alternate functionality overview

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
ACMP0_O	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Analog comparator ACMP0, digital output.
ACMP1_O	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Analog comparator ACMP1, digital output.
ADC0_EXTN	0: PA0								Analog to digital converter ADC0 external reference input negative pin
ADC0_EXTP	0: PA1								Analog to digital converter ADC0 external reference input positive pin
BOOT_RX	0: PF1								Bootloader RX
BOOT_TX	0: PF0								Bootloader TX
CMU_CLK0	0: PA1 1: PB15 2: PC6 3: PC11	5: PD14 6: PF2 7: PF7							Clock Management Unit, clock output number 0.
CMU_CLK1	0: PA0 1: PB14 2: PC7 3: PC10	4: PD10 5: PD15 6: PF3 7: PF6							Clock Management Unit, clock output number 1.
DBG_SWCLKTCK	0: PF0								Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to pin out of reset, and has a built-in pull down.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
DBG_SWDIOTMS	0: PF1								Debug-interface Serial Wire data input / output and JTAG Test Mode Select. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	0: PF2 1: PB13 2: PD15 3: PC11								Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
DBG_TDI	0: PF3								Debug-interface JTAG Test Data In. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_TDO	0: PF2								Debug-interface JTAG Test Data Out. Note that this function is enabled to pin out of reset.
FRC_DCLK	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Frame Controller, Data Sniffer Clock.
FRC_DFRAME	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Frame Controller, Data Sniffer Frame active
FRC_DOUT	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Frame Controller, Data Sniffer Output.
GPIO_EM4WU0	0: PF2								Pin can be used to wake the system up from EM4
GPIO_EM4WU1	0: PF7								Pin can be used to wake the system up from EM4

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
GPIO_EM4WU4	0: PD14								Pin can be used to wake the system up from EM4
GPIO_EM4WU8	0: PA3								Pin can be used to wake the system up from EM4
GPIO_EM4WU9	0: PB13								Pin can be used to wake the system up from EM4
GPIO_EM4WU12	0: PC10								Pin can be used to wake the system up from EM4
I2C0_SCL	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	I2C0 Serial Clock Line input / output.
I2C0_SDA	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	I2C0 Serial Data input / output.
LETIM0_OUT0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Low Energy Timer LETIM0, output channel 1.
LEU0_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	LEUART0 Receive input.
LEU0_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	0: PB14								Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	0: PB15								Low Frequency Crystal (typically 32.768 kHz) positive pin.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
MODEM_ANT0	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	MODEM antenna control output 0, used for antenna diversity.
MODEM_ANT1	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	MODEM antenna control output 1, used for antenna diversity.
MODEM_DCLK	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	MODEM data clock out.
MODEM_DIN	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	MODEM data in.
MODEM_DOUT	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	MODEM data out.
PCNT0_S0IN	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Pulse Counter PCNT0 input number 1.
PRS_CH0	0: PF0 1: PF1 2: PF2 3: PF3	4: PF4 5: PF5 6: PF6 7: PF7	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11					Peripheral Reflex System PRS, channel 0.
PRS_CH1	0: PF1 1: PF2 2: PF3 3: PF4	4: PF5 5: PF6 6: PF7 7: PF0							Peripheral Reflex System PRS, channel 1.
PRS_CH2	0: PF2 1: PF3 2: PF4 3: PF5	4: PF6 5: PF7 6: PF0 7: PF1							Peripheral Reflex System PRS, channel 2.
PRS_CH3	0: PF3 1: PF4 2: PF5 3: PF6	4: PF7 5: PF0 6: PF1 7: PF2	9: PD10 10: PD11 11: PD12	12: PD13 13: PD14 14: PD15					Peripheral Reflex System PRS, channel 3.
PRS_CH4	1: PD10 2: PD11 3: PD12	4: PD13 5: PD14 6: PD15							Peripheral Reflex System PRS, channel 4.
PRS_CH5	0: PD10 1: PD11 2: PD12 3: PD13	4: PD14 5: PD15							Peripheral Reflex System PRS, channel 5.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
PRS_CH6	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15	12: PD10 13: PD11 14: PD12 15: PD13	16: PD14 17: PD15				Peripheral Reflex System PRS, channel 6.
PRS_CH7	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PA0						Peripheral Reflex System PRS, channel 7.
PRS_CH8	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PA0 10: PA1						Peripheral Reflex System PRS, channel 8.
PRS_CH9	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PA0 9: PA1 10: PA2 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11				Peripheral Reflex System PRS, channel 9.
PRS_CH10	0: PC6 1: PC7 2: PC8 3: PC9	4: PC10 5: PC11							Peripheral Reflex System PRS, channel 10.
PRS_CH11	0: PC7 1: PC8 2: PC9 3: PC10	4: PC11 5: PC6							Peripheral Reflex System PRS, channel 11.
TIM0_CC0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	0: PA5 1: PB11 2: PB12 3: PB13	4: PB14 5: PB15 6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11	 13: PD10 14: PD11 15: PD12	16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Timer 1 Capture Compare input / output channel 0.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
TIM1_CC1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Timer 1 Capture Compare input / output channel 2.
TIM1_CC3	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	Timer 1 Capture Compare input / output channel 3.
US0_CLK	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	USART0 clock input / output.
US0_CS	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	USART0 chip select input / output.
US0_CTS	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	USART0 clear to send hardware flow control input.
US0_RTS	0: PA5 1: PB11 2: PB12 3: PB13	4: PB14 5: PB15 6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11	13: PD10 14: PD11 15: PD12	16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	USART0 request to send hardware flow control output.
US0_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	USART1 clock input / output.
US1_CS	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	USART1 chip select input / output.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
US1_CTS	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	USART1 clear to send hardware flow control input.
US1_RTS	0: PA5 1: PB11 2: PB12 3: PB13	4: PB14 5: PB15 6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11	 13: PD10 14: PD11 15: PD12	16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	USART1 request to send hardware flow control output.
US1_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

6.3 GPIO Pinout Overview

The GPIO pins are organized as 16-bit ports indicated by letters A through F, and the individual pins on each port is indicated by a number from 15 down to 0.

Table 6.3. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	-	-	-	-	-	PA5 (5V)	PA4 (5V)	PA3 (5V)	PA2 (5V)	PA1	PA0
Port B	PB15	PB14	PB13 (5V)	PB12 (5V)	PB11 (5V)	-	-	-	-	-	-	-	-	-	-	-
Port C	-	-	-	-	PC11 (5V)	PC10 (5V)	PC9 (5V)	PC8 (5V)	PC7 (5V)	PC6 (5V)	-	-	-	-	-	-
Port D	PD15 (5V)	PD14 (5V)	PD13 (5V)	PD12 (5V)	PD11 (5V)	PD10 (5V)	-	-	-	-	-	-	-	-	-	-
Port E	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	PF7 (5V)	PF6 (5V)	PF5 (5V)	PF4 (5V)	PF3 (5V)	PF2 (5V)	PF1 (5V)	PF0 (5V)

6.4 Analog Port (APORT)

The Analog Port (APORT) is an infrastructure used to connect chip pins with on-chip analog clients such as analog comparators, ADCs, and DACs. The APORT consists of wires, switches, and control needed to configurably implement the routes. Please see EFR32 Reference Manual for complete description.

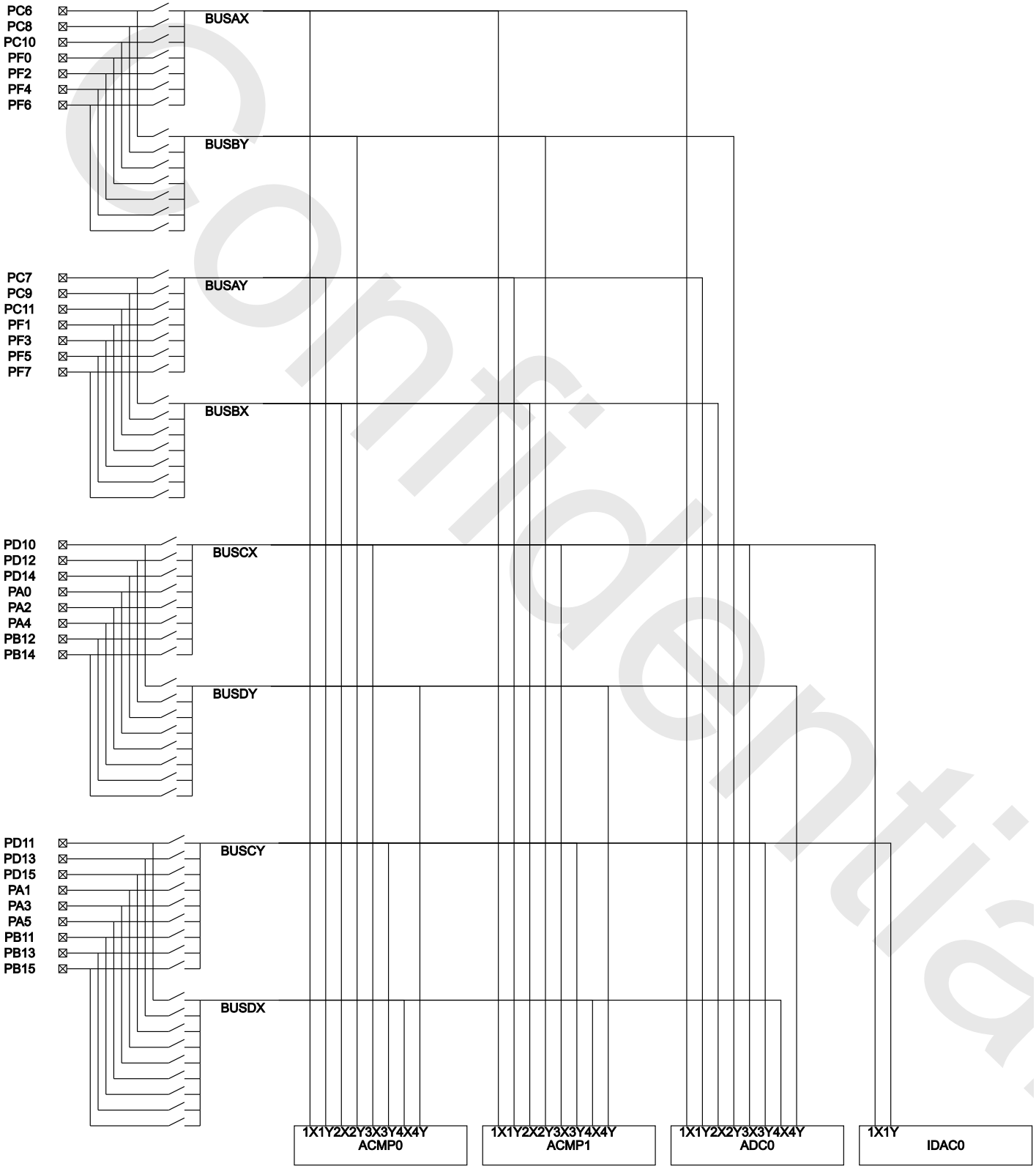


Figure 6.2. EFR32MG1X232 APORT

Table 6.4. APORT Client Map

Analog Module	Analog Module Channel	Shared Bus	Pin
ACMP0	APORT1XCH6	BUSAX	PC6
	APORT1XCH8		PC8
	APORT1XCH10		PC10
	APORT1XCH16		PF0
	APORT1XCH18		PF2
	APORT1XCH20		PF4
	APORT1XCH22		PF6
	APORT1YCH7	BUSAY	PC7
	APORT1YCH9		PC9
	APORT1YCH11		PC11
	APORT1YCH17		PF1
	APORT1YCH19		PF3
	APORT1YCH21		PF5
	APORT1YCH23		PF7
	APORT2XCH7	BUSBX	PC7
	APORT2XCH9		PC9
	APORT2XCH11		PC11
	APORT2XCH17		PF1
	APORT2XCH19		PF3
	APORT2XCH21		PF5
	APORT2XCH23		PF7
	APORT2YCH6	BUSBY	PC6
	APORT2YCH8		PC8
	APORT2YCH10		PC10
	APORT2YCH16		PF0
	APORT2YCH18		PF2
	APORT2YCH20		PF4
	APORT2YCH22		PF6
	APORT3XCH2	BUSCX	PD10
	APORT3XCH4		PD12
	APORT3XCH6		PD14
	APORT3XCH8		PA0
	APORT3XCH10		PA2
	APORT3XCH12		PA4
	APORT3XCH28		PB12
	APORT3XCH30		PB14

Analog Module	Analog Module Channel	Shared Bus	Pin
ACMP1	APORT1XCH6	BUSAX	PC6
	APORT1XCH8		PC8
	APORT1XCH10		PC10
	APORT1XCH16		PF0
	APORT1XCH18		PF2
	APORT1XCH20		PF4
	APORT1XCH22		PF6
	APORT1YCH7	BUSAY	PC7
	APORT1YCH9		PC9
	APORT1YCH11		PC11
	APORT1YCH17		PF1
	APORT1YCH19		PF3
	APORT1YCH21		PF5
	APORT1YCH23		PF7
	APORT2XCH7	BUSBX	PC7
	APORT2XCH9		PC9
	APORT2XCH11		PC11
	APORT2XCH17		PF1
	APORT2XCH19		PF3
	APORT2XCH21		PF5
	APORT2XCH23		PF7
	APORT2YCH6	BUSBY	PC6
	APORT2YCH8		PC8
	APORT2YCH10		PC10
	APORT2YCH16		PF0
	APORT2YCH18		PF2
	APORT2YCH20		PF4
	APORT2YCH22		PF6
	APORT3XCH2	BUSCX	PD10
	APORT3XCH4		PD12
	APORT3XCH6		PD14
	APORT3XCH8		PA0
	APORT3XCH10		PA2
	APORT3XCH12		PA4
	APORT3XCH28		PB12
	APORT3XCH30		PB14
	APORT3YCH3	BUSCY	PD11
	APORT3YCH5		PD13

Analog Module	Analog Module Channel	Shared Bus	Pin
ADC0	APORT1XCH6	BUSAX	PC6
	APORT1XCH8		PC8
	APORT1XCH10		PC10
	APORT1XCH16		PF0
	APORT1XCH18		PF2
	APORT1XCH20		PF4
	APORT1XCH22		PF6
	APORT1YCH7	BUSAY	PC7
	APORT1YCH9		PC9
	APORT1YCH11		PC11
	APORT1YCH17		PF1
	APORT1YCH19		PF3
	APORT1YCH21		PF5
	APORT1YCH23		PF7
	APORT2XCH7	BUSBX	PC7
	APORT2XCH9		PC9
	APORT2XCH11		PC11
	APORT2XCH17		PF1
	APORT2XCH19		PF3
	APORT2XCH21		PF5
	APORT2XCH23		PF7
	APORT2YCH6	BUSBY	PC6
	APORT2YCH8		PC8
	APORT2YCH10		PC10
	APORT2YCH16		PF0
	APORT2YCH18		PF2
	APORT2YCH20		PF4
	APORT2YCH22		PF6
	APORT3XCH2	BUSCX	PD10
	APORT3XCH4		PD12
	APORT3XCH6		PD14
	APORT3XCH8		PA0
	APORT3XCH10		PA2
	APORT3XCH12		PA4
	APORT3XCH28		PB12
	APORT3XCH30		PB14
	APORT3YCH3	BUSCY	PD11
	APORT3YCH5		PD13

Analog Module	Analog Module Channel	Shared Bus	Pin
IDAC0	APORT1XCH2	BUSCX	PD10
	APORT1XCH4		PD12
	APORT1XCH6		PD14
	APORT1XCH8		PA0
	APORT1XCH10		PA2
	APORT1XCH12		PA4
	APORT1XCH28		PB12
	APORT1XCH30		PB14
	APORT1YCH3	BUSCY	PD11
	APORT1YCH5		PD13
	APORT1YCH7		PD15
	APORT1YCH9		PA1
	APORT1YCH11		PA3
	APORT1YCH13		PA5
	APORT1YCH27		PB11
	APORT1YCH29		PB13
	APORT1YCH31		PB15

6.5 QFN48 Package Dimensions

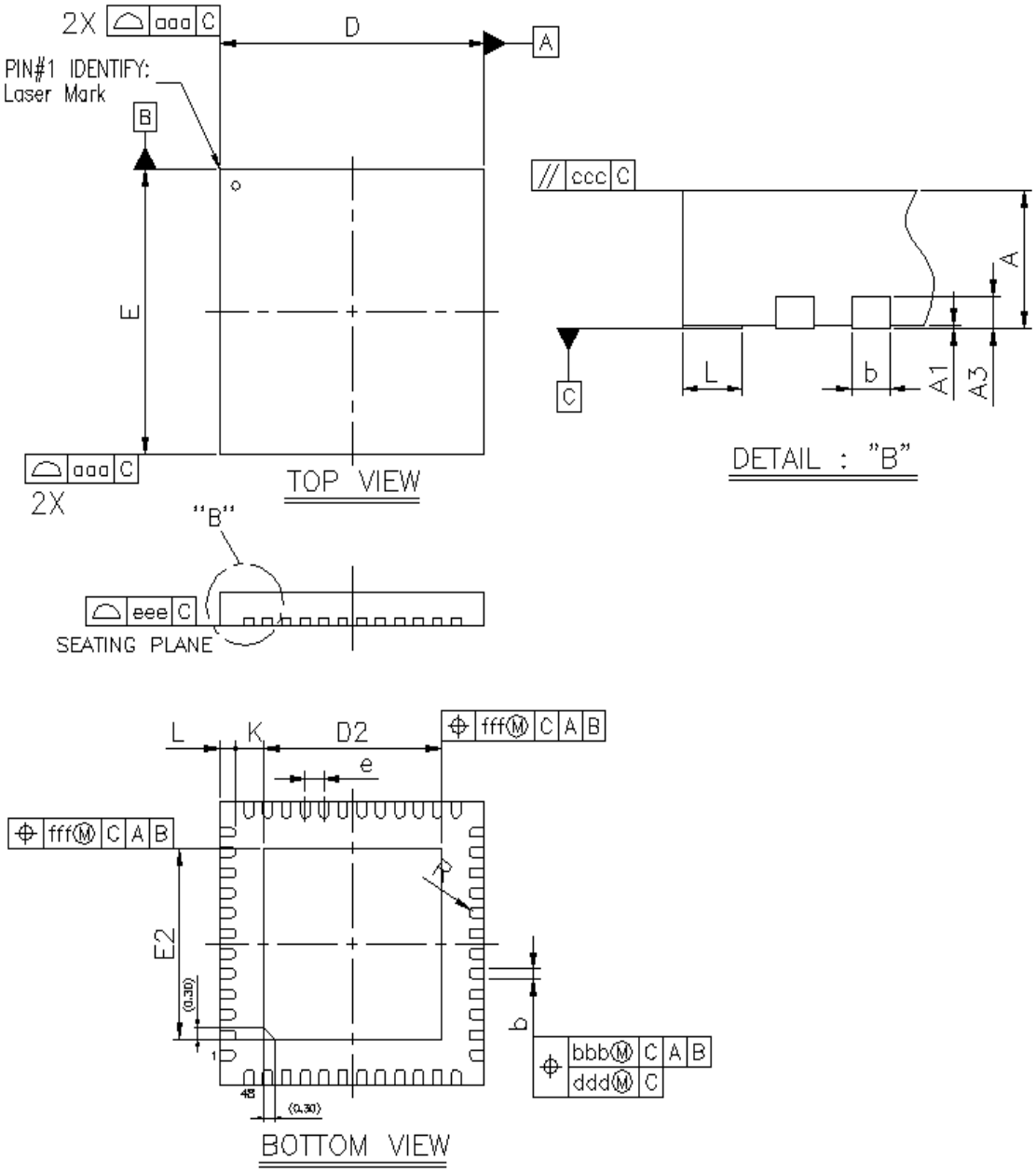


Figure 6.3. QFN48 Package Drawing

Table 6.5. QFN48 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D	6.90	7.00	7.10

Dimension	Min	Typ	Max
E	6.90	7.00	7.10
D2	4.60	4.70	4.80
E2	4.60	4.70	4.80
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
R	0.09	—	0.14
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.6 QFN48 PCB Land Pattern

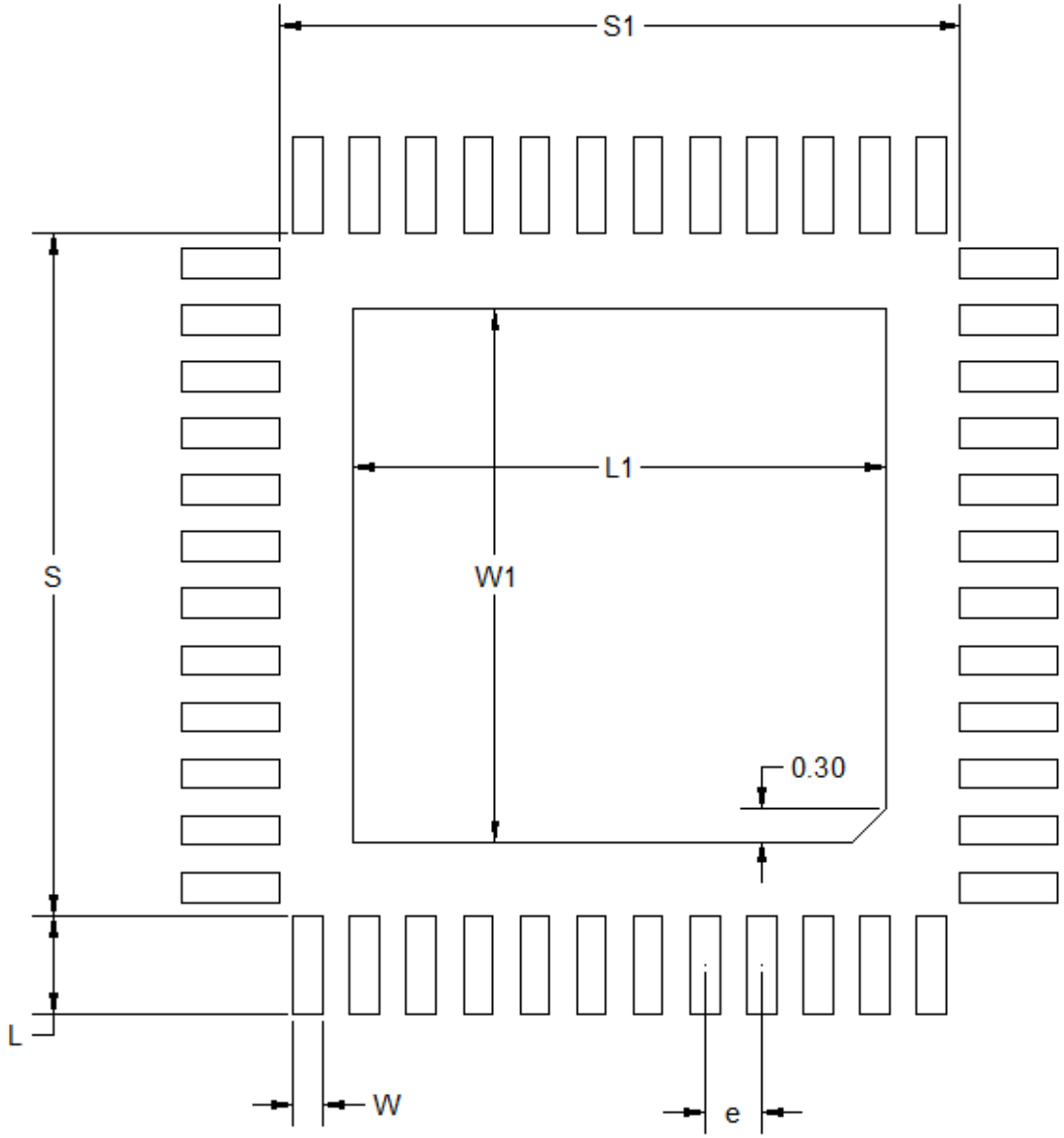


Figure 6.4. QFN48 PCB Land Pattern Drawing

Table 6.6. QFN48 PCB Land Pattern Dimensions

Dimension	Typ
S1	6.01
S	6.01
L1	4.70
W1	4.70
e	0.50
W	0.26

Dimension	Typ
L	0.86

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
7. A 4x4 array of 0.75 mm square openings on a 1.00 mm pitch can be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.7 QFN48 Package Marking

Figure 6.5. QFN48 Package Marking

The package marking consists of:

- PPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # - The firmware revision.

7. Revision History

7.1 Revision 0.71

2015-09-08

Revisions specific to Mighty Gecko

- Front Page: Key Features
- Section 1. Features. Modulation Formats Supported, 2.4GHz-only devices
- Section 3.3.4 Receiver Architecture
- Section 3.3.8 Flexible Frame Handling
- Section 3.3.17 Integrated Voltage Regulators
- Section 4. Electrical Characteristics. Table column ordering.
- Section 4.10 RFSENSE. Correct unit.

7.2 Revision 0.7

2015-08-31

Outcome of comprehensive review cycle of EFR32BG Datasheets. Major changes span the following sections

- Section 2: Ordering Information
- Section 3.3.4: Receiver Architecture
- Section 3.3.5: Transmitter Architecture
- Section 4: Electrical Characteristics
- Section 4.3.1: General Operating Conditions
- Section 4.4: DC-DC Converter
- Section 4.5: Current Consumption
- Section 4.9.1: RF Transmitter Characteristics for 2.4 GHz Band
- Section 4.9.2: RF Receiver General Characteristics for 2.4 GHz Band
- Section 4.9.3: RF Transmitter Characteristics for Bluetooth Smart in 2.4 GHz Band
- Section 4.9.4: RF Receiver Characteristics for Bluetooth Smart in 2.4 GHz Band
- Section 4.11.1: LFXO
- Section 4.11.2: HFXO
- Section 4.12: GPIO
- Section 4.13: VMON
- Section 4.14: ADC
- Section 4.15: IDAC
- Section 4.16: Analog Comparator
- Section 5: Application Circuits
- Section 6.5: QFNxx Package
- Section 6.7: QFNxx Package Marking

7.3 Revision 0.63

2015-07-07

Section 1. Features. correct Ultra Low Energy Timer/Counter bit width.

Section 2. Ordering information : revisions of Max TX power according to part number.

Section 3. System Summary: clarify Crypto options. Revise text desribing Transmitter Architecture and Flexible Frame Handling.

Section 4. Electrical Characteristics: revise RF performance specification tables.

7.4 Revision 0.62

2015-06-18

Revise current consumption table format.

8. Abbreviations

Table 8.1 Abbreviations on page 74 lists abbreviations used in this document.

Table 8.1. Abbreviations

Abbreviation	Description
ACP	Adjacent Channel Power
ACS	Adjacent Channel Selectivity
ADC	Analog to Digital Converter
AGC	Automatic Gain Control
ASK	Amplitude-Shift Keying
BALUN	BALanced UNbalanced (differential to single ended conversion)
BPSK	Binary Phase-Shift Keying
BT	Bandwidth Time
CMU	Clock Management Unit
CRC	Cyclic Redundancy Check
CSP	Channel Separation
CSMA-CA	Carrier Sense Multiple Access - Collision Avoidance
DAC	Digital to Analog Converter
DMA	Direct Memory Access
DSSS	Direct Sequence Spread Spectrum
ECC	Elliptic Curve Cryptography
EFR	Energy Friendly Radio
EMU	Energy Management Unit
EM	Energy Mode
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
FEC	Forward Error Correction
FPU	Floating Point Unit
FRC	Frame Controller
FSK	Frequency-Shift Keying
GCM	Galois Counter Mode
GFSK	Gaussian Frequency-Shift Keying
IF	Intermediate Frequency
LBT	Listen Before Talk
LNA	Low Noise Amplifier
LO	Local Oscillator
MSC	Memory System Controller
MSK	Minimum-Shift Keying

Abbreviation	Description
OOK	On-Off Keying
O-QPSK	Offset Quadrature Phase-Shift Keying
PA	Power Amplifier
PRS	Peripheral Reflex System
PSK	Phase-Shift Keying
PWM	Pulse-Width Modulation
RF	Radio Frequency
RMU	Reset Management Unit
RSSI	Received Signal Strength Indicator
RTCC	Real Time Counter and Calendar
SPI	Serial Peripheral Interface
SRI	Simplified Radio Interface
TCXO	Temperature Compensated Crystal Oscillator

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