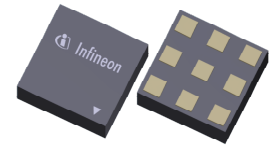


# BGSA200ML9

## Two throws low resistance antenna tuning switch

### Features

- Low  $R_{ON}$  resistance of  $1.40\ \Omega$  at each port in ON state
- Low  $C_{OFF}$  capacitance of 157 fF at each port in OFF state
- High RF operating peak voltage handling of 50 V in OFF state
- Low harmonic generation
- MIPI RFFE 2.1 control interface
- Support of MIPI and GPIO control modes
- 1.8 V and 1.2 V  $V_{IO}$  operation
- Extremely low current consumption of 22  $\mu$ A
- Switching time  $<5\ \mu$ s
- Self-resonant frequency  $>8250\ \text{MHz}$
- Small form factor 1.1 mm x 1.1 mm (MSL1, 260 °C per JEDEC J-STD-020)



- ✓ RoHS
- Ⓜ Halogen-Free
- Ⓟ Lead-Free
- 🌿 Green

### Potential applications

- Impedance, antenna and inductance tuning
- Tunable filters

### Product validation

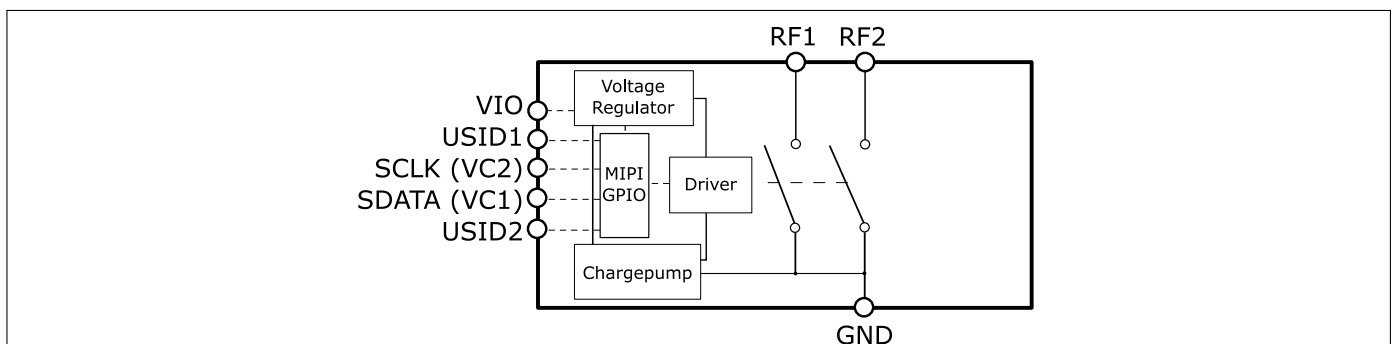
Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

### Description

The BGSA200ML9 is a versatile shunt to ground 2 x Single-Pole Single-Throw (2xSPST) RF antenna tuning switch. It is optimized for low  $C_{OFF}$  as well as low  $R_{ON}$  enabling applications up to 8.25GHz; ideally fitting for antenna tuning purpose.

The BGSA200ML9 integrates on-chip CMOS logic and power supply regulation. Thanks to its 4 states USID1 and USID2 feature, it can be controlled either with GPIO lines or MIPI RFFE bus. Each switch throw can be programmed individually or altogether. Up to 3 instantiations of the same device can be controlled using the same RFFE bus when in MIPI RFFE mode.

### Block diagram



Type	Marking	Package	Ordering Information
BGSA200ML9	A2	TSLP-9-8	BGSA 200ML9 E6327

# BGSA200ML9

## Two throws low resistance antenna tuning switch

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# BGSA200ML9

## Two throws low resistance antenna tuning switch

### Maximum ratings

## 1 Maximum ratings

**Table 1: Maximum ratings table** at  $T_A = 25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency range	$f$	0.4	–	8.25	GHz	<sup>1)</sup>
RFFE supply voltage <sup>2)</sup>	$V_{IO}$	-0.3	–	2.2	V	Only for infrequent and short duration time periods
Storage temperature range	$T_{STG}$	-55	–	150	°C	–
RF peak voltage	$V_{RF\_max}$	–	–	55	V	Short term peaks (1 $\mu$ s in 0.1% duty cycle), exceeding typical linearity, $R_{ON}$ and $C_{OFF}$ parameters, in Isolation mode, test condition schematic in Fig. 1
ESD robustness, CDM <sup>3)</sup>	$V_{ESDCDM}$	-1	–	+1	kV	
ESD robustness, HBM <sup>4)</sup>	$V_{ESDHBM}$	-2	–	+2	kV	
Junction temperature	$T_j$	–	–	125	°C	–
Thermal resistance junction - soldering point	$R_{thJS}$	–	–	50	K/W	–
Maximum DC-voltage on RF-Ports and RF-Ground	$V_{RFDC}$	0	–	0	V	No DC voltages allowed on RF-Ports
RFFE control voltage levels	$V_{SCLK}$ , $V_{SDATA}$	-0.7	–	$V_{IO}+0.7$ (max. 2.2)	V	–

<sup>1)</sup> Switch has a low-pass response. For higher frequencies, losses have to be considered for their impact on thermal heating. The DC voltage at RF ports  $V_{RFDC}$  has to be 0V.

<sup>2)</sup> Note: Consider any ripple voltages on top of  $V_{IO}$ . A high RF ripple at the  $V_{IO}$  can exceed the maximum ratings by  $V_{IO} = V_{DC} + V_{Ripple}$ .

<sup>3)</sup> Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.

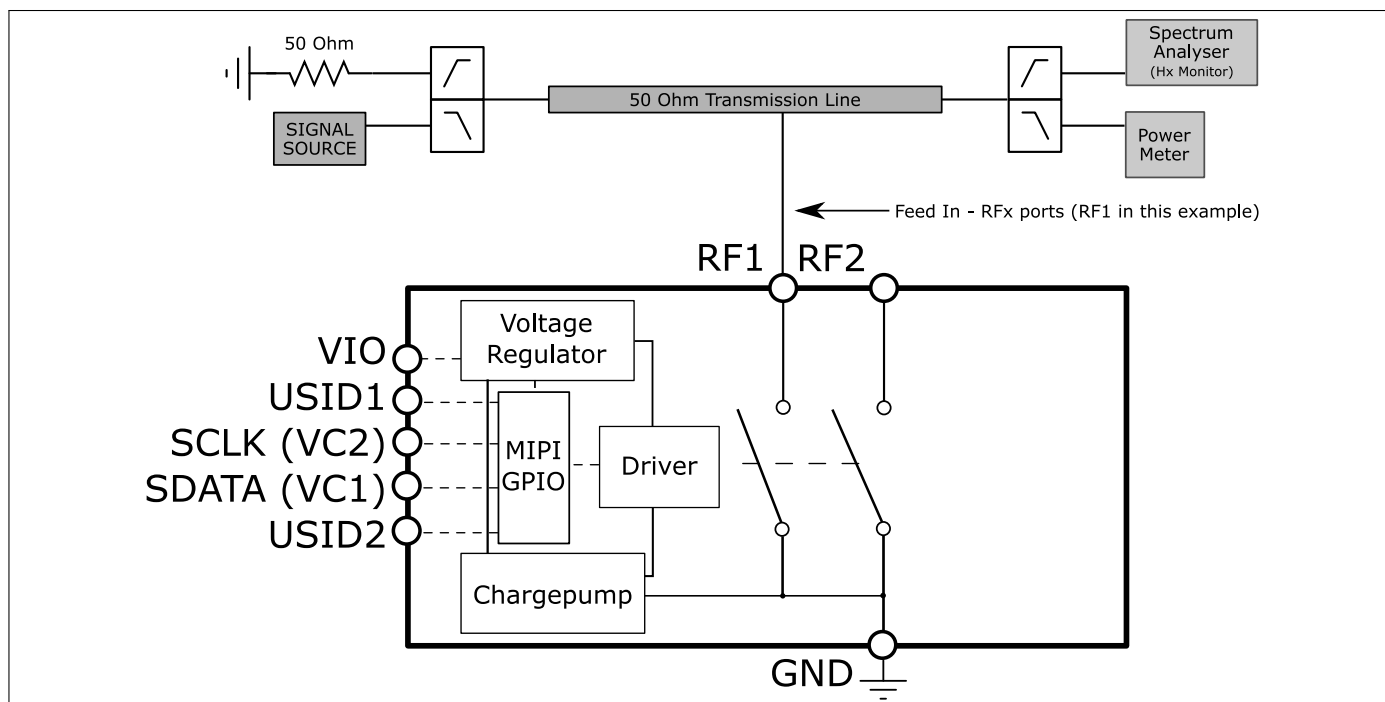
<sup>4)</sup> Human Body Model ANSI/ESDA/JEDEC JS-001 (R=1.5 k $\Omega$ , C=100 pF).

**Warning: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.**

# BGSA200ML9

## Two throws low resistance antenna tuning switch

### Maximum ratings



**Figure 1:** RF operating voltage and harmonic distortion measurement configuration

# BGSA200ML9

## Two throws low resistance antenna tuning switch

### DC characteristics

## 2 DC characteristics

**Table 2: DC characteristics** at  $T_A = -40\text{ °C}$  to  $85\text{ °C}$

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	$V_{IO}$	1.1		1.3	V	–
Supply voltage	$V_{IO}$	1.65		1.95	V	–
Input high voltage <sup>1)</sup>	$V_{IH}$	$0.7 \cdot V_{IO}$	–	$V_{IO}$	V	–
Input low voltage <sup>1)</sup>	$V_{IL}$	0	–	$0.3 \cdot V_{IO}$	V	–
Output high voltage <sup>1)</sup>	$V_{OH}$	$0.8 \cdot V_{IO}$	–	$V_{IO}$	V	–
Output low voltage <sup>1)</sup>	$V_{OL}$	0	–	$0.2 \cdot V_{IO}$	V	–
Control input capacitance	$C_{Ctrl}$	–	–	2	pF	–
Supply current	$I_{VIO}$	–	22	40	$\mu\text{A}$	Normal operating conditions after power ON in either MIPI RFFE <sup>2)</sup> or GPIO control mode, $\leq 35\text{ dBm}$ RF power
		–	1.1	1.7	$\mu\text{A}$	SECONDARY_ACTIVE mode (LOW POWER) in MIPI RFFE mode <sup>2)</sup> with analog circuitry powered OFF

<sup>1)</sup>SCLK (VC2) and SDATA (VC1)

<sup>2)</sup>No traffic on MIPI bus

# BGSA200ML9

## Two throws low resistance antenna tuning switch

### RF small signal characteristics

### 3 RF small signal characteristics

**Table 3: Parametric specifications for each SPST** at  $T_A = 25\text{ °C}$ ,  $Z_0 = 50\ \Omega$ ,  $V_{IO} = 1.1\text{ V} \dots 1.3\text{ V} / 1.65\text{ V} \dots 1.95\text{ V}$

Parameter	Symbol	Values			Unit	STATE / Notes
		Min.	Typ.	Max.		
RF1 or RF2 to GND DC ON resistance	$R_{ON_{SPST}}$	–	1.40	1.55	$\Omega$	
RF1 or RF2 to GND OFF capacitance, 1 GHz <sup>1)</sup>	$C_{OFF_{SPST}}$	–	157	165	fF	

<sup>1)</sup> OFF capacitance calculated from Y11 parameters

**Table 4: RF electrical parameters** at  $T_A = -40\text{ °C}$  to  $85\text{ °C}$ ,  $Z_0 = 50\ \Omega$ ,  $V_{IO} = 1.1\text{ V} \dots 1.3\text{ V} / 1.65\text{ V} \dots 1.95\text{ V}$

**Isolation RF to RF (All OFF / Isolation Mode)** <sup>1)</sup>

380 - 600 MHz	<i>ISO</i>	47	50	–	dB	<i>State 0</i>
600 - 960 MHz		43	45	–	dB	
1160 - 1300 MHz		41	42	–	dB	
1400 - 1700 MHz		38	40	–	dB	
1700 - 2200 MHz		37	38	–	dB	
2200 - 2700 MHz		35	37	–	dB	
3300 - 4200 MHz		32	34	–	dB	
4400 - 5000 MHz		31	32	–	dB	
5150 - 5925 MHz		31	32	–	dB	
5950 - 7125 MHz		31	32	–	dB	

**Isolation RF to RF (RFx ON Mode)** <sup>1)</sup>

380 - 600 MHz	<i>ISO</i>	67	72	–	dB	<i>State 1, 2</i>
600 - 960 MHz		59	64	–	dB	
1160 - 1300 MHz		55	56	–	dB	
1400 - 1700 MHz		50	52	–	dB	
1700 - 2200 MHz		45	49	–	dB	
2200 - 2700 MHz		42	45	–	dB	
3300 - 4200 MHz		35	38	–	dB	
4400 - 5000 MHz		32	34	–	dB	
5150 - 5925 MHz		29	31	–	dB	
5950 - 7125 MHz		27	29	–	dB	

<sup>1)</sup> On application board without any matching components

**RF large signal parameter**
**4 RF large signal parameter**
**Table 5: RF large signal specifications** at  $T_A = -40\text{ °C}$  to  $85\text{ °C}$ ,  $Z_0 = 50\ \Omega$ ,  $V_{IO} = 1.1\text{ V} \dots 1.3\text{ V} / 1.65\text{ V} \dots 1.95\text{ V}$ , unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RF operating voltage	$V_{RF\_opr}$	-	-	50	V	In Isolation mode, 900MHz test condition schematic in Fig. 1. For $H2/H3 \leq -40\text{ dBm}$ , $T_A = 25\text{ °C}$
<b>Harmonic Generation up to 15 GHz, OFF mode</b>						
All RF ports 2nd order harmonics	$P_{H2}$	-	-88	-78	dBm	26 dBm, $50\ \Omega$ , $f_0 = 663\text{ MHz}$
All RF ports 3rd order harmonics	$P_{H3}$	-	-99	-86	dBm	26 dBm, $50\ \Omega$ , $f_0 = 663\text{ MHz}$
All RF ports 2nd order harmonics	$P_{H2}$	-	-72	-66	dBm	35 dBm, $50\ \Omega$ , $f_0 = 915\text{ MHz}$
All RF ports 3rd order harmonics	$P_{H3}$	-	-75	-70	dBm	35 dBm, $50\ \Omega$ , $f_0 = 915\text{ MHz}$
All RF ports 2nd order harmonics	$P_{H2}$	-	-71	-67	dBm	33 dBm, $50\ \Omega$ , $f_0 = 1910\text{ MHz}$
All RF ports 3rd order harmonics	$P_{H3}$	-	-75	-73	dBm	33 dBm, $50\ \Omega$ , $f_0 = 1910\text{ MHz}$
All RF ports 2nd order harmonics	$P_{H2}$	-	-72	-68	dBm	29 dBm, $50\ \Omega$ , $f_0 = 2690\text{ MHz}$
All RF ports 3rd order harmonics	$P_{H3}$	-	-84	-81	dBm	29 dBm, $50\ \Omega$ , $f_0 = 2690\text{ MHz}$
All RF ports 2nd order harmonics	$P_{H2}$	-	-67	-65	dBm	29 dBm, $50\ \Omega$ , $f_0 = 3600\text{ MHz}$
All RF ports 3rd order harmonics	$P_{H3}$	-	-80	-77	dBm	29 dBm, $50\ \Omega$ , $f_0 = 3600\text{ MHz}$
All RF ports 2nd order harmonics	$P_{H2}$	-	-67	-64	dBm	29 dBm, $50\ \Omega$ , $f_0 = 4400\text{ MHz}$
All RF ports 3rd order harmonics	$P_{H3}$	-	-77	-74	dBm	29 dBm, $50\ \Omega$ , $f_0 = 4400\text{ MHz}$
All RF ports 2nd order harmonics	$P_{H2}$	-	-61	-58	dBm	29 dBm, $50\ \Omega$ , $f_0 = 5000\text{ MHz}$
All RF ports 3rd order harmonics	$P_{H3}$	-	-77	-74	dBm	29 dBm, $50\ \Omega$ , $f_0 = 5000\text{ MHz}$
All RF ports 2nd order harmonics	$P_{H2}$	-	-64	-61	dBm	26 dBm, $50\ \Omega$ , $f_0 = 6000\text{ MHz}$
All RF ports 3rd order harmonics	$P_{H3}$	-	-86	-83	dBm	26 dBm, $50\ \Omega$ , $f_0 = 6000\text{ MHz}$
All RF ports > 3rd order harmonics	$P_{Hx}$	-	-	-80	dBm	29 dBm, $50\ \Omega$

# BGSA200ML9

## Two throws low resistance antenna tuning switch

### RF large signal parameter

**Table 6: RF large signal specifications** at  $T_A = -40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$ ,  $Z_0 = 50\ \Omega$ ,  $V_{IO} = 1.1\text{ V} \dots 1.3\text{ V} / 1.65\text{ V} \dots 1.95\text{ V}$

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
<b>Intermodulation distortion IIP2</b>						
IIP2, low	IIP2,l	117	139	–	dBm	IIP2 conditions Tab. 7
IIP2, high	IIP2,h	120	144	–	dBm	
<b>Intermodulation distortion IIP3</b>						
IIP3	IIP3	76	86	–	dBm	IIP3 conditions Tab. 8

**Table 7: IIP2 conditions table**

Band	In-Band frequency [MHz]	Blocker frequency 1 [MHz]	Blocker power 1 [dBm]	Blocker frequency 2 [MHz]	Blocker power 2 [dBm]
Band 1 Low	2140	1950	20	190	0
Band 1 High	2140	1950	20	4090	0
Band 5 Low	881.5	836.5	20	45	0
Band 5 High	881.5	836.5	20	1718	0
Band 7 Low	2655	2535	20	120	0
Band 7 High	2655	2535	20	5190	0

**Table 8: IIP3 conditions table**

Band	In-Band frequency [MHz]	Blocker frequency 1 [MHz]	Blocker power 1 [dBm]	Blocker frequency 2 [MHz]	Blocker power 2 [dBm]
Band 1	2140	1950	20	1760	0
Band 5	881.5	836.5	20	791.5	0
Band 7	2655	2535	20	2415	0

# BGSA200ML9

## Two throws low resistance antenna tuning switch

### MIPI RFFE specification

## 5 MIPI RFFE specification

The MIPI RFFE interface is implemented according to the following specifications and documents:

- MIPI Alliance Specification for RF Front-End Control Interface version 2.1 - 18 December 2017
- MIPI Alliance Errata 01 for MIPI RFFE Specification Version v2.1 - 24 February 2019
- Qualcomm RFFE Vendor specification 80-N7876-1 Rev. Y (December 3, 2018)

**Table 9: MIPI features**

Feature	Supported	Comment
MIPI RFFE 2.1 standard	Yes	Backward compatible to MIPI 2.0 standard
Register 0 write command sequence	No	
Register read and write command sequence	Yes	
Extended register read and write command sequence	Yes	
Support for standard frequency range operations for SCLK	Yes	Up to 26 MHz
Support for extended frequency range operations for SCLK	Yes	Up to 52 MHz
Longer Reach RFFE Bus Length Feature	Yes	
Programmable driver strength	Yes	Up to 80 pF
Programmable Group SID	Yes	
Programmable USID	Yes	
Trigger functionality	Yes	
Extended Triggers and Trigger Masks	Yes	
Broadcast / GSID write to PM TRIG register	Yes	
Reset	Yes	Via VIO, PM TRIG or software register
Status / error sum register	Yes	
Extended product ID register	Yes	
Revision ID register	Yes	
Group SID register	Yes	
USID select pin	Yes	See Tab. 16

**Table 10: Startup Behavior**

Feature	State	Comment
Power status	Low power	Device in SECONDARY_ACTIVE mode (LOW POWER) after start-up
Trigger function	Enabled	Enabled after start-up. Programmable via behavior control register

# BGSA200ML9

## Two throws low resistance antenna tuning switch

### MIPI RFFE specification

**Table 11: Switching time behavior** at  $T_A = 25\text{ °C}$ ,  $Z_0 = 50\ \Omega$ ,  $V_{IO} = 1.1\text{ V} \dots 1.3\text{ V} / 1.65\text{ V} \dots 1.95\text{ V}$

Parameter	Symbol	Values			Unit	STATE / Notes <sup>1), 2)</sup>
		Min.	Typ.	Max.		
ON switching time in MIPI control mode	$t_{ON\ MIPI}$	–	4.0	5.0	$\mu\text{s}$	Time from 50% last SCLK rising edge of the register write command to $V_{stop} + 0.1 \cdot (V_{start} - V_{stop})$ , see Fig. 2
ON switching time in GPIO control mode	$t_{ON\ GPIO}$	–	4.0	5.0	$\mu\text{s}$	Time from VC1 / VC2 low to high transition to $V_{stop} + 0.1 \cdot (V_{start} - V_{stop})$ , see Fig. 3
OFF switching time in MIPI control mode	$t_{OFF\ MIPI}$	–	1.0	2.0	$\mu\text{s}$	Time from 50% last SCLK rising edge of the register write command to $V_{start} + 0.9 \cdot (V_{stop} - V_{start})$ , see Fig. 2
OFF switching time in GPIO control mode	$t_{OFF\ GPIO}$	–	1.0	2.0	$\mu\text{s}$	Time from VC1 / VC2 high to low transition to $V_{start} + 0.9 \cdot (V_{stop} - V_{start})$ , see Fig. 3

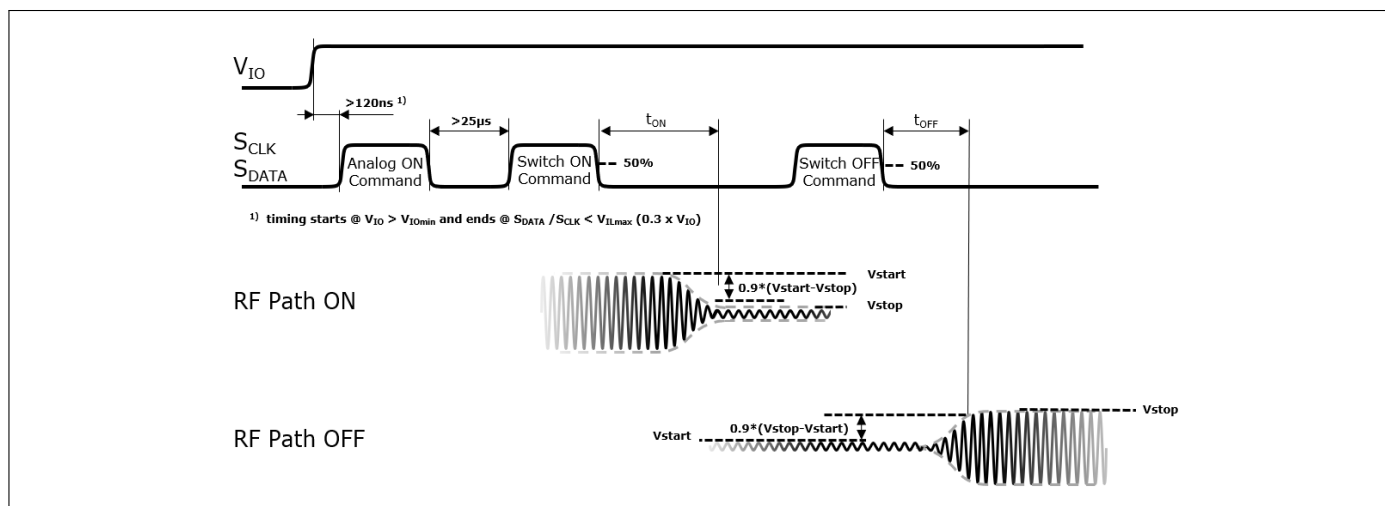
<sup>1)</sup>  $V_{start}$  is the starting RF voltage amplitude of the signal;  $V_{stop}$  is the ending RF voltage amplitude of the signal.

<sup>2)</sup> RF power can be applied only 25  $\mu\text{s}$  after analog ON command when in MIPI RFFE control mode and 25  $\mu\text{s}$  after VIO powered up in GPIO control mode, see Fig. 2 and Fig. 3.

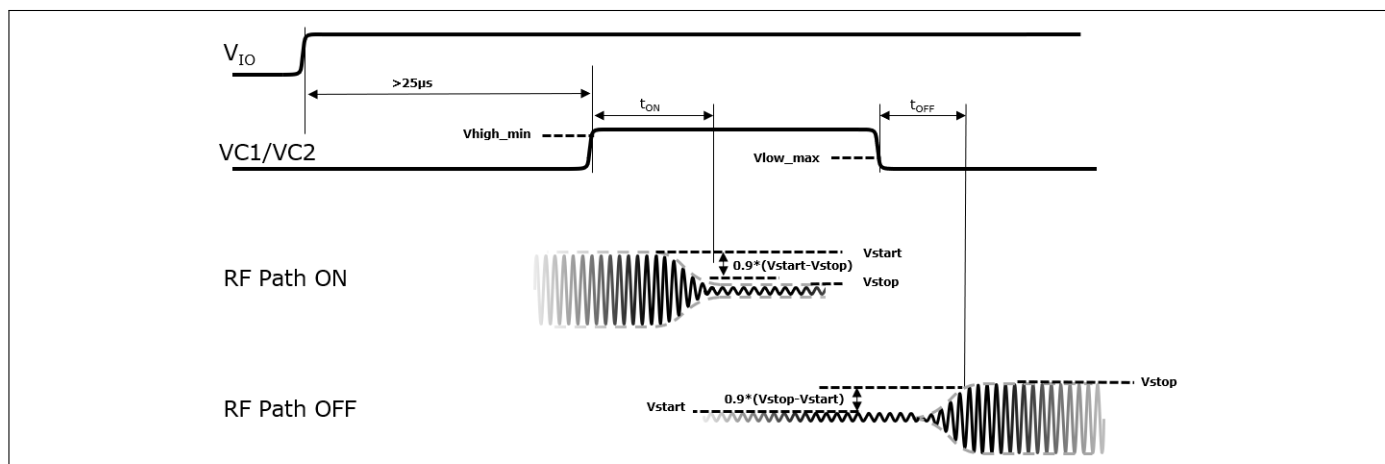
# BGSA200ML9

## Two throws low resistance antenna tuning switch

### MIPI RFFE specification



**Figure 2:** BGSA200ML9 MIPI switching time behavior



**Figure 3:** BGSA200ML9 GPIO switching time behavior

### MIPI RFFE specification

**Table 12: Register mapping, Table I**

Register address	Register name	Data bits	Function	Description	Default	Broadcast_ID support	Trigger support	R/W MW	
0x01	REGISTER_1	7:0	MODE_CTRL	RF Switch Control	00000000	No	Yes Trigger 0-10	R/W MW	
0x1C	PM_TRIG	7	PWR_MODE(1) Operation Mode	0: Normal operation (ACTIVE)	1	Yes	No	R/W MW	
				1: Low Power Mode (SECONDARY_ACTIVE)					
		6	PWR_MODE(0) State Bit Vector	0: No action (ACTIVE)	0				
				1: Powered Reset (ACTIVE to STARTUP)					
		5	TRIGGER_MASK_2	0: Data masked (held in shadow REG)	0				No
				1: Data not masked (ready for transfer to active REG)					
		4	TRIGGER_MASK_1	0: Data masked (held in shadow REG)	0				
				1: Data not masked (ready for transfer to active REG)					
		3	TRIGGER_MASK_0	0: Data masked (held in shadow REG)	0				
1: Data not masked (ready for transfer to active REG)									
2	TRIGGER_2	0: No action (data held in shadow REG)	0	Yes					
		1: Data transferred to active REG							
1	TRIGGER_1	0: No action (data held in shadow REG)	0						
		1: Data transferred to active REG							
0	TRIGGER_0	0: No action (data held in shadow REG)	0						
		1: Data transferred to active REG							
0x1D	PRODUCT_ID	7:0	PRODUCT_ID		This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	10111101	No	No	R
0x1E	MAN_ID	7:0	MANUFACTURER_ID [7:0]		This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value.	00011010	No	No	R
0x1F	MAN_USID	7:4	MANUFACTURER_ID [11:8]		These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value.	0001			
		3:0	USID[3:0]	USID_Sel pin	See Tab. 16	No	No	R/W	

### MIPI RFFE specification

**Table 13: Register mapping, Table II**

Register address	Register name	Data bits	Function	Description	Default	Broadcast_ID support	Trigger support	R/W MW
0x20	EXT_PRODUCT_ID	7:0	EXT_PRODUCT_ID	Extension to PRODUCT_ID in register 0x1D. This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	00000000	No	No	R
0x21	REV_ID	7:4	MAIN_REVISION	Chip main revision	0000	No	No	R
		3:0	SUB_REVISION	Chip sub revision	0000			
0x22	GSID	7:4	GSID0[3:0]	Primary Group Slave ID.	0000	No	No	R/W
		3:0	GSID1[3:0]	Secondary Group Slave ID.	0000			
0x23	UDR_RST	7	UDR_RST	Reset all configurable non-RFFE Reserved registers to default values. 0: Normal operation 1: Software reset	0	Yes	No	R/W
		6:0	RESERVED	Reserved for future use	00000000			
0x24	ERR_SUM	7	RESERVED	Reserved for future use	0	No	No	R
		6	COMMAND_FRAME_PARITY_ERR	Command Sequence received with parity error – discard command.	0			
		5	COMMAND_LENGTH_ERR	Command length error.	0			
		4	ADDRESS_FRAME_PARITY_ERR	Address frame with parity error.	0			
		3	DATA_FRAME_PARITY_ERR	Data frame with parity error.	0			
		2	READ_UNUSED_REG	Read command to an invalid address.	0			
		1	WRITE_UNUSED_REG	Write command to an invalid address.	0			
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_ID.	0			
0x2B	BUS_LD	7:3	RESERVED	Reserved for future use	0x0	No	No	R/W
		2:0	BUS_LD[2:0]	Program the drive strength of the SDATA driver in readback modes.  0x0: 10 pF 0x1: 20 pF 0x2: 30 pF 0x3: 40 pF 0x4: 50 pF 0x5: 60 pF 0x6: 80 pF 0x7: 80 pF 0x8-0xF: reserved	0x4			

**Table 14: Register mapping, Table III**

Register address	Register name	Data bits	Function	Description	Default	Broadcast_ID support	Trigger support	R/W MW
0x2D	EXT_TRIG_MASK	7	TRIGGER_MASK_10	0: Data writes to registers tied to EXT_TRIGGER_10 are masked. Data is held in shadow registers until the EXT_TRIGGER_10 bit is set to 1.	1	No	No	R/W  MW
				1: Data writes to registers tied to EXT_TRIGGER_10 are not masked. Data writes go directly to the active registers.				
		6	TRIGGER_MASK_9	0: Data writes to registers tied to EXT_TRIGGER_9 are masked. Data is held in shadow registers until the EXT_TRIGGER_9 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_9 are not masked. Data writes go directly to the active registers.				
		5	TRIGGER_MASK_8	0: Data writes to registers tied to EXT_TRIGGER_8 are masked. Data is held in shadow registers until the EXT_TRIGGER_8 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_8 are not masked. Data writes go directly to the active registers.				
		4	TRIGGER_MASK_7	0: Data writes to registers tied to EXT_TRIGGER_7 are masked. Data is held in shadow registers until the EXT_TRIGGER_7 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_7 are not masked. Data writes go directly to the active registers.				
		3	TRIGGER_MASK_6	0: Data writes to registers tied to EXT_TRIGGER_6 are masked. Data is held in shadow registers until the EXT_TRIGGER_6 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_6 are not masked. Data writes go directly to the active registers.				
		2	TRIGGER_MASK_5	0: Data writes to registers tied to EXT_TRIGGER_5 are masked. Data is held in shadow registers until the EXT_TRIGGER_5 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_5 are not masked. Data writes go directly to the active registers.				
		1	TRIGGER_MASK_4	0: Data writes to registers tied to EXT_TRIGGER_4 are masked. Data is held in shadow registers until the EXT_TRIGGER_4 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_4 are not masked. Data writes go directly to the active registers.				
0	TRIGGER_MASK_3	0: Data writes to registers tied to EXT_TRIGGER_3 are masked. Data is held in shadow registers until the EXT_TRIGGER_3 bit is set to 1.	1					
		1: Data writes to registers tied to EXT_TRIGGER_3 are not masked. Data writes go directly to the active registers.						

### MIPI RFFE specification

**Table 15: Register mapping, Table IV**

Register address	Register name	Data bits	Function	Description	Default	Broadcast_ID support	Trigger support	R/W MW
0x2E	EXT_TRIG	7	TRIGGER_10	0: No action. Data is held in shadow registers.	0	Yes	No	R/W MW
				1: Data is transferred from shadow registers to active registers for registers tied to EXT_TRIGGER_10				
		6	TRIGGER_9	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for registers tied to EXT_TRIGGER_9				
		5	TRIGGER_8	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for registers tied to EXT_TRIGGER_8				
		4	TRIGGER_7	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for registers tied to EXT_TRIGGER_7				
		3	TRIGGER_6	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for registers tied to EXT_TRIGGER_6				
		2	TRIGGER_5	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for registers tied to EXT_TRIGGER_5				
		1	TRIGGER_4	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for registers tied to EXT_TRIGGER_4				
		0	TRIGGER_3	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for registers tied to EXT_TRIGGER_3				

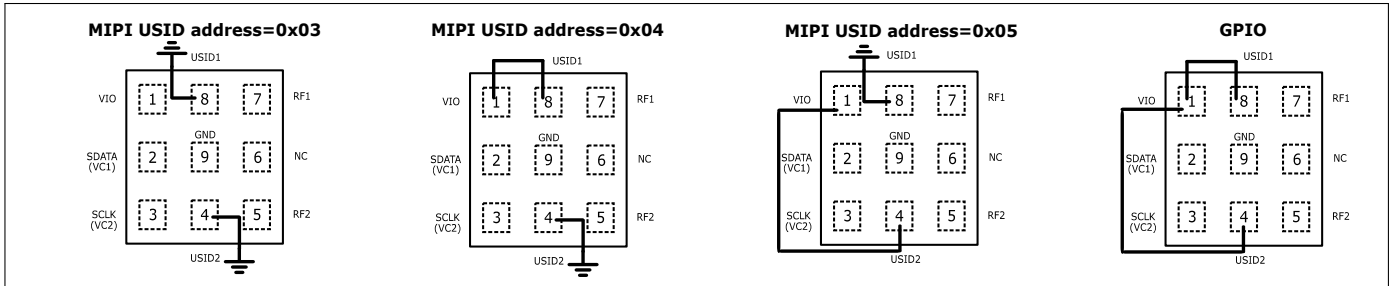
# BGSA200ML9

## Two throws low resistance antenna tuning switch

### MIPI RFFE specification

**Table 16: MIPI RFFE or GPIO mode selection**

-	USID1	USID2
MIPI RFFE mode (USID address=0x03)	GND	GND
MIPI RFFE mode (USID address=0x04)	VIO	GND
MIPI RFFE mode (USID address=0x05)	GND	VIO
GPIO mode	VIO	VIO



**Figure 4:** BGSA200ML9 mode selection and USID configuration

**Table 17: MIPI mode control logic register**

-	D7	D6	D5	D4	D3	D2	D1	D0
RF1+RF2 OFF (state 0)	X	X	X	X	X	X	0	0
RF1 ON (state 1)	X	X	X	X	X	X	0	1
RF2 ON (state 2)	X	X	X	X	X	X	1	0
RF1+RF2 ON (state 3)	X	X	X	X	X	X	1	1

**Table 18: GPIO mode control**

-	VC1	VC2
RF1+RF2 OFF (state 0)	0	0
RF1 ON (state 1)	1	0
RF2 ON (state 2)	0	1
RF1+RF2 ON (state 3)	1	1

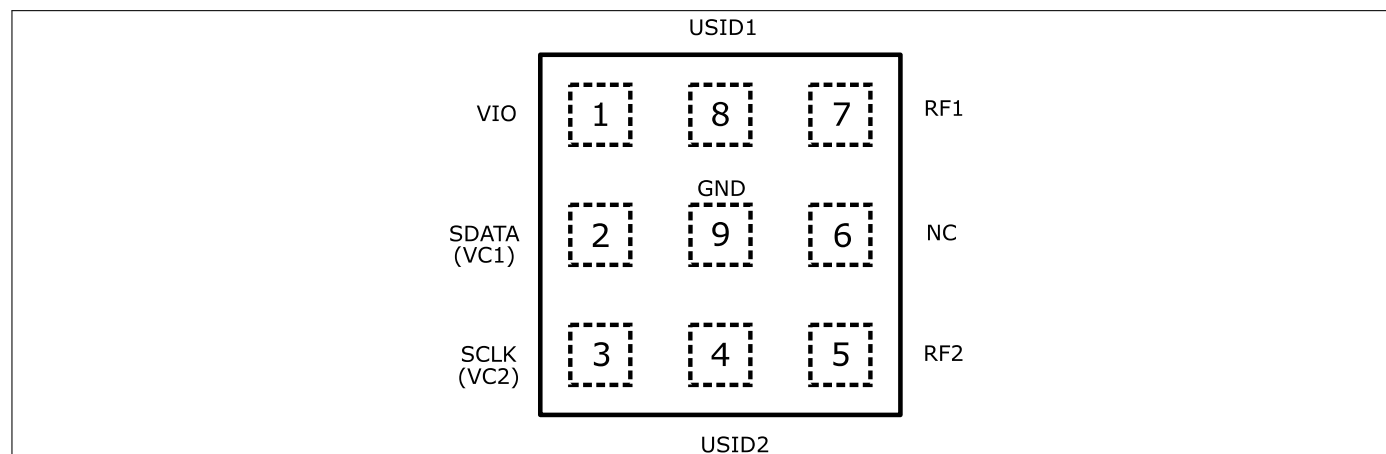
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## Two throws low resistance antenna tuning switch

### Application information

## 6 Application information

### Pin configuration and function



**Figure 5:** BGSA200ML9 pin configuration (top view)

**Table 19: Pin definition and function**

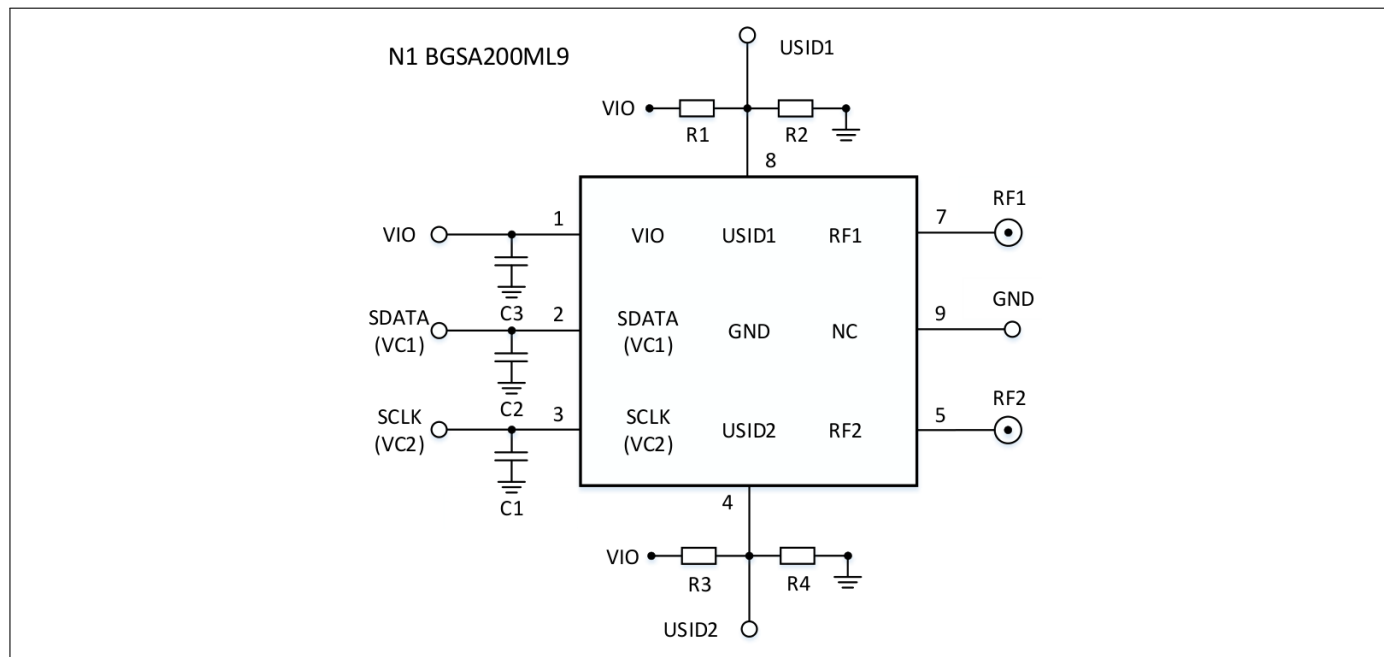
Pin No.	Name	Function
1	VIO	Voltage supply compatible with MIPI RFFE specification
2	SDATA(VC1)	MIPI RFFE data input / output ( digital input when in GPIO mode)
3	SCLK(VC2)	MIPI RFFE clock input ( digital input when in GPIO mode)
4	USID2	GPIO / MIPI mode (and USID default address) selection (see Tab. 16)
5	RF2	RF2 port
6	NC	Not connected
7	RF1	RF1 port
8	USID1	GPIO / MIPI mode (and USID default address) selection (see Tab. 16)
9	GND	Ground

# BGSA200ML9

## Two throws low resistance antenna tuning switch

### Application information

### Evaluation board description



**Figure 6:** BGSA200ML9 application schematic

**Table 20: Bill of Materials Table**

Name	Part Type	Package	Manufacturer	Function
C1 (1nF optional) <sup>1)</sup>	Capacitor	0402	Various	De-coupling capacitor
C2 (1nF optional) <sup>1)</sup>	Capacitor	0402	Various	De-coupling capacitor
C3 (1nF optional) <sup>1)</sup>	Capacitor	0402	Various	De-coupling capacitor
N1	BGSA200ML9	TSLP-9-8	Infineon	Antenna tuner
R1 (do not place), R2 (0 Ω) R3 (do not place), R4 (0 Ω)	Resistor	0402	Various	MIPI RFFE, USID address 0x03 (USID1 to GND and USID2 to GND)
R1 (0 Ω), R2 (do not place) R3 (do not place), R4 (0 Ω)	Resistor	0402	Various	MIPI RFFE, USID address 0x04 (USID1 to VIO and USID2 to GND)
R1 (do not place), R2 (0 Ω) R3 (0 Ω), R4 (do not place)	Resistor	0402	Various	MIPI RFFE, USID address 0x05 (USID1 to GND and USID2 to VIO)
R1 (0 Ω), R2 (do not place) R3 (0 Ω), R4 (do not place)	Resistor	0402	Various	GPIO (USID1 to VIO and USID2 to VIO)

<sup>1)</sup> This capacitor is optional and value is only indicative. Decoupling capacitor value has to be chosen in order VIO ramp-up time is within MIPI RFFE version v2.1 specification



**Table 21: Year date code marking - digit "Y"**

Year	"Y"	Year	"Y"	Year	"Y"
2010	0	2020	0	2030	0
2011	1	2021	1	2031	1
2012	2	2022	2	2032	2
2013	3	2023	3	2033	3
2014	4	2024	4	2034	4
2015	5	2025	5	2035	5
2016	6	2026	6	2036	6
2017	7	2027	7	2037	7
2018	8	2028	8	2038	8
2019	9	2029	9	2039	9

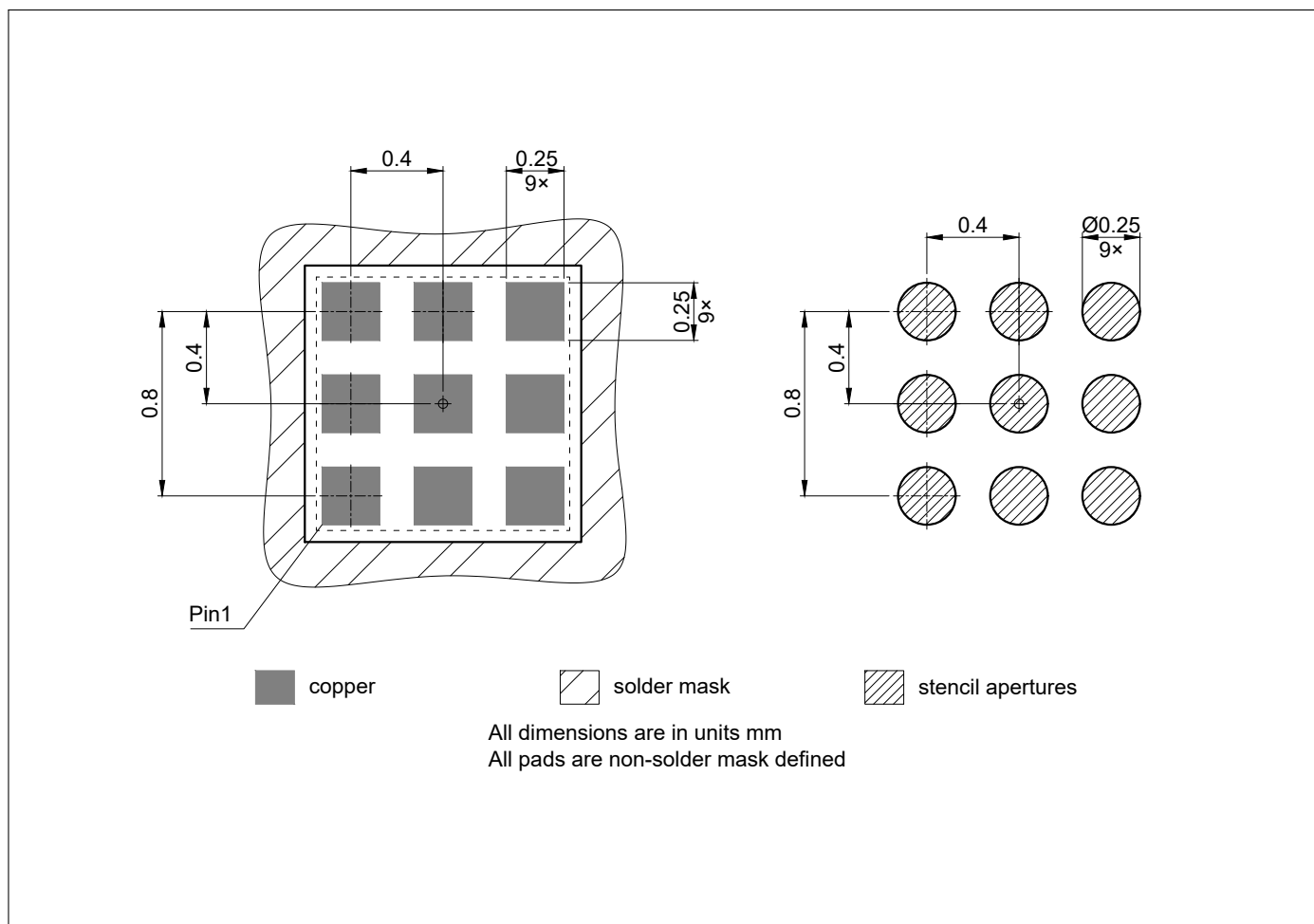
**Table 22: Week date code marking - digit "W"**

Week	"W"	Week	"W"	Week	"W"	Week	"W"	Week	"W"
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s	53	M
10	K	21	Y	32	f	43	t		
11	L	22	Z	33	g	44	u		

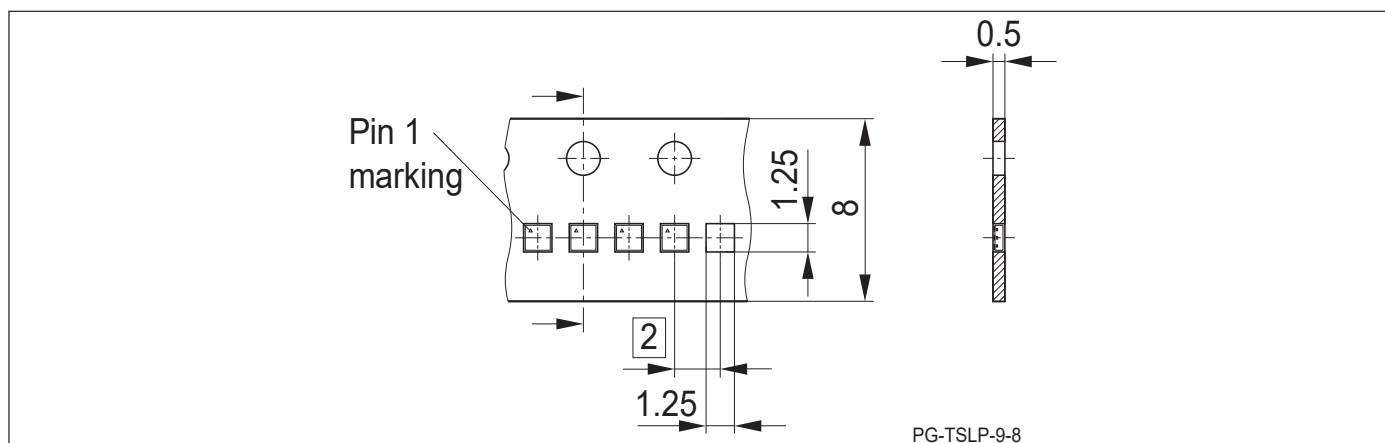
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## Two throws low resistance antenna tuning switch

### Package information



**Figure 9:** Footprint recommendation



**Figure 10:** TSLP-9-8 carrier tape drawing (top and side views)

# BGSA200ML9

## Two throws low resistance antenna tuning switch

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### Revision History

Page or Item	Subjects (major changes since previous revision)
<b>Revision 1.0, 2023-06-13</b>	
All	Creation of datasheet

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