

TS8043N - 100W CW, Broadband SP4T GaN RF Switch

1.0 Features

- Low insertion loss: 0.37dB @ 1GHz
- High isolation: 45dB @ 400MHz, 36dB @ 1GHz
- 100W CW, 200W Peak Power
- No external DC blocking capacitors on RF lines
- Versatile 2.6-5.25V power supply
- Operating frequency: 30MHz to 2.5GHz

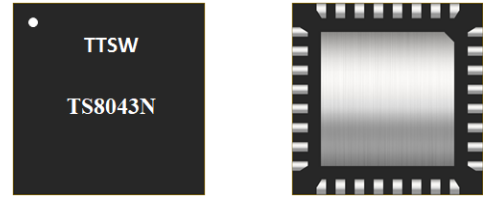


Figure 1 Device Image
(32 Pin 5×5×0.85mm QFN Package)

2.0 Applications

- Private mobile and military radios
- Public safety handsets
- Cellular infrastructure
- Small cells
- LTE relays and microcells
- Satellite terminals



**RoHS/REACH/Halogen Free
Compliance**

3.0 Description

The TS8043N is a 2nd Generation symmetrical reflective Single Pole Four Throw (SP4T) switch designed for broadband, high power switching applications. With a simple broadband match, the TS8043N can cover 30MHz to 2.5GHz bandwidth and provide low insertion loss, high isolation, and high linearity within a small package size. TS8043N is an excellent switch for all applications requiring low insertion loss, high isolation, and high linearity within a small package size.

The TS8043N is packaged into a compact Quad Flat No lead (QFN) 5x5mm 32 leads plastic package.

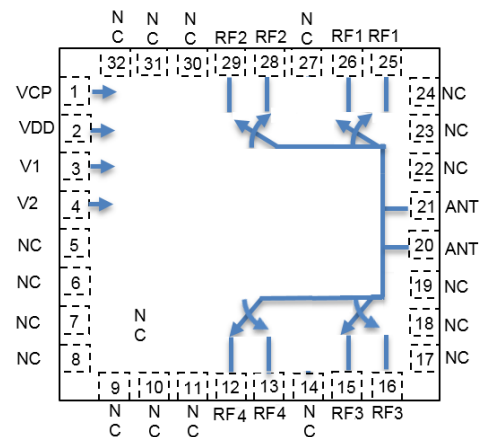


Figure 2 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 1a Ordering Information

Device Part Number	Package Type	Eval Board Part Number
TS8043N	32 Pin 5×5×0.85mm QFN	TS8043N -EVB

Table 1b Tape and Reel Information

Form	Quantity	Reel Diameter	Reel Width
Tape and Reel	3,000	13" (330mm)	18mm

5.0 Pin Description

Table 2 Pin Definition

Pin Number	Pin Name	Description
1	VCP	Internal charge pump voltage output. Connect a 1nF capacitor to GND on this pin to improve switching time.
2	VDD	DC power supply
3	V1	Switch control input 1
4	V2	Switch control input 2
5,6,7,8,9,10,17, 18,23,24,31,32	NC	No internal connection, can be grounded
11,14,19,22,27,30	NC	No internal connection. Do not connect to ground
20,21	ANT	Antenna port
25,26	RF1	RF port 1
28,29	RF2	RF port 2
15,16	RF3	RF port 3
12,13	RF4	RF port 4

Note: The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias, and adequate heat sinking must be used to ensure proper operation and thermal management.

6.0 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Power Supply Voltage	VDD	5.5	V
Storage Temperature Range	T _{st}	-55 to +125	°C
Operating Temperature Range	T _{op}	-40 to +85	°C
Maximum Junction Temperature	T _J	+140	°C
Maximum RF input power(400MHz~1000MHz)	RFx/ANT	51	dBm
Maximum RF input power(30MHz~400MHz)	RFx/ANT	50	dBm
Maximum RF input power (30MHz, VSWR 8:1)	RFx/ANT	47	dBm
Maximum RF input Peak Voltage (30MHz, VSWR 8:1)	RFx/ANT	140	V
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	R _{θJC}	3.5	°C/W
Thermal Resistance (junction-to-top)	R _{θJT}	≤ 26	°C/W
Soldering Temperature	T _{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C3	≥1000	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention:

Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 Electrical Specifications

Table 4 Electrical Specifications @T_A=+25°C Unless Otherwise Specified; VDD=+3.3V; 50Ω Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency		30		2500	MHz
Insertion loss, RFx	100MHz		0.16	0.35	dB
	200MHz		0.17		
	400MHz		0.22		
	1000MHz		0.37		
	2300MHz (matched)		0.43		
Isolation ANT-RFx	100MHz		56		dB
	200MHz		51		
	400MHz		45		
	1000MHz		36		
	2300MHz (matched)		22		
Return loss ANT, RFx	100MHz		35		dB
	200MHz		33		
	400MHz		30		
	1000MHz		20		
	2300MHz (matched)		20		
Harmonic distortion					
H2	800MHz, Pin=47dBm		76		dBc
H3	800MHz, Pin=47dBm		79		dBc
IIP3	800MHz				dBm
P0.1dB ^[1]	800MHz, CW		50		dBm
P0.1dB ^[1]	30MHz, CW		50		dBm
Peak P0.1dB ^[1]	800MHz, 1% duty cycle, 1 mS period.		54		dBm
Switching time	50% ctrl to 10/90% of the RF value is settled. CP=1nF to ground on VCP pin.		12		μs
Control voltage	Power Supply VDD	2.6	3.3	5.25	V
	All control pins high, V _{ih}	1.0	3.3	5.25	V
	All control pins low, V _{il}	-0.3		0.5	V
Control current	All control pins low, I _{il}		0		μA
	All control pins high, I _{ih}			7.5	μA
Current consumption, I _{DD}	Active mode (VDD on)		160	200	μA

Note:

[1] P0.1dB is a figure of merit.

[2] No external DC blocking capacitors required on RF pins unless DC voltage is applied on a RF pin.

8.0 Switch Truth Table

Table 5 Switch Truth Table

V1	V2	Active RF Path
0	0	ANT-RF1 ON
1	0	ANT-RF2 ON
0	1	ANT-RF3 ON
1	1	ANT-RF4 ON

Attention:

- [1] VDD should be applied first before V1 and V2, otherwise may cause damage to the device.
- [2] There are internal pull-downs to ground on both V1 and V2 control pins, the state at start-up without any control voltage applied will be ANT-RF1 ON.

9.0 Evaluation Board

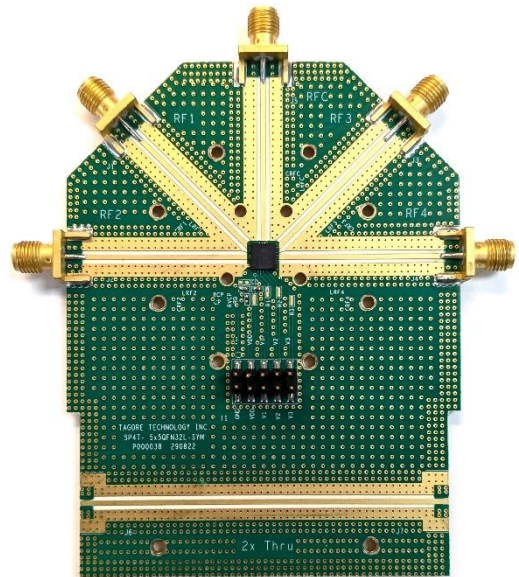
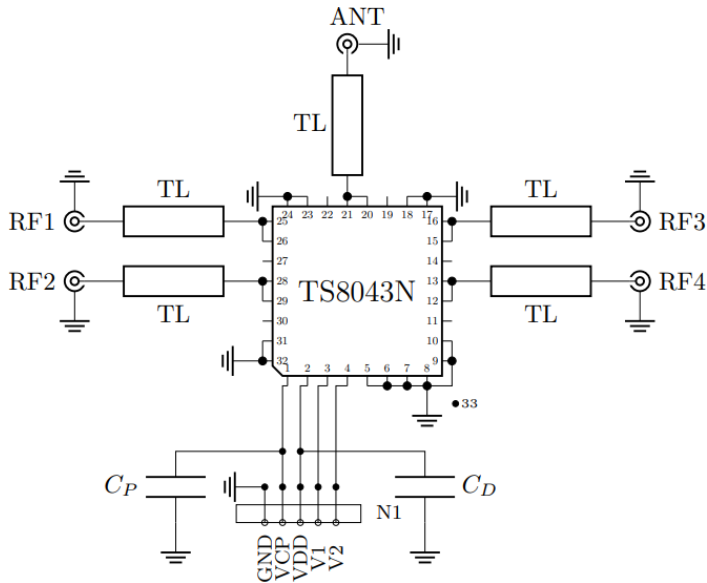


Figure 3 Evaluation Board and Schematic

Attention:

- [1] 33 refers to the center pad of the device. Multiple Plugged through hole vias should be added on this Ground Pad and adequate heat sinking should be used.
- [2] The purpose of connection between VCP and connector N1 is to monitor VCP, do not apply external voltage to VCP.
- [3] Place matching components close to pin of the part.

10.1 Typical Characteristics – Unmatched

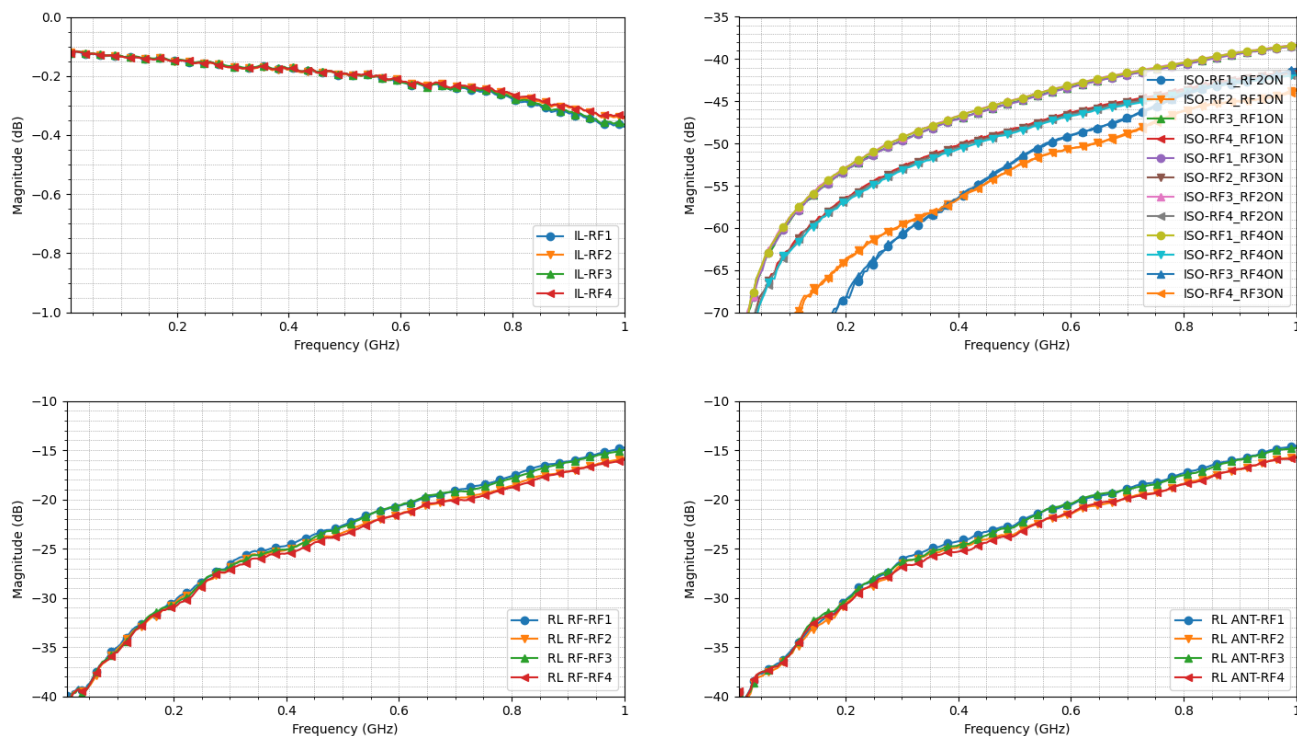


Figure 4.1 Typical characteristics (Unmatched)

10.2 Typical Characteristics – Matched (2200 MHz – 2500 MHz)

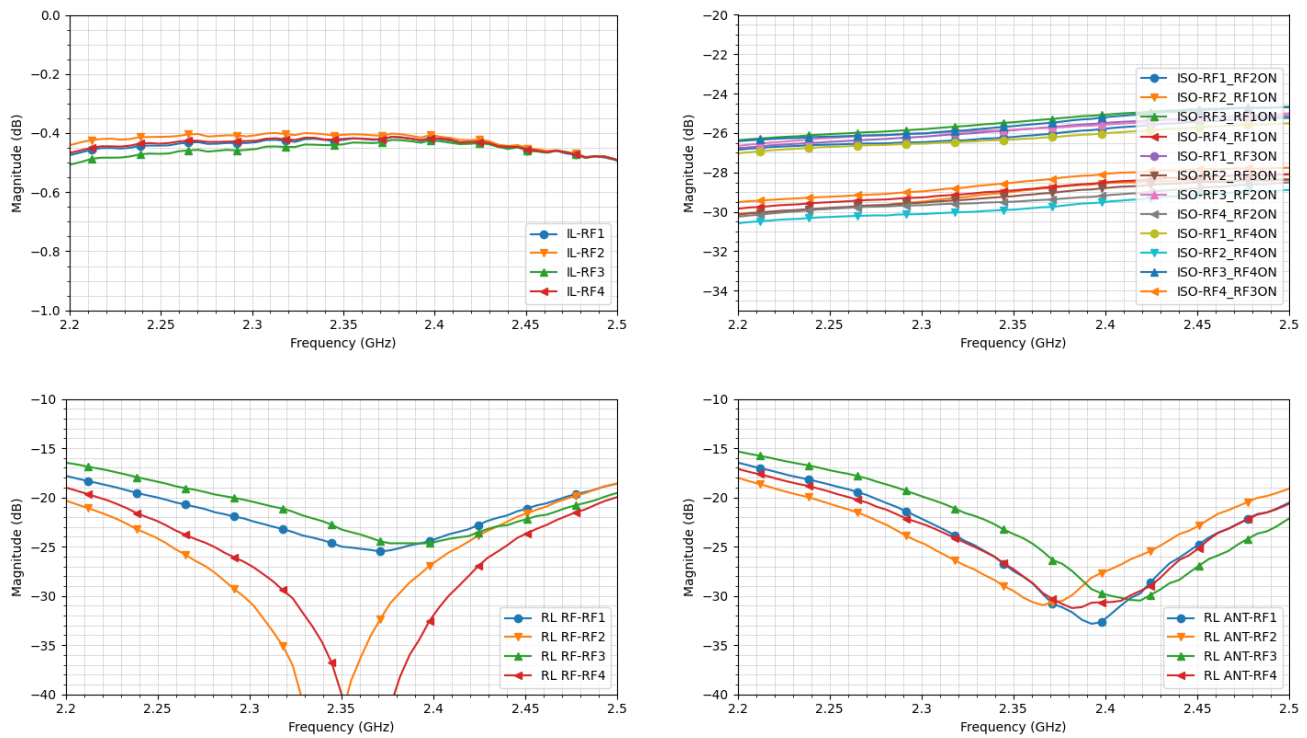


Figure 4.2 Typical characteristics (2200 MHz – 2500 MHz)

Table 6.1 Bill of Materials – Unmatched*

Component	Part Number	Description	Notes
C _P	GRM155R71H102KA01D	Ceramic capacitor, 1 nF, 50 V, ±10%.	
C _D	GRM155R71H103KA88	Ceramic capacitor, 10 nF, 50 V, ±15%.	

* For additional details, please contact the TagoreTech support team.

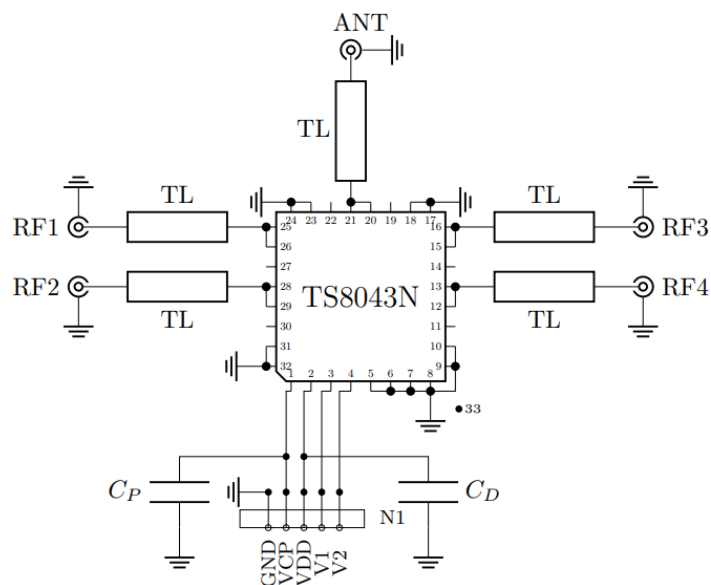


Figure 5.1 Schematic for Unmatched Condition

Table 6.2 Bill of Materials – Matching* (2200 MHz – 2500 MHz)

Component	Part Number	Description	Notes
C_P	GRM155R71H102KA01D	Ceramic capacitor, 1 nF, 50 V, $\pm 10\%$.	
C_D	GRM155R71H103KA88	Ceramic capacitor, 10 nF, 50 V, $\pm 15\%$.	
T_{0a}	1.0 mm	PCB transmission line length.	From the IC-reference plane.
T_{0b}	0.5 mm	PCB transmission line length.	
L_{0a}	1512SP-2N5K1E_	Mini Air Core Inductor, 2.5 nH, $\pm 10\%$.	
C_{0a}	0603N1R2BW251	Ceramic capacitor, 1.2 pF, 250V, $\pm 0.1\text{pF}$.	

* For additional details, please contact the TagoreTech support team.

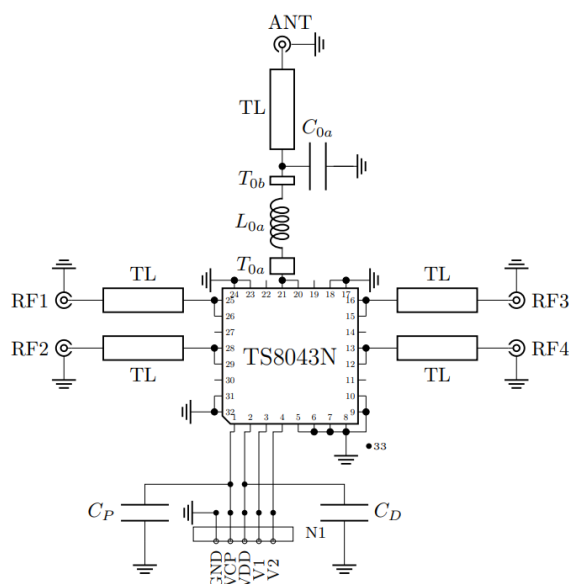


Figure 5.2 Schematic for Matching (2200 MHz – 2500 MHz)

11.0 Device Package Information

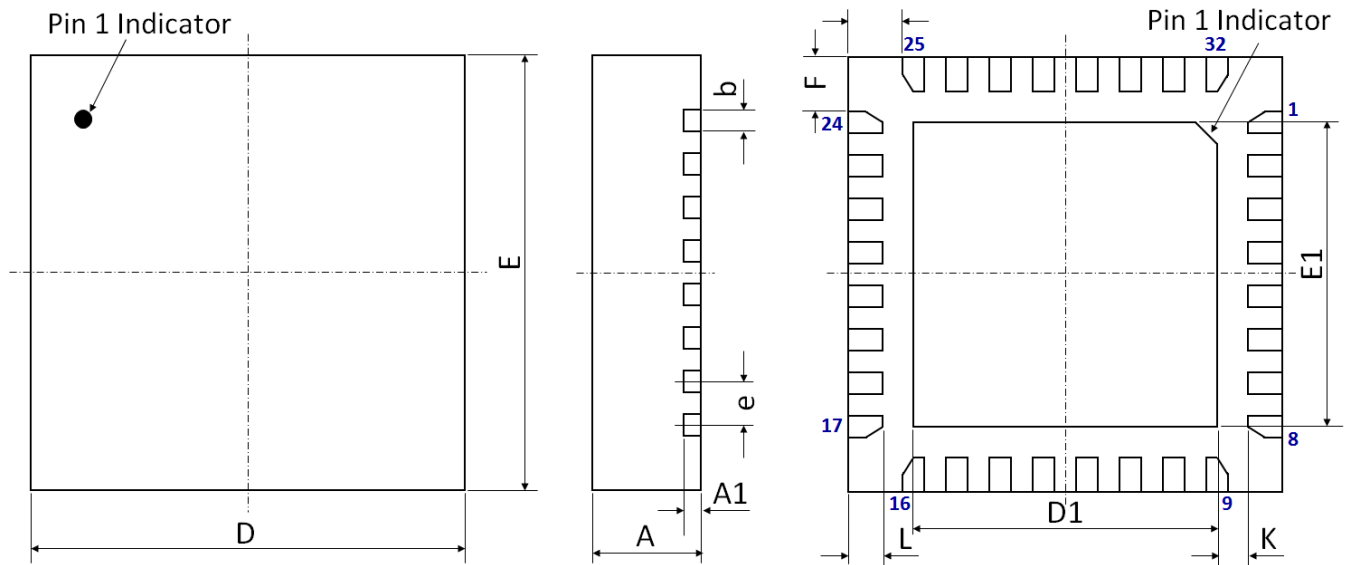


Figure 5 Device Package Drawing
(All dimensions are in mm)

Table 7 Device Package Dimensions

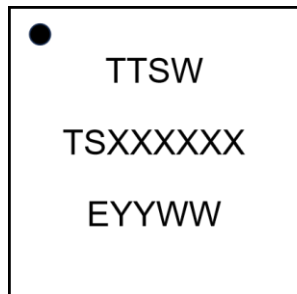
Dimension (mm)	Value (mm)	Tolerance (mm)	Dimension (mm)	Value (mm)	Tolerance (mm)
A	0.85	±0.05	E	5.00 BSC	±0.05
A1	0.203	±0.02	E1	3.20	±0.06
b	0.25	+0.05/-0.07	F	0.625	±0.05
D	5.00 BSC	±0.05	G	0.625	±0.05
D1	3.20	±0.06	L	0.40	±0.05
e	0.50 BSC	±0.05	K	0.50	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5µm ~ 20µm (Typical 10µm ~ 12µm)

Attention:

Please refer to application notes [TN-001](#) and [TN-002](#) at <http://www.tagoretech.com> for PCB and soldering related guidelines.

Top-marking specification:



- = Pin 1 indicator
- TTSW = Tagore Technology SWitch
- TSXXXXXX = Part number (8 digits max)
- E = A fixed letter before the date code
- YY = Last two digits of assembly year
- WW = Assembly work week

12.0 PCB Land Design

Guidelines:

- [1] 4-layer PCB is recommended.
- [2] Via diameter is recommended to be 0.3mm to prevent solder wicking inside the vias.
- [3] Thermal vias shall only be placed on the center pad.
- [4] The maximum via number for the center pad is $5(X) \times 5(Y) = 25$.

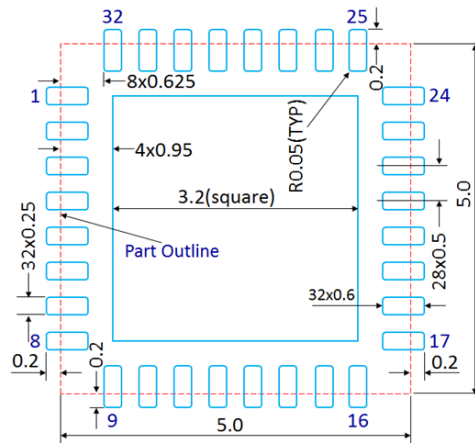


Figure 6 PCB Land Pattern
(Dimensions are in mm)

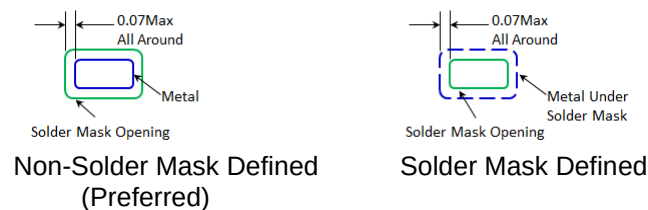


Figure 7 Solder Mask Pattern
(Dimensions are in mm)

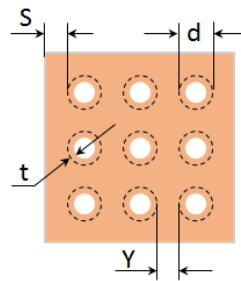


Figure 8 Thermal Via Pattern

(Recommended Values: $S \geq 0.15\text{mm}$; $Y \geq 0.20\text{mm}$; $d = 0.3\text{mm}$; Plating Thickness $t = 25\mu\text{m}$ or $50\mu\text{m}$)

13.0 PCB Stencil Design

Guidelines:

- [1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.
- [2] Stencil thickness is recommended to be 125µm.

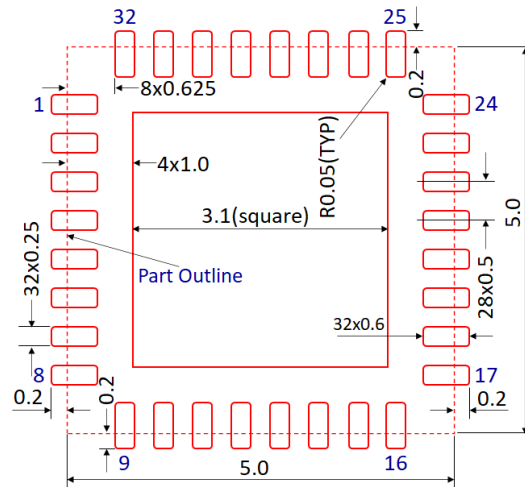


Figure 9 Stencil Openings
(Dimensions are in mm)

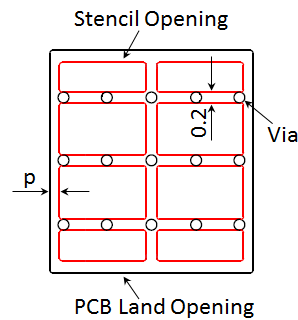


Figure 10 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

14.0 Tape and Reel Information

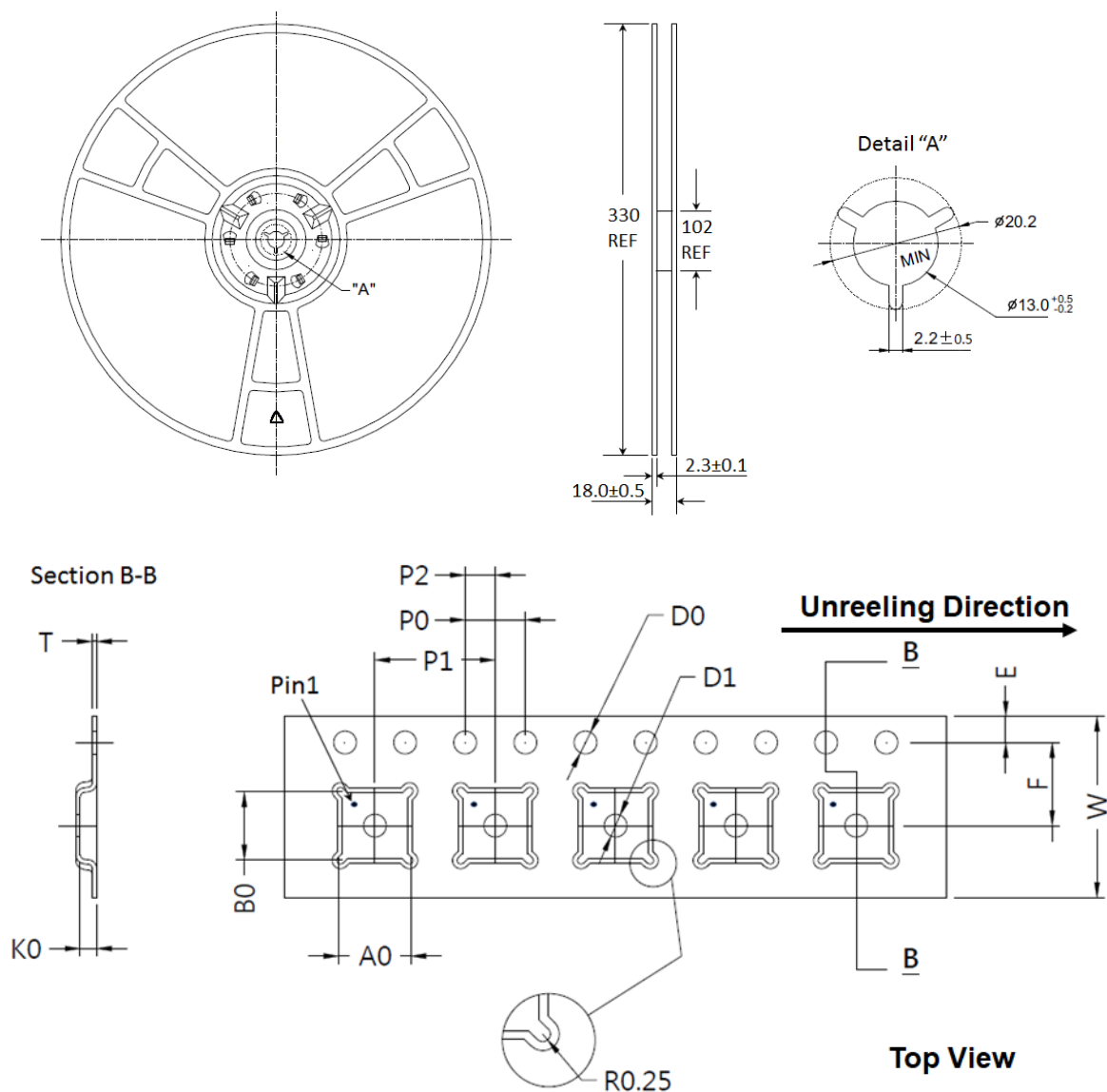


Figure 11 Tape and Reel Drawing

Table 8 Tape and Reel Dimensions

Dimension (mm)	Value (mm)	Tolerance (mm)	Dimension (mm)	Value (mm)	Tolerance (mm)
A0	5.25	±0.10	K0	1.10	±0.10
B0	5.25	±0.10	P0	4.00	±0.10
D0	1.5	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	+0.3/-0.1

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Information

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