# THE DATASHEET OF

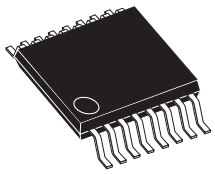
# L6732

# L6732

## Adjustable step-down controller with synchronous rectification

## Features

- Input voltage range from 1.8 V to 14 V
- Supply voltage range from 4.5 V to 14 V
- Adjustable output voltage down to 0.6 V with ± 0.8 % accuracy over line voltage and temperature (0 °C~125 °C)
- Fixed frequency voltage mode control
- $T_{ON}$ lower than 100 ns
- 0 % to 100 % duty cycle
- External input voltage reference
- Soft-start and inhibit
- High current embedded drivers
- Predictive anti-cross conduction control
- Programmable high-side and low-side $R_{DS(on)}$ sense over-current-protection
- Selectable switching frequency 250 kHz / 500 kHz
- Pre-bias start up capability
- Power good output
- Master/slave synchronization with 180° phase shift
- Over voltage protection
- Thermal shutdown
- Package: HTSSOP16



**HTSSOP16 (exposed pad)**

## Applications

- LCD and PDP TV
- High performance / high density DC-DC modules
- Low voltage distributed DC-DC
- niPoL converters
- DDR memory supply
- Graphic cards

**Table 1. Device summary**

| Order codes | Package | Packing |
|---|---|---|
| L6732 | HTSSOP16 | Tube |
| L6732TR | HTSSOP16 | Tape and reel |

# Contents

# 1 Summary description

The controller is an integrated circuit realized in BCD5 (BiCMOS-DMOS, version 5) fabrication that provides complete control logic and protection for high performance step-down DC-DC and niPoL converters.

It is designed to drive N-channel MOSFETs in a synchronous rectified buck topology. The output voltage of the converter can be precisely regulated down to 600 mV with a maximum tolerance of ±0.8 % and it is also possible to use an external reference from 0 V to 2.5 V.

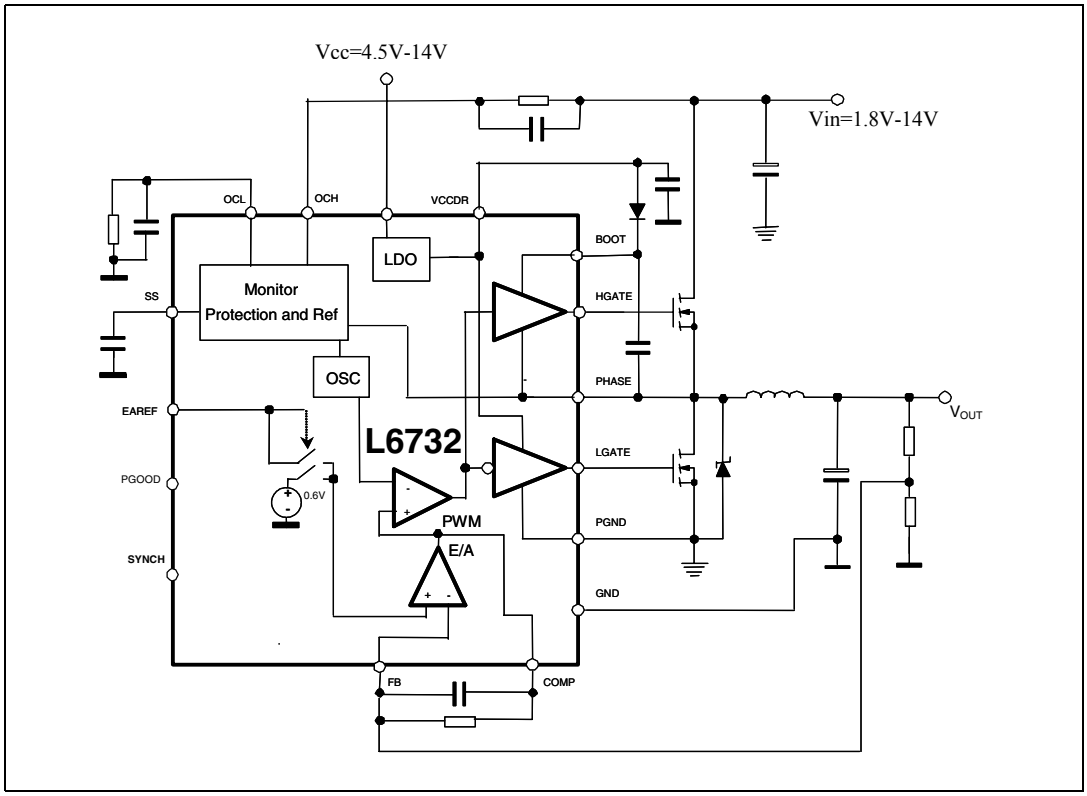
The input voltage can range from 1.8 V to 14 V, while the supply voltage can range from 4.5 V to 14 V. High peak current gate drivers provide for fast switching to the external power section, and the output current can be in excess of 20 A. The PWM duty cycle can range from 0 % to 100 % with a minimum on-time ($T_{ON, MIN}$) lower than 100 ns making possible conversions with very low duty cycle at high switching frequency. The device provides voltage-mode control that includes a selectable frequency oscillator (250 kHz or 500 kHz).

The error amplifier features a 10 MHz gain-bandwidth-product and 5 V/µs slew-rate that permits to realize high converter bandwidth for fast transient response. The device monitors the current by using the $R_{DS(on)}$ of both the high-side and low-side MOSFET(s), eliminating the need for a current sensing resistor and guaranteeing an effective over-current-protection in all the application conditions. When necessary, two different current limit protections can be externally set through two external resistors.

During the soft-start phase a constant current protection is provided while after the soft-start the device enters in hiccup mode in case of over-current. During the soft-start, the sink mode capability is disabled in order to allow a proper start-up also in pre-biased output voltage conditions. After the soft-start the device can sink current. Other features are power good, master/slave synchronization (with 180° phase shift), over-voltage-protection, feed-back disconnection and thermal shutdown. The HTSSOP16 package allows the realization of really compact DC/DC converters.

## 1.1 Functional description

**Figure 1. Block diagram**



# 2 Electrical data

## 2.1 Maximum rating

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | $V_{CC}$ to GND and PGND, OCH, PGOOD | -0.3 to 18 | V |
| $V_{BOOT}$ - $V_{PHASE}$ | Boot voltage | 0 to 6 | V |
| $V_{HGATE}$ - $V_{PHASE}$ | | 0 to $V_{BOOT}$ - $V_{PHASE}$ | V |
| $V_{BOOT}$ | BOOT | -0.3 to 24 | V |
| $V_{PHASE}$ | PHASE | -1 to 18 | V |
| | PHASE spike, transient < 50 ns ($F_{SW}$ = 500 kHz) | -3 | |
| | | +24 | |
| | SS, FB, EAREF, SYNC, OCL, LGATE, COMP, $V_{CCDR}$ | -0.3 to 6 | V |
| OCH pin | Maximum withstanding voltage range test condition: CDF-AEC-Q100-002 “human body model” acceptance criteria: “normal performance” | ±1500 | V |
| PGOOD pin | | ±1000 | |
| Other pins | | ±2000 | |

## 2.2 Thermal data

**Table 3. Thermal data**

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $R_{thJA}$ | Thermal resistance junction to ambient | 50 | °C/W |
| $T_{STG}$ | Storage temperature range | -40 to +150 | °C |
| $T_J$ | Junction operating temperature range | -40 to +125 | °C |
| $T_A$ | Ambient operating temperature range | -40 to +85 | °C |

# 3 Pin connection and function

**Figure 2. Pin connection (top view)**

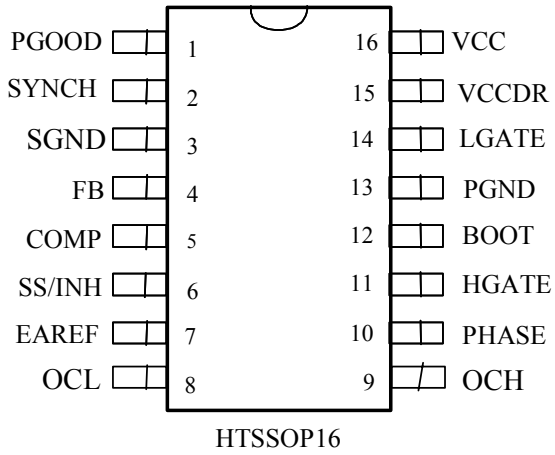



**Table 4. Pin functions**

| Pin n. | Name | Function |
|---|---|---|
| 1 | PGOOD | This pin is an open collector output and it is pulled low if the output voltage is not within the specified thresholds (90 %-110 %). If not used it may be left floating. Pull-up this pin to $V_{CCDR}$ with a 10 k resistor to obtain a logical signal. |
| 2 | SYNCH | It is a Master-Slave pin. Two or more devices can be synchronized by simply connecting the SYNCH pins together. The device operating with the highest FSW will be the Master. The Slave devices will operate with 180° phase shift from the Master. The best way to synchronize devices together is to set their FSW at the same value. If it is not used the SYNCH pin can be left floating. |
| 3 | SGND | All the internal references are referred to this pin. |
| 4 | FB | This pin is connected to the error amplifier inverting input. Connect it to $V_{OUT}$ through the compensation network. This pin is also used to sense the output voltage in order to manage the over voltage conditions and the PGood signal. |
| 5 | COMP | This pin is connected to the error amplifier output and is used to compensate the voltage control feedback loop. |
| 6 | SS/INH | The soft-start time is programmed connecting an external capacitor from this pin and GND. The internal current generator forces a current of 10 A through the capacitor. When the voltage at this pin is lower than 0.5 V the device is disabled. |

**Table 4. Pin functions (continued)**

| Pin n. | Name | Function |
|---|---|---|
| 7 | EAREF | By setting the voltage at this pin is possible to select the internal/external reference and the switching frequency:<br>$V_{EAREF}$ 0-80 % of $V_{CCDR}$ -> external reference/$F_{SW}$ = 250 kHz<br>$V_{EAREF}$ = 80 %-95 % of $V_{CCDR}$ -> $V_{REF}$ = 0.6 V/$F_{SW}$ = 500 kHz<br>$V_{EAREF}$ = 95 %-100 % of $V_{CCDR}$ -> $V_{REF}$ = 0.6 V/$F_{SW}$ = 250 kHz<br>An internal clamp limits the maximum $V_{EAREF}$ at 2.5 V (typ.). The device captures the analog value present at this pin at the start-up when $V_{CC}$ meets the UVLO threshold. |
| 8 | OCL | A resistor connected from this pin to ground sets the valley- current-limit. The valley current is sensed through the low-side MOSFET(s). The internal current generator sources a current of 100 µA ($I_{OCL}$) from this pin to ground through the external resistor ($R_{OCL}$). The over-current threshold is given by the following equation:<br>$I_{VALLEY} = \frac{I_{OCL} \bullet R_{OCL}}{2 \bullet R_{DSONLS}}$<br>Connecting a capacitor from this pin to GND helps in reducing the noise injected from $V_{CC}$ to the device, but can be a low impedance path for the high-frequency noise related to the GND. Connect a capacitor only to a “clean” GND. |
| 9 | OCH | A resistor connected from this pin and the high-side MOSFET(s) drain sets the peak-current-limit. The peak current is sensed through the high-side MOSFET(s). The internal 100 µA current generator ($I_{OCH}$) sinks a current from the drain through the external resistor ($R_{OCH}$). The over-current threshold is given by the following equation:<br>$I_{PEAK} = \frac{I_{OCH} \bullet R_{OCH}}{R_{DSONHS}}$ |
| 10 | PHASE | This pin is connected to the source of the high-side MOSFET(s) and provides the return path for the high-side driver. This pin monitors the drop across both the upper and lower MOSFET(s) for the current limit together with OCH and OCL. |
| 11 | HGATE | This pin is connected to the high-side MOSFET(s) gate. |
| 12 | BOOT | Through this pin is supplied the high-side driver. Connect a capacitor from this pin to the PHASE pin and a diode from $V_{CCDR}$ to this pin (cathode versus BOOT). |
| 13 | PGND | This pin has to be connected closely to the low-side MOSFET(s) source in order to reduce the noise injection into the device. |
| 14 | LGATE | This pin is connected to the low-side MOSFET(s) gate. |
| 15 | $V_{CCDR}$ | 5 V internally regulated voltage. It is used to supply the internal drivers. Filter it to ground with at least 1 µF ceramic cap. |
| 16 | $V_{CC}$ | Supply voltage pin.<br>The operative supply voltage range is from 4.5 V to 14 V. |

# 4 Electrical characteristics

**Table 5. Electrical characteristics ($V_{CC}$ = 12 V, $T_A$ = 25 °C, unless otherwise specified)**

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **$V_{CC}$ supply current** | | | | | | |
| $I_{CC}$ | $V_{CC}$ stand by current | OSC = open; SS to GND | | 7 | 9 | mA |
| | $V_{CC}$ quiescent current | OSC = open; HG = open, LG = open, PH = open | | 8.5 | 10 | |
| **Power-ON** | | | | | | |
| $V_{CC}$ | Turn-ON $V_{CC}$ threshold | $V_{OCH}$ = 1.7 V | 4.0 | 4.2 | 4.4 | V |
| | Turn-OFF $V_{CC}$ threshold | $V_{OCH}$ = 1.7 V | 3.6 | 3.8 | 4.0 | V |
| $V_{IN\ OK}$ | Turn-ON $V_{OCH}$ threshold | | 1.1 | 1.25 | 1.47 | V |
| $V_{IN\ OK}$ | Turn-OFF $V_{OCH}$ threshold | | 0.9 | 1.05 | 1.27 | V |
| **$V_{CCDR}$ regulation** | | | | | | |
| | $V_{CCDR}$ voltage | $V_{CC}$ = 5.5 V to 14 V<br>$I_{DR}$ = 1 mA to 100 mA | 4.5 | 5 | 5.5 | V |
| **Soft-start and inhibit** | | | | | | |
| $I_{SS}$ | Soft-start current | SS = 2 V | 7 | 10 | 13 | µA |
| | | SS = 0 to 0.5 V | 20 | 30 | 45 | |
| **Oscillator** | | | | | | |
| $f_{OSC}$ | Accuracy | | 237 | 250 | 263 | kHz |
| | | | 450 | 500 | 550 | kHz |
| $\Delta V_{OSC}$ | Ramp amplitude | | | 2.1 | | V |
| **Output voltage** | | | | | | |
| $V_{FB}$ | Output voltage | $V_{DIS}$ = 0 to $V_{th}$ | 0.597 | 0.6 | 0.603 | V |
| **Error amplifier** | | | | | | |
| $R_{EAREF}$ | EAREF input resistance | Vs GND | 70 | 100 | 150 | kΩ |
| $I_{FB}$ | I.I. bias current | $V_{FB}$ = 0 V | | 0.290 | 0.5 | µA |
| Ext ref clamp | | | 2.3 | | | V |
| $V_{OFFSET}$ | Error amplifier offset | Vref = 0.6 V | -5 | | +5 | mV |
| $G_V$ | Open loop voltage gain | Guaranteed by design | | 100 | | dB |
| GBWP | Gain-bandwidth product | Guaranteed by design | | 10 | | MHz |
| SR | Slew-rate | COMP = 10 pF<br>Guaranteed by design | | 5 | | V/µs |

**Table 5. Electrical characteristics ($V_{CC}$ = 12 V, $T_A$ = 25 °C, unless otherwise specified) (continued)**

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Gate drivers** | | | | | | |
| $R_{HGATE\_ON}$ | High side source resistance | $V_{BOOT}$ - $V_{PHASE}$ = 5 V | | 1.7 | | Ω |
| $R_{HGATE\_OFF}$ | High side sink resistance | $V_{BOOT}$ - $V_{PHASE}$ = 5 V | | 1.12 | | Ω |
| $R_{LGATE\_ON}$ | Low side source resistance | $V_{CCDR}$ = 5 V | | 1.15 | | Ω |
| $R_{LGATE\_OFF}$ | Low side sink resistance | $V_{CCDR}$ = 5 V | | 0.6 | | Ω |
| **Protections** | | | | | | |
| $I_{OCH}$ | OCH current source | $V_{OCH}$ = 1.7 V | 90 | 100 | 110 | µA |
| $I_{OCL}$ | OCL current source | | 90 | 100 | 110 | µA |
| OVP | Over voltage trip (VFB / VEAREF) | $V_{FB}$ rising $V_{EAREF}$ = 0.6 V | | 120 | | % |
| | | $V_{FB}$ falling $V_{EAREF}$ = 0.6 V | | 117 | | % |
| | Under voltage threshold ($V_{FB}$ / $V_{EAREF}$) | $V_{FB}$ falling | | 80 | | % |
| **Power good** | | | | | | |
| | Upper threshold ($V_{FB}$ / $V_{EAREF}$) | $V_{FB}$ rising | 108 | 110 | 112 | % |
| | Lower threshold ($V_{FB}$ / $V_{EAREF}$) | $V_{FB}$ falling | 88 | 90 | 92 | % |
| $V_{PGOOD}$ | PGOOD voltage low | $I_{PGOOD}$ = -5 mA | | 0.5 | | V |

**Table 6. Thermal characteristics** ($V_{CC}$ = 12 V)

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Output voltage** | | | | | | |
| $V_{FB}$ | Output voltage | $T_J$ = 0 °C ~ 125 °C | 0.596 | 0.6 | 0.605 | V |
| | | $T_J$ = -40 °C ~ 125 °C | 0.593 | 0.6 | 0.605 | |

# 5 Device description

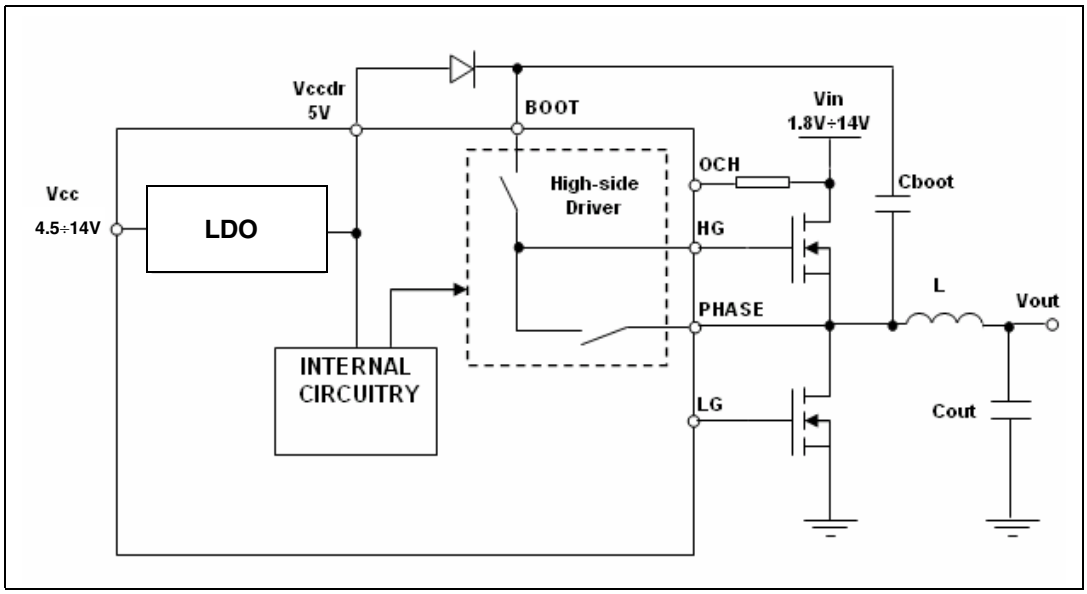
## 5.1 Oscillator

The switching frequency can be fixed to two values: 250 kHz or 500 kHz by setting the proper voltage at the EAREF pin (see *Table 4.* pins function and section 4.3 Internal and external reference).

## 5.2 Internal LDO

An internal LDO supplies the internal circuitry of the device. The input of this stage is the $V_{CC}$ pin and the output (5 V) is the $V_{CCDR}$ pin (*Figure 3.*).

**Figure 3. LDO block diagram**

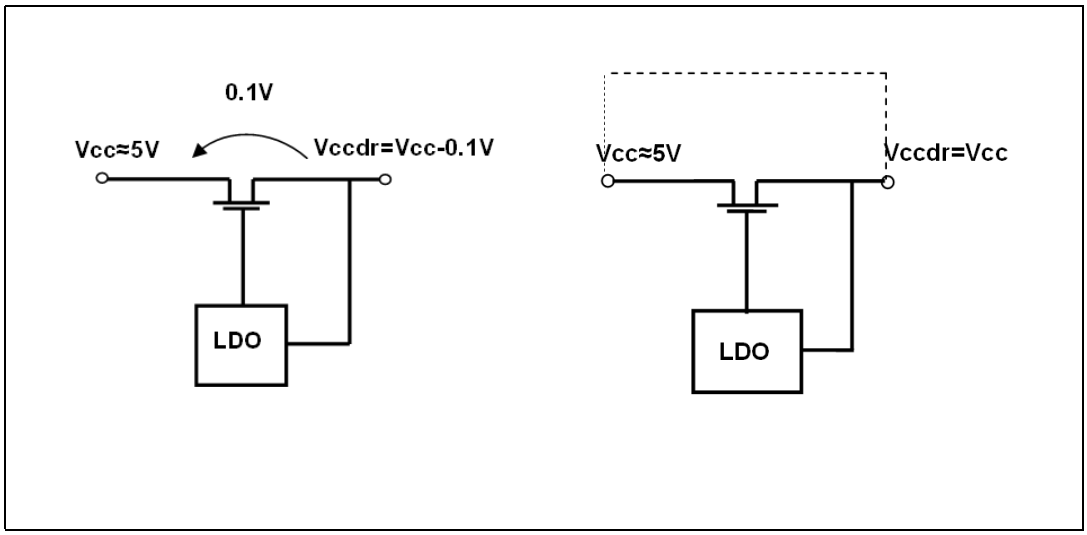



The LDO can be by-passed, providing directly a 5 V voltage to $V_{CCDR}$. In this case $V_{CC}$ and $V_{CCDR}$ pins must be shorted together as shown in *Figure 4.* $V_{CCDR}$ pin must be filtered with at least 1 µF capacitor to sustain the internal LDO during the recharge of the bootstrap capacitor. $V_{CCDR}$ also represents a voltage reference for PGOOD pin (see *Table 4.* pins function).

## 5.3 Bypassing the LDO to avoid the voltage drop with low Vcc

If $V_{CC} \approx 5$ V the internal LDO works in dropout with an output resistance of about 1 Ω. The maximum LDO output current is about 100 mA and so the output voltage drop is 100 mV, to avoid this the LDO can be by passed.

**Figure 4. Bypassing the LDO**




## 5.4 Internal and external references

It is possible to set the internal/external reference and the switching frequency by setting the proper voltage at the EAREF pin. The maximum value of the external reference depends on the $V_{CC}$: with $V_{CC}$ = 4 V the clamp operates at about 2 V (typ.), while with $V_{CC}$ greater than 5V the maximum external reference is 2.5 V (typ.).

- $V_{EAREF}$ from 0 % to 80 % of $V_{CCDR}$ -> External reference/Fsw = 250 kHz
- $V_{EAREF}$ from 80 % to 95 % of $V_{CCDR}$ -> $V_{REF}$ = 0.6V/Fsw = 500 kHz
- $V_{EAREF}$ from 95 % to 100 % of $V_{CCDR}$ -> $V_{REF}$ = 0.6V/Fsw = 250 kHz

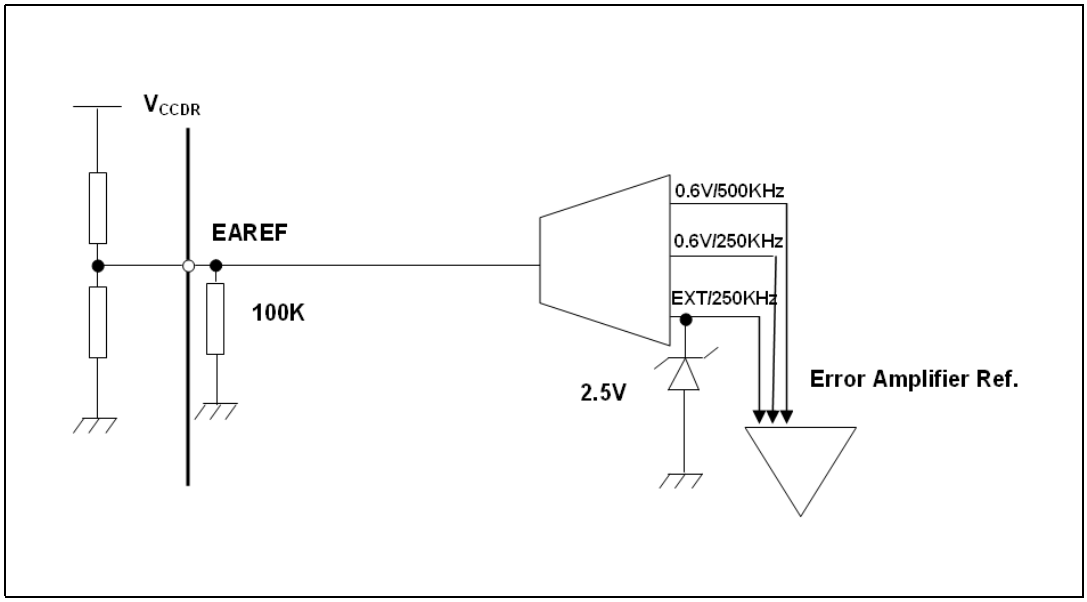
Providing an external reference from 0 V to 450 mV the output voltage will be regulated but some restrictions must be considered:

- OV threshold saturates to a minimum value of 300 mV (OV is tracking the reference; tracking small references will result in a narrow threshold reducing noise immunity)
- The under-voltage-protection doesn't work;
- The PGOOD signal remains low;

To set the resistor divider it must be considered that a 100 k pull-down resistor is integrated into the device (see *Figure 5.*). Finally it must be taken into account that the voltage at the EAREF pin is captured by the device at the start-up when $V_{CC}$ is about 4 V.

## 5.5 Error amplifier

**Figure 5. Error amplifier reference**




## 5.6 Soft-start

When both $V_{CC}$ and $V_{IN}$ are above their turn-ON thresholds ($V_{IN}$ is monitored by the OCH pin) the start-up phase takes place. Otherwise the SS pin is internally shorted to GND. At start-up, a ramp is generated charging the external capacitor $C_{SS}$ with an internal current generator. The initial value for this current is 35 µA and charges the capacitor up to 0.5 V. After that it becomes 10 µA until the final charge value of approximately 4 V (see *Figure 6*). The output of the error amplifier is clamped with this voltage ($V_{SS}$) until it reaches the programmed value. No switching activity is observable if $V_{SS}$ is lower than 0.5 V and both MOSFETs are OFF. When $V_{SS}$ is between 0.5 V and 1.1 V the low-side MOSFET is turned on because the comp signal is lower than the valley of the triangular wave and so the duty-cycle is 0 %. As $V_{SS}$ reaches 1.1 V (i.e. the oscillator triangular wave inferior limit) even the high-side MOSFET begins to switch and the output voltage starts to increase. The L6732 can only source current during the soft-start phase in order to manage the pre-bias start-up applications. This means that when the start-up occurs with output voltage greater than 0V (pre-bias startup), even when Vss is between 0.5 V and 1.1 V the low-side MOSFET is kept OFF (see *Figure 7* and *Figure 8*).

Figure 6. Device start-up: voltage at the SS pin

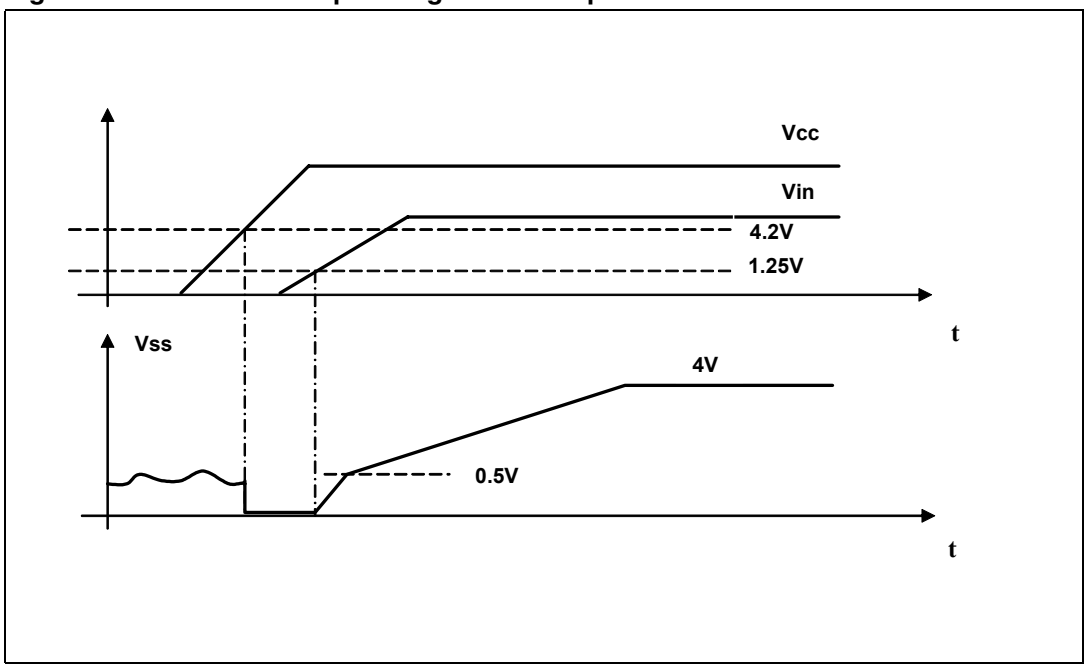



Figure 7. Start-up without pre-bias

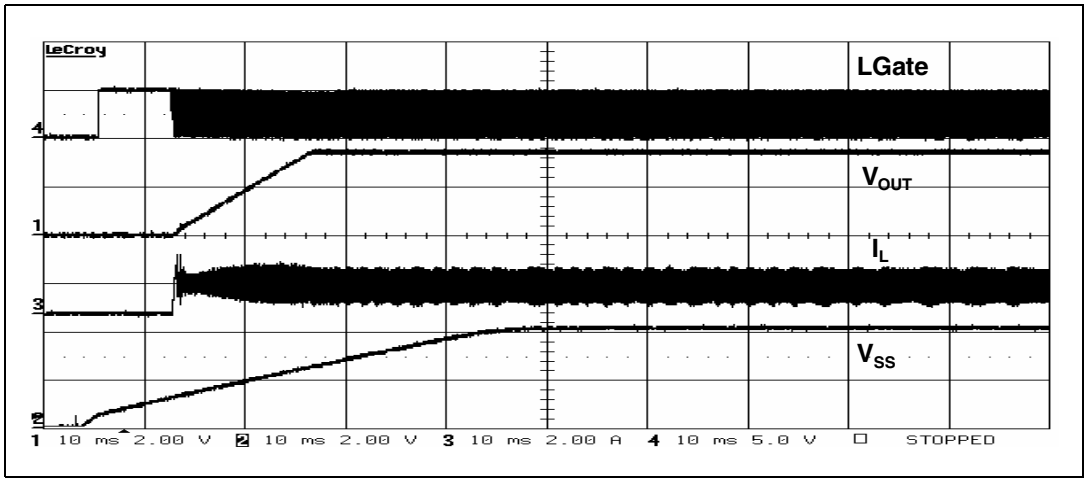
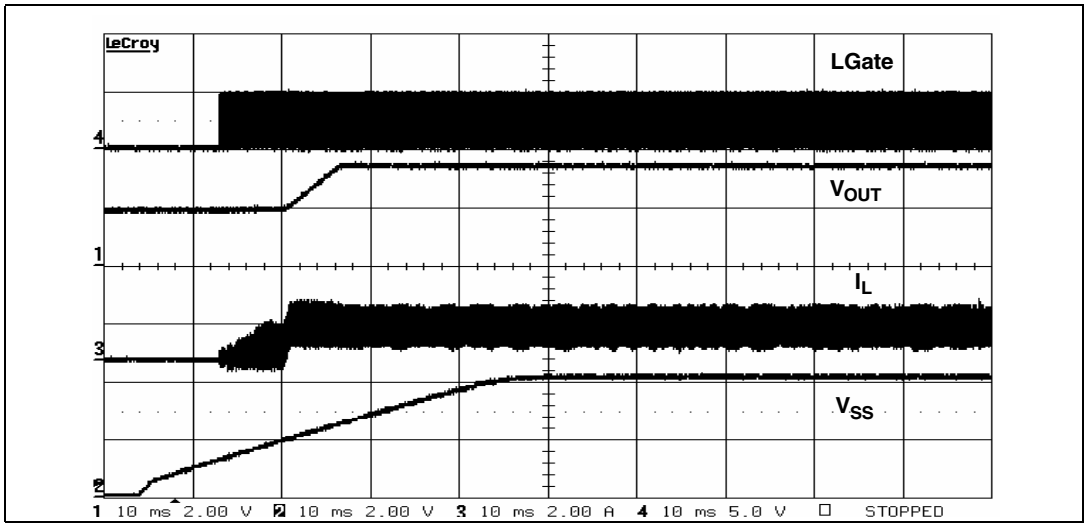
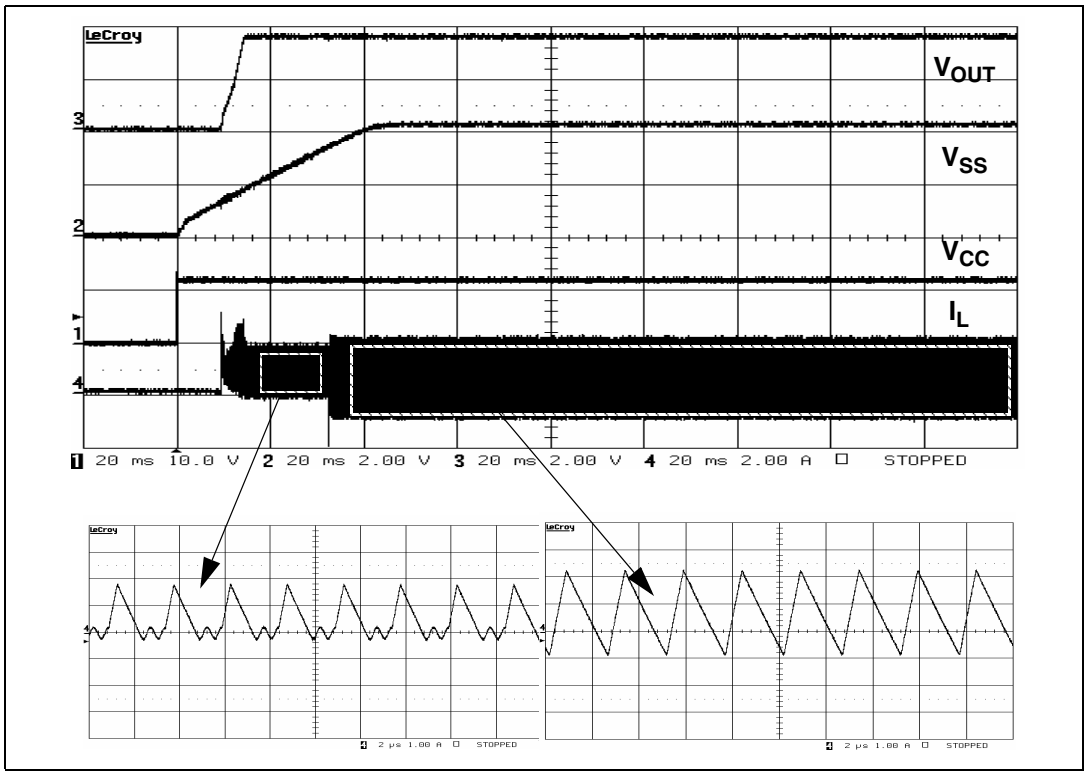


**Figure 8. Start-up with pre-bias**




The L6732 can sink or source current after the soft-start phase (see *Figure 9.*). If an over current is detected during the soft-start phase, the device provides a constant-current-protection. In this way, in case of short soft-start time and/or small inductor value and/or high output capacitors value and so, in case of high ripple current during the soft-start, the converter can start in any case, limiting the current (see section 4.6 monitoring and protections) but not entering in HICCUP mode.

**Figure 9. Inductor current during and after soft-start**




During normal operation, if any under-voltage is detected on one of the two supplies, the SS pin is internally shorted to GND and so the SS capacitor is rapidly discharged.

## 5.7 Driver section

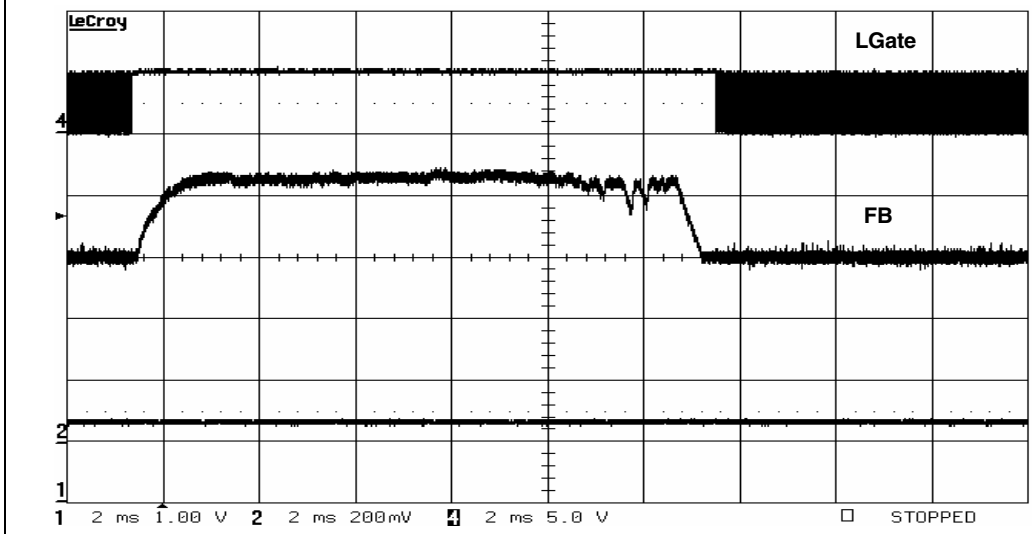
The high-side and low-side drivers allow using different types of power MOSFETs (also multiple MOSFETs to reduce the $R_{DS(on)}$ maintaining fast switching transitions.
The low-side driver is supplied by $V_{CCDR}$ while the high-side driver is supplied by the BOOT pin. A predictive dead time control avoids MOSFETs cross-conduction maintaining very short dead time duration in the range of 20 ns. The control monitors the phase node in order to sense the low-side body diode recirculation. If the phase node voltage is less than a certain threshold (-350 mV typ.) during the dead time, it will be reduced in the next PWM cycle. The predictive dead time control doesn't work when the high-side body diode is conducting because the phase node doesn't go negative. This situation happens when the converter is sinking current for example and, in this case, an adaptive dead time control operates.

## 5.8 Monitoring and protections

The output voltage is monitored by means of pin FB. If it is not within ±10 % (typ.) of the programmed value, the Power good (PGOOD) output is forced low.

The device provides over-voltage-protection: when the voltage sensed on FB pin reaches a value 20% (typ.) greater than the reference, the low-side driver is turned on as long as the over voltage is detected (see *Figure 10.*).

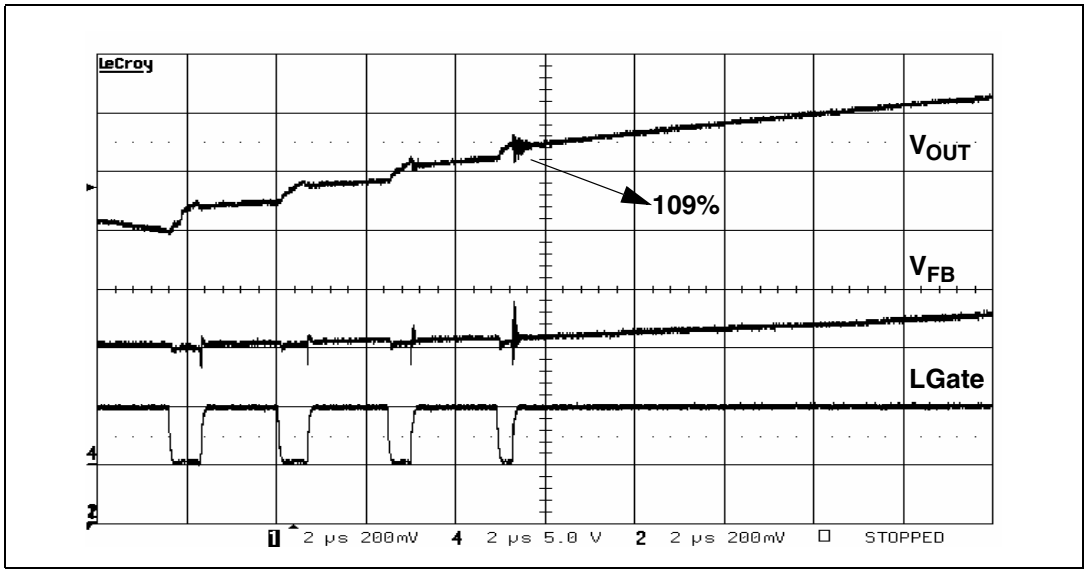
**Figure 10. OVP**




It must be taken into account that there is an electrical network between the output terminal and the FB pin and therefore the voltage at the pin is not a perfect replica of the output voltage. However due to the fact that the converter can sink current, in the most of cases the low-side will turn-on before the output voltage exceeds the over-voltage threshold, because the error amplifier will throw off balance in advance. Even if the device doesn't report an over-voltage, the behavior is the same, because the low-side is turned-on immediately. The following figure shows the device behavior during an over-voltage event. The output voltage

rises with a slope of 100 mV/µs, emulating in this way the breaking of the high-side MOSFET as an over-voltage cause.

**Figure 11. OVP: the low-side MOSFET is turned-on in advance**




The device realizes the over-current-protection (OCP) sensing the current both on the high-side MOSFET(s) and the low-side MOSFET(s) and so 2 current limit thresholds can be set (see OCH pin and OCL pin in *Table 4.* Pins function):

- Peak current limit
- Valley current limit

The peak current protection is active when the high-side MOSFET(s) is turned on, after a masking time of about 100 ns. The valley-current-protection is enabled when the low-side MOSFET(s) is turned on after a masking time of about 400 ns. If, when the soft-start phase is completed, an over current event occurs during the on time (peak-current-protection) or during the off time (valley-current-protection) the device enters in HICCUP mode: the high-side and low-side MOSFET(s) are turned off, the soft-start capacitor is discharged with a constant current of 10 µA and when the voltage at the SS pin reaches 0.5 V the soft-start phase restarts. During the soft-start phase the OCP provides a constant-current-protection. If during the $T_{ON}$ the OCH comparator triggers an over current the high-side MOSFET(s) is immediately turned off (after the masking time and the internal delay) and returned on at the next PWM cycle. The limit of this protection is that the $T_{ON}$ can't be less than masking time plus propagation delay because during the masking time the peak-current-protection is disabled. In case of very hard short circuit, even with this short $T_{ON}$, the current could escalate. The valley-current-protection is very helpful in this case to limit the current. If during the off-time the OCL comparator triggers an over current, the high-side MOSFET(s) is not turned on until the current is over the valley-current-limit. This implies that, if it is necessary, some pulses of the high-side MOSFET(s) will be skipped, guaranteeing a maximum current due to the following formula:

**Equation 4**

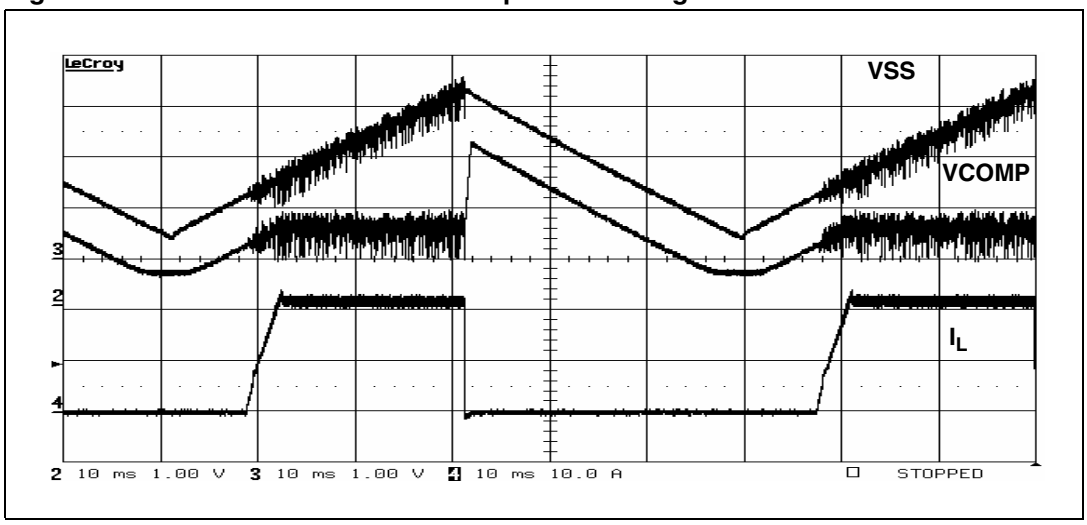
$$I_{MAX} = I_{VALLEY} + \frac{Vin - Vout}{L} \cdot T_{ON,MIN}$$

During soft-start the OC acts in constant current mode: a current control loop limits the value of the error amplifier output (comp), in order to avoid its saturation and thus recover faster when the output returns in regulation. *Figure 12.* shows the behavior of the device during an over current condition that persists also in the soft-start phase.

L6732 provides under voltage (UV) protection: when the voltage on FB pin falls below 80 % of the reference, the IC will enter HICCUP mode.

Feedback disconnection is also provided by sourcing a 100 nA current from FB pin. if FB results being floating, the IC will detect and OV so latching its condition with Low Side MOSFET firmly ON

**Figure 12. Constant current and hiccup mode during an OCP**




## 5.9 Thermal shutdown

When the junction temperature reaches 150 °C ±10 °C the device enters in thermal shutdown. Both MOSFETs are turned off and the soft-start capacitor is rapidly discharged with an internal switch. The device doesn't restart until the junction temperature goes down to 120 °C and, in any case, until the voltage at the soft-start pin reaches 500 mV.

## 5.10 Synchronization

The presence of many converters on the same board can generate beating frequency noise. To avoid this it is important to make them operate at the same switching frequency. Moreover, a phase shift between different modules helps to minimize the RMS current on the common input capacitors. *Figure 13* and *Figure 14* shows the results of two modules in synchronization. Two or more devices can be synchronized simply connecting together the SYNCH pins. The device with the higher switching frequency will be the Master while the

other one will be the slave. The Slave controller will increase its switching frequency reducing the ramp amplitude proportionally and then the modulator gain will be increased.

**Figure 13. Synchronization: PWM signal**

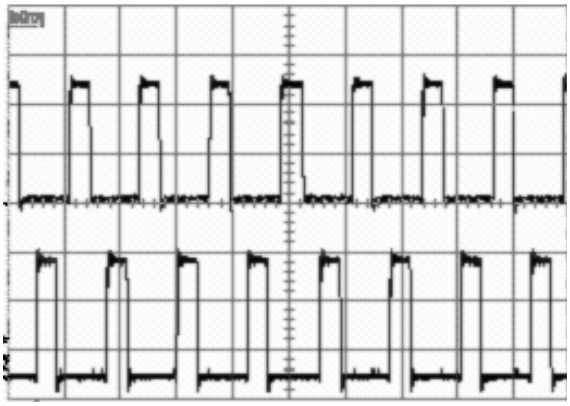
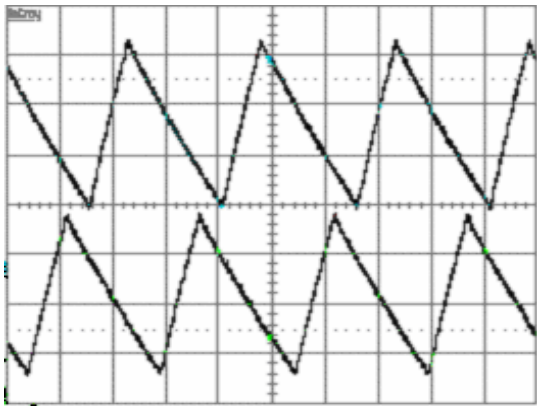


**Figure 14. Synchronization: Inductor currents**



To avoid a huge variation of the modulator gain, the best way to synchronize two or more devices is to make them work at the same switching frequency and, in any case, the switching frequencies can differ for a maximum of 50 % of the lowest one. If, during synchronization between two (or more) L6732, it's important to know in advance which the master is, it's timely to set its switching frequency at least 15 % higher than the slave. Using an external clock signal ($f_{EXT}$) to synchronize one or more devices that are working at a different switching frequency ($f_{SW}$) it is recommended to follow the below formula:

**Equation 5**

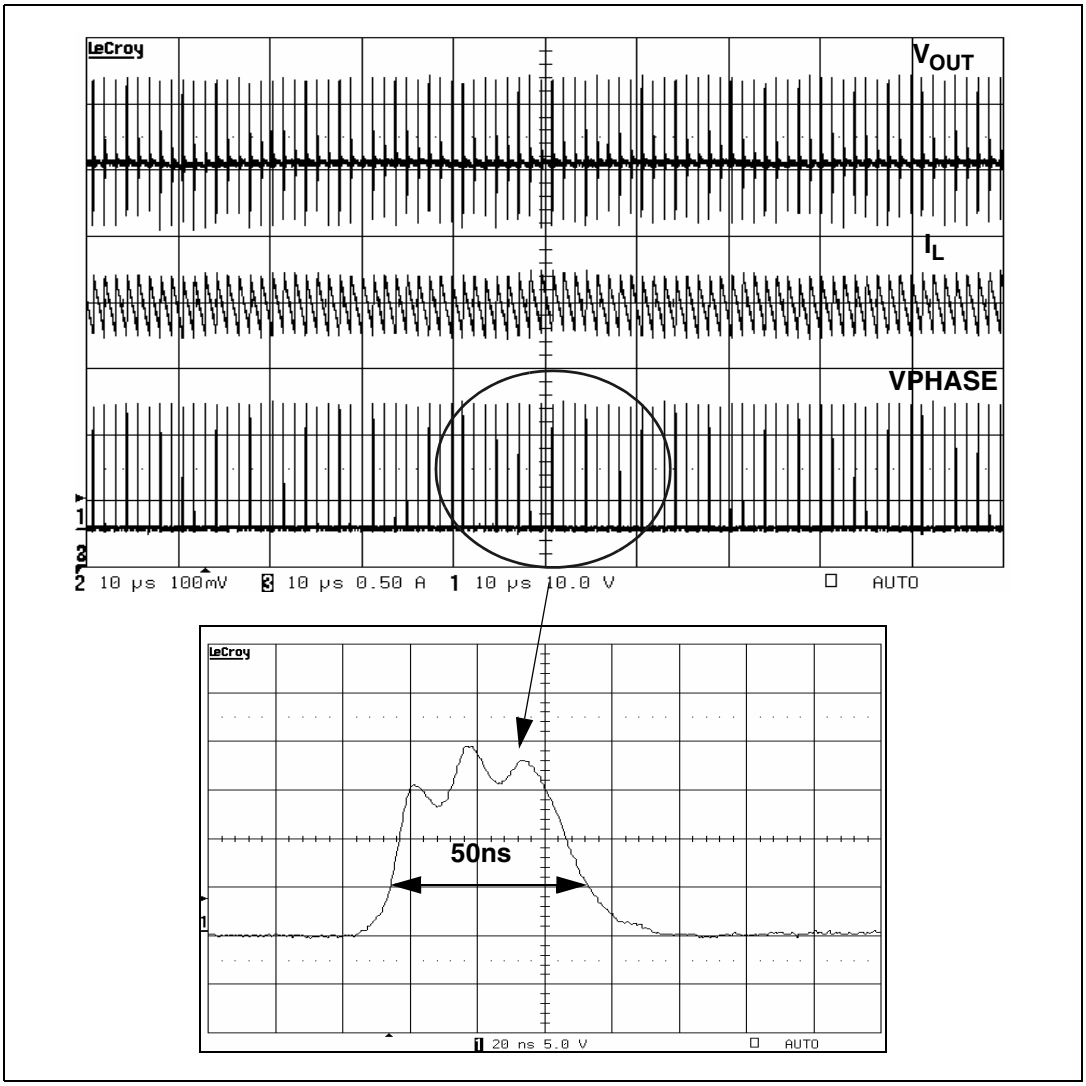
$$f_{SW} \leq f_{EXT} \leq 1{,}3 \cdot f_{SW}$$

The phase shift between master and slaves is approximately 180 °.

## 5.11 Minimum on-time ($T_{ON, MIN}$)

The device can manage minimum on-times lower than 100 ns. This feature comes down from the control topology and from the particular over-current-protection system of the L6732. In fact, in a voltage mode controller the current has not to be sensed to perform the regulation and, in the case of L6732, neither for the over-current protection, given that during the off-time the valley-current-protection can operate in every case. The first advantage related to this feature is the possibility to realize extremely low conversion ratios. *Figure 15* shows a conversion from 14 V to 0.3 V at 500 kHz with a $T_{ON}$ of about 50 ns.

**Figure 15. 14 V -> 0.3 V @ 500 kHz, 5 A**




The on-time is limited by the turn-on and turn-off times of the MOSFETs.

## 5.12 Bootstrap anti-discharging system

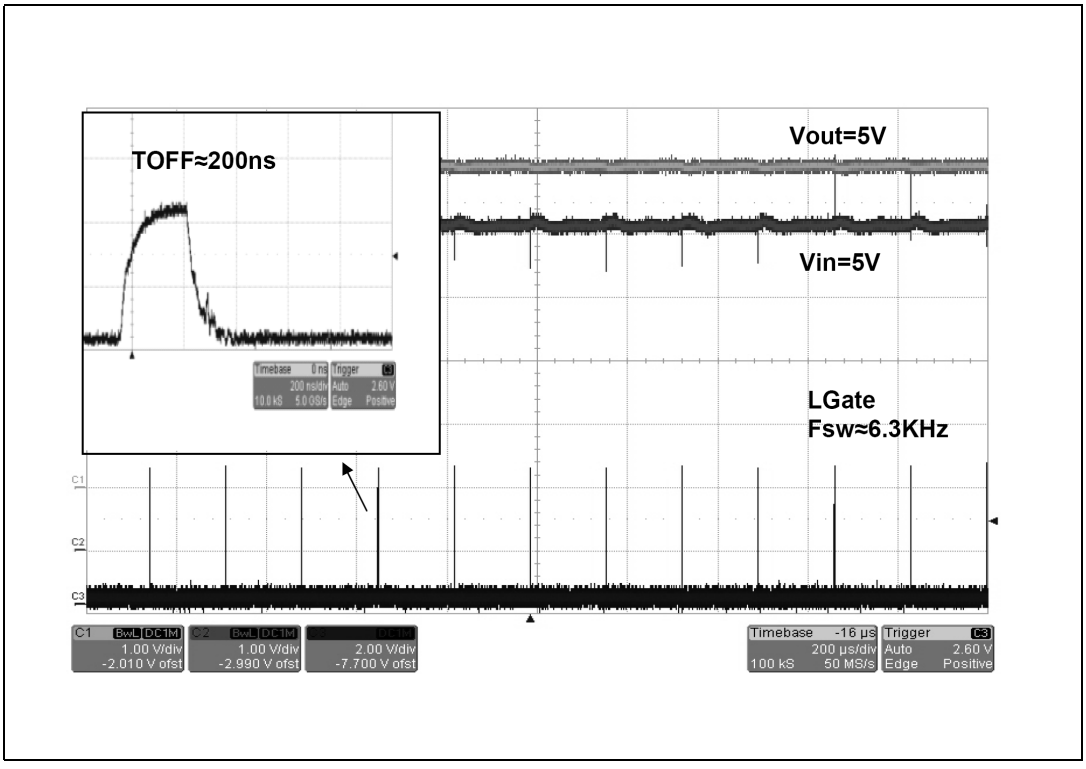
This built-in system avoids that the voltage across the bootstrap capacitor becomes less than 3.3 V. An internal comparator senses the voltage across the external bootstrap capacitor keeping it charged, eventually turning-on the low-side MOSFET for approximately 200 ns. If the bootstrap capacitor is not enough charged the high-side MOSFET cannot be effectively turned-on and it will present a higher $R_{DS(on)}$. In some cases the OCP can be also triggered. The bootstrap capacitor can be discharged during the soft-start in case of very long soft-start time and light loads. It's also possible to mention one application condition during which the bootstrap capacitor can be discharged:

### 5.12.1 Fan's power supply

In many applications the FAN is a DC MOTOR driven by a voltage-mode DC/DC converter. Often only the speed of the MOTOR is controlled by varying the voltage applied to the input terminal and there's no control on the torque because the current is not directly controlled. In order to vary the MOTOR speed the output voltage of the converter must be varied. The L6732 has a dedicated pin called EAREF (see the related section) that allows providing an external reference to the non-inverting input of the error-amplifier.

In these applications the duty cycle depends on the MOTOR's speed and sometimes 100 % has to be set in order to go at the maximum speed. Unfortunately in these conditions the bootstrap capacitor can not be recharged and the system cannot work properly. Some PWM controller limits the maximum duty-cycle to 80-90 % in order to keep the bootstrap cap charged but this make worse the performance during the load transient. Thanks to the “bootstrap anti-discharging system” the L6732 can work at 100 % without any problem. The following picture shows the device behavior when input voltage is 5 V and 100 % is set by the external reference.

**Figure 16. 100 % duty cycle operation**



# 6 Application details

## 6.1 Inductor design

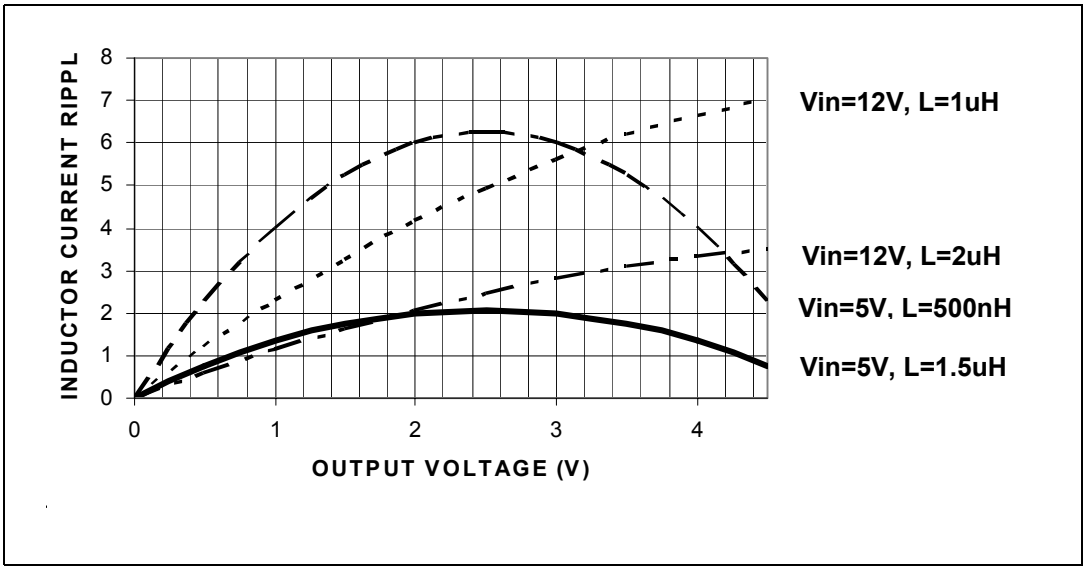
The inductance value is defined by a compromise between the transient response time, the efficiency, the cost and the size. The inductor has to be calculated to sustain the output and the input voltage variation to maintain the ripple current ($\Delta I_L$) between 20 % and 30 % of the maximum output current. The inductance value can be calculated with the following relationship:

**Equation 6**

$$L \cong \frac{Vin - Vout}{Fsw \cdot \Delta I_L} \cdot \frac{Vout}{Vin}$$

Where $F_{SW}$ is the switching frequency, $V_{IN}$ is the input voltage and $V_{OUT}$ is the output voltage. *Figure 17.* shows the ripple current vs. the output voltage for different values of the inductor, with $V_{IN}$ = 5 V and $V_{IN}$ = 12 V at a switching frequency of 500 kHz.

**Figure 17. Inductor current ripple**




Increasing the value of the inductance reduces the ripple current but, at the same time, increases the converter response time to a load transient. If the compensation network is well designed, during a load transient the device is able to set the duty cycle to 100 % or to 0 %. When one of these conditions is reached, the response time is limited by the time required to change the inductor current. During this time the output current is supplied by the output capacitors. Minimizing the response time can minimize the output capacitor size.

## 6.2 Output capacitors

The output capacitors are basic components for the fast transient response of the power supply. They depend on the output voltage ripple requirements, as well as any output voltage deviation requirement during a load transient. During a load transient, the output capacitors supply the current to the load or absorb the current stored in the inductor until the converter reacts. In fact, even if the controller recognizes immediately the load transient and sets the duty cycle at 100% or 0%, the current slope is limited by the inductor value. The output voltage has a first drop due to the current variation inside the capacitor (neglecting the effect of the ESL):

**Equation 7**

$$\Delta Vout_{ESR} = \Delta Iout \cdot ESR$$

Moreover, there is an additional drop due to the effective capacitor discharge or charge that is given by the following formulas:

**Equation 8**

$$\Delta Vout_{COUT} = \frac{\Delta Iout^2 \cdot L}{2 \cdot Cout \cdot (Vin, \min \cdot D \max - Vout)}$$

**Equation 9**

$$\Delta Vout_{COUT} = \frac{\Delta Iout^2 \cdot L}{2 \cdot Cout \cdot Vout}$$

Formula (8) is valid in case of positive load transient while the formula (9) is valid in case of negative load transient. $D_{MAX}$ is the maximum duty cycle value that in the L6732 is 100%. For a given inductor value, minimum input voltage, output voltage and maximum load transient, a maximum ESR and a minimum $C_{OUT}$ value can be set. The ESR and $C_{OUT}$ values also affect the static output voltage ripple. In the worst case the output voltage ripple can be calculated with the following formula:

**Equation 10**

$$\Delta Vout = \Delta I_L \cdot (ESR + \frac{1}{8 \cdot Cout \cdot Fsw})$$

Usually the voltage drop due to the ESR is the biggest one while the drop due to the capacitor discharge is almost negligible.

## 6.3 Input capacitors

The input capacitors have to sustain the RMS current flowing through them, that is:

**Equation 11**

$$Irms = Iout \cdot \sqrt{D \cdot (1 - D)}$$

Where D is the duty cycle. The equation reaches its maximum value, $I_{OUT}$ /2 with D = 0.5. The losses in worst case are:

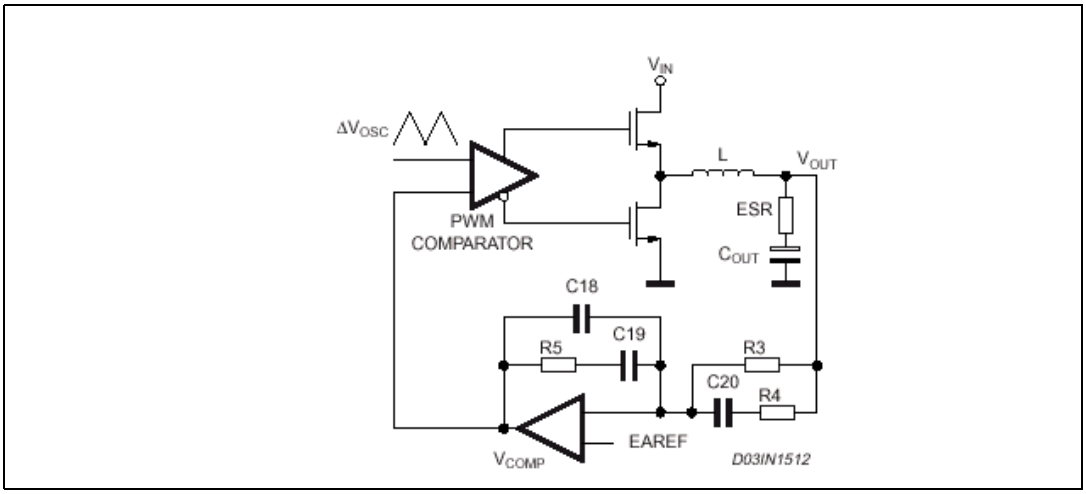
**Equation 12**

$$P = ESR \cdot (0.5 \cdot Iout)^2$$

## 6.4 Compensation network

The loop is based on a voltage mode control (*Figure 18.*). The output voltage is regulated to the internal/external reference voltage and scaled by the external resistor divider. The error amplifier output $V_{COMP}$ is then compared with the oscillator triangular wave to provide a pulse-width modulated (PWM) with an amplitude of $V_{IN}$ at the PHASE node. This waveform is filtered by the output filter. The modulator transfer function is the small signal transfer function of $V_{OUT}/V_{COMP}$. This function has a double pole at frequency $F_{LC}$ depending on the L-$C_{OUT}$ resonance and a zero at FESR depending on the output capacitor's ESR. The DC Gain of the modulator is simply the input voltage $V_{IN}$ divided by the peak-to-peak oscillator voltage: $V_{OSC}$.

**Figure 18. Compensation network**




The compensation network consists in the internal error amplifier, the impedance networks $Z_{IN}$ (R3, R4 and C20) and $Z_{FB}$ (R5, C18 and C19). The compensation network has to provide a closed loop transfer function with the highest 0dB crossing frequency to have fastest transient response (but always lower than fsw/10) and the highest gain in DC conditions to minimize the load regulation error. A stable control loop has a gain crossing the 0dB axis with -20dB/decade slope and a phase margin greater than 45 °. To locate poles and zeroes of the compensation networks, the following suggestions may be used:

- Modulator singularity frequencies:

**Equation 13**

$$\omega_{LC} = \frac{1}{\sqrt{L \cdot Cout}}$$

**Equation 14**

$$\omega_{ESR} = \frac{1}{ESR \cdot Cout}$$

- Compensation network singularity frequencies:

**Equation 15**

$$\omega_{P1} = \frac{1}{R_5 \cdot \left( \frac{C_{18} \cdot C_{19}}{C_{18} + C_{19}} \right)}$$

**Equation 16**

$$\omega_{P2} = \frac{1}{R_4 \cdot C_{20}}$$

**Equation 17**

$$\omega_{Z1} = \frac{1}{R_5 \cdot C_{19}}$$

**Equation 18**

$$\omega_{Z2} = \frac{1}{C_{20} \cdot (R_3 + R_4)}$$

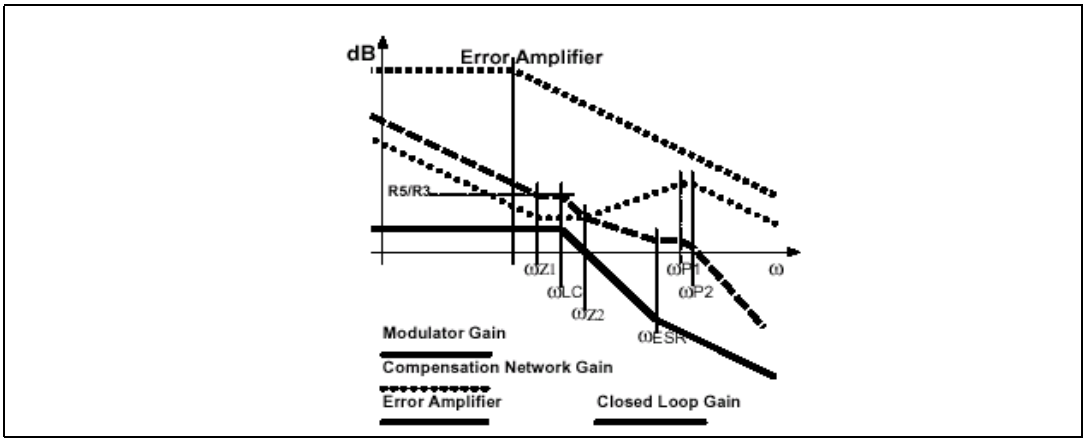
- Compensation network design:
  - Put the gain $R_5/R_3$ in order to obtain the desired converter bandwidth

**Equation 19**

$$\varpi_C = \frac{R_5}{R_3} \cdot \frac{Vin}{\Delta Vosc} \cdot \varpi_{LC}$$

  - Place $\omega_{Z1}$ before the output filter resonance $\omega_{LC}$;
  - Place $\omega_{Z2}$ at the output filter resonance $\omega_{LC}$;
  - Place $\omega_{P1}$ at the output capacitor ESR zero $\omega_{ESR}$;
  - Place $\omega_{P2}$ at one half of the switching frequency;
  - Check the loop gain considering the error amplifier open loop gain.

**Figure 19. Asymptotic bode plot of converter's open loop gain**



# 7 L6732 demonstration board

## 7.1 20 A board description and PCB layout

L6732 20 A demonstration board realizes in a four layer PCB a step-down DC/DC converter and shows the operation of the device in a general purpose application. The input voltage can range from 4.5 V to 14 V and the output voltage is at 3.3 V. The module can deliver an output current in excess of 20 A. The switching frequency is set at 250 kHz (controller free-running Fsw) but it can be set to 500 kHz acting on the EAREF pin.

**Figure 20. Demonstration board schematic**

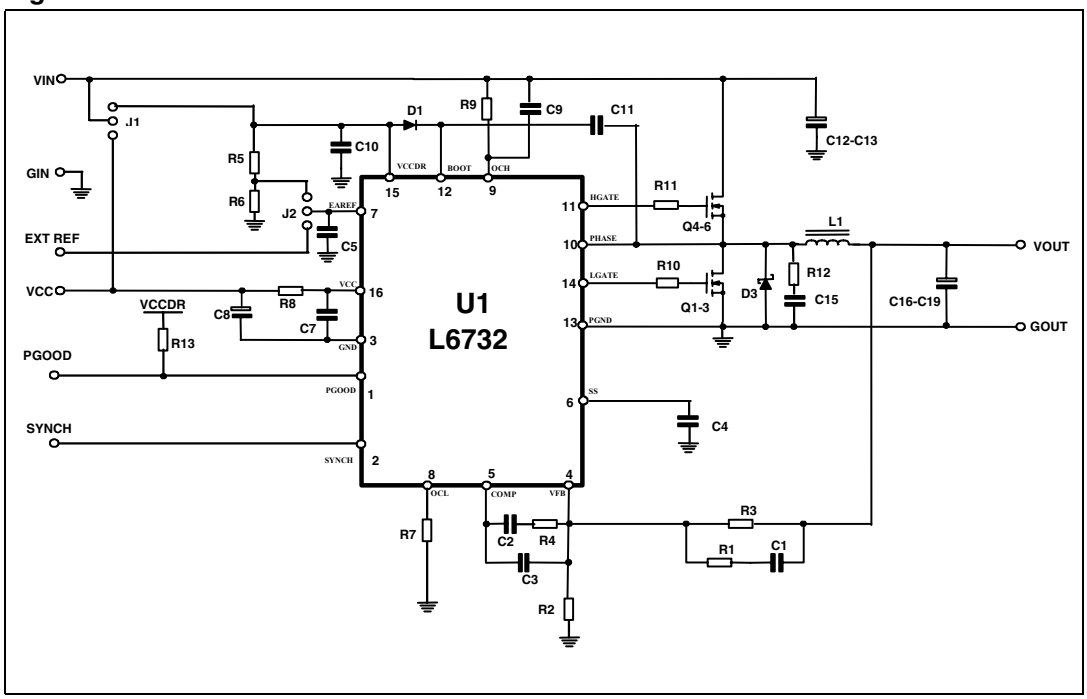


Table 7. Demonstration board part list

| Reference | Value | Manufacturer | Package | Supplier |
|---|---|---|---|---|
| R1 | 1 kΩ | Neohm | SMD 0603 | IFARCAD |
| R2 | 1 kΩ | Neohm | SMD 0603 | IFARCAD |
| R3 | 4 k7 | | | |
| R4 | 2 k7 | Neohm | SMD 0603 | IFARCAD |
| R5 | 0 Ω | Neohm | SMD 0603 | IFARCAD |
| R6 | N.C. | Neohm | SMD 0603 | IFARCAD |
| R7 | 2 K | Neohm | SMD 0603 | IFARCAD |
| R8 | 10 Ω | Neohm | SMD 0603 | IFARCAD |
| R9 | 1 k5 | Neohm | SMD 0603 | IFARCAD |
| R10 | 2.2 Ω | Neohm | SMD 0603 | IFARCAD |
| R11 | 2.2 Ω | Neohm | SMD 0603 | IFARCAD |
| R12 | N.C. | Neohm | SMD 0603 | IFARCAD |
| R13 | 10 k | Neohm | SMD 0603 | IFARCAD |
| C1 | 4.7 nF | Kemet | SMD 0603 | IFARCAD |
| C2 | 47 nF | Kemet | SMD 0603 | IFARCAD |
| C3 | 1 nF | Kemet | SMD 0603 | IFARCAD |
| C4 | 100 nF | Kemet | SMD 0603 | IFARCAD |
| C5 | 100 nF | Kemet | SMD 0603 | IFARCAD |
| C6 | N.C. | / | / | / |
| C7 | 100 nF | Kemet | SMD 0603 | IFARCAD |
| C8 | 4.7 µF 20 V | AVX | SMA6032 | IFARCAD |
| C9 | 1 nF | Kemet | SMD 0603 | IFARCAD |
| C10 | 1 µF | Kemet | SMD 0603 | IFARCAD |
| C11 | 220 nF | Kemet | SMD 0603 | IFARCAD |
| C12-13 | 3X 15 µF | / | / | ST (TDK) |
| C15 | N.C. | / | / | / |
| C16-19 | 2X 330 µF | / | / | ST (poscap) |
| L1 | 1.8 µH | Panasonic | SMD | ST |
| D1 | STPS1L30M | ST | DO216AA | ST |
| D3 | STPS1L30M | ST | DO216AA | ST |
| Q1-Q2 | STS12NH3LL | ST | SO8 | ST |
| Q4-Q5 | STS25NH3LL | ST | SO8 | ST |
| U1 | L6732 | ST | HTSSOP16 | ST |

**Table 8. Other inductor manufacturer**

| Manufacturer | Series | Inductor value (µH) | Saturation current (A) |
|---|---|---|---|
| Wurth elektronic | 744318180 | 1.8 | 20 |
| SUMIDA | CDEP134-2R7MC-H | 2.7 | 15 |
| EPCOS | HPI_13 T640 | 1.4 | 22 |
| TDK | SPM12550T-1R0M220 | 1 | 22 |
| TOKO | FDA1254 | 2.2 | 14 |
| COILTRONICS | HCF1305-1R0 | 1.15 | 22 |
| | HC5-1R0 | 1.3 | 27 |

**Table 9. Other capacitor manufacturer**

| Manufacturer | Series | Capacitor value (µF) | Rated voltage (V) |
|---|---|---|---|
| TDK | C4532X5R1E156M | 15 | 25 |
| | C3225X5R0J107M | 100 | 6.3 |
| NIPPON CHEMI-CON | 25PS100MJ12 | 100 | 25 |
| PANASONIC | ECJ4YB0J107M | 100 | 6.3 |

**Figure 21. Demonstration board efficiency**

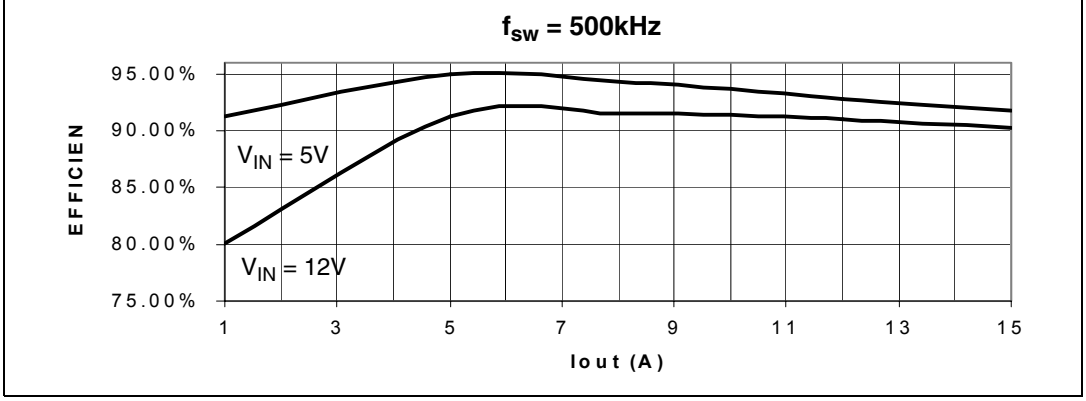


Figure 22. Top layer

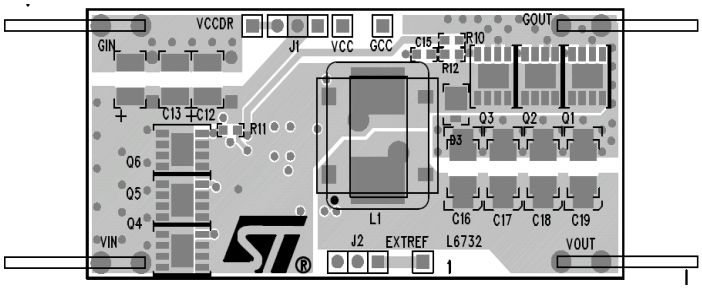



Figure 23. Power ground layer

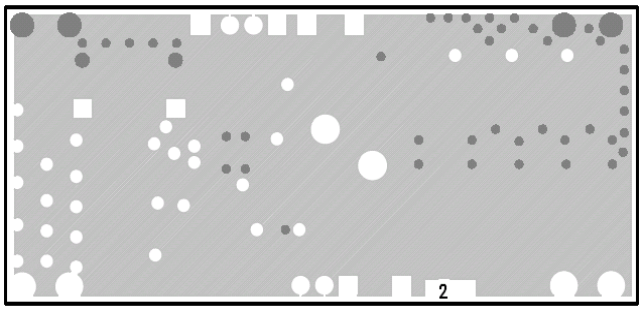



Figure 24. Signal-ground layer

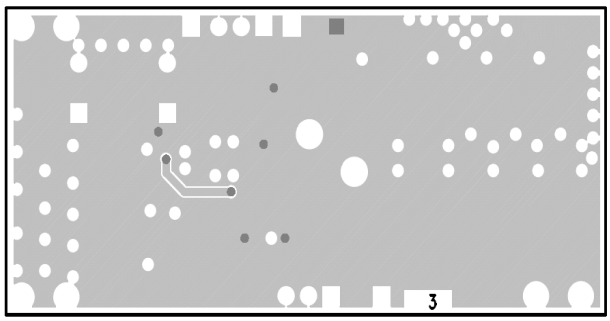
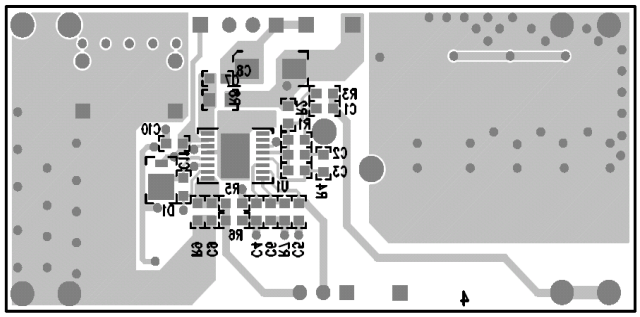



Figure 25. Bottom layer



## 7.2 5 A board description and PCB layout

L6732 5 A demonstration board realizes in a two layer PCB a step-down DC/DC converter and shows the operation of the device in a general purpose application. The input voltage can range from 4.5 V to 14 V and the output voltage is at 3.3 V. The module can deliver an output current of up to 5 A. The switching frequency is set at 250 kHz (controller free-running $F_{SW}$) but it can be set to 500 kHz acting on the EAREF pin. Compared to the 20 A version, the only difference of this board, compared to the first one, is the presence of a dual MOSFET chip, for the high-side and low-side MOSFETs; besides R15 has been inserted between High side MOSFET gate and phase pin; R14 has been inserted between low side MOSFET gate and Pgnd pin.

**Table 10. Demonstration board part list**

| Reference | Value | Manufacturer | Package | Supplier |
|---|---|---|---|---|
| R1 | 1 kΩ | Neohm | SMD 0603 | IFARCAD |
| R2 | 1 kΩ | Neohm | SMD 0603 | IFARCAD |
| R3 | 4 K7 | | | |
| R4 | 2 k7 | Neohm | SMD 0603 | IFARCAD |
| R5 | 0 Ω | Neohm | SMD 0603 | IFARCAD |
| R6 | N.C. | Neohm | SMD 0603 | IFARCAD |
| R7 | 4 k99 | Neohm | SMD 0603 | IFARCAD |
| R8 | 10 Ω | Neohm | SMD 0603 | IFARCAD |
| R9 | 2 k49 | Neohm | SMD 0603 | IFARCAD |
| R10 | 2.2 Ω | Neohm | SMD 0603 | IFARCAD |
| R11 | 2.2 Ω | Neohm | SMD 0603 | IFARCAD |
| R12 | N.C. | Neohm | SMD 0603 | IFARCAD |
| R13 | 10 K | Neohm | SMD 0603 | IFARCAD |
| R14 | N.C. | Neohm | SMD 0603 | IFARCAD |
| R15 | N.C. | Neohm | SMD 0603 | IFARCAD |
| C1 | 4.7 nF | Kemet | SMD 0603 | IFARCAD |
| C2 | 47 nF | Kemet | SMD 0603 | IFARCAD |
| C3 | 1 nF | Kemet | SMD 0603 | IFARCAD |
| C4 | 100 nF | Kemet | SMD 0603 | IFARCAD |
| C5 | 100 nF | Kemet | SMD 0603 | IFARCAD |
| C6 | N.C. | / | / | / |
| C7 | 100 nF | Kemet | SMD 0603 | IFARCAD |
| C8 | 4.7 µF 20 V | AVX | SMA6032 | IFARCAD |
| C9 | 1 nF | Kemet | SMD 0603 | IFARCAD |
| C10 | 1 µF | Kemet | SMD 0603 | IFARCAD |
| C11 | 220 nF | Kemet | SMD 0603 | IFARCAD |

Table 10. Demonstration board part list (continued)

| Reference | Value | Manufacturer | Package | Supplier |
|---|---|---|---|---|
| C12-13 | 3X 10 µF | / | / | ST (TDK) |
| C15 | N.C. | / | / | / |
| C16-19 | 2X 330 µF | / | / | ST (poscap) |
| L1 | 2,7 µH DO3316P-272HC | Coilcraft | SMD | ST |
| D1 | STPS1L30M | ST | DO216AA | ST |
| D3 | STPS1L30M | ST | DO216AA | ST |
| Q1 | STS8DNH3LL (Dual MOSFET) | ST | SO8 | ST |
| U1 | L6732 | ST | HTSSOP16 | ST |

Figure 26. Demonstration board efficiency

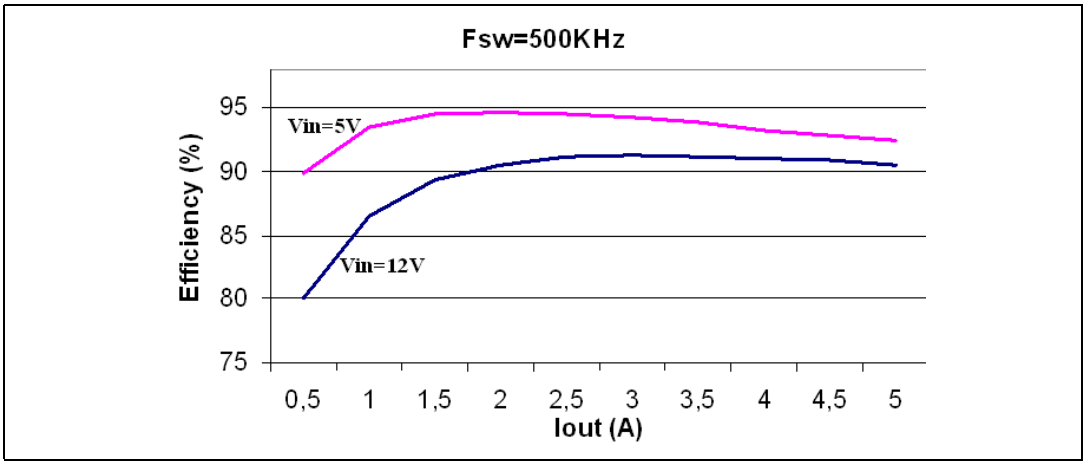


Figure 27. Top layer

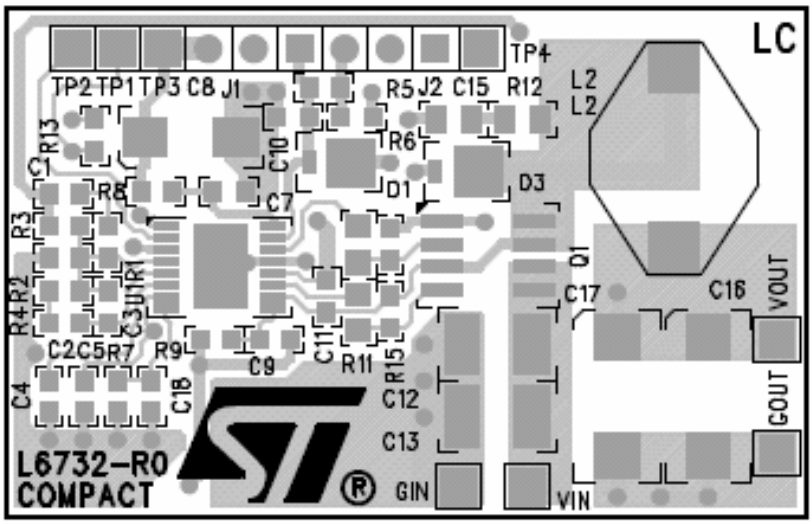
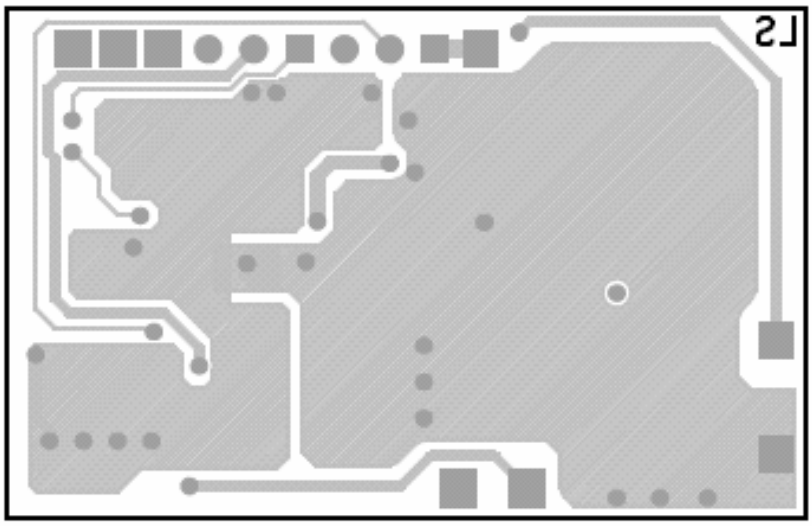



Figure 28. Power ground layer

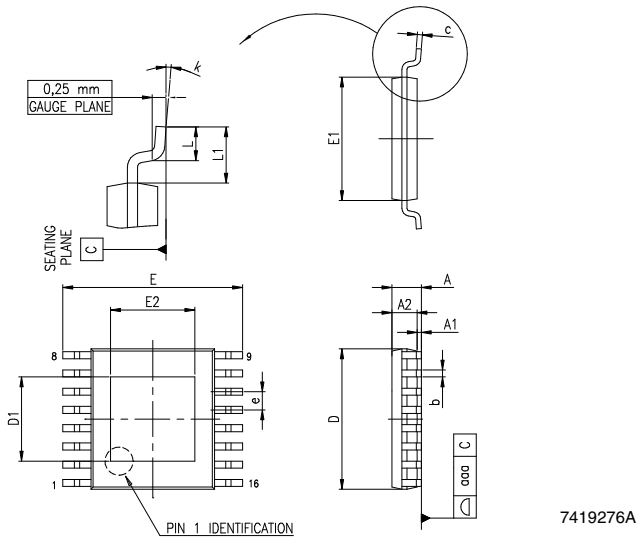


# 8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

**Figure 29. HTSSOP16 mechanical data**

| TSSOP16 EXPOSED PAD MECHANICAL DATA | | | | | | |
|---|---|---|---|---|---|---|
| DIM. | mm. | | | inch | | |
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.2 | | | 0.047 |
| A1 | | | 0.15 | | 0.004 | 0.006 |
| A2 | 0.8 | 1 | 1.05 | 0.031 | 0.039 | 0.041 |
| b | 0.19 | | 0.30 | 0.007 | | 0.012 |
| c | 0.09 | | 0.20 | 0.004 | | 0.0089 |
| D | 4.9 | 5 | 5.1 | 0.193 | 0.197 | 0.201 |
| D1 | | 3.0 | | | 0.118 | |
| E | 6.2 | 6.4 | 6.6 | 0.244 | 0.252 | 0.260 |
| E1 | 4.3 | 4.4 | 4.5 | 0.169 | 0.173 | 0.177 |
| E2 | | 3.0 | | | 0.118 | |
| e | | 0.65 | | | 0.0256 | |
| K | 0° | | 8° | 0° | | 8° |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |



# 9 Revision history

Table 11. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 20-Dec-2005 | 1 | Initial release |
| 24-Jan-2006 | 2 | Improved description of soft-start, in case of pre-bias start-up |
| 29-May-2006 | 3 | New template, thermal data updated |
| 26-Jun-2006 | 4 | Note page 10 deleted |
| 25-Sep-2006 | 5 | New demonstration boards *Section 7: L6732 demonstration board on page 27* |
| 04-Jun-2008 | 6 | Updated: *Table 4 on page 7*, *Table 5 on page 9*, *Section 5.4 on page 12* |

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