THE DATASHEET OF

L99PM62XPTR

L99PM62XP

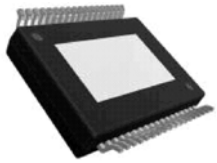
Power management IC with LIN and high speed CAN

Features

- Two 5V voltage regulators for microcontroller and peripheral supply
- No electrolytic capacitor required on regulator outputs
- Ultra low quiescent current in standby modes
- Programmable reset generator for power-on and undervoltage
- Configurable window watchdog and fail safe output
- LIN 2.1 compliant (SAEJ2602 compatible) transceiver
- Advanced HS CAN transceiver (ISO 11898-2/-5 and SAE J2284 compliant) with local failure and bus failure diagnosis
- HS CAN transceiver supports partial networking
- Complete 3 channel contact monitoring interface with programmable cyclic sense functionality
- Programmable periodic system wake up feature
- ST SPI interface for mode control and diagnosis
- 5 fully protected high-side drivers with internal 4-channel PWM generator
- 2 low-side drivers with active zener clamping
- 4 internal PWM timers
- 2 operational amplifiers with rail-to-rail outputs (V_S) and low voltage inputs
- Temperature warning and thermal shutdown

Applications

- Automotive ECU's such as door zone and body control modules



PowerSSO-36

Description

The L99PM62XP is a power management system IC providing electronic control units with enhanced system power supply functionality including various standby modes as well as LIN and HS CAN physical communication layers. It contains two low drop voltage regulators to supply the system microcontroller and external peripheral loads such as sensors and provides enhanced system standby functionality with programmable local and remote wake up capability.

In addition, five high-side drivers, two low-side drivers and two operational amplifiers increase the system integration level.

The ST standard SPI interface (3.0) allows control and diagnosis of the device and enables generic software development.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-36	L99PM62XP	L99PM62XPTR

Contents

List of tables

List of figures

1 Block diagram and pin descriptions

Figure 1. Block diagram

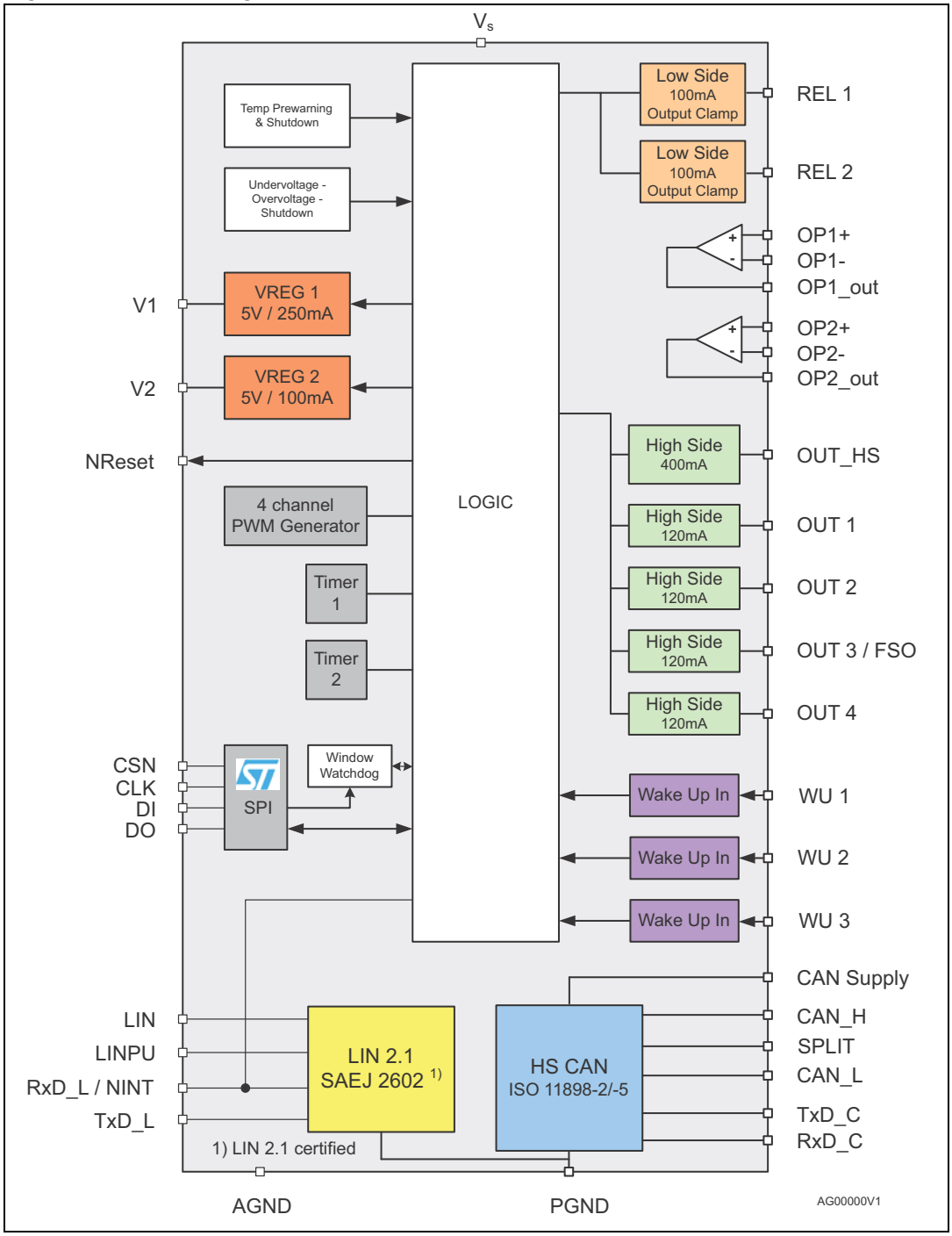


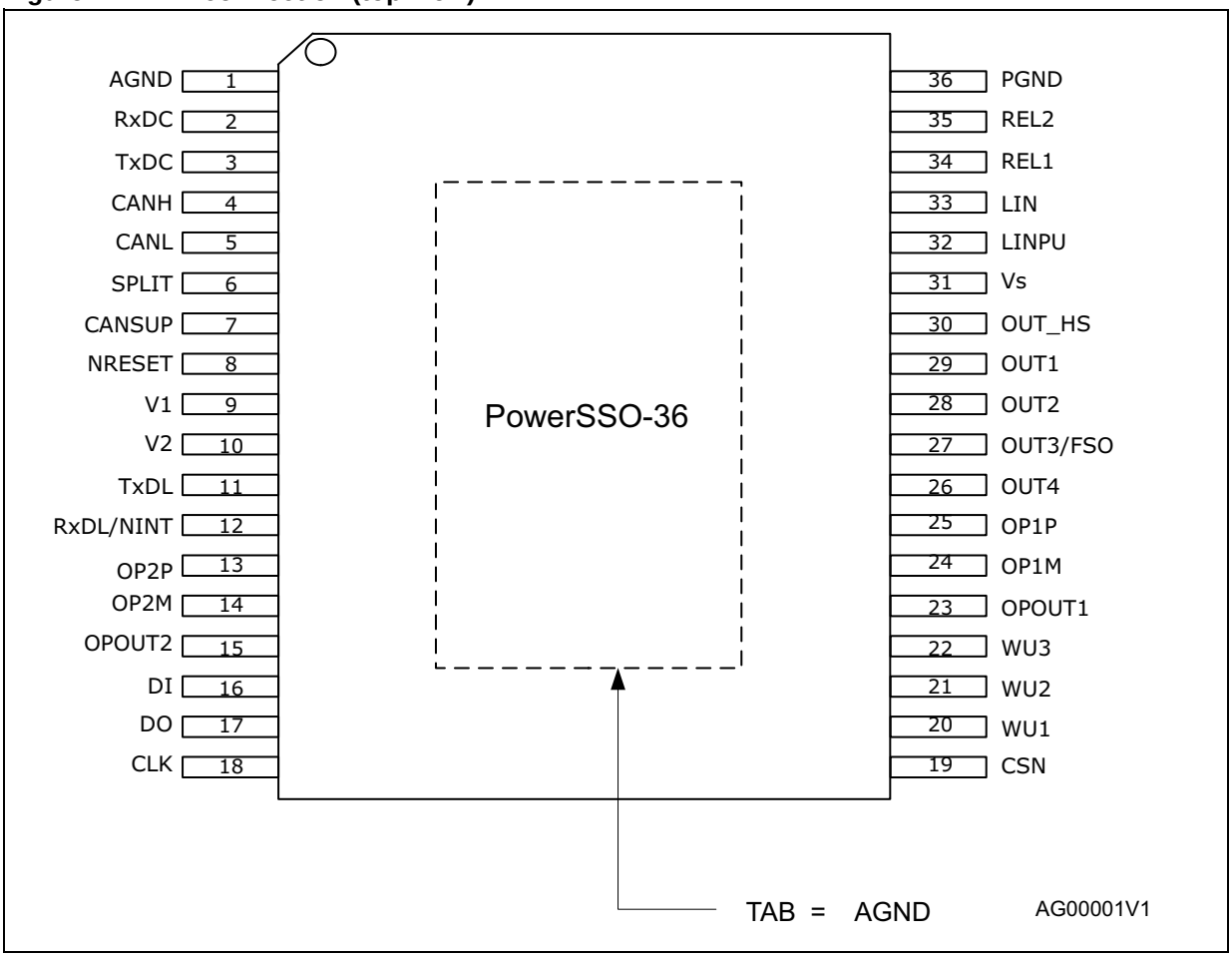
Table 2. Pin definition

Pin	Symbol	Function
1	AGND	Analog ground
2	RxDC	CAN receive data output
3	TxDC	CAN transmit data input
4	CANH	CAN high level voltage I/O
5	CANL	CAN low level voltage I/O
6	SPLIT	CAN reference voltage output, CAN termination
7	CANSUP	CAN supply input; to allow external CAN supply from V_1 or V_2 regulator.
8	NRESET	Nreset output to micro controller; Internal pull-up of typ. 100 KΩ (reset state = LOW)
9	V_1	Voltage regulator 1 output: 5 V supply e.g. micro controller, CAN transceiver
10	V_2	Voltage regulator 2 output: 5 V supply for external loads (IR receiver, potentiometer, sensors) or CAN Transceiver. V_2 is protected against reverse supply.
11	TxDL	LIN Transmit data input
12	RxDL/NINT	RxDL -> LIN receive data output NINT -> indicates local/remote wake-up events or provides a programmable timer interrupt signal
13	OP2+	Non inverting input of operational amplifier 2
14	OP2-	Inverting input of operational amplifier 2
15	OP2_OUT	Output of operational amplifier 2
16	DI	SPI: serial data input
17	DO	SPI: serial data output
18	CLK	SPI: serial clock input
19	CSN	SPI: chip select not input
20…22	WU1…3	Wake-up Inputs 1to 3: Input pins for static or cyclic monitoring of external contacts
23	OP1_OUT	Output of operational amplifier 1
24	OP1-	Inverting input of operational amplifier 1
25	OP1+	Non inverting input of operational amplifier 1
26	OUT4	High-side driver output (7 Ω, typ)
27	OUT3/FSO	Configurable as high-side driver output (7 Ω, typ) or fail safe output pin (default)
28	OUT2	High-side driver output (7 Ω, typ)
29	OUT1	High-side driver output (7 Ω, typ)
30	OUT_HS	High-side driver (1 Ω, typ)
31	V_S	Power supply voltage
32	LINPU	High-side driver output to switch off LIN master pull up resistor
33	LIN	LIN bus line
34	REL1	Low-side driver output (2 Ω typ)

Table 2. Pin definition (continued)

Pin	Symbol	Function
35	REL2	Low-side driver output (2 Ω typ)
36	PGND	Power ground (REL1/2, LIN and CAN GND), to be externally connected to AGND

Figure 2. Pin connection (top view)



Note: It is recommended to connect the PGND pin directly to the TAB.

2 Description

2.1 Voltage regulators

The L99PM62XP contains 2 independent and fully protected low drop voltage regulators, which are designed for very fast transient response and do not require electrolytic output capacitors for stability.

The output voltage is stable with ceramic load capacitors $\geq$ 220 nF.

2.1.1 Voltage regulator: V_1

The V_1 voltage regulator provides 5 V supply voltage and up to 250 mA continuous load current and is mainly intended for supply of the system microcontroller. The V_1 regulator is embedded in the power management and fail-safe functionality of the device and operates according to the selected operating mode.

It can be used to supply the internal HS CAN Transceiver via the CANSUP pin externally. In case of a short circuit condition on the CAN bus, the output current of the transmitter is limited to 100 mA and the transceiver is turned off in order to ensure continued supply of the microcontroller.

In addition the regulator V_1 drives the L99PM62XP internal 5 V loads. The voltage regulator is protected against overload and overtemperature. An external reverse current protection has to be provided by the application circuitry to prevent the input capacitor from being discharged by negative transients or low input voltage. The output voltage precision is better than +/- 2% (incl. temperature drift and line-/load regulation) in active mode; respectively +/- 3% during low current operation (i. e. in V_1 standby mode). Current limitation of the regulator ensures fast charge of external bypass capacitors. The output voltage is stable for ceramic load capacitors $\geq$ 220 nF.

If the device temperature exceeds the TSD1 threshold, all outputs (OUTx, RELx, V_2, LIN) is deactivated except V_1. Hence the micro controller has the possibility for interaction or error logging. In case of exceeding TSD2 threshold (TSD2>TSD1), also V_1 is deactivated (see state chart in *Chapter 3: Protection and diagnosis*). A timer is started and the voltage regulator is deactivated for t_{TSD} = 1sec. During this time, all other wakeup sources (CAN, LIN, WU1 to3 and wake up of µC by timer) are disabled. After 1 sec, the voltage regulator tries to restart automatically. If the restart fails 7 times, within one minute, without clearing and thermal shutdown condition still exists, the L99PM62XP enters the forced V_{BAT} standby Mode.

In case of short to GND at "V_1" after initial turn on (V_1 < 2V for at least 4ms) the L99PM62XP enters the forced V_{BAT} standby Mode. Reactivation (wake-up) of the device can be achieved with signals from CAN, LIN, WU1..3 or *periodic wake by timer* (see *Section 2.2.8: Timer interrupt / wake-up of microcontroller by timer*).

2.1.2 Voltage regulator: V_2

The voltage regulator V_2 can supply additional 5 V loads (e.g. logic components or the integrated HS CAN transceiver or external loads such as sensors or potentiometers). The

maximum continuous load current is 100 mA. The regulator provides accuracy better than ± 3% at 50 mA (4 % at 100 mA and is protected against.

- Overload
- Overtemperature
- Short circuit (short to ground and battery supply voltage)
- Reverse biasing

2.1.3 Increased output current capability for voltage regulator V_2

For applications which require high output currents, the output current capability of the regulator can be increased my means of the integrated operational amplifiers and an external pass transistor.

Figure 3. Voltage source with external PNP

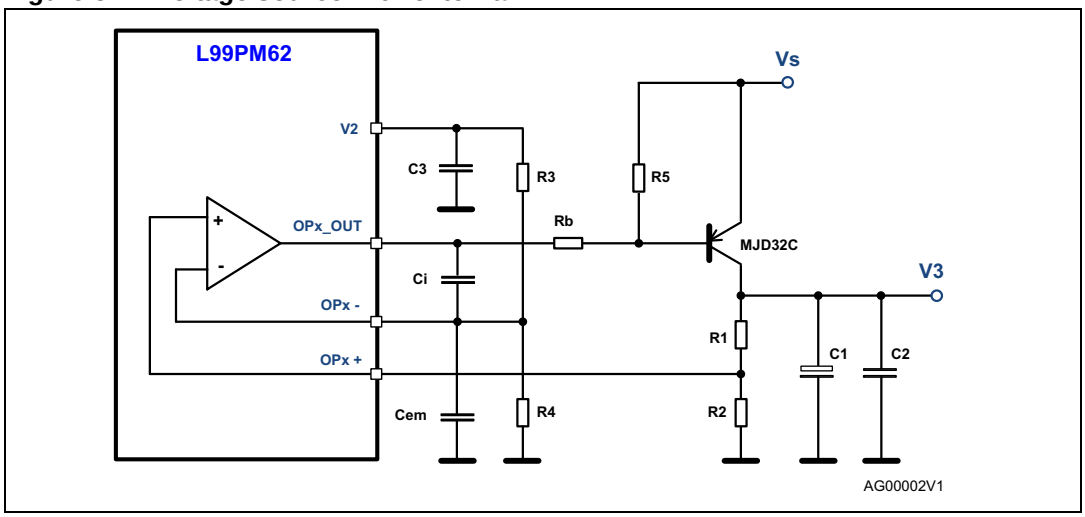


Figure 4. Voltage source with external PNP and current limitation

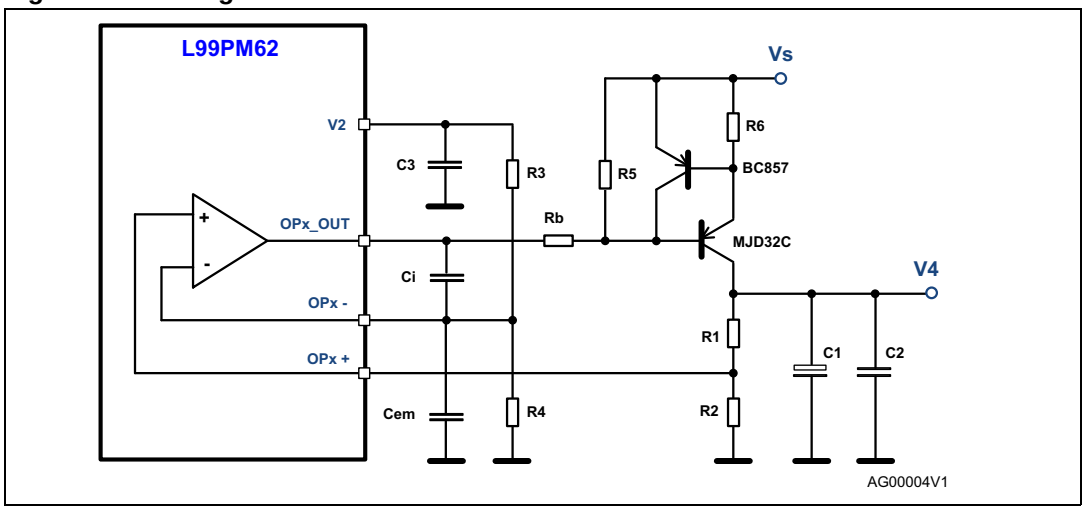


Figure 3 shows a possible configuration with a PNP pass element using voltage regulator 2 to provide the voltage reference for the regulated output voltage V3.

The Vs operating range for this circuit is 5.5 V to 18 V. It is important the respect the input common mode range specified for the operational amplifiers.

The output voltage V3 can be calculated using the following formula:

$$v_3 = \frac{v_2}{2} \cdot \frac{R_1 + R_2}{R_2}[V]$$

The circuit in *Figure 4* provides additional current limitation using an additional PNP transistor and R6 which allows setting the current limit.

Figure 5. Voltage source with external NPN

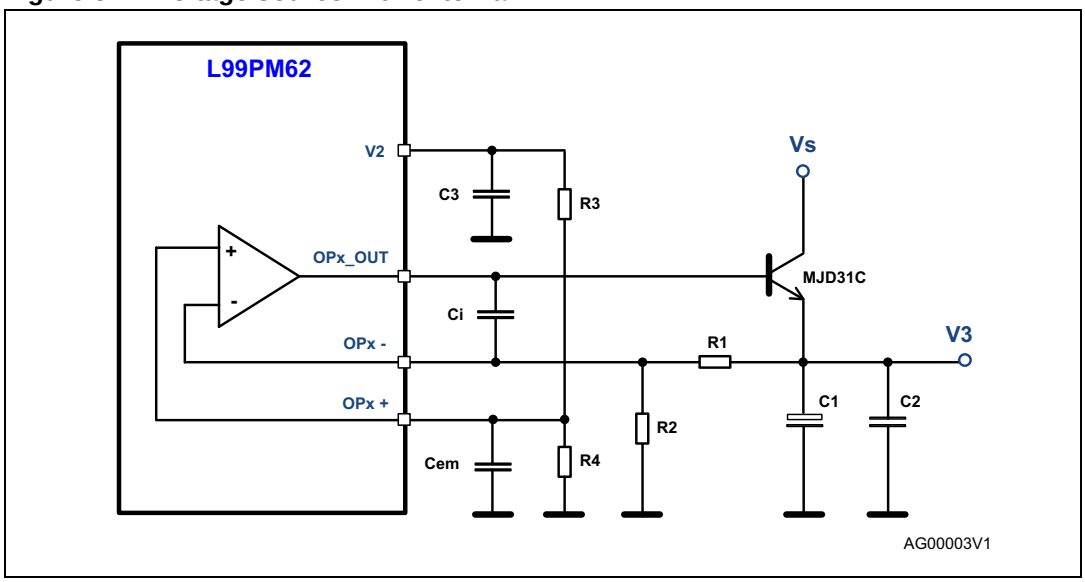


Figure 6. Voltage source with external NPN and current limitation

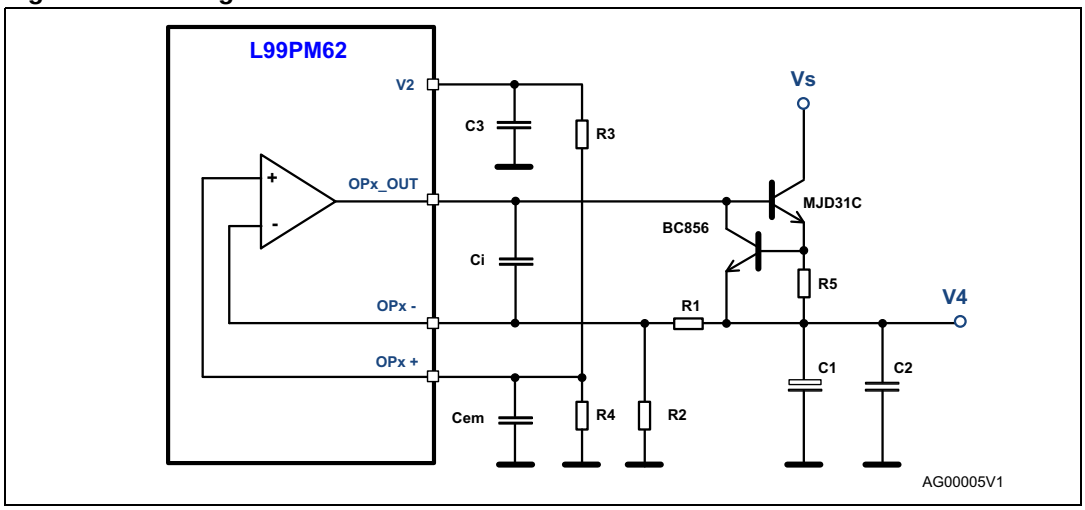


Figure 5 shows a possible configuration with an NPN pass element using voltage regulator 2 to provide the voltage reference for the regulated output voltage V3. This circuit requires fewer components compared to the configuration in *Figure 3* but has a limited Vs operating range (6 V to 18 V).

The output voltage V3 can be calculated using the following formula:

$$v_3 = \frac{v_2}{2} \cdot \frac{R_1 + R_2}{R_2} [V]$$

The circuit in *Figure 6* provides additional current limitation using an additional NPN transistor and R5 which allows setting the current limit.

Alternatively, voltage regulator 1 can be used to provide the 5 V reference for this topology. However, the additional current consumption through R3 and R4 has to be considered in V_1standby mode.

2.1.4 Voltage regulator failure

The $V_{1,}$ and V_2 regulator output voltages are monitored.

In case of a drop below the $V_{1,}$ V_2 – fail thresholds ($V_{1,2}$ < 2 V, typ for t > 2 µs), the $V_{1,2}$-fail bits are latched. The fail bits can be cleared by a dedicated SPI command.

Short to ground detection

If 4 ms after turn on of the regulator the $V_{1,2}$ voltage is below the $V_{1,2}$ fail thresholds, (independent for $V_{1,2}$), the L99PM62XP identifies a short circuit condition at the related regulator output and the regulator is switched off.

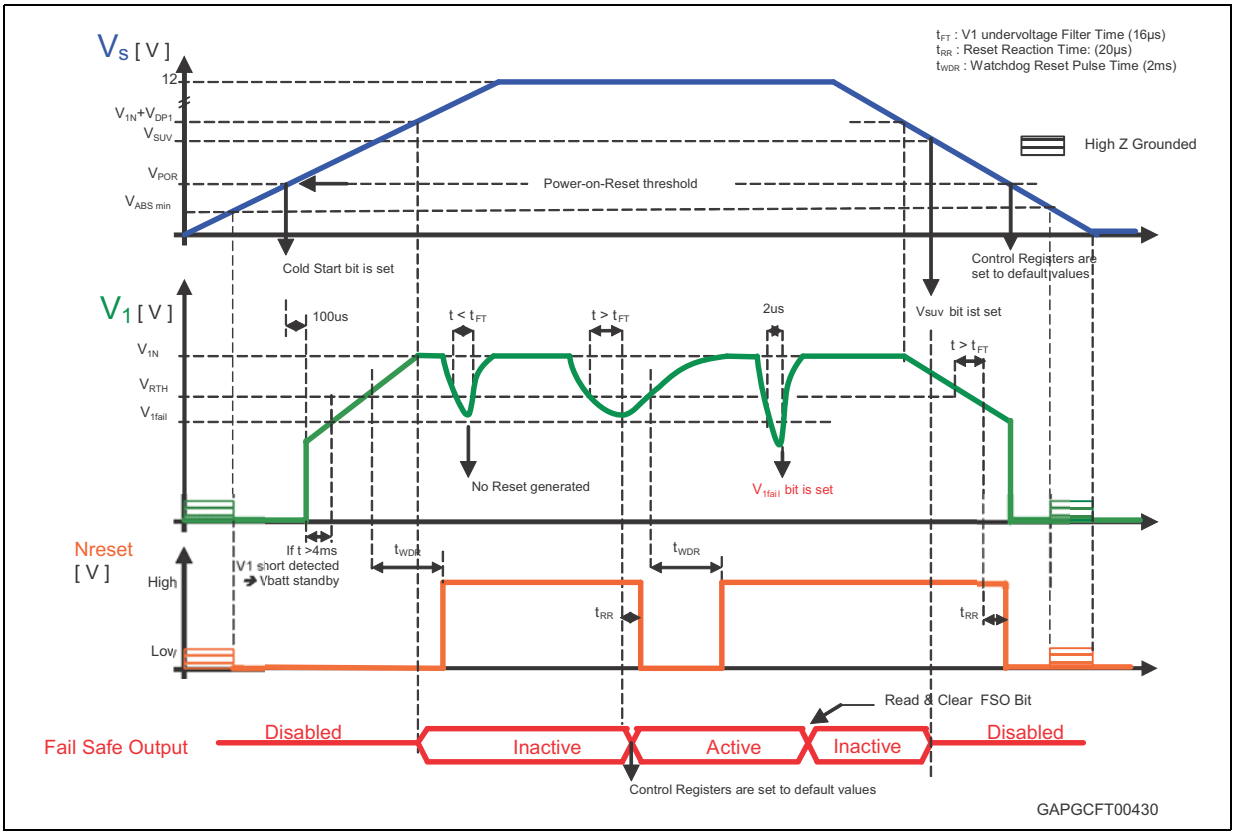
In case of V_1 short to GND failure the device enters V_{BAT} standby mode automatically. Bits Forced V_{BAT} STD2/SHTV_1 and V_1 fail were set.

In case of a V_2 short to GND failure the V_2short and V_2 fail bit is set.

If the output voltage of the corresponding regulator once exceeded the $V_{1,2}$ fail thresholds the short to ground detection is disabled. If a short to ground condition occurs the regulator outputs switches off due to thermal shutdown (V_1 at TSD2; V_2 at TSD1).

2.1.5 Voltage regulator behaviour

Figure 7. Voltage regulator behaviour and diagnosis during supply voltage ramp-up / ramp-down conditions



2.2 Operating modes

The L99PM62XP can be operated in 4 different operating modes:

- Active
- Flash
- V_1 standby
- V_{BAT} standby

A cyclic monitoring of wake-up inputs and a periodic interrupt/wake-up by timer is available in standby modes.

2.2.1 Active mode

All functions are available and the device is controlled by the ST SPI Interface.

2.2.2 Flash mode

To program the system microcontroller, the L99PM62 can be operated in Flash mode where the internal watchdog is disabled. This mode can also be used for software debugging.

Except for the disabled watchdog, the Flash mode is identical to active mode and all device features are available.

The mode can be entered if one of the following conditions is applied:

- $V_{TxDL} \geq V_{Flash}$
- $V_{TxDC} \geq V_{Flash}$

At exit from Flash mode ($V_{TxD} < V_{Flash}$) no NReset pulse is generated and the watchdog starts with a long open window.

Note: Setting both TxDL and TxDC to high voltage levels (> V_{Flash}) is not allowed

2.2.3 V_1 standby mode

The transition from active mode to V_1 standby mode is controlled by SPI.

To supply the micro controller in a low power mode, the voltage regulator 1 (V_1) remains active. In order to reduce the current consumption, the regulator goes in low current mode as soon as the supply current of the microcontroller goes below the I_{cmp} current threshold. At this transition, the L99PM62 also deactivates the internal watchdog.

Relay outputs, LIN and CAN transmitters is switched off in V_1 standby mode. High-side outputs and the V_2 regulator remain in the configuration programmed prior to the standby command.

A cyclic supply of external contacts and a synchronized monitoring of the contact state can be activated and configured by SPI.

In V_1 standby mode various wake up sources can be individually programmed. Each wake up event puts the device into active mode and forces the RxDL/NINT pin to a low level indicating the wake-up condition to the microcontroller.

After power ON reset (POR) all wake up sources are activated by default except the periodic interrupt/wake timer.

With the interrupt timer the micro controller can be forced from ‘stop’ to ‘run’ after a programmable period. The RxDL/NINT pin is forced low after the timer is elapsed. The L99PM62XP enters active mode and is awaiting a valid watchdog trigger.

Both internal timers can be used for this feature.

The interrupt timer (T_{INT}) at pin RxDL/NINT is only available in V_1 standby mode.

Note: Inputs TxDL, TxDC and CSN must be at high level or at high impedance in order to achieve minimum standby current in V_1 standby mode.

Inputs DI and CLK must be at GND or at high impedance to achieve minimum standby current in V_1 standby mode.

Interrupt

The interrupt signal (linked to RxDL/NINT internally) indicates a wake-up event from V_1 standby mode. In case of a wake-up by Wake-up Inputs, activity on LIN or CAN, SPI access or timer-interrupt the NINT pin is pulled low for 56 µs.

In case of V_1 standby mode and ($I_{V1} > I_{cmp}$), the device remains in standby mode, the V_1 regulator switches to high current mode and the watchdog starts. No Interrupt signal is generated.

2.2.4 V_{BAT} standby mode

The transition from active mode to V_{BAT} standby mode is initiated by an SPI command.

In V_{BAT} standby mode, the V_1 voltage regulator, relay outputs, LIN and CAN transmitters are switched off. High-side outputs and the V_2 regulator remain in the configuration programmed prior to the standby command.

In V_{BAT} standby mode the current consumption of the L99PM62XP is reduced to a minimum level.

Note: Inputs TXDL, TXDC and CSN must be terminated to GND in V_{BAT} standby to achieve minimum standby current.

This can be achieved with the internal ESD protection diodes of the microcontroller (microcontroller is not supplied in this mode; V_1 is pulled to GND).

2.2.5 Wake up from standby modes

A wake-up from standby mode switches the device to active mode. This can be initiated by one or more of the following events:

Table 3. Wake up sources

Wake up source	Description
LIN bus activity	Can be disabled by SPI
CAN bus activity	Can be disabled by SPI
Level change of WU1 - 3	Can be individually configured or disabled by SPI
$I_{V1} > I_{cmp}$	Device remains in V_1 standby mode but watchdog is enabled (If $I_{cmp} = 0$) and the V_1 regulator goes into high current mode (increased current consumption). No interrupt is generated.
Timer interrupt / wake up of µC by TIMER	Programmable by SPI – V_1 standby mode: device wakes up and Interrupt signal is generated at RxDL/NINT when programmable timeout has elapsed – V_{BAT} standby mode: device wakes up, V_1 regulator is turned on and NReset signal is generated when programmable timeout has elapsed
SPI access	Always active (except in V_{BAT} standby mode) Wake up event: CSN is low and first rising edge on CLK

To prevent the system from a deadlock condition (no wake up possible) a configuration where the periodic timer interrupt and wake up by LIN and HS CAN are disabled, is not allowed. The default configuration is entered for all wake-up sources in case of such an invalid setting.

All wake-up events from V_1 standby mode (except $I_{V1} > I_{cmp}$) are indicated to the microcontroller by a low-pulse at RxDL/NINT (duration: 56 µs).

Wake-up from V_1 standby by SPI Access might be used to check the interrupt service handler.

2.2.6 Wake-up inputs

The de-bounced digital inputs WU1 to WU3 can be used to wake up the L99PM62XP from standby modes. These inputs are sensitive to any level transition (positive and negative edge)

For static contact monitoring, a filter time of 64 µs is implemented at WU1-3. The filter is started when the input voltage passes the specified threshold.

In addition to the continuous sensing (static contact monitoring) at the wake up inputs, a cyclic sense functionality is implemented. This feature allows periodical activation of the wake-up inputs to read the status of the external contacts. The periodical activation can be linked to Timer1 or Timer2 (see *Section 2.2.7: Cyclic contact supply*). The input signal is filtered with a filter time of 16 µs after a programmable delay (80 µs or 800 µs) according to the configured timer on-time. A wake-up is processed if the status has changed versus the previous cycle.

The outputs OUT_HS and OUT1-4 can be used to supply the external contacts with the timer setting according to the cyclic monitoring of the wake-up inputs.

If the wake-up inputs are configured for cyclic sense mode the input filter timing and input filter delay (*WUx_filt* in control register 2) must correspond to the setting of the high-side output which supplies the external contact switches (OUTx in control register 0).

In standby mode, the inputs WU1-3 are SPI configurable for pull-up or pull-down current source configuration according to the setup of the external. In active mode the inputs have a pull down resistor.

In active mode, the input status can be read by SPI (Status Register 2). Static sense should be configured (Control Register 2) before the read operation is started (In cyclic sense configuration, the input status is updated according to the cyclic sense timing; Therefore, reading the input status in this mode may not reflect the actual status).

2.2.7 Cyclic contact supply

In V_1 standby and V_{BAT} standby modes, any high-side driver output (OUT1..4, OUTHS) can be used to periodically supply external contacts.

The timing is selectable by SPI

Timer 1: period is Xs. The on-time is 10 ms resp. 20 ms: With X ∈ {1, 2, 3, 4 s}

Timer 2: period is X ms. The on- time is 100 µs resp. 1ms: With X ∈ {10, 20, 50, 200 ms}

2.2.8 Timer interrupt / wake-up of microcontroller by timer

During standby modes the cyclic wake up feature, configured via SPI, allows waking up the µC after a programmable timeout according to timer1 or timer2.

From V_1 standby mode, the L99PM62XP wakes up (after the selected timer has elapsed) and sends an interrupt signal (via RxDL/NINT pin) to the µC. The device enters active mode and the watchdog is started with a long open window. The microcontroller can send the device back into V_1 standby after finishing its tasks.

From V_{BAT} standby mode, the L99PM62XP wakes up (after the selected timer has elapsed), turns on the V_1 regulator and provides an NReset signal to the µC. The device enters active mode and the watchdog is started with a long open window. The microcontroller can send the device back into V_{BAT} standby after finishing its tasks.

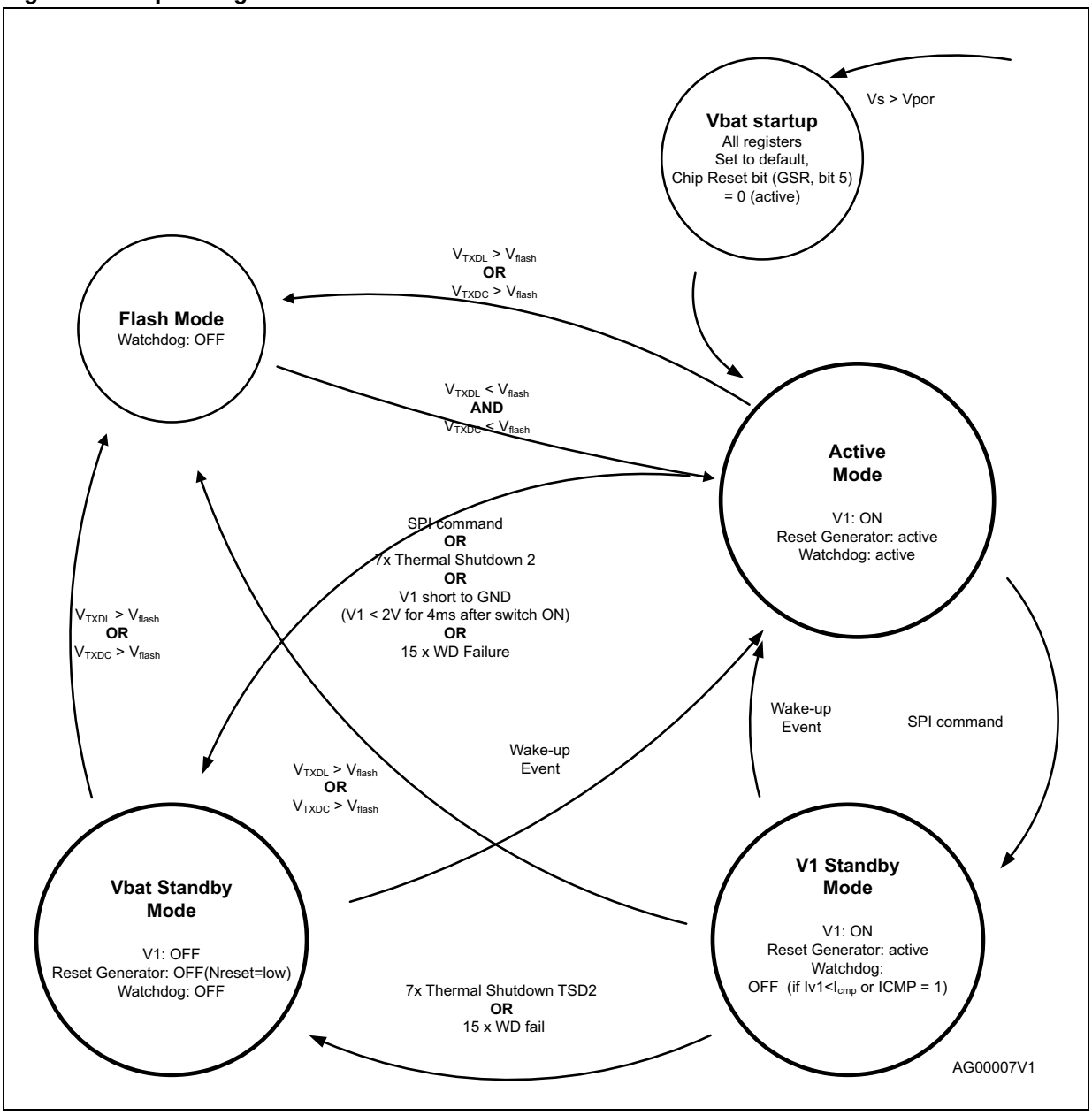
2.3 Functional overview (truth table)

Table 4. Functional overview (truth table)

Function	Comments	Operating modes		
		Active mode	V_1-standby static mode (cyclic sense)	V_{BAT}-standby static mode (cyclic sense)
Voltage-regulator, V_1	V_{OUT} = 5 V	On	On(1)	Off
Voltage-regulator, V_2	V_{OUT} = 5 V	On/ Off (2)	On(2) / Off	On(2) / Off
Reset-generator		On	On	Off
Window watchdog	V_1 monitor	On	Off (On: I_V_1 > I_{cmp}-threshold and I_{cmp} = 0)	Off
Wake up		Off	Active(3)	Active(3)
HS-cyclic supply	Oscillator time base	On / Off	On(2) / Off	On(2) / Off
Relay driver		On	Off	Off
Operational amplifiers		On	Off	Off
LIN	LIN 2.1	On	Off(4)	Off(4)
HS_CAN		On	Off(4)	Off(4)
FSO (if configured by SPI), active by default	Fail safe output	OUT3/FSO Off(5)	OUT3/FSO Off(5)	OUT3/FSO Off(5)
Oscillator		On	(6)	(6)
Vs-monitor		On	(7)	(7)

1. Supply the processor in low current mode.
2. Only active when selected via SPI.
3. Unless disabled by SPI.
4. The bus state is internally stored when going to standby mode. A change of bus state leads a wake-up after exceeding of internal filter time (if wake-up by LIN or CAN is not disabled by SPI).
5. ON in fail-safe condition: If Standby mode is entered with active Fail Safe mode, the output remains ON in Standby mode.
6. Activation = ON if cyclic sense is selected.
7. cyclic activation = pulsed ON during cyclic sense.

Figure 8. Operating modes



2.4 Configurable window watchdog

During normal operation, the watchdog monitors the micro controller within a programmable trigger cycle: (10 ms, 50 ms, 100 ms, 200 ms)

In V_{BAT} standby and Flash program modes, the watchdog circuit is automatically disabled. In V_1 standby mode a wake up by timer is programmable in order to wake up the µC (see *Section 2.2.8: Timer interrupt / wake-up of microcontroller by timer*). After wake-up, the watchdog starts with a long open window. After serving the watchdog, the µC may send the device back to V_1 standby mode.

After power-on or standby mode, the watchdog is started with a long open window (65 ms nominal). The long open window allows the micro controller to run its own setup and then to trigger the watchdog via the SPI. The trigger is processed when the CSN input becomes HIGH after the transmission of the SPI word.

Writing '1' to the watchdog trigger bit terminates the long open window and start the window watchdog (the timing is programmable by SPI). Subsequently, the micro controller has to serve the watchdog by alternating the watchdog trigger bit within the safe trigger area (refer to *Figure 27*). A correct watchdog trigger signal is immediately start the next cycle.

After 8 watchdog failures in sequence, the V_1 regulator is switched off for 200ms. If subsequently, 7 additional watchdog failures occur, the V_1 regulator is completely turned off and the device goes into V_{BAT} standby mode until a wakeup occurs.

In case of a watchdog failure, the outputs (RELx, OUTx, V_2) are switched off and the device enters fail-safe mode (i. e. all control registers are set to default values except the 'OUT3 control bit').

The following diagrams illustrate the watchdog behavior of the L99PM62. The diagrams are split into 3 parts. First diagram shows the functional behavior of the watchdog without any error. The second diagram covers the behavior covering all the error conditions, which can affect the watchdog behavior. Third diagram shows the transition in and out of Flash mode. All 3 diagrams can be overlapped to get all the possible state transitions under all circumstances. For a better readability, they were split in normal operating, operating with errors and Flash mode.

Figure 9. Watchdog in normal operating mode (no errors)

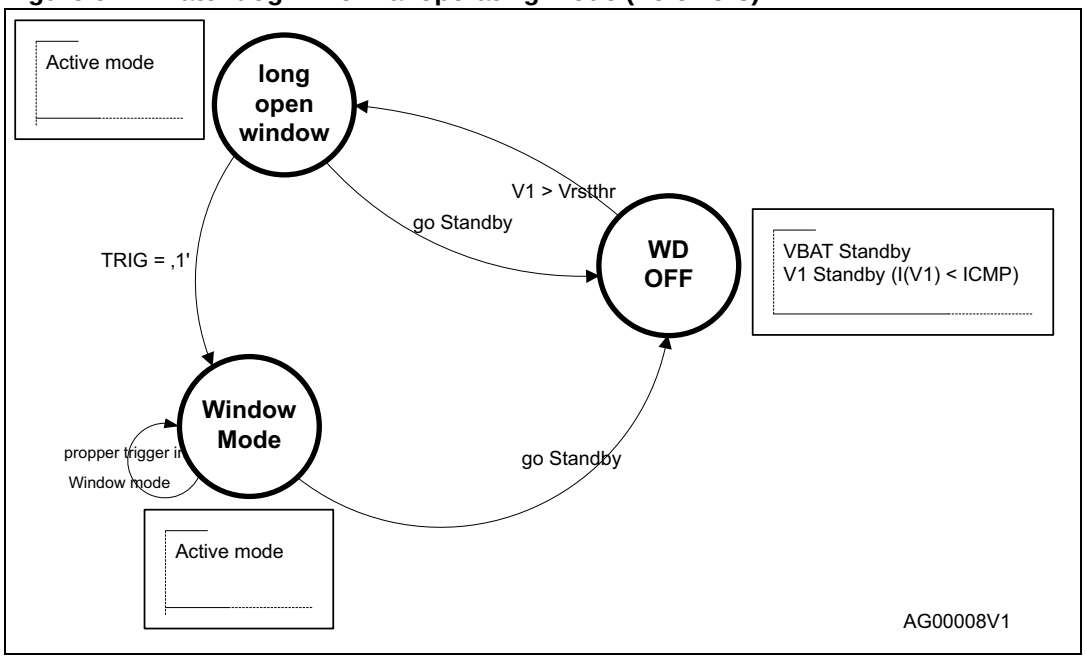


Figure 10. Watchdog with error conditions

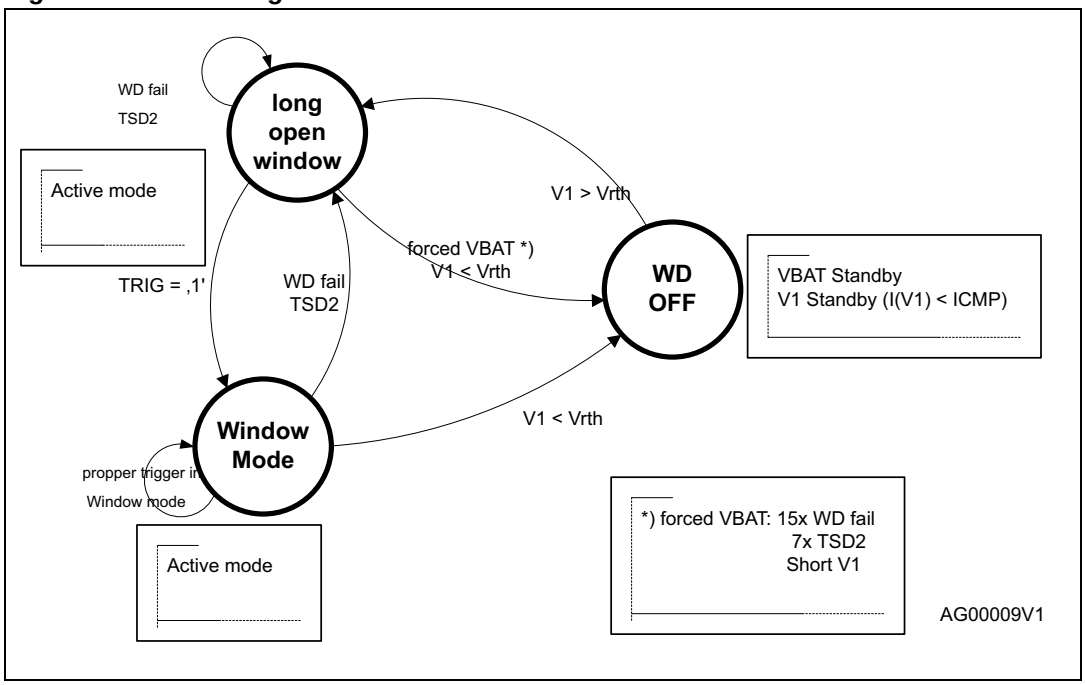
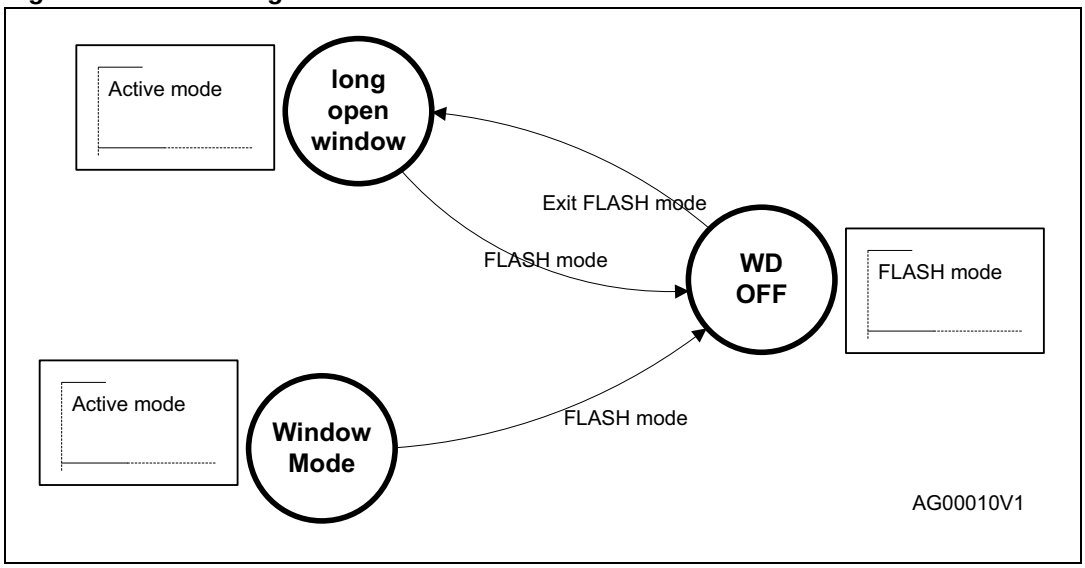


Figure 11. Watchdog in Flash mode



2.4.1 Change watchdog timing

There are 4 programmable watchdog timings available, which represent the nominal trigger time in window mode. To change the watchdog timing, a new timing has to be written by SPI. The new timing gets active with the next valid watchdog trigger. The following figures illustrate the sequence, which is recommended to use, changing the timing within long open window and within window mode.

Figure 12. Change watchdog timing within long open window

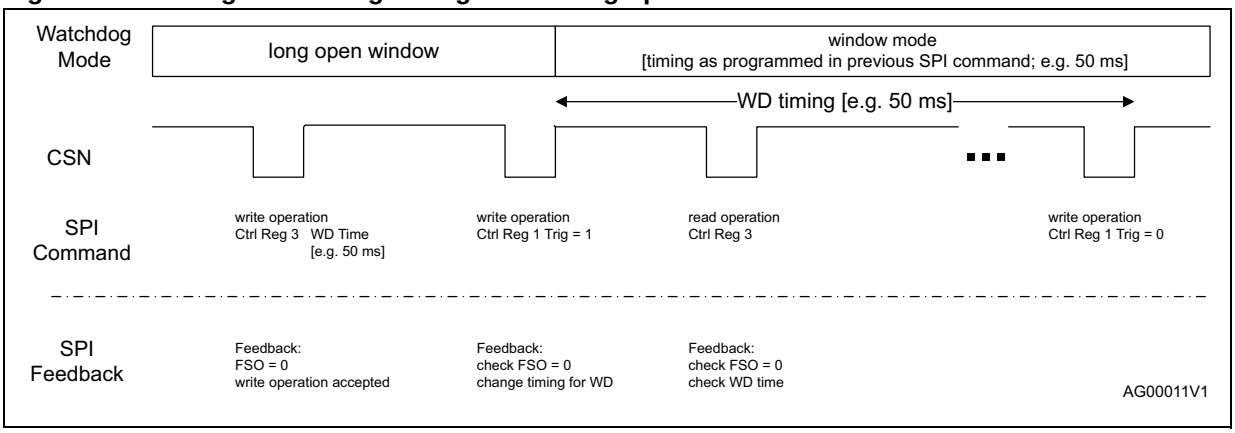
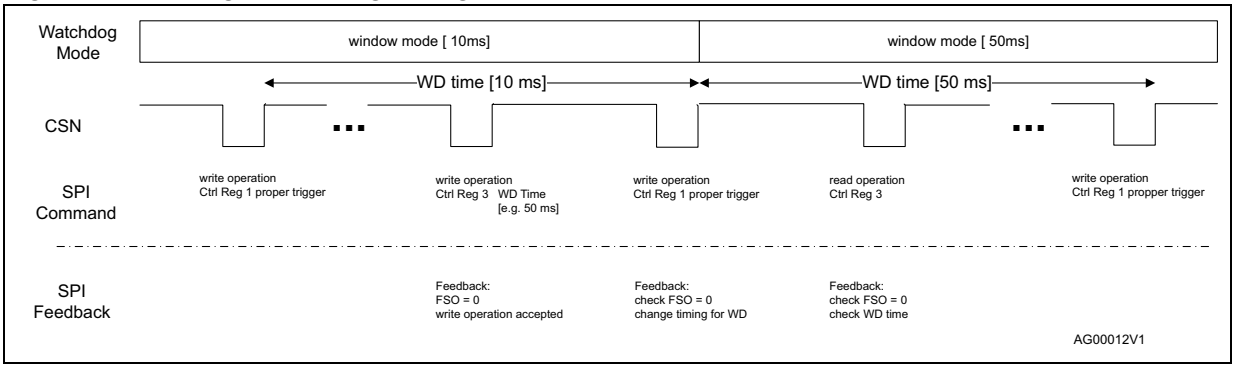


Figure 13. Change watchdog timing within window mode



If the device is in fail-safe mode, the control registers are locked for writing. To change the watchdog timing out of fail-safe mode, first the fail-safe condition must be solved, respective confirmed from the microcontroller. Afterwards the new watchdog timing can be programmed using the sequence from *Figure 14*. Since the actions to remove, a fail-safe condition can differ from the root cause of the fail safe the following diagram shows the general procedure how to change the watchdog timing out of fail-safe mode. *Figure 15* shows the procedure to change watchdog timing with a previous watchdog failure, since this is a special fail-safe scenario.

Figure 14. General procedure to change watchdog timing out of fail safe mode

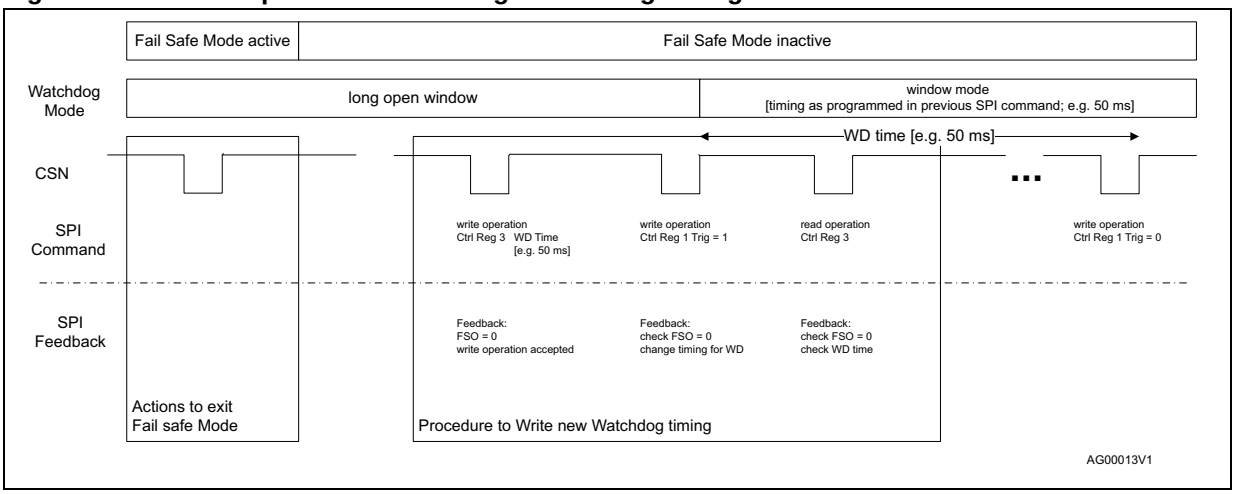
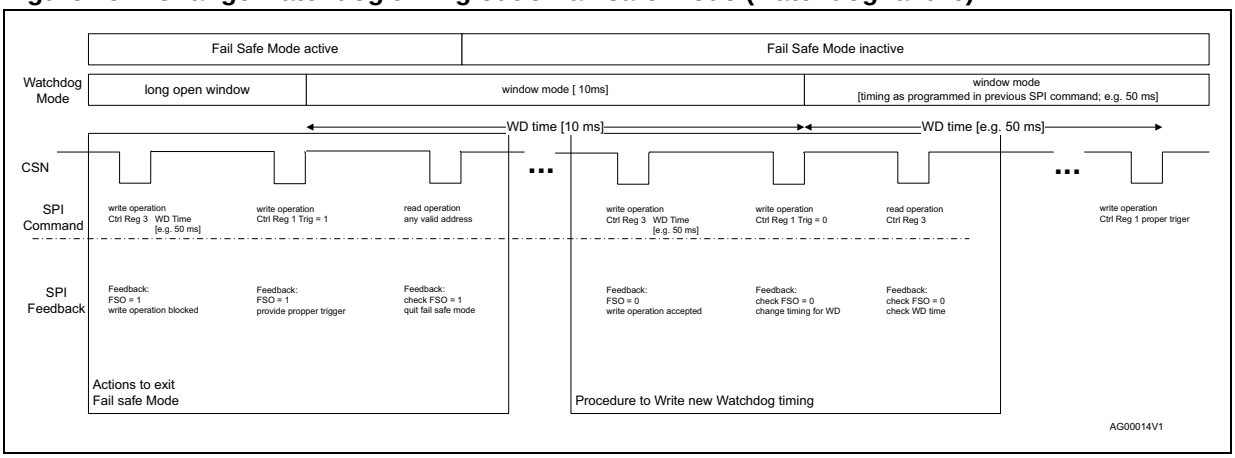


Figure 15. Change watchdog timing out of fail safe mode (watchdog failure)



2.5 Fail safe mode

2.5.1 Single failures

L99PM62XP enters fail safe mode in case of:

- Watchdog failure
- V_1 turn on failure
  - V_1 short ($V_1 < V_{1fail}$ for t > 4 ms)
- V_1 undervoltage ($V_1 <$ Vrth for t > 8 µs)
- Thermal shutdown TSD2
- SPI failure
  - DI stuck to GND or V_{CC} (SPI frame = ’00 00 00’ or ‘FF FF FF’

The fail safe functionality is also available in V_1 standby mode. During V_1 standby mode the fails safe mode is entered in the following cases:

- V_1 undervoltage (V_1 < Vrth for t > 8 µs)
- Watchdog failure (if watchdog still running due to $I_{V1} > I_{cmp}$)
- Thermal shutdown TSD2

In fail safe mode the L99PM62 returns to a default. The fail safe condition is indicated to the remaining system in the global status register. The conditions during fails safe mode are:

- All outputs are turned off
- All control registers are set to default values (except OUT3/FSO configuration)
- Write operations to control registers are blocked until the fail safe condition is cleared (see *Table 5*)
- LIN and HS CAN transmitter, OpAmps and SPI remain on
- Corresponding failure bits in status registers are set.
- FSO Bit (Bit 0 global status register) is set
- OUT3/FSO is activated if configured as fail safe output

If OUT3 is configured as FSO, the internal fail safe mode can be monitored at OUT3 (high-side driver is turned on in fail-safe mode). Self protection features for OUT3 when configured as FSO are active (see *Section 3.3: High-side driver outputs*).

OUT3 is configured as fail safe output by default. It can be configured to normal high-side driver operation by SPI. It this case, the configuration remains until Vs power on.

If the fail safe mode was entered it keeps active until the fail safe condition is removed and the fail safe was read by spi. depending on the root cause of the fail safe operation, the actions to exit fail safe mode are as shown in the following table.

Table 5. Fail safe conditions and exit modes

Failure source	Failure condition	Diagnosis	Exit from fail-safe mode
µC (oscillator)	Watchdog early write failure or expired window	Fail-safe = 1 WDfail = n+1	TRIG = 1 during LOWi and read fail-safe bit
V_1	Short at turn-on	Fail-safe = 1 Forced Sleep TSD2/SHTV_1 = 1	Read&Clear SR3 after wake
	Undervoltage	Fail-safe = 1 V_{1fail} = 1(1)	V_1 > Vrth Read Fail-safe bit
Temperature	T_j > TSD2	Fail-safe = 1 TW = 1 TSD1 = 1 TSD2 = 1	T_j < TSD2 Read&Clear SR3
SPI	DI short to GND or V_{CC}	Fail-safe = 1	Valid SPI command

1. if $V_1 < V_{1fail}$ (for t >2µs)
The fail-safe bit is located in the global status register (Bit 0)
multiple failures – entering forced V_{BAT} standby mode

If the fail-safe condition persists and all attempts to return to normal system operation fail, the L99PM62 enters the *forced* V_{BAT} standby *mode* in order to prevent damage to the

system. The *forced* V_{BAT} standby mode can be terminated by any regular wake-up event. The root cause of the *forced* V_{BAT} standby is indicated in the SPI status registers

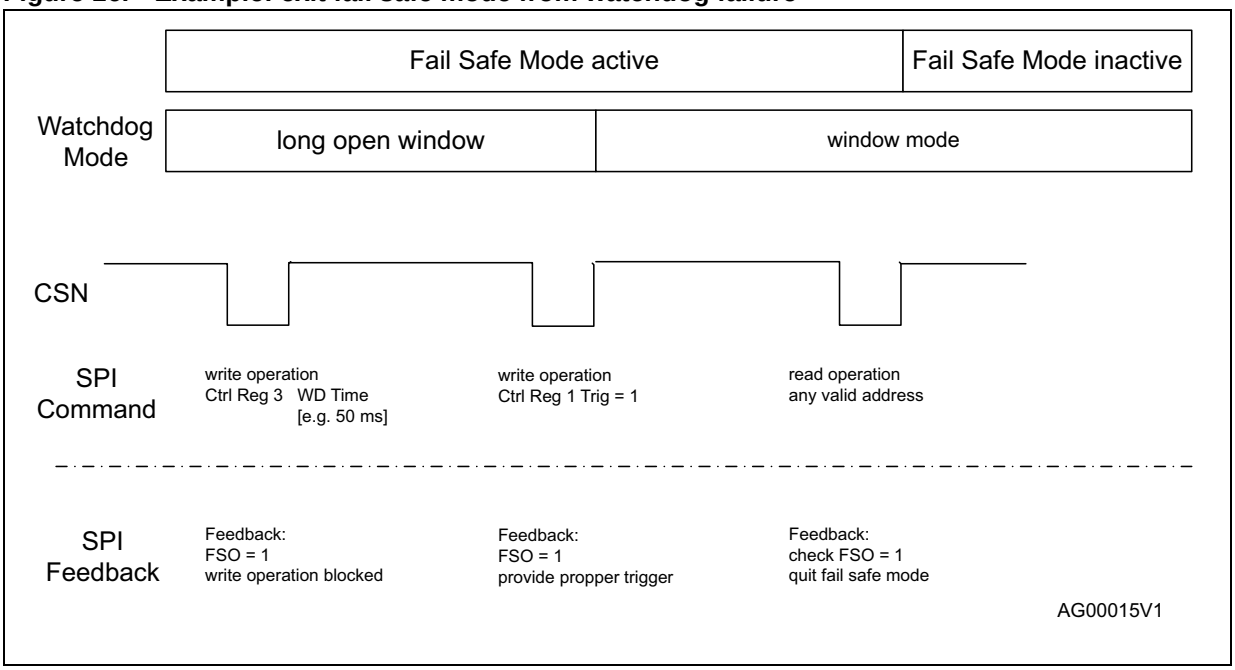
The *forced* V_{BAT} standby *mode* is entered in case of:

- Multiple watchdog failures: forced sleep WD = 1 (15x watchdog failure)
- Multiple thermal shutdown 2: forced sleep TSD2/SHTV1 = 1 (7x TSD2)
- V_1 short at turn-on: forced sleep TSD2/SHTV1 = 1 ($V_1 < V_{1fail}$ for t > 4 ms)

Table 6. Persisting fail safe conditions and exit modes

Failure source	Failure condition	Diagnosis	Exit from fail-safe mode
µC (oscillator)	15 consecutive watchdog failures	Fail-safe = 1 ForcedSleepWD = 1	Wake-up TRIG = 1 during LOWi read & clear SR3
V_1	short at turn-on	Fail-safe = 1 ForcedSleepTSD2/SHTV$_1$ = 1	Read&clear SR3 after wake-up
Temperature	7 times TSD2	Fail-safe = 1 TW = 1 TSD1 = 1 TSD2 = 1 ForcedSleepTSD2/SHTV$_1$ = 1	Read&clear SR3 after wake-up

Figure 16. Example: exit fail safe mode from watchdog failure



2.6 Reset output (NRESET)

If V_1 is turned on and the voltage exceeds the V_1 reset threshold, the reset output "NRESET" is pulled up by internal pull up resistor to V_1 voltage after a 2 ms reset delay time. This is necessary for a defined start of the micro controller when the application is switched on. Since the NRESET output is realized as an open drain output it is also possible to connect an external NRESET open drain NRESET source to the output. It must be considered that as soon the NRESET is released from the L99PM62 the Watchdog timing starts.

A reset pulse (2 ms) is generated in case of:

- V_1 drops below Vrth (configurable by SPI) for more than 8 µs
- Watchdog failure

Note: An external pull-up resistor (1kΩ) to V_1 is recommended in order to ensure $I_{LOAD1} > I_{cmp}$ during reset condition

2.7 Operational amplifiers

The operational amplifiers are especially designed to be used for sensing and amplifying the voltage drop across ground connected shunt resistors. Therefore the input common mode range includes -0.2 V to 3 V.

The operational amplifiers are designed for -0.2 V to +3 V input voltage swing and rail-to-rail output voltage range.

All pins (positive, negative and outputs) are available to be able to operate in non-inverting and inverting mode. Both operational amplifiers are on-chip compensated for stability over the whole operating range within the defined load impedance.

The operational amplifiers may also be used to setup an additional high current voltage source with an external pass element. Refer to *Section 2.1.3* for a detailed description.

2.8 LIN bus interface

Features:

- Speed communication up to 20 kbit/s.
- LIN 2.1 compliant (SAEJ2602 compatible) transceiver.
- Function range from +40 V to -18 V DC at LIN pin.
- GND disconnection fail safe at module level.
- Off mode: does not disturb network.
- GND shift operation at system level.
- Micro controller Interface with CMOS compatible I/O pins.
- Internal pull up resistor.
- Internal high-side switch to disconnect master pull-up resistor in case of short circuit of bus signal.
- ESD and transient immunity according to ISO7637 and EN / IEC61000-4-2.
- Matched output slopes and propagation delay.

In order to further reduce the current consumption in standby mode, the integrated LIN bus interface offers an ultra low current consumption.

Note: Use of master pull-up switch is optional.

2.8.1 Error handling

The L99PM62XP provides the following 3 error handling features which are not described in the LIN Spec. $V_{2.1}$, but are realized in different stand alone LIN transceivers / micro controllers to switch the application back to normal operation mode.

Dominant TxDL time out

If TXDL is in dominant state (low) for more than 12 ms (typ) the transmitter is disabled, the status bit is latched and can be read and optionally cleared by SPI. The transmitter remains disabled until the status register is cleared. This feature can be disabled via SPI.

Permanent recessive

If TXDL changes to dominant (low) state but RXDL signal does not follow within 40 µs the transmitter is disabled, the status bit is latched and can be read and optionally cleared by SPI. The transmitter remains disabled until the status register is cleared.

Permanent dominant

If the bus state is dominant (low) for more than 12 ms a permanent dominant status is detected. The status bit is latched and can be read and optionally cleared by SPI. The transmitter is not disabled.

2.8.2 Wake up (from LIN)

In standby mode the L99PM62XP can receive a wake up from LIN bus. For the wake up feature the L99PM62XP logic differentiates two different conditions.

Normal wake up

Normal wake up can occur when the LIN transceiver was set in standby mode while LIN was in recessive (high) state. A dominant level at LIN for t_{linbus}, switches the L99PM62XP to active mode.

Wake up from short to GND condition

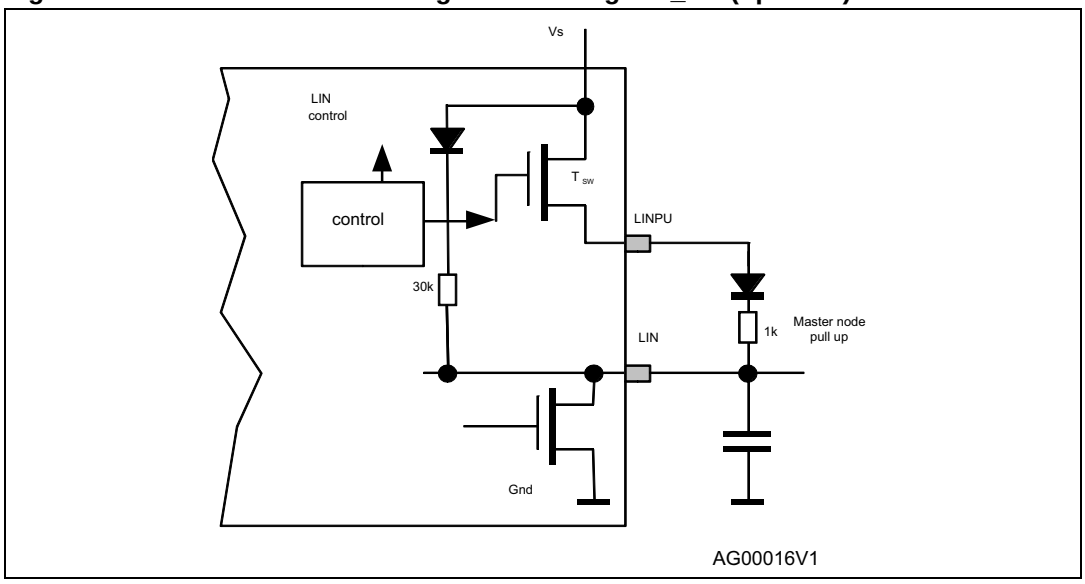
If the LIN transceiver was set in standby mode while LIN was in dominant (low) state, recessive level at LIN for t_{linbus}, switches the L99PM62XP to active mode.

Note: A wake up caused by a message on the bus starts the voltage regulator and the microcontroller to switch the application back to normal operation mode.

2.8.3 LIN pull-up

The master node pull-up resistor (1 kΩ) can be connected to Vs using the internal LIN_PU high-side switch. This high-side switch can be controlled by SPI in order to allow disconnection of the pull-up resistor in case of LIN bus short to GND conditions.

Figure 17. LIN master node configuration using LIN_PU (optional)



LIN_PU high-side driver characteristics:

- Activated by default and can be turned off by SPI command (CR4).
- Remains active in standby modes.
- Switch off only in case of over temperature (TSD2 = thermal shutdown #2).
- No over current protection.
- Typical R_{DS}on, 10 Ω.

2.9 High speed CAN bus transceiver

General requirements

- Speed communication up to 1 Mbit/s.
- ISO 11898-2 and ISO 11898-5 compliant
- SAE J2284 compliant
- Function range from +40 V to -27 V DC at CAN pins.
- GND disconnection fail safe at module level.
- GND shift operation at system level.
- Micro controller Interface with CMOS compatible I/O pins.
- ESD and transient immunity according to ISO7637 and EN / IEC61000-4-2
- Matched output slopes and propagation delay
- Split output pin for stabilizing the recessive bus level
- Receive-only mode available

In order to further reduce the current consumption in standby mode, the integrated CAN bus interface offers an ultra low current consumption.

2.9.1 CAN error handling

The L99PM62XP provides the following 4 error handling features which are not described in the ISO 11898-2/ISO 11898-5, but are realized in different stand alone CAN transceivers / micro controllers to switch the application back to normal operation mode.

Dominant TxDC time out

If TXDC is in dominant state (low) for $t > t_{dom(TxD)}$ the transmitter is disabled, status bit is latched and can be read and optionally cleared by SPI. The transmitter remains disabled until the status register is cleared.

CAN permanent recessive

If TXDC changes to dominant (low) state but CAN bus does not follow for 4 times, the transmitter is disabled, status bit is latched and can be read and optionally cleared by SPI. The transmitter remains disabled until the status register is cleared.

CAN permanent dominant

If the bus state is dominant (low) for $t > t_{CAN}$ a permanent dominant status is detected. The status bit is latched and can be read and optionally cleared by SPI. The transmitter is not disabled.

RXDC permanent recessive

If RXDC pin is clamped to recessive (high) state, the controller is not able to recognize a bus dominant state and could start messages at any time, which results in disturbing the overall bus communication. Therefore, if RXDC does not follow TXDC for 4 times the transmitter is disabled. The status bit is latched and can be read and optionally cleared by SPI. The transmitter remains disabled until the status register is cleared.

2.9.2 Wake up (from CAN)

When the L99PM62XP is in standby mode with CAN wake up option enabled, the CAN bus traffic is detected. For the wake up feature the L99PM62XP logic differentiates different conditions. During V_1 Standby mode RXDC output is kept at recessive level. Independent from the wakeup pattern selected and independent from the previous Standby mode, the RXDC reflect immediately the bus state after the wakeup. This feature allows implementation of a ‘partial networking’ functionality controlled by the system microcontroller.

Normal pattern wake up

Normal pattern wake up can occur when CAN pattern wake up option is enabled and the CAN transceiver was set in standby mode while CAN bus was in recessive (high) state or dominant (low) state. In order to wake up the L99PM62XP, the following criteria must be fulfilled:

- The CAN interface wake-up receiver must receive a series of two consecutive valid dominant pulses, each of which must be longer than 2 µs
- The distance between 2 pulses must be longer than 2 µs.
- The two pulses must occur within a time frame of 1.0 ms

Wake up from short to GND condition

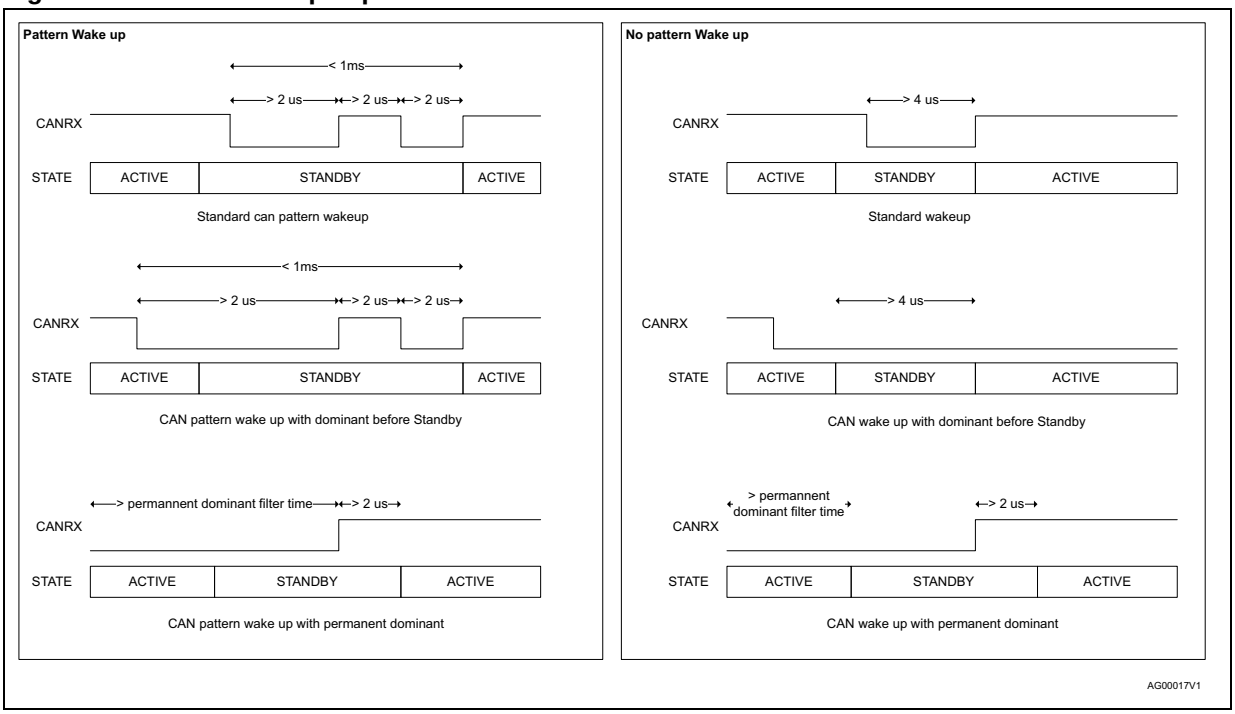
Even if CAN pattern wake up option is enabled, but the CAN transceiver was set in standby mode after a qualified permanent dominant state, recessive level at CAN, switches the L99PM62XP to active mode.

No pattern wake up

If the CAN pattern wake up option is disabled, any transition either dominant (low) state to recessive (high) state or recessive (high) state to dominant (low) state switches the L99PM62XP to active mode (after a filtering time of 2 µs).

Note: A wake up caused by a message on the bus starts the voltage regulator and the microcontroller to switch the application back to normal operation mode.

Figure 18. CAN wake up capabilities



Note: Pictures above illustrate the wake up behaviour from V_1 standby mode. For wake up from V_{BAT} standby mode the NRESET signal (with 2 ms timing) is generated instead of the RXDL (Interrupt) signal.

2.9.3 CAN sleep mode

During active mode it is possible to deactivate the CAN transceiver with a dedicated SPI command (CR4, CAN_act = 0). The CAN transceiver remains deactivated until it is activated again. With a deactivated CAN the receiver input termination network is disconnected from the bus and the CANH, CANL bus lines is driven to GND. The SPLIT output is also deactivated in this case.

2.9.4 CAN receive only mode

With the CAN_rec_only bit in control register 4 it is possible to disable the CAN transmitter in active mode. In this mode it is possible to listen to the bus but not sending to it. The receiver termination network is still activated in this mode.

2.9.5 CAN looping mode

If the CAN_Loop_en bit in control register 4 is set the TXDC input is mapped directly to the RXDC pin. This mode can be used in combination with the CAN receive only mode, to run diagnosis for the CAN protocol handler of the micro controller.

2.10 Serial peripheral interface (ST SPI standard)

A 24 bit SPI is used for bi-directional communication with the micro controller.

During active mode, the SPI

- Triggers the watchdog
- Controls the modes and status of all L99PM62XP modules (incl. input and output drivers)
- Provides driver output diagnostic
- Provide L99PM62XP diagnostic (incl. over temperature warning, L99PM62XP operation status)

The SPI can be driven by a micro controller with its SPI peripheral running in following mode:

CPOL = 0 and CPHA = 0.

For this mode input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

This device is not limited to micro controller with a built-in SPI. Only three CMOS-compatible output pins and one input pin is needed to communicate with the device. A fault condition can be detected by setting CSN to low. If CSN = 0, the DO-pin reflects the global error flag (fault condition) of the device.

Chip select not (CSN)

The input pin is used to select the serial interface of this device. When CSN is high, the output pin (DO) is in high impedance state. A low signal activates the output driver and a serial communication can be started. The state during CSN = 0 is called a communication frame.

If CSN = low for $t > t_{CSNfail}$ the DO output is switched to high impedance in order to not block the signal line for other SPI nodes.

Serial data in (DI)

The input pin is used to transfer data serial into the device. The data applied to the DI is sampled at the rising edge of the CLK signal and shifted into an internal 24 bit shift register. At the rising edge of the CSN signal the contents of the shift register is transferred to Data Input Register. The writing to the selected data input register is only enabled if exactly 24 bits are transmitted within one communication frame (i.e. CSN low). If more or less clock

pulses are counted within one frame the complete frame is ignored. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame.

Note: Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected IC's is recommended.

Serial data out (DO)

The data output driver is activated by a logical low level at the CSN input and goes from high impedance to a low or high level depending on the global error flag (fault condition). The first rising edge of the CLK input after a high to low transition of the CSN pin transfers the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK shifts the next bit out.

Serial clock (CLK)

The CLK input is used to synchronize the input and output serial bit streams. The data input (DI) is sampled at the rising edge of the CLK and the data output (DO) changes with the falling edge of the CLK signal. The SPI can be driven with a CLK Frequency up to 1MHz.

3 Protection and diagnosis

3.1 Power supply fail

Over and under-voltage detection on Vs

3.1.1 Vs overvoltage

If the supply voltage Vs reaches the over voltage threshold (V_{SOV}):

- Outputs OUTx, RELx and LIN are switched to high impedance state (load protection). CAN is not disabled. Recovery of outputs when the overvoltage condition disappears is depending on the setting of VLOCKOUT_EN bit in Control Register 4.
  - VLOCKOUT_EN = 1: Outputs are off until read and clear SR3.
  - VLOCKOUT_EN = 0: Outputs switch automatically on when overvoltage condition disappears.
- The over voltage bit is set and can be cleared with a ‘Read and Clear’ command. The overvoltage bit is removed automatically if VLOCKOUT_EN = 0 and the overvoltage condition disappears.
- Outputs REL1,2 can be excluded from a shutdown in case of overvoltage by SPI (LSOVUV_ Shutdown_en in CR4)

3.1.2 Vs undervoltage

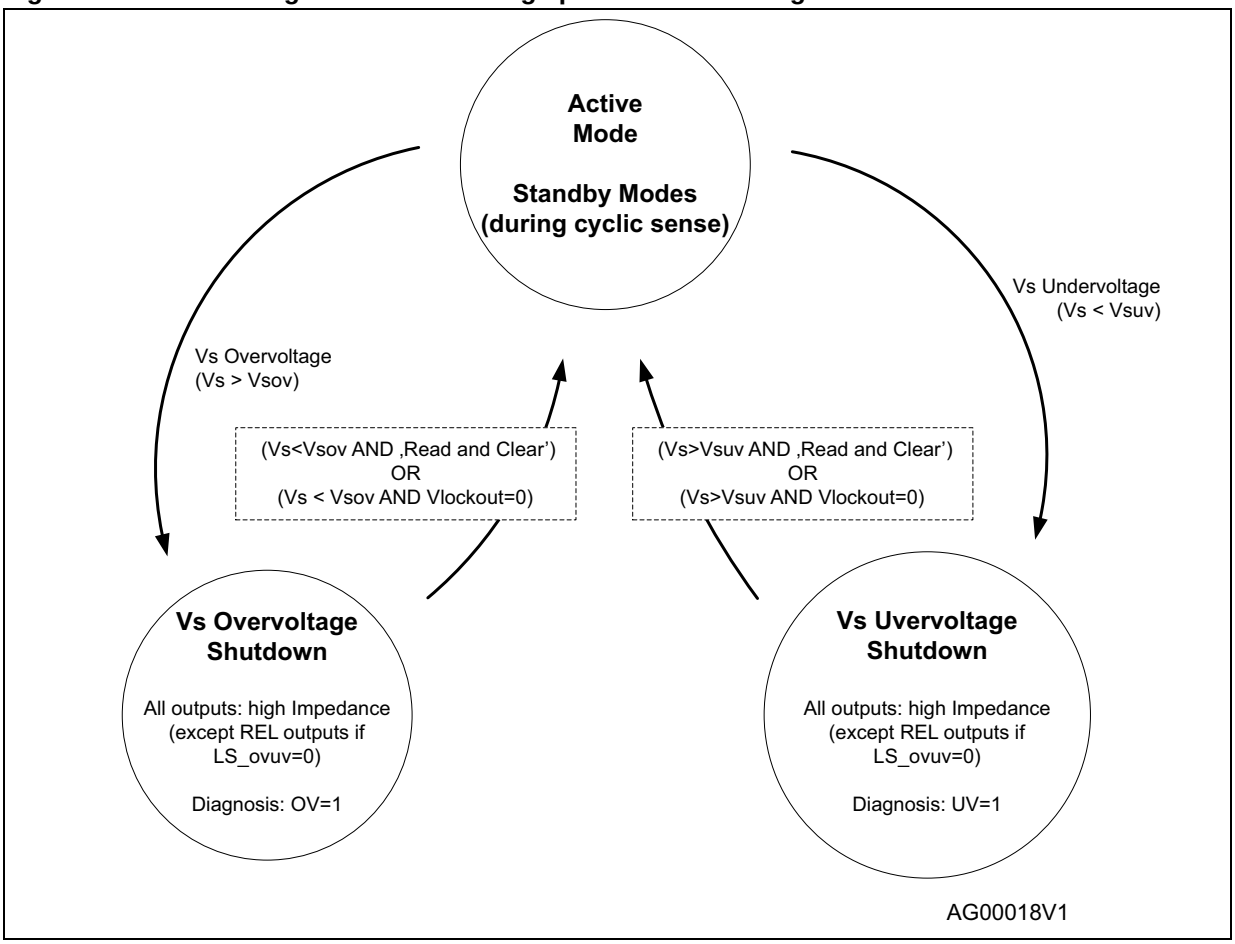
If the supply voltage Vs drops below the under voltage threshold voltage (V_{SUV})

- Outputs OUTx, RELx and LIN are switched to high impedance state (load protection). CAN is not disabled. Recovery of outputs when the undervoltage condition disappears is depending on the setting of VLOCKOUT_EN bit.

  VLOCKOUT_EN = 1: Outputs are off until read and clear SR3.

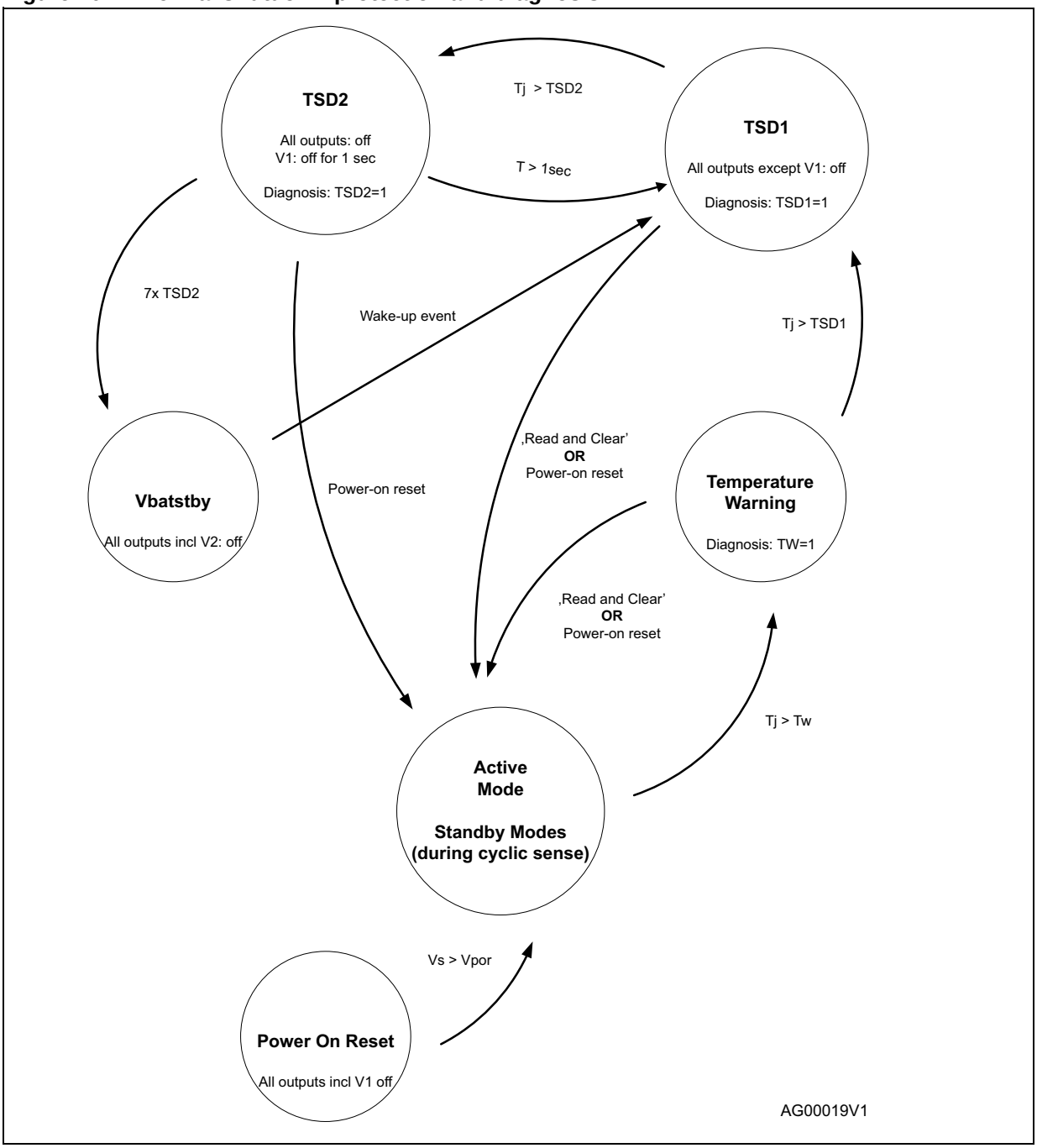
  VLOCKOUT_EN = 0: Outputs switch on automatically when undervoltage condition disappears.
- The undervoltage bit is set and can be cleared with a ‘Read and Clear’ command. The undervoltage bit is removed automatically if VLOCKOUT_EN = 0 and the undervoltage condition disappears
- Outputs REL1,2 can be excluded from a shutdown in case of undervoltage by SPI (LSOVUV_shutdown_en in CR4)

Figure 19. Over voltage and under voltage protection and diagnosis



3.2 Temperature warning and thermal shutdown

Figure 20. Thermal shutdown protection and diagnosis



Note: The thermal state machine recovers the same state were it was before entering standby mode. In case of a TSD2 it enters TSD1 state.

3.3 High-side driver outputs

The component provides a total of 4 high-side outputs Out1 to 4, (7 Ω typ. at @ 25°C) to drive e.g. LED's or hall sensors and 1 high-side output OUT_HS with 1 Ω typ. at @ 25 °C).

The high-side outputs switch off in case of:

- Vs over and undervoltage
- Over current
- Overtemperature with pre warning[(a)]

In case of overload or over temperature (TSD1) condition, the drivers switchs off. The according status bit is latched and can be read and optionally cleared by SPI. The drivers remain off until the status is cleared.

In case over/under voltage condition, the drivers is switched off. The according status bit is latched and can be read and optionally cleared by SPI. If the Vlockout bit (Control Register 4) is set to '1' the drivers remain off until the status is cleared. If the Vlockout bit is set to '0' the drivers switches on automatically if the error condition disappears.

In case of open-load condition, the according status register is latched. The status can be read and optionally cleared by SPI. The high-sides not switches off.

For OUT_HS the auto recovery feature (OUTHSREC bit Control Register 4) can be enabled. If this bit is set to '1' the driver is automatically restart from a overload condition. This overload recovery feature is intended for loads which have an initial current higher than the over current limit of the output (e.g. Inrush current of cold light bulbs). During auto recovery mode the over current status bit can not be read from SPI.

The device itself can not distinguish between a real overload and a non linear load like a light bulb. A real overload condition can only be qualified by time. As an example, the micro controller can switch on light bulbs by setting the over current recovery bit for the first 50ms. After clearing the recovery bit, the output is automatically disabled if the overload condition still exists.

In case of a fail safe condition, the high-side drivers are switched off. The control bits are set to default values. (except OUT3/FSO if it is used as a high-side driver output)

Note: The maximum voltage and current applied to the high-side outputs is specified in Section 2.1: Voltage regulators. Appropriate external protection may be required in order to respect these limits under application conditions.

3.4 Low-side driver outputs REL1, REL2

The outputs REL1, REL2 (R_{DSon} = 2 Ω typ. @25 °C) are specially designed to drive relay loads.

The outputs provide an active output zener clamping (45 V typ.) feature for the demagnetization of the relay coil, even though a load dump condition exists.

For fail-safe reasons the relay drivers are linked with the fail safe operation: in case of entering the fail safe mode, the relay drivers switchs off and the SPI control bits are set to default (i.e. driver is off).

a. Except OUT3 when configured as FSO.

The low-side drivers switch off in case of:

- Vs over and undervoltage
- Over current
- Overtemperature with pre warning

In case of overload or overtemperature (TSD1) condition, the drivers switches off. The according status bit is latched and can be read and optionally cleared by SPI. The drivers remain off until the status is cleared.

In case Vs over/undervoltage condition, the drivers is switched off. The according status bit is latched and can be read and optionally cleared by SPI. If the Vlockout bit (Control Register 4) is set to ‘1’ the drivers remain off until the status is cleared. If the Vlockout bit is set to ‘0’ the drivers is switched on automatically if the error condition disappears.

With the LSOVUV_shutdown_en bit (Control Register 4) the drivers can be excluded from a switch off in case of Vs over/undervoltage. If the bit is set to ‘1’ the driver switchs off, otherwise the drivers remain on.

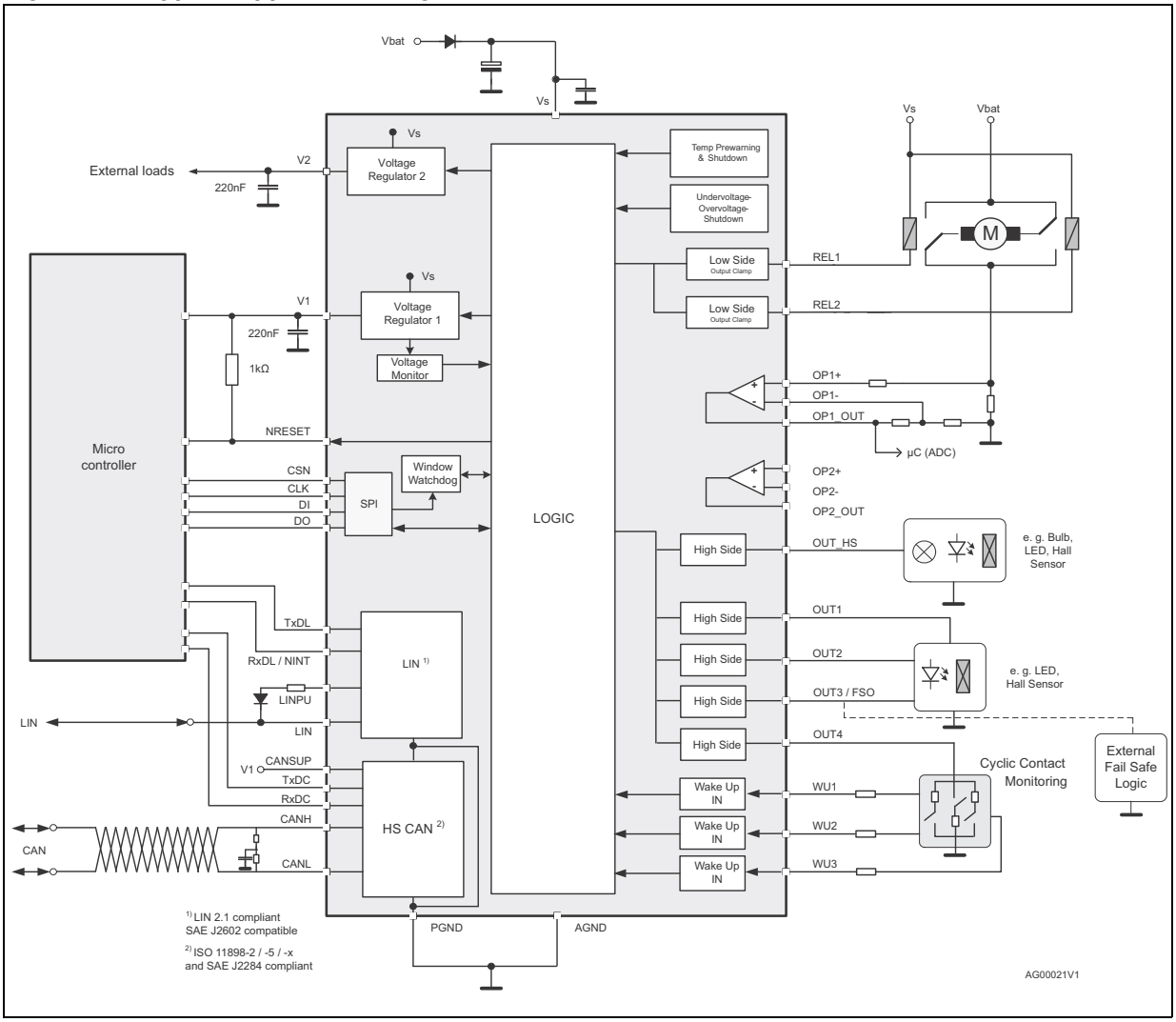
3.5 SPI diagnosis

Digital diagnosis features are provided by SPI (for details please refer to *Section 6.2: SPI registers* .

- V_1 reset threshold programmable
- Overtemperature including. pre warning
- Open-load separately for each output stage except REL1/REL2
- Overload status separately for each output stage
- Vs-supply over/under voltage
- V_1 and V_2 fail bit
- V_2 output short to GND
- Status of the WU1 to 3
- Wake-up sources (CAN, LIN, SPI, Timer, WU1…3)
- chip reset bit (start from power-on reset)
- Number of unsuccessful V_1 restarts after thermal shutdown
- Number of sequential watchdog failures
- LIN diagnosis (permanent recessive/dominant, dominant TxD)
- CAN diagnosis (permanent recessive/dominant, dominant TxD, recessive RXD)
- Device State (wake-up from V1 standby or V_{BAT} standby)
- Forced V_{BAT} standby after WD-fail, forced V_{BAT} standby after overtemperature
- Watchdog timer state (diagnosis of watchdog)
- Fail-safe status
- SPI communication error

4 Typical application

Figure 21. Typical application diagram



5 Electrical specifications

5.1 Absolute maximum rating

Table 7. Absolute maximum rating

Symbol	Parameter/test condition	Value [DC voltage]	Unit
V_S	DC supply voltage / "jump start"	-0.3 to +28	V
	Single pulse / t_{max} < 400 ms "transient load dump"	-0.3 to +40	V
V_1	Stabilized supply voltage, logic supply	-0.3 to +5.25	V
V_2	Stabilized supply voltage	-0.3 to +28	V
V_{DI} V_{CLK} V_{DO} V_{RXDL} V_{NRESET} V_{RXDC}	Logic input / output voltage range	-0.3 to V_1+0.3	V
V_{TXDC}, V_{TXDL}, V_{CSN}	Multi level inputs	-0.3 to Vs+0.3	V
V_{REL1}, V_{REL2},	Low-side output voltage range	-0.3 to +40	V
$V_{OUT1..3}$, V_{OUT_HS}	High-side output voltage range	-0.3 to V_S+0.3	V
$V_{WU1...4}$	Wake up input voltage range	-0.3 to V_S+0.3	V
V_{OP1P},V_{OP1M}, V_{OP2P}, V_{OP2M},	Opamp1 input voltage range Opamp2 input voltage range	-0.3 to V_1+0.3	V
V_{OPOUT1}, V_{OPOUT2}	Analog Output voltage range	-0.3 to V_S+0.3	V
V_{LIN}, V_{LINPU}	LIN bus I/O voltage range	-20 to +40	V
I_{Input}	Current injection into Vs related input pins	10	mA
Iout_inj	Current injection into Vs related outputs	10	mA
V_{CANSUP}	CAN supply	-0.3 to +5.25	V
V_{CANH}, V_{CANL}, V_{SPLIT}	CAN bus I/O voltage range	-27 to +40	V

Note: All maximum ratings are absolute ratings. Leaving the limitation of any of these values may cause an irreversible damage of the integrated circuit!

Loss of ground or ground shift with externally grounded loads: ESD structures are configured for nominal currents only. If external loads are connected to different grounds, the current load must be limited to this nominal current.

5.2 ESD protection

Table 8. ESD protection

Parameter	Value	Unit
All pins(1)	+/-2	kV
All output pins(2)	+/-4	kV
LIN	+/-8(2) +/-6(3)	kV
CAN_H, CAN_L	+/-8(2) +/-6(3)	kV
All pins (charge device model)	+/-500	V
Corner pins (charge device model)	+/-750	V
All pins(4)	+/-200	V

1. HBM (human body model, 100pF, 1.5 kΩ) according to MIL 883C, method 3015.7 or EIA/JESD22A114-A
2. HBM with all none zapped pins grounded.
3. EN / IEC61000-4-2 according to report from external test house.
4. Acc. machine model: C = 200 pF; R = 0 Ω.

5.3 Thermal data

Table 9. Operating junction temperature

Symbol	Parameter	Value	Unit
T_j	Operating junction temperature	-40 to 150	°C
R_{thjA}	Thermal resistance junction / ambient	See *Figure 23*	°K/W

Table 10. Temperature warning and thermal shutdown

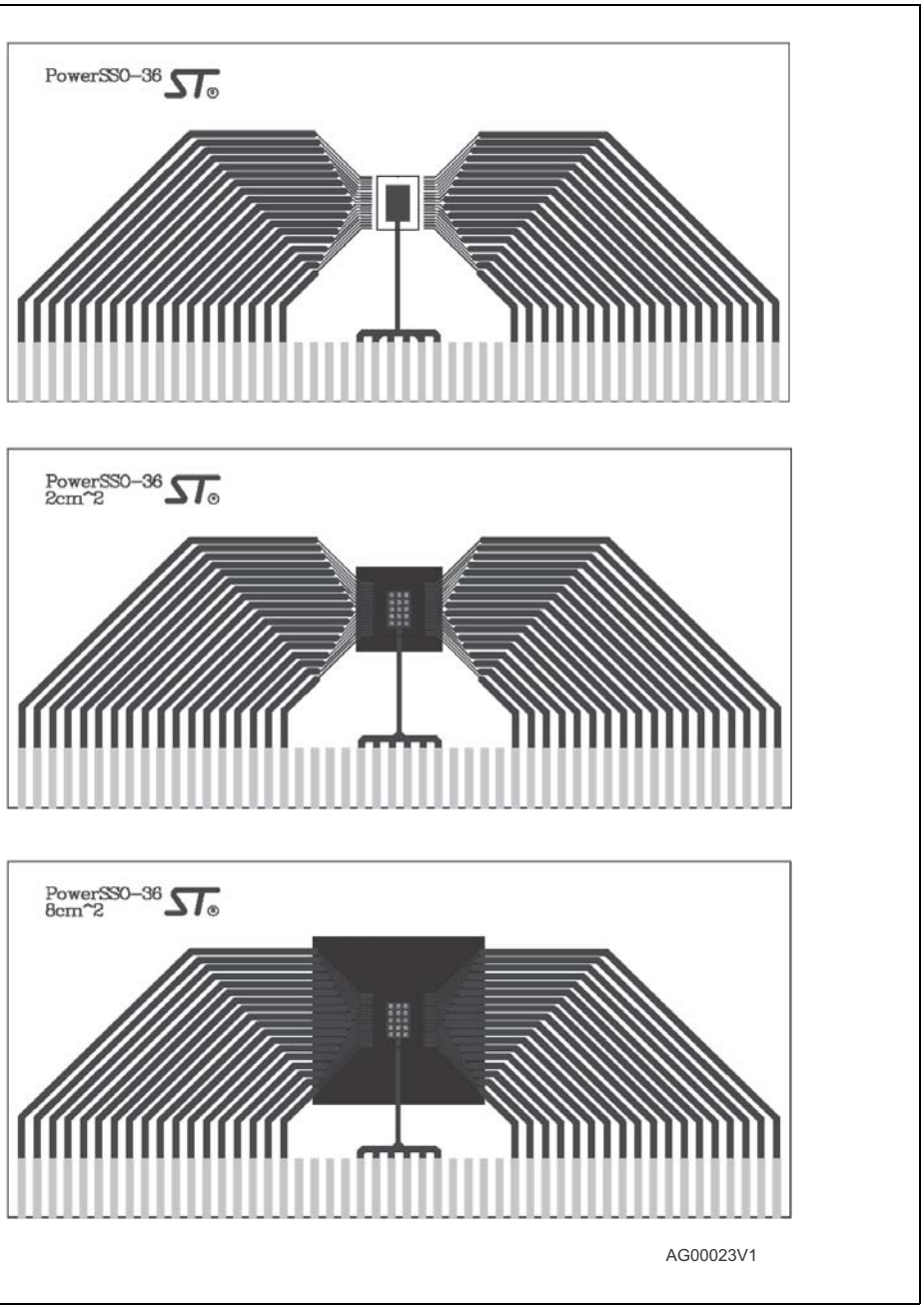
Symbol	Parameter		Min.	Typ.	Max.	Unit
$T_{W\ ON}$	Thermal over temperature warning threshold	T_j(1)	120	130	140	°C
$T_{SD1\ OFF}$	Thermal shutdown junction temperature 1	T_j(1)	130	140	150	°C
$T_{SD2\ OFF}$	Thermal shutdown junction temperature 2	T_j(1)	140	155	170	°C
$T_{SD2\ ON}$		Hysteresis		5		°C
$T_{SD12hys}$						

1. Non-overlapping

5.4 Package and PCB thermal data

5.4.1 PowerSSO-36 thermal data

Figure 22. PowerSSO-36 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (board finish thickness 1.6 mm +/- 10% board double layer, board dimension 129x60, board Material FR4, Cu thickness 0.070 mm (front and back side), thermal vias separation 1.2 mm, thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm).

Figure 23. PowerSSO-36 thermal resistance junction to ambient vs PCB copper area (V1 ON)

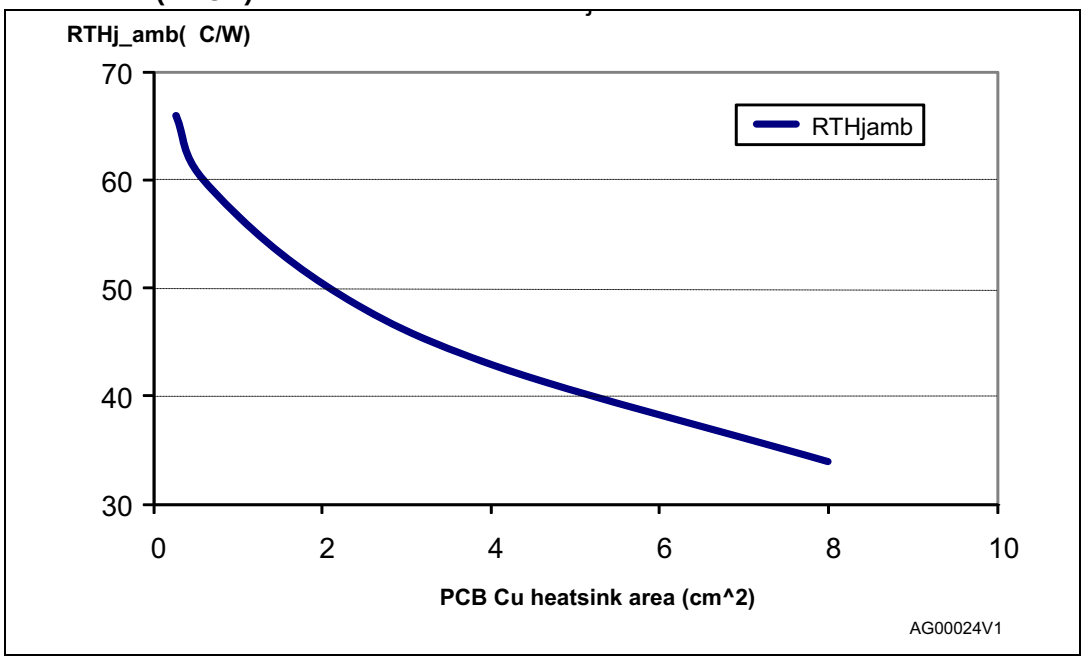


Figure 24. PowerSSO-36 Thermal Impedance junction to ambient vs PCB copper area (single pulse with V1 ON)

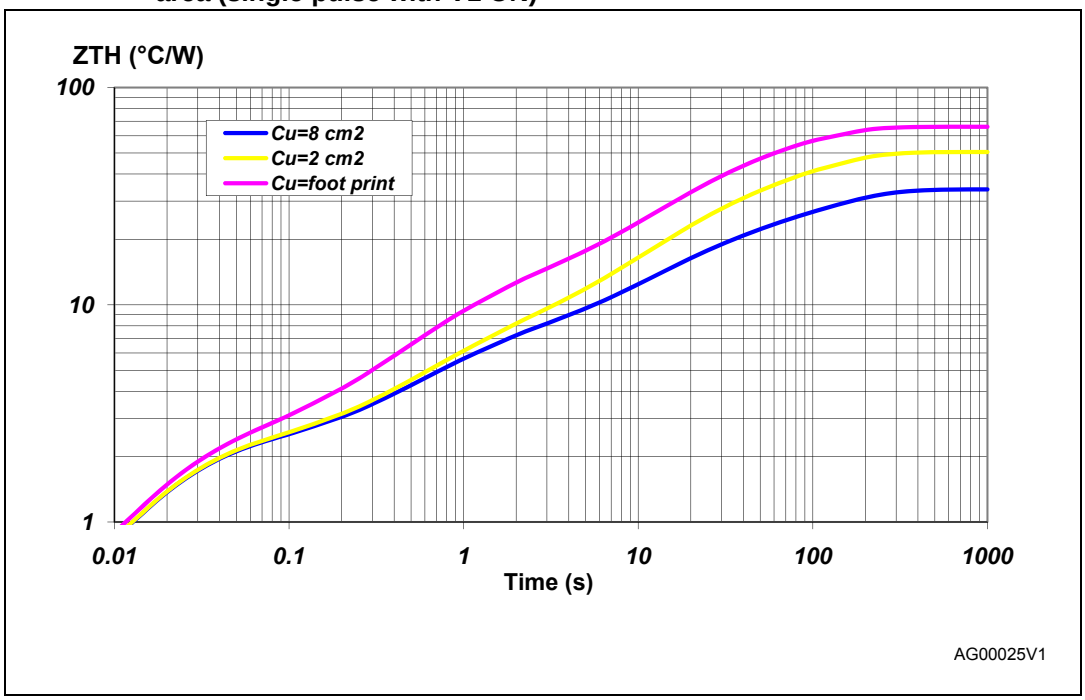
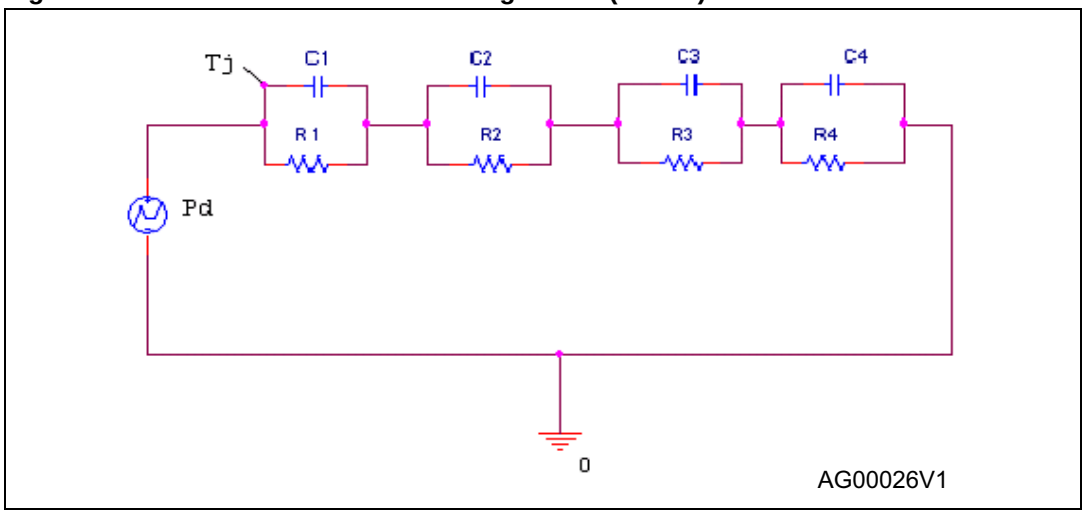


Figure 25. PowerSSO-36 thermal fitting model (V1 ON)



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1-\delta)$$

where $\delta = t_p / T$

Table 11. Thermal parameter

Area/island (cm^2)	Footprint	2	8
R1 (°C/W)	2		
R2 (°C/W)	8	4	4
R3 (°C/W)	20	15.5	10
R4 (°C/W)	36	29	18
C1 (W.s/°C)	0.01		
C2 (W.s/°C)	0.1	0.2	0.2
C3 (W.s/°C)	0.8	1	1.5
C4 (W.s/°C)	2	3	6

5.5 Electrical characteristics

5.5.1 Supply and supply monitoring

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin T_j = -40 °C to 130 °C, unless otherwise specified.

Table 12. Supply and supply monitoring

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_S	Supply voltage range		6	13.5	18	V
V_{SUV}	V_S undervoltage threshold	V_S increasing / decreasing	5.11		5.81	V
V_{hyst_UV}	Vs undervoltage hysteresis		0.0	0.1	0.15	V
V_{SOV}	V_S overvoltage threshold	V_S increasing / decreasing	18.5		22	V
V_{hyst_OV}	Vs overvoltage hysteresis	Hysteresis	0.5	1	1.5	V
t_{ovuv_filt}	Vs over/undervoltage filter time			64*T_{osc}		
$I_{V(act)}$	Current consumption in active mode	Vs = 12V TxD CAN = high TxD LIN = high V_1 = on, V_2 = on		6	12	mA
$I_{V(BAT)}$	Current consumption in V_{BAT} standby mode	V_S = 12V Both voltage regulators deactivated, no wake-up request(1)	8	12	28	µA
$I_{V(BAT)CS}$	Current consumption in V_{BAT} standby mode with cyclic sense enabled	V_S = 12V Both voltage regulators deactivated, T = 50 ms, ton = 100 µs no wake-up request(1)	40	75	125	µA
$I_{V(BAT)CW}$	Current consumption in V_{BAT} standby mode with cyclic wake enabled	V_S = 12V Both voltage regulators deactivated During standby phase no wake-up request(1)	40	75	125	µA
$I_{(V1)}$	Current consumption in V_1-standby mode	V_S = 12V Voltage Regulator V_1 active, (I_{v1} < I_{cmp}) no wake-up request(1)	16	51	76	µA

1. Conditions for no wake-up request are (all conditions must be met):
   2 V < LIN < (Vs-2 V)
   0.4 V < (CAN_H – CAN_L) < 1,2 V
   1 V < V_{WUth} < (Vs-2 V)
   The current consumption in standby modes with cyclic sense can be calculated using the following formulas:
   $I_{V(BAT)CS} = I_{V(BAT)}$ + 55 µA + (2 mA * (t_{ON} + 100 µs) / T)
   $I_{(V1)CS} = I_{V1}$ + 55 µA + (2 mA * (t_{ON} + 100 µs) / T)

5.5.2 Oscillator

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 4.5 V ≤ V_S ≤ 28 V; all outputs open; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 13. Oscillator

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
F_{CLK}	Oscillation frequency		0.80	1.0	1.35	MHz

5.5.3 Power-on reset (V_S)

All outputs open; T_j = -40°C to 130°C, unless otherwise specified.

Table 14. Power-on reset (V_S)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{POR}	V_{POR} threshold	Vs increasing		3.45	4.5	V
V_{POR}	V_{POR} threshold	Vs decreasing(1)	2.65		3.5	V

1. This threshold is valid if Vs had already reached 7V previously

5.5.4 Voltage regulator V_1

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 4.5 V ≤ V_S ≤ 28 V; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 15. Voltage regulator V_1

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_1	Output voltage			5.0		V
V_1	Output voltage tolerance Active mode	I_{LOAD1} = 1mA to 100 mA, V_S = 13.5 V			+/- 2	%
$V_{hc}1$	Output voltage tolerance active mode, high current	I_{LOAD1} = 100 mA to 250 mA, V_S = 13.5 V			+/- 3	%
		I_{LOAD1} = 250 mA V_S = 13.5 V			+/- 5%	%
$V_{STB}1$	Output voltage tolerance V_1-standby mode	I_{LOAD1} = 0 µA to 1 mA, V_S = 13.5 V			+/- 4%	%
$V_{DP}1$	Drop-out Voltage	I_{LOAD1} = 50 mA, V_S = 5 V I_{LOAD1} = 100 mA, V = 4.5 V I_{LOAD1} = 100 mA, V_S = 5 V I_{LOAD1} = 150 mA, V_S = 4.5 V I_{LOAD1} = 150 mA, V_S = 5.0 V		0.2 0.2 0.3 0.45 0.45	0.4 0.5 0.5 0.6 0.6	V V V V V
$I_{CC}1$	Output current in active mode	Max. continuous load current			250	mA
I_{CC}max1	Short circuit output current	Current limitation	400	600	950	mA
C_{load1}	Load capacitor1	Ceramic (+/- 20%)	0.22(1)			µF

Table 15. Voltage regulator V_1 (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{TSD}	V_1 deactivation time after thermal shutdown			1		sec
I_{cmp_ris}	Current comp. rising thresh.	Rising current	1.2	2.5	4	mA
I_{cmp_fal}	Current comp. falling threshold	Falling current	0.8	1.95	2.8	mA
I_{cmp_hys}	Current comp. hysteresis			0.5		mA
V_{1fail}	V_1 fail threshold	V_1 forced		2		V
tV_{1fail}	V_1 fail filter time			2		µs
tV_{1short}	V_1 short filter time			4		ms

1. Nominal capacitor value required for stability of the regulator. Tested with 220 nF ceramic (+/- 20 %). Capacitor must be located close to the regulator output pin.

5.5.5 Voltage regulator V_2

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 4.5 V ≤ V_S ≤ 28 V; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 16. Voltage regulator V_2

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_2	Output voltage			5,0		V
V_2	Output voltage tolerance active mode	I_{LOAD2} = 1 mA to 50 mA, V_S = 13.5 V			+/- 3	%
V_{hc1}	Output voltage tolerance active mode	I_{LOAD2} = 50 mA to 80 mA, V_S = 13,5 V			+/- 4	%
V_2	Output voltage tolerance active mode, high current	I_{LOAD2} = 100 mA, V_S = 13,5 V			+/- 6	%
V_{STB2}	Output voltage tolerance V_1 standby mode	I_{LOAD2} = 0 µA to 1 mA V_S = 13,5 V			+/-6	%
V_{DP2}	Drop-out voltage	I_{LOAD2} = 25 mA, Vs = 5.25 V I_{LOAD2} = 50 mA, Vs = 5.25 V		0.3 0.4	0.4 0.7	V V
I_{CC2}	Output current in active mode	Max. continuous load current			100	mA
I_{CCmax2}	Short circuit output current	Current limitation	200	300	500	mA
C_{load}	Load capacitor	Ceramic (+/- 20 %)	0.22(1)			µF
V_{2fail}	V_2 fail threshold	V_2 forced			2	V
t_{V2fail}	V_2 fail filter time			2		µs
$t_{V2short}$	V_2 short filter time			4		ms

1. Nominal capacitor value required for stability of the regulator. Tested with 220 nF ceramic (+/- 20 %). Capacitor must be located close to the regulator output pin.

5.5.6 Reset output

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin. 4.0 V < V_S = 28 V; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 17. Reset output

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{RT1}	Reset threshold voltage1	V_1 decreasing	3.7	3.9	4.1	V
V_{RT2}	Reset threshold voltage2	V_1 decreasing	4.2	4.3	4.45	V
V_{RT3}	Reset threshold voltage3	V_1 decreasing	4.25	4.4	4.55	V
V_{RT4}	Reset threshold voltage4	$_{V1}$ decreasing	4.5	4.60	4.75	V
VRT4	Reset threshold voltage4	V_1 increasing	4.7	4.8	4.9	V
V_{RESET}	Reset pin low output voltage	V_1 > 1V, I_{RESET} = 5 mA		0,2	0,4	V
R_{RESET}	Reset pull up int. resistor		80	110	150	kΩ
t_{RR}	Reset reaction time	I_{LOAD1} = 1 mA	6		40	µs
t_{UV1}	V_1 under-voltage filter time			16		µs
Trd	Reset pulse duration		1.5	2	2.5	ms

5.5.7 Watchdog

4.5 V < V_S < 28 V; 4.8 V < V_1 < 5.2 V; T_j = -40 °C to 130 °C, unless otherwise specified, see *Figure 26* and *Figure 27*.

Table 18. Watchdog

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{LW}	Long open window	TBD	48,75	65	81,25	ms
T_{EFW1}	Early failure window 1				4.5	ms
T_{LFW1}	Late failure window 1		20			ms
T_{SW1}	Safe window 1		7.5		12	ms
T_{EFW2}	Early failure window 2				22.5	ms
T_{LFW2}	Late failure window 2		100			ms
T_{SW2}	Safe window 2		37.5		60	ms
T_{EFW3}	Early failure window 3				45	ms
T_{LFW3}	Late failure window 3		200			ms
T_{SW3}	Safe window 3		75		120	ms
T_{EFW4}	Early failure window 4				90	ms
T_{LFW4}	Late failure window 4		400			ms
T_{SW4}	Safe window 4		150		240	ms

Figure 26. Watchdog timing (long, early, late and safe window)

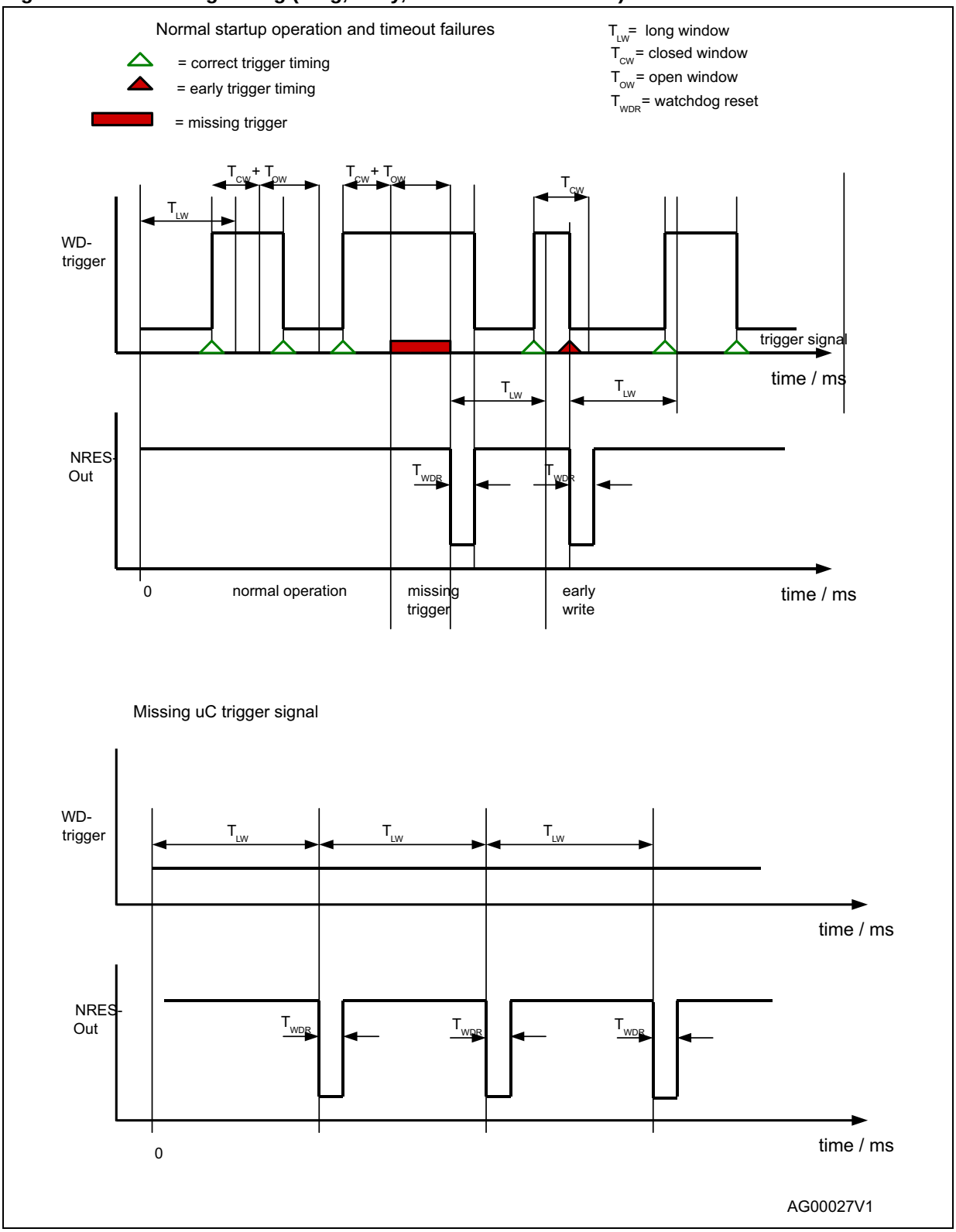
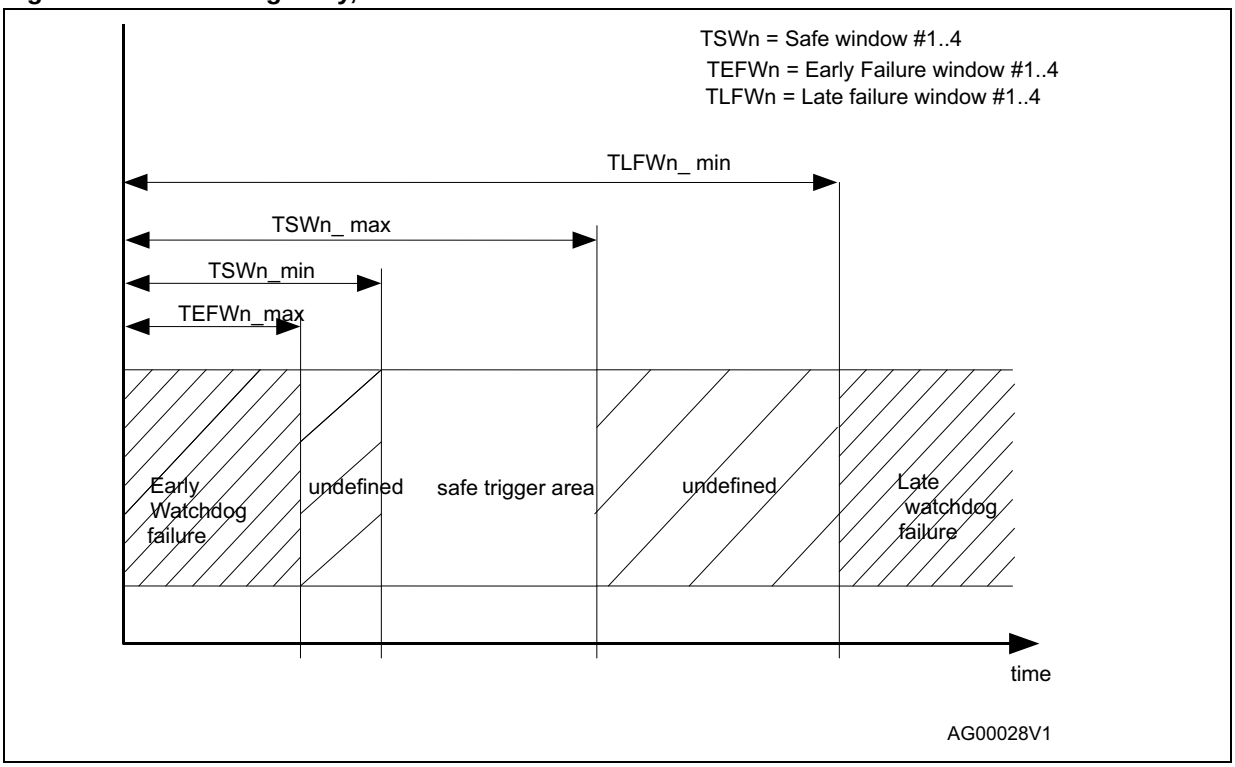


Figure 27. Watchdog early, late and safe windows



5.5.8 High-side outputs

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 18 V; 4.8 V ≤ V_1 ≤ 5.2 V; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 19. Output (OUT_HS)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$R_{DS}ON$	Static drain source on-resistance (IOUT_HS = 150 mA)	T_j = 25 °C		1,0	2	Ω
		T_j = 125 °C		1.6	3	Ω
t_dON	Switch on delay time	0.2 V_S	5	35	60	µs
t_dOFF	Switch off delay time	0.8 V_S	40	95	150	µs
t_{SCF}	Short circuit filter time	Tested by scan chain		64*T_{OSC}		
t_dARHS	Auto recovery filter time	Tested by scan chain		400*T_{OSC}		
dV_{OUT}/dt	Slew rate		0,18	0,5	0,8	V/µs
I_{OUT}	Short circuit shutdown current		480	900	1320	mA
I_{OLD}	Open-load detection current		40	80	120	mA
t_{OLDT}	Open-load detection time	Tested by scan chain		64*T_{OSC}		
I_{FW} [1]	Loss of GND current (ESD structure)		100			mA

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 18 V; 4.8 V ≤ V_1 ≤ 5.2 V; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 20. Outputs (OUT1...4)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$R_{DS}ON$	Static drain source on-resistance (IOUT_HS = 150mA)	I_{LOAD} = 60 mA @ T_j = +25 °C		7	13	Ω
I_{OUT}	Short circuit shutdown current	8 V < V_s < 16 V	140	235	350	mA
I_{OLD}	Open-load detection current 1		0.9	2	4.5	mA
dV_{OUT}/dt	Slew rate		0.2	0.5	0.8	V/µs
t_{dON}	Switch ON delay time	0.2 V_s	5	35	60	µs
t_{dOFF}	Switch OFF delay time	0.8 V_s	30	95	150	µs
t_{SCF}	Short circuit filter time	Tested by scan chain		64*T_{OSC}		
I_{FW}(1)	Loss of GND current (ESD structure)		100			mA
t_{OLDT}	Open-load detection time	Tested by scan chain		64*T_{OSC}		

1. Parameter guaranteed by design

5.5.9 Relay drivers

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 18 V; 4.8 V ≤ V_1 ≤ 5.2 V; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 21. Relay drivers

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{DSON}	DC output resistance	I_{LOAD} = 100 mA @ T_j = +25 °C		2	3	Ω
I_{OUT}	Short circuit shutdown current	8 V < V_s < 16 V	250	375	500	mA
V_Z	Output clamp voltage(1)	I_{LOAD} = 100 mA	40		48	V
t_{ONHL}	Turn on delay time to 10% V_{OUT}		5	50	100	µs
t_{OFFLH}	Turn off delay time to 90% V_{OUT}		5	50	100	µs
t_{SCF}	Short circuit filter time	Tested by scan chain		64*T_{OSC}		
dV_{OUT}/dt	Slew Rate		0.2	2	4	V/µs

1. The output is capable to switch off relay coils with the impedance of R_L = 160Ω; L = 300mH (R_L = 220Ω; L = 420mH); at V_S = 40V (Load dump condition)

5.5.10 Wake up inputs (*WU*1... *WU*3)

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 18 V; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 22. Wake up inputs (*WU*1... *WU*3)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{WUthp}	Wake-up negative edge threshold voltage		0,4*V_s	0.45*V_s	0,5*V_s	V
V_{WUthn}	Wake-up positive edge threshold voltage		0,5*V_s	0,55*V_s	0,6*V_s	V
V_{HYST}	Hysteresis		0.05*V_s	0.1*V_s	0.15*V_s	V
t_{WU_stat}	Static wake filter time			64*T_{OSC}		µs
I_{WU_stdby}	Input current in standby mode	1 V > V_{in} > (V_s - 2 V)	10	20	30	µA
R_{WU_act}	Input resistor to Gnd in active mode and in standby mode during wake-up request		80	160	300	kΩ
t_{WU_cyc}	Cyclic wake filter time			16(1)		µs

1. Blanking time 80 µs or 800 µs.

5.5.11 High speed CAN transceiver(b)

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

6 V ≤ V_S ≤ 18 V; 4.8 V ≤ Vcansup. ≤ 5.2 V; $T_{junction}$ = -40 °C to 130 °C, unless otherwise specified.

Table 23. CAN transmit data input: pin TXDC

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{TXDCLOW}$	Input voltage dominant level	Active mode, V_1 = 5 V	1.35	1.8		V
$V_{TXDCHIGH}$	Input voltage recessive level	Active mode, V_1 = 5 V		2.5	2.8	V
$V_{TXDCHYS}$	$V_{TXDCHIGH}$-$V_{TXDCLOW}$	Active mode, V_1 = 5 V	0.7	1		V
R_{TXDCPU}	TXDC pull up resistor	Active mode, V_1 = 5 V	10	20	35	kΩ

Table 24. CAN receive data output: pin RXDC

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{RXDCLOW}$	Output voltage dominant level	Active mode, V_1 = 5 V, 2 mA		0.2	0.5	V
$V_{RXDCHIGH}$	Output voltage recessive level	Active mode, V_1 = 5 V, 2 mA	4.5			V

b. ISO 11898-2 and ISO 11898-5 compliant; SAE J2284 compliant.

Table 25. CAN bus common mode stabilization output termination: pin SPLIT

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{SPLIT,I}$	Split output voltage, loaded condition (normal mode)	Active mode; $V_{TXDC} = V_{TXDCHIGH}$; |Isplit| = 500 µA	0.3* V_{CANSUP}	0.5* V_{CANSUP}	0.7* V_{CANSUP}	V
$V_{SPLIT,u}$	Split output voltage, unloaded condition (normal mode)	Active mode; $V_{TXDC} = V_{TXDCHIGH}$; No Load		0.5* V_{CANSUP}	0.55* V_{CANSUP}	V
I_{SPLIT}	Split leakage current (low power mode)	V_1-standby mode; -12 V < V_{SPLIT} < 12 V			5	µA

Table 26. CAN transmitter and receiver: pins CANH and CANL

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{CANHdom}$	CANH voltage level in dominant state	Active mode; $V_{TXDC} = V_{TXDCLOW}$; R_L = 60 Ω	2.75		4.5	V
$V_{CANLdom}$	CANL voltage level in dominant state	Active mode; $V_{TXDC} = V_{TXDCLOW}$; R_L = 60 Ω	0.5		2.25	V
$V_{DIFF,domOUT}$	Differential output voltage in dominant state: $V_{CANHdom}$ - $V_{CANLdom}$	Active mode; $V_{TXDC} = V_{TXDCLOW}$; R_L = 60 Ω	1.5		3	V
V_{CM}	Driver symmetry: $V_{CANHdom}$ + 0$V_{CANLdom}$	Active mode; $V_{TXDC} = V_{TXDCLOW}$; R_L = 60 Ω; C_{SPLIT} = 4.7 pF	0.9* V_{CANSUP}	V_{CANSUP}	1.1* V_{CANSUP}	V
$V_{CANHrec}$	CANH voltage level in recessive state (normal mode)	Active mode; $V_{TXDC} = V_{TXDCHIGH}$; no load	2	2.5	3	V
$V_{CANLrec}$	CANL voltage level in recessive state (normal mode)	Active mode; $V_{TXDC} = V_{TXDCHiGH}$; no load	2	2.5	3	V
$V_{CANHrecLP}$	CANH voltage level in recessive state (low power mode)	V_1 standby mode; $V_{TXDC} = V_{TXDCHIGH}$; no load	-0.1	0	0.1	V
$V_{CANLrecLP}$	CANL voltage level in recessive state (low power mode)	V_1 standby mode; $V_{TXDC} = V_{TXDCHiGH}$; no load	-0.1	0	0.1	V
$V_{DIFF,recOUT}$	Differential output voltage in recessive state (normal mode): $V_{CANHrec}$ - $V_{CANLrec}$	Active mode; $V_{TXDC} = V_{TXDCHIGH}$; no load	-50		50	mV
$V_{DIFF,recOUTLP}$	Differential output voltage in recessive state (low power mode): $V_{CANHrec}$ - $V_{CANLrec}$	V_1 standby mode; $V_{TXDC} = V_{TXDCHIGH}$; no load	-50		50	mV

Table 26. CAN transmitter and receiver: pins CANH and CANL (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{CANHL,CM}$	Common mode Bus voltage	Measured with respect to the ground of each CAN node	-12		12	V
$I_{OCANH,dom}$	CANH output current in dominant state	Active mode; $V_{TXDC} = V_{TXDCLOW}$; V_{CANH} = 0 V	-160	-75	-45	mA
$I_{OCANL,dom}$	CANL output current in dominant state	Active mode; $V_{TXDC} = V_{TXDCLOW}$; V_{CANL} = 5 V	45	75	160	mA
$I_{Leakage}$	Input leakage current	Unpowered device; V_{BUS} = 5 V	0		250	µA
R_{in}	Internal resistance	Active mode & V_1 standby mode; $V_{TXDC} = V_{TXDCHIGH}$; no load	20	27.5	38	kΩ
$R_{in,diff}$	Differential internal resistance	Active mode & V_1 standby mode; $V_{TXDC} = V_{TXDCHIGH}$; no load	50	60	75	kΩ
C_{in}	Internal capacitance	Guaranteed by design		20		pF
$C_{in,diff}$	Differential internal capacitance	Guaranteed by design		10		pF
V_{THdom}	Differential receiver threshold voltage recessive to dominant state (normal mode)	Active mode			0.9	V
$V_{THdomLP}$	Differential receiver threshold voltage recessive to dominant state (low power mode)	V_1 standby mode			1.15	V
V_{THrec}	Differential receiver threshold voltage dominant to recessive state (normal mode)	Active mode	0.5			V
$V_{THrecLP}$	Differential receiver threshold voltage dominant to recessive state (low power mode)	V_1 standby mode	0.4			V

Table 27. CAN transceiver timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
tTXpd,hl	Propagation delay TXDC to RXDC (high to low)	Active mode; 50 % V_{TXDC} to 50 % V_{RXDC}; C_{RXDC} = 100 pF; R_L = 60 Ω	0		255	ns
tTXpd,lh	Propagation delay TXDC to RXDC (low to high)	Active mode; 50 % V_{TXDC} to 50 % V_{RXDC}; C_{RXDC} = 100 pF; R_L = 60 Ω	0		255	ns
t_{wake}	Wake up filter time		0.5		5	µs

Table 27. CAN transceiver timing (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{dom(TXDC)}$	TXDC dominant time-out			700		µs
t_{CAN}	CAN permanent dominant time-out			700		µs

5.5.12 LIN transceiver(c)

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

6 V ≤ V_S ≤ 18 V; 4.8 V ≤ V_1 ≤ 5.2 V; $T_{junction}$ = -40 °C to 130 °C unless otherwise specified.

Table 28. LIN transmit data input: pin TXD

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{TXDLOW}	Input voltage dominant level	Active mode; V_1 = 5 V	1,35	1.8		V
$V_{TXDHIGH}$	Input voltage recessive level	Active mode; V_1 = 5 V		2.5	2.8	V
V_{TXDHYS}	$V_{TXDHIGH}$-V_{TXDLOW}	Active mode; V_1 = 5 V	0.7	1		V
R_{TXDPU}	TXD pull up resistor	Active mode; V_1 = 5 V	10	20	35	kΩ

Table 29. LIN receive data output: pin RXD

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{RXDLOW}	Output voltage dominant level	Active mode; V_1 = 5 V, I_{LOAD1} = 2 mA		0.2	0.5	V
$V_{RXDHIGH}$	Output voltage recessive level	Active mode; V_1 = 5 V, I_{LOAD1} = 2 mA	4.5			V

Table 30. LIN transmitter and receiver: pin LIN

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{THdom}	Receiver threshold voltage recessive to dominant state		0.4*V_S	0.45*V_S	0.5*V_S	V
V_{THrec}	Receiver threshold voltage dominant to recessive state		0.5*V_S	0.55*V_S	0.6*V_S	V
V_{THhys}	Receiver threshold hysteresis: V_{THrec} -V_{THdom}		0.07*V_S	0.1*V_S	0.175*V_S	V
V_{THcnt}	Receiver tolerance center value: (V_{THrec} +V_{THdom})/2		0.475*V_S	0.5*V_S	0.525*V_S	V
V_{THwkup}	Receiver wakeup threshold voltage		1.0	1.5	2	V

c. LIN 2.1 compliant for Baud rates up to 20 kBit/s
SAE J2602 compatible

Table 30. LIN transmitter and receiver: pin LIN (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{THwkdwn}$	Receiver wakeup threshold voltage		V_S-3.5	V_S-2.5	V_S-1.5	V
t_{linbus}	Dominant time for wakeup via bus	Sleep mode; edge: rec-dom		64*T_{OSC}		µs
$I_{LINDomSC}$	Transmitter input current limit in dominant state	$V_{TXD} = V_{TXDLOW}$; $V_{LIN} = V_{BATMAX}$ = 18 V	40	100	180	mA
$I_{bus\_PAS\_dom}$	Input leakage current at the receiver incl. pull-up resistor	$V_{TXD} = V_{TXDHIGH}$; V_{LIN} = 0 V; V_{BAT} = 12 V(1)	-1			mA
$I_{bus\_PAS\_rec}$	Transmitter input current in recessive state	$V_{TXD} = V_{TXDHIGH}$; 8 V < V_{LIN}; V_{BAT} < 18 V; V_{LIN} >= V_{BAT} in standby modes			20	µA
$I_{bus\_NO\_GND}$	Input current if loss of GND at device	GND = V_S; 0 V < V_{LIN} < 18 V; V_{BAT} = 12 V	-1		1	mA
I_{bus}	Input current if loss of V_{BAT} at device	GND = V_S; 0 V < V_{LIN} < 18 V			100	µA
V_{LINdom}	LIN voltage level in dominant state	Active mode; $V_{TXD} = V_{TXDLOW}$; I_{LIN} = 40 mA			1.2	V
V_{LINrec}	LIN voltage level in recessive state	Active mode; $V_{TXD} = V_{TXDHIGH}$; I_{LIN} = 10 µA	0.8*V_S		1	V
R_{LINup}	LIN output pull up resistor	V_{LIN} = 0 V	20	40	60	kΩ

1. Slave mode.

Table 31. LIN transceiver timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{RXpd}	Receiver propagation delay time	t_{RXpd} = max(t_{RXpdr}, t_{RXpdf}); t_{RXpdf} = t(0.5 V_{RXD}) - t(0.45 V_{LIN}); t_{RXpdr} = t(0.5 V_{RXD}) - t(0.55 V_{LIN}); V_S = 12 V; C_{RXD} = 20 pF; R_{bus}, = 1 kΩ, C_{bus} = 1 nF; R_{bus} = 660 Ω, C_{bus} = 6.8 nF; R_{bus} = 500 Ω, C_{bus} = 10 nF			6	µs
t_{RXpd_sym}	Symmetry of receiver propagation delay time (rising vs. falling edge)	t_{RXpd_sym} = t_{RXpdr} - t_{RXpdf}; V_S = 12 V; R_{bus} = 1 kΩ, C_{bus} = 1 nF	-2		2	µs

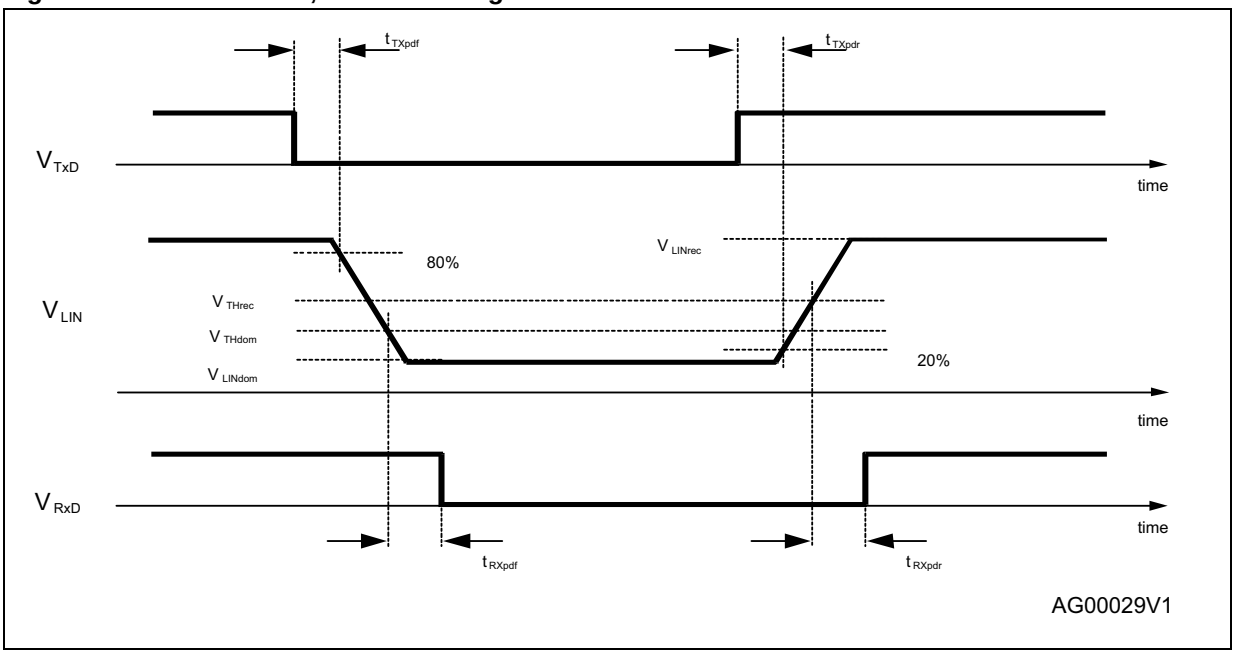
Table 31. LIN transceiver timing (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
D1	Duty cycle 1	$TH_{Rec}(max) = 0.744*V_S$; $TH_{Dom}(max) = 0.581*V_S$; V_S = 7 V to 18 V, t_{bit} = 50 µs; D1 = $t_{bus\_rec}(min)/(2xt_{bit})$; R_{bus} = 1 kΩ, C_{bus} = 1 nF; R_{bus} = 660 Ω, C_{bus} = 6.8 nF; R_{bus} = 500 Ω, C_{bus} = 10 nF	0.396			
D2	Duty cycle 2	$TH_{Rec}(min) = 0.284*V_S$; $TH_{Dom}(min) = 0.422*V_S$; V_S = 7.6 to 18 V, t_{bit} = 50 µs; D2 = $t_{bus\_rec}(max)/(2xt_{bit})$; R_{bus} = 1 kΩ, C_{bus} = 1 nF; R_{bus} = 660 Ω, C_{bus} = 6.8 nF; R_{bus} = 500 Ω, C_{bus} = 10 nF			0.581	
D3	Duty cycle 3	$TH_{Rec}(max) = 0.778*V_S$; $TH_{Dom}(max) = 0.616*V_S$; V_S = 7 V to 18 V, t_{bit} = 96 µs; D3 = $t_{bus\_rec}(min)/(2xt_{bit})$; R_{bus} = 1 kΩ, C_{bus} = 1 nF; R_{bus} = 660 Ω, C_{bus} = 6.8 nF; R_{bus} = 500 Ω, C_{bus} = 10 nF	0.417			
D4	Duty cycle 4	$TH_{Rec}(min) = 0.251*V_S$; $TH_{Dom}(min) = 0.389*V_S$; V_S = 7.6 V to 18 V, t_{bit} = 96 µs; D4 = $t_{bus\_rec}(max)/(2xt_{bit})$; R_{bus} = 1 kΩ, C_{bus} = 1 nF; R_{bus} = 660 Ω, C_{bus} = 6.8 nF; R_{bus} = 500 Ω, C_{bus} = 10 nF			0.590	
$t_{dom(TXDL)}$	TXDL dominant time-out			12		ms
t_{LIN}	LIN permanent recessive time-out			40		µs
$t_{dom(BUS)}$	LIN bus permanent dominant time-out			12		ms

Table 32. LIN pull-up: pin LINPU

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
RDS_{ON}	ON resistance			10.5	16	Ω
I_{leak}	Leakage current				1	µA

Figure 28. LIN transmit, receive timing



5.5.13 Operational amplifier

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 18 V; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 33. Operational amplifier

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
GBW	GBW product		1	3.5	7.0	MHz
$AVOL_{DC}$	DC open loop gain		80			dB
PSRR	Power supply rejection	DC, Vin = 150 mV	80			dB
V_{off}	Input offset voltage		-5		+5	mV
V_{ICR}	Common mode input range		-0.2	0	3	V
V_{OH}	Output voltage range high	I_{LOAD} = 1 mA to Gnd	V_S-0.2		V_S	V
V_{OL}	Output voltage range low	I_{LOAD} = 1 mA to V_S	0		0.2	V
I_{Lim+}	Output current limitation +	DC	10	15	30	mA
I_{lim-}	Output current limitation -	DC	-10	15	-30	mA
SR+	Slew rate positive		1	4	10	V/µs
SR-	Slew rate negative		-1	-4	-10	V/µs

Note: The operational amplifier is on-chip stabilized for external capacitive loads C_L ≤ 25 pF (all operating conditions)

5.5.14 SPI

Input: CSN

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 18 V; 4.5 V ≤ V_1 ≤ 5.3 V; all outputs open; T_j = -40 °C to 130 °C, unless otherwise specified.

Input: CSN

Table 34. Input: CSN

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VCSNLOW	Input voltage low level	Normal mode, V_1 = 5 V	1.35	1.8		V
VCSNHIGH	Input voltage high level	Normal mode, V_1 = 5 V		2	2.8	V
VCSNHYS	VCSNHIGH - VCSNLOW	Normal mode, V_1 = 5 V	0.6	1.0	1.5	V
ICSNPU	CSN pull up resistor	Normal mode, V_1 = 5 V	10	20	35	kΩ

CLK, DI

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 18 V; 4.5 V ≤ V_1 ≤ 5.3 V; all outputs open; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 35. Input CLK, DI

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{set}	delay time from standby to active mode	Switching from standby to active mode. Time until output drivers are enabled after CSN going to high.		160	300	µs
$V_{in\ L}$	input low level	V_1 = 5 V	1.0	2.05	2.5	V
$V_{in\ H}$	input high level	V_1 = 5 V	1.5	2.8	3.5	V
$V_{in\ Hyst}$	input hysteresis	V_1 = 5 V	0.4	0.75	1.5	V
I_{in}	pull down current at input	V_{in} = 1.5 V	5	30	60	µA
C_{in}(1)	input capacitance at input CSN, CLK, DI and $PWM_{1,2}$	0 V < V_1 < 5.3 V		10	15	pF
f_{CLK}	SPI input frequency at CLK				1	MHz

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

DI timing

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 18 V; 4.5 V ≤ V_1 ≤ 5.3 V; all outputs open; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 36. DI timing(1)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{CLK}	Clock period	V_1 = 5 V	1000	-		ns
t_{CLKH}	Clock high time	V_1 = 5 V	400	-		ns
t_{CLKL}	Clock low time	V_1 = 5 V	400	-		ns
$t_{set\ CSN}$	CSN setup time, CSN low before rising edge of CLK	V_1 = 5 V	400	-		ns
$t_{set\ CLK}$	CLK setup time, CLK high before rising edge of CSN	V_1 = 5 V	400	-		ns
$t_{set\ DI}$	DI setup time	V_1 = 5 V	200	-		ns
$t_{hold\ DI}$	DI hold time	V_1 = 5 V	200	-		ns
$t_{r\ in}$	Rise time of input signal DI, CLK, CSN	V_1 = 5 V		-	100	ns
$t_{f\ in}$	Fall time of input signal DI, CLK, CSN	V_1 = 5 V		-	100	ns

1. See *Figure 30*.

DO

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 18 V; 4.5 V ≤ V_1 ≤ 5.3 V; all outputs open; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 37. DO output pin

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DOL}	Output low level	V_1 = 5 V, I_D = -4 mA			0.5	V
V_{DOH}	output high level	V = 5 V, I_D = 4 mA	4.5			V
I_{DOLK}	3-state leakage current	V_{CSN} = V_1, 0 V < V_{DO} < V_1	-10		10	µA
C_{DO} [2]	3-state input capacitance	V_{CSN} = V_1, 0 V < V_1 < 5.3 V		10	15	pF

DO timing

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 18 V; 4.5 V ≤ V_1 ≤ 5.3 V; all outputs open; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 38. DO timing(1)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{r\ DO}$	DO rise time	C_L = 100 pF, I_{LOAD} = -1 mA	-	50	100	ns
$t_{f\ DO}$	DO fall time	C_L = 100 pF, I_{LOAD} = 1 mA	-	50	100	ns
$t_{en\ DO\ tri\ L}$	DO enable time from 3-state to low level	C_L = 100 pF, I_{LOAD} = 1 mA pull-up load to V_1	-	50	250	ns

Table 38. DO timing(1) (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{dis\ DO\ L\ tri}$	DO disable time from low level to 3-state	C_L = 100 pF, I_{LOAD} = 4 mA pull-up load to V_1	-	50	250	ns
$t_{en\ DO\ tri\ H}$	DO enable time from 3-state to high level	C_L = 100 pF, I_{LOAD} = -1 mA pull-down load to GND	-	50	250	ns
$t_{dis\ DO\ H\ tri}$	DO disable time from high level to 3-state	C_L = 100 pF, I_{LOAD} = -4 mA pull-down load to GND	-	50	250	ns
$t_{d\ DO}$	DO delay time	V_{DO} < 0.3 V_1, V_{DO} > 0.7 V_1, C_L = 100 pF	-	50	250	ns

1. See *Figure 31* and *Figure 32*.

CSN timing

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 18 V; 4.5 V ≤ V_1 ≤ 5.3 V; all outputs open; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 39. CSN timing(1)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
tCSN_HI,min	Minimum CSN HI time, active mode	Transfer of SPI-command to Input register	6			µs
$t_{CSNfail}$	CSN low timeout	Tested by scan chain	20	35	50	ms

1. See *Figure 33*.

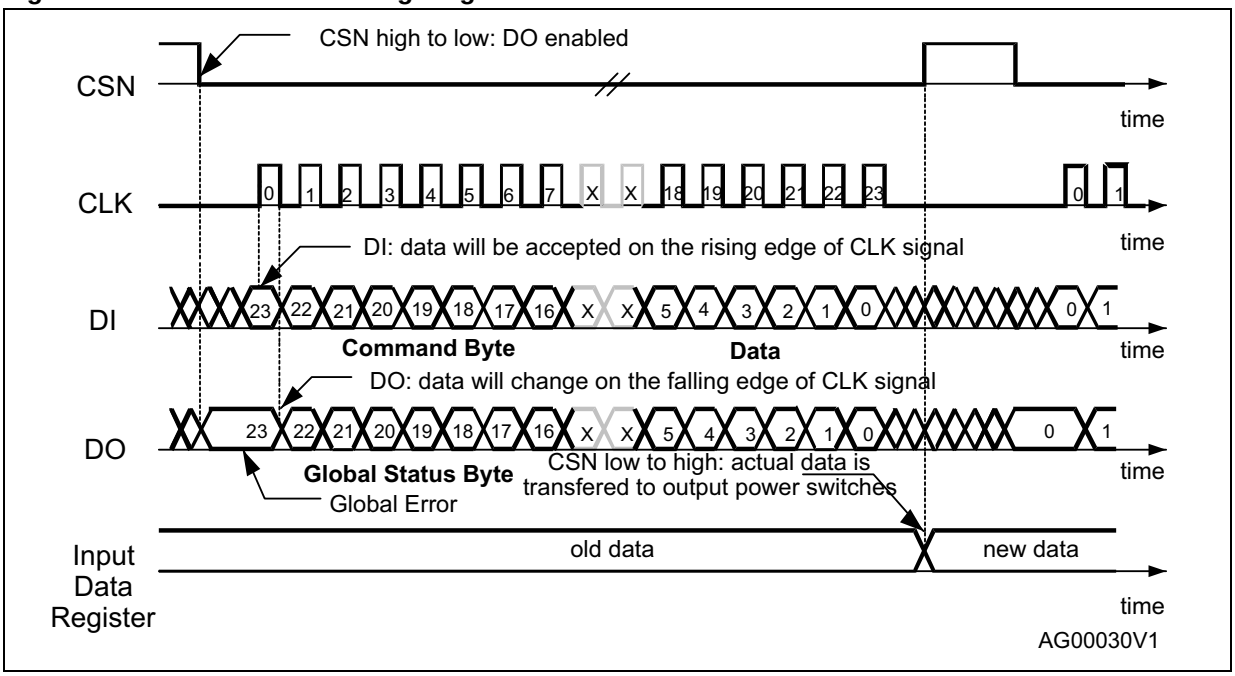
5.5.15 Inputs TxD_C and TxD_L for Flash mode

6 V ≤ Vs ≤ 18 V; 4.5 V ≤ V_1 ≤ 5.3 V; T_j = -40 °C to 130 °C, voltages are referred to PGND, all outputs open

Table 40. Inputs TxD_C and TxD_L for Flash mode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{FlashL}	Input low level ($V_{TXDC/L}$ rising)	V_1 = 5 V	6.1	7.25	8.4	V
V_{FlashH}	Input high level ($V_{TXDC/L}$ falling)	V_1 = 5 V	7.4	8.4	9.4	V
$V_{FlashHYS}$	Input Voltage Hysteresis	V_1 = 5 V	0.6	0.8	1.0	V

Figure 29. SPI – transfer timing diagram



The SPI can be driven by a micro controller with its SPI peripheral running in following mode:

CPOL = 0 and CPHA = 0.

For this mode input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

Figure 30. SPI - input timing

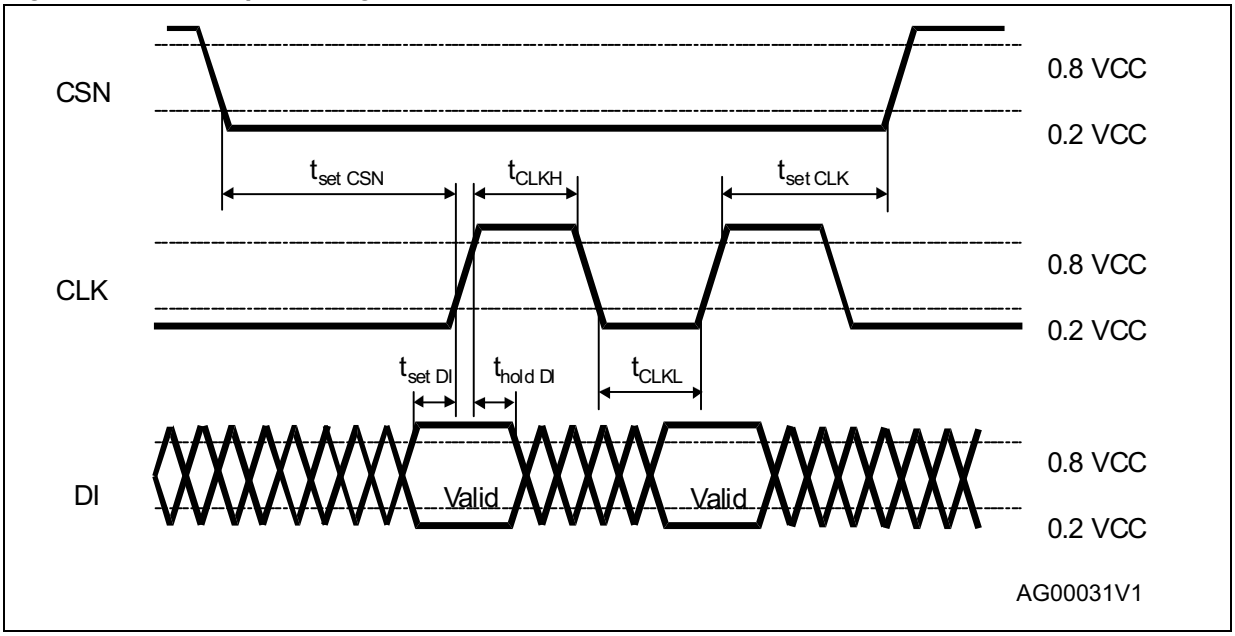


Figure 31. SPI output timing (part 1)

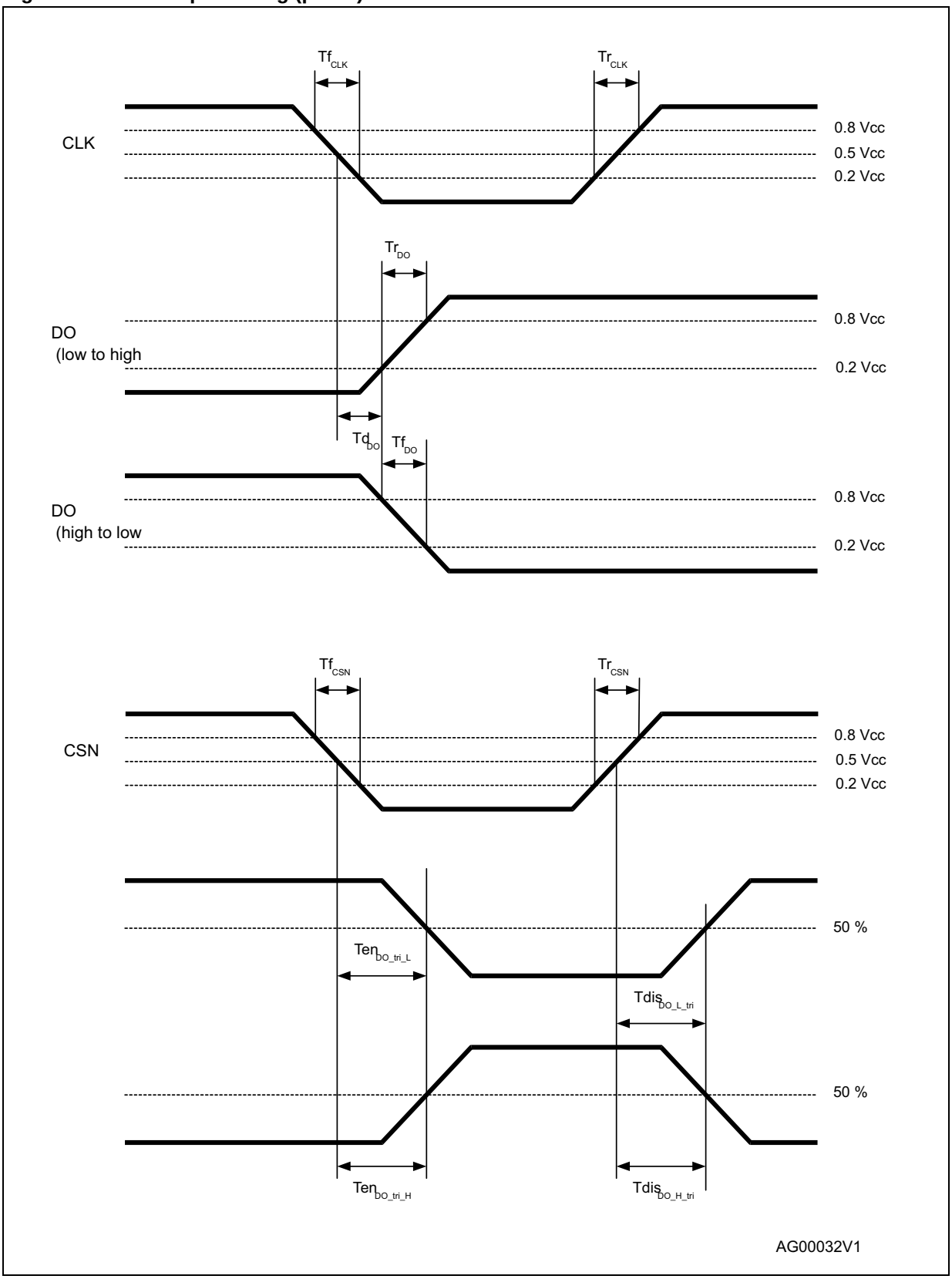


Figure 32. SPI output timing (part 2)

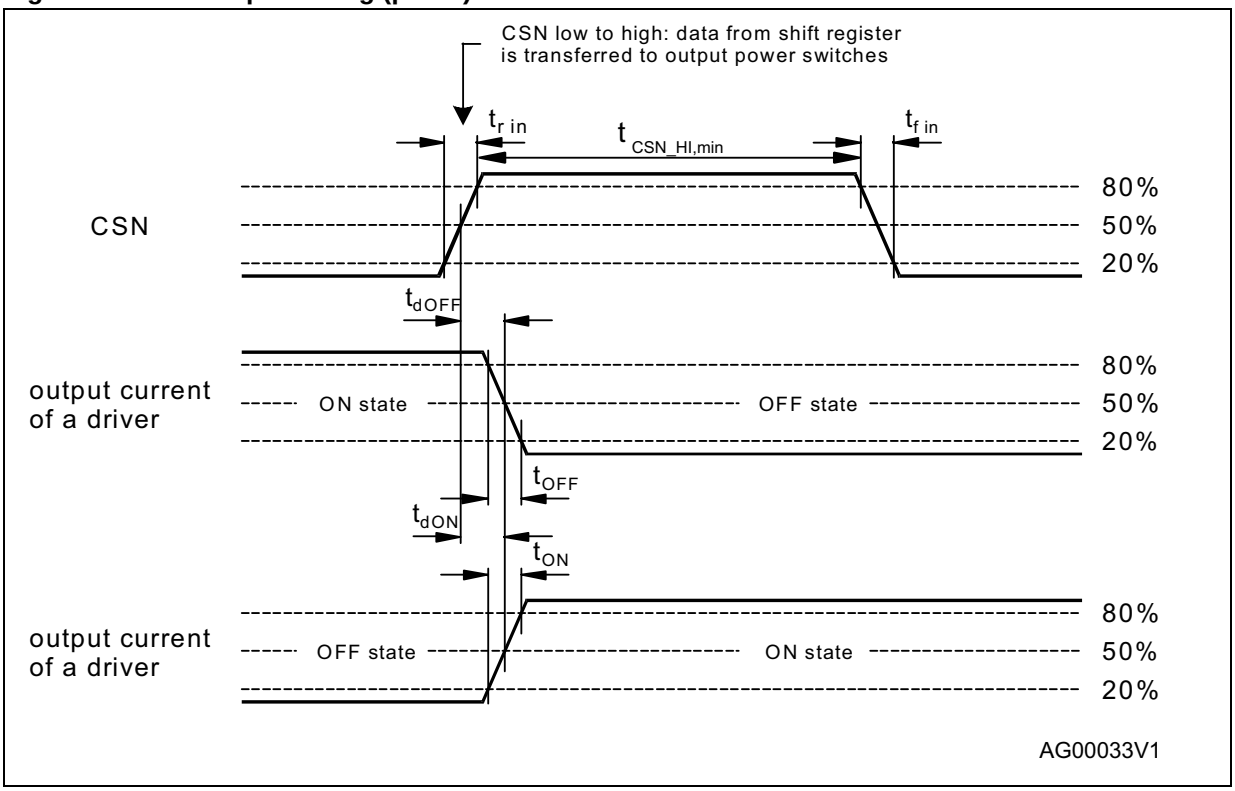
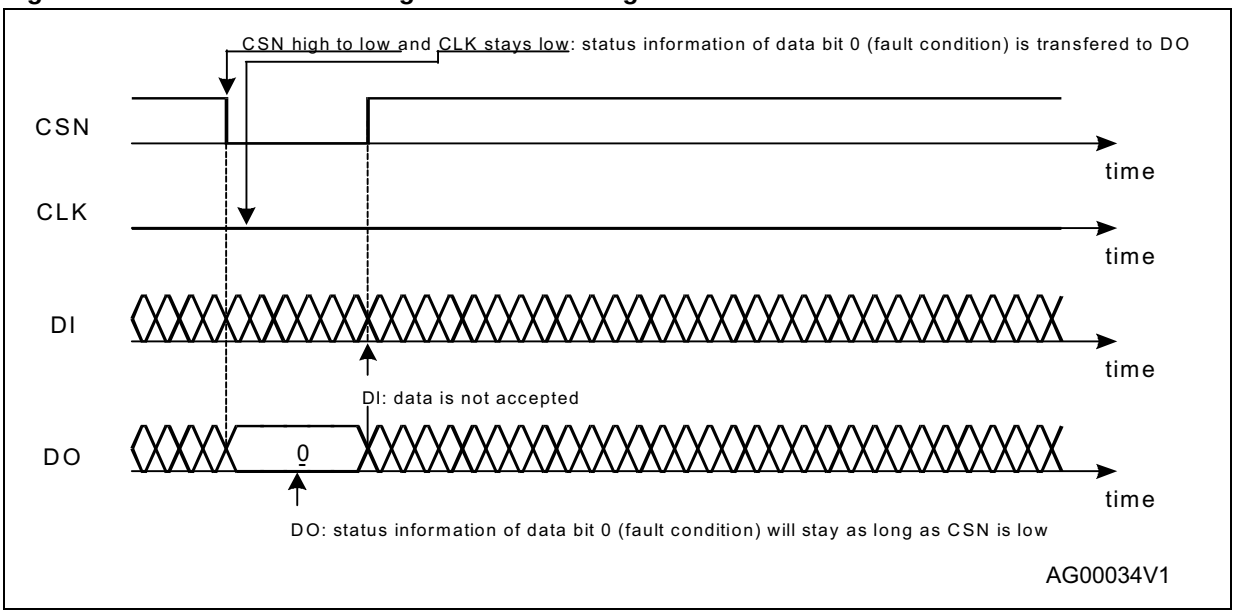


Figure 33. SPI – CSN low to high transition and global status bit access



6 ST SPI

6.1 SPI communication flow

6.1.1 General description

The proposed SPI communication is based on a standard SPI interface structure using CSN (Chip Select Not), SDI (Serial Data In), SDO (Serial Data Out/Error) and SCK (Serial Clock) signal lines.

At device start-up the master reads the <*SPI-frame-ID*> register (ROM address 3EH) of the slave device. This 8-bit register indicates the SPI frame length (24bit) and the availability of additional features.

Each communication frame consists of an instruction byte which is followed by 2 data bytes.

The data returned on SDO within the same frame always starts with the <Global Status> register. It provides general status information about the device. It is followed by 2 data bytes (i. e. 'In-frame-response').

For write cycles the <*Global Status*> register is followed by the previous content of the addressed register.

For read cycles the <Global Status> register is followed by the content of the addressed register.

A write command is only accepted as a valid command by the device if the counted number of clocks is exact 24, otherwise the command is rejected.

Command byte

Each communication frame starts with a command byte. It consists of an operating code which specifies the type of operation (<Write>, <Read>, <Read and Clear>, <Read Device Information>) and a 6 bit address. If less than 6 address bits are required, the remaining bits are unused but are reserved.

Table 41. Command byte

MSB							**LSB**
Op code		Address					
OC1	OC0	A5	A4	A3	A2	A1	A0

OCx: operating code

Ax: address

6.1.2 Operating code definition

Table 42. Operating code definition

OC1	**OC0**	**Meaning**
0	0	<Write Mode>
0	1	<Read Mode>

Table 42. Operating code definition (continued)

OC1	OC0	Meaning
1	0	<Read and Clear Status>
1	1	<Read Device Information>

The <Write Mode> <Read Mode> and <Read and Clear Status> operations allow access to the RAM of the device, i. e. to write to control registers or read status information.

A <Read and Clear Status> operation addressed to a device specific status register reads back and subsequently clear this status register.

A <Read and Clear Status> operation with address 3FH clears all status registers (including the Global Status Register). Configuration register is read by this operation.

<Read Device Information> allows access to the ROM area which contains device related information such as the product family, product name, silicon version, register width and availability of a watchdog.

More detailed descriptions of the device information are available in 'Read Device Information'.

6.1.3 Global status register[(d)]

Table 43. Global status register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Global error flag (GEF)	Comm error	Not (chip reset OR comm error)	TSD2	TSD1	V_1 Fail	VS Fail (OV/UV)	Fail safe

6.1.4 Configuration register

The <Configuration> register is accessible at RAM address 3FH.

For the config register, the 8 bits are located in the low byte (LSB).

The configuration register is implemented for compliance purpose to ST SPI standard.

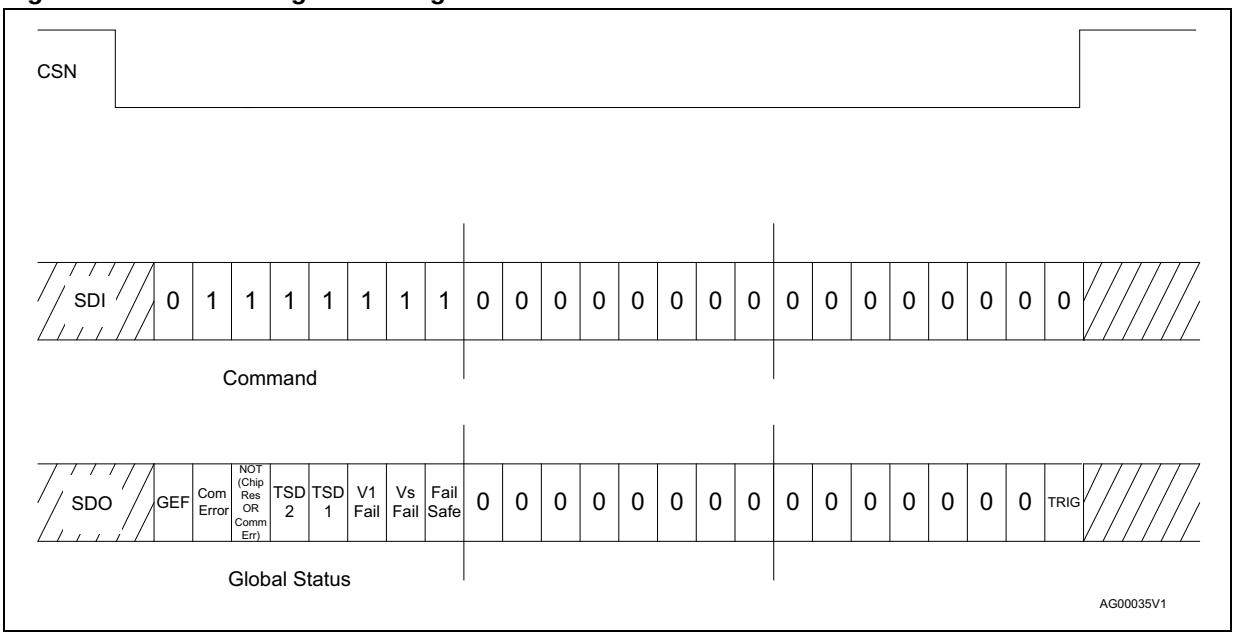
Table 44. Configuration register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	WD trigger

<WD trigger>: this bit is reserved to serve the watchdog.

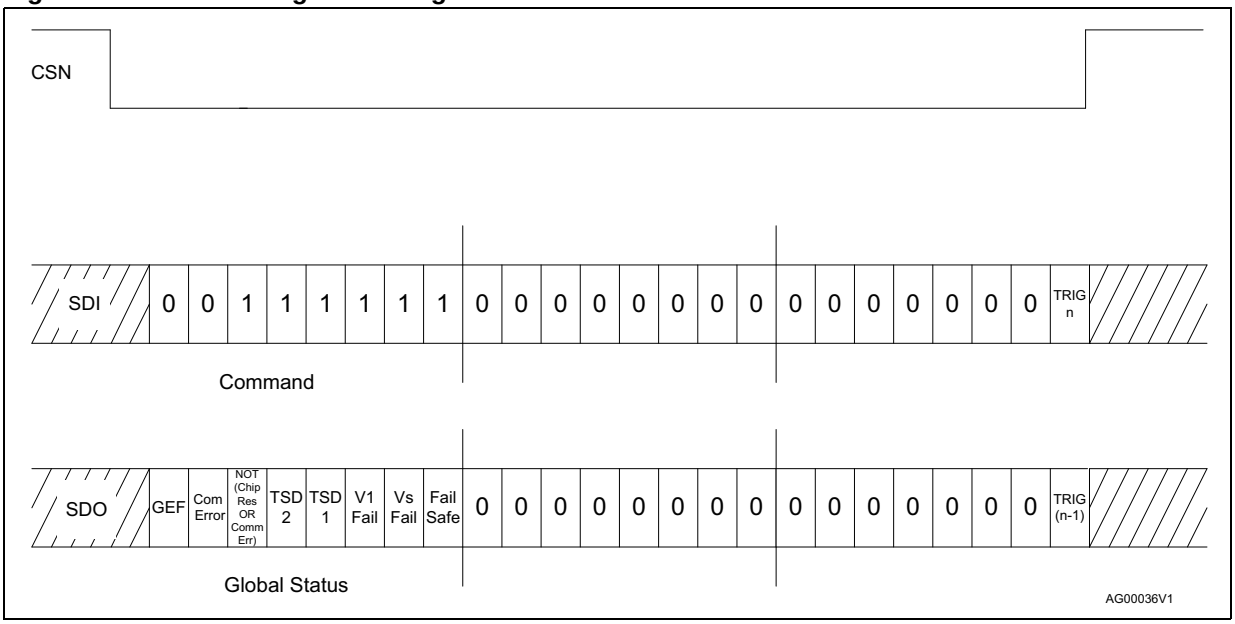
d. See *Section 6.2* for details.

Figure 34. Read configuration register



1. The configuration register is implemented for compliance with ST standard SPI 3.0 and contains only the watchdog trigger bit at D0

Figure 35. Write configuration register



1. The configuration register is implemented for compliance with ST standard SPI 3.0 and contains only the watchdog trigger bit at D0

6.1.5 Address mapping

Table 45. Address mapping

RAM adress	Description	Access
3FH	<Configuration>	R/W
13H	Status register 3	R
12H	Status register 2	R
11H	Status register 1	R
06H	Control register 6	R/W
05H	Control register 5	R/W
04H	Control register 4	R/W
03H	Control register 3	R/W
02H	Control register 2	R/W
01H	Control register 1	R/W
00H	Reserved	R/W

ROM adress	Description	Access
3FH	Reserved	N/A
3EH	<SPI frame ID>	R
…	Unused	N/A
03H	<product code 2>	N/A
02H	<product code 1>	R
01H	<silicon version>	R
00H	<ID Header>	R

The RAM memory area consists of 16 bit registers.

For the device information (ROM memory area) the eight most significant bits of the memory cell are used. The remaining 8 are zero.

All unused RAM and ROM addresses is read as ‘0’.

Note: 1 The register definition for RAM address 00H is unused. A register value of all 0 must cause the device to enter a fail-safe state (interpreted as ‘SDI stuck to GND’ failure).

2 ROM address 3FH is unused. An attempt to access this address must be recognized as a communication error (‘SDI stuck to V_{CC}’ failure) and must cause the device to enter a fail-safe state.

6.1.6 Write operation

The write operation starts with a command byte followed by 2 data bytes. The number of data bytes is specified in the <*SPI-frame-ID*>.

Write command format

Table 46. Write command format: command byte

MSB							LSB
Op Code		Address					
0	0	A5	A4	A3	A2	A1	A0

Table 47. Write command format: data byte 1

MSB							LSB
D15	D14	D13	D12	D11	D10	D9	D8

Table 48. Write command format: data byte 2

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

OC0, OC1: operating code (00 for ‘write’ mode)

A0 to A5: address bits

An attempt to write 00H at RAM address 00H is recognized as a failure (SDI stuck to GND). The device enters a fail-safe state.

6.1.7 Format of data shifted out at SDO during write cycle

Table 49. Format of data shifted out at SDO during write cycle: global status register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Global error flag (GEF)	Comm error	Not (chip reset or comm error)	TSD2	TSD1	V_1 Fail	V_S Fail (OV/UV)	Fail safe

Table 50. Format of data shifted out at SDO during write cycle: data byte 1

MSB	Previous content of addressed register						LSB
D15	D14	D13	D12	D11	D10	D9	D8

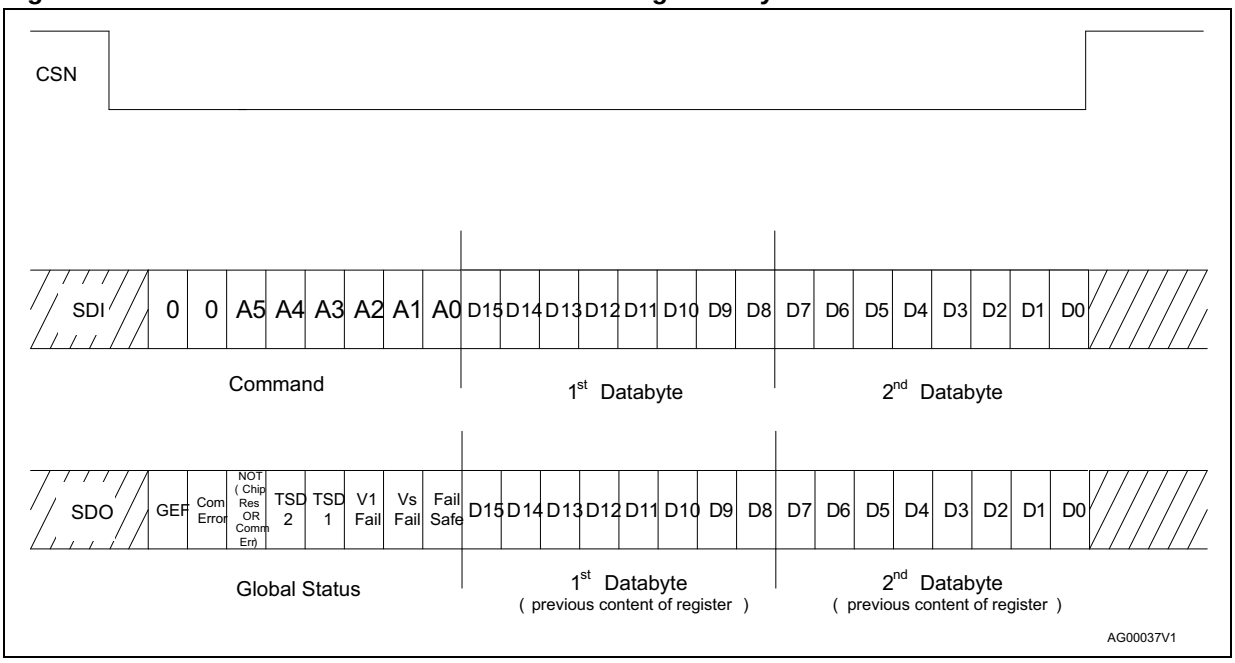
Table 51. Format of data shifted out at SDO during write cycle: data byte 2

MSB	Previous content of addressed register						LSB
D7	D6	D5	D4	D3	D2	D1	D0

Failures are indicated by activating the corresponding bit of the <Global Status> register.

The returned data byte(s) represent(s) the previous content of the accessed register.

Figure 36. Format of data shifted out at SDO during write cycle



6.1.8 Read operation

The read operation starts with a command byte followed by 2 data bytes. The number of data bytes is specified in the <*SPI-frame-ID*>. The content of the data bytes is ‘don’t care’. The content of the addressed register is shifted out at SDO within the same frame (‘in-frame response’).

Read command format

Table 52. Read command format: command byte

MSB							LSB
Op Code		Address					
0	1	A5	A4	A3	A2	A1	A0

Table 53. Read command format: data byte 1

MSB							LSB
0	0	0	0	0	0	0	0

Table 54. Read command format: data byte 2

MSB							LSB
0	0	0	0	0	0	0	0

OC0, OC1: operating code (01 for ‘read’ mode)

A0 to A5: address bits

6.1.9 Format of data shifted out at SDO during read cycle

Table 55. Format of data shifted out at SDO during read cycle: global status register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Global error flag (GEF)	Comm error	Not (chip reset or comm error)	TSD2	TSD1	V_1 Fail	V_S Fail (OV/UV)	Fail safe

Table 56. Format of data shifted out at SDO during read cycle: data byte 1

MSB	Previous content of addressed register						LSB
D15	D14	D13	D12	D11	D10	D9	D8

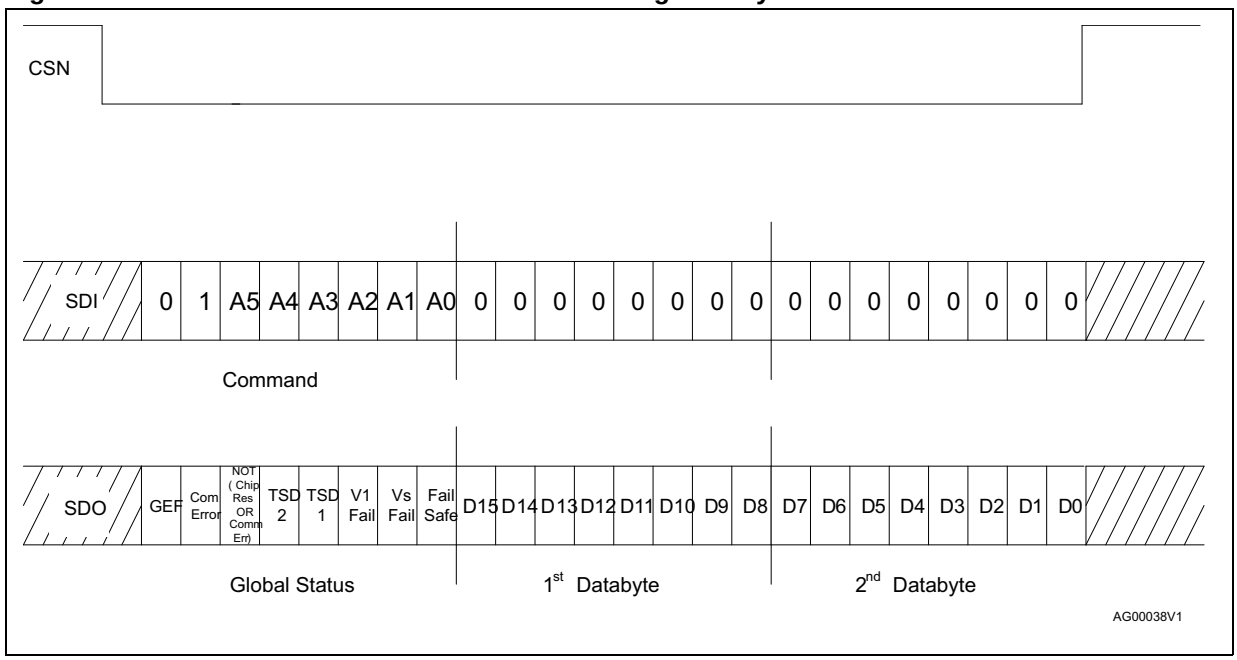
Table 57. Format of data shifted out at SDO during read cycle: data byte 2

MSB	Previous content of addressed register						LSB
D7	D6	D5	D4	D3	D2	D1	D0

Failures are indicated by activating the corresponding bit of the <Global Status> register.

The returned data byte(s) represent(s) the content of the register to be read.

Figure 37. Format of data shifted out at SDO during read cycle



6.1.10 Read and clear status operation

The 'Read and Clear Status' operation starts with a command byte followed by 2 data bytes. The number of data bytes is specified in the <*SPI-frame-ID*>. The content of the data bytes

is ‘don’t care’. The content of the addressed status register is transferred to SDO within the same frame (‘in-frame response’) and is subsequently cleared.

A ‘Read and Clear Status’ operation with address 3FH clears all status registers (incl. the <*Global Status*> register). The configuration register is read by this operation.

Read and clear status command format

Table 58. Read and clear status command format: command byte

MSB							LSB
Op Code		Address					
1	01	A5	A4	A3	A2	A1	A0

Table 59. Read and clear status command format: data byte 1

MSB							LSB
0	0	0	0	0	0	0	0

Table 60. Read and clear status command format: data byte 2

MSB							LSB
0	0	0	0	0	0	0	0

OC0, OC1: operating code (10 for ‘read and clear status’ mode)

A0 to A5: address bits

Format of data shifted out at SDO during read and clear status operation

Table 61. Format of data shifted out at SDO during read and clear status: global status register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Global error flag (GEF)	Comm error	Not (chip reset or comm error)	TSD2	TSD1	V_1 Fail	V_S Fail (OV/UV)	Fail safe

Table 62. Format of data shifted out at SDO during read and clear status: data byte 1

MSB	Previous content of addressed register						LSB
D15	D14	D13	D12	D11	D10	D9	D8

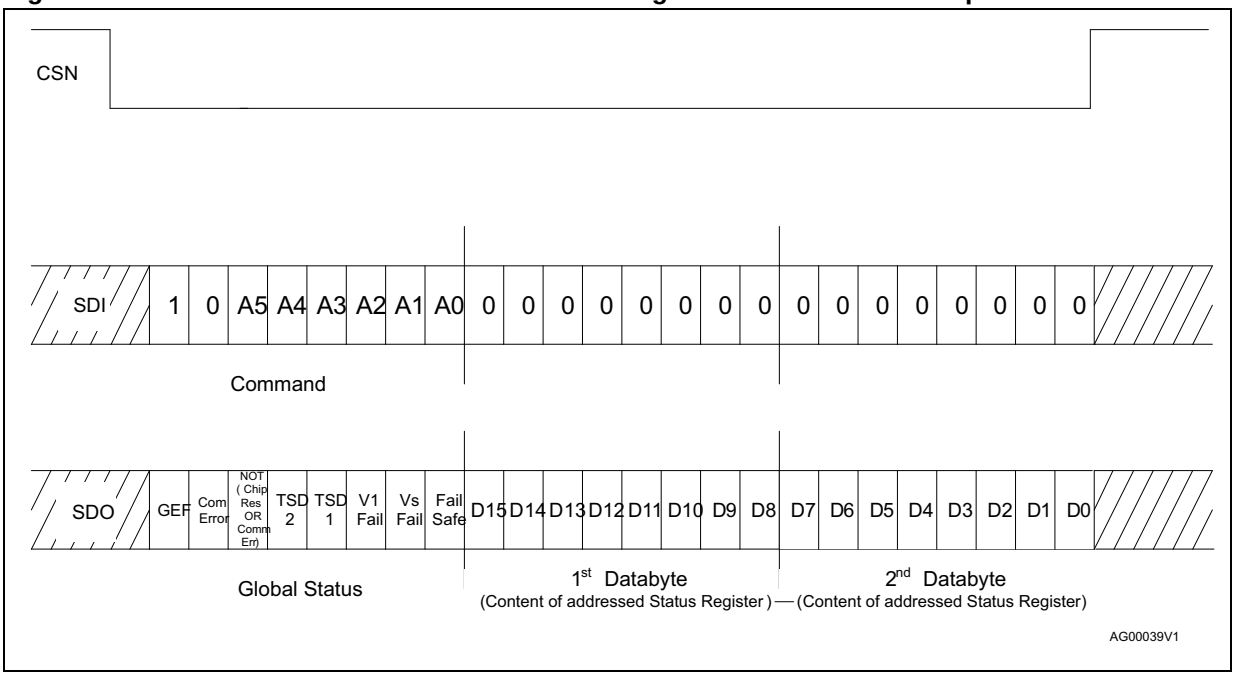
Table 63. Format of data shifted out at SDO during read and clear status: data byte 2

MSB	Previous content of addressed register						LSB
D7	D6	D5	D4	D3	D2	D1	D0

Failures are indicated by activating the corresponding bit of the <Global Status> register.

The returned data byte(s) represent(s) the content of the register to be read.

Figure 38. Format of data shifted out at SDO during read and clear status operation



6.1.11 Read device information

The device information is stored at the ROM addresses defined below and is read using the respective operating code.

Table 64. Read device information

Op code		ROM address	Device information	Value
OC1	OC0			
1	1	3FH	Reserved	00
1	1	3EH	<SPI frame ID> includes frame width and availability of watchdog	42 Hex
1	1	04H to 3DH	unused	00
1	1	03H	<product code 2> unique product identifier	4E Hex
1	1	02H	<product code 1> unique product identifier	44 Hex
1	1	01H	<silicon version> indicates Design Version	According to silicon version
1	1	00H	<ID Header> device family max adress of device information	43 Hex

The <*ID-Header*> (ROM address 00H) indicates the product family and specifies the highest address which contains product information

Table 65. ID-header

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	0	0	1	1
Family Identifier		Highest address containing device information					

<*Family Identifier*>*:* 01 Hex (BCD)

<Highest address>: 03 Hex

Table 66. Family identifier

Bit 7	Bit 6	Meaning
0	0	VIPower
0	1	BCD
1	0	VIPower hybrid
1	1	Tbd

The <*Product Code 1*> *(*ROM address 02H) and <*Product Code 2*> *(*ROM address 03H) represents a unique code to identify the product name.

<*Product Code 1*> 44 Hex

<*Product Code 2*> 4E Hex

The <*Silicon Version*> (ROM address 01H) provides information about the silicon version according to the table below:

Table 67. Silicon version identifier

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				Silicon version			

The <*SPI-frame-ID*> (ROM address 3EH) provides information about the register width (1, 2, 3 bytes) and the availability of ‘Burst Mode Read’ and watchdog.

Table 68. SPI-frame-ID

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	0	0	1	0
BR	WD	X	X	X	32-bit	24-bit	16-bit

BR: burst-mode read (1 = burst-mode read is supported)

WD: watchdog (1 = available, 0 = not available)

32-bit, 24-bit, 16-bit: width of SPI frame (see table below)

<Burst Mode>: not supported

<Watchdog>: available

<Frame Width>: 24 bit

6.2 SPI registers

6.2.1 Overview

Overview command byte

Table 69. SPI register: command byte

Read/write		Address					
x	x	x	x	x	x	x	x

Table 70. SPI register: mode selection

Read/write		Mode selection
0	0	Write
0	1	Read
1	0	Read and clear
1	1	Read device info

Table 71. SPI register: CTRL register selection

CTRL register 1…6						CTRL register selection
0	0	0	0	0	1	CTRL register1
0	0	0	0	1	0	CTRL register2
0	0	0	0	1	1	CTRL register3
0	0	0	1	0	0	CTRL register4
0	0	0	1	0	1	CTRL register5
0	0	0	1	1	0	CTRL register6

Table 72. SPI register: STAT register selection

STAT register. 1…3						STAT register selection
0	1	0	0	0	1	STAT register1
0	1	0	0	1	0	STAT register2
0	1	0	0	1	1	STAT register3

Overview of control register data bytes

6.2.2 Control registers

Table 73. Overview of control registers data bytes

	1st data byte <15:8>								2nd data byte <7:0>							
	Control register 1, data															
Defaults	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0
Function	OUT HS	OUT HS	OUT 4	OUT 4	OUT HS_EXT	OUT 3	OUT 2	OUT 1	REL 2	REL 1	V_2	V_2	Res	Stby sel	Go Stby	Trig
Group	HS control								LS Output, V_2 and mode control							
	Control register 2, data															
Defaults			0	0	0	0	0	0	0	0	0	0		1	1	1
Function	Res	Res	Inp. Filt 3	Inp. Filt 3	Inp. Filt 2	Inp. Filt 2	Inp. Filt 1	Inp. Filt1	Res	Input Pu/Pd 3	Input Pu/Pd 2	Input Pu/Pd 1	Res	WU EN 3	WU EN 2	WU EN 1
Group	Wake-up control								Wake-up control							
	Control register 3, data															
Defaults		0	0	0		0	0	0			0	0	1	1	0	0
Function	Res	T1 On	T1 Per	T1 Per	Res	T2 On	T2 Per	T2 Per	Res	Res	WD time	WD time	LIN WU En	CAN WU En	Wake timer En	Wake Timer Select
Group	Timer Settings								Watchdog and cyclic wake up settings							
	Control register 4, data															
Defaults		0	0	1		1	0	0	1	1	1	1	0	1	1	0
Function	Res	I_{CMP}	OutHS Rec En	Vlock Out En	Res	LS OV/UV shut down_en	V_1 Reset Level	V_1 Reset Level	LIN Pu En	Res	Lin TxD Tout En	CAN ACT	CAN Loop En	CAN Patt. wake En	CAN split On	CAN Rec Only
Group	Control (other)								Transceiver settings							
	Control register 5, data															
Defaults		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Function	Res	PWM2 Off-DC	PWM2 Off-DC	PWM2 Off-DC	PWM2 Off-DC	PWM2 Off-DC	PWM2 Off-DC	PWM2 Off-DC	PWM Freq	PWM1 ON-DC	PWM1 ON-DC	PWM1 ON-DC	PWM1 ON-DC	PWM1 ON-DC	PWM1 ON-DC	PWM1 ON-DC
Group	PWM2 setting								PWM1 setting							
	Control register 6, data															
Defaults		1	1	1	1	1	1	1		0	0	0	0	0	0	0
Function	Res	PWM4 Off-DC	PWM4 Off-DC	PWM4 Off-DC	PWM4 Off-DC	PWM4 Off-DC	PWM4 Off-DC	PWM4 Off-DC	Res	PWM3 ON-DC	PWM3 ON-DC	PWM3 ON-DC	PWM3 ON-DC	PWM3 ON-DC	PWM3 ON-DC	PWM3 ON-DC
Group	PWM4 setting								PWM3 setting							

Control register 1

Table 74. Control register 1: command and data bytes

Command byte								1st data byte	2nd data byte
Read/write		Address							
x	x	0	0	0	0	0	1	Data, 8bit	Data, 8 bit

Table 75. Control register 1, data bytes

	1st data byte <15:8>								2nd data byte <7:0>							
Defaults	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0
Function	OUT HS_2	OUT HS_1	OUT 4_2	OUT 4_1	OUT HS_EXT	OUT 3	OUT 2	OUT 1	REL 2	REL 1	V_{2_2}	V_{2_1}	Res	Stby sel	Go Stby	Trig
Group	HS control								LS Output, V_2 and mode control							

Table 76. Control register 1, bits

Bit	Name	Comment
15	OUTHS	Select mode of OUTHS
14		**OUTHS_EXT** / **OUTHS_2** / **OUTHS_1** / **Mode** 0 / 0 / 0 / HS off 0 / 0 / 1 / HS cyclic on with timer 1 0 / 1 / 0 / HS controlled by PWM4 0 / 1 / 1 / HS cyclic on with Timer 2 1 / 1 / 0 / PWM3(1) 1 / x / 1 / HS on Mode: Active and standby mode 1) PWM4 (CR6) must be unequal 0% in order to enable PWM3 To turn off OUT4, we recommend to use the setting 'HS Off' (OUT4_1 = 0, OUT4_2 = 0)
13	OUT4	Select mode of OUT4
12		**OUT4_2** / **OUT4_1** / **Mode** 0 / 0 / HS off 0 / 1 / HS on 1 / 0 / HS controlled by PWM4 1 / 1 / HS cyclic on with Timer 2 Mode: Active and standby mode
11	OUTHS_EXT	Extended function of OUTHS; see table OUTHS

Table 76. Control register 1, bits (continued)

<table>
<tr><th>Bit</th><th>Name</th><th>Comment</th></tr>
<tr><td>10</td><td>OUT3</td><td>Select mode of OUT3
<table>
<tr><th>OUT3</th><th></th><th>Mode</th></tr>
<tr><td>0</td><td>Select FSO</td><td>Active and standby mode</td></tr>
<tr><td>1</td><td>Select PWM3</td><td></td></tr>
</table></td></tr>
<tr><td>9</td><td>OUT2</td><td>Select mode of OUT2
<table>
<tr><th>OUT2</th><th></th><th>Mode</th></tr>
<tr><td>0</td><td>Select PWM2</td><td rowspan="2">Active and standby mode</td></tr>
<tr><td>1</td><td>Select timer2</td></tr>
</table></td></tr>
<tr><td>8</td><td>OUT1</td><td>Select mode of OUT1
<table>
<tr><th>OUT1</th><th></th><th>Mode</th></tr>
<tr><td>0</td><td>Select PWM1</td><td rowspan="2">Active and standby mode</td></tr>
<tr><td>1</td><td>Select timer1</td></tr>
</table></td></tr>
<tr><td>7</td><td>REL2</td><td>Select mode of REL2
<table>
<tr><th>REL2</th><th></th><th>Mode</th></tr>
<tr><td>0</td><td>REL2 off</td><td>Active and standby mode</td></tr>
<tr><td>1</td><td>REL2 on</td><td>Active mode</td></tr>
</table></td></tr>
<tr><td>6</td><td>REL1</td><td>Select mode of REL1
<table>
<tr><th>REL1</th><th></th><th>Mode</th></tr>
<tr><td>0</td><td>REL1 off</td><td>Active and standby mode</td></tr>
<tr><td>1</td><td>REL1 on</td><td>Active mode</td></tr>
</table></td></tr>
</table>

Table 76. Control register 1, bits (continued)

<table>
<tr><th>Bit</th><th>Name</th><th>Comment</th></tr>
<tr><td>5</td><td rowspan="2">V_2</td><td rowspan="2"></td></tr>
<tr><td>4</td></tr>
<tr><td>3</td><td>RES</td><td>Reserved</td></tr>
<tr><td>2</td><td>STBY_SEL</td><td>Select standby mode</td></tr>
<tr><td>1</td><td>GO_STBY</td><td>Execute standby mode</td></tr>
<tr><td>0</td><td>TRIG</td><td>Trigger Bit for Watchdog</td></tr>
</table>

V_{2_2}	V_{2_1}	
0	0	V_2 OFF in all modes
0	1	V_2 ON in active mode; OFF in V_1/V_{BAT} standby mode
1	0	V_2 ON in Active/V_1 standby mode; OFF in V_{BAT} standby mode
1	1	V_2 ON in all modes

0	V_{BAT} standby mode
1	V_1standby mode

0	No action
1	Execute standby mode

Control register 2

Table 77. Control register 2: command and data bytes

Command byte								1st data byte	2nd data byte
Read/write		Address							
x	x	0	0	0	0	1	0	Data, 8bit	Data, 8 bit

Table 78. Control register 2, data bytes

	1st data byte <15:8>								2nd data byte <7:0>							
Defaults			0	0	0	0	0	0		0	0	0		1	1	1
Function	Res	Res	Wu3 Filt_MSB	Wu3 Filt_LSB	WU2 Filt_MSB	WU2 Filt_LSB	WU1 Filt_MSB	WU1 Filt_LSB	Res	WU3 Pu/Pd	WU2 Pu/Pd	WU1 Pu/Pd	Res	WU3 EN	WU2 EN	WU1 EN
Group	Wakeup control								Wakeup control							

Table 79. Control register 2, bits

Bit	Name	Comment		
15	Res	Reserved		
14	Res	Reserved		
13, 12	WU3_Filt	Wakeup filter configuration		
11, 10	WU2_Filt	**MSB**	**LSB**	
9, 8	WU1_Filt	0	0	Static, 64 µs
		0	1	Enabled with timer 2; 80 µs blank
		1	0	Enabled with timer 2; 800 µs blank
		1	1	Enabled with timer 1; 800 µs blank
7	Res	Reserved		
6	WU3_Pu/Pd	Pull up or pull down configuration		
5	WU2_Pu/Pd	0	Pull down	
4	WU1_Pu/Pd	1	Pull up	
3	Res	Reserved		
2	WU3_EN	Enable Wake up source		
1	WU2_EN	0	Disable	
0	WU1_EN	1	Enable	

Control register 3

Table 80. Control register 3: command data bytes

Command byte								1st data byte	2nd data byte
Read/write		Address							
x	x	0	0	0	0	1	1	Data, 8bit	Data, 8 bit

Table 81. Control register 3, data bytes

	1st data byte <15:8>								2nd data byte <7:0>							
Defaults		0	0	0	0	0	0	0			0	0	1	1	0	0
Function	Res	T1 On	T1 Per MSB	T1 Per LSB	Res	T2 On	T2 Per MSB	T2 Per LSB	Res	Res	WD time MSB	WD time LSB	LIN WU En	CAN WU En	Wake timer En	Wake timer select
Group	Timer Settings								Watchdog and cyclic wake up settings							

Table 82. Control register 3, bits

<table>
<tr><th>Bit</th><th>Name</th><th>Comment</th></tr>
<tr><td>15</td><td>RES</td><td>Reserved</td></tr>
<tr><td>14</td><td>T1_On</td><td>Timer 1 “ON” time selections
0 | 10 ms
1 | 20 ms</td></tr>
<tr><td>13</td><td>T1_Per_MSB</td><td rowspan="2">Timer 1 period selection
MSB | LSB |
0 | 0 | 1 s
0 | 1 | 2 s
1 | 0 | 3 s
1 | 1 | 4 s
Timer 1 is restarted with a valid write command to control register 3</td></tr>
<tr><td>12</td><td>T1_Per_LSB</td></tr>
<tr><td>11</td><td>Res</td><td></td></tr>
<tr><td>10</td><td>T2_On</td><td>Timer 2 “ON” time selection
0 | 0.1 ms
1 | 1 ms</td></tr>
<tr><td>9</td><td>T2_Per_MSB</td><td rowspan="2">Timer 2 period selection
MSB | LSB |
0 | 0 | 10 ms
0 | 1 | 50 ms
1 | 0 | 100 ms
1 | 1 | 200 ms
Timer 2 is restarted with a valid write command to control register 3</td></tr>
<tr><td>8</td><td>T2_Per_LSB</td></tr>
<tr><td>7</td><td>Res</td><td>Reserved</td></tr>
<tr><td>6</td><td>Res</td><td>Reserved</td></tr>
</table>

Table 82. Control register 3, bits (continued)

<table>
<tr><th>Bit</th><th>Name</th><th>Comment</th></tr>
<tr><td>5</td><td>WD_time_MSB</td><td rowspan="2">Trigger window selection
<table><tr><th>MSB</th><th>LSB</th><th></th></tr><tr><td>0</td><td>0</td><td>10 ms</td></tr><tr><td>0</td><td>1</td><td>20 ms</td></tr><tr><td>1</td><td>0</td><td>50 ms</td></tr><tr><td>1</td><td>1</td><td>200 ms</td></tr></table></td></tr>
<tr><td>4</td><td>WD_time_LSB</td></tr>
<tr><td>3</td><td>LIN_WU_En</td><td>Enable LIN as wake up source
<table><tr><td>0</td><td>Disabled</td></tr><tr><td>1</td><td>Enabled</td></tr></table></td></tr>
<tr><td>2</td><td>CAN_WU_En</td><td>Enable CAN as wake up source
<table><tr><td>0</td><td>Disabled</td></tr><tr><td>1</td><td>Enabled</td></tr></table></td></tr>
<tr><td>1</td><td>Wake_timer_En</td><td>Enable wake up by timer from V_1 standby mode (Interrupt) or V_{BAT} standby Mode (Nreset)
<table><tr><td>0</td><td>Disabled</td></tr><tr><td>1</td><td>Enabled</td></tr></table></td></tr>
<tr><td>0</td><td>Wake_timer_select</td><td>Timer selection for timer interrupt / wake-up of µC by timer
<table><tr><td>0</td><td>Timer 2</td></tr><tr><td>1</td><td>Timer 1</td></tr></table></td></tr>
</table>

Control register 4

Table 83. Control register 4: command and data bytes

Command byte								1st data byte	2nd data byte
Read/Write		Address							
x	x	0	0	0	1	0	0	Data, 8bit	Data, 8 bit

Table 84. Control register 4, data bytes

	1st data byte <15:8>								2nd data byte <7:0>							
Defaults		0	0	1	0	1	0	0	1	1	1	1	0	1	1	0
Function	RES	I_{CMP}	OutHS Rec En	Vlock Out_en	RES	LS OV/UV shut down_en	V_1 Reset Lev_2	V_1 Reset Lev_1	LIN Pu En	Res	Lin TxD Tout En	CAN ACT	CAN Loop En	CAN Patt. wake En	CAN split On	CAN Rec only
Group	Control (other)								Transceiver settings							

Table 85. Control register 4, bits

Bit	Name	Comment
15	Res	Reserved; must be set to zero
14	I_{cmp}	V_1 load current supervision 0: Enabled; Watchdog is disabled in V_1 Standby when the $V_{1loadcurrent} < I_{cmpthreshold}$ 1: Disabled; Watchdog is automatically disabled when V_1 standby is entered
13	OUTHS_rec_en	Overcurrent Auto recovery mode for OUTHS 0: Disabled 1: Enabled
12	Vlock_out_en	Voltage lock out: OV/UV status 0: Over/under voltage status recovers automatically when condition disappears 1: Over/under voltage status is latched until a read and clear command is performed
11	Res	Reserved
10	LS_OV/UV shut_down_en	Shutdown of low-side drivers in case of over-/under voltage 0: No shutdown of low-sides in case of over/under voltage 1: Shutdown low-sides in case of over/under voltage

Table 85. Control register 4, bits (continued)

<table>
<tr><th>Bit</th><th>Name</th><th>Comment</th></tr>
<tr><td>9</td><td>V1Reset_level_1</td><td>Select reset level</td></tr>
<tr><td>8</td><td>V1Reset_level_2</td><td>
<table>
<tr><th>V1RSTlev_2</th><th>V1RSTlev_1</th><th>V1 reset level</th></tr>
<tr><td>0</td><td>0</td><td>4.6 V</td></tr>
<tr><td>0</td><td>1</td><td>4.35 V</td></tr>
<tr><td>1</td><td>0</td><td>4.1 V</td></tr>
<tr><td>1</td><td>1</td><td>3.8 V</td></tr>
</table>
</td></tr>
<tr><td>7</td><td>LIN_PU_EN</td><td>Enable internal Lin pull up
<table>
<tr><td>0</td><td>No LIN master pull-up</td></tr>
<tr><td>1</td><td>LIN master pull-up</td></tr>
</table>
</td></tr>
<tr><td>6</td><td>Res</td><td>Must be written to ‘1’</td></tr>
<tr><td>5</td><td>Lin_TxD_Tout_En</td><td>Enable / disable monitoring via TxD
<table>
<tr><td>0</td><td>No TxD monitoring</td></tr>
<tr><td>1</td><td>TxD monitoring; LIN transmitter is switched off if TXDL is dominant for t > 12 ms</td></tr>
</table>
</td></tr>
<tr><td>4</td><td>CAN_ACT</td><td>Activate CAN transceiver
<table>
<tr><td>0</td><td>CAN transceiver deactivated</td><td rowspan="2">Active mode</td></tr>
<tr><td>1</td><td>CAN transceiver activated</td></tr>
</table>
</td></tr>
<tr><td>3</td><td>CAN_Loop_En</td><td>Enable looping of CANTX to CANRXD in V_1 standby0
<table>
<tr><td>0</td><td>No looping</td></tr>
<tr><td>1</td><td>TXDC is looped to RXDC in V_1 standby</td></tr>
</table>
</td></tr>
<tr><td>2</td><td>CAN_Patt_wake_En</td><td>Enable pattern wake up for CAN
<table>
<tr><td>0</td><td>No pattern wake up</td></tr>
<tr><td>1</td><td>Pattern wake up</td></tr>
</table>
</td></tr>
<tr><td>1</td><td>CAN_split_On</td><td>Enable SPLIT termination for CAN
<table>
<tr><td>0</td><td>Split termination disabled</td><td rowspan="2">Active mode</td></tr>
<tr><td>1</td><td>Split termination enabled</td></tr>
</table>
</td></tr>
</table>

Table 85. Control register 4, bits (continued)

Bit	Name	Comment		
0	CAN_Rec_only	Enable CAN receive only mode		
		0	CAN in transceiver mode	Active mode
		1	CAN in receive only mode	

Control register 5

Table 86. Control register 5: command and data bytes

Command byte								1st data byte	2nd data byte
Read/write		Address							
x	x	0	0	0	1	0	1	Data, 8bit	Data, 8 bit

Table 87. Control register 5, data bytes

	1st data byte <15:8>								2nd data byte <7:0>							
Defaults		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Function	Res	PWM2 Off-DC	PWM2 Off-DC	PWM2 Off-DC	PWM2 Off-DC	PWM2 Off-DC	PWM2 Off-DC	PWM2 Off-DC	PWM Freq	PWM1 ON-DC	PWM1 ON-DC	PWM1 ON-DC	PWM1 ON-DC	PWM1 ON-DC	PWM1 ON-DC	PWM1 ON-DC
Group	PWM2 setting								PWM1 setting							

Table 88. Control register 5, bits

Bit	Name	Comment							
15	RES	Reserved; must be set to zero							
14	PWM2_ Off_DC_6								
13	PWM2_ Off_DC_5	**PWM2 OFF_ DC_6**	**PWM2 OFF_ DC_5**	**PWM2 OFF_ DC_4**	**PWM2 OFF_ DC_3**	**PWM2 OFF_ DC_2**	**PWM2 OFF_ DC_1**	**PWM2 OFF_ DC_0**	**PWM duty cycle**
12	PWM2_ Off_DC_4	1	1	1	1	1	1	1	0%, HS OFF
11	PWM2_ Off_DC_3	...							
10	PWM2_ Off_DC_2	0	0	0	0	0	1	0	98.5%
9	PWM2_ Off_DC_1	0	0	0	0	0	0	1	99.25%
8	PWM2_ Off_DC_0	0	0	0	0	0	0	0	100% HS ON

Table 88. Control register 5, bits (continued)

Bit	Name	Comment							
7	PWM_ FREQ	Select PWM frequency 0 – 128 Hz 1 – 256 Hz							
6	PWM1_ ON_DC_6								
5	PWM1_ ON_DC_5	**PWM1 ON_ DC_6**	**PWM1 ON_ DC_5**	**PWM1 ON_ DC_4**	**PWM1 ON_ DC_3**	**PWM1 ON_ DC_2**	**PWM1 ON_ DC_1**	**PWM1 ON_ DC_0**	**PWM duty cycle**
4	PWM1_ ON_DC_4	1	1	1	1	1	1	1	100%, HS ON
3	PWM1_ ON_DC_3	...							
2	PWM1_ ON_DC_2	0	0	0	0	0	1	0	1.5%
1	PWM1_ ON_DC_1	0	0	0	0	0	0	1	0.75%
0	PWM1_ ON_DC_0	0	0	0	0	0	0	0	0% HS OFF

Control register 6

Table 89. Control register 6: command and data bytes

Command byte								1st data byte	2nd data byte
Read/Write		Address							
x	x	0	0	0	1	1	0	Data, 8bit	Data, 8 bit

Table 90. Control register 6, data bytes

	1st data byte <15:8>								2nd data byte <7:0>							
Defaults		1	1	1	1	1	1	1		0	0	0	0	0	0	0
Function	Res	PWM4 Off_ DC_6	PWM4 Off_ DC_5	PWM4 Off_ DC_4	PWM4 Off_ DC_3	PWM4 Off_ DC_2	PWM4 Off_ DC_1	PWM4 Off_ DC_0	Res	PWM3 ON_ DC_6	PWM3 ON_ DC_5	PWM3 ON_ DC_4	PWM3 ON-DC_3	PWM3 ON_ DC_2	PWM3 ON_ DC_1	PWM3 ON_ DC_0
Group	PWM4 setting								PWM3 setting							

Table 91. Control register 6, bits

Bit	Name	Comment							
15	RES	Reserved; must be set to zero							
14	PWM4_ Off_DC_6								
13	PWM4_ Off_DC_5	**PWM4 OFF_ DC_6**	**PWM4 OFF_ DC_5**	**PWM4 OFF_ DC_4**	**PWM4 OFF_ DC_3**	**PWM4 OFF_ DC_2**	**PWM4 OFF_ DC_1**	**PWM4 OFF_ DC_0**	**PWM4 duty cycle**
12	PWM4_ Off_DC_4	1	1	1	1	1	1	1	0%, HS OFF
11	PWM4_ Off_DC_3	...							
10	PWM4_ Off_DC_2	0	0	0	0	0	1	0	98.5%
9	PWM4_ Off_DC_1	0	0	0	0	0	0	1	99.25%
8	PWM4_ Off_DC_0	0	0	0	0	0	0	0	100% HS ON
7	RES	Reserved; must be set to zero							
6	PWM3_ ON_DC_6								
5	PWM3_ ON_DC_5	**PWM3 ON_ DC_6**	**PWM3 ON_ DC_5**	**PWM3 ON_ DC_4**	**PWM3 ON_ DC_3**	**PWM3 ON_ DC_2**	**PWM3 ON_ DC_1**	**PWM3 ON_ DC_0**	**PWM3 duty cycle**
4	PWM3_ ON_DC_4	1	1	1	1	1	1	1	100%, HS ON
3	PWM3_ ON_DC_3	...							
2	PWM3_ ON_DC_2	0	0	0	0	0	1	0	1.5%
1	PWM3_ ON_DC_1	0	0	0	0	0	0	1	0.75%
0	PWM3_ ON_DC_0	0	0	0	0	0	0	0	0% HS OFF

6.2.3 Status registers

Table 92. Overview of status register data bytes

	1st data byte <15:8>								2nd data byte <7:0>							
	Status register 1, data <15:0>															
Function	OL HS	OL OUT4	OL OUT3	OL OUT2	OL OUT1	UV	V_2 fail	V_2 short	OV	OC HS	OC Out4	OC Out3	OC OUT2	OC Out1	OC Rel2	OC Rel1
Group	Diagnosis 1								Diagnosis 2							
	Status register 2, data <15:0>															
Function	WU3 state	WU2 state	WU1 state	WU3 wake	WU2 wake	WU1 Wake	Wake CAN	Wake LIN	Wake Timer int	LIN perm. dom.	LIN TxD perm dom.	LIN perm. rec.	CAN RxD perm rec.	CAN perm. rec.	CAN perm. dom.	CAN TxD perm dom
Group	Diagnosis 3								Diagnosis 4							
	Status register 3, data <15:0>															
Function	TSD1	TW	Device state	Device state	V_1 fail	V_1 restart	V_1 restart	V_1 restart	WD fail	WD fail	WD fail	WD fail	Forced sleep WD	Forced sleep TSD2 SHTV1	WD timer state	WD timer state
Group	Diagnosis 5								Diagnosis 6							

Table 93. Global status register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex value
	Global error flag(1)	Communication error(2)	NOT (chip reset or comm. error) i.e. cold start (3)	TSD2(4)	TSD1	V_1 Fail	Vs fail(5) (OV/UV)	Fail safe(6)	
Active high/low	High	High	Low	High	High	High	High	High	
Default value in normal mode - after correct WD trigger or after read & clear on error flags	0	0	1	0	0	0	0	0	20
Power ON	1	0	0	0	0	0	0	0	80
Power ON weak battery(7)	1	0	0	0	0	0	1	0	82
Communication error	1	1	0	0	0	0	0	0	C0
Vs over or under-voltage	1	0	1	0	0	0	1	0	A2
WD failure	1	0	1	0	0	0	0	1	A1

Table 93. Global status register (continued)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex value
	Global error flag(1)	Communication error(2)	NOT (chip reset or comm. error) i.e. cold start (3)	TSD2(4)	TSD1	V_1 Fail	Vs fail(5) (OV/UV)	Fail safe(6)	
SPI error (DI stuck)	1	0	1	0	0	0	0	1	A1
TSD1	1	0	1	0	1	0	0	0	A8
TSD2	1	0	1	1	1	0	0	1	B9
V_1 fail	1	0	1	0	0	1	0	0	A4
Other device failure(8)	1	0	1	0	0	0	0	0	A0

1. The following status bits are reported in the global error flag:

   Global status register: Bits 0 - 6

   Status register 1: Bits 0 – 10

   Status register 3: Bits 2, 3, 15
2. Invalid CLOCK COUNT.
3. Cleared with CLR command on SR3.
4. Cleared with “READ and CLEAR” on SR3 (-> TSD1).
5. Diagnosis bit only, Vs Fail is not a fail-safe event; cleared by read&clear. Bit is automatically cleared at (Vs > VsUV) and. (Vs < VsOV) if Vlock_out_en = 0.
6. Cleared with a valid WD trigger (WD fail) or by clearing the corresponding status register related to failure.
7. Slow Vs ramp-up (Vs undervoltage is filtered with 64 µs after Power-on reset).
8. The global error flag is raised due to a failure condition which is not reported in the global status register. The Failure is reported in the status registers 1 – 3.

Status register 1

Table 94. Status register 1: command and data bytes

Command byte								1st data byte	2nd data byte
Read/write		Address						Bit <15:8>	Bit<7:0>
x	x	0	1	0	0	0	1	Data, 8bit	Data, 8 bit

Table 95. Status register 1, data bytes

	1st data byte <15:8>								2nd data byte <7:0>							
Function	OL HS	OL OUT4	OL OUT3	OL OUT2	OL OUT1	UV	V_2 fail	V_2 short	OV	OC HS	OC Out4	OC Out3	OC OUT2	OC Out1	OC Rel2	OC Rel1
Group	Diagnosis 1								Diagnosis 2							

Table 96. Status register 1, bits

<table>
<tr><th>Bit</th><th>Name</th><th>Comment</th><th>Information storage</th></tr>
<tr><td>15</td><td>OL_HS</td><td rowspan="5">Open-load event occurred since last read out</td><td rowspan="5">Bit is latched until a “read and clear” access</td></tr>
<tr><td>14</td><td>OL_OUT4</td></tr>
<tr><td>13</td><td>OL_OUT3</td></tr>
<tr><td>12</td><td>OL_OUT2</td></tr>
<tr><td>11</td><td>OL_OUT1</td></tr>
<tr><td>10</td><td>UV</td><td>Under voltage event on V_S occurred since last read out</td><td><table><tr><th>VLOCKOUTEN (CR4)</th><th>Information storage</th></tr><tr><td>0</td><td>automatically reset when UV condition disappears</td></tr><tr><td>1</td><td>Bit is latched until a “read and clear” access</td></tr></table></td></tr>
<tr><td>9</td><td>V_2_fail</td><td>V_2 fail (V_2 < 2 V for t> 2 µs) event occurred since last readout</td><td>Bit is latched until a “Read and clear” access</td></tr>
<tr><td>8</td><td>V_2_short</td><td>V_2 short (V_2 < 2 V for t > 4ms during start up) event occurred since last readout</td><td>Bit is latched until a “Read and clear” access</td></tr>
<tr><td>7</td><td>OV</td><td>Over voltage event on V_S occurred since last read out</td><td><table><tr><th>VLOCKOUTEN (CR4)</th><th>Information storage</th></tr><tr><td>0</td><td>automatically reset when OV condition disappears</td></tr><tr><td>1</td><td>Bit is latched until a “read and clear” access</td></tr></table></td></tr>
<tr><td>6</td><td>OC_HS</td><td rowspan="7">Over current event occurred since last read out</td><td rowspan="7">Bit is latched until a “read and clear” access</td></tr>
<tr><td>5</td><td>OC_OUT4</td></tr>
<tr><td>4</td><td>OC_OUT3</td></tr>
<tr><td>3</td><td>OC_OUT2</td></tr>
<tr><td>2</td><td>OC_OUT1</td></tr>
<tr><td>1</td><td>OC_REL2</td></tr>
<tr><td>0</td><td>OC_REL1</td></tr>
</table>

Status register 2

Table 97. Status register 2: command and data bytes

Command byte								1st data byte	2nd data byte
Read/write		Address						Bit <15:8>	Bit<7:0>
x	x	0	1	0	0	1	0	Data, 8bit	Data, 8 bit

Table 98. Status register 2, data bytes

	1st data byte <15:8>								2nd data byte <7:0>							
Function	WU3 state	WU2 state	WU1 state	WU3 wake	WU2 wake	WU1 wake	Wake CAN	Wake LIN	Wake Timer int	LIN perm. dom.	LIN TxD perm dom.	LIN perm. rec.	CAN RxD perm rec.	CAN perm. rec.	CAN perm. dom.	CAN TxD perm dom
Group	Diagnosis 3								Diagnosis 4							

Table 99. Status register 2, bits

Bit	Name	Comment	Information storage
15	WU3_state	State of WUx input;	“Live bits” not clearable
14	WU2_state		
13	WU1_state		
12	WU3_wake	Shows wake up source (‘1’ = wake-up)	Bits are latched until a “Read and clear” access
11	WU2_wake		
10	WU1_wake		
9	WAKE_CAN		
8	WAKE_LIN		
7	Wake_TIMER_int		
6	LIN_perm_DOM	LIN bus is dominant for t > 12 ms	
5	LIN_TxD_perm_DOM	TxDL pin is dominant for t > 12 ms; Transmitter is disabled	
4	LIN_perm_REC	LIN bus does not follow TxDL within 40 µs; Transmitter is disabled	
3	CAN_RxD_perm_rec	RxDC has not followed TxDC for 4 times; Transmitter is disabled	
2	CAN_perm_REC	CAN has not followed TxDC for 4 times; Transmitter is disabled	
1	CAN_perm_DOM	CAN bus is dominant for t > 700 µs	
0	CAN_TxD_perm_DOM	TxDC pin is dominant for t > 700 µs; Transmitter is disabled	

Status register 3

Table 100. Status register 3: command and data bytes

Command byte								1st data byte	2nd data byte
Read/write		Address						Bit <15:8>	Bit<7:0>
x	x	0	1	0	0	1	1	Data, 8bit	Data, 8 bit

Table 101. Status register 3, data bytes

	1st data byte <15:8>								2nd data byte <7:0>							
Function	TSD1	TW	Device state_2	Device state_1	V_1 fail	V_1 restart_2	V_1 restart_1	V_1 restart_0	WD fail_3	WD fail_2	WD fail_1	WD fail_0	Forced sleep WD	Forced sleep TSD2 SHTV1	WD timer state_1	WD timer state_0
Group	Diagnosis 5								Diagnosis 6							

Table 102. Status register 3, bits

Bit	Name	Comment	Information storage
15	TSD1	Thermal warning / shutdown1 occurred since last readout	Bit is latched until a “read and clear access”
14	TW		
13	Device_state	State from which the device woke up	Bit is latched until a “read and clear access” after a “read and clear access”, the device state is updated after a wake up, device state is 01: V_1 standby or 10: V_{BAT} standby
12		**Device state_2** / **Device state_1** / **State from which the device woke up**: 0 / 0 / Active 0 / 1 / V_1 standby 1 / 0 / V_{BAT} standby 1 / 1 / Flash	
11	V_1_fail	V_1 fail (V_1 < 2 V for t > 2 µs) event occurred since last read out	Bit is latched until a “read and clear access”
10	V_1_restart_2	Number of TSD2 events which caused a restart of V_1 regulator (7 TSD2 events forces the device into V_{BAT} standby)	Bits are not clearable; is cleared automatically if no additional TSD2 event occurs within 1 min.
9	V_1_restart_1		
8	V_1_restart_0		
7	WD_fail_3	Number of missing watchdog triggers (15 missing watchdog trigger forces the device into V_{BAT} standby)	Bits are not clearable; is cleared with a proper Watchdog trigger
6	WD_fail_2		
5	WD_fail_1		
4	WD_fail_0		

Table 102. Status register 3, bits (continued)

<table>
<tr><th>Bit</th><th>Name</th><th>Comment</th><th>Information storage</th></tr>
<tr><td>3</td><td>Forced_sleep_WD</td><td>Device was forced to V_{BAT} standby mode because of multiple watchdog errors</td><td rowspan="2">Bits are latched until a read and clear access</td></tr>
<tr><td>2</td><td>Forced_sleep_TSD2_SHTV$_1$</td><td>Device was forced to V_{BAT} standby or multiple thermal shutdown events
or
a short on V_1 during startup.</td></tr>
<tr><td>1</td><td>WD_timer_state_1</td><td rowspan="2">Status of watchdog counter of selected watchdog timing
<table><tr><th>WD_timer_state_1</th><th>WD_timer_state_0</th><th>Counter</th></tr><tr><td>0</td><td>0</td><td>0 – 33%</td></tr><tr><td>0</td><td>1</td><td>33 – 66%</td></tr><tr><td>1</td><td>1</td><td>66 – 100%</td></tr></table></td><td rowspan="2">Bits are not clearable</td></tr>
<tr><td>0</td><td>WD_timer_state_0</td></tr>
</table>

7 Package and packing information

7.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

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7.2 PowerSSO-36 package information

Figure 39. PowerSSO-36 package dimensions

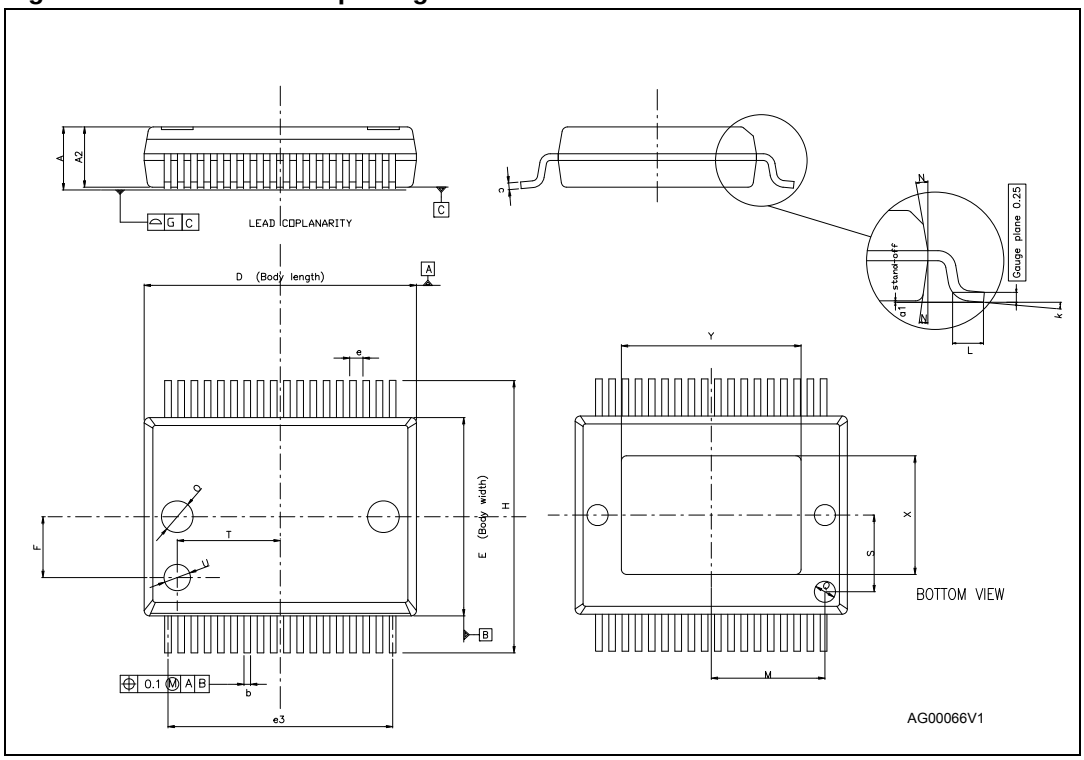

Table 103. PowerSSO-36 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.15	—	2.45
A2	2.15	—	2.35
a1	0	—	0.1
b	0.18	—	0.36
c	0.23	—	0.32
D	10.10	—	10.50
E	7.4	—	7.6
e	—	0.5	—
e3	—	8.5	—
F	—	2.3	—
G	—	—	0.1
H	10.1	—	10.5
h	—	—	0.4
k	0°	—	8°
L	0.55	—	0.85
M	—	4.3	—
N	—	-	10°
O	—	1.2	—
Q	—	0.8	—
S	—	2.9	—
T	—	3.65	—
U	—	1.0	—
X	4.1	—	4.7
Y	6.5	—	7.1

8 Revision history

Table 104. Document revision history

Date	Revision	Change
14-Dec-2009	1	Initial release.
18-Dec-2009	2	Updated *Table 5: Fail safe conditions and exit modes*. *Table 12: Supply and supply monitoring*: – Updated $I_{V(BAT)CS}$ and $I_{V(BAT)CW}$ max value from 110µA to 125µA *Table 19: Output (OUT_HS)*: – Updated t_dON min value from 10µs to 5µs. *Table 20: Outputs (OUT1...4)*: – Updated I_{OLD} min value from 1mA to 0.9mA and max value from 4mA to 4.5mA *Table 39: CSN timing*: – Added $t_{CSNfail}$ parameter.
29-Nov-2011	3	Updated footnote on *Table 21: Relay drivers* Updated *Figure 39: PowerSSO-36 package dimensions* Updated *Table 103: PowerSSO-36 mechanical data*
19-Sep-2013	4	Updated disclaimer.

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