LAN91C113

16-Bit 10/100 Non-PCI Ethernet Single Chip MAC + PHY

Datasheet

Product Features

- Single Chip Ethernet Controller
- Dual Speed - 10/100 Mbps
- Fully Supports Full Duplex Switched Ethernet
- 8 Kbytes Internal Memory for Receive and Transmit FIFO Buffers
- Enhanced Power Management Features
- Optional Configuration via Serial EEPROM Interface
- Supports 8, 16 Bit CPU Accesses
- Internal 16 Bit Wide Data Path (Into Packet Buffer Memory)
- Early TX, Early RX Functions
- Built-in Transparent Arbitration for Slave Sequential Access Architecture
- Flat MMU Architecture with Symmetric Transmit and Receive Structures and Queues
- 3.3V Operation with 5V Tolerant IO Buffers (See Pin List Description for Additional Details)
- Single 25 MHz Reference Clock for Both PHY and MAC
- External 25Mhz-output pin for an external PHY supporting PHYs physical media.
- Low Power CMOS Design
- Supports Multiple Embedded Processor Host Interfaces
  - ARM
  - SH
  - Power PC
  - Coldfire
  - 680X0, 683XX
  - MIPS R3000
- 3.3V MII (Media Independent Interface) MAC-PHY Interface Running at Nibble Rate
- MII Management Serial Interface
- 128 Pin QFP Package; Green, Lead-Free Package also available
- 128 Pin TQFP Package, 1.0 mm height; Green, Lead-Free Package also available
- Temperature Range from 0°C to 85°C

Network Interface

- Fully Integrated IEEE 802.3/802.3u-100Base-TX / 10Base-T Physical Layer
- Auto Negotiation: 10/100, Full / Half Duplex
- On Chip Wave Shaping - No External Filters Required
- Adaptive Equalizer
- Baseline Wander Correction
- LED Outputs (User selectable – Up to 2 LED functions at one time)
  - Link
  - Activity
  - Full Duplex
  - 10/100
  - Transmit
  - Receive

ORDERING INFORMATION

Order Number(s):

LAN91C113-NC for 128 Pin QFP Package
LAN91C113-NE for 128 Pin TQFP Package (1.0 mm height)
LAN91C113-NS for 128 Pin QFP Package (Green, Lead-Free)
LAN91C113-NU for 128 Pin TQFP Package (1.0 mm height) (Green, Lead-Free)

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Chapter 1 General Description

The SMSC LAN91C113 is designed to facilitate the implementation of a third generation of Fast Ethernet connectivity solutions for embedded applications. For this third generation of products, flexibility and integration dominate the design requirements. The LAN91C113 is a mixed signal Analog/Digital device that implements the MAC and PHY portion of the CSMA/CD protocol at 10 and 100 Mbps. The design will also minimize data throughput constraints utilizing a 16-bit or 8-bit bus Host interface in embedded applications.

The total internal memory FIFO buffer size is 8 Kbytes, which is the total chip storage for transmit and receive operations.

The SMSC LAN91C113 is software compatible with the LAN9000 family of products.

Memory management is handled using a patented optimized MMU (Memory Management Unit) architecture and a 16-bit wide internal data path. This I/O mapped architecture can sustain back-to-back frame transmission and reception for superior data throughput and optimal performance. It also dynamically allocates buffer memory in an efficient buffer utilization scheme, reducing software tasks and relieving the host CPU from performing these housekeeping functions.

The SMSC 91C113 provides a flexible slave interface for easy connectivity with industry-standard buses. The Bus Interface Unit (BIU) can handle synchronous as well as asynchronous transfers, with different signals being used for each one. Asynchronous bus support for ISA is supported even though ISA cannot sustain 100 Mbps traffic. Fast Ethernet data rates are attainable for ISA-based nodes on the basis of the aggregate traffic benefits.

Two different interfaces are supported on the network side. The first Interface is a standard Magnetics transmit/receive pair interfacing to 10/100Base-T utilizing the internal physical layer block. The second interface follows the MII (Media Independent Interface) specification standard, consisting of 4 bit wide data transfers at the nibble rate. This interface is applicable to 10 Mbps standard Ethernet or 100 Mbps Ethernet networks. Three of the LAN91C113's pins are used to interface to the two-line MII serial management protocol.

The SMSC LAN91C113 integrates IEEE 802.3 Physical Layer for twisted pair Ethernet applications. The PHY can be configured for either 100 Mbps (100Base-TX) or 10 Mbps (10Base-T) Ethernet operation. The Analog PHY block consists of a 4B5B/Manchester encoder/decoder, scrambler/de-scrambler, transmitter with wave shaping and output driver, twisted pair receiver with on chip equalizer and baseline wander correction, clock and data recovery, Auto-Negotiation, controller interface (MII), and serial port (MI). Internal output wave shaping circuitry and on-chip filters eliminate the need for external filters normally required in 100Base-TX and 10Base-T applications.

The LAN91C113 can automatically configure itself for 100 or 10 Mbps and Full or Half Duplex operation with the on-chip Auto-Negotiation algorithm. The LAN91C113 is ideal for media interfaces for embedded application desiring Ethernet connectivity as well as 100Base-TX/10Base-T adapter cards, motherboards, repeaters, switching hubs. The LAN91C113 operates from a single 3.3V supply. The inputs and outputs of the host Interface are 5V tolerant and will directly interface to other 5V devices.

Chapter 2 Pin Configurations

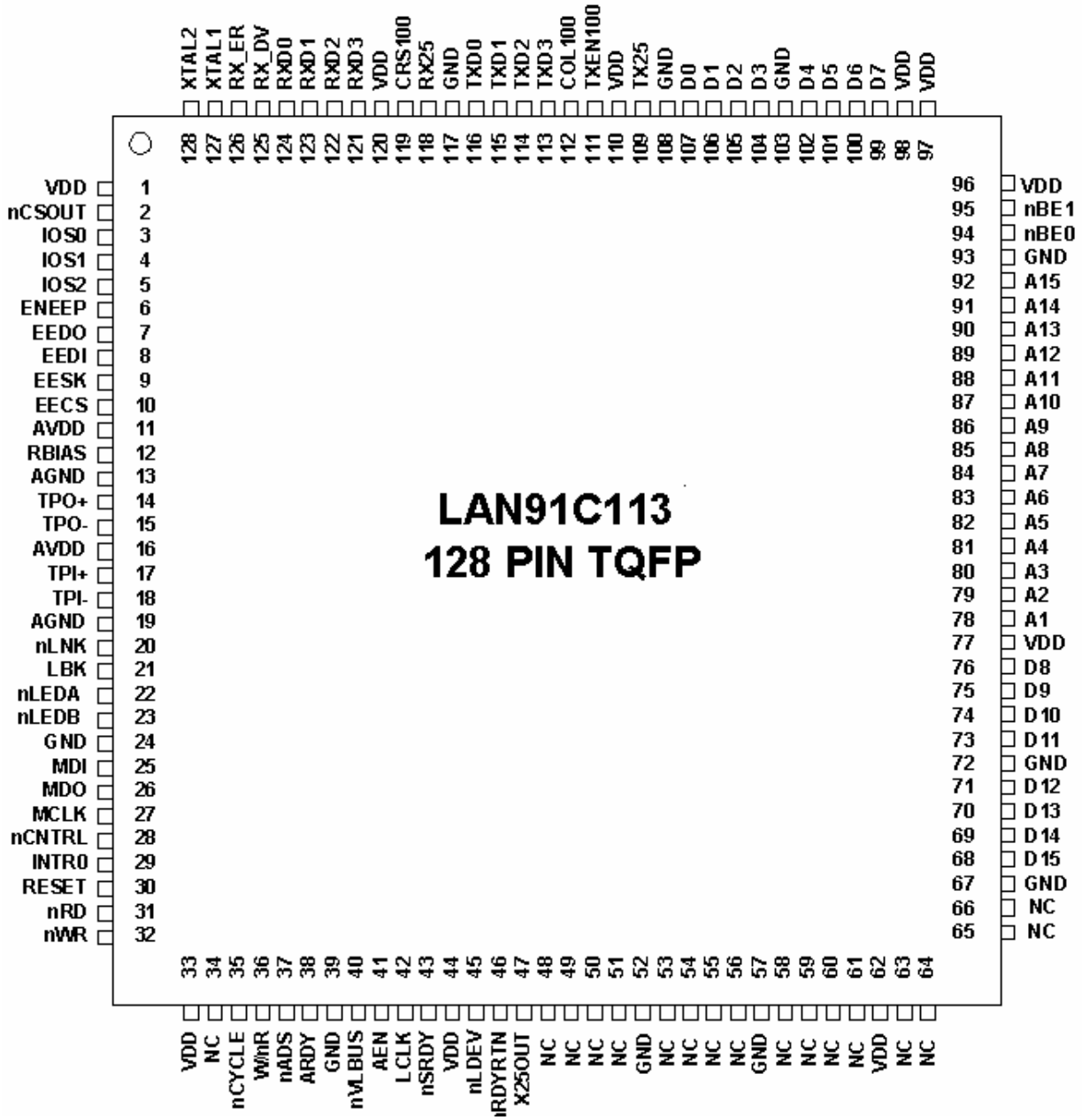


Figure 2.1 - Pin Configuration - LAN91C113 128 Pin TQFP

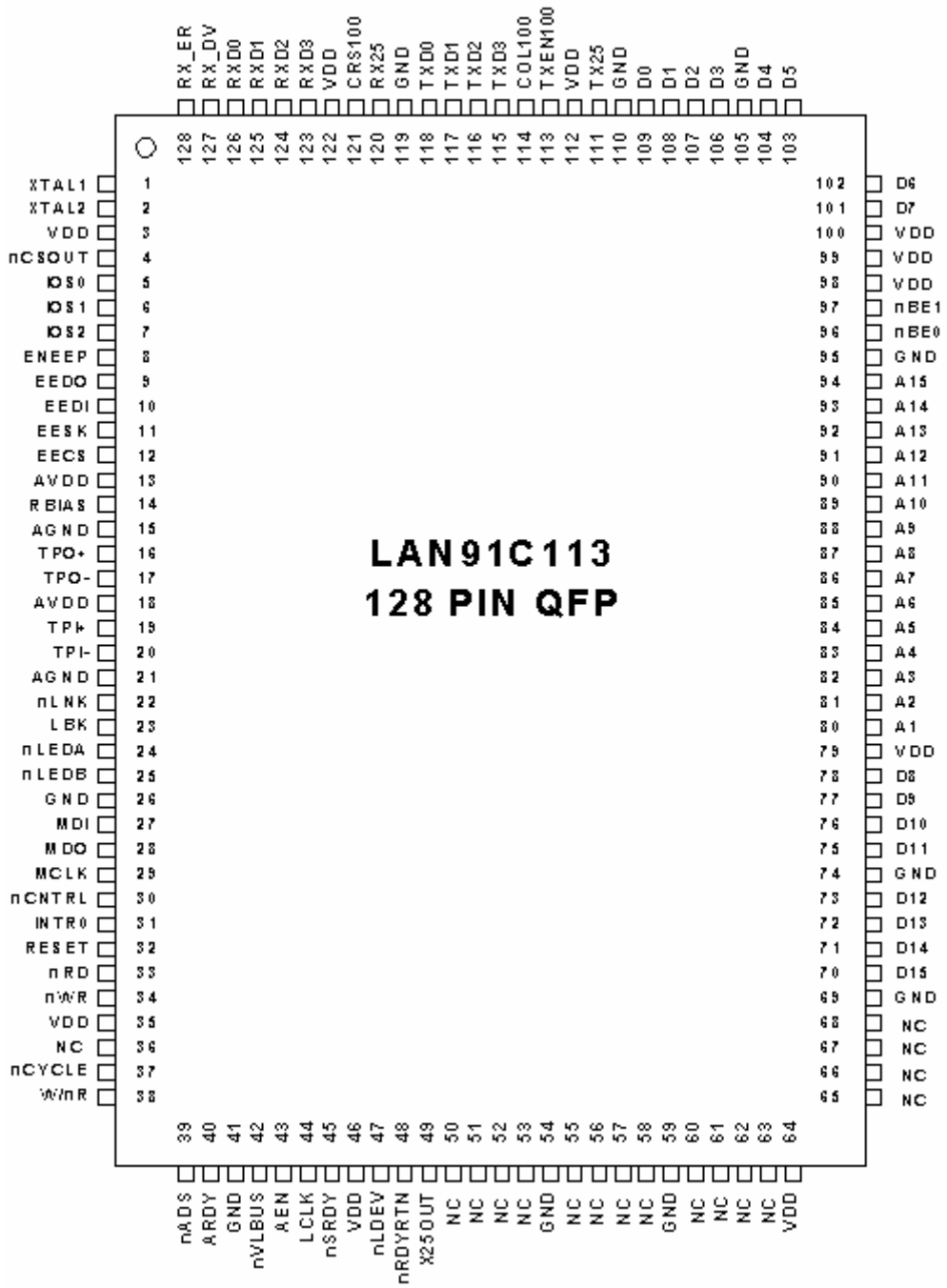


Figure 2.2 - Pin Configuration - LAN91C113 128 Pin QFP

Chapter 3 Block Diagrams

The diagram shown in Figure 3.1 - LAN91C113 - Basic Functional Block Diagram, describes the device basic functional blocks. The SMSC LAN91C113 is a single chip solution for embedded designs with minimal Host and external supporting devices required to implement 10/100 Ethernet connectivity solutions.

The optional Serial EEPROM is used to store information relating to default IO offset parameters as well as which of the Interrupt line are used by the host.

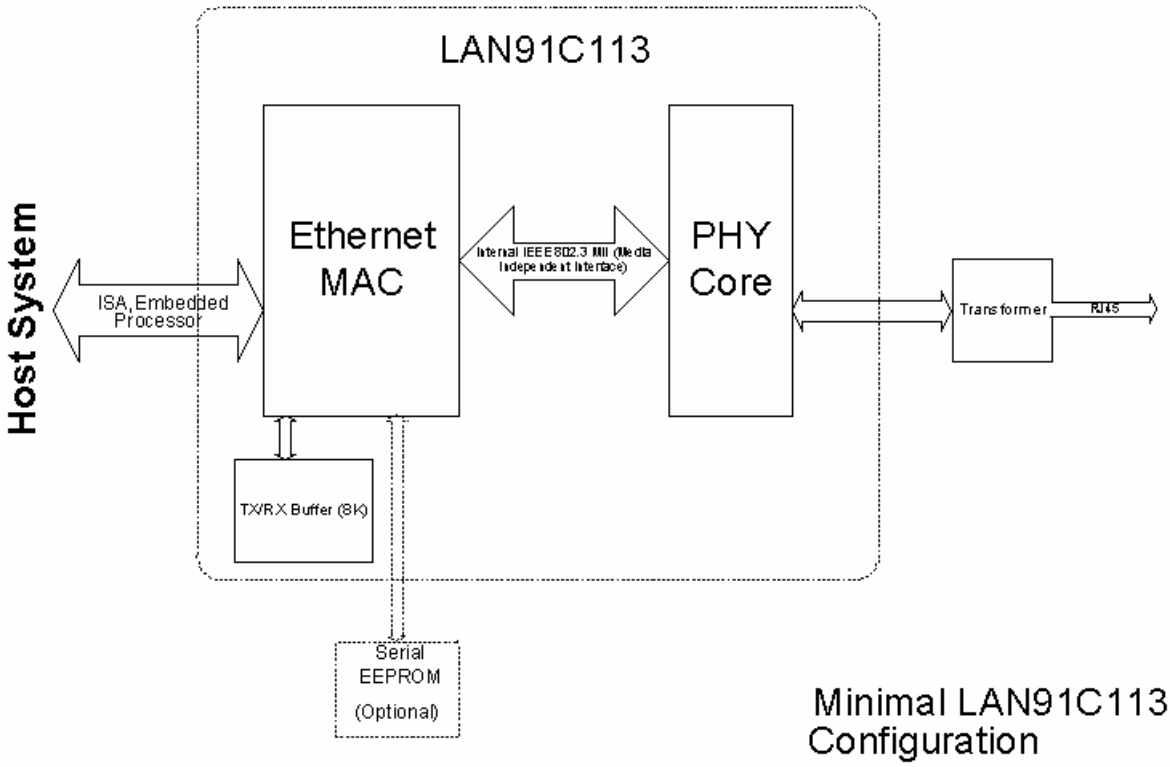


Figure 3.1 - LAN91C113 - Basic Functional Block Diagram

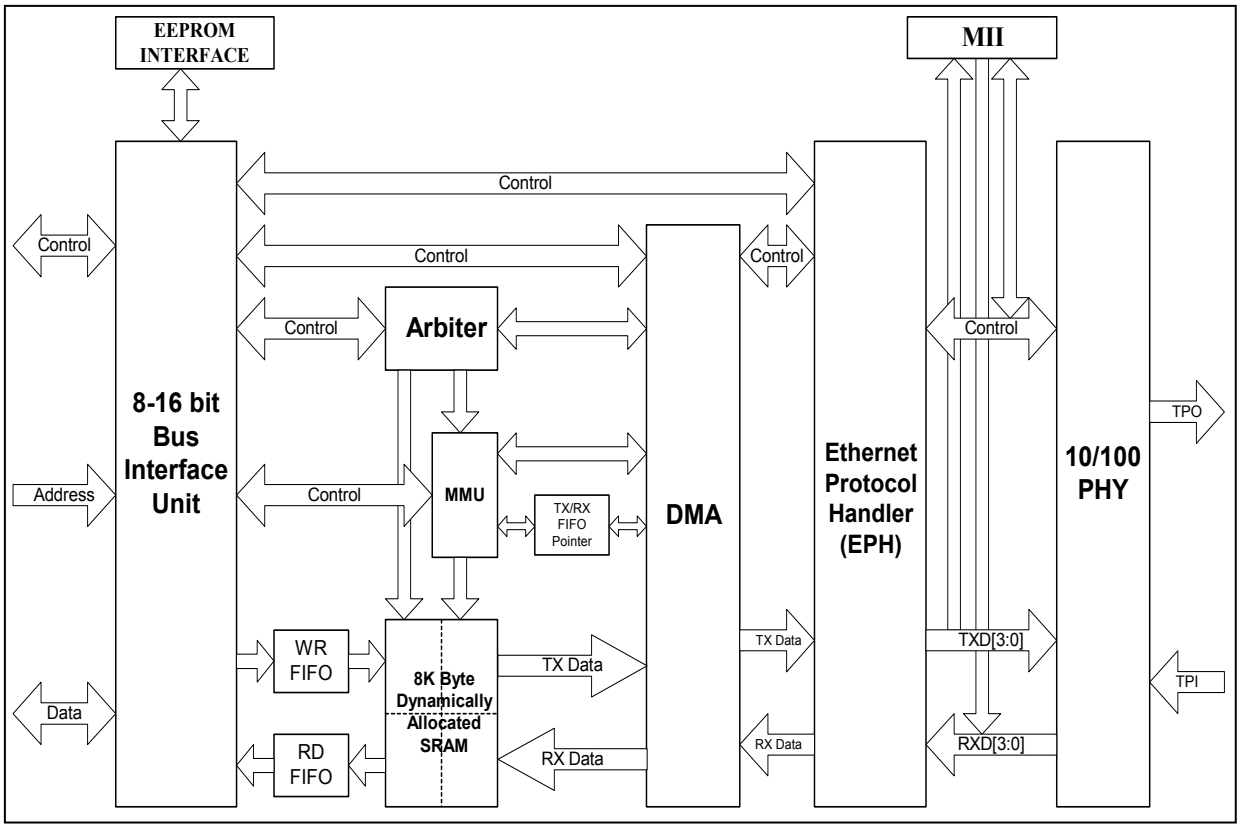


Figure 3.2 - Block Diagram

The diagram shown in Figure 3.2 describes the supported Host interfaces, which include ISA or Generic Embedded. The Host interface is an 8 or 16 bit wide address / data bus with extensions for embedded RISC and ARM processors.

The figure shown next page describes the SMSC LAN91C113 functional blocks required to integrate a 10/100 Ethernet Physical layer framer to the internal MAC.

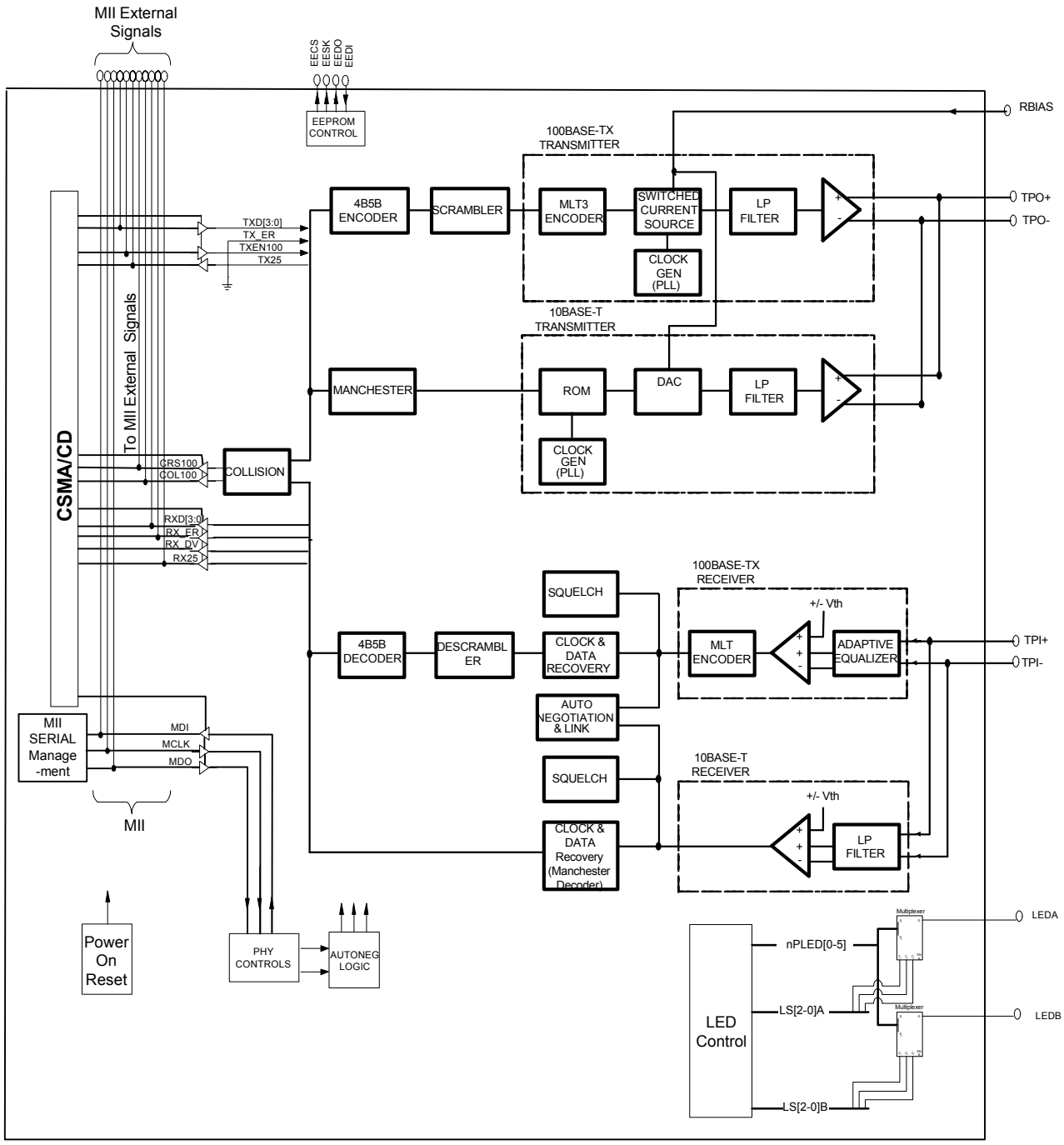


Figure 3.3 - LAN91C113 Physical Layer to Internal Mac Block Diagram

Chapter 4 Signal Descriptions

Table 4.1 - LAN91C113 Pin Requirements (128 Pin QFP and 1.0mm TQFP package)

FUNCTION	PIN SYMBOLS	NUMBER OF PINS
System Address Bus	A1-A15, AEN, nBE0, nBE1	18
System Data Bus	D0-D15	16
System Control Bus	RESET, nADS, LCLK, ARDY, nRDYRTN, nSRDY, INTR0, nLDEV, nRD, nWR, nCYCLE, W/nR, nVLBUS	13
Serial EEPROM	EEDI, EEDO, EECS, EESK, ENEEP, IOS0-IOS2	8
LEDs	nLEDA, nLEDB	2
PHY	TPO+, TPO-, TPI+, TPI-, nLNK, LBK, nCNTRL, RBIAS	8
Crystal Oscillator	XTAL1, XTAL2	2
Power	VDD, AVDD	29
Ground	GND, AGND	12
Physical Interface 100 Mbps	TXEN100, CRS100, COL100, RX_DV, RX_ER, TXD0-TXD3, RXD0-RXD3, MDI, MDO, MCLK, RX25, TX25	18
MISC	nCSOUT, X25OUT,	2
TOTAL		128

Chapter 5 Description of Pin Functions

PIN NO.		NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
TQFP	QFP				
81-92	83-94	Address	A4-A15	I**	Input. Decoded by LAN91C113 to determine access to its registers.
78-80	80-82	Address	A1-A3	I**	Input. Used by LAN91C113 for internal register selection.
41	43	Address Enable	AEN	I**	Input. Used as an address qualifier. Address decoding is only enabled when AEN is low.
94-95	96-97	nByte Enable	nBE0-nBE1	I**	Input. Used during LAN91C113 register accesses to determine the width of the access and the register(s) being accessed.
107-104, 102-99, 76-73, 71-68	109-106, 104-101, 78-75, 73-70	Data Bus	D0-D15	I/O24**	Bidirectional. 16 bit data bus used to access the LAN91C113's internal registers. Data bus has weak internal pullups. Supports direct connection to the system bus without external buffering.
30	32	Reset	RESET	IS**	Input. When this pin is asserted high, the controller performs an internal system (MAC & PHY) reset. It programs all the registers to their default value, the controller will read the EEPROM device through the EEPROM interface. **(Note 5.1)** This input is not considered active unless it is active for at least 100ns to filter narrow glitches.
37	39	nAddress Strobe	nADS	IS**	Input. For systems that require address latching, the rising edge of nADS indicates the latching moment for A1-A15 and AEN. All LAN91C113 internal functions of A1-A15, AEN are latched except for nLDEV decoding.
35	37	nCycle	nCYCLE	I**	Input. This active low signal is used to control LAN91C113 synchronous bus cycles. For write operation, this signal should be asserted one bus clock prior to data valid. For read operation, this signal should be asserted two bus clocks prior to data valid.
36	38	Write/ nRead	W/nR	IS**	Input. Defines the direction of synchronous cycles. Write cycles when high, read cycles when low.

PIN NO.		NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
TQFP	QFP				
40	42	nVL Bus Access	nVLBUS	I with pullup**	Input. When low, the LAN91C113 synchronous bus interface is configured for Local Bus mode accesses. Otherwise, the LAN91C113 is configured for EISA accesses. Does not affect the asynchronous bus interface.
42	44	Local Bus Clock	LCLK	I**	Input. Used to interface synchronous buses. Maximum frequency is 50 MHz. This pin should be tied high if it is in asynchronous mode.
38	40	Asynchronous Ready	ARDY	OD16	Open drain output. ARDY may be used when interfacing asynchronous buses to extend accesses. Its rising (access completion) edge is controlled by the XTAL1 clock and, therefore, asynchronous to the host CPU or bus clock.
43	45	nSynchronous Ready	nSRDY	O16	Output. This output is used when interfacing synchronous buses and nVLBUS=0 to extend accesses. This signal remains normally inactive, and its falling edge indicates completion. This signal is synchronous to the bus clock LCLK.
46	48	nReady Return	nRDYRTN	I**	Input. This input is used to complete synchronous read cycles.
29	31	Interrupt	INTR0	O24	Interrupt Output – Active High, it's used to interrupt the Host on a status event. Note: The selection bits used to determined by the value of INT SEL 1-0 bits in the Configuration Register are no longer required and have been set to reserved in this revision of the FEAST family of devices.
45	47	nLocal Device	nLDEV	O16	Output. This active low output is asserted when AEN is low and A4-A15 decode to the LAN91C113 address programmed into the high byte of the Base Address Register. nLDEV is a combinatorial decode of unlatched address and AEN signals.
31	33	nRead Strobe	nRD	IS**	Input. Used in asynchronous bus interfaces.
32	34	nWrite Strobe	nWR	IS**	Input. Used in asynchronous bus interfaces.
9	11	EEPROM Clock	EESK	O4	Output. 4 μsec clock used to shift data in and out of the serial EEPROM.
10	12	EEPROM Select	EECS	O4	Output. Serial EEPROM chip select. Used for selection and command framing of the serial EEPROM.

PIN NO.		NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
TQFP	QFP				
7	9	EEPROM Data Out	EEDO	O4	Output. Connected to the DI input of the serial EEPROM.
8	10	EEPROM Data In	EEDI	I with pulldown **	Input. Connected to the DO output of the serial EEPROM.
3-5	5-7	I/O Base	IOS0-IOS2	I with pullup**	Input. External switches can be connected to these lines to select between predefined EEPROM configurations.
6	8	Enable EEPROM	ENEEP	I with pullup**	Input. Enables (when high or open) LAN91C113 accesses to the serial EEPROM. Must be grounded if no EEPROM is connected to the LAN91C113.
127, 128	1, 2	Crystal 1 Crystal 2	XTAL1 XTAL2	Iclk	An external 25 MHz crystal is connected across these pins. If a TTL clock is supplied instead, it should be connected to XTAL1 and XTAL2 should be left open.
1, 33, 44, 62, 77, 98, 110, 120, 96, 97	3, 35, 46, 64, 79, 100, 112, 122, 98, 99	Power	VDD		+3.3V Power supply pins.
11, 16	13, 18	Analog Power	AVDD		+3.3V Analog power supply pins.
24, 39, 52, 57, 67, 72, 93, 103, 108, 117	26, 41, 54, 59, 69, 74, 95, 105, 110, 119	Ground	GND		Ground pins.
13, 19	15, 21	Analog Ground	AGND		Analog Ground pins
21	23	Loopback	LBK	O4	Output. Active when LOOP bit is set (TCR bit 1).
20	22	nLink Status	nLNK	I with pullup	Input. General-purpose input port used to convey LINK status (EPHSR bit 14).
28	30	nCNTRL	nCNTRL	O12	General Purpose Control Pin
47	49	X25out	X25out	O12	25Mhz Output to external PHY
111	113	Transmit Enable 100 Mbps	TXEN100	O12	Output to MII PHY. Envelope to 100 Mbps transmission.
119	121	Carrier Sense 100 Mbps	CRS100	I with pulldown	Input from MII PHY. Envelope of packet reception used for deferral and backoff purposes.
125	127	Receive Data Valid	RX_DV	I with pulldown	Input from MII PHY. Envelope of data valid reception. Used for receive data framing.
112	114	Collision Detect 100 Mbps	COL100	I with pulldown	Input from MII PHY. Collision detection input.

PIN NO.		NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
TQFP	QFP				
113-116	115-118	Transmit Data	TXD3-TXD0	O12	Outputs. Transmit Data nibble to MII PHY.
109	111	Transmit Clock	TX25	I with pullup	Input. Transmit clock input from MII. Nibble rate clock (25MHz for 100Mbps & 2.5MHz for 10Mbps).
118	120	Receive Clock	RX25	I with pullup	Input. Receive clock input from MII PHY. Nibble rate clock. (25MHz for 100Mbps & 2.5MHz for 10Mbps).
121-124	123-126	Receive Data	RXD3-RXD0	I with pullup	Inputs. Received Data nibble from MII PHY.
25	27	Management Data Input	MDI	I with pulldown	MII management data input.
26	28	Management Data Output	MDO	O4	MII management data output.
27	29	Management Clock	MCLK	O4	MII management clock.
126	128	Receive Error	RX_ER	I with pulldown	Input. Indicates a code error detected by PHY. Used by the LAN91C113 to discard the packet being received. The error indication reported for this event is the same as a bad CRC (Receive Status Word bit 13).
2	4	nChip Select Output	nCSOUT	O4	Output. Chip Select provided for mapping of PHY functions into LAN91C113 decoded space. Active on accesses to LAN91C113's eight lower addresses when the BANK SELECTED is 7.
12	14	External Resistor	RBIAS	NA	Transmit Current Set. An external resistor connected between this pin and GND will set the output current for the TP transmit outputs
14	16		TPO+	O/I	Twisted Pair Transmit Output, Positive.
15	17		TPO-	O/I	Twisted Pair Transmit Output, Negative
17	19		TPI+	I/O	Twisted Pair Receive Input, Positive
18	20		TPI-	I/O	Twisted Pair Receive Input, Negative.
22	24		nLEDA	OD24	PHY LED Output
23	25		nLEDB	OD24	PHY LED Output
34, 48-51, 53-56, 58-61, 63-66	36, 50-53, 55-58, 60-63, 65-68		NC		No Connection

Note 5.1 If the EEPROM is enabled.

5.1 Signal Description Parameters

This section provides a detailed description of each SMSC LAN91C113 signal. The signals are arranged in functional groups according to their associated function.

The 'n' symbol at the beginning of a signal name indicates that it is an active low signal. When 'n' is not present before the signal name, it indicates an active high signal.

The term "assert" or "assertion" indicates that a signal is active; independent of whether that level is represented by a high or low voltage. The term negates or negation indicates that a signal is inactive.

The term High-Z means tri-stated.

The term Undefined means the signal could be high, low, tri-stated, or in some in-between level.

5.2 Buffer Types

O4	Output buffer with 2mA source and 4mA sink
O12	Output buffer with 6mA source and 12mA sink
O16	Output buffer with 8mA source and 16mA sink
O24	Output buffer with 12mA source and 24mA sink
OD16	Open drain buffer with 16mA sink
OD24	Open drain buffer with 24mA sink
I/O4	Bidirectional buffer with 2mA source and 4mA sink
I/O24	Bidirectional buffer with 12mA source and 24mA sink
I/OD	Bidirectional Open drain buffer with 4mA sink
I	Input buffer
IS	Input buffer with Schmitt Trigger Hysteresis
Iclk	Clock input buffer
I/O	Differential Input
O/I	Differential Output
**	5V tolerant. Input pins are able to accept 5V signals

DC levels and conditions defined in the DC Electrical Characteristics section.

Chapter 6 Functional Description

6.1 Clock Generator Block

1) The XTAL1 and XTAL2 pins are to be connected to a 25 MHz crystal.

2) TX25 is an input clock. It will be the nibble rate of the particular PHY connected to the MII (2.5 MHz for a 10 Mbps PHY, and 25 MHz for a 100 Mbps PHY).

3) RX25 - This is the MII nibble rate receive clock used for sampling received data nibbles and running the receive state machine. (2.5 MHz for a 10 Mbps PHY, and 25 MHz for a 100 Mbps PHY).

4) LCLK - Bus clock - Used by the BIU for synchronous accesses. Maximum frequency is 50 MHz for VL BUS mode, and 8.33 MHz for EISA slave DMA.

6.2 CSMA/CD Block

This is a 16 bit oriented block, with fully- independent Transmit and Receive logic. The data path in and out of the block consists of two 16-bit wide uni-directional FIFOs interfacing the DMA block. The DMA port of the FIFO stores 32 bits to exploit the 32 bit data path into memory, but the FIFOs themselves are 16 bit wide. The Control Path consists of a set of registers interfaced to the CPU via the BIU.

6.2.1 DMA Block

This block accesses packet memory on the CSMA/CD's behalf, fetching transmit data and storing received data. It interfaces the CSMA/CD Transmit and Receive FIFOs on one side and the Arbiter block on the other. To increase the bandwidth into memory, a 50 MHz clock is used by the DMA block, and the data path is 32 bits wide.

For example, during active reception at 100 Mbps, the CSMA/CD block will write a word into the Receive FIFO every 160ns. The DMA will read the FIFO and accumulate two words on the output port to request a memory cycle from the Arbiter every 320ns.

The DMA machine is able to support full duplex operation. Independent receive and transmit counters are used. Transmit and receive cycles are alternated when simultaneous receive and transmit accesses are needed.

6.2.2 Arbiter Block

The Arbiter block sequences accesses to packet RAM requested by the BIU and by the DMA blocks. BIU requests represent pipelined CPU accesses to the Data Register, while DMA requests represent CSMA/CD data movement.

Internal SRAM read accesses are always 32 bit wide, and the Arbiter steers the appropriate byte(s) to the appropriate lanes as a function of the address.

The CPU Data Path consists of two uni-directional FIFOs mapped at the Data Register location. These FIFOs can be accessed in any combination of bytes or word. The Arbiter will indicate 'Not Ready' whenever a cycle is initiated that cannot be satisfied by the present state of the FIFO.

6.3 MMU Block

The Hardware Memory Management Unit allocates memory and transmit and receive packet queues. It also determines the value of the transmit and receive interrupts as a function of the queues. The page size is 2048 bytes, with a maximum memory size of 8kbytes. MIR values are interpreted in 2048 byte units.

6.4 BIU Block

The Bus Interface Unit can handle synchronous as well as asynchronous buses; different signals are used for each one. Transparent latches are added on the address path using rising nADS for latching.

When working with an asynchronous bus like ISA, the read and write operations are controlled by the edges of nRD and nWR. ARDY is used for notifying the system that it should extend the access cycle. The leading edge of ARDY is generated by the leading edge of nRD or nWR while the trailing edge of ARDY is controlled by the internal LAN91C113 clock and, therefore, asynchronous to the bus.

In the synchronous VL Bus type mode, nCYCLE and LCLK are used to for read and write operations. Completion of the cycle may be determined by using nSRDY. nSRDY is controlled by LCLK and synchronous to the bus.

The BIU is implemented using the following principles:

1) Address decoding is based on the values of A15-A4 and AEN.
2) Address latching is performed by using transparent latches that are transparent when nADS=0 and nRD=1, nWR=1 and latch on nADS rising edge.
3) Byte and word accesses to all registers and Data Path are supported.
4) No bus byte swapping is implemented (no eight bit mode).
5) Word swapping as a function of A1 is implemented for 16 bit bus support.
6) The asynchronous interface uses nRD and nWR strobes. If necessary, ARDY is negated on the leading edge of the strobe. The ARDY trailing edge is controlled by CLK.
7) The VLBUS synchronous interface uses LCLK, nADS, and W/nR as defined in the VESA specification as well as nCYCLE to control read and write operations and generate nSRDY.
8) Synchronous and asynchronous cycles can be mixed as long as they are not active simultaneously.

6.5 MAC-PHY Interface

The LAN91C113 integrates the IEEE 802.3 Physical Layer (PHY) and Media Access Control (MAC) into the same silicon. The data path connection between the MAC and the internal PHY is provided by the internal MII. The LAN91C113 also supports the EXT_PHY mode for the use of an external PHY, such as HPNA. This mode isolates the internal PHY to allow interface with an external PHY through the MII pins. To enter this mode, set EXT PHY bit to 1 in the Configuration Register.

6.5.1 Management Data Software Implementation

The MII interface contains of a pair of signals that physically transport the management information across the MII, a frame format and a protocol specification for exchanging management frames, and a register set that can be read and written using these frames. MII management refers to the ability of a management entity to communicate with PHY via the MII serial management interface (MI) for the purpose of displaying, selecting and/or controlling different PHY options. The host manipulates the MAC to drive the MII management serial interface. By manipulating the MAC's registers, MII management frames are

generated on the management interface for reading or writing information from the PHY registers. Timing and framing for each management command is to be generated by the CPU (host).

The MAC and external PHY communicate via MDIO and MDC of the MII Management serial interface.

MDIO: Management Data input/output. Bi-directional between MAC and PHY that carries management data. All control and status information sent over this pin is driven and sampled synchronously to the rising edge of MDC signal.

MDC: Management Data Clock. Sourced by the MAC as a timing reference for transfer of information on the MDIO signal. MDC is a periodic signal with no maximum high or low times. The minimum high and low times should be 160ns each and the minimum period of the signal should be 400ns. These values are regardless of the nominal period of the TX and RX clocks.

6.5.2 Management Data Timing

A timing diagram for a MI serial port frame is shown in Figure 6.1. The MI serial port is idle when at least 32 continuous 1's are detected on MDIO and remains idle as long as continuous 1's are detected. During idle, MDIO is in the high impedance state. When the MI serial port is in the idle state, a 01 pattern on the MDIO initiates a serial shift cycle. Data on MDIO is then shifted in on the next 14 rising edges of MDC (MDIO is high impedance). If the register access mode is not enabled, on the next 16 rising edges of MDC, data is either shifted in or out on MDIO, depending on whether a write or read cycle was selected with the bits READ and WRITE. After the 32 MDC cycles have been completed, one complete register has been read/written, the serial shift process is halted, data is latched into the device, and MDIO goes into high impedance state. Another serial shift cycle cannot be initiated until the idle condition (at least 32 continuous 1's) is detected.

6.5.3 MI Serial Port Frame Structure

The structure of the PHY serial port frame is shown in Table 8.1 and timing diagram of a frame is shown in Figure 6.1. Each serial port access cycle consists of 32 bits (or 192 bits if multiple register access is enabled and REGAD[4:0]=11111), exclusive of idle. The first 16 bits of the serial port cycle are always write bits and are used for addressing. The last 16/176 bits are from one/all of the 11 data registers.

The first 2 bits in Table 8.1 and Figure 6.1 are start bits and need to be written as a 01 for the serial port cycle to continue. The next 2 bits are a read and write bit which determine if the accessed data register bits will be read or write. The next 5 bits are device addresses. The next 5 bits are register address select bits, which select one of the five data registers for access. The next 2 bits are the turnaround bits which are not actual register bits but extra time to switch MDIO from write to read if necessary, as shown in Figure 6.1. The final 16 bits of the PHY MI serial port cycle (or 176 bits if multiple register access is enabled and REGAD[4:0]=11111) come from the specific data register designated by the register address bits REGAD[4:0].

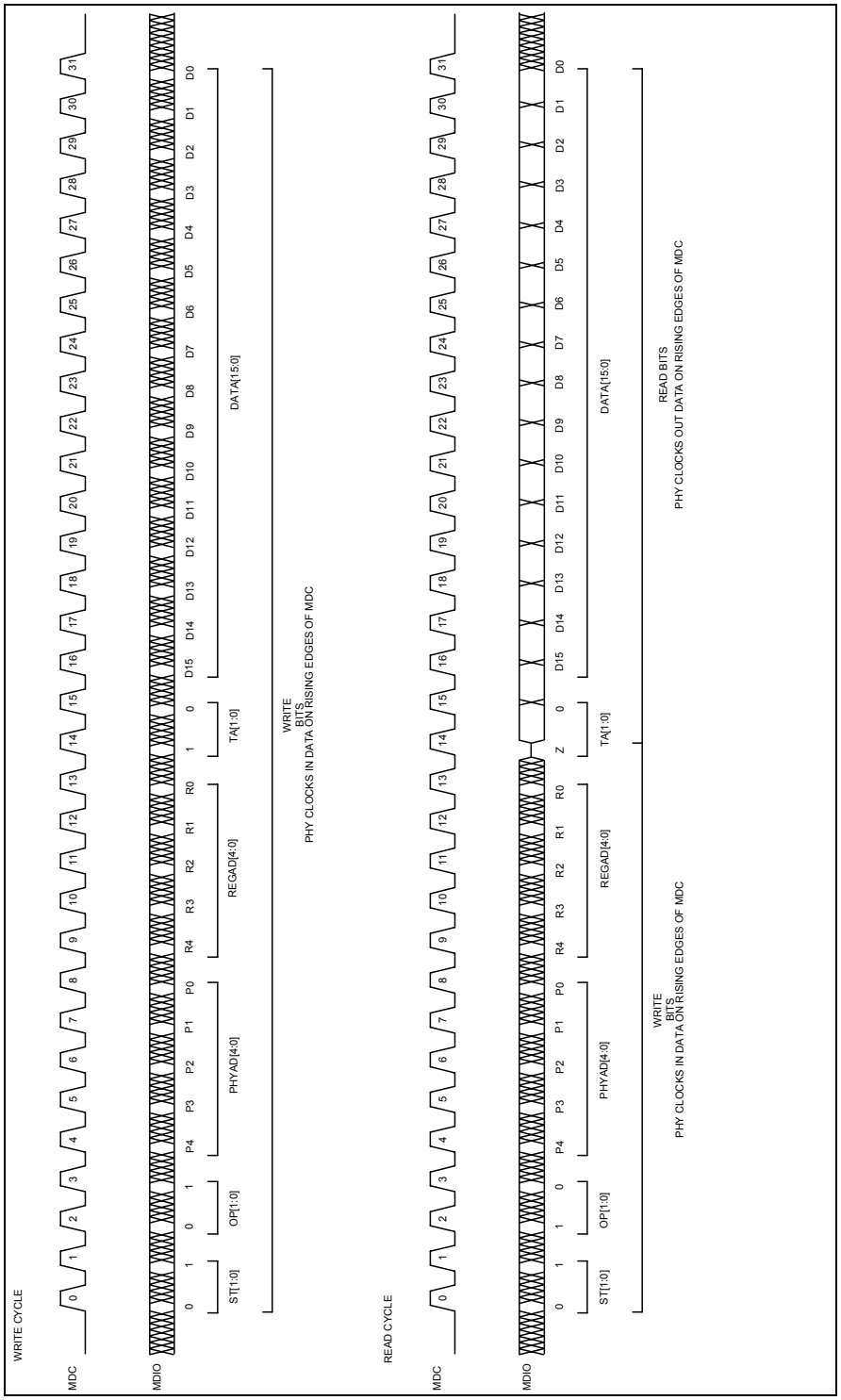


Figure 6.1 - MI Serial Port Frame Timing Diagram

6.5.4 MII Packet Data Communication with External PHY

The MII is a nibble wide packet data interface defined in IEEE 802.3. The LAN91C113 meets all the MII requirements outlined in IEEE 802.3 and shown in Figure 6.2.

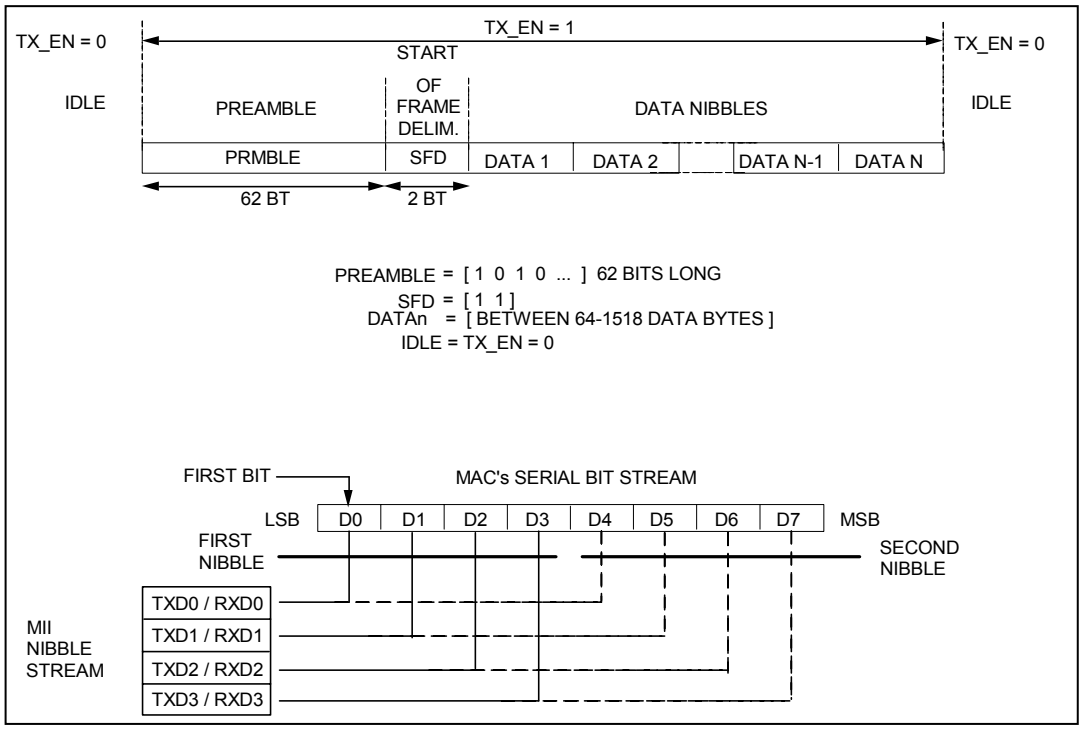


Figure 6.2 - MII Frame Format & MII Nibble Order

The MII consists of the following signals: four transmit data bits (TXD[3:0]), transmit clock (TX25),transmit enable (TXEN100), four receive data bits(RXD[3:0]), receive clock(RX25), carrier sense (CRS100), receive data valid (RX_DV), receive data error (RX_ER), and collision (COL100). Transmit data is clocked out using the TX25 clock input, while receive data is clocked in using RX25. The transmit and receive clocks operate at 25 MHz in 100Mbps mode and 2.5 MHz in 10Mbps.

In 100 Mbps mode, the LAN91C113 provides the following interface signals to the PHY:

- For transmission: TXEN100, TXD0-3, TX25
- For reception: RX_DV, RX_ER RXD0-3, RX25
- For CSMA/CD state machines: CRS100, COL100

A transmission begins by TXEN100 going active (high), and TXD0-TXD3 having the first valid preamble nibble. TXD0 carries the least significant bit of the nibble (that is the one that would go first out of the EPH at 100 Mbps), while TXD3 carries the most significant bit of the nibble. TXEN100 and TXD0-TXD3 are clocked by the LAN91C113 using TX25 rising edges. TXEN100 goes inactive at the end of the packet on the last nibble of the CRC.

During a transmission, COL100 might become active to indicate a collision. COL100 is asynchronous to the LAN91C113's clocks and will be synchronized internally to TX25.

Reception begins when RX_DV (receive data valid) is asserted. A preamble pattern or flag octet will be present at RXD0-RXD3 when RX_DV is activated. The LAN91C113 requires no training sequence beyond a full flag octet for reception. RX_DV as well as RXD0-RXD3 are sampled on RX25 rising edges. RXD0

carries the least significant bit and RXD3 the most significant bit of the nibble. RX_DV goes inactive when the last valid nibble of the packet (CRC) is presented at RXD0-RXD3.

RX_ER might be asserted during packet reception to signal the LAN91C113 that the present receive packet is invalid. The LAN91C113 will discard the packet by treating it as a CRC error.

RXD0-RXD3 should always be aligned to packet nibbles, therefore, opening flag detection does not consider misaligned cases. Opening flag detection expects the 5Dh pattern and will not reject the packet on non-preamble patterns.

CRS100 is used as a frame envelope signal for the CSMA/CD MAC state machines (deferral and backoff functions), but it is not used for receive framing functions. CRS100 is an asynchronous signal and it will be active whenever there is activity on the cable, including LAN91C113 transmissions and collisions.

6.6 Serial EEPROM Interface

This block is responsible for reading the serial EEPROM upon hardware reset (or equivalent command) and defining defaults for some key registers. A write operation is also implemented by this block, that under CPU command will program specific locations in the EEPROM. This block is an autonomous state machine and controls the internal Data Bus of the LAN91C113 during active operation.

6.7 Internal Physical Layer

The LAN91C113 integrates the IEEE 802.3 physical layer (PHY) internally. The EXT PHY bit in the Configuration Register is 0 as the default configuration to set the internal PHY enabled. The internal PHY address is 00000, the driver must use this address to talk to the internal PHY. The internal PHY is placed in isolation mode at power up and reset. It can be removed from isolation mode by clearing the MII_DIS bit in the PHY Control Register. If necessary, the internal PHY can be enabled by clearing the EXT_PHY bit in the Configuration Register.

The internal PHY of LAN91C113 has nine main sections: controller interface, encoder, decoder, scrambler, descrambler, clock and data recovery, twisted pair transmitter, twisted pair receiver, and MI serial port.

The LAN91C113 can operate as a 100BASE-TX device (hereafter referred to as 100Mbps mode) or as a 10BASE-T device (hereafter referred to as 10Mbps mode). The difference between the 100Mbps mode and the 10Mbps mode is data rate, signaling protocol, and allowed wiring. The 100Mbps TX mode uses two pairs of category 5 or better UTP or STP twisted pair cable with 4B5B encoded, scrambled, and MLT-3 coded 62.5 MHz ternary data to achieve a throughput of 100Mbps. The 10Mbps mode uses two pairs of category 3 or better UTP or STP twisted pair cable with Manchester encoded, 10MHz binary data to achieve a 10Mbps throughput. The data symbol format on the twisted pair cable for the 100 and 10Mbps modes are defined in IEEE 802.3 specifications and shown in Figure 6.3.

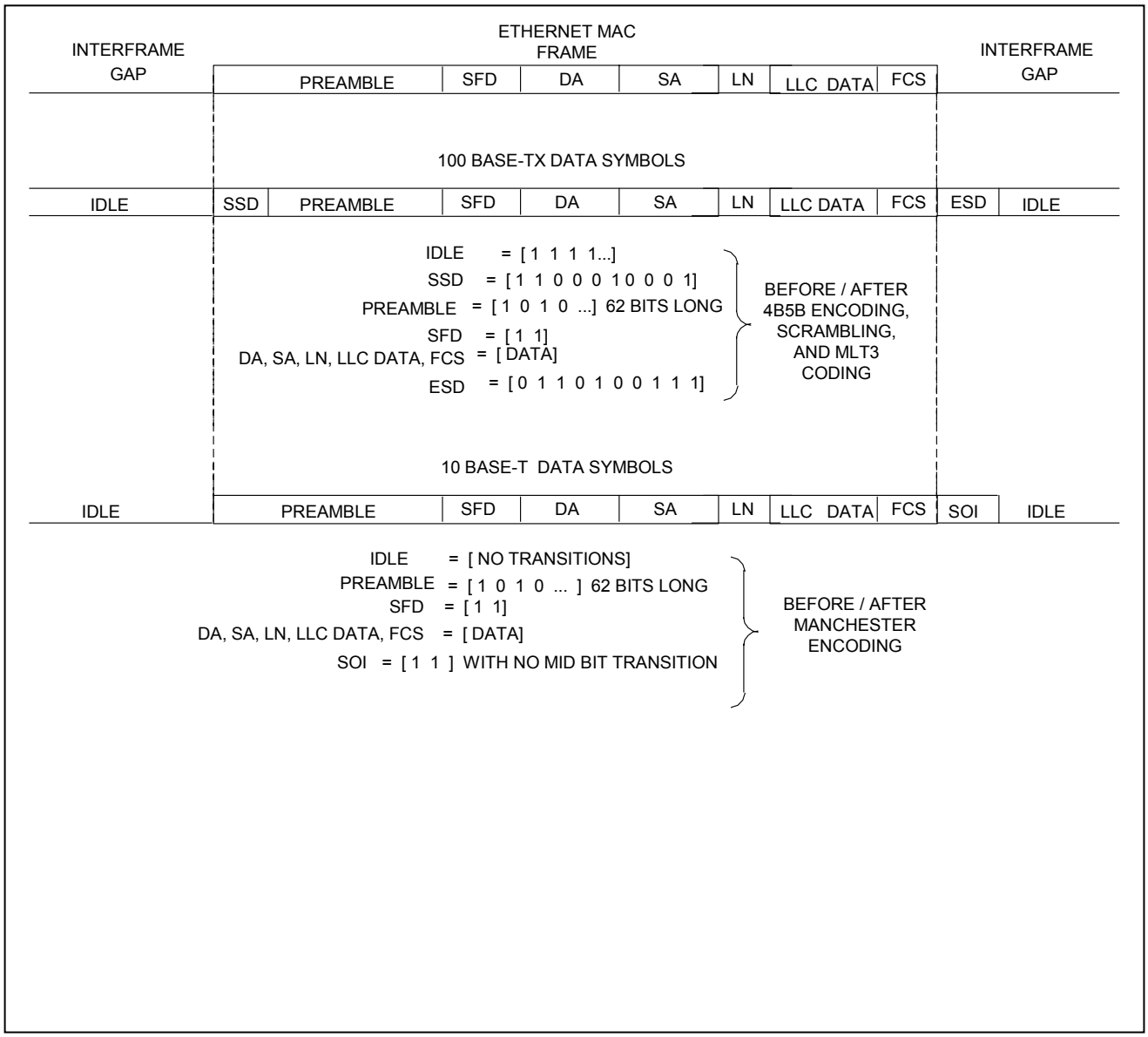


Figure 6.3 - TX/10BT Frame Format

On the transmit side for 100Mbps TX operation, data is received on the controller and then sent to the 4B5B encoder for formatting. The encoded data is then sent to the scrambler. The scrambled and encoded data is then sent to the TP transmitter. The TP transmitter converts the encoded and scrambled data into MLT-3 ternary format, reshapes the output, and drives the twisted pair cable.

On the receive side for 100Mbps TX operation, the twisted pair receiver receives incoming encoded and scrambled MLT-3 data from the twisted pair cable, remove any high frequency noise, equalizes the input signal to compensate for the effects of the cable, qualifies the data with a squelch algorithm, and converts the data from MLT-3 coded twisted pair levels to internal digital levels. The output of the twisted pair receiver then goes to a clock and data recovery block which recovers a clock from the incoming data, uses

the clock to latch in valid data into the device, and converts the data back to NRZ format. The NRZ data is then unscrambled and decoded by the 4B5B decoder and descrambler, respectively, and outputted to the Ethernet controller.

10Mbps operation is similar to the 100Mbps TX operation except, (1) there is no scrambler/descrambler, (2) the encoder/decoder is Manchester instead of 4B5B, (3) the data rate is 10Mbps instead of 100Mbps, and (4) the twisted pair symbol data is two level Manchester instead of ternary MLT-3.

The Management Interface, (hereafter referred to as the MI serial port), is a two pin bi-directional link through which configuration inputs can be set and status outputs can be read. Each block plus the operating modes are described in more detail in the following sections.

6.7.1 MII Disable

The internal PHY MII interface can be disabled by setting the MII disable bit in the MI serial port Control register. When the MII is disabled, the MII inputs are ignored, the MII outputs are placed in high impedance state, and the TP output is high impedance.

6.7.2 Encoder

4B5B Encoder - 100 Mbps

100BASE-TX requires that the data be 4B5B encoded. 4B5B coding converts the 4-Bit data nibbles into 5-Bit date code words. The mapping of the 4B nibbles to the 5B code words is specified in IEEE 802.3. The 4B5B encoder on the LAN91C113 takes 4B nibbles from the controller interface, converts them into 5B words and sends the 5B words to the scrambler. The 4B5B encoder also substitutes the first 8 bits of the preamble with the SSD delimiters (a.k.a. /J/K/ symbols) and adds an ESD delimiter (a.k.a. MR/ symbols) to the end of every packet, as defined in IEEE 802.3. The 4B5B encoder also fills the period between packets, called the idle period, with the continuous stream of idle symbols.

Manchester Encoder - 10 Mbps

The Manchester encoding process combines clock and NRZ data such that the first half of the data bit contains the complement of the data, and the second half of the data bit contains the true data, as specified in IEEE 802.3. This guarantees that a transition always occurs in the middle of the bit call. The Manchester encoder on the LAN91C113 converts the 10Mbps NRZ data from the controller interface into a Manchester Encoded data stream for the TP transmitter and adds a start of idle pulse (SOI) at the end of the packet as specified in IEEE 802.3. The Manchester encoding process is only done on actual packet data, and the idle period between packets is not Manchester encoded and filled with link pulses.

6.7.3 Decoder

4B5B Decoder - 100 Mbps

Since the TP input data is 4B5B encoded on the transmit side, it must also be decoded by the 4B5B decoder on the receive side. The mapping of the 5B nibbles to the 4B code words is specified in IEEE

802.3. The 4B5B decoder on the LAN91C113 takes the 5B code words from the descrambler, converts them into 4B nibbles per Table 2, and sends the 4B nibbles to the controller interface. The 4B5B decoder also strips off the SSD delimiter (a.k.a. /J/K/ symbols) and replaces them with two 4B Data 5 nibbles (a.k.a. /5/ symbol), and strips off the ESD delimiter (a.k.a. /T/R/ symbols) and replaces it with two 4B Data 0 nibbles (a.k.a. /I/symbol), per IEEE 802.3 specifications and shown in Figure 6.3.

Table 6.1 - 4B/5B Symbol Mapping

SYMBOL NAME	DESCRIPTION	5B CODE	4B CODE
0	Data 0	11110	0000
1	Data 1	01001	0001
2	Data 2	10100	0010
3	Data 3	10101	0011
4	Data 4	01010	0100
5	Data 5	01011	0101
6	Data 6	01110	0110
7	Data 7	01111	0111
8	Data 8	10010	1000
9	Data 9	10011	1001
A	Data A	10110	1010
B	Data B	10111	1011
C	Data C	11010	1100
D	Data D	11011	1101
E	Data E	11100	1110
F	Data F	11101	1111
I	Idle	11111	0000
J	SSD #1	11000	0101
K	SSD #2	10001	0101
T	ESD #1	01101	0000
R	ESD #2	00111	0000
H	Halt	00100	Undefined
---	Invalid codes	All others*	0000*

* These 5B codes are not used. For decoder, these 5B codes are decoded to 4B 0000. For encoder, 4B 0000 is encoded to 5B 11110, as shown in symbol Data 0.

The 4B5B decoder detects SSD, ESD and codeword errors in the incoming data stream as specified in IEEE 802.3. These errors are indicated by asserting RX_ER output while the errors are being transmitted across RXD[3:0], and they are also indicated in the serial port by setting SSD, ESD, and codeword error bits in the PHY MI serial port Status Output register.

Manchester Decoder - 10 Mbps

In Manchester coded data, the first half of the data bit contains the complement of the data, and the second half of the data bit contains the true data. The Manchester decoder in the LAN91C113 converts the Manchester encoded data stream from the TP receiver into NRZ data for the controller interface by decoding the data and stripping off the SOI pulse. Since the clock and data recovery block has already separated the clock and data from the TP receiver, the Manchester decoding process to NRZ data is inherently performed by that block.

6.7.4 Clock and Data Recovery

Clock Recovery - 100 Mbps

Clock recovery is done with a PLL. If there is no valid data present on the TP inputs, the PLL is locked to the 25 MHz TX25. When valid data is detected on the TP inputs with the squelch circuit and when the adaptive equalizer has settled, the PLL input is switched to the incoming data on the TP input. The PLL then recovers a clock by locking onto the transitions of the incoming signal from the twisted pair wire. The

recovered dock frequency is a 25 MHz nibble dock, and that clock is outputted on the controller interface signal RX25.

Data Recovery - 100 Mbps

Data recovery is performed by latching in data from the TP receiver with the recovered clock extracted by the PLL. The data is then converted from a single bit stream into nibble wide data word according to the format shown in Figure 6.2.

Clock Recovery - 10 Mbps

The clock recovery process for 10Mbps mode is identical to the 100Mbps mode except, (1) the recovered clock frequency is 2.5 MHz nibble clock, (2) the PLL is switched from TX25 to the TP input when the squelch indicates valid data, (3) The PLL takes up to 12 transitions (bit times) to lock onto the preamble, so some of the preamble data symbols are lost, but the dock recovery block recovers enough preamble symbols to pass at least 6 nibbles of preamble to the receive controller interface as shown in Figure 6.2.

Data Recovery - 10 Mbps

The data recovery process for 10Mbps mode is identical to the 100Mbps mode. As mentioned in the Manchester Decoder section, the data recovery process inherently performs decoding of Manchester encoded data from the TP inputs.

6.7.5 Scrambler

100 Mbps

100BASE-TX requires scrambling to reduce the radiated emissions on the twisted pair. The LAN91C113 scrambler takes the encoded data from the 4B5B encoder, scrambles it per the IEEE 802.3 specifications, and sends it to the TP transmitter.

10 Mbps

A scrambler is not used in 10Mbps mode.

Scrambler Bypass

The scrambler can be bypassed by setting the bypass scrambler/descrambler bit in the PHY MI serial port Configuration 1 register. When this bit is set, the 5B data bypasses the scrambler and goes directly from the 4B5B encoder to the twisted pair transmitter.

6.7.6 Descrambler

100 Mbps

The LAN91C113 descrambler takes the scrambled data from the data recovery block, descrambles it per the IEEE 802.3 specifications, aligns the data on the correct 5B word boundaries, and sends it to the 4B5B decoder.

The algorithm for synchronization of the descrambler is the same as the algorithm outlined in the IEEE 802.3 specification. Once the descrambler is synchronized, it will maintain synchronization as long as enough descrambled idle pattern 1's are detected within a given interval. To stay in synchronization, the descrambler needs to detect at least 25 consecutive descrambled idle pattern 1's in a 1ms interval. If 25

consecutive descrambled idle pattern 1's are not detected within the 1ms interval, the descrambler goes out of synchronization and restarts the synchronization process.

If the descrambler is in the unsynchronized state, the descrambler loss of synchronization detect bit is set in the MI serial port Status Output register to indicate this condition. Once this bit is set, it will stay set until the descrambler achieves synchronization.

10 Mbps

A descrambler is not used in 10 Mbps mode.

Descrambler Bypass

The descrambler can be bypassed by setting the bypass scrambler/descrambler bit in the PHY MI serial port Configuration 1 register. When this bit is set, the data bypasses the descrambler and goes directly from the TP receiver to the 4B5B decoder.

6.7.7 Twisted Pair Transmitter

Transmitter - 100 Mbps

The TX transmitter consists of MLT-3 encoder, waveform generator and line driver.

The MLT-3 encoder converts the NRZ data from the scrambler into a three level MLT-3 code required by IEEE 802.3. MLT-3 coding uses three levels and converts 1's to transitions between the three levels, and converts 0's to no transitions or changes in level.

The purpose of the waveform generator is to shape the transmit output pulse. The waveform generator takes the MLT-3 three level encoded waveform and uses an array of switched current sources to control the rise/fall time and level of the signal at the Output. The output of the switched current sources then goes through a low pass filter in order to "smooth" the current output and remove any high frequency components. In this way, the waveform generator preshapes the output waveform transmitted onto the twisted pair cable to meet the pulse template requirements outlined in IEEE 802.3. The waveform generator eliminates the need for any external filters on the TP transmit output.

The line driver converts the shaped and smoothed waveform to a current output that can drive 100 meters of category 5 unshielded twisted pair cable or 150 Ohm shielded twisted pair cable.

Transmitter - 10 Mbps

The transmitter operation in 10 Mbps mode is much different than the 100 Mbps transmitter. Even so, the transmitter still consists of a waveform generator and line driver.

The purpose of the waveform generator is to shape the output transmit pulse. The waveform generator consists of a ROM, DAC, dock generator, and filter. The DAC generates a stair-stepped representation of the desired output waveform. The stairstepped DAC output then goes through a low pass filter in order to "smooth' the DAC output and remove any high frequency components. The DAC values are determined from the ROM outputs; the ROM contents are chosen to shape the pulse to the desired template and are clocked into the DAC at high speed by the clock generator. In this way, the waveform generator preshapes the output waveform to be transmitted onto the twisted pair cable to meet the pulse template requirements outlined in IEEE 802.3 Clause 14 and also shown in Figure 6.4. The waveshaper replaces and eliminates external filters on the TP transmit output.

The line driver converts the shaped and smoothed waveform to a current output that can drive 100 meters of category 3/4/5 100 Ohm unshielded twisted pair cable or 150 Ohm shielded twisted pair cable tied

directly to the TP output pins without any external filters. During the idle period, no output signal is transmitted on the TP outputs (except link pulse).

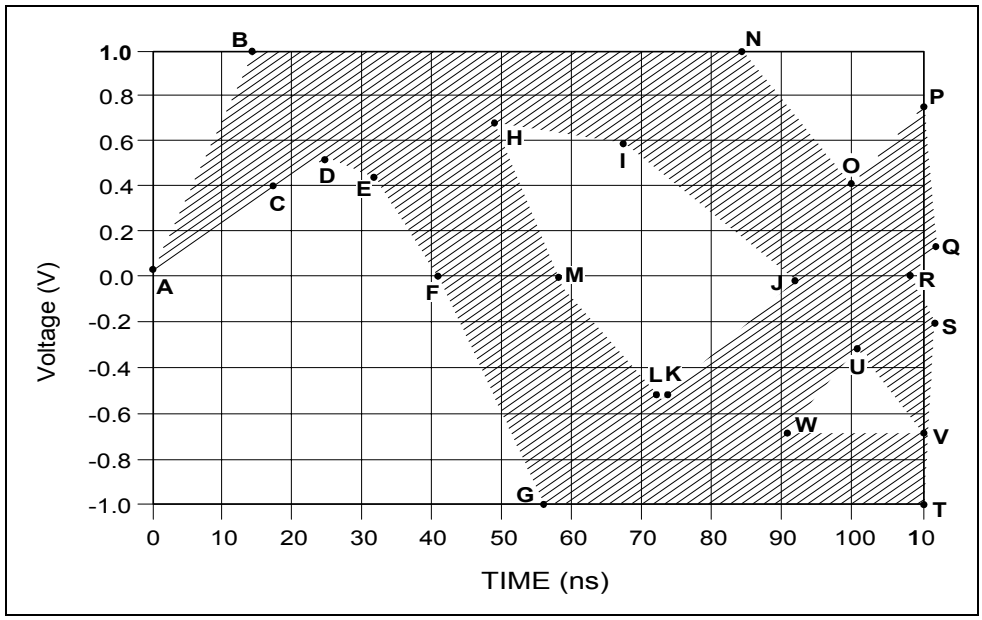


Figure 6.4 - TP Output Voltage Template – 10 MBPS

REFERENCE	TIME (NS) INTERNAL MAU	VOLTAGE (V)
A	0	0
B	15	1.0
C	15	0.4
D	25	0.55
E	32	0.45
F	39	0
G	57	-1.0
H	48	0.7
I	67	0.6
J	89	0
K	74	-0.55
L	73	-0.55
M	61	0
N	85	1.0
O	100	0.4
P	110	0.75
Q	111	0.15
R	111	0
S	111	-0.15
T	110	-1.0
U	100	-0.3

REFERENCE	TIME (NS) INTERNAL MAU	VOLTAGE (V)
V	110	-0.7
W	90	-0.7

Transmit Level Adjust

The transmit output current level is derived from an internal reference voltage and the external resistor on RBIAS pin. The transmit level can be adjusted with either (1) the external resistor on the RBIAS pin, or (2) the four transmit level adjust bits in the PHY MI serial port Configuration 1 register as shown in Table 6.2. The adjustment range is approximately -14% to +16% in 2% steps.

Table 6.2 - Transmit Level Adjust

TLVL[3:0]	GAIN
0000	1.16
0001	1.14
0010	1.12
0011	1.10
0100	1.08
0101	1.06
0110	1.04
0111	1.02
1000	1.00
1001	0.98
1010	0.96
1011	0.94
1100	0.92
1101	0.90
1110	0.88
1111	0.86

Transmit Rise and Fall Time Adjust

The transmit output rise and fall time can be adjusted with the two transmit rise/fall time adjust bits in the PHY MI serial port Configuration 1. The adjustment range is -0.25ns to +0.5ns in 0.25ns steps.

STP (150 Ohm) Cable Mode

The transmitter can be configured to drive 150 Ohm shielded twisted pair cable. The STP mode can be selected by appropriately setting the cable type select bit in the PHY MI serial port Configuration 1 register. When STP mode is enabled, the output current is automatically adjusted to comply with IEEE 802.3 levels.

Transmit Disable

The TP transmitter can be disabled by setting the transmit disable bit in the PHY MI serial port Configuration 1 register. When the transmit disable bit is set, the TP transmitter is forced into the idle state, no data is transmitted, no link pulses are transmitted, and internal loopback is disabled.

Transmit Powerdown

The TP transmitter can be powered down by setting the transmit powerdown bit in the PHY MI serial port Configuration 1 register. When the transmit powerdown bit is set, the TP transmitter is powered down, the TP transmit outputs are high impedance, and the rest of the LAN91C113 operates normally.

6.7.8 Twisted Pair Receiver

Receiver - 100 Mbps

The TX receiver detects input signals from the twisted pair input and converts it to a digital data bit stream ready for dock and data recovery. The receiver can reliably detect data from a 100BASE-TX transmitter that has been passed through 0-100 meters of 100-Ohm category 5 UTP or 150 Ohm STP.

The TX receiver consists of an adaptive equalizer, baseline wander correction circuit, comparators, and MLT-3 decoder. The TP inputs first go to an adaptive equalizer. The adaptive equalizer compensates for the low pass characteristic of the cable, and it has the ability to adapt and compensate for 0-100 meters of category 5, 100 Ohm UTP or 150 Ohm STP twisted pair cable. The baseline wander correction circuit restores the DC component of the input waveform that was removed by external transformers. The comparators convert the equalized signal back to digital levels and are used to qualify the data with the squelch circuit. The MLT-3 decoder takes the three level MLT-3 digital data from the comparators and converts it to back to normal digital data to be used for dock and data recovery.

Receiver - 10 Mbps

The 10 Mbps receiver is able to detect input signals from the twisted pair cable that are within the template shown in Figure 6.5. The inputs are biased by internal resistors. The TP inputs pass through a low pass filter designed to eliminate any high frequency noise on the input. The output of the receive filter goes to two different types of comparators, squelch and zero crossing. The squelch comparator determines whether the signal is valid, and the zero crossing comparator is used to sense the actual data transitions once the signal is determined to be valid. The output of the squelch comparator goes to the squelch circuit and is also used for link pulse detection, SOI detection, and reverse polarity detection; the output of the zero crossing comparator is used for clock and data recovery in the Manchester decoder.

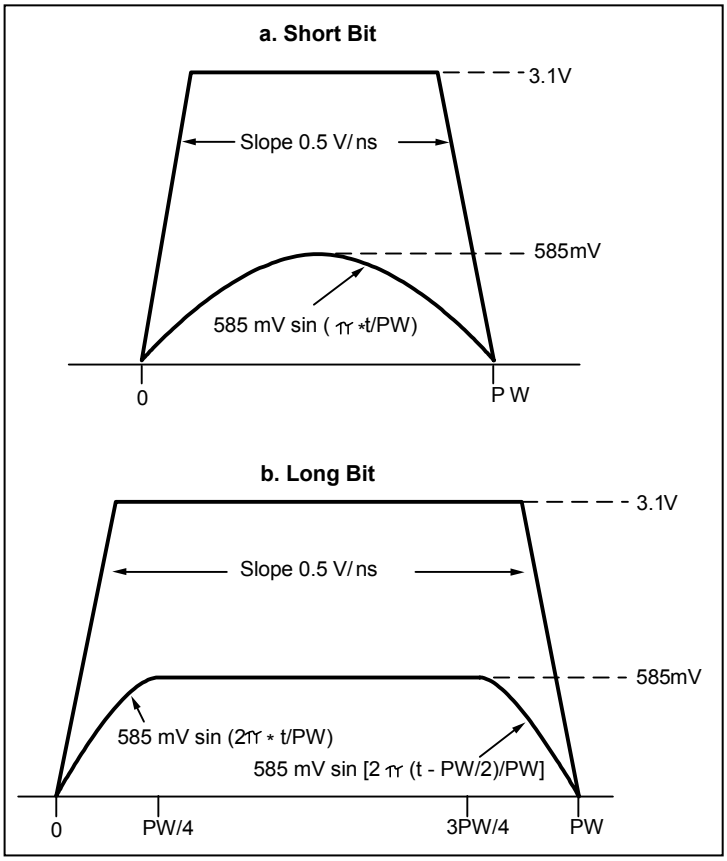


Figure 6.5 - TP Input Voltage Template – 10 MBPS

TP Squelch - 100 Mbps

The squelch block determines if the TP input contains valid data. The 100 Mbps TP squelch is one of the criteria used to determine link integrity. The squelch comparators compare the TP inputs against fixed positive and negative thresholds, called squelch levels. The output from the squelch comparator goes to a digital squelch circuit which determines if the receive input data on that channel is valid. If the data is invalid, the receiver is in the squelched state. If the input voltage exceeds the squelch levels at least 4 times with alternating polarity within a 10 μS interval, the data is considered to be valid by the squelch circuit and the receiver now enters into the unsquelch state. In the unsquelch state, the receive threshold level is reduced by approximately 30% for noise immunity reasons and is called the unsquelch level. When the receiver is in the unsquelch state, then the input signal is deemed to be valid. The device stays in the unsquelch state until loss of data is detected. Loss of data is detected if no alternating polarity unsquelch transitions are detected during any 10 μS interval. When the loss of data is detected, the receive squelch is turned on again.

TP Squelch, 10 Mbps

The TP squelch algorithm for 10 Mbps mode is identical to the 100 Mbps mode except, (1) the 10 Mbps TP squelch algorithm is not used for link integrity but to sense the beginning of a packet, (2) the receiver goes into the unsquelch state if the input voltage exceeds the squelch levels for three bit times with alternating polarity within a 50-250 nS interval, (3) the receiver goes into the squelch state when idle is detected, (4) unsquelch detection has no affect on link integrity, link pulses are used for that in 10 Mbps mode, (5) start

of packet is determined when the receiver goes into the unsquelch state an a CRS100 is asserted, and (6) the receiver meets the squelch requirements defined in IEEE 802.3 Clause 14.

Equalizer Disable

The adaptive equalizer can be disabled by setting the equalizer disable bit in the PHY MI serial port Configuration 1 register. When disabled, the equalizer is forced into the response it would normally have if zero cable length was detected.

Receive Level Adjust

The receiver squelch and unsquelch levels can be lowered by 4.5 dB by setting the receive level adjust bit in the PHY MI serial port Configuration 1 register. By setting this bit, the device may be able to support longer cable lengths.

6.7.9 Collision

100 Mbps

Collision occurs whenever transmit and receive occur simultaneously while the device is in Half Duplex.

Collision is sensed whenever there is simultaneous transmission (packet transmission on TPO±) and reception (non-idle symbols detected on TP input). When collision is detected, the MAC is notified. Once collision starts, the receive and transmit packets that caused the collision are terminated by their respective MACs until the responsible MACs terminate the transmission, the PHY continues to pass the data on.

The collision function is disabled if the device is in the Full Duplex mode, is in the Link Fail State, or if the device is in the diagnostic loopback mode.

10 Mbps

Collision in 10Mbps mode is identical to the 100Mbps mode except, (1) reception is determined by the 10Mbps squelch criteria, (2) data being passed to the MAC are forced to all 0's, (3) MAC is notified of the collision when the SQE test is performed, (4) MAC is notified of the collision when the jabber condition has been detected.

Collision Test

The MAC and PHY collision indication can be tested by setting the collision test register bit in the PHY MI serial port Control register. When this bit is set, internal TXEN from the MAC is looped back onto COL and the TP outputs are disabled.

6.7.10 Start of Packet

100 Mbps

Start of packet for 100 Mbps mode is indicated by a unique Start of Stream Delimiter (referred to as SSD). The SSD pattern consists of the two /J/K/ 5B symbols inserted at the beginning of the packet in place of the first two preamble symbols, as defined in IEEE 802.3 Clause 24.

The transmit SSD is generated by the 4B5B encoder and the /J/K/ symbols are inserted by the 4B5B encoder at the beginning of the transmit data packet in place of the first two 5B symbols of the preamble.

The receive pattern is detected by the 4B5B decoder by examining groups of 10 consecutive code bits (two 5B words) from the descrambler. Between packets, the receiver will be detecting the idle pattern, which is 5B /I/ symbols. While in the idle state, the MAC is notified that no data/invalid data is received.

If the receiver is in the idle state and 10 consecutive code bits from the receiver consist of the /J/K/ symbols, the start of packet is detected, data reception is begun, the MAC is notified that valid data is received, and 5/5/ symbols are substituted in place of the /J/K/ symbols.

If the receiver is in the idle state and 10 consecutive code bits from the receiver consist of a pattern that is neither /I/I/ nor /J/K/ symbols but contains at least 2 non contiguous 0's, then activity is detected but the start of packet is considered to be faulty and a False Carrier Indication (also referred to as bad SSD) is signaled to the controller interface. When False Carrier is detected, the MAC is notified of false carrier and invalid received, and the bad SSD bit is set in the PHY MI serial port Status Output register. Once a False Carrier Event is detected, the idle pattern (two /I/I/ symbols) must be detected before any new SSD's can be sensed.

If the receiver is in the idle state and 10 consecutive code bits from the receiver consist of a pattern that is neither /I/I/ nor /J/K/ symbols but does not contain at least 2 non-contiguous 0's, the data is ignored and the receiver stays in the idle state.

10 Mbps

Since the idle period in 10 Mbps mode is defined to be the period when no data is present on the TP inputs, then the start of packet for 10 Mbps mode is detected when valid data is detected by the TP squelch circuit. When start of packet is detected, carrier sense signal at internal MII is asserted as described in the Controller Interface section. Refer to the TP squelch section for 10 Mbps mode for the algorithm for valid data detection.

6.7.11 End of Packet

100 Mbps

End of packet for 100 Mbps mode is indicated by the End of Stream Delimiter (referred to as ESD). The ESD pattern consists of the two /T/R/ 4B5B symbols inserted after the end of the packet, as defined in IEEE 802.3 Clause 24.

The transmit ESD is generated by the 4B5B encoder and the /T/R/ symbols are inserted by the 4B5B encoder after the end of the transmit data packet.

The receive ESD pattern is detected by the 4B5B decoder by examining groups of 10 consecutive code bits (two 5B words) from the descrambler during valid packet reception to determine if there is an ESD.

If the 10 consecutive code bits from the receiver during valid packet reception consist of the /T/R/ symbols, the end of packet is detected, data reception is terminated, the MAC is notified of valid data received, and /I/I/ symbols are substituted in place of the /T/R/ symbols.

If 10 consecutive code bits from the receiver during valid packet reception do not consist of /T/R/ symbols but consist of /I/I/ symbols instead, then the packet is considered to have been terminated prematurely and abnormally. When this premature end of packet condition is detected, the MAC is notified of invalid data received for the nibble associated with the first /I/ symbol. Premature end of packet condition is also indicated by setting the bad ESD bit in the PHY MI serial port Status Output register.

10 Mbps

The end of packet for 10 Mbps mode is indicated with the SOI (Start of Idle) pulse. The SOI pulse is a positive pulse containing a Manchester code violation inserted at the end of every packet.

The transmit SOI pulse is generated by the TP transmitter and inserted at the end of the data packet after TXEN is deasserted. The transmitted SOI output pulse at the TP output is shaped by the transmit waveshaper to meet the pulse template requirements specified in IEEE 802.3 Clause 14 and shown in Figure 6.6.

The receive SOI pulse is detected by the TP receiver by sensing missing data transitions. Once the SOI pulse is detected, data reception is ended and the MAC is notified of no data/invalid data received.

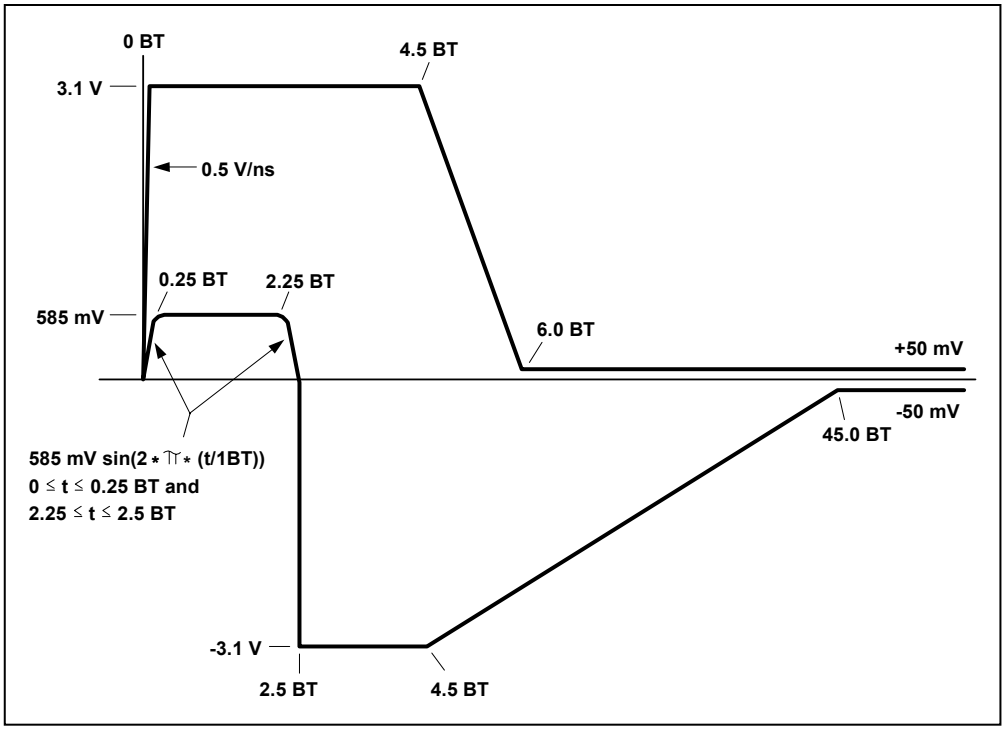


Figure 6.6 - SOI Outage Voltage Template – 10MBPS

6.7.12 Link Integrity & Autonegotiation

General

The LAN91C113 can be configured to implement either the standard link integrity algorithms or the AutoNegotiation algorithm.

The standard link integrity algorithms are used solely to establish an active link to and from a remote device. There are different standard link integrity algorithms for 10 and 100 Mbps modes. The AutoNegotiation algorithm is used for two purposes: (1) To automatically configure the device for either 10/100 Mbps and Half/Full Duplex modes, and (2) to establish an active link to and from a remote device. The standard link integrity and AutoNegotiation algorithms are described below.

AutoNegotiation is only specified for 100BASE-TX and 10BASE-T operation.

10BASE-T Link Integrity Algorithm - 10Mbps

The LAN91C113 uses the same 10BASE-T link integrity algorithm that is defined in IEEE 802.3 Clause 14. This algorithm uses normal link pulses, referred to as NLP's and transmitted during idle periods, to determine if a device has successfully established a link with a remote device (called Link Pass State). The transmit link pulse meets the template defined in IEEE 802.3 Clause 14 and shown in Figure 6.7. Refer to IEEE 802.3 Clause 14 for more details if needed.

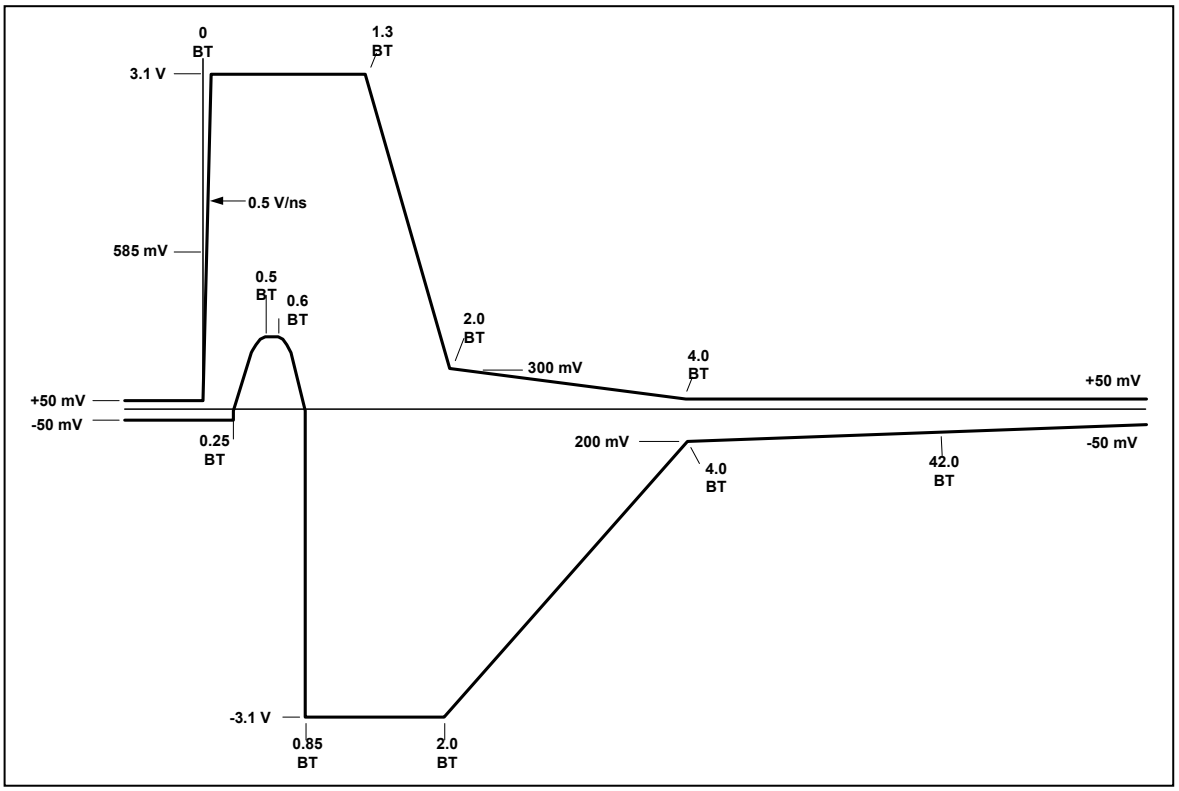


Figure 6.7 - Link Pulse Output Voltage Template – NLP, FLP

100BASE-TX Link Integrity Algorithm - 100Mbps

Since 100BASE-TX is defined to have an active idle signal, then there is no need to have separate link pulses like those defined for 10BASE-T. The LAN91C113 uses the squelch criteria and descrambler synchronization algorithm on the input data to determine if the device has successfully established a link with a remote device (called Link Pass State). Refer to IEEE 802.3 for both of these algorithms for more details.

AutoNegotiation Algorithm

As stated previously, the AutoNegotiation algorithm is used for two purposes: (1) To automatically configure the device for either 10/100 Mbps and Half/ Full Duplex modes, and (2) to establish an active link to and from a remote device. The AutoNegotiation algorithm is the same algorithm that is defined in IEEE 802.3 Clause 28. AutoNegotiation uses a burst of link pulses, called fast link pulses and referred to as FLP'S, to pass up to 16 bits of signaling data back and forth between the LAN91C113 and a remote device. The transmit FLP pulses meet the templated specified in IEEE 802.3 and shown in Figure 6.7. A timing diagram contrasting NLP's and FLP's is shown in Figure 6.8.

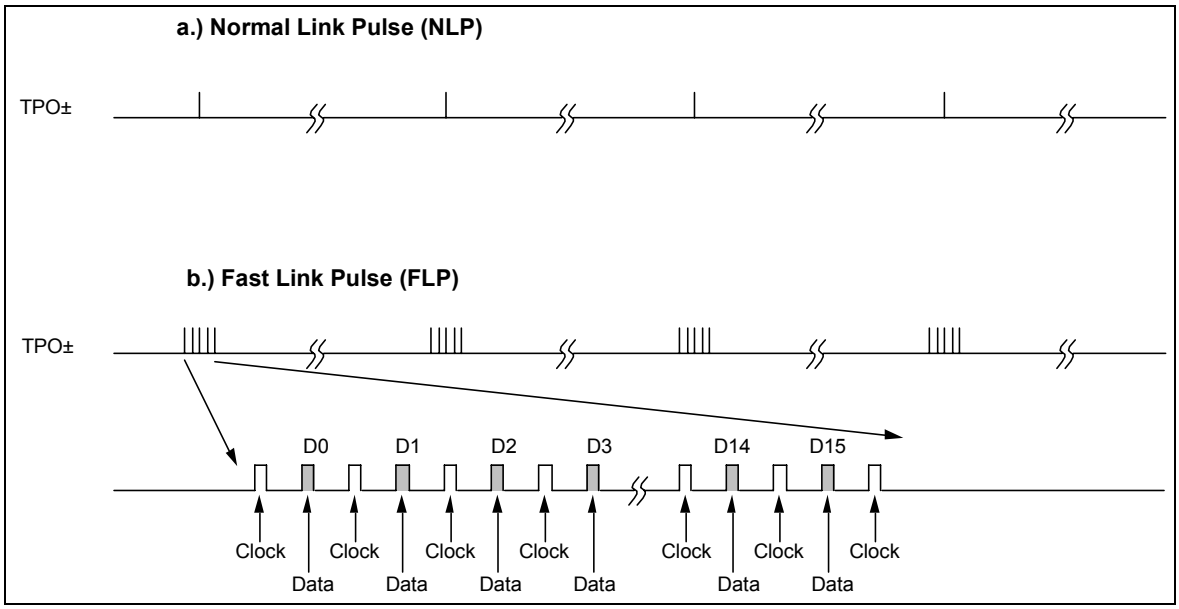


Figure 6.8 - NLP VS. FLP Link Pulse

The AutoNegotiation algorithm is initiated by any of these events: (1) AutoNegotiation enabled, (2) a device enters the Link Fail State, (3) AutoNegotiation Reset. Once a negotiation has been initiated, the LAN91C113 first determines if the remote device has AutoNegotiation capability. If the remote device is not AutoNegotiation capable and is just transmitting either a 10BASE-T or 100BASE-TX signal, the LAN91C113 will sense that and place itself in the correct mode. If the LAN91C113 detects FLP's from the remote device, then the remote device is determined to have AutoNegotiation capability and the device then uses the contents of the MI serial port AutoNegotiation Advertisement register and FLP's to advertise its capabilities to a remote device. The remote device does the same, and the capabilities read back from the remote device are stored in the PHY MI serial port AutoNegotiation Remote End Capability register. The LAN91C113 negotiation algorithm then matches it's capabilities to the remote device's capabilities and determines what mode the device should be configured to according to the priority resolution algorithm defined in IEEE 802.3 Clause 28. Once the negotiation process is completed, the LAN91C113 then configures itself for either 10 or 100 Mbps mode and either Full or Half Duplex modes (depending on the outcome of the negotiation process), and it switches to either the 100BASETX or 10BASE-T link integrity algorithms (depending on which mode was enabled by AutoNegotiation). Refer to IEEE 802.3 Clause 28 for more details.

AutoNegotiation Outcome Indication

The outcome or result of the AutoNegotiation process is stored in the speed detect and duplex detect bits in the PHY MI serial port Status Output register.

AutoNegotiation Status

The status of the AutoNegotiation process can be monitored by reading the AutoNegotiation acknowledgement bit in the MI serial port Status register. The MI serial port Status register contains a single AutoNegotiation acknowledgement bit which indicates when an AutoNegotiation has been initiated and successfully completed.

AutoNegotiation Enable

The AutoNegotiation algorithm can be enabled by setting both the ANEG bit in the MAC Receive/PHY Control Register and the ANEG_EN bit in the MI PHY Register 0 (Control Register). Clearing either of these two bits will turn off AutoNegotiation mode. When the AutoNegotiation algorithm is enabled, the device halts all transmissions including link pulses for 1200-1500 ms, enters the Link Fail State, and restarts the negotiation process. When AutoNegotiation mode is turned on or reset, the software driver should wait for at least 1500ms to read the ANEG_ACK bit in the MI PHY Status Register to determine whether the AutoNegotiation process has been completed. When the ANEG bit in the Receive/PHY Control Register is cleared, the AutoNegotiation algorithm is disabled, the selection of 10/100 Mbps mode and duplex mode is determined by the SPEED bit and the DPLX bit in the MAC Receive/PHY Control register. When the ANEG bit in the Receive/PHY Control Register is set and the ANEG_EN bit in the MI PHY Register 0 (Control Register) is cleared, the AutoNegotiation algorithm is disabled, the selection of 10/100 Mbps mode and duplex mode is determined by the SPEED bit and the DPLX bit in the MI PHY Register 0 (Control Register).

AutoNegotiation Reset

The AutoNegotiation algorithm can be initiated at any time by setting the AutoNegotiation reset bit in the PHY MI serial port Control register.

Link Disable

The link integrity function can be disabled by setting the link disable bit in the MI PHY serial port Configuration 1 register. When the link integrity function is disabled, the device is forced into the Link Pass state, configures itself for Half/Full Duplex based on the value of the duplex bit in the PHY MI serial port Control register, configures itself for 100/10 Mbps operation based on the values of the speed bit in the MI serial port Control register, and continues to transmit NLP'S or TX idle patterns, depending on whether the device is in 10 or 100 Mbps mode.

6.7.13 Jabber

100 Mbps

Jabber function is disabled in the 100 Mbps mode.

10 Mbps

Jabber condition occurs when the transmit packet exceeds a predetermined length. When jabber is detected, the TP transmit outputs are forced to the idle state, collision is asserted, and register bits in the PHY MI serial port Status and Status Output registers are set.

Jabber Disable

The jabber function can be disabled by setting the jabber disable bit in the PHY MI serial port Configuration 2 register.

6.7.14 Receive Polarity Correction

100 Mbps

No polarity detection or correction is needed in 100Mbps mode.

10 Mbps

The polarity of the signal on the TP receive input is continuously monitored. If either 3 consecutive link pulses or one SOI pulse indicates incorrect polarity on the TP receive input, the polarity is internally determined to be incorrect, and a reverse polarity bit is set in the PHY MI serial port Status Output register.

The LAN91C113 will automatically correct for the reverse polarity condition provided that the autopolarity feature is not disabled.

Autopolarity Disable

The autopolarity feature can be disabled by setting the autopolarity disable bit in the PHY MI serial port Configuration 2 register.

6.7.15 Full Duplex Mode

100 Mbps

Full Duplex mode allows transmission and reception to occur simultaneously. When Full Duplex mode is enabled, collision is disabled.

The device can be either forced into Half or Full Duplex mode, or the device can detect either Half or Full Duplex capability from a remote device and automatically place itself in the correct mode.

The device can be forced into the Full or Half Duplex modes by either setting the duplex bit in the MI serial port Control register.

The device can automatically configure itself for Full or Half Duplex modes by using the AutoNegotiation algorithm to advertise and detect Full and Half Duplex capabilities to and from a remote terminal. All of this is described in detail in the Link Integrity and AutoNegotiation section.

10 Mbps

Full Duplex in 10 Mbps mode is identical to the 100 Mbps mode.

100/10 Mbps SELECTION

General

The device can be forced into either the 100 or 10 Mbps mode, or the device also can detect 100 or 10 Mbps capability from a remote device and automatically place itself in the correct mode.

The device can be forced into either the 100 or 10 Mbps mode by setting the speed select bit in the PHY MI serial port Control register assuming AutoNegotiation is not enabled.

The device can automatically configure itself for 100 or 10 Mbps mode by using the AutoNegotiation algorithm to advertise and detect 100 and 10 Mbps capabilities to and from a remote terminal. All of this is described in detail in the Link Integrity & AutoNegotiation section.

6.7.16 Loopback

Diagnostic Loopback

A diagnostic loopback mode can also be selected by setting the loopback bit in the MI serial port Control register. When diagnostic loopback is enabled, transmit data at internal MII is looped back onto receive data output at internal MII, transmit enable signal is looped back onto carrier sense output at internal MII, the TP receive and transmit paths are disabled, the transmit link pulses are halted, and the Half/Full Duplex modes do not change.

6.7.17 PHY Powerdown

The internal PHY of LAN91C113 can be powered down by setting the powerdown bit in the PHY MI serial port Control register. In powerdown mode, the TP outputs are in high impedance state, all functions are disabled except the PHY MI serial port, and the power consumption is reduced to a minimum. To restore PHY to normal power mode, set the PDN bit in PHY MI Register 0 to 0. The PHY is then in isolation mode (MII_DIS bit is set). This MII_DIS bit is needed to be cleared. The device is guaranteed to be ready for normal operation 500mS after powerdown is deasserted.

6.7.18 PHY Interrupt

The LAN91C113 PHY has interrupt capability. The interrupt is triggered by certain output status bits (also referred to as interrupt bits) in the serial port. R/LT bits are read bits that latch on transition. R/LT bits are also interrupt bits if they are not masked out with the Mask register bits. Interrupt bits automatically latch themselves into their register locations and assert the interrupt indication when they change state. Interrupt bits stay latched until they are read. When interrupt bits are read, the interrupt indication is deasserted and the interrupt bits that caused the interrupt to happen are updated to their current value. Each interrupt bit can be individually masked and subsequently be removed as an interrupt bit by setting the appropriate mask register bits in the Mask register.

Interrupt indication is done in two ways: (1) MDINT bit in Interrupt Status Register, (2) INT bit in the PHY MI Serial Port Status Output register. The INT bit is an active high interrupt register bit that resides in the PHY MI Serial Port Status Output register.

6.8 Reset

The chip (MAC & PHY) performs an internal system reset when either (1) the RESET pin is asserted high for at least 100ns, (2) writing “1” to the SOFT_RST bit in the Receive Control Register, this reset bit is not a self-clearing bit, reset can be terminated by writing the bit low. It programs all registers to their default value. When reset is initiated by (1) and the EEPROM is presented and enabled, the controller will load the EEPROM to obtain the following configurations: 1) Configuration Register, 2) BASE Register, or/and 3) MAC Address. The internal MAC is not a power on reset device, thus reset is required after power up to ensure all register bits are in default state.

The internal PHY is reset when either (1) VDD is applied to the device, (2) the RST bit is set in the PHY MI serial port Control register, this reset bit is a self-clearing bit, and the PHY will return a “1” on reads to this bit until the reset is completed, 3) the RESET pin is asserted high, (4) the SOFT_RST bit is set high and then cleared. When reset is initiated by (1) or (2), an internal power-on reset pulse is generated which resets all internal circuits, forces the PHY MI serial port bits to their default values, and latches in new values for the MI address. After the power-on reset pulse has finished, the reset bit in the PHY MI serial port Control registers cleared and the device is ready for normal operation. When reset is initiated by (3), the same procedure occurs except the device stays in the reset state as long as the RESET pin is held high. The internal PHY is guaranteed to be ready for normal operation 50 mS after the reset pin was de-

asserted or the reset bit is set. Software driver requires to wait for 50mS after setting the RST bit to high to access the internal PHY again.

Chapter 7 Data Structures and Registers

7.1 Frame Format In Buffer Memory

The frame format in memory is similar for the Transmit and Receive areas. The first word is reserved for the status word. The next word is used to specify the total number of bytes, and it is followed by the data area. The data area holds the frame itself.

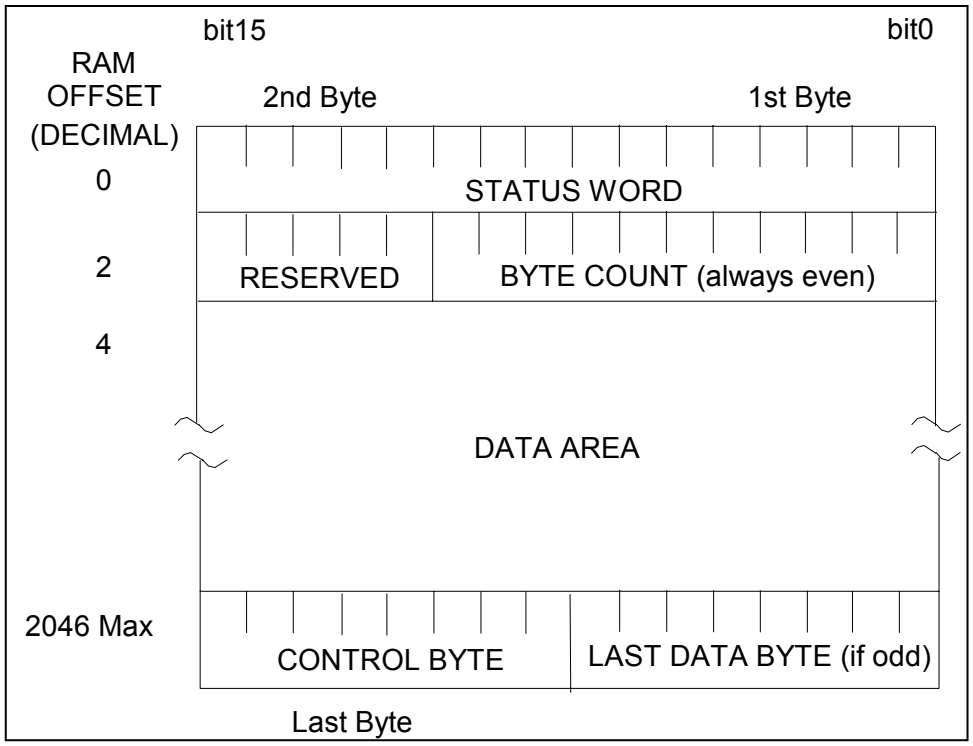


Figure 7.1 - Data Frame Format

	TRANSMIT PACKET	RECEIVE PACKET
STATUS WORD	Written by CSMA upon transmit completion (see Status Register)	Written by CSMA upon receive completion (see RX Frame Status Word)
BYTE COUNT	Written by CPU	Written by CSMA
DATA AREA	Written/modified by CPU	Written by CSMA
CONTROL BYTE	Written by CPU to control odd/even data bytes	Written by CSMA; also has odd/even bit

BYTE COUNT - Divided by two, it defines the total number of words including the STATUS WORD, the BYTE COUNT WORD, the DATA AREA and the CONTROL BYTE. The maximum number of bytes in a RAM page is 2048 bytes.

The receive byte count always appears as even; the ODDFRM bit of the receive status word indicates if the low byte of the last word is relevant.

The transmit byte count least significant bit will be assumed 0 by the controller regardless of the value written in memory.

DATA AREA - The data area starts at offset 4 of the packet structure and can extend up to 2043 bytes.

The data area contains six bytes of DESTINATION ADDRESS followed by six bytes of SOURCE ADDRESS, followed by a variable-length number of bytes. On transmit, all bytes are provided by the CPU, including the source address. The LAN91C113 does not insert its own source address. On receive, all bytes are provided by the CSMA side.

The 802.3 Frame Length word (Frame Type in Ethernet) is not interpreted by the LAN91C113. It is treated transparently as data both for transmit and receive operations.

CONTROL BYTE - For transmit packets the CONTROL BYTE is written by the CPU as:

X	X	ODD	CRC	0	0	0	0

ODD - If set, indicates an odd number of bytes, with the last byte being right before the CONTROL BYTE. If clear, the number of data bytes is even and the byte before the CONTROL BYTE is not transmitted.

CRC - When set, CRC will be appended to the frame. This bit has only meaning if the NOCRC bit in the TCR is set.

For receive packets the CONTROL BYTE is written by the controller as:

0	1	ODD	0	0	0	0	0

ODD - If set, indicates an odd number of bytes, with the last byte being right before the CONTROL BYTE. If clear, the number of data bytes is even and the byte before the CONTROL BYTE should be ignored.

7.2 Receive Frame Status Word

This word is written at the beginning of each receive frame in memory. It is not available as a register.

HIGH BYTE	ALGN ERR	BROD CAST	BAD CRC	ODD FRM	TOOLNG	TOO SHORT		
LOW BYTE	HASH VALUE							MULT CAST
	Reserved	5	4	3	2	1	0	

ALGNERR - Frame had alignment error.

BRODCAST - Receive frame was broadcast. When a broadcast packet is received, the MULTCAST bit may be also set on the status word in addition to the BRODCAST bit. The software implement may just ignore the MULTCAST bit if for BRODCAST packet.

BADCRC - Frame had CRC error, or RX_ER was asserted during reception.

ODDFRM - This bit when set indicates that the received frame had an odd number of bytes.

TOOLNG - Frame length was longer than 802.3 maximum size (1518 bytes on the cable).

TOOSHORT - Frame length was shorter than 802.3 minimum size (64 bytes on the cable).

HASH VALUE - Provides the hash value used to index the Multicast Registers. Can be used by receive routines to speed up the group address search. The hash value consists of the six most significant bits of the CRC calculated on the Destination Address, and maps into the 64 bit multicast table. Bits 5,4,3 of the hash value select a byte of the multicast table, while bits 2,1,0 determine the bit within the byte selected. Examples of the address mapping:

ADDRESS	HASH VALUE 5-0	MULTICAST TABLE BIT
ED 00 00 00 00 00	000 000	MT-0 bit 0
0D 00 00 00 00 00	010 000	MT-2 bit 0
01 00 00 00 00 00	100 111	MT-4 bit 7
2F 00 00 00 00 00	111 111	MT-7 bit 7

MULTCAST - Receive frame was multicast. If hash value corresponds to a multicast table bit that is set, and the address was a multicast, the packet will pass address filtering regardless of other filtering criteria.

7.3 I/O Space

The base I/O space is determined by the IOS0-IOS2 inputs and the EEPROM contents. To limit the I/O space requirements to 16 locations, the registers are assigned to different banks. The last word of the I/O area is shared by all banks and can be used to change the bank in use. Registers are described using the following convention:

OFFSET **NAME** **TYPE** **SYMBOL**

HIGH BYTE	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
	X	X	X	X	X	X	X	X
LOW BYTE	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	X	X	X	X	X	X	X	X

OFFSET - Defines the address offset within the IOBASE where the register can be accessed at, provided the bank select has the appropriate value.

The offset specifies the address of the even byte (bits 0-7) or the address of the complete word.

The odd byte can be accessed using address (offset + 1).

Some registers (like the Interrupt Ack., or like Interrupt Mask) are functionally described as two eight bit registers, in that case the offset of each one is independently specified.

Regardless of the functional description, all registers can be accessed as words or bytes.

The default bit values upon hard reset are highlighted below each register.

Table 7.1 - Internal I/O Space Mapping

	BANK0	BANK1	BANK2	BANK3
0	TCR	CONFIG	MMU COMMAND	MT0-1
2	EPH STATUS	BASE	PNR	MT2-3
4	RCR	IA0-1	FIFO PORTS	MT4-5
6	COUNTER	IA2-3	POINTER	MT6-7
8	MIR	IA4-5	DATA	MGMT
A	RPCR	GENERAL	DATA	REVISION
C	RESERVED	CONTROL	INTERRUPT	ERCV
E	BANK	BANK	BANK	BANK

A special BANK (BANK7) exists to support the addition of external registers.

7.4 Bank Select Register

OFFSET	NAME	TYPE	SYMBOL
E	BANK SELECT REGISTER	READ/WRITE	BSR

HIGH BYTE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	0	0	1	1	0	0	1	1
LOW BYTE						BS2	BS1	BS0
	X	X	X	X	X	0	0	0

BS2, BS1, BS0 Determine the bank presently in use. This register is always accessible and is used to select the register bank in use.

The upper byte always reads as 33h and can be used to help determine the I/O location of the LAN91C113.

The BANK SELECT REGISTER is always accessible regardless of the value of BS0-2

BANK 7 has no internal registers other than the BANK SELECT REGISTER itself. On valid cycles where BANK7 is selected (BS0=BS1=BS2=1), and A3=0, nCSOUT is activated to facilitate implementation of external registers.

Note: BANK7 does not exist in LAN91C9x devices. For backward S/W compatibility BANK7 accesses should be done if the Revision Control register indicates the device is the LAN91C113.

Bank 7 is a new register Bank to the SMSC LAN91C113 device. This bank has extended registers that allow the extended feature set of the SMSC LAN91C113.

7.5 Bank 0 - Transmit Control Register

OFFSET	NAME	TYPE	SYMBOL
0	TRANSMIT CONTROL REGISTER	READ/WRITE	TCR

This register holds bits programmed by the CPU to control some of the protocol transmit options.

HIGH BYTE	SWFDUP	Reserved	EPH LOOP	STP SQET	FDUPLX	MON_ CSN	Reserved	NOCRC
	0	0	0	0	0	0	0	0
LOW BYTE	PAD_EN	Reserved	Reserved	Reserved	Reserved	FORCOL	LOOP	TXENA
	0	0	0	0	0	0	0	0

SWFDUP - Enables Switched Full Duplex mode. In this mode, transmit state machine is inhibited from recognizing carrier sense, so deferrals will not occur. Also inhibits collision count, therefore, the collision related status bits in the EPHSR are not valid (CTR_ROL, LATCOL, SQET, 16COL, MUL COL, and SNGL COL). Uses COL100 as flow control, limiting backoff and jam to 1 clock each before inter-frame gap, then retry will occur after IFG. If COL100 is active during preamble, full preamble will be output before jam. When SWFDUP is high, the values of FDUPLX and MON_CSN have no effect.

EPH_LOOP - Internal loopback at the EPH block. Serial data is internally looped back when set. Defaults low. When EPH_LOOP is high the following transmit outputs are forced inactive: TXD0-TXD3 = 0h, TXEN100 = 0. The following and external inputs are blocked: CRS100=0, COL100=0, RX_DV= RX_ER=0.

STP_SQET - Stop transmission on SQET error. If this bit is set, LAN91C113 will stop and disable the transmitter on SQE test error. If the external SQET generator on the network, generates the SQET pulse during the IPG (Inter Frame Gap), this bit will not be set and subsequent transmits will occur as in case of implementing “Auto Release” for multiple transmit packets. If this bit is cleared, then the SQET bit in the EPH Status register will be cleared. Defaults low.

FDUPLX - When set, the LAN91C113 will cause frames to be received if they pass the address filter regardless of the source for the frame. When clear, the node will not receive a frame sourced by itself. This bit does not control the duplex mode operation, the duplex mode operation is controlled by the SWFDUP bit.

MON_CSN - When set the LAN91C113 monitors carrier while transmitting. It must see its own carrier by the end of the preamble. If it is not seen, or if carrier is lost during transmission, the transmitter aborts the frame without CRC and turns itself off and sets the LOST CARR bit in the EPHSR. When this bit is clear the transmitter ignores its own carrier. Defaults low. Should be 0 for MII operation.

NOCRC - Does not append CRC to transmitted frames when set. Allows software to insert the desired CRC. Defaults to zero, namely CRC inserted.

PAD_EN - When set, the LAN91C113 will pad transmit frames shorter than 64 bytes with 00. For TX, the CPU should write the actual BYTE COUNT before pad by the LAN91C113 to the buffer RAM, excludes the padded 00. When this bit is cleared, the LAN91C113 does not pad frames.

FORCOL - When set, the FORCOL bit will force a collision by not deferring deliberately. This bit is set and cleared only by the CPU. When TXENA is enabled with no packets in the queue and while the FORCOL bit is set, the LAN91C113 will transmit a preamble pattern the next time a carrier is seen on the line. If a packet is queued, a preamble and SFD will be transmitted. This bit defaults low to normal operation. NOTE: The LATCOL bit in the EPHSR, setting up as a result of FORCOL, will reset TXENA to 0. In order to force another collision, TXENA must be set to 1 again.

LOOP - Loopback. General purpose output port used to control the LBK pin. Typically used to put the PHY chip in loopback mode.

TXENA - Transmit enabled when set. Transmit is disabled if clear. When the bit is cleared the LAN91C113 will complete the current transmission before stopping. When stopping due to an error, this bit is automatically cleared.

7.6 Bank 0 - EPH Status Register

OFFSET	NAME	TYPE	SYMBOL
2	EPH STATUS REGISTER	READ ONLY	EPHSR

This register stores the status of the last transmitted frame. This register value, upon individual transmit packet completion, is stored as the first word in the memory area allocated to the packet. Packet interrupt processing should use the copy in memory as the register itself will be updated by subsequent packet transmissions. The register can be used for real time values (like TXENA and LINK OK). If TXENA is cleared the register holds the last packet completion status.

HIGH BYTE	TX UNRN	LINK_ OK	Reserved	CTR _ROL	EXC _DEF	LOST CARR	LATCOL	Reserved
	0	-nLNK pin	0	0	0	0	0	0
LOW BYTE	TX DEFR	LTX BRD	SQET	16COL	LTX MULT	MUL COL	SNGL COL	TX_SUC
	0	0	0	0	0	0	0	0

TXUNRN - Transmit Under Run. Set if under run occurs, it also clears TXENA bit in TCR. Cleared by setting TXENA high. This bit may only be set if early TX is being used.

LINK_OK - General purpose input port driven by nLNK pin inverted. Typically used for Link Test. A transition on the value of this bit generates an interrupt.

CTR_ROL - Counter Roll Over. When set one or more 4 bit counters have reached maximum count (15). Cleared by reading the ECR register.

EXC_DEF - Excessive Deferral. When set last/current transmit was deferred for more than 1518 * 2 byte times. Cleared at the end of every packet sent.

LOST_CARR - Lost Carrier Sense. When set indicates that Carrier Sense was not present at end of preamble. Valid only if MON_CSN is enabled. This condition causes TXENA bit in TCR to be reset. Cleared by setting TXENA bit in TCR.

LATCOL - Late collision detected on last transmit frame. If set a late collision was detected (later than 64 byte times into the frame). When detected the transmitter jams and turns itself off clearing the TXENA bit in TCR. Cleared by setting TXENA in TCR.

TX_DEFR - Transmit Deferred. When set, carrier was detected during the first 6.4 μs of the inter frame gap. Cleared at the end of every packet sent.

LTX_BRD - Last transmit frame was a broadcast. Set if frame was broadcast. Cleared at the start of every transmit frame.

SQET - Signal Quality Error Test. This bit is set under the following conditions:

1) LAN91C113 is set to operate in Half Duplex mode (SWFDUP=0);
2) When STP_SQET=1 and SWFDUP=0, SQET bit will be set upon completion of a transmit operation and no SQET Pulse has occurred during the IPG (Inter Frame Gap). If a pulse has occurred during the IPG, SQET bit will not get set.
3) Once SQET bit is set, setting the TXENA bit in TCR register, or via hardware /software reset can clear this bit.

16COL - 16 collisions reached. Set when 16 collisions are detected for a transmit frame. TXENA bit in TCR is reset. Cleared when TXENA is set high.

LTX_MULT - Last transmit frame was a multicast. Set if frame was a multicast. Cleared at the start of every transmit frame.

MULCOL - Multiple collision detected for the last transmit frame. Set when more than one collision was experienced. Cleared when TX_SUC is high at the end of the packet being sent.

SNGLCOL - Single collision detected for the last transmit frame. Set when a collision is detected. Cleared when TX_SUC is high at the end of the packet being sent.

TX_SUC - Last transmit was successful. Set if transmit completes without a fatal error. This bit is cleared by the start of a new frame transmission or when TXENA is set high. Fatal errors are:

- 16 collisions (1/2 duplex mode only)
- SQET fail and STP_SQET = 1 (1/2 duplex mode only)
- FIFO Underrun
- Carrier lost and MON_CSN = 1 (1/2 duplex mode only)
- Late collision (1/2 duplex mode only)

7.7 Bank 0 - Receive Control Register

OFFSET	NAME	TYPE	SYMBOL
4	RECEIVE CONTROL REGISTER	READ/WRITE	RCR

HIGH BYTE	SOFT RST	FILT CAR	ABORT_ENB	Reserved	Reserved	Reserved	STRIP CRC	RXEN
	0	0	0	0	0	0	0	0
LOW BYTE	Reserved	Reserved	Reserved	Reserved	Reserved	ALMUL	PRMS	RX_ ABORT
	0	0	0	0	0	0	0	0

SOFT_RST - Software-Activated Reset. Active high. Initiated by writing this bit high and terminated by writing the bit low. The LAN91C113's configuration is not preserved except for Configuration, Base, and IA0-IA5 Registers. EEPROM is not reloaded after software reset.

FILT_CAR - Filter Carrier. When set filters leading edge of carrier sense for 12 bit times (3 nibble times). Otherwise recognizes a receive frame as soon as carrier sense is active. (Does NOT filter RX DV on MII!)

ABORT_ENB - Enables abort of receive when collision occurs. Defaults low. When set, the LAN91C113 will automatically abort a packet being received when the appropriate collision input is activated. This bit has no effect if the SWFDUP bit in the TCR is set.

STRIP_CRC - When set it strips the CRC on received frames. When clear the CRC is stored in memory following the packet. Defaults low.

RXEN - Enables the receiver when set. If cleared, completes receiving current frame and then goes idle. Defaults low on reset.

ALMUL - When set accepts all multicast frames (frames in which the first bit of DA is '1'). When clear accepts only the multicast frames that match the multicast table setting. Defaults low.

PRMS - Promiscuous mode. When set receives all frames. Does not receive its own transmission unless it is in Full Duplex!

RX_ABORT - This bit is set if a receive frame was aborted due to length longer than 2K bytes. The frame will not be received. The bit is cleared by RESET or by the CPU writing it low.

Reserved - Must be 0.

7.8 Bank 0 - Counter Register

OFFSET	NAME	TYPE	SYMBOL
6	COUNTER REGISTER	READ ONLY	ECR

Counts four parameters for MAC statistics. When any counter reaches 15 an interrupt is issued. All counters are cleared when reading the register and do not wrap around beyond 15.

HIGH BYTE	NUMBER OF EXC. DEFFERED TX				NUMBER OF DEFFERED TX			
	0	0	0	0	0	0	0	0
LOW BYTE	MULTIPLE COLLISION COUNT				SINGLE COLLISION COUNT			
	0	0	0	0	0	0	0	0

Each four bit counter is incremented every time the corresponding event, as defined in the EPH STATUS REGISTER bit description, occurs. Note that the counters can only increment once per enqueued transmit packet, never faster, limiting the rate of interrupts that can be generated by the counters. For example if a packet is successfully transmitted after one collision the SINGLE COLLISION COUNT field is incremented by one. If a packet experiences between 2 to 16 collisions, the MULTIPLE COLLISION COUNT field is incremented by one. If a packet experiences deferral the NUMBER OF DEFERRED TX field is incremented by one, even if the packet experienced multiple deferrals during its collision retries.

The COUNTER REGISTER facilitates maintaining statistics in the AUTO RELEASE mode where no transmit interrupts are generated on successful transmissions.

Reading the register in the transmit service routine will be enough to maintain statistics.

7.9 Bank 0 - Memory Information Register

OFFSET	NAME	TYPE	SYMBOL
8	MEMORY INFORMATION REGISTER	READ ONLY	MIR

HIGH BYTE	FREE MEMORY AVAILABLE (IN BYTES * 2K * M)							
	0	0	0	0	0	1	0	0
LOW BYTE	MEMORY SIZE (IN BYTES *2K * M)							
	0	0	0	0	0	1	0	0

FREE MEMORY AVAILABLE - This register can be read at any time to determine the amount of free memory. The register defaults to the MEMORY SIZE upon POR (Power On Reset) or upon the RESET MMU command.

MEMORY SIZE - This register can be read to determine the total memory size.

All memory related information is represented in 2K * M byte units, where the multiplier M is 1 for LAN91C113.

7.10 Bank 0 - Receive/PHY Control Register

OFFSET	NAME	TYPE	SYMBOL
A	RECEIVE/PHY CONTROL REGISTER	READ/WRITE	RPCR

HIGH BYTE	Reserved	Reserved	SPEED	DPLX	ANEG	Reserved	Reserved	Reserved
	0	0	0	0	0	0	0	0
LOW BYTE	LS2A	LS1A	LS0A	LS2B	LS1B	LS0B	Reserved	Reserved
	0	0	0	0	0	0	0	0

SPEED – Speed select Input. This bit selects 10/100 PHY operation only when the ANEG Bit = 0, this bit overrides the SPEED bit in the PHY Register 0 (Control Register) and determines the speed mode. When this bit is set (1), the Internal PHY will operate at 100Mbps. When this bit is cleared (0), the Internal PHY will operate at 10Mbps. When the ANEG bit = 1, this bit is ignored and 10/100 operation is determined by the outcome of the Auto-negotiation or this bit is overridden by the SPEED bit in the PHY Register 0 (Control Register) when the ANEG_EN bit in the PHY Register 0 (Control Register) is clear.

DPLX – Duplex Select - This bit selects Full/Half Duplex operation. This bit is valid and selects duplex operation only when the ANEG Bit = 0, this bit overrides the DPLX bit in the PHY Register 0 (Control Register) and determines the duplex mode. When this bit is set (1), the Internal PHY will operate at full duplex mode. When this bit is cleared (0), the Internal PHY will operate at half Duplex mode. When the ANEG bit = 1, this bit is ignored and duplex mode is determined by the outcome of the Auto-negotiation or this bit is overridden by the DPLX bit in the PHY Register 0 (Control Register) when the ANEG_EN bit in the PHY Register 0 (Control Register) is clear.

ANEG – Auto-Negotiation mode select - The PHY is placed in Auto-Negotiation mode when both the ANEG bit and the ANEG_EN bit in PHY Register 0 (Control Register) are set. When either of these bits is cleared (0), the PHY is placed in manual mode.

WHAT DO YOU WANT TO DO?	**AUTO-NEGOTIATION CONTROL BITS**		**AUTO-NEGOTIATION ADVERTISEMENT REGISTER**				**DUPLEX MODE CONTROL FOR THE MAC**
Try to Auto-Negotiate to ……	ANEG *Bit*	ANEG_EN *Bit*	*TX_FDX Bit*	*TX_HDX Bit*	*10_FDX Bit*	*10_HDX Bit*	*SWFDUP Bit*
	RPCR (MAC)	Register 0 (PHY)	Register 4 (PHY)	Register 4 (PHY)	Register 4 (PHY)	Register 4 (PHY)	Transmit Control Register (MAC)
100 Full Duplex	1	1	1	1	1	1	1
100 Half Duplex	1	1	0	1	1	1	0
10 Full Duplex	1	1	0	0	1	1	1
10 Half Duplex	1	1	0	0	0	1	0

WHAT DO YOU WANT TO DO?	AUTO-NEGOTIATION CONTROL BITS		SPEED AND DUPLEX MODE CONTROL FOR THE PHY				DUPLEX MODE CONTROL FOR THE MAC
Try to Manually Set to ……	ANEG Bit	ANEG_EN Bit	*SPEED Bit*	*DPLX Bit*	*SPEED Bit*	*DPLX Bit*	*SWFDUP Bit*
	RPCR (MAC Bank 0 Offset A)	Register 0 (PHY)	RPCR (MAC Bank 0 Offset A)	RPCR (MAC Bank 0 Offset A)	Register 0 (PHY)	Register 0 (PHY)	Transmit Control Register (MAC)
100 Full Duplex	0	0	1	1	X	X	1
	0	1	1	1	X	X	1
	1	0	X	X	1	1	1
100 Half Duplex	0	0	1	0	X	X	0
	0	1	1	0	X	X	0
	1	0	X	X	1	0	0
10 Full Duplex	0	0	0	1	X	X	1
	0	1	0	1	X	X	1
	1	0	X	X	0	1	1
10 Half Duplex	0	0	0	0	X	X	0
	0	1	0	0	X	X	0
	1	0	X	X	0	0	0

LS2A, LS1A, LS0A – LED select Signal Enable. These bits define what LED control signals are routed to the LEDA output pin on the LAN91C113 Ethernet Controller. The default is 10/100 Link detected.

LS2A	LS1A	LS0A	LED SELECT SIGNAL – LEDA
0	0	0	nPLED3+ nPLED0 – Logical OR of 100Mbps Link detected 10Mbps Link detected (default)
0	0	1	Reserved
0	1	0	nPLED0 - 10Mbps Link detected
0	1	1	nPLED1 - Full Duplex Mode enabled
1	0	0	nPLED2 - Transmit or Receive packet occurred
1	0	1	nPLED3 - 100Mbps Link detected
1	1	0	nPLED4 - Receive packet occurred
1	1	1	nPLED5 - Transmit packet occurred

LS2B, LS1B, LS0B – LED select Signal Enable. These bits define what LED control signals are routed to the LEDB output pin on the LAN91C113 Ethernet Controller. The default is 10/100 Link detected.

LS2B	LS1B	LS0B	LED SELECT SIGNAL – LEDB
0	0	0	nPLED3+ nPLED0 – Logical OR of 100Mbps Link detected 10Mbps Link detected (default)
0	0	1	Reserved
0	1	0	nPLED0 - 10Mbps Link detected
0	1	1	nPLED1 – Full Duplex Mode enabled
1	0	0	nPLED2 – Transmit or Receive packet occurred
1	0	1	nPLED3 - 100Mbps Link detected
1	1	0	nPLED4 - Receive packet occurred
1	1	1	nPLED5 - Transmit packet occurred

Reserved – Must be 0.

7.11 Bank 1 - Configuration Register

OFFSET	NAME	TYPE	SYMBOL
0	CONFIGURATION REGISTER	READ/WRITE	CR

The Configuration Register holds bits that define the adapter configuration and are not expected to change during run-time. This register is part of the EEPROM saved setup.

HIGH BYTE	EPH Power EN	Reserved	Reserved	NO WAIT	Reserved	GPCNTRL	EXT PHY	Reserved
	1	0	1	0	0	0	0	0
LOW BYTE	Reserved	Reserved	Reserved			Reserved	Reserved	Reserved
	1	0	1	1	0	0	0	1

EPH Power EN - Used to selectively power transition the EPH to a low power mode. When this bit is cleared (0), the Host will place the EPH into a low power mode. The Ethernet MAC will gate the 25Mhz TX and RX clock so that the Ethernet MAC will no longer be able to receive and transmit packets. The Host interface however, will still be active allowing the Host access to the device through Standard IO access. All LAN91C113 registers will still be accessible. However, status and control will not be allowed until the EPH Power EN bit is set AND a RESET MMU command is initiated.

NO WAIT - When set, does not request additional wait states. An exception to this are accesses to the Data Register if not ready for a transfer. When clear, negates ARDY for two to three clocks on any cycle to the LAN91C113.

GPCNTRL - This bit is a general purpose output port. Its inverse value drives pin nCNTRL and it is typically connected to a SELECT pin of the external PHY device such as a power enable. It can be used to select the signaling mode for the external PHY or as a general purpose non-volatile configuration pin. Defaults low.

EXT PHY – External PHY Enabled.

This bit, when set (1):

1) Enables the external MII.
2) The Internal PHY is disabled and is disconnected (Tri-stated from the internal MII along with any sideband signals (such as MDINT) going to the MAC Core).

When this bit is cleared (0 - Default):

1) The internal PHY is enabled.
2) The external MII pins, including the MII Management interface pins are tri-stated.

Reserved – Reserved bits.

7.12 Bank 1 - Base Address Register

OFFSET	NAME	TYPE	SYMBOL
2	BASE ADDRESS REGISTER	READ/WRITE	BAR

This register holds the I/O address decode option chosen for the LAN91C113. It is part of the EEPROM saved setup and is not usually modified during run-time.

HIGH BYTE	A15	A14	A13	A9	A8	A7	A6	A5
	0	0	0	1	1	0	0	0
LOW BYTE	Reserved							Reserved
	0	0	0	0	0	0	0	1

A15 - A13 and A9 - A5 - These bits are compared against the I/O address on the bus to determine the IOBASE for the LAN91C113's registers. The 64k I/O space is fully decoded by the LAN91C113 down to a 16 location space, therefore the unspecified address lines A4, A10, A11 and A12 must be all zeros.

All bits in this register are loaded from the serial EEPROM. The I/O base decode defaults to 300h (namely, the high byte defaults to 18h).

Reserved – Reserved bits.

Below chart shows the decoding of I/O Base Address 300h:

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

7.13 Bank 1 - Individual Address Registers

OFFSET	NAME	TYPE	SYMBOL
4 THROUGH 9	INDIVIDUAL ADDRESS REGISTERS	READ/WRITE	IAR

These registers are loaded starting at word location 20h of the EEPROM upon hardware reset or EEPROM reload. The registers can be modified by the software driver, but a STORE operation will not modify the EEPROM Individual Address contents. Bit 0 of Individual Address 0 register corresponds to the first bit of the address on the cable.

LOW BYTE	ADDRESS 0							
	0	0	0	0	0	0	0	0
HIGH BYTE	ADDRESS 1							
	0	0	0	0	0	0	0	0
LOW BYTE	ADDRESS 2							
	0	0	0	0	0	0	0	0
HIGH BYTE	ADDRESS 3							
	0	0	0	0	0	0	0	0
LOW BYTE	ADDRESS 4							
	0	0	0	0	0	0	0	0
HIGH BYTE	ADDRESS 5							
	0	0	0	0	0	0	0	0

7.14 Bank 1 - General Purpose Register

OFFSET	NAME	TYPE	SYMBOL
A	GENERAL PURPOSE REGISTER	READ/WRITE	GPR

HIGH BYTE	HIGH DATA BYTE							
	0	0	0	0	0	0	0	0
LOW BYTE	LOW DATA BYTE							
	0	0	0	0	0	0	0	0

This register can be used as a way of storing and retrieving non-volatile information in the EEPROM to be used by the software driver. The storage is word oriented, and the EEPROM word address to be read or written is specified using the six lowest bits of the Pointer Register.

This register can also be used to sequentially program the Individual Address area of the EEPROM, that is normally protected from accidental Store operations.

This register will be used for EEPROM read and write only when the EEPROM SELECT bit in the Control Register is set. This allows generic EEPROM read and write routines that do not affect the basic setup of the LAN91C113.

7.15 Bank 1 - Control Register

OFFSET	NAME	TYPE	SYMBOL
C	CONTROL REGISTER	READ/WRITE	CTR

HIGH BYTE	Reserved	RCV_ BAD	Reserved	Reserved	AUTO RELEASE	Reserved	Reserved	Reserved
	0	0	0	1	0	0	1	0
LOW BYTE	LE ENABLE	CR ENABLE	TE ENABLE	Reserved	Reserved	EEPROM SELECT	RELOAD	STORE
	0	0	0	1	0	0	0	0

RCV_BAD - When set, bad CRC packets are received. When clear bad CRC packets do not generate interrupts and their memory is released.

AUTO RELEASE - When set, transmit pages are released by transmit completion if the transmission was successful (when TX_SUC is set). In that case there is no status word associated with its packet number, and successful packet numbers are not even written into the TX COMPLETION FIFO. A sequence of transmit packets will generate an interrupt only when the sequence is completely transmitted (TX EMPTY INT will be set), or when a packet in the sequence experiences a fatal error (TX INT will be set). Upon a fatal error TXENA is cleared and the transmission sequence stops. The packet number that failed, is present in the FIFO PORTS register, and its pages are not released, allowing the CPU to restart the sequence after corrective action is taken.

LE ENABLE - Link Error Enable. When set it enables the LINK_OK bit transition as one of the interrupts merged into the EPH INT bit. Clearing the LE ENABLE bit after an EPH INT interrupt, caused by a LINK_OK transition, will acknowledge the interrupt. LE ENABLE defaults low (disabled).

CR ENABLE - Counter Roll over Enable. When set, it enables the CTR_ROL bit as one of the interrupts merged into the EPH INT bit. Reading the COUNTER register after an EPH INT interrupt caused by a counter rollover, will acknowledge the interrupt. CR ENABLE defaults low (disabled).

TE ENABLE - Transmit Error Enable. When set it enables Transmit Error as one of the interrupts merged into the EPH INT bit. An EPH INT interrupt caused by a transmitter error is acknowledged by setting TXENA bit in the TCR register to 1 or by clearing the TE ENABLE bit. TE ENABLE defaults low (disabled). Transmit Error is any condition that clears TXENA with TX_SUC staying low as described in the EPHSR register.

EEPROM SELECT - This bit allows the CPU to specify which registers the EEPROM RELOAD or STORE refers to. When high, the General Purpose Register is the only register read or written. When low, RELOAD reads Configuration, Base and Individual Address, and STORE writes the Configuration and Base registers.

RELOAD - When set it will read the EEPROM and update relevant registers with its contents. Clears upon completing the operation.

STORE - When set, stores the contents of all relevant registers in the serial EEPROM. Clears upon completing the operation.

Note: When an EEPROM access is in progress the STORE and RELOAD bits will be read back as high. The remaining 14 bits of this register will be invalid. During this time attempted read/write operations, other than polling the EEPROM status, will NOT have any effect on the internal registers. The CPU can resume accesses to the LAN91C113 after both bits are low. A worst case RELOAD operation initiated by RESET or by software takes less than 750 μs.

7.16 Bank 2 - MMU Command Register

OFFSET	NAME	TYPE	SYMBOL
0	MMU COMMAND REGISTER	WRITE ONLY BUSY Bit Readable	MMUCR

This register is used by the CPU to control the memory allocation, de-allocation, TX FIFO and RX FIFO control.

The three command bits determine the command issued as described below:

HIGH BYTE								
								0
LOW BYTE	COMMAND			Reserved	Reserved	Reserved	Reserved	BUSY
	Operation Code							

COMMAND SET:

OPERATION CODE	DECIMAL VALUE	COMMAND
000	0	NOOP - NO OPERATION
001	1	ALLOCATE MEMORY FOR TX
010	2	RESET MMU TO INITIAL STATE - Frees all memory allocations, clears relevant interrupts, resets packet FIFO pointers.
011	3	REMOVE FRAME FROM TOP OF RX FIFO - To be issued after CPU has completed processing of present receive frame. This command removes the receive packet number from the RX FIFO and brings the next receive frame (if any) to the RX area (output of RX FIFO).
100	4	REMOVE AND RELEASE TOP OF RX FIFO - Like 3) but also releases all memory used by the packet presently at the RX FIFO output. The MMU busy time after issuing REMOVE and RELEASE command depends on the time when the busy bit is cleared. The time from issuing REMOVE and RELEASE command on the last receive packet to the time when receive FIFO is empty depends on RX INT bit turning low. An alternate approach can be checking the read RX FIFO register.
101	5	RELEASE SPECIFIC PACKET - Frees all pages allocated to the packet specified in the PACKET NUMBER REGISTER. Should not be used for frames pending transmission. Typically used to remove transmitted frames, after reading their completion status. Can be used following 3) to release receive packet memory in a more flexible way than 4).
110	6	ENQUEUE PACKET NUMBER INTO TX FIFO - This is the normal method of transmitting a packet just loaded into RAM. The packet number to be enqueued is taken from the PACKET NUMBER REGISTER.
111	7	RESET TX FIFOs - This command will reset both TX FIFOs: The TX FIFO holding the packet numbers awaiting transmission and the TX Completion FIFO. This command provides a mechanism for canceling packet transmissions, and reordering or bypassing the transmit queue. The RESET TX FIFOs command should only be used when the transmitter is disabled. Unlike the RESET MMU command, the RESET TX FIFOs does not release any memory.

Notes:

- When using the RESET TX FIFOS command, the CPU is responsible for releasing the memory associated with outstanding packets, or re-enqueuing them. Packet numbers in the completion FIFO can be read via the FIFO ports register before issuing the command.

- MMU commands releasing memory (commands 4 and 5) should only be issued if the corresponding packet number has memory allocated to it.

COMMAND SEQUENCING

A second allocate command (command 1) should not be issued until the present one has completed. Completion is determined by reading the FAILED bit of the allocation result register or through the allocation interrupt.

A second release command (commands 4, 5) should not be issued if the previous one is still being processed. The BUSY bit indicates that a release command is in progress. After issuing command 5, the contents of the PNR should not be changed until BUSY goes low. After issuing command 4, command 3 should not be issued until BUSY goes low.

BUSY BIT - Readable at bit 0 of the MMU command register address. When set indicates that MMU is still processing a release command. When clear, MMU has already completed last release command. BUSY and FAILED bits are set upon the trailing edge of command.

7.17 Bank 2 - Packet Number Register

OFFSET	NAME	TYPE	SYMBOL
2	PACKET NUMBER REGISTER	READ/WRITE	PNR

Reserved	Reserved	PACKET NUMBER AT TX AREA					
0	0	0	0	0	0	0	0

PACKET NUMBER AT TX AREA - The value written into this register determines which packet number is accessible through the TX area. Some MMU commands use the number stored in this register as the packet number parameter. This register is cleared by a RESET or a RESET MMU Command.

OFFSET	NAME	TYPE	SYMBOL
3	ALLOCATION RESULT REGISTER	READ ONLY	ARR

This register is updated upon an ALLOCATE MEMORY MMU command.

FAILED	Reserved	ALLOCATED PACKET NUMBER					
1	0	0	0	0	0	0	0

FAILED - A zero indicates a successful allocation completion. If the allocation fails the bit is set and only cleared when the pending allocation is satisfied. Defaults high upon reset and reset MMU command. For polling purposes, the ALLOC_INT in the Interrupt Status Register should be used because it is synchronized to the read operation. Sequence:

1) Allocate Command
2) Poll ALLOC_INT bit until set
3) Read Allocation Result Register

ALLOCATED PACKET NUMBER - Packet number associated with the last memory allocation request. The value is only valid if the FAILED bit is clear.

Note: For software compatibility with future versions, the value read from the ARR after an allocation request is intended to be written into the PNR as is, without masking higher bits (provided FAILED = 0).

7.18 Bank 2 - FIFO Ports Register

OFFSET	NAME	TYPE	SYMBOL
4	FIFO PORTS REGISTER	READ ONLY	FIFO

This register provides access to the read ports of the Receive FIFO and the Transmit completion FIFO. The packet numbers to be processed by the interrupt service routines are read from this register.

HIGH BYTE	REMPTY	Reserved	RX FIFO PACKET NUMBER						
	1	0	0	0	0	0	0	0	
LOW BYTE	TEMPTY	Reserved	TX FIFO PACKET NUMBER						
	1	0	0	0	0	0	0	0	

REMPTY - No receive packets queued in the RX FIFO. For polling purposes, uses the RCV_INT bit in the Interrupt Status Register.

TOP OF RX FIFO PACKET NUMBER - Packet number presently at the output of the RX FIFO. Only valid if REMPTY is clear. The packet is removed from the RX FIFO using MMU Commands 3) or 4).

TEMPTY - No transmit packets in completion queue. For polling purposes, uses the TX_INT bit in the Interrupt Status Register.

TX FIFO PACKET NUMBER - Packet number presently at the output of the TX FIFO. Only valid if TEMPTY is clear. The packet is removed when a TX INT acknowledge is issued.

Note: For software compatibility with future versions, the value read from each FIFO register is intended to be written into the PNR as is, without masking higher bits (provided TEMPTY and REMPTY = 0 respectively).

7.19 Bank 2 - Pointer Register

OFFSET	NAME	TYPE	SYMBOL
6	POINTER REGISTER	READ/WRITE NOT EMPTY is a read only bit	PTR

HIGH BYTE	RCV	AUTO INCR.	READ	ETEN	NOT EMPTY	POINTER HIGH			
	0	0	0	0	0	0	0	0	
LOW BYTE	POINTER LOW								
	0	0	0	0	0	0	0	0	

POINTER REGISTER - The value of this register determines the address to be accessed within the transmit or receive areas. It will auto-increment on accesses to the data register when AUTO INCR. is set. The increment is by one for every byte access, by two for every word access, and by four for every double word access. When RCV is set the address refers to the receive area and uses the output of RX FIFO as the packet number, when RCV is clear the address refers to the transmit area and uses the packet number at the Packet Number Register.

READ - Determines the type of access to follow. If the READ bit is high the operation intended is a read. If the READ bit is low the operation is a write. Loading a new pointer value, with the READ bit high, generates a pre-fetch into the Data Register for read purposes.

Readback of the pointer will indicate the value of the address last accessed by the CPU (rather than the last pre-fetched). This allows any interrupt routine that uses the pointer, to save it and restore it without affecting the process being interrupted. The Pointer Register should not be loaded until the Data Register

FIFO is empty. The NOT EMPTY bit of this register can be read to determine if the FIFO is empty. On reads, if ARDY is not connected to the host, the Data Register should not be read before 370ns after the pointer was loaded to allow the Data Register FIFO to fill.

If the pointer is loaded using 8 bit writes, the low byte should be loaded first and the high byte last.

ETEN - When set enables EARLY Transmit underrun detection. Normal operation when clear.

NOT EMPTY - When set indicates that the Write Data FIFO is not empty yet. The CPU can verify that the FIFO is empty before loading a new pointer value. This is a read only bit.

Note: If AUTO INCR. is not set, the pointer must be loaded with a dword aligned value.

7.20 Bank 2 - Data Register

OFFSET	NAME	TYPE	SYMBOL
8 THROUGH Bh	DATA REGISTER	READ/WRITE	DATA

DATA HIGH							
X	X	X	X	X	X	X	X
DATA LOW							
X	X	X	X	X	X	X	X

DATA REGISTER - Used to read or write the data buffer byte/word presently addressed by the pointer register.

This register is mapped into two uni-directional FIFOs that allow moving words to and from the LAN91C113 regardless of whether the pointer address is even, odd or dword aligned. Data goes through the write FIFO into memory, and is pre-fetched from memory into the read FIFO. If byte accesses are used, the appropriate (next) byte can be accessed through the Data Low or Data High registers. The order to and from the FIFO is preserved. Byte or word accesses can be mixed on the fly in any order.

This register is mapped into two consecutive word locations to facilitate double word move operations regardless of the actual bus width. The DATA register is accessible at any address in the 8 through Bh range, while the number of bytes being transferred is determined by A1 and nBE0-nBE1. The FIFOs are 12 bytes each.

7.21 Bank 2 - Interrupt Status Registers

OFFSET	NAME	TYPE	SYMBOL
C	INTERRUPT STATUS REGISTER	READ ONLY	IST

MDINT	ERCV INT	EPH INT	RX_OVRN INT	ALLOC INT	TX EMPTY INT	TX INT	RCV INT
0	0	0	0	0	1	0	0

OFFSET	NAME	TYPE	SYMBOL
C	INTERRUPT ACKNOWLEDGE REGISTER	WRITE ONLY	ACK

MDINT	ERCV INT		RX_OVRN INT		TX EMPTY INT	TX INT	

OFFSET	NAME	TYPE	SYMBOL
D	INTERRUPT MASK REGISTER	READ/WRITE	MSK

MDINT MASK	ERCV INT MASK	EPH INT MASK	RX_OVRN INT MASK	ALLOC INT MASK	TX EMPTY INT MASK	TX INT MASK	RCV INT MASK
0	0	0	0	0	0	0	0

This register can be read and written as a word or as two individual bytes.

The Interrupt Mask Register bits enable the appropriate bits when high and disables them when low. A MASK bit being set will cause a hardware interrupt.

MDINT - Set when the following bits in the PHY MI Register 18 (Serial Port Status Output Register) change state.

1) LNKFAIL, 2) LOSSSYNC, 3) CWRD, 4) SSD, 5) ESD, 6) PROL, 7) JAB, 8) SPDDET, 9) DPLXDET.

These bits automatically latch upon changing state and stay latched until they are read. When they are read, the bits that caused the interrupt to happen are updated to their current value. The MDINT bit will be cleared by writing the acknowledge register with MDINT bit set.

ERCV INT - Early receive interrupt. Set whenever a receive packet is being received, and the number of bytes received into memory exceeds the value programmed as ERCV THRESHOLD (Bank 3, Offset Ch). ERCV INT stays set until acknowledged by writing the INTERRUPT ACKNOWLEDGE REGISTER with the ERCV INT bit set.

EPH INT - Set when the Ethernet Protocol Handler section indicates one out of various possible special conditions. This bit merges exception type of interrupt sources, whose service time is not critical to the execution speed of the low level drivers. The exact nature of the interrupt can be obtained from the EPH Status Register (EPHSR), and enabling of these sources can be done via the Control Register. The possible sources are:

LINK - Link Test transition

CTR_ROL - Statistics counter roll over

TXENA cleared - A fatal transmit error occurred forcing TXENA to be cleared. TX_SUC will be low and the specific reason will be reflected by the bits:

TXUNRN - Transmit under-run
SQET - SQE Error
LOST CARR - Lost Carrier
LATCOL - Late Collision
16COL - 16 collisions

Any of the above interrupt sources can be masked by the appropriate ENABLE bits in the Control Register.

1) LE ENABLE (Link Error Enable), 2) CR ENABLE (Counter Roll Over), 3) TE ENABLE (Transmit Error Enable)

EPH INT will only be cleared by the following methods:

a) Clearing the LE ENABLE bit in the Control Register if an EPH interrupt is caused by a LINK_OK transition.
b) Reading the Counter Register if an EPH interrupt is caused by statistics counter roll over.
c) Setting TXENA bit high if an EPH interrupt is caused by any of the fatal transmit error listed above (3.1 to 3.5).

RX_OVRN INT - Set when 1) the receiver aborts due to an overrun due to a failed memory allocation, 2) the receiver aborts due to a packet length of greater than 2K bytes, or 3) the receiver aborts due to the RCV DISCRD bit in the ERCV register set. The RX_OVRN INT bit latches the condition for the purpose of being polled or generating an interrupt, and will only be cleared by writing the acknowledge register with the RX_OVRN INT bit set.

ALLOC INT - Set when an MMU request for TX ram pages is successful. This bit is the complement of the FAILED bit in the ALLOCATION RESULT register. The ALLOC INT bit is cleared by the MMU when the next allocation request is processed or allocation fails.

TX EMPTY INT - Set if the TX FIFO goes empty, can be used to generate a single interrupt at the end of a sequence of packets enqueued for transmission. This bit latches the empty condition, and the bit will stay set until it is specifically cleared by writing the acknowledge register with the TX EMPTY INT bit set. If a real time reading of the FIFO empty is desired, the bit should be first cleared and then read.

The TX_EMPTY MASK bit should only be set after the following steps:

a) A packet is enqueued for transmission
b) The previous empty condition is cleared (acknowledged)

TX INT - Set when at least one packet transmission was completed or any of the below transmit fatal errors occurs:

1) TXUNRN - Transmit under-run
2) SQET - SQE Error
3) LOST CARR - Lost Carrier
4) LATCOL - Late Collision
5) 16COL - 16 collisions

The first packet number to be serviced can be read from the FIFO PORTS register. The TX INT bit is always the logic complement of the TEMPTY bit in the FIFO PORTS register. After servicing a packet number, its TX INT interrupt is removed by writing the Interrupt Acknowledge Register with the TX INT bit set.

RCV INT - Set when a receive interrupt is generated. The first packet number to be serviced can be read from the FIFO PORTS register. The RCV INT bit is always the logic complement of the REMPTY bit in the FIFO PORTS register.

Receive Interrupt is cleared when RX FIFO is empty.

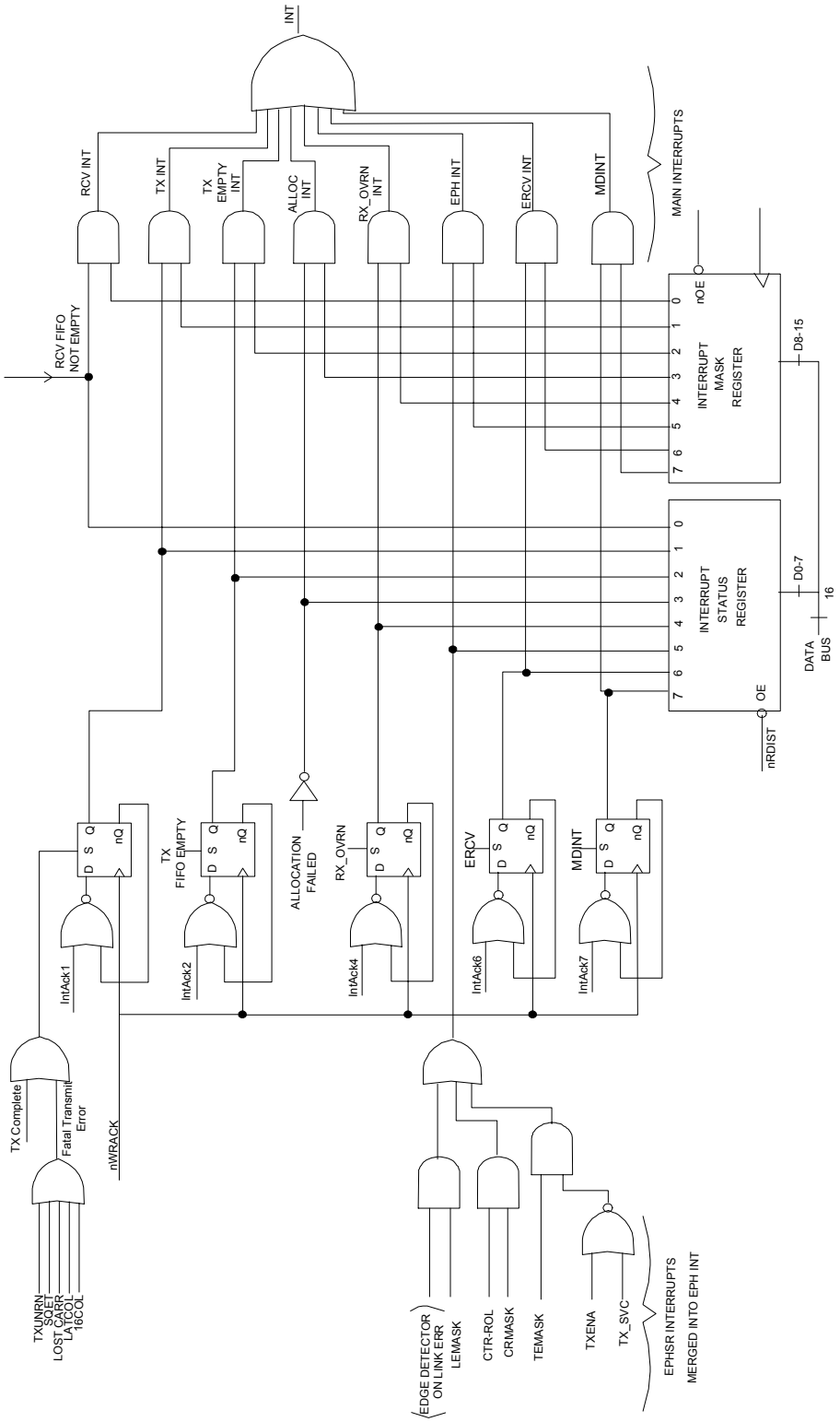


Figure 7.2 - Interrupt Structure

7.22 Bank 3 - Multicast Table Registers

OFFSET	NAME	TYPE	SYMBOL
0 THROUGH 7	MULTICAST TABLE	READ/WRITE	MT

LOW BYTE	MULTICAST TABLE 0								
	0	0	0	0	0	0	0	0	
HIGH BYTE	MULTICAST TABLE 1								
	0	0	0	0	0	0	0	0	
LOW BYTE	MULTICAST TABLE 2								
	0	0	0	0	0	0	0	0	
HIGH BYTE	MULTICAST TABLE 3								
	0	0	0	0	0	0	0	0	
LOW BYTE	MULTICAST TABLE 4								
	0	0	0	0	0	0	0	0	
HIGH BYTE	MULTICAST TABLE 5								
	0	0	0	0	0	0	0	0	
LOW BYTE	MULTICAST TABLE 6								
	0	0	0	0	0	0	0	0	
HIGH BYTE	MULTICAST TABLE 7								
	0	0	0	0	0	0	0	0	

The 64 bit multicast table is used for group address filtering. The hash value is defined as the six most significant bits of the CRC of the destination addresses. The three msb's determine the register to be used (MT0-MT7), while the other three determine the bit within the register.

If the appropriate bit in the table is set, the packet is received.

If the ALMUL bit in the RCR register is set, all multicast addresses are received regardless of the multicast table values.

Hashing is only a partial group addressing filtering scheme, but being the hash value available as part of the receive status word, the receive routine can reduce the search time significantly. With the proper memory structure, the search is limited to comparing only the multicast addresses that have the actual hash value in question.

7.23 Bank 3 - Management Interface

OFFSET	NAME	TYPE	SYMBOL
8	MANAGEMENT INTERFACE	READ/WRITE	MGMT

HIGH BYTE	Reserved	MSK_ CRS100	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	0	0	1	1	0	0	1	1
LOW BYTE	Reserved				MDOE	MCLK	MDI	MDO
	0	0	1	1	0	0	MDI Pin	0

MSK_CRS100 - Disables CRS100 detection during transmit in half duplex mode (SWFDUP=0).

MDO - MII Management output. The value of this bit drives the MDO pin.

MDI - MII Management input. The value of the MDI pin is readable using this bit.

MDCLK - MII Management clock. The value of this bit drives the MDCLK pin.

MDOE - MII Management output enable. When high pin MDO is driven, when low pin MDO is tri-stated.

The purpose of this interface, along with the corresponding pins is to implement MII PHY management in software.

7.24 Bank 3 - Revision Register

OFFSET	NAME	TYPE	SYMBOL
A	REVISION REGISTER	READ ONLY	REV

HIGH BYTE								
	0	0	1	1	0	0	1	1
LOW BYTE	CHIP				REV			
	1	0	0	1	0	0	0	1

CHIP - Chip ID. Can be used by software drivers to identify the device used.

REV - Revision ID. Incremented for each revision of a given device.

7.25 Bank 3 - Early RCV Register

OFFSET	NAME	TYPE	SYMBOL
C	EARLY RCV REGISTER	READ/WRITE	ERCV

HIGH BYTE	Reserved							
	0	0	0	0	0	0	0	0
LOW BYTE	RCV DISCRD	Reserved	Reserved	ERCV THRESHOLD				
	0	0	0	1	1	1	1	1

RCV DISCRD - Set to discard a packet being received. Will discard packets only in the process of being received. When set prior to the end of receive packet, bit 4 (RXOVRN) of the interrupt status register will

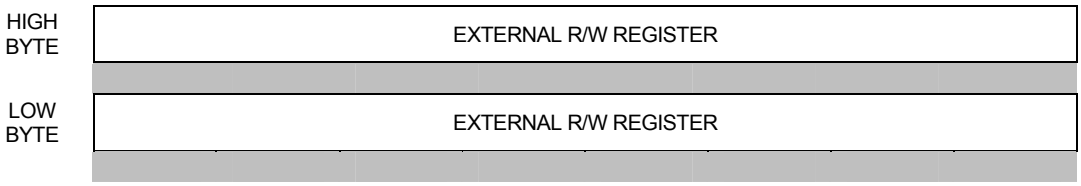
be set to indicate that the packet was discarded. Otherwise, the packet will be received normally and bit 0 set (RCVINT) in the interrupt status register. RCV DISCRD is self clearing.

ERCV THRESHOLD - Threshold for ERCV interrupt. Specified in 64 byte multiples. Whenever the number of bytes written in memory for the presently received packet exceeds the ERCV THRESHOLD, ERCV INT bit of the INTERRUPT STATUS REGISTER is set.

7.26 Bank 7 - External Registers

OFFSET	NAME	TYPE	SYMBOL
0 THROUGH 7	EXTERNAL REGISTERS		

nCSOUT is driven low by the LAN91C113 when a valid access to the EXTERNAL REGISTER range occurs.



CYCLE	NCSOUT	LAN91C113 DATA BUS
AEN=0 A3=0 A4-15 matches I/O BASE BANK SELECT = 7	Driven low. Transparently latched on nADS rising edge.	Ignored on writes. Tri-stated on reads.
BANK SELECT = 4,5,6	High	Ignore cycle.
Otherwise	High	Normal LAN91C113 cycle.

Chapter 8 PHY MII Registers

Multiple Register Access

Multiple registers can be accessed on a single PHY MI serial port access cycle with the multiple register access features. The multiple register access features can be enabled by setting the multiple register access enables bit in the PHY MI serial port Configuration 2 register. When multiple register access is enabled, multiple registers can be accessed on a single PHY MI serial port access cycle by setting the register address to 11111 during the first 16 MDC clock cycles. There is no actual register residing in register address location 11111, so when the register address is then set to 11111, all eleven registers are accessed on the 176 rising edges of MDC that occur after the first 16 MDC clock cycles of the PHY MI serial port access cycle. The registers are accessed in numerical order from 0 to 20. After all 192 MDC clocks have been completed, all the registers have been read/written, and the serial shift process is halted, data is latched into the device, and MDIO goes into high impedance state. Another serial shift cycle cannot be initiated until the idle condition (at least 32 continuous 1's) is detected.

Bit Types

Since the serial port is bi-directional, there are many types of bits. Write bits (W) are inputs during a write cycle and are high impedance during a read cycle. Read bits (R) are outputs during a read cycle and high impedance during a write cycle. Read/Write bits (RW) are actually write bits, which can be read out during a read cycle. R/WSC bits are R/W bits that are self-clearing after a set period of time or after a specific event has completed. R/LL bits are read bits that latch themselves when they go low, and they stay latched low until read. After they are read, they are reset high. R/LH bits are the same as R/LL bits except that they latch high. R/LT are read bits that latch themselves whenever they make a transition or change value, and they stay latched until they are read. After R/LT bits are read, they are updated to their current value. R/LT bits can also be programmed to assert the interrupt function.

Bit Type Definition

R: Read Only
W: Write Only
RW: Read/Write
R/LT: Read/Latch on Transition
R/WSC: Read/Write Self Clearing
R/LH: Read/Latch high
R/LL: Read/Latch low

REGISTER ADDRESS	REGISTER NAME
0	Control
1	Status
2,3	PHY ID
4	Auto-Negotiation Advertisement
5	Auto-Negotiation Remote End Capability
6....15	Reserved
16	Configuration 1
17	Configuration 2
18	Status Output
19	Mask
20	Reserved

PHY Register Description

Table 8.1 - MII Serial Frame Structure

<Idle>	<Start>	<Read>	<Write>	<PHY Addr.>	<REG.Addr.>	<Turnaround>	<Data>
IDLE	ST[1:0]	READ	WRITE	PHYAD[4:0]	REGAD[4:0]	TA[1:0]	D[15:0]

D[15:0]

↓

Register 0	Control
Register 1	Status
Register 2	PHY ID#1
Register 3	PHY ID#2
Register 4	AutoNegotiation Advertisement
Register 5	AutoNegotiation Remote End Capability
Register 16	Configuration 1
Register 17	Configuration 2
Register 18	Status Output
Register 19	Mask
Register 20	Reserved

SYMBOL	NAME	DEFINITION	R/W
IDLE	Idle Pattern	These bits are an idle pattern. Device will not initiate an MI cycle until it detects at least 32 1's	W
ST1 ST0	Start Bits	When ST[1:0]=01, a MI Serial Port access cycle starts.	W
READ	Read Select	1 = Read Cycle	W
WRITE	Write Select	1 = Write Cycle	W
PHYAD[4:0]	Physical Device Address	PHYSICAL ADDRESS	R
REGAD[4:0]	Register Address	If REGAD[4:0] = 00000-11110, these bits determine the specific register from which D[15:0] is read/written. If multiple register access is enabled and REGAD[4:0] = 11111, all registers are read/written in a single cycle.	W
TA1 TA0	Turnaround Time	These bits provide some turnaround time for MDIO When READ = 1, TA[1:0] = Z0 When WRITE = 1, TA[1:0] = 10 The turnaround time is a 2 bit time spacing between the Register Address field and the Data field of a management frame to avoid contention during a read transaction. For a read transaction, both the STA and the PHY shall remain in a high impedance state for the first bit time of the turnaround. The PHY shall drive a zero bit during the second bit time of the turnaround of a read transaction. During a write transaction, the STA shall drive a one bit for the first bit time of the turnaround and a zero bit for the second bit time of the turnaround.	R/W
D[15:0]....	Data	These 16 bits contain data to/from one of the eleven registers selected by register address bits REGAD[4:0].	Any

Table 8.2 - MII Serial Port Register MAP

		x.15	x.14	x.13	x.12	x.11	x.10	x.9	x.8	x.7	x.6	x.5	x.4	x.3	x.2	x.1	x.0
0	Control	RST	LPBK	SPEED	ANEG_EN	PDN	MII_DIS	ANEG_RST	DPLX	COLTST	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		R/WSC	R/W	R/W	R/W	R/W	R/W	R/WSC	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		0	0	1	1	0	1 or 0	0	0	0	0	0	0	0	0	0	0
1	Status	CAP_T4	CAP_TXF	CAP_TXH	CAP_TF	CAP_TH	Reserved	Reserved	Reserved	Reserved	CAP_SUPR	ANEG_ACK	REM_FLT	CAP_ANEG	LINK	JAB	EXREG
		R	R	R	R	R	R	R	R	R	R	R	R/LH	R	R/LL	R/LH	R
		0	1	1	1	1	0	0	0	0	0	0	0	1	0	0	1
2	PHY ID #1	OUI3	OUI4	OUI5	OUI6	OUI7	OUI8	OUI9	OUI10	OUI11	OUI12	OUI13	OUI14	OUI15	OUI16	OUI17	OUI18
		R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
		0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0
3	PHY ID #2	OUI19	OUI20	OUI21	OUI22	OUI23	OUI24	PART5	PART4	PART3	PART2	PART1	PART0	REV3	REV2	REV1	REV0
		R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
		1	1	1	1	1	0	0	0	0	1	0	0	0	0	0	0
4	AutoNegot. Advertisement	NP	ACK	RF	Reserved	Reserved	Reserved	T4	TX_FDX	TX_HDX	10_FDX	10_HDX	Reserved	Reserved	Reserved	Reserved	CSMA
		R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	1
5	AutoNegot. Remote Capability	NP	ACK	RF	Reserved	Reserved	Reserved	T4	TX_FDX	TX_HDX	10_FDX	10_HDX	Reserved	Reserved	Reserved	Reserved	CSMA
		R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16	Configuration 1	LNKDIS	XMTDIS	XMTPDN	Reserved	Reserved	BYPSCR	UNSCDS	EQLZR	CABLE	RLVL0	TLVL3	TLVL2	TLVL1	TLVL0	TRF1	TRF0
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0
17	Configuration 2	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	APOLDIS	JABDIS	MREG	INTMDIO	Reserved	Reserved
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
18	Status Output	INT	LNKFAIL	LOSSSYNC	CWRD	SSD	ESD	RPOL	JAB	SPDDET	DPLXDET	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		R	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R	R	R	R
		0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
19	Mask	MINT	MLNKFAIL	MLOSSSYN	MCWRD	MSSD	MESD	MRPOL	MJAB	MSPDDT	MDPLDT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
20	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

8.1 Register 0. Control Register

RST	LPBK	SPEED	ANEG_EN	PDN	MII_DIS	ANEG_RST	DPLX
RW, SC	RW	RW	RW	RW	RW	RW. SC	RW
0	0	1	1	0	1	0	0

COLST	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

RST - Reset

A '1' written to this bit will initiate a reset of the PHY. The bit is self-clearing, and the PHY will return a '1' on reads to this bit until the reset is completed. Write transactions to this register may be ignored while the PHY is processing the reset. All PHY registers will be driven to their default states after a reset. The internal PHY is guaranteed to be ready for normal operation 50 mS after the RST bit is set. The software driver must wait for 50mS after setting the RST bit high to access the internal PHY again.

LPBK - Loopback

Writing a '1' will put the PHY into loopback mode.

Speed (Speed Selection)

When Auto Negotiation is disabled this bit can be used to manually select the link speed. Writing a '1' to this bit selects 100 Mbps, a '0' selects 10 Mbps.

When Auto-Negotiation is enabled reading or writing this bit has no meaning/effect.

ANEN_EN - Auto-Negotiation Enable

Auto-negotiation (ANEG) is on when this bit is '1'. In that case the contents of bits Speed and Duplex are ignored and the ANEG process determines the link configuration.

PDN - Power down

Setting this bit to '1' will put the PHY in PowerDown mode. In this state the PHY will respond to management transactions.

MII_DIS - MII DISABLE

Setting this bit will set the PHY to an isolated mode in which it will respond to MII management frames over the MII management interface but will ignore data on the MII data interface. *The internal PHY is placed in isolation mode at power up and reset. It can be removed from isolation mode by clearing the MII_DIS bit in the PHY Control Register. If necessary, the internal PHY can be enabled by clearing the EXT_PHY bit in the Configuration Register.*

ANEG_RST - Auto-Negotiation Reset

This bit will return 0 if the PHY does not support ANEG or if ANEG is disabled through the ANEG_EN bit. If neither of the previous is true, setting this bit to '1' resets the ANEG process. This bit is self clearing and the PHY will return a '1' until ANEG is initiated, writing a '0' does not affect the ANEG process.

DPLX - Duplex mode

When Auto Negotiation is disabled this bit can be used to manually select the link duplex state. Writing a '1' to this bit selects full duplex while a '0' selects half duplex.

When Auto-Negotiation is enabled reading or writing this bit has no effect.

COLTST - Collision test

Setting a '1' allows for testing of the MII COL signal. '0' allows normal operation.

Reserved: Reserved, Must be 0 for Proper Operation

8.2 Register 1. Status Register

CAP_T4	CAP_TXF	CAP_TXH	CAP_TF	CAP_TH	Reserved	Reserved.	Reserved
R	R	R	R	R	R	R	R
0	1	1	1	1	0	0	0

Reserved	CAP_SUPR	ANEG_ACK	REM_FLT	CAP_ANEG	LINK	JAB	EXREG
R	R	R	R, LH	R	R, LL	R, LH	R
0	0	0	0	1	0	0	1

CAP_T4 - 100BASE-T4 Capable

'1' Indicates 100Base-T4 capable PHY, '0' not capable.

CAP_TXF - 100BASE-TX Full Duplex Capable

'1' Indicates 100Base-X full duplex capable PHY, '0' not capable.

CAP_TXH - 100BASE-TX Half Duplex Capable

'1' Indicates 100Base-X alf duplex capable PHY, '0' not capable.

CAP_TF - 10BASE-T Full Duplex Capable

'1' Indicates 10Mbps full duplex capable PHY, '0' not capable.

CAP_TH - 10BASE-T Half Duplex Capable

'1' Indicates 10Mbps half duplex capable PHY, '0' not capable.

Reserved: Reserved, Must be 0 for Proper Operation.

CAP_SUPR - MI Preamble Suppression Capable

'1' indicates the PHY is able to receive management frames even if not preceded by a preamble. '0' when it is not able.

ANEG_ACK - Auto-Negotiation Acknowledgment

When read as '1' indicate ANEG has been completed and that contents in registers 4,5,6 and 7 are valid. '0' means ANEG has not completed and contents in registers 4,5,6 and 7 are meaningless. The PHY returns zero if ANEG is disabled.

REM_FLT- Remote Fault Detect

'1' indicates a Remote Fault. Latches the '1' condition and is cleared by reading this register or resetting the PHY.

CAP_ANEG - AutoNegotiation Capable

Indicates the ability ('1') to perform ANEG or not ('0').

LINK - Link Status

A '1' indicates a valid Link and a '0' and invalid Link. The '0' condition is latched until this register is read.

JAB - Jabber Detect

Jabber condition detected when ‘1’ for 10Mbps. ‘1’ latched until this register is read or the PHY is reset. Always ‘0’ for 100Mbps

EXREG - Extended Capability register

‘1’ Indicates extended registers are implemented

8.3 Register 2&3. PHY Identifier Register

These two registers (offsets 2 and 3) provide a 32-bit value unique to the PHY.

REG	BITS	NAME	DEFAULT VALUE	R/W	SOFT RESET
2	15-0	Company ID	0000000000010110	R	Retains Original Value
3	15-10	Company ID	111110	R	Retains Original Value
3	9-4	Manufacturer's ID	000100	R	Retains Original Value
3	3-0	Manufacturer's Revision #	- - - -	R	Retains Original Value

8.4 Register 4. Auto-Negotiation Advertisement Register

NP	ACK	RF	Reserved	Reserved	Reserved	T4	TX_FDX
RW	R	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	1

TX_HDX	10_FDX	10_HDX	Reserved	Reserved	Reserved	Reserved	CSMA
RW	RW	RW	RW	RW	RW	RW	RW
1	1	1	0	0	0	0	1

This register control the values transmitted by the PHY to the remote partner when advertising its abilities

NP - Next Page

A ‘1’ indicates the PHY wishes to exchange Next Page information.

ACK - Acknowledge

It is used by the Auto-negotiation function to indicate that a device has successfully received its Link Partner’s Link code Word.

RF - Remote Fault

When set, an advertisement frame will be sent with the corresponding bit set. This in turn will cause the PHY receiving it to set the Remote Fault bit in its Status register

T4 - 100BASE-T4

A '1' indicates the PHY is capable of 100BASE-T4

TX_FDX - 100BASE-TX Full Duplex Capable

A '1' indicates the PHY is capable of 100BASE-TX Full Duplex

TX_HDX - 100BASE-TX Half Duplex Capable

A '1' indicates the PHY is capable of 100BASE-TX Half Duplex

10_FDX - 10BASE-T Full Duplex Capable

A '1' indicates the PHY is capable of 10BASE-T Full Duplex

10_HDX - 10BASE-T Half Duplex Capable

A '1' indicates the PHY is capable of 10BASE-T Half Duplex

The management entity sets the value of this field prior to AutoNegotiation.

'1' in these bit indicates that the mode of operation that corresponds to these will be acceptable to be auto-negotiated to. Only modes supported by the PHY can be set.

CSMA

A '1' indicates the PHY is capable of 802.3 CSMA Operation

8.5 Register 5. Auto-Negotiation Remote End Capability Register

NP	ACK	RF	Reserved	Reserved	Reserved	T4	TX_FDX
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

TX_HDX	10_FDX	10_HDX	Reserved	Reserved	Reserved	Reserved	CSMA
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

The bit definitions are analogous to the Auto Negotiation Advertisement Register.

8.6 Register 16. Configuration 1-- Structure and Bit Definition

LNKDIS	XMTDIS	XMTPDN	Reserved	Reserved	BYPSCR	UNSCDS	EQLZR
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

CABLE	RLVL0	TLVL3	TLVL2	TLVL1	TLVL0	TRF1	TRF0
RW	RW	RW	RW	RW	RW	RW	RW
0	0	1	0	0	0	1	0

LNKDIS: Link Disable — 1 = Receive Link Detect Function Disabled (Force Link Pass)
0 = Normal

XMTDIS: TP Transmit — 1 = TP Transmitter Disabled
0 = Normal

XMTPDN: TP Transmit Powerdown — 1 = TP Transmitter Powered Down
0 = Normal

RESERVED: *RESERVED* — Reserved, Must be 0 for Proper Operation

BYPSCR: Bypass Scrambler/Descr-ambler Select — 1 = Bypass Scrambler/Descrambler
0 = No Bypass

UNSCDS: Unscrambled Idle Reception Disable — 1 = Disable AutoNegotiation with devices that transmit unscrambled idle on powerup and various instances
0 = Enables AutoNegotiation with devices that transmit unscrambled idle on powerup and various instances

EQLZR: Receive Equalizer Select — 1 = Receive Equalizer Disabled, Set To 0 Length; 0 = Receive Equalizer On (For 100MB Mode Only)

CABLE Cable Type Select — 1 = STP (150 Ohm); 0 = UTP (100 Ohm)

RLVL0 Receive Input Level Adjust — 1 = Receive Squelch Levels Reduced By 4.5 dB R/W; 0 = Normal

TLVL0-3 Transmit OutputSee Table 3 Level Adjust

TRF0-1 Transmitter Rise/Fall Time Adjust — 11 = -0.25nS; 10 = +0.0nS; 01 = +0.25nS; 00 = +0.50nS

8.7 Register 17. Configuration 2 - Structure and Bit Definition

Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R	R	R	R	R	R	R	R
1	1	1	1	1	1	1	1

Reserved	Reserved	APOLDIS	JABDIS	MREG	INTMDIO	Reserved	Reserved
R	R	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

APOLDIS: Auto Polarity Disable — 1 = Auto Polarity Correction Function Disabled; 0 = Normal

JABDIS: Jabber Disable Select — 1 = Jabber Disabled R/W; 0 = Enabled

MREG: Multiple Register Access Enable — 1 = Multiple Register Access Enabled; 0 = No Multiple Register Access

INTMDIO: Interrupt Scheme Select — 1= Interrupt Signaled With MDIO Pulse During Idle; 0 = Interrupt Not Signaled On MDIO

RESERVED: Reserved for Factory Use

8.8 Register 18. Status Output - Structure and Bit Definition

INT	LNKFAIL	LOSSSYNC	CWRD	SSD	ESD	RPOL	JAB
R	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT
0	0	0	0	0	0	0	0

SPDDET	DPLXDET	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R/LT	R/LT	R	R	R	R	R	R
1	0	0	0	0	0	0	0

INT: Interrupt Detect — 1 = Interrupt Bit(s) Have Changed Since Last Read Operation. 0 = No Change

LNKFAIL: Link Fail Detect — 1 = Link Not Detected; 0 = Normal

LOSSSYNC: Descrambler Loss of Synchronization Detect — 1 = Descrambler Has Lost Synchronization; 0 = Normal

CWRD: Codeword Error — 1 = Invalid 4B5B Code Detected On Receive Data; 0 = Normal

SSD: Start Of Stream Error — 1 = No Start Of Stream Delimiter Detected on Receive Data; 0 = Normal

ESD: End Of Stream Error — 1 = No End Of Stream Delimiter Detected on Receive Data; 0 = Normal

RPOL: Reverse Polarity Detect — 1 = Reverse Polarity Detected; 0 = Normal

JAB: Jabber Detect — 1 = Jabber Detected; 0 = Normal

SPDDET: 100/10 Speed Detect — 1 = Device in 100Mbps Mode (100BASE-TX); 0 = Device in 10Mbps Mode (10BASE-T)

DPLXDET: Duplex Detect — 1 = Device In Full Duplex; 0 = Device In Half Duplex

Reserved: Reserved — Reserved for Factory Use

8.9 Register 19. Mask - Structure and Bit Definition

MINT	MLNKFAIL	MLOSSSYN	MCWRD	MSSD	MESD	MRPOL	MJAB
RW	RW	RW	RW	RW	RW	RW	RW
1	1	1	1	1	1	1	1

MSPDDT	MDPLDT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
RW	RW	RW	RW	RW	RW	RW	RW
1	1	0	0	0	0	0	0

MINT: Interrupt Mask Interrupt Detect — 1 = Mask Interrupt For INT In Register 18; 0 = No Mask

MLNKFAIL: Interrupt Mask Link Fail Detect — 1 = Mask Interrupt For LNKFAIL In Register 18; 0 = No Mask

MLOSSSYN: Interrupt Mask Descrambler Loss of Synchronization Detect — 1 = Mask Interrupt For LOSSSYNC In Register 18; 0 = No Mask

MCWRD: Interrupt Mask Codeword Error — 1 = Mask Interrupt For CWRD In Register 18; 0 = No Mask

MSSD: Interrupt Mask Start Of Stream Error — 1 = Mask Interrupt For SSD In Register 18; 0 = No Mask

MESD: Interrupt Mask End Of Stream Error — 1 = Mask Interrupt For ESD In Register 18; 0 = No Mask

MRPOL:	Interrupt Mask Reverse Polarity Detect	1 = Mask Interrupt For RPOL In Register 18 0 = No Mask
MJAB:	Interrupt Mask Jabber Detect	1 = Mask Interrupt For JAB In Register 18 0 = No Mask
MSPDDT:	Interrupt Mask 100/10 Speed Detect	1 = Mask Interrupt For SPDDET In Register 18 0 = No Mask
MDPLDT:	Interrupt Mask Duplex Detect	1 = Mask Interrupt For DPLXDET In Register 18 0 = No Mask
Reserved:	Reserved	Reserved for Factory Use

8.10 Register 20. Reserved - Structure and Bit Definition

Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
RW	RW	RW	RW	RW	RW	RW	RW
1	0	1	0	0	0	0	0

Reserved: Reserved for Factory Use

Chapter 9 Software Driver and Hardware Sequence Flow

9.1 Software Driver and Hardware Sequence Flow for Power Management

This section describes the sequence of events and the interaction between the Host Driver and the Ethernet controller to perform power management. The Ethernet controller has the ability to reduce its power consumption when the Device is not required to receive or transmit Ethernet Packets.

Power Management is obtained by disabling the EPH clocks, including the Clocks derived from the Internal PHY block to reduce internal switching, this reducing current consumption.

The Host interface however, will still be accessible. As discussed in Table 9.1 - Typical Flow Of Events For Placing Device In Low Power Mode and Table 9.2 - Flow Of Events For Restoring Device In Normal Power Mode, the tables describe the interaction between the EPH and Host driver allowing the Device to transition from low power state to normal functionality and vice versa.

Table 9.1 - Typical Flow Of Events For Placing Device In Low Power Mode

	S/W DRIVER	CONTROLLER FUNCTION
1	Disable Transmitter – Clear the TXENA bit of the Transmit Control Register	Ethernet MAC finishes packet currently being transmitted.
2	Remove and release all TX completion packet numbers on the TX completion FIFO.	
3	Disable Receiver – Clear the RXEN bit of the Receive Control Register.	The receiver completes receiving the current frame, if any, and then goes idle. Ethernet MAC will no longer receive any packets.
4	Process all Received packets and Issue a Remove and Release command for each respective RX packet buffer.	RX and TX completion FIFO's are now Empty and all MMU packet numbers are now free.
5	Disable Interrupt sources – Clear the Interrupt Status Register	
	Save Device Context – Save all Specific Register Values set by the driver.	
6	Set PDN bit in PHY MI Register 0 to 1	
7		The internal PHY entered in powerdown mode, the TP outputs are in high impedance state.
8	Write 0 to the "EPH Power EN" Bit located in the configuration register, Bank 1 Offset 0.	
9		Ethernet MAC gates the RX Clock, TX clock derived from the Internal PHY. The EPH Clock is also disabled.

	S/W DRIVER	CONTROLLER FUNCTION
10	The Ethernet MAC is now in low power mode. The Host may access all Runtime IO mapped registers. All IO registers are still accessible. However, the Host should not read or write to the registers with the exception of: Configuration Register Control Register Bank Register	

Table 9.2 - Flow Of Events For Restoring Device In Normal Power Mode

	S/W DRIVER	CONTROLLER FUNCTION
1	Write and set (1) the “EPH Power EN” Bit, located in the configuration register, Bank 1 Offset 0.	
2		Ethernet MAC Enables the RX Clock, TX clock derived from the Internal PHY. The EPH Clock is also enabled.
3	Write the PDN bit in PHY MI Register 0 to 0	This will set the PHY in isolation mode (MII_DIS bit is set). Need to clear this MII_DIS bit, and, need 500ms for the PHY to restore to normal.
4		Internal PHY entered normal operation mode
5	Issue MMU Reset Command	
6	Restore Device Register Level Context.	
7	Enable Transmitter – Set the TXENA bit of the Transmit Control Register	Ethernet MAC can now transmit Ethernet Packets.
8	Enable Receiver – Set (1) the RXEN bit of the Receive Control Register.	Ethernet MAC is now able to receive Packets.
9		Ethernet MAC is now restored for normal operation.

9.2 Typical Flow of Events for Transmit (Auto Release = 0)

	S/W DRIVER	MAC SIDE
1	ISSUE ALLOCATE MEMORY FOR TX - N BYTES - the MMU attempts to allocate N bytes of RAM.	
2	WAIT FOR SUCCESSFUL COMPLETION CODE - Poll until the ALLOC INT bit is set or enable its mask bit and wait for the interrupt. The TX packet number is now at the Allocation Result Register.	
3	LOAD TRANSMIT DATA - Copy the TX packet number into the Packet Number Register. Write the Pointer Register, then use a block move operation from the upper layer transmit queue into the Data Register.	
4	ISSUE "ENQUEUE PACKET NUMBER TO TX FIFO" - This command writes the number present in the Packet Number Register into the TX FIFO. The transmission is now enqueued. No further CPU intervention is needed until a transmit interrupt is generated.	

	S/W DRIVER	MAC SIDE
5		The enqueued packet will be transferred to the MAC block as a function of TXENA (nTCR) bit and of the deferral process (1/2 duplex mode only) state.
6		a) Upon transmit completion the first word in memory is written with the status word. The packet number is moved from the TX FIFO into the TX completion FIFO. Interrupt is generated by the TX completion FIFO being not empty. b) If a TX failure occurs on any packets, TX INT is generated and TXENA is cleared, transmission sequence stops. The packet number of the failure packet is presented at the TX FIFO PORTS Register.
7	a) SERVICE INTERRUPT - Read Interrupt Status Register. If it is a transmit interrupt, read the TX FIFO Packet Number from the FIFO Ports Register. Write the packet number into the Packet Number Register. The corresponding status word is now readable from memory. If status word shows successful transmission, issue RELEASE packet number command to free up the memory used by this packet. Remove packet number from completion FIFO by writing TX INT Acknowledge Register. b) Option 1) Release the packet. Option 2) Check the transmit status in the EPH STATUS Register, write the packet number of the current packet to the Packet Number Register, re-enable TXENA, then go to step 4 to start the TX sequence again.	

9.3 Typical Flow of Events for Transmit (Auto Release = 1)

	S/W DRIVER	MAC SIDE
1	ISSUE ALLOCATE MEMORY FOR TX - N BYTES - the MMU attempts to allocate N bytes of RAM.	
2	WAIT FOR SUCCESSFUL COMPLETION CODE - Poll until the ALLOC INT bit is set or enable its mask bit and wait for the interrupt. The TX packet number is now at the Allocation Result Register.	
3	LOAD TRANSMIT DATA - Copy the TX packet number into the Packet Number Register. Write the Pointer Register, then use a block move operation from the upper layer transmit queue into the Data Register.	

	S/W DRIVER	MAC SIDE
4	ISSUE "ENQUEUE PACKET NUMBER TO TX FIFO" - This command writes the number present in the Packet Number Register into the TX FIFO. The transmission is now enqueued. No further CPU intervention is needed until a transmit interrupt is generated.	
5		The enqueued packet will be transferred to the MAC block as a function of TXENA (nTCR) bit and of the deferral process (1/2 duplex mode only) state.
6		Transmit pages are released by transmit completion.
7		a) The MAC generates a TXEMPTY interrupt upon a completion of a sequence of enqueued packets. b) f a TX failure occurs on any packets, TX INT is generated and TXENA is cleared, transmission sequence stops. The packet number of the failure packet is presented at the TX FIFO PORTS Register.
8	a) SERVICE INTERRUPT – Read Interrupt Status Register, exit the interrupt service routine. b) Option 1) Release the packet. Option 2) Check the transmit status in the EPH STATUS Register, write the packet number of the current packet to the Packet Number Register, re-enable TXENA, then go to step 4 to start the TX sequence again.	

9.4 Typical Flow of Event For Receive

	S/W DRIVER	MAC SIDE
1	ENABLE RECEPTION - By setting the RXEN bit.	
2		A packet is received with matching address. Memory is requested from MMU. A packet number is assigned to it. Additional memory is requested if more pages are needed.
3		The internal DMA logic generates sequential addresses and writes the receive words into memory. The MMU does the sequential to physical address translation. If overrun, packet is dropped and memory is released.
4		When the end of packet is detected, the status word is placed at the beginning of the receive packet in memory. Byte count is placed at the second word. If the CRC checks correctly the packet number is written into the RX FIFO. The RX FIFO, being not empty, causes RCV INT (interrupt) to be set. If CRC is incorrect the packet memory is released and no interrupt will occur.

	S/W DRIVER	MAC SIDE
5	SERVICE INTERRUPT - Read the Interrupt Status Register and determine if RCV INT is set. The next receive packet is at receive area. (Its packet number can be read from the FIFO Ports Register). The software driver can process the packet by accessing the RX area, and can move it out to system memory if desired. When processing is complete the CPU issues the REMOVE AND RELEASE FROM TOP OF RX command to have the MMU free up the used memory and packet number.	

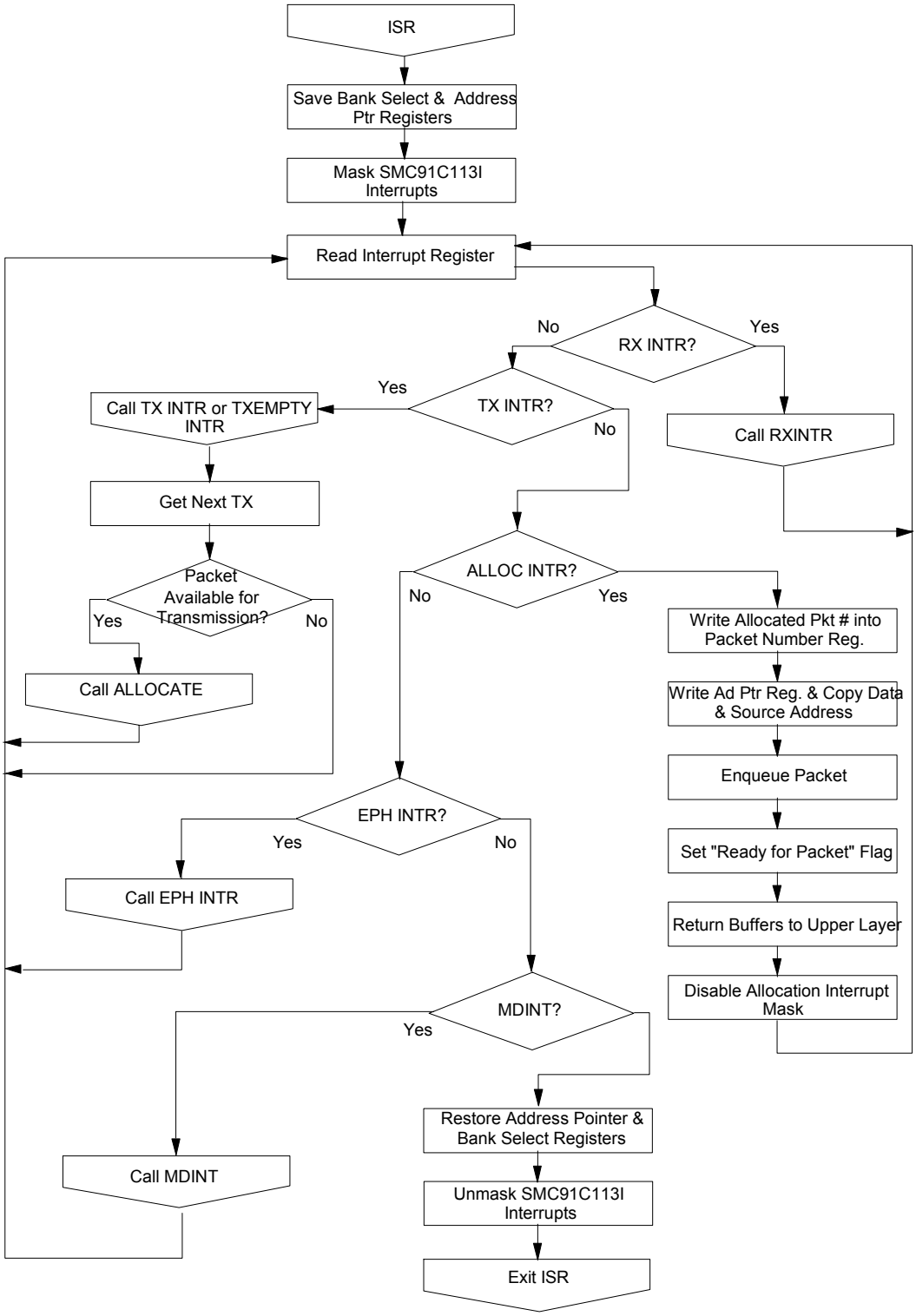


Figure 9.1 - Interrupt Service Routine

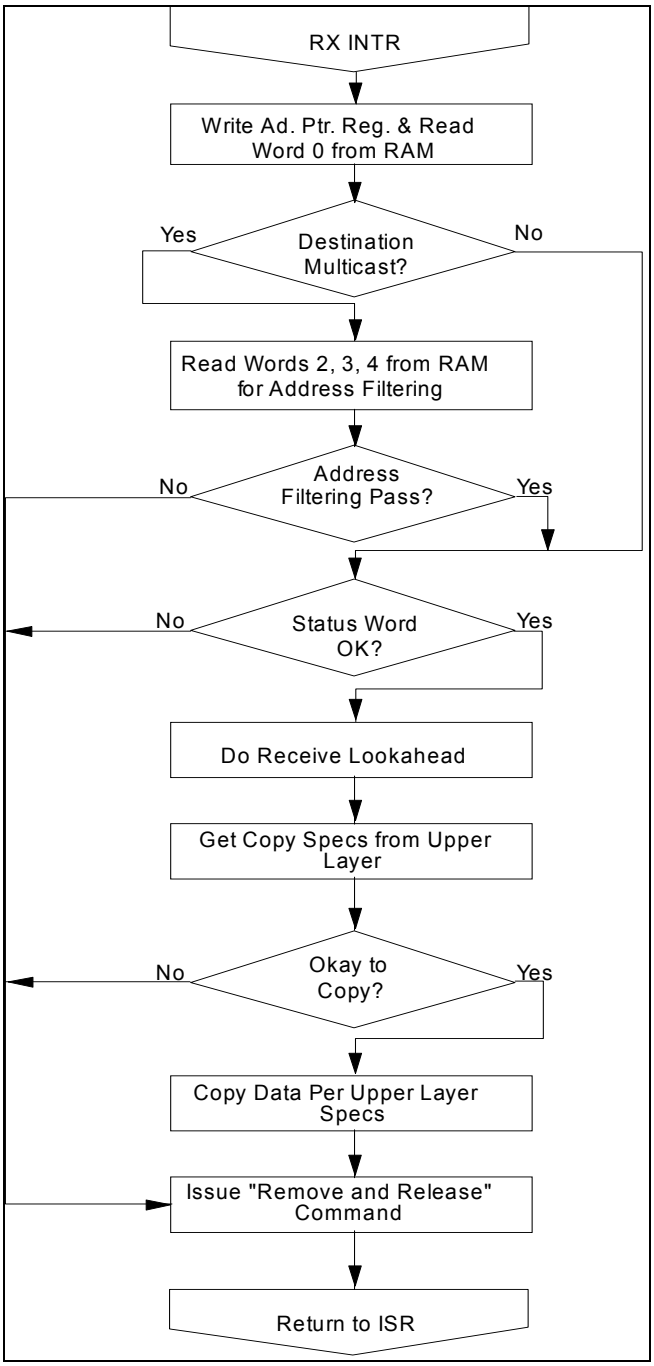


Figure 9.2 - RX INTR

TX Interrupt With AUTO_RELEASE = FALSE

1. Save the Packet Number Register
   Saved_PNR = Read **Byte** (Bank 2, Offset 2)

2. Read the EPH Status Register

   Temp = Read (Bank 0, Offset 2)

3. Acknowledge TX Interrupt
   Write **Byte** (0x02, (Bank 2, Offset C));

4. Check for Status of Transmission

```
If ( Temp AND 0x0001)
{
        //If Successful Transmission
        Step 4.1.1: Issue MMU Release (Release Specific Packet)
                Write (0x00A0, (Bank2, Offset 0));

        Step 4.1.2: Return from the routine
}
else
{
        //Transmission has FAILED

        // Now we can either release or re-enqueue the packet
        Step 4.2.1: Get the packet to release/re-enqueue, stored in FIFO
                Temp = Read (Bank 2, Offset 4)
                Temp = Temp & 0x003F

        Step 4.2.2: Write to the PNR
                Write (Temp, (Bank2, Offset 2))

        Step 4.2.3
                // Option 1: Release the packet
                        Write (0x00A0, (Bank2, Offset 0));
                //Option 2: Re-Enqueue the packet
                        Write (0x00C0, (Bank2, Offset 0));

        Step 4.2.4: Re-Enable Transmission
                Temp = Read(Bank0, Offset 0);
                Temp = Temp2 OR 0x0001
                Write (Temp2, (Bank 0, Offset 0));

        Step 4.2.5: Return from the routine

}
```

5. Restore the Packet Number Register
   Write **Byte** (Saved_PNR, (Bank 2, Offset 2))

Figure 9.3 - TX INTR

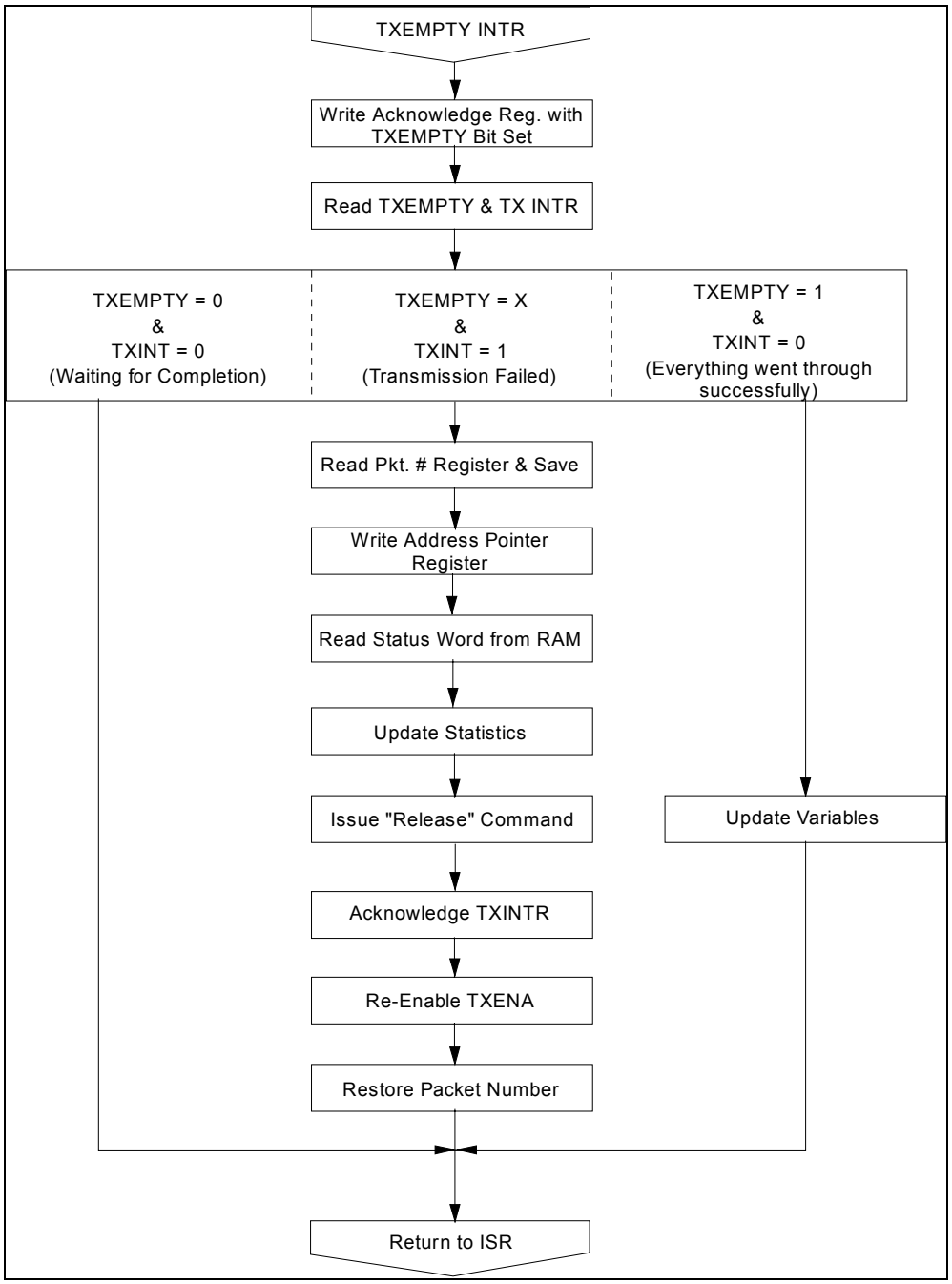


Figure 9.4 - TXEMPTY INTR (Assumes Auto Release Option Selected)

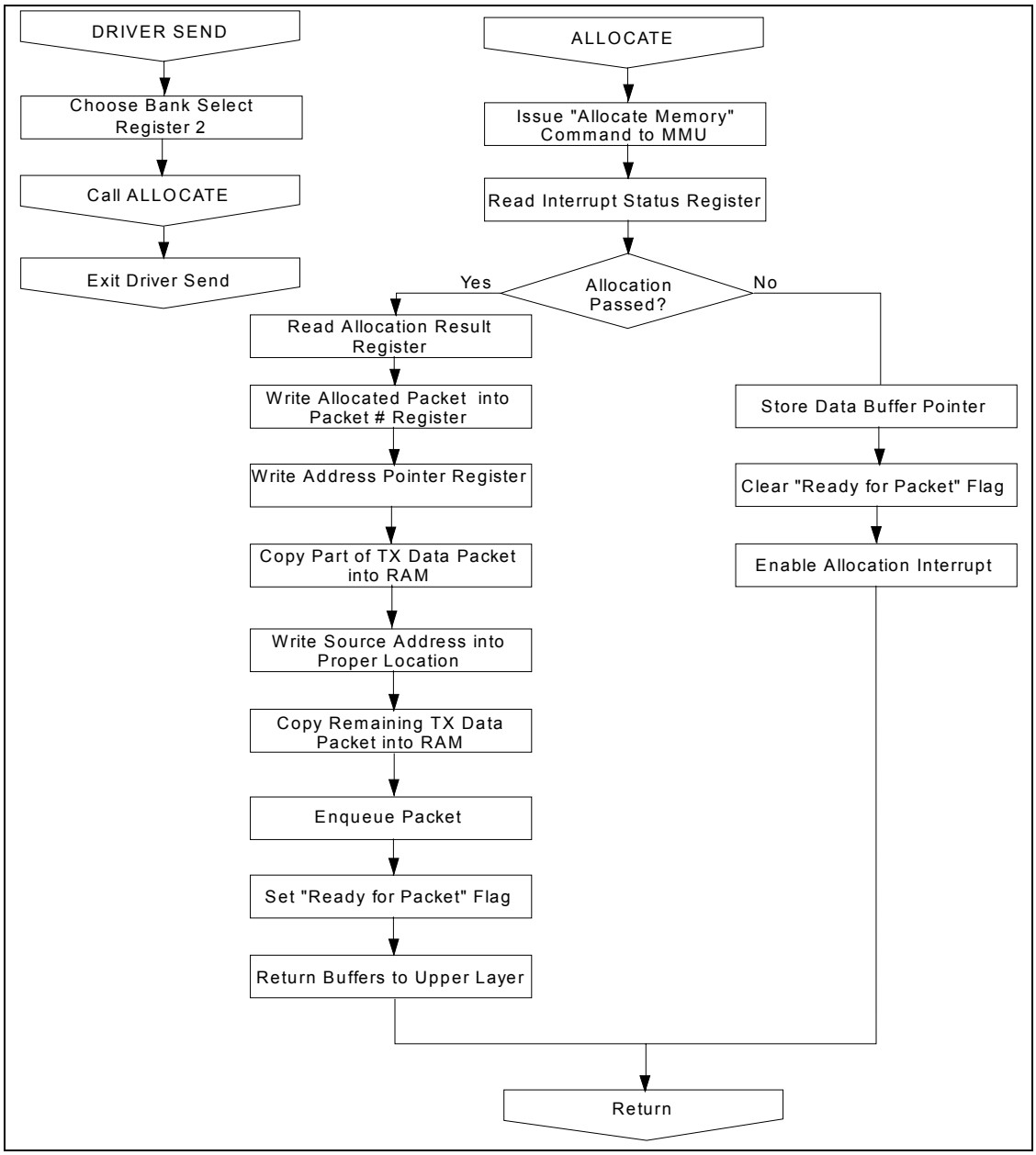


Figure 9.5 – Drive Send and Allocate Routines

MEMORY PARTITIONING

Unlike other controllers, the LAN91C113 does not require a fixed memory partitioning between transmit and receive resources. The MMU allocates and de-allocates memory upon different events. An additional mechanism allows the CPU to prevent the receive process from starving the transmit memory allocation.

Memory is always requested by the side that needs to write into it, that is: the CPU for transmit or the MAC for receive. The CPU can control the number of bytes it requests for transmit but it cannot determine the number of bytes the receive process is going to demand. Furthermore, the receive process requests will be dependent on network traffic, in particular on the arrival of broadcast and multicast packets that might not be for the node, and that are not subject to upper layer software flow control.

INTERRUPT GENERATION

The interrupt strategy for the transmit and receive processes is such that it does not represent the bottleneck in the transmit and receive queue management between the software driver and the controller. For that purpose there is no register reading necessary before the next element in the queue (namely transmit or receive packet) can be handled by the controller. The transmit and receive results are placed in memory.

The receive interrupt will be generated when the receive queue (FIFO of packets) is not empty and receive interrupts are enabled. This allows the interrupt service routine to process many receive packets without exiting, or one at a time if the ISR just returns after processing and removing one.

There are two types of transmit interrupt strategies:

1) One interrupt per packet.

2) One interrupt per sequence of packets.

The strategy is determined by how the transmit interrupt bits and the AUTO RELEASE bit are used.

TX INT bit - Set whenever the TX completion FIFO is not empty.

TX EMPTY INT bit - Set whenever the TX FIFO is empty.

AUTO RELEASE - When set, successful transmit packets are not written into completion FIFO, and their memory is released automatically.

1) One interrupt per packet: enable TX INT, set AUTO RELEASE=0. The software driver can find the completion result in memory and process the interrupt one packet at a time. Depending on the completion code the driver will take different actions. Note that the transmit process is working in parallel and other transmissions might be taking place. The LAN91C113 is virtually queuing the packet numbers and their status words.

   In this case, the transmit interrupt service routine can find the next packet number to be serviced by reading the TX PACKET NUMBER at the FIFO PORTS register. This eliminates the need for the driver to keep a list of packet numbers being transmitted. The numbers are queued by the LAN91C113 and provided back to the CPU as their transmission completes.

2) One interrupt per sequence of packets: Enable TX EMPTY INT and TX INT, set AUTO RELEASE=1. TX EMPTY INT is generated only after transmitting the last packet in the FIFO.

TX INT will be set on a fatal transmit error allowing the CPU to know that the transmit process has stopped and therefore the FIFO will not be emptied.

This mode has the advantage of a smaller CPU overhead, and faster memory de-allocation. Note that when AUTO RELEASE=1 the CPU is not provided with the packet numbers that completed successfully.

Note: The pointer register is shared by any process accessing the LAN91C113 memory. In order to allow processes to be interruptible, the interrupting process is responsible for reading the pointer value before modifying it, saving it, and restoring it before returning from the interrupt.

Typically there would be three processes using the pointer:

1) Transmit loading (sometimes interrupt driven)
2) Receive unloading (interrupt driven)
3) Transmit Status reading (interrupt driven).

1) and 3) also share the usage of the Packet Number Register. Therefore saving and restoring the PNR is also required from interrupt service routines.

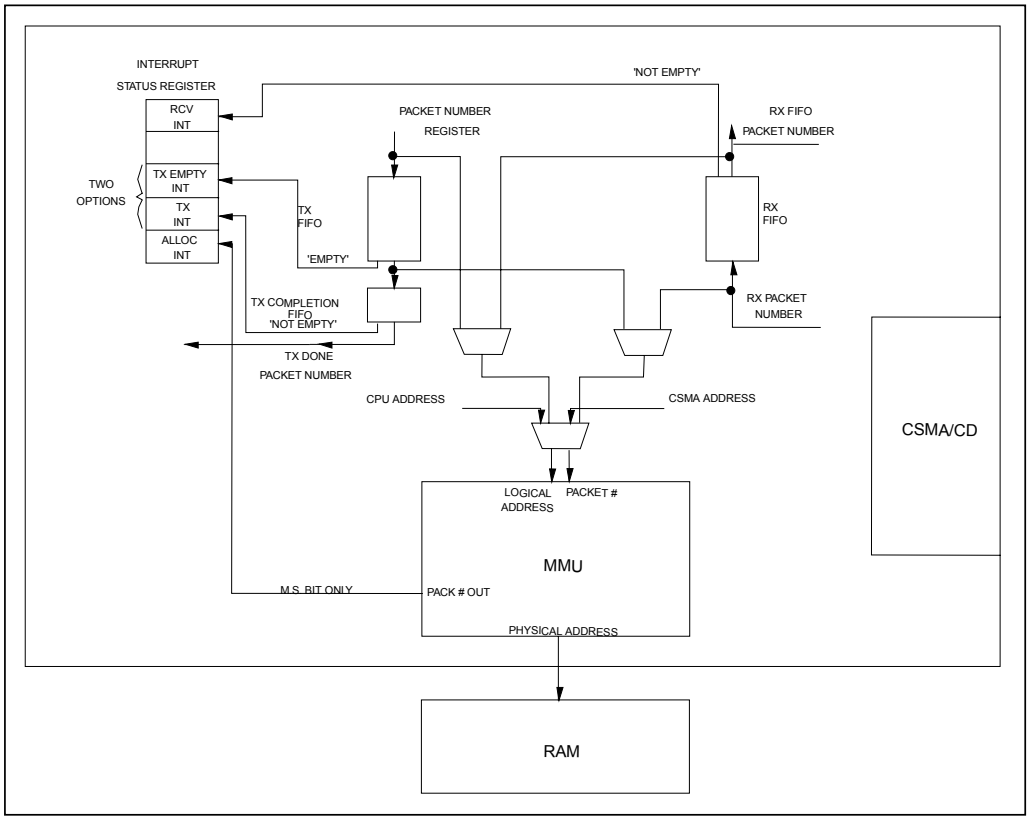


Figure 9.6 – Interrupt Generation for Transmit, Receive, MMU

Chapter 10 Board Setup Information

The following parameters are obtained from the EEPROM as board setup information:

- ETHERNET INDIVIDUAL ADDRESS
- I/O BASE ADDRESS
- MII INTERFACE

All the above mentioned values are read from the EEPROM upon hardware reset. Except for the INDIVIDUAL ADDRESS, the value of the IOS switches determines the offset within the EEPROM for these parameters, in such a way that many identical boards can be plugged into the same system by just changing the IOS jumpers.

In order to support a software utility based installation, even if the EEPROM was never programmed, the EEPROM can be written using the LAN91C113. One of the IOS combination is associated with a fixed default value for the key parameters (I/O BASE) that can always be used regardless of the EEPROM based value being programmed. This value will be used if all IOS pins are left open or pulled high.

The EEPROM is arranged as a 64 x 16 array. The specific target device is the 9346 1024-bit Serial EEPROM. All EEPROM accesses are done in words. All EEPROM addresses in the spec are specified as word addresses.

REGISTER	EEPROM WORD ADDRESS
Configuration Register	IOS Value * 4
Base Register	(IOS Value * 4) + 1

INDIVIDUAL ADDRESS 20-22 hex

If IOS2-IOS0 = 7, only the INDIVIDUAL ADDRESS is read from the EEPROM. Currently assigned values are assumed for the other registers. These values are default if the EEPROM read operation follows hardware reset.

The EEPROM SELECT bit is used to determine the type of EEPROM operation: a) normal or b) general purpose register.

a) NORMAL EEPROM OPERATION - EEPROM SELECT bit = 0

On EEPROM read operations (after reset or after setting RELOAD high) the CONFIGURATION REGISTER and BASE REGISTER are updated with the EEPROM values at locations defined by the IOS2-0 pins. The INDIVIDUAL ADDRESS registers are updated with the values stored in the INDIVIDUAL ADDRESS area of the EEPROM.

On EEPROM write operations (after setting the STORE bit) the values of the CONFIGURATION REGISTER and BASE REGISTER are written in the EEPROM locations defined by the IOS2-IOS0 pins.

The three least significant bits of the CONTROL REGISTER (EEPROM SELECT, RELOAD and STORE) are used to control the EEPROM. Their values are not stored nor loaded from the EEPROM.

b) GENERAL PURPOSE REGISTER - EEPROM SELECT bit = 1

On EEPROM read operations (after setting RELOAD high) the EEPROM word address defined by the POINTER REGISTER 6 least significant bits is read into the GENERAL PURPOSE REGISTER.

On EEPROM write operations (after setting the STORE bit) the value of the GENERAL PURPOSE REGISTER is written at the EEPROM word address defined by the POINTER REGISTER 6 least significant bits.

RELOAD and STORE are set by the user to initiate read and write operations respectively. Polling the value until read low is used to determine completion. When an EEPROM access is in progress the STORE and RELOAD bits of CTR will readback as both bits high. No other bits of the LAN91C113 can be read or written until the EEPROM operation completes and both bits are clear. This mechanism is also valid for reset initiated reloads.

Note: If no EEPROM is connected to the LAN91C113, for example for some embedded applications, the ENEEP pin should be grounded and no accesses to the EEPROM will be attempted. Configuration, Base, and Individual Address assume their default values upon hardware reset and the CPU is responsible for programming them for their final value.

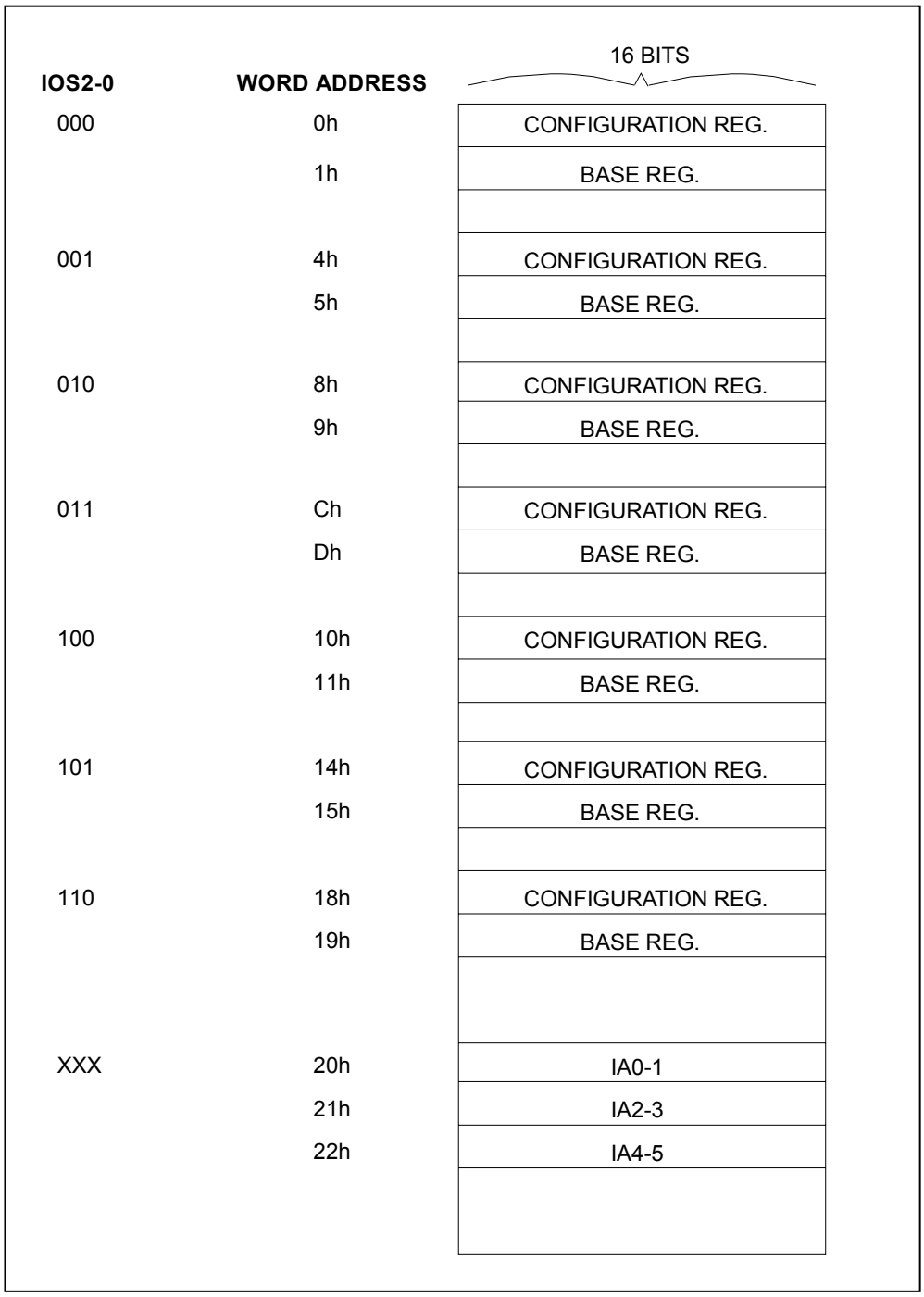


Figure 10.1 - 64 X 16 Serial EEPROM Map

Chapter 11 Application Considerations

The LAN91C113 is envisioned to fit a few different bus types. This section describes the basic guidelines, system level implications and sample configurations for the most relevant bus types. All applications are based on buffered architectures with a private SRAM bus.

FAST ETHERNET SLAVE ADAPTER

Slave non-intelligent board implementing 100 Mbps and 10 Mbps speeds.

Adapter requires:

a) LAN91C113 chip
b) Serial EEPROM (93C46)
c) Some bus specific glue logic

Target systems:

a) Local Bus 16 bit systems
b) High-end ISA
c) EISA 16 bit slave

Local Bus 16 Bit Systems

On VL Local Bus and other embedded systems, the LAN91C113 is accessed as a 16 bit peripheral in terms of the bus interface. All registers except the DATA REGISTER will be accessed using byte or word instructions. Accesses to the DATA REGISTER could use byte or word instructions.

Table 11.1 - Local Bus Signal Connections

VL BUS SIGNAL	LAN91C113 SIGNAL	NOTES
A2-A15	A2-A15	Address bus used for I/O space and register decoding, latched by nADS rising edge, and transparent on nADS low time.
M/nIO	AEN	Qualifies valid I/O decoding - enabled access when low. This signal is latched by nADS rising edge and transparent on nADS low time.
W/nR	W/nR	Direction of access. Sampled by the LAN91C113 on first rising clock that has nCYCLE active. High on writes, low on reads.
nRDYRTN	nRDYRTN	Ready return. Direct connection to VL bus.
nLRDY	nSRDY and some logic	nSRDY has the appropriate functionality and timing to create the VL nLRDY except that nLRDY behaves like an open drain output most of the time.
LCLK	LCLK	Local Bus Clock. Rising edges used for synchronous bus interface transactions.
nRESET	RESET	Connected via inverter to the LAN91C113.
nBE0 nBE1	nBE0 nBE1	Byte enables. Latched transparently by nADS rising edge.
nADS	nADS, nCYCLE	Address Strobe is connected directly to the VL bus. nCYCLE is created typically by using nADS delayed by one LCLK.
IRQn	INTR0	Typically uses the interrupt lines on the ISA edge connector of VL bus
D0-D15	D0-D15	16 bit data bus. The bus byte(s) used to access the device are a function of nBE0-nBE1

VL BUS SIGNAL	LAN91C113 SIGNAL	NOTES
nLDEV	nLDEV	nLDEV is a totem pole output. nLDEV is active on valid decodes of A15-A4 and AEN=0.
UNUSED PINS		
VCC	nRD nWR	
GND	A1 nVLBUS	

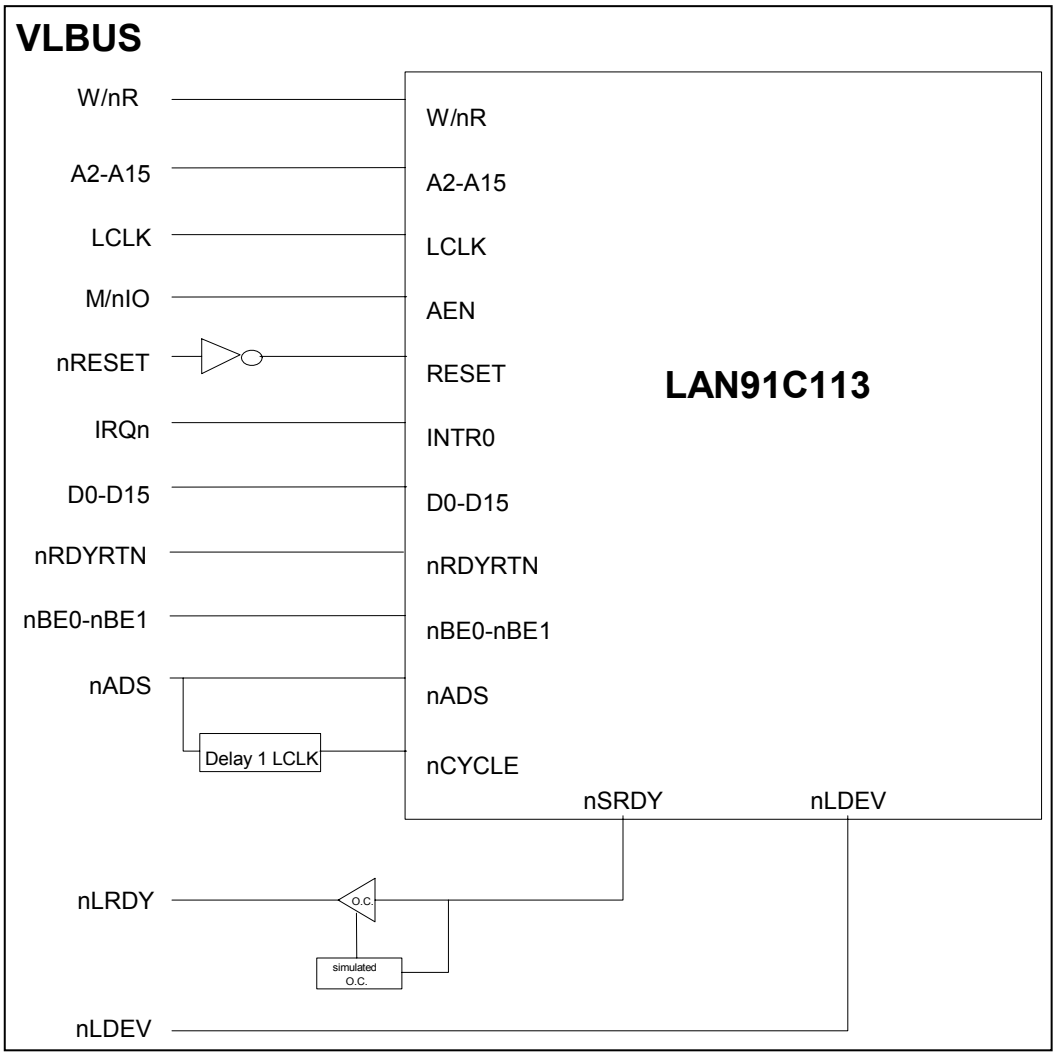


Figure 11.1 - LAN91C113 on VL Bus

HIGH-END ISA or EISA MACHINES

On ISA machines, the LAN91C113 is accessed as a 16 bit peripheral. The signal connections are listed in the following table:

Table 11.2 - High-End ISA or EISA Machines Signal Connectors

ISA BUS SIGNAL	LAN91C113 SIGNAL	NOTES
A1-A15	A1-A15	Address bus used for I/O space and register decoding.
AEN	AEN	Qualifies valid I/O decoding - enabled access when low.
nIORD	nRD	I/O Read strobe - asynchronous read accesses. Address is valid before leading edge.
nIOWR	nWR	I/O Write strobe - asynchronous write access. Address is valid before leading edge. Data is latched on trailing edge.
IOCHRDY	ARDY	This signal is negated on leading nRD, nWR if necessary. It is then asserted on CLK rising edge after the access condition is satisfied.
RESET	RESET	
A0	nBE0	
nSBHE	nBE1	
IRQn	INTR0	
D0-D15	D0-D15	16 bit data bus. The bus byte(s) used to access the device are a function of nBE0 and nBE1: nBE0 nBE1 D0-D7 D8-D15 0 0 Lower Upper 0 1 Lower Not used 1 0 Not used Upper Not used = tri-state on reads, ignored on writes
nIOCS16	nLDEV buffered	nLDEV is a totem pole output. Must be buffered using an open collector driver. nLDEV is active on valid decodes of A15-A4 and AEN=0.
UNUSED PINS		
GND	nADS	
VCC	nCYCLE, W/nR, nRDYRTN, LCLK	No upper word access.

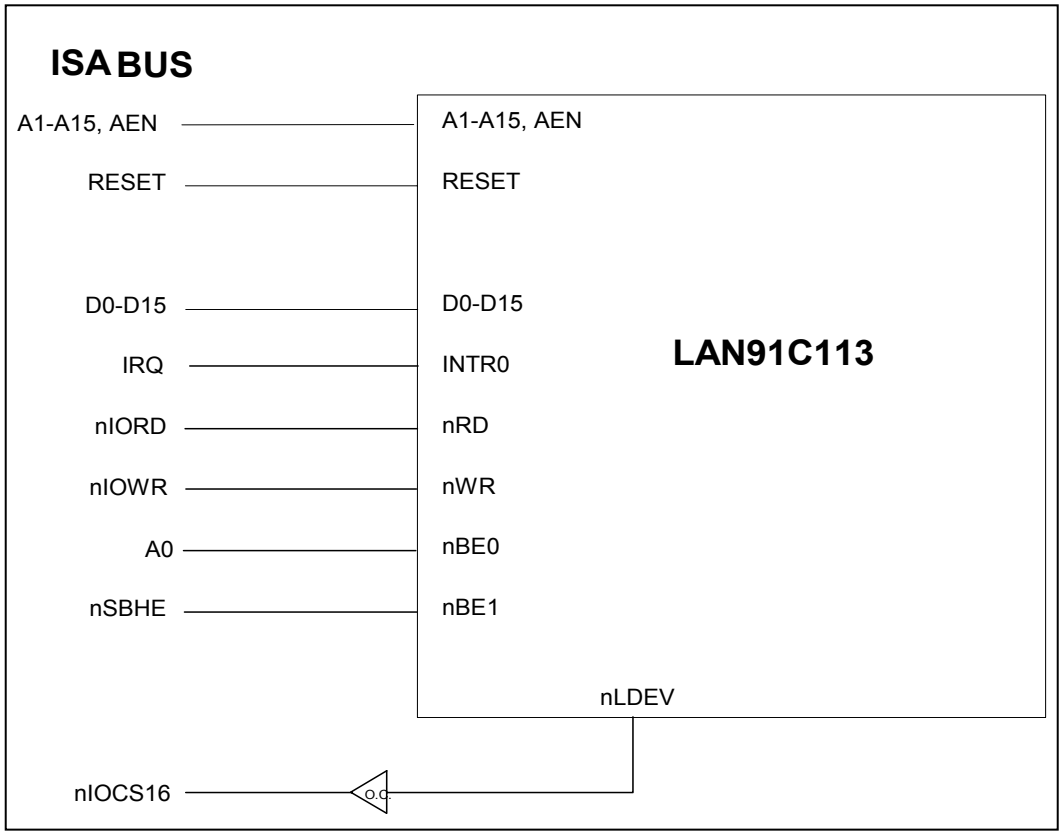


Figure 11.2 - LAN91C113 on ISA Bus

EISA 16 BIT SLAVE

On EISA the LAN91C113 is accessed as a 16 bit I/O slave. As an I/O slave, the LAN91C113 uses asynchronous accesses. In creating nRD and nWR inputs, the timing information is externally derived from nCMD edges. Given that the access will be at least 1.5 to 2 clocks (more than 180ns at least) there is no need to negate EXRDY, simplifying the EISA interface implementation.

Table 11.3 - EISA 16 Bit Slave Signal Connections

EISA BUS SIGNAL	LAN91C113 SIGNAL	NOTES
LA2-LA15	A2-A15	Address bus used for I/O space and register decoding, latched by nADS (nSTART) trailing edge.
M/nIO AEN	AEN	Qualifies valid I/O decoding - enabled access when low. These signals are externally ORed. Internally the AEN pin is latched by nADS rising edge and transparent while nADS is low.
Latched W-R combined with nCMD	nRD	I/O Read strobe - asynchronous read accesses. Address is valid before its leading edge.
Latched W-R combined with nCMD	nWR	I/O Write strobe - asynchronous write access. Address is valid before leading edge . Data latched on trailing edge.

EISA BUS SIGNAL	LAN91C113 SIGNAL	NOTES
nSTART	nADS	Address strobe is connected to EISA nSTART.
RESDRV	RESET	
nBE0 nBE1	nBE0 nBE1	Byte enables. Latched on nADS rising edge.
IRQn	INTR0	Interrupts used as active high edge triggered
D0-D15	D0-D15	16 bit data bus. The bus byte(s) used to access the device are a function of nBE0-nBE1.
nEX32 nNOWS (optional additional logic)	nLDEV	nLDEV is a totem pole output. nLDEV is active on valid decodes of LAN91C113 pins A15-A4, and AEN=0. nNOWS is similar to nLDEV except that it should go inactive on nSTART rising. nNOWS can be used to request compressed cycles (1.5 BCLK long, nRD/nWR will be 1/2 BCLK wide).
UNUSED PINS		
VCC	nVLBUS,	
GND	A1	

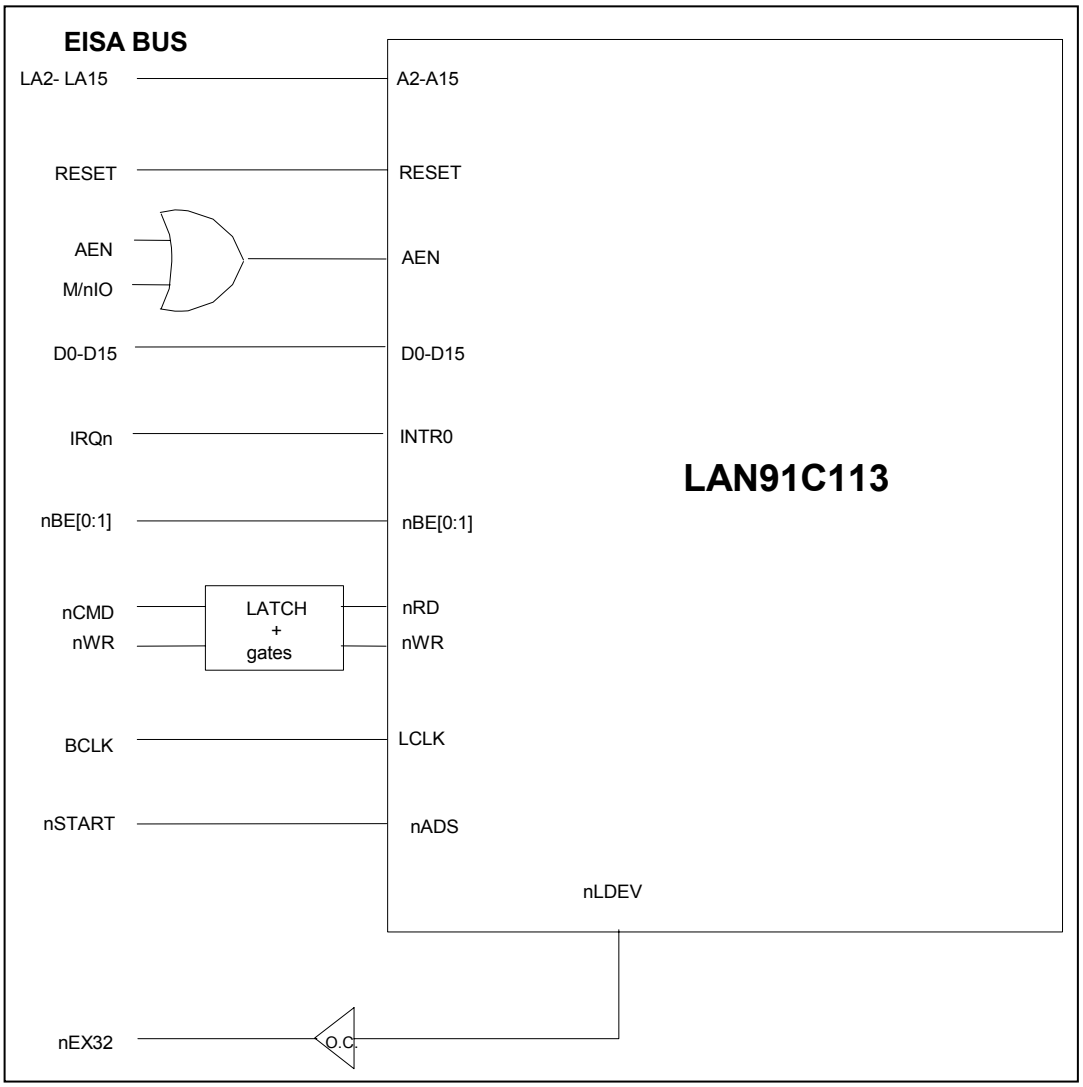


Figure 11.3 - LAN91C113 On EISA Bus

Chapter 12 Operational Description

12.1 Maximum Guaranteed Ratings*

Operating Temperature Range ..... 0°C to 85°C

Storage Temperature Range ..... -55C°to + 150°C

Lead Temperature Range (soldering, 10 seconds) ..... +325°C

Positive Voltage on any pin, with respect to Ground ..... V_{CC} + 0.3V

Negative Voltage on any pin, with respect to Ground ..... -0.3V

Maximum V_{CC} ..... +5V

*Stresses above those listed above could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

12.2 DC Electrical Characteristics

(V_{CC} = +3.3 V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
IS Type Input Buffer						
Low Input Level	V_{ILIS}			0.8	V	Schmitt Trigger
High Input Level	V_{IHIS}	2.2			V	Schmitt Trigger
Schmitt Trigger Hysteresis	V_{HYS}		250		mV	
I_{CLK} Input Buffer						
Low Input Level	V_{ILCK}			0.8	V	
High Input Level	V_{IHCK}	2.2			V	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
Input Leakage (All I and IS buffers except pins with pullups/pulldowns)						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	µA	V_{IN} = V_{CC}
IP Type Buffers						
Input Current	I_{IL}	-110	-45		µA	V_{IN} = 0
ID Type Buffers						
Input Current	I_{IH}		+45	+110	µA	V_{IN} = V_{CC}
O4 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 6 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -4 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
I/O4 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 6 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -4 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 20 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -10 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
O16 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 35 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -15 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
O24 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 35 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -15 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
I/O24 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 35 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -15 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
I/OD Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 4 mA
High Output Level	V_{OH}	2.4			V	na
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
Supply Current Active	I_{CC}		100	140	mA	Dynamic Current (Assuming internal PHY is used)
Powerdown Supply Current	I_{PDN}		15	38	mA	Internal PHY in Powerdown mode
			14	36	mA	Internal MAC+PHY in Powerdown mode

CAPACITANCE T_A = 25°C; fc = 1MHz; V_{CC} = 3.3V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{IN}			20	pF	All pins except pin under test tied to AC ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

CAPACITIVE LOAD ON OUTPUTS

ARDY, D0-D15 (non VLBUS)	45 pF
D0-D15 in VLBUS	45 pF
All other outputs	45 pF

12.3 Twisted Pair Characteristics, Transmit

1) V_{DD} = 3.3v +/- 5%

2) RBIAS = 11K +/- 1 %, no load

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
T_{ov}	TP Differential Output Voltage	0.950	1.000	1.050	Vpk	100 Mbps, UTP Mode, 100 Ohm Load
		1.165	1.225	1.285	Vpk	100 Mbps, STP Mode, 150 Ohm Load
		2.2	2.5	2.8	Vpk	10 Mbps, UTP Mode, 100 Ohm Load
		2.694	3.062	3.429	Vpk	10 Mbps, STP Mode, 150 Ohm Load
T_{ovs}	TP Differential Output Voltage Symmetry	98		102	%	100 Mbps, Ratio of Positive And Negative Amplitude Peaks on TPO±
T_{ORF}	TP Differential Output Rise And Fall Time	3.0		5.0	nS	100 Mbps TRFADJ [1:0] = 10
T_{ORFS}	TP Differential Output Rise And Fall Time Symmetry			+/-0.5	nS	100 Mbps, Difference Between Rise and Fall Times on TPO±
T_{oDC}	TP Differential Output Duty Cycle Distortion			+/- 0.25	nS	100 Mbps, Output Data=0101... NRZ Pattern Unscrambled, Measure At 50% Points
T_{oJ}	TP Differential Output Jitter			+/-1.4	nS	100 Mbps, Output Data=scrambled /H/
T_{oo}	TP Differential Output Overshoot			5.0	%	100 Mbps
T_{OVT}	TP Differential Output Voltage Template	**(See Figure 6.4)**				10 Mbps
T_{SOI}	TP Differential Output SOI Voltage Template	**(See Figure 6.6)**				10 Mbps
T_{LPT}	TP Differential Output Link Pulse Voltage Template	**(See Figure 6.7)**				10 Mbps, NLP and FLP
T_{OIV}	TP Differential Output Idle Voltage			+/-50	mV	10 Mbps.
T_{OIA}	TP Output Current	38	40	42	mA pk	100 Mbps, UTP with TLVL[3:0]=1000
		31.06	32.66	34.26	mA pk	100 Mbps, STP with TLVL[3:0]=1000
		88	100	112	mA pk	10 Mbps, UTP with TLVL[3:0]=1000
		71.86	81.64	91.44	mA pk	10 Mbps, STP with TLVL[3:0]=1000
T_{OIR}	TP Output Current Adjustment Range	0.80		1.2		V_{DD} = 3.3V, Adjustable with RBIAS, relative to T_{OIA} with RBIAS=11K

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
		0.86		1.16		V_{DD} = 3.3V, Adjustable with TLVL[3:0] Relative to Value at TLVL[3:0]=1000
T_{ORA}	TP Output Current TLVL Step Accuracy			+/-50	%	Relative to Ideal Values in Table 3. Table 3 Values Relative to Output with TLVL[3:0]=1000.
T_{OR}	TP Output Resistance		10K		Ohm	
T_{OC}	TP Output Capacitance		15		pF	

12.4 Twisted Pair Characteristics, Receive

Unless otherwise noted, all test conditions are as follows:

1) Vcc = 3.3V +/-5%
2) RBIAS = 11K +/- 1 %, no load
3) 62.5/10 Mhz Square Wave on TP inputs in 100/10 Mbps

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
RST	TP Input Squelch Threshold	166		500	mV pk	100 Mbps, RLVL=0
		310		540	mV pk	10 Mbps, RLVL=0
		60		200	mV pk	100 Mbps, RLVL=1
		186		324	mV pk	10 Mbps, RLVL=1
RUT	TP Input Unsquelch Threshold	100		300	mV pk	100 Mbps, RLVL=0
		186		324	mV pk	10 Mbps, RLVL=0
		20		90	mV pk	100 Mbps, RLVL=1
		112		194	mV pk	10 Mbps, RLVL=1
	TP Input Open Circuit Voltage		VDD-2.4 ± 0.2		Volt	Voltage on Either TPI+ or TPI- with Respect to GND.
RCMR	TP Input Common Mode Voltage Range		ROCV ± 0.25		Volt	Voltage on TPI± with Respect to GND.
RDR	TP Input Differential Voltage Range			VDD	Volt	
RIR	TP Input Resistance	5K			Ohm	
RIC	TP Input Capacitance		10		pF	

Chapter 13 Timing Diagrams

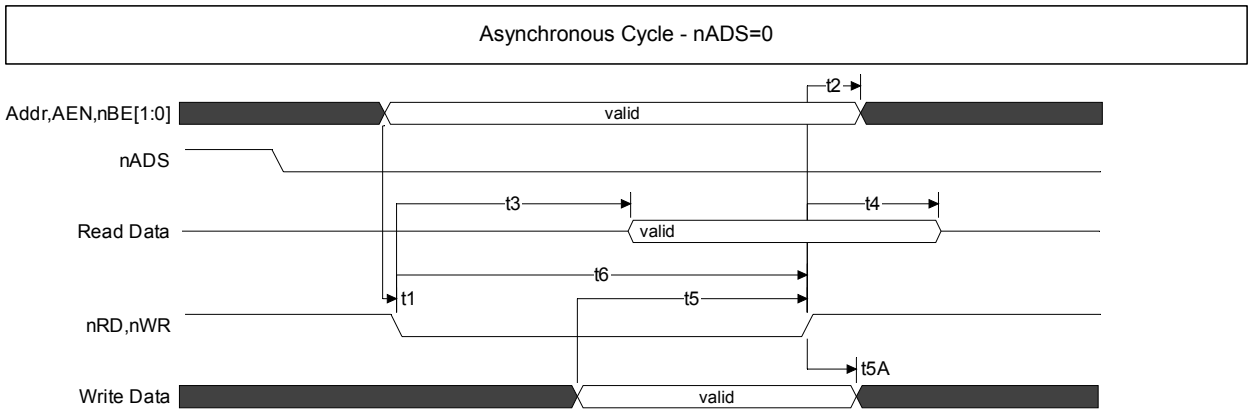


Figure 13.1 – Asynchronous Cycle - nADS=0

	PARAMETER	MIN	TYP	MAX	UNITS
t1	A1-A15, AEN, nBE[1:0] Valid to nRD, nWR Active	2			ns
t2	A1-A15, AEN, nBE[1:0] Hold After nRD, nWR Inactive (Assuming nADS Tied Low)	5			ns
t3	nRD Low to Valid Data			15	ns
t4	nRD High to Data Invalid	15			ns
t5	Data Setup to nWR Inactive	10			ns
t5A	Data Hold After nWR Inactive	5			ns
t6	nRD Strobe Width	15			ns

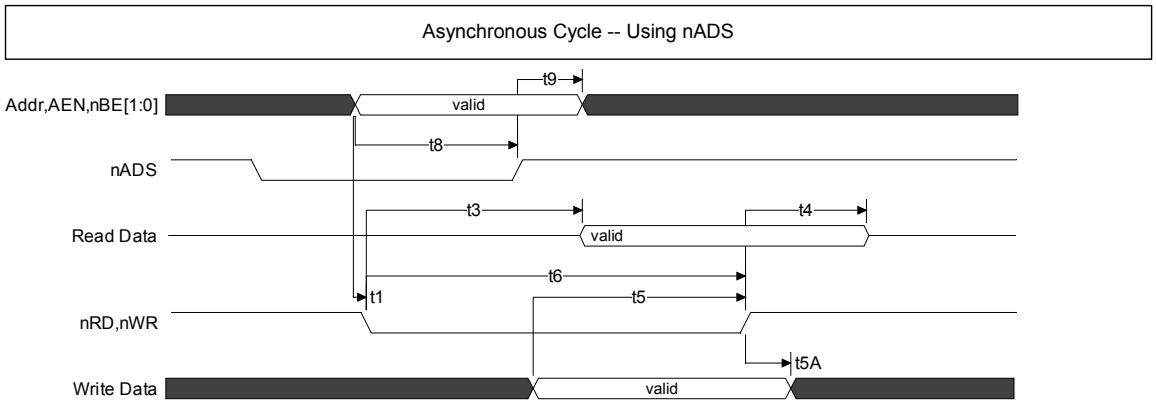


Figure 13.2 - Asynchronous Cycle - Using nADS

	PARAMETER	MIN	TYP	MAX	UNITS
t1	A1-A15, AEN, nBE[1:0] Valid to nRD, nWR Active	2			ns
t3	nRD Low to Valid Data			15	ns
t4	nRD High to Data Invalid	15			ns
t5	Data Setup to nWR Inactive	10			ns
t5A	Data Hold After nWR Inactive	5			ns
t6	nRD Strobe Width	15			ns
t8	A1-A15, AEN, nBE[1:0] Setup to nADS Rising	8			ns
t9	A1-A15, AEN, nBE[1:0] Hold after nADS Rising	5			ns

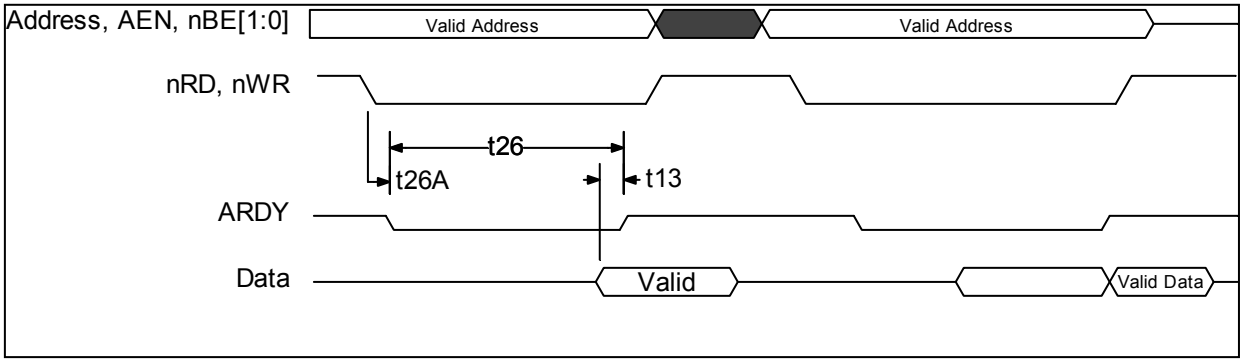


Figure 13.3 – Asynchronous Ready

	PARAMETER	MIN	TYP	MAX	UNITS
t26	ARDY Low Pulse Width	100		150	ns
t26A	Control Active to ARDY Low			10	ns
t13	Valid Data to ARDY High	10			ns

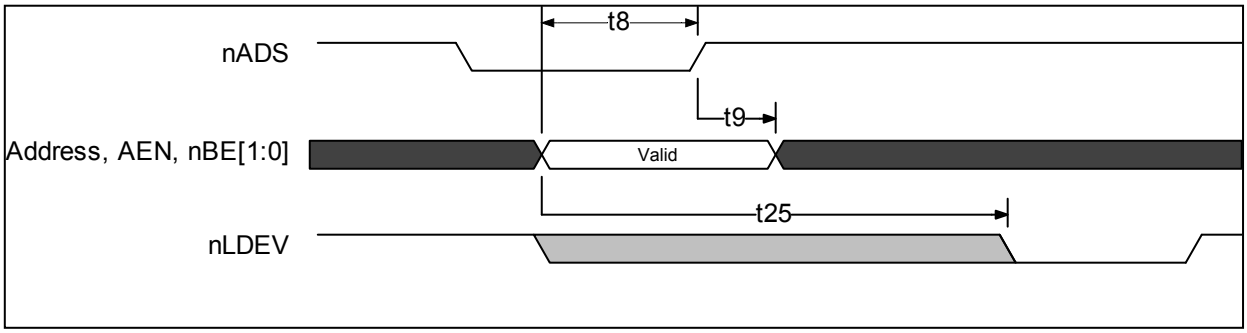


Figure 13.4 – Address Latching for all Modes

	PARAMETER	MIN	TYP	MAX	UNITS
t8	A1-A15, AEN, nBE[1:0] Setup to nADS Rising	8			ns
t9	A1-A15, AEN, nBE[1:0] Hold After nADS Rising	5			ns
t25	A4-A15, AEN to nLDEV Delay			30	ns

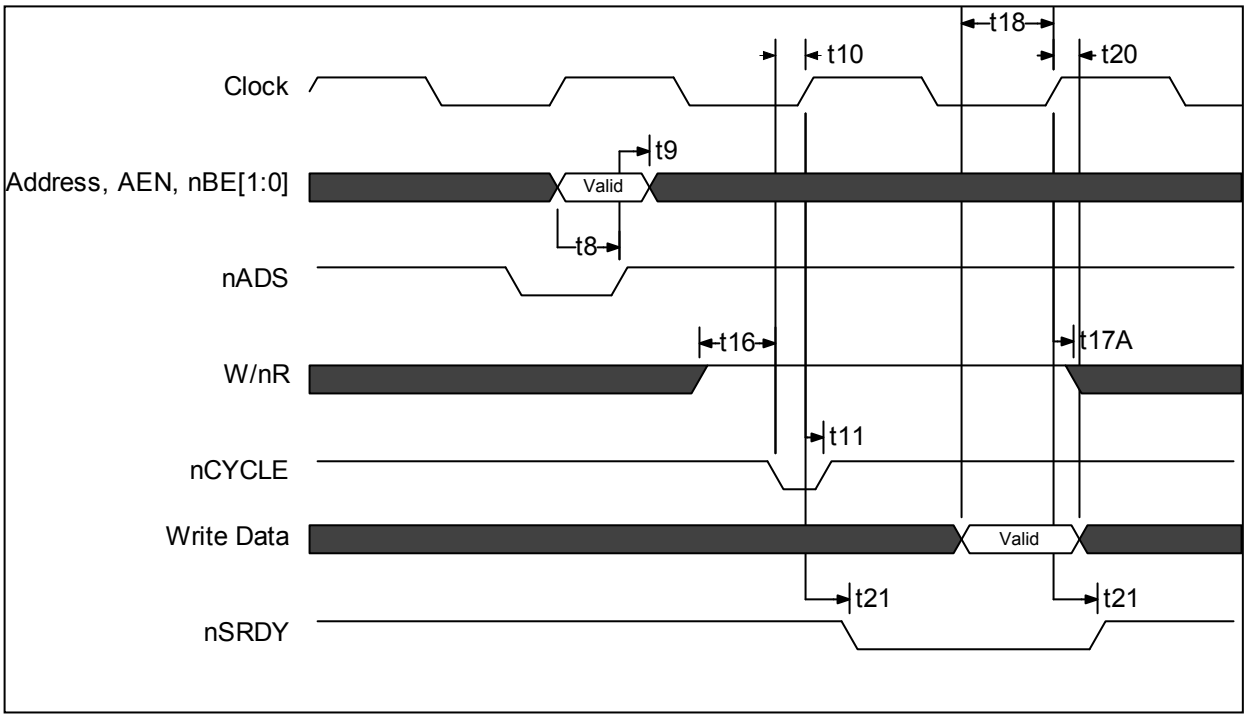


Figure 13.5 – Synchronous Write Cycle - nVLBUS=0

	PARAMETER	MIN	TYP	MAX	UNITS
t8	A1-A15, AEN, nBE[1:0] Setup to nADS Rising	8			ns
t9	A1-A15, AEN, nBE[1:0] Hold After nADS Rising	5			ns
t10	nCYCLE Setup to LCLK Rising	5			ns
t11	nCYCLE Hold after LCLK Rising	3			ns
t16	W/nR Setup to nCYCLE Active	0			ns
t17A	W/nR Hold after LCLK Rising with nSRDY Active	3			ns
t18	Data Setup to LCLK Rising (Write)	15			ns
t20	Data Hold from LCLK Rising (Write)	4			ns
t21	nSRDY Delay from LCLK Rising			7	ns

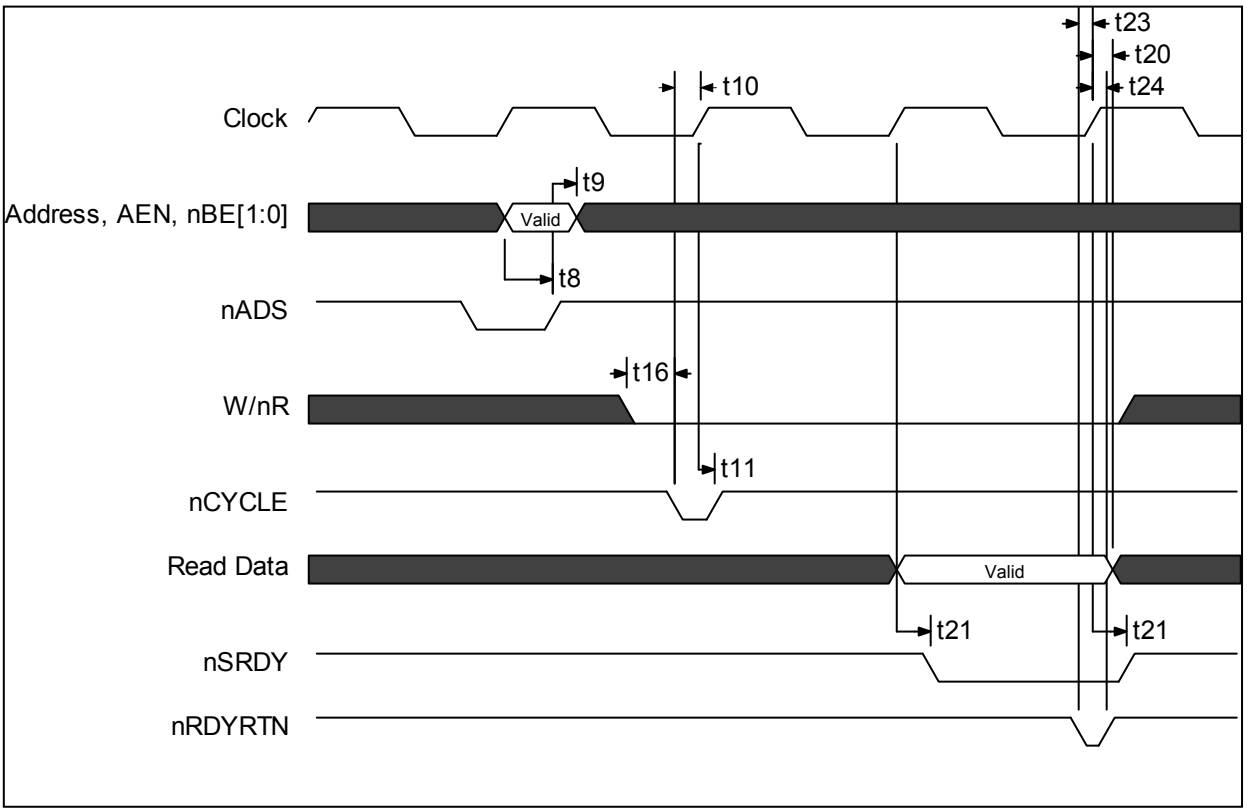


Figure 13.6 – Synchronous Read Cycle - nVLBUS=0

	PARAMETER	MIN	TYP	MAX	UNITS
t8	A1-A15, AEN, nBE[1:0] Setup to nADS Rising	8			ns
t9	A1-A15, AEN, nBE[1:0] Hold After nADS Rising	5			ns
t10	nCYCLE Setup to LCLK Rising	5			ns
t11	nCYCLE Hold after LCLK Rising	3			ns
t16	W/nR Setup to nCYCLE Active	0			ns
t20	Data Hold from LCLK Rising (Read)	4			ns
t21	nSRDY Delay from LCLK Rising			7	ns
t23	nRDYRTN Setup to LCLK Rising	3			ns
t24	nRDYRTN Hold after LCLK Rising	3			ns

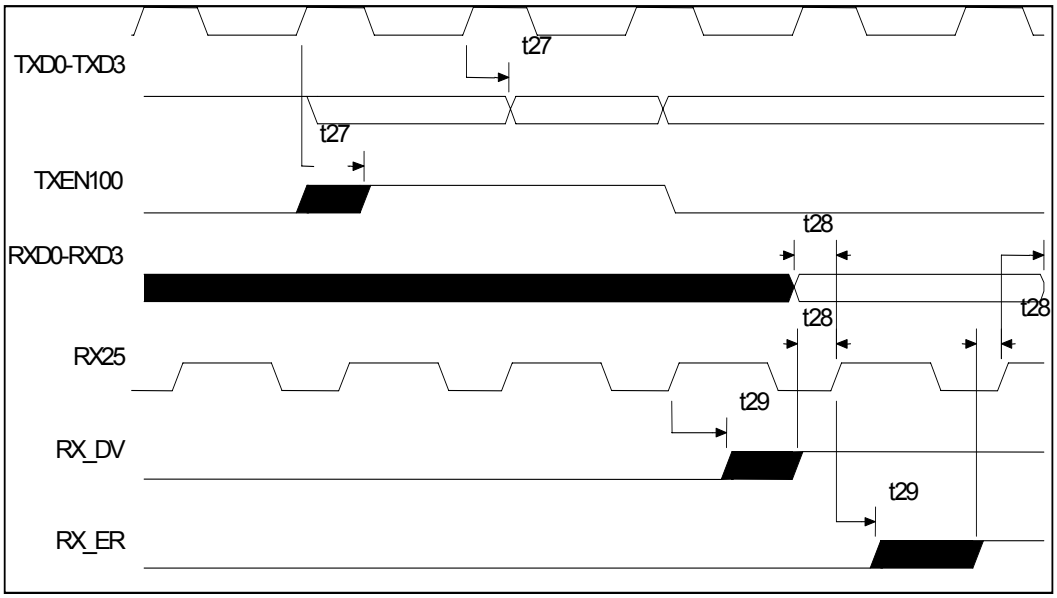


Figure 13.7 - MII Timing

	PARAMETER	MIN	TYP	MAX	UNITS
t27	TXD0-TXD3, TXEN100 Delay from TX25 Rising	0		15	ns
t28	RXD0-RXD3, RX_DV, RX_ER Setup to RX25 Rising	10			ns
t29	RXD0-RXD3, RX_DV, RX_ER Hold After RX25 Rising	10			ns

AC TEST TIMING CONDITIONS

Unless otherwise noted, all test conditions are as follows:

1) V_{DD} = 3.3V +/-5%
2) RBIAS = 11K +/- 1%, no load
3) Measurement Points:
4) TPO±, TPI±: 0.0 V During Data, ±0.3V at start/end of packet
5) All other inputs and outputs: 1.4 Volts

Table 13.1 – Transmit Timing - Characteristics

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t30	Transmit Propagation Delay	60		140	nS	100Mbps
				600	nS	10Mbps
t31	Transmit Output Jitter			±0.7	nS pk-pk	100Mbps
				±5.5	nS pk-pk	10Mbps
t32	Transmit SOI Pulse Width to 0.3V	250			nS	10Mbps
t33	Transmit SOI Pulse Width to 40mV			4500	nS	10Mbps
t34	LEDn Delay Time			25	mS	
t35	LEDn Pulse Width	80		105	mS	

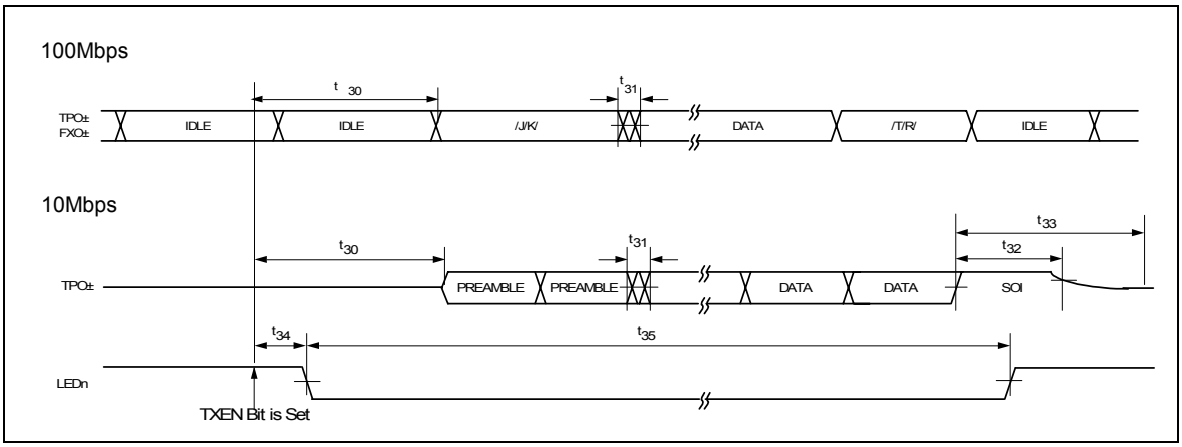


Figure 13.8 – Transit Timing

Table 13.2 - Receive Timing Characteristics

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t36	Receive Input Jitter			±3.0	nS pk-pk	100Mbps
				±13.5	nS pk-pk	10Mbps
t37	SOI Pulse Minimum Width Required for Idle Detection	125		200	nS	10Mbps Measure TPI± from last zero cross to 0.3V point

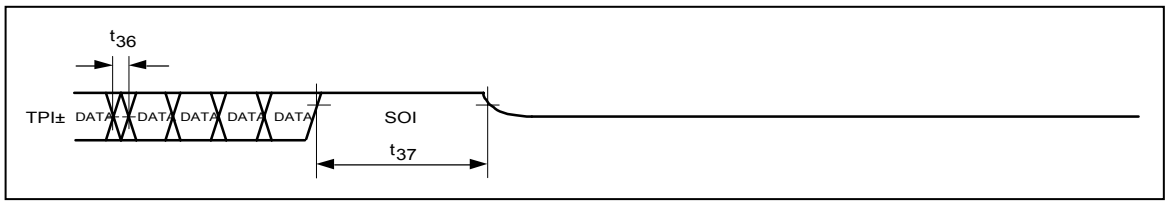


Figure 13.9 – Receive Timing, End of Packet - 10 MBPS

Table 13.3 – Collision and Jam Timing Characteristics

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t38	Rcv Packet Start to COL Assert Time			200	nS	100Mbps
				700	nS	10Mbps
				300	nS	10Mbps
t39	Xmt Packet Start to COL Assert Time			200	nS	100Mbps
				700	nS	10Mbps
t40	Start of Packet to Transmit JAM Packet Start During JAM			500	nS	100Mbps
				1500	nS	10Mbps
t41	Xmt Packet Start to COL Assert Time			200	nS	100Mbps
				700	nS	10Mbps

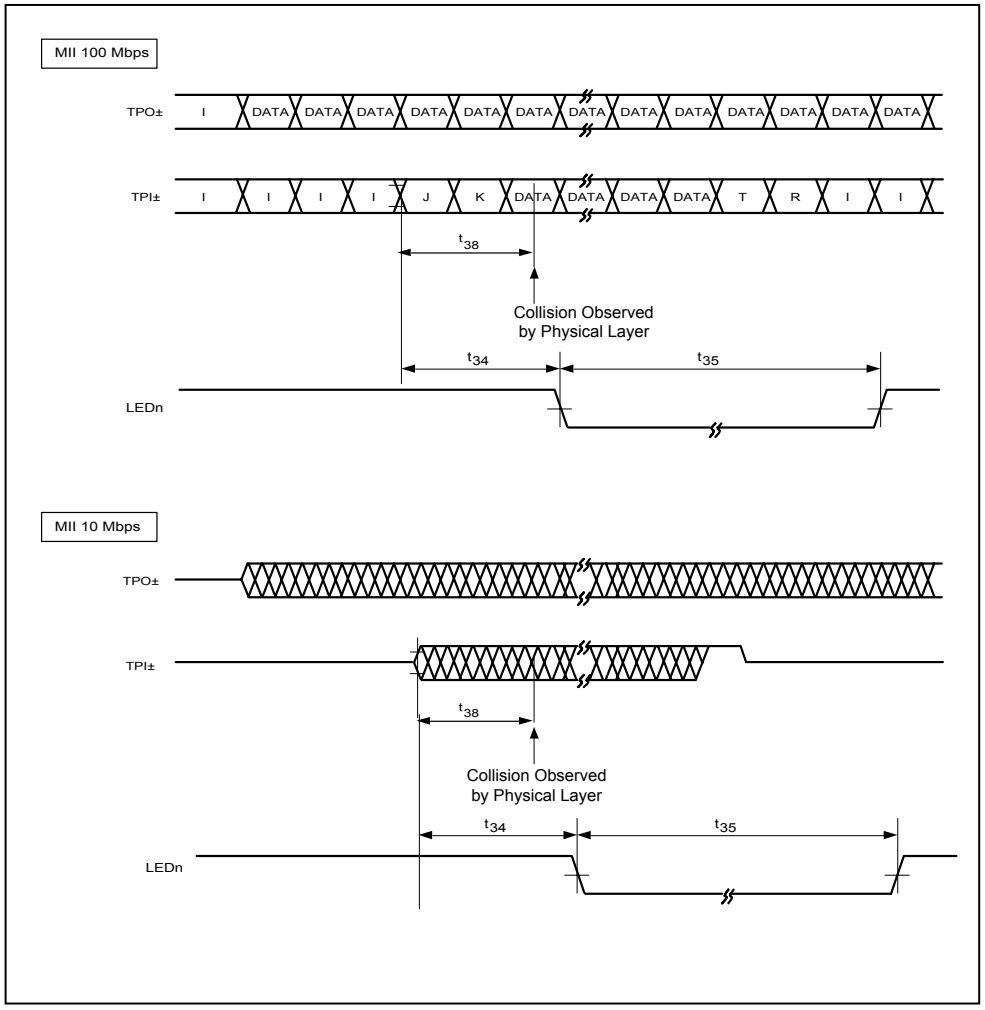


Figure 13.10 – Collision Timing, Receive

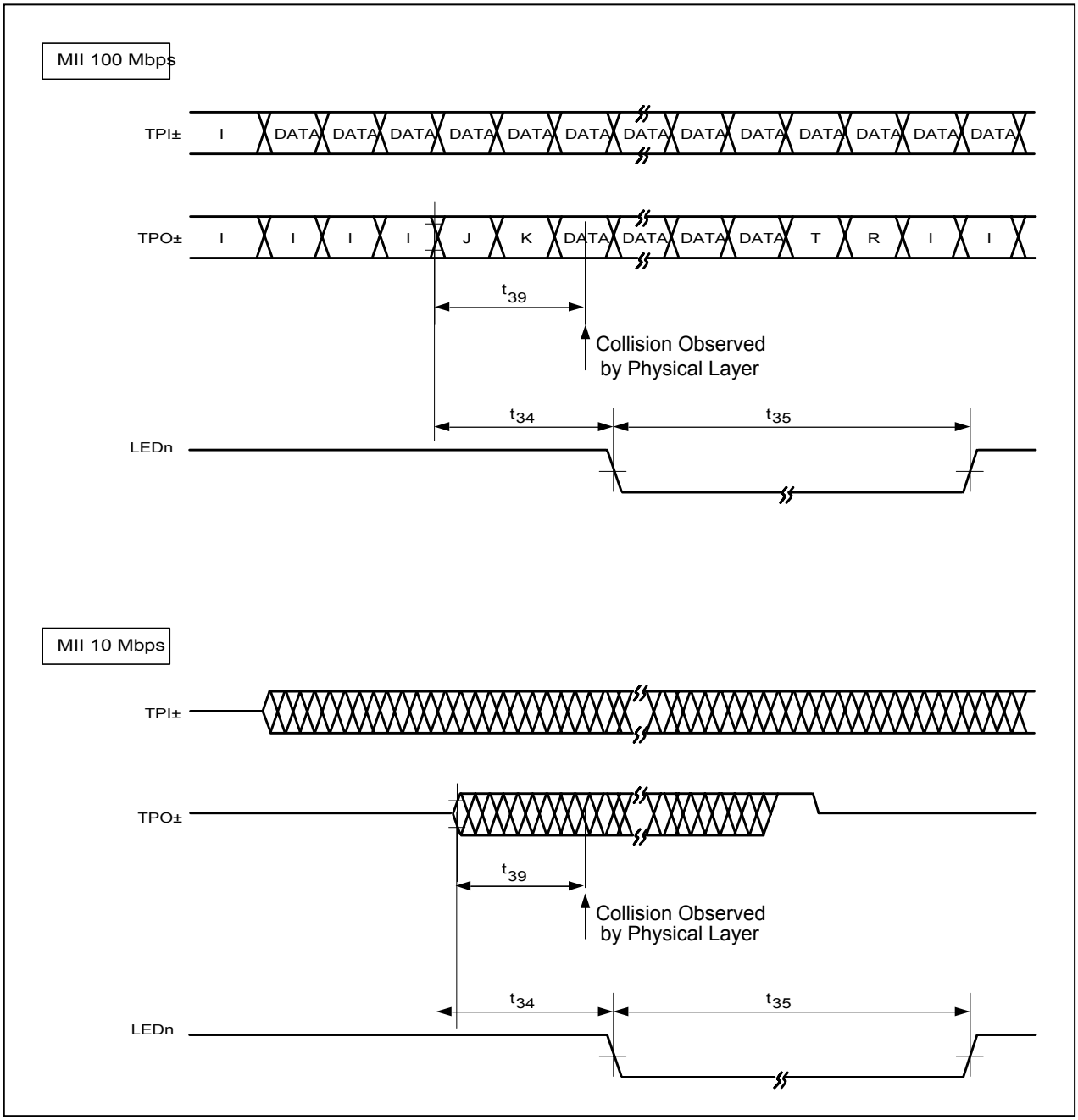


Figure 13.11 – Collision Timing, Transmit

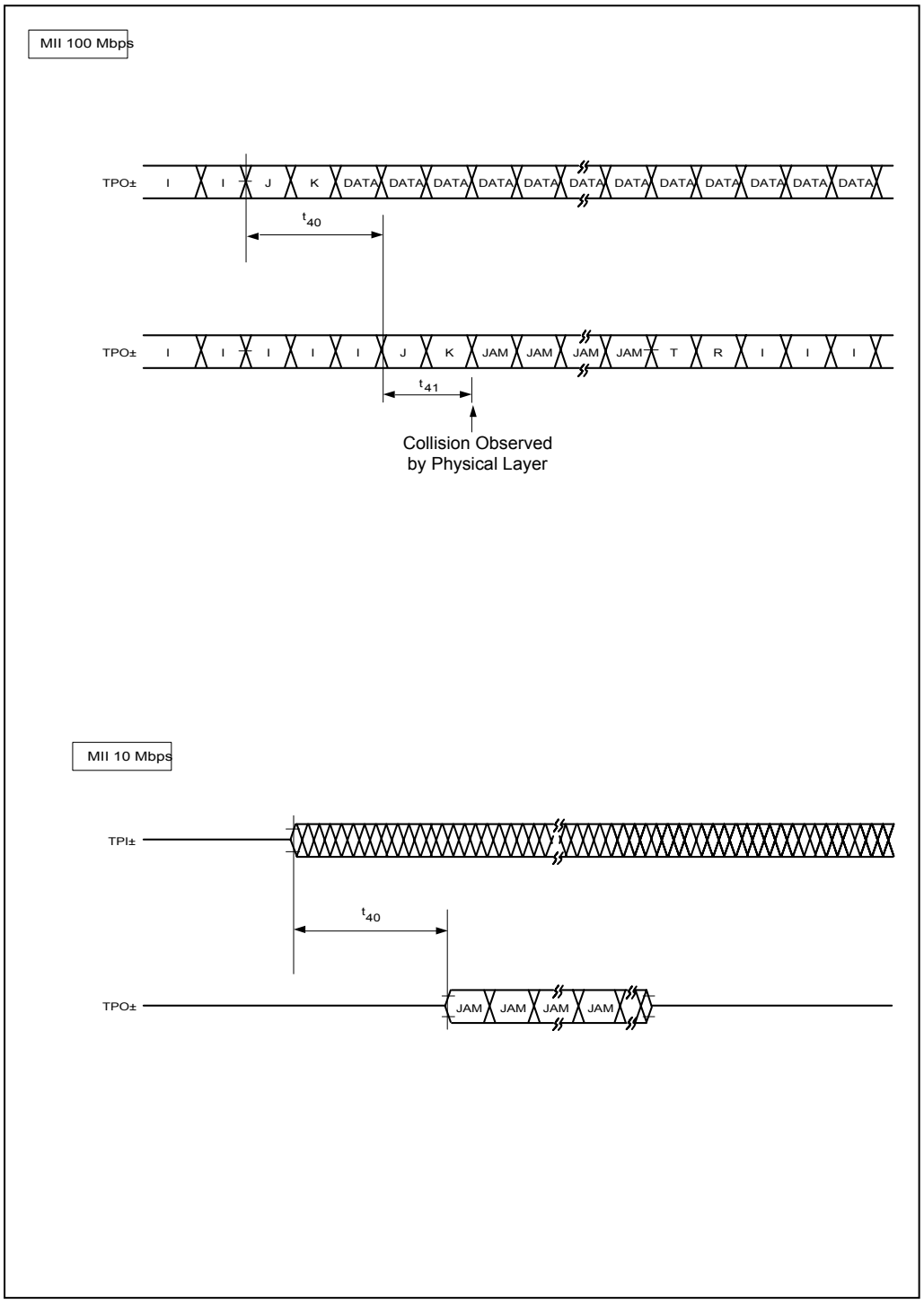


Figure 13.12 – Jam Timing

Table 13.4 – Link Pulse Timing Characteristics

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t42	NLP Transmit Link Pulse Width	(See Figure 6.8)			nS	
t43	NLP Transmit Link Pulse Period	8		24	mS	
t44	NLP Receive Link Pulse Width Required For Detection	50			nS	
t45	NLP Receive Link Pulse Minimum Period Required For Detection	6		7	mS	link_test_min
t46	NLP Receive Link Pulse Maximum Period Required For Detection	50		150	mS	link_test_max
t47	NLP Receive Link Pulse Required To Exit Link Fail State	3	3	3	Link Pulses	lc_max
t48	FLP Transmit Link Pulse Width	100		150	nS	
t49	FLP Transmit Clock Pulse to Data Pulse Period	55.5	62.5	69.5	µS	interval_timer
t50	FLP Transmit Clock Pulse to Clock Pulse Period	111	125	139	µS	
t51	FLP Transmit Link Pulse Burst Period	8		22	mS	transmit_link_burst_timer
t52	FLP Receive Link Pulse Width Required For Detection	50			nS	
t53	FLP Receive Link Pulse Minimum Period Required For Clock Pulse Detection	5		25	µS	flp_test_min_timer
t54	FLP Receive Link Pulse Maximum Period Required For Clock Pulse Detection	165		185	µS	flp_test_max_timer
t55	FLP Receive Link Pulse Minimum Period Required For Data Pulse Detection	15		47	µS	data_detect_min_timer
t56	FLP Receive Link Pulse Maximum Period Required For Data Pulse Detection	78		100	µS	data_detect_max_timer
t57	FLP Receive Link Pulse Burst Minimum Period Required For Detection	5		7	mS	nlp_test_min_timer
t58	FLP Receive Link Pulse Burst Maximum Period Required For Detection	50		150	mS	nlp_test_max_timer
t59	FLP Receive Link Pulses Bursts Required To Detect AutoNegotiation Capability	3	3	3	Link Pulses	

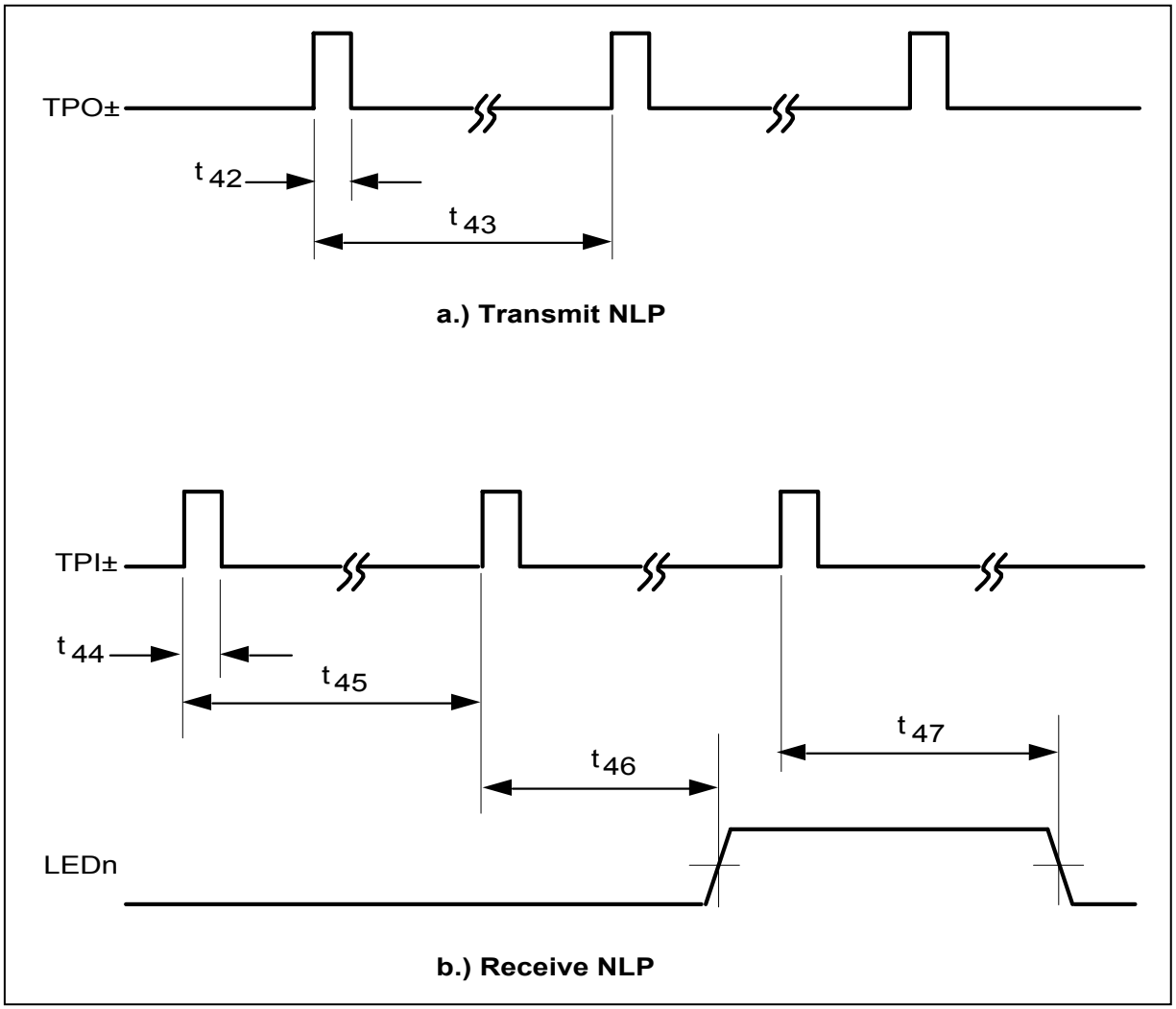


Figure 13.13 – Link Pulse Timing

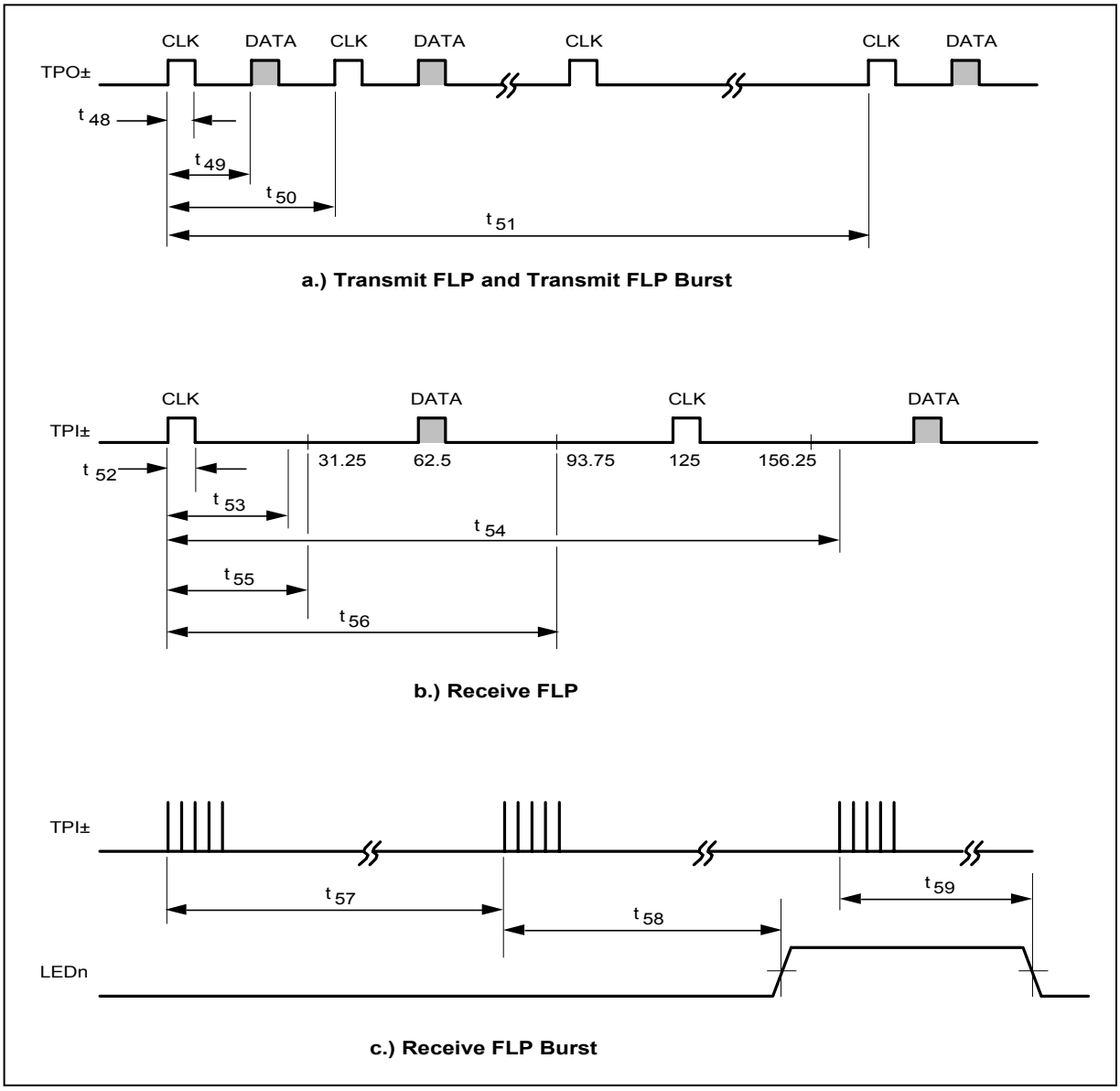


Figure 13.14 - FLP Link Pulse Timing

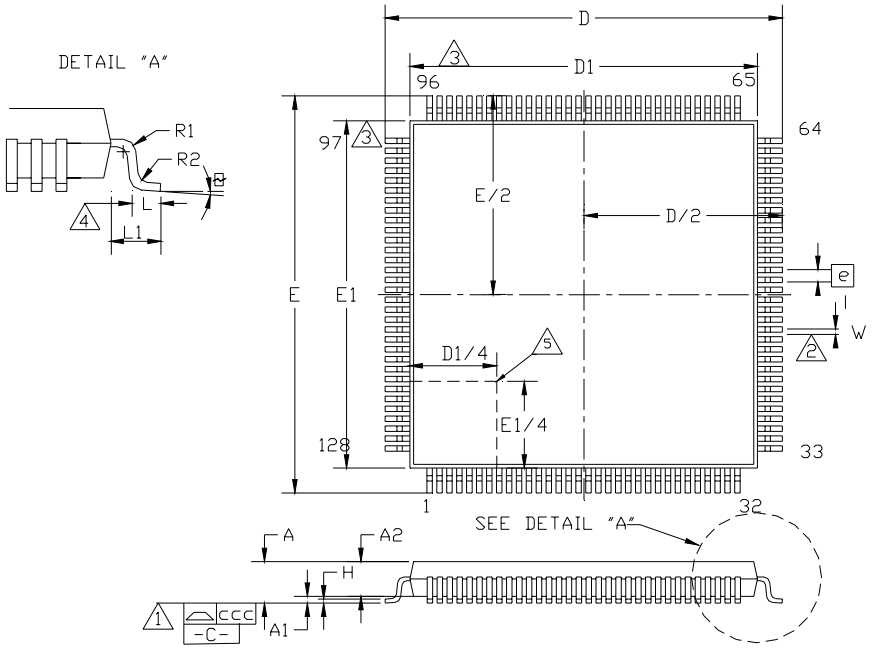


Figure 13.15 - 128 Pin TQFP Package Outline, 14X14X1.0 Body

Table 13.5 - 128 Pin TQFP Package Parameters

	MIN	NOMINAL	MAX	REMARK
A	~	~	1.20	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	0.95	1.00	1.05	Body Thickness
D	15.80	16.00	16.20	X Span
D/2	7.90	8.00	8.10	$^1/_2$ X Span Measure from Centerline
D1	13.80	14.00	14.20	X body Size
E	15.80	16.00	16.20	Y Span
E/2	7.90	8.00	8.10	$^1/_2$ Y Span Measure from Centerline
E1	13.80	14.00	14.20	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length from Centerline
L1	~	1.00	~	Lead Length
e		0.40 Basic		Lead Pitch
θ	0^o	~	7^o	Lead Foot Angle
W	0.13	0.18	0.23	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.0762	Coplanarity *(Assemblers)*
ccc	~	~	0.08	Coplanarity *(Test House)*

Notes:
1. Controlling Unit: millimeter
2. Tolerance on the position of the leads is ± 0.035 mm maximum.
3. Package body dimensions D1 and E1 do not include the mold protrusion.
4. Maximum mold protrusion is 0.25 mm.
5. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane is 0.78-1.08 mm.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. Shoulder widths must conform to JEDEC MS-026 dimension 'S' of a minimum of 0.20mm.

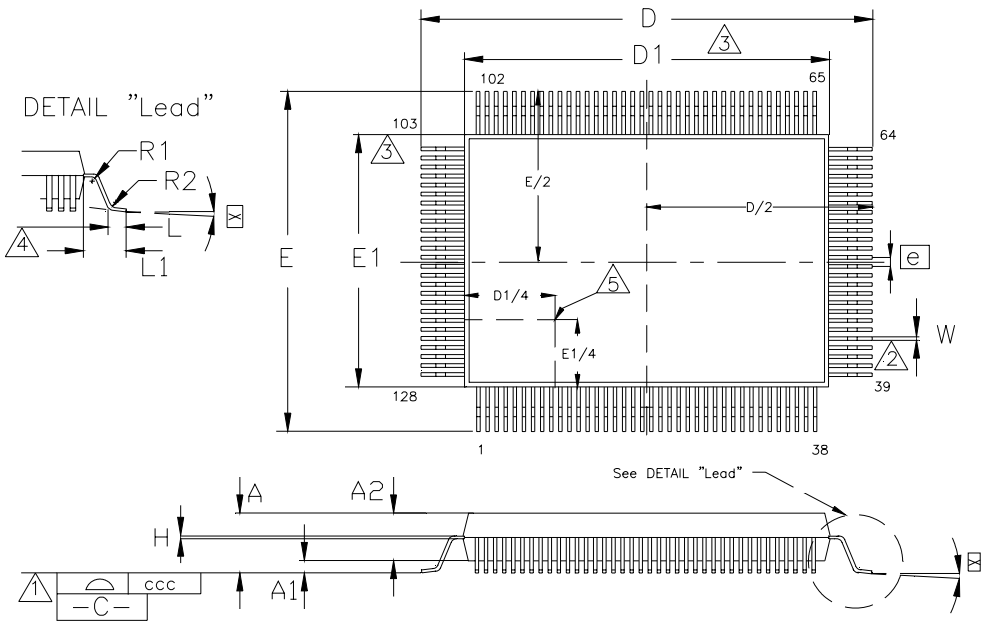


Figure 13.16 - 128 Pin QFP Package Outline, 3.9 MM Footprint

Table 13.6 - 128 Pin QFP Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	~	~	3.4	Overall Package Height
A1	0.05	~	0.5	Standoff
A2	2.55	~	3.05	Body Thickness
D	23.70	23.90	24.10	X Span
D/2	11.85	11.95	12.05	$^1/_2$ X Span Measured from Centerline
D1	19.90	20.0	20.10	X body Size
E	17.70	17.90	18.10	Y Span
E/2	8.85	8.95	9.05	$^1/_2$ Y Span Measured from Centerline
E1	13.90	14.00	14.10	Y body Size
H	~	~	~	Lead Frame Thickness
L	0.73	0.88	1.03	Lead Foot Length
L1	~	1.95	~	Lead Length
e	0.5 Basic			Lead Pitch
θ	0^o	~	7^o	Lead Foot Angle
W	0.10	~	0.30	Lead Width
R1	0.13	~	~	Lead Shoulder Radius
R2	0.13	~	0.30	Lead Foot Radius
ccc	~	~	0.0762	Coplanarity *(Assemblers)*
ccc	~	~	0.08	Coplanarity *(Test House)*

Notes:
1. Controlling Unit: millimeter.
2. Tolerance on the position of the leads is ± 0.04 mm maximum.
3. Package body dimensions D1 and E1 do not include the mold protrusion.
4. Maximum mold protrusion is 0.25 mm.
5. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.

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