

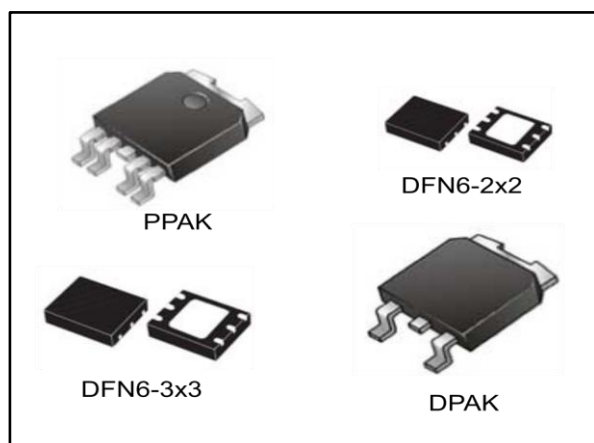


# THE DATASHEET OF LDFM50PT-TR



## 500 mA very low drop voltage regulator

Datasheet - production data



### Applications

- PCs and laptop computers
- Battery-powered equipment
- Industrial and medical equipment
- Portable equipment

### Description

The LDFM is a fast, very low drop linear regulator which operates from an input supply voltage in the range of 2.5 V to 16 V.

It is available in fixed and adjustable output voltage versions, from 0.8 V to 12 V.

The LDFM features high output precision, very low dropout voltage, low noise, and low quiescent current, therefore suitable for low voltage microprocessors and memory applications.

Enable logic control pin and Power Good output are featured on PPAK/DFN packages.

Current and thermal protection are provided.

### Features

- Input voltage from 2.5 to 16 V
- Very low dropout voltage (300 mV max. at 500 mA load)
- Low quiescent current (200  $\mu$ A typ. @ 500 mA load)
- Available in 1 % precision in PPAK and DFN6 packages, 2 % in DPAK
- 500 mA guaranteed output current
- Wide range of output voltages available on request: adjustable from 0.8 V, fixed up to 12 V in 100 mV steps
- Logic-controlled electronic shutdown
- Power Good (PPAK and DFN packages)
- Fast dynamic response to line and load changes
- Internal current and thermal protection
- Temperature range: - 40 °C to 125 °C

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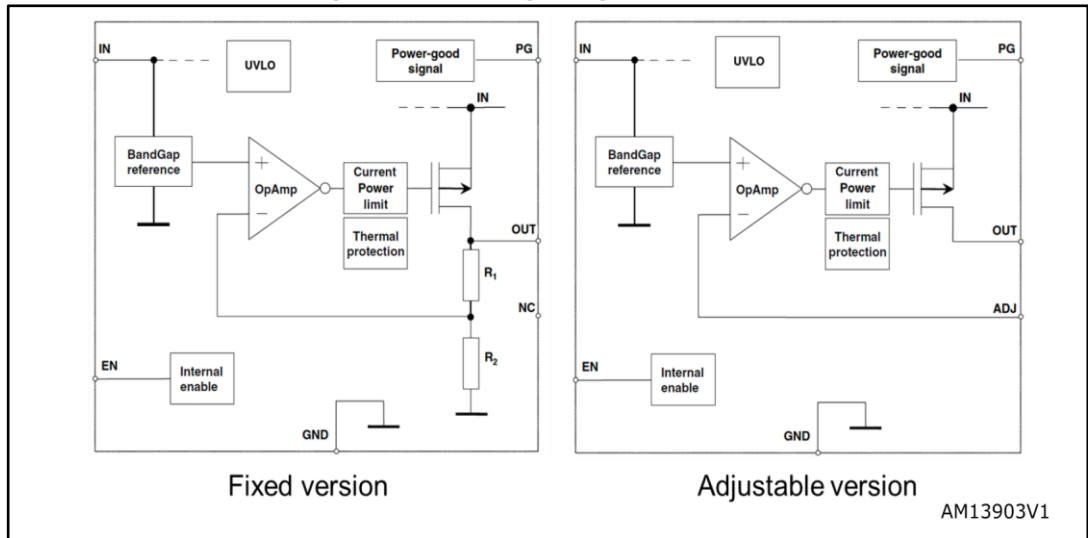
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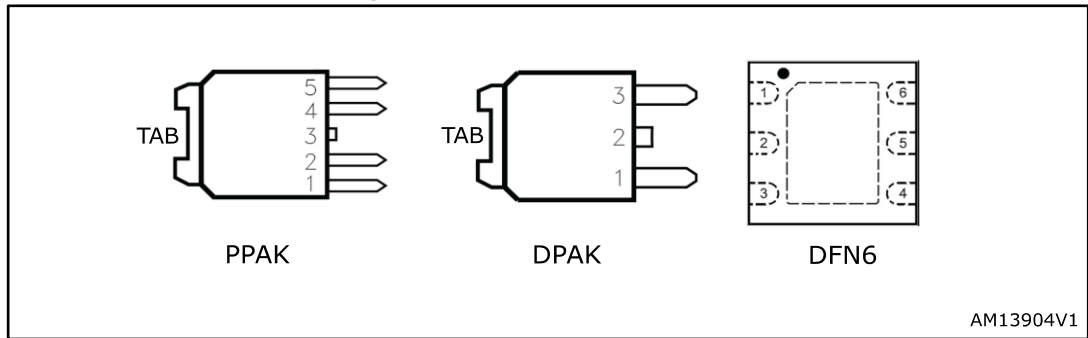
# 1 Block diagram

Figure 1: Block diagram (generic version)



## 2 Pin configuration

Figure 2: Pin connection (top view)



AM13904V1

Table 1: Pin description DPAK, PPAK

Pin n°		Symbol	Function
PPAK	DPAK		
5	-	ADJ/PG	For adjustable versions: error amplifier input pin. For fixed version: Power Good output
2	1	V <sub>IN</sub>	Input voltage
4	3	V <sub>OUT</sub>	Output voltage
1	-	EN	Enable pin logic input: Low = shutdown, High = active
3	2	GND	Ground
TAB	TAB	GND	Ground

Table 2: Pin description DFN6-2x2 and 3x3

Pin n°	Symbol	Function
2	ADJ/NC	For adjustable versions: error amplifier input pin. For fixed version: not connected
6	V <sub>IN</sub>	Input voltage
1	V <sub>OUT</sub>	Output Voltage
5	EN	Enable pin logic input: low = shutdown, high = active
3	PG	Power good output
4	GND	Ground
exposed pad	GND	Ground

### 3 Typical application

Figure 3: Fixed versions

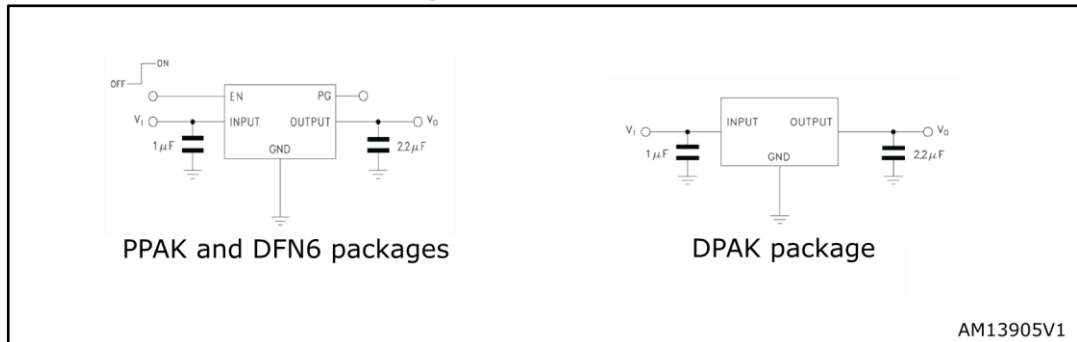
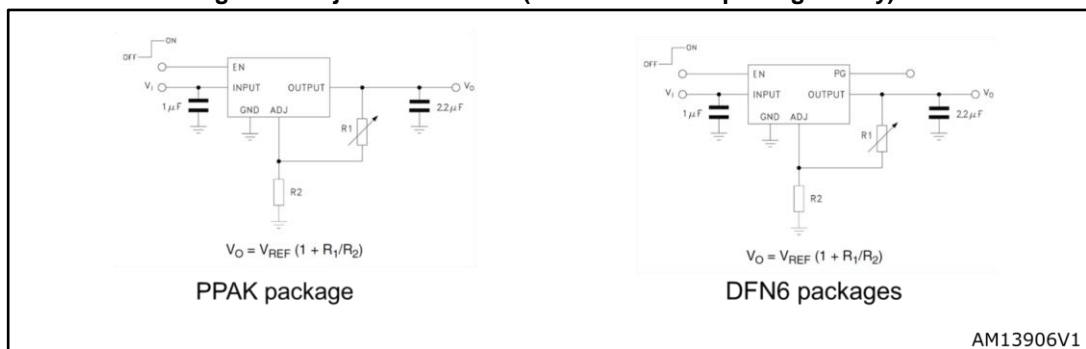


Figure 4: Adjustable version (PPAK and DFN6 packages only)



## 4 Absolute maximum ratings

Table 3: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>IN</sub>	DC input voltage	- 0.3 to 20	V
V <sub>OUT</sub>	DC output voltage	- 0.3 to V <sub>IN</sub> + 0.3	V
V <sub>EN</sub>	Enable input voltage	- 0.3 to V <sub>IN</sub> + 0.3	V
V <sub>ADJ</sub>	Adjust pin voltage	- 0.3 to 2	V
V <sub>PG</sub>	Power Good pin voltage	- 0.3 to V <sub>IN</sub> + 0.3	V
I <sub>LOAD</sub>	Output current	Internally limited	mA
P <sub>D</sub>	Power dissipation	Internally limited	mW
T <sub>STG</sub>	Storage temperature range	- 65 to 150	°C
T <sub>OP</sub>	Operating junction temperature range	- 40 to 125	°C



Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 4: Thermal data

Symbol	Parameter	Value				Unit
		PPAK	DPAK	DFN6-2x2	DFN6-3x3	
R <sub>thJA</sub>	Thermal resistance junction-ambient	100	100	65	55	°C/W
R <sub>thJC</sub>	Thermal resistance junction-case	8	8	6.5	10	°C/W

## 5 Electrical characteristics

$T_J = 25\text{ °C}$ ,  $V_{IN} = V_{OUT(NOM)} + 1\text{ V}^a$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT} = 2.2\text{ }\mu\text{F}$ ,  $I_{LOAD} = 10\text{ mA}$ ,  $V_{EN} = 2\text{ V}$ , unless otherwise specified.

**Table 5: Electrical characteristics for LDFM (fixed versions)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IN}$	Operating input voltage		2.5		16	V
$V_{OUT}$	$V_{OUT}$ accuracy, PPAK and DFN6 versions	$V_{OUT}+1\text{ V} \leq V_{IN} \leq 16\text{ V}^{(1)}$ $I_{LOAD} = 10\text{ mA}$	-1		1	%
		$10\text{ mA} \leq I_{LOAD} \leq 500\text{ mA}$ $T_J = -40\text{ to }125\text{ °C}$	-1.5		1.5	%
$V_{OUT}$	$V_{OUT}$ accuracy, DPAK version	$V_{OUT}+1\text{ V}^{(1)} \leq V_{IN} \leq 16\text{ V}$ $I_{LOAD} = 10\text{ mA}$	-2		2	%
		$10\text{ mA} \leq I_{LOAD} \leq 500\text{ mA}$ $T_J = -40\text{ to }125\text{ °C}$	-3		3	%
$\Delta V_{OUT}$	Static line regulation	$V_{OUT}+1\text{ V}^{(1)} \leq V_{IN} \leq 16\text{ V}$		0.01		%V
		$V_{OUT}+1\text{ V}^{(1)} \leq V_{IN} \leq 16\text{ V}$ , $T_J = -40\text{ to }125\text{ °C}$			0.04	
$\Delta V_{OUT}$	Static load regulation	$10\text{ mA} \leq I_{LOAD} \leq 500\text{ mA}$		0.1		%A
		$10\text{ mA} \leq I_{LOAD} \leq 500\text{ mA}$ , $T_J = -40\text{ to }125\text{ °C}$		0.15	0.4	
		$10\text{ mA} \leq I_{LOAD} \leq 500\text{ mA}$ , $T_J = -40\text{ to }125\text{ °C}$ DFN6 version				10
$V_{DROP}$	Dropout voltage <sup>(2)</sup>	$I_{LOAD} = 500\text{ mA}$ , $-40\text{ °C} < T_J < 125\text{ °C}$		125	300	mV
$I_Q$	Quiescent current	ON mode: $V_{EN} = 2\text{ V}$ $I_{LOAD} = 10\text{ mA to }500\text{ mA}$ , $T_J = -40\text{ to }125\text{ °C}$		200	800	$\mu\text{A}$
		OFF Mode: $V_{EN} = \text{GND}$ , PPAK and DFN versions		30		
		OFF Mode: $V_{EN} = \text{GND}$ , PPAK and DFN versions, $-40\text{ °C} < T_J < 125\text{ °C}$			120	
$I_{SC}$	Short-circuit current			0.8		A
$V_{EN}$	Enable input logic low	$V_{IN} = 2.5\text{ V to }16\text{ V}$ , $-40\text{ °C} < T_J < 125\text{ °C}$			0.8	V
	Enable input logic high		2			
$I_{EN}$	Enable pin input current	$V_{EN} = V_{IN}$		5	10	$\mu\text{A}$
PG	Power Good output threshold	Rising edge		0.92* $V_{OUT}$		V

<sup>a</sup> For  $V_{OUT} < 1.5\text{ V}$ ;  $V_{IN} = 2.5\text{ V}$ .

**Electrical characteristics**
**LDFM**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
		Falling edge		0.8* $V_{OUT}$		
	Power Good output voltage low	$I_{SINK} = 6 \text{ mA}$ , open drain output		0.4		
SVR	Supply voltage rejection	$V_{IN} = 6 \text{ V} \pm 0.5 V_{RIPPLE}$ Freq. = 120 Hz, $V_{OUT} = 5 \text{ V}$		60		dB
		$V_{IN} = 6 \text{ V} \pm 0.5 V_{RIPPLE}$ Freq. = 10 kHz, $V_{OUT} = 5 \text{ V}$		52		
$e_N$	Output noise voltage	Bw = 10 Hz to 100 kHz, $I_{LOAD} = 100 \text{ mA}$ $C_{OUT} = 2.2 \mu\text{F}$		45		$\mu\text{V}_{RMS}/V_{OUT}$
$T_{SHDN}$	Thermal shutdown			170		$^{\circ}\text{C}$
	Hysteresis			10		

**Notes:**

(1) For  $V_{OUT} < 1.5 \text{ V}$ ;  $V_{IN} = 2.5 \text{ V}$ .

(2) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply for output voltages below 1.5 V.

$T_J = 25\text{ °C}$ ,  $V_{IN} = V_{OUT(NOM)} + 1\text{ V}^a$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT} = 2.2\text{ }\mu\text{F}$ ,  $I_{LOAD} = 10\text{ mA}$ ,  $V_{EN} = 2\text{ V}$ , unless otherwise specified.

**Table 6: Electrical characteristics for LDFM (adjustable version)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IN}$	Operating input voltage		2.5		16	V
$V_{ADJ}$	Reference voltage	$V_{IN} = V_{OUT} + 1\text{ V}^{(1)}$		0.8		V
	Reference voltage tolerance	$V_{OUT} + 1\text{ V}^{(1)} \leq V_{IN} \leq 16\text{ V}$ $I_{LOAD} = 10\text{ mA}$	-1		1	%
$10\text{ mA} \leq I_{LOAD} \leq 500\text{ mA}$ $T_J = -40\text{ to }125\text{ °C}$		-1.5		1.5		
$\Delta V_{OUT}$	Static line regulation	$V_{OUT} + 1\text{ V}^{(1)} \leq V_{IN} \leq 16\text{ V}$		0.01		%V
		$V_{OUT} + 1\text{ V}^{(1)} \leq V_{IN} \leq 16\text{ V}$ , $T_J = -40\text{ to }125\text{ °C}$			0.04	
$\Delta V_{OUT}$	Static load regulation	$10\text{ mA} \leq I_{LOAD} \leq 500\text{ mA}$		0.06		%A
		$10\text{ mA} \leq I_{LOAD} \leq 500\text{ mA}$ , $T_J = -40\text{ to }125\text{ °C}$		0.2	0.4	
		$10\text{ mA} \leq I_{LOAD} \leq 500\text{ mA}$ , $T_J = -40\text{ to }125\text{ °C}$ DFN6 version			10	
$V_{DROP}$	Dropout voltage <sup>(2)</sup>	$V_{OUT}$ fixed to 2.5 V, $I_{LOAD} = 500\text{ mA}$ , $-40\text{ °C} < T_J < 125\text{ °C}$		125	300	mV
$I_Q$	Quiescent current	ON mode: $V_{EN} = 2\text{ V}$ $I_{LOAD} = 10\text{ mA to }500\text{ mA}$ , $T_J = -40\text{ to }125\text{ °C}$		200	800	$\mu\text{A}$
		OFF Mode: $V_{EN} = \text{GND}$ , PPAK and DFN versions		30		
		OFF Mode: $V_{EN} = \text{GND}$ , PPAK and DFN versions, $-40\text{ °C} < T_J < 125\text{ °C}$			120	
$I_{SC}$	Short-circuit current			0.8		A
$V_{EN}$	Enable input logic low	$V_{IN} = 2.5\text{ V to }16\text{ V}$ , $-40\text{ °C} < T_J < 125\text{ °C}$			0.8	V
	Enable input logic high		2			
$I_{EN}$	Enable pin input current	$V_{EN} = V_{IN}$		5	10	$\mu\text{A}$
PG	Power Good output threshold	Rising edge		0.92*		V
		Falling edge		0.8*		
	Power Good output voltage low	$I_{SINK} = 6\text{ mA}$ , open drain output			0.4	

<sup>a</sup> For  $V_{OUT} < 1.5\text{ V}$ ;  $V_{IN} = 2.5\text{ V}$ .

**Electrical characteristics**

**LDFM**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
SVR	Supply voltage rejection	$V_{IN} = V_{OUT} + 1\text{ V} \pm 0.5 V_{RIPPLE}$ Freq. = 120 Hz, $V_{OUT} = 0.8\text{ V}$		62		dB
		$V_{IN} = V_{OUT} + 1\text{ V} \pm 0.5 V_{RIPPLE}$ Freq. = 10 kHz, $V_{OUT} = 0.8\text{ V}$		55		
$e_N$	Output noise voltage	Bw = 10 Hz to 100 kHz, $I_{LOAD} = 100\text{ mA}$ $C_{OUT} = 2.2\text{ }\mu\text{F}$		50		$\mu\text{V}_{RMS}/V_{OUT}$
$T_{SHDN}$	Thermal shutdown			170		°C
	Hysteresis			10		

**Notes:**

<sup>(1)</sup>For  $V_{OUT} < 1.5\text{ V}$ ;  $V_{IN} = 2.5\text{ V}$ .

<sup>(2)</sup>Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply for output voltages below 1.5 V.



## 6 Application information

### 6.1 External capacitors

The LDFM requires external capacitors for regulator stability. These capacitors must be selected to meet the requirements of minimum capacitance and equivalent series resistance (see [Figure 25: "Stability plane adj \(C<sub>OUT</sub>, ESR\)"](#) and [Figure 26: "Stability plane 3.3 V \(C<sub>OUT</sub>, ESR\)"](#)). It is advisable to locate the input/output capacitors as close as possible to the relative pins.

#### 6.1.1 Input capacitor

An input capacitor with a minimum value of 1  $\mu\text{F}$  is required with the LDFM. This capacitor must be located a distance of not more than 0.5" from the input pin of the device and returned to a clean analog ground. Any good quality ceramic capacitors can be used for this capacitor.

#### 6.1.2 Output capacitor

It is possible to use ceramic capacitors but the output capacitor must meet the requirements for minimum amount of capacitance and E.S.R. (equivalent series resistance) value.

A minimum capacitance of 2.2  $\mu\text{F}$  is a good choice to guarantee the stability of the regulator. However, other C<sub>OUT</sub> values can be used according to [Figure 25: "Stability plane adj \(C<sub>OUT</sub>, ESR\)"](#) and [Figure 26: "Stability plane 3.3 V \(C<sub>OUT</sub>, ESR\)"](#), showing the allowable ESR range as a function of the output capacitance.

The output capacitor must maintain its ESR in the stable region over the full operating temperature range to assure stability. Also, capacitor tolerance and variation with temperature must be kept in consideration in order to assure the minimum amount of capacitance at all times.

### 6.2 Enable pin operation

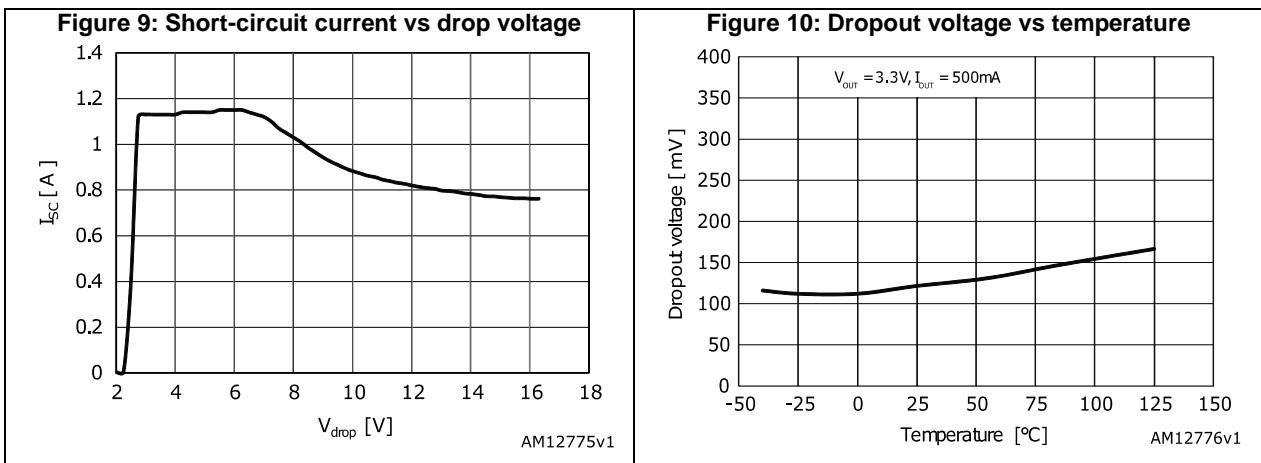
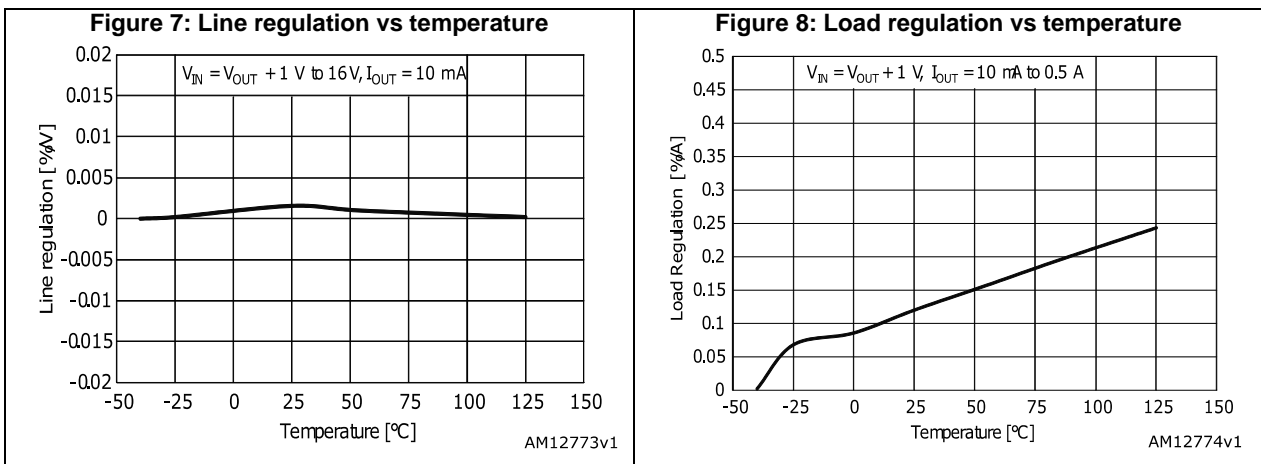
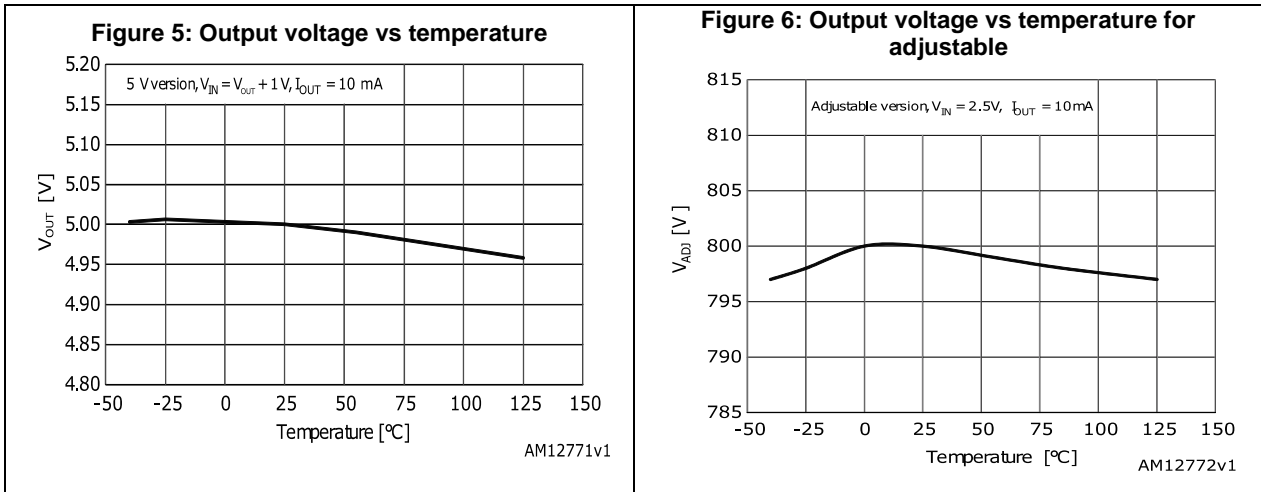
The Enable pin can be used to turn OFF the regulator when pulled down, so drastically reducing the current consumption. When the enable feature is not used, this pin must be tied to V<sub>IN</sub> to keep the regulator output ON at all times. To assure proper operation, the signal source used to drive the Enable pin must be able to swing above and below the specified thresholds listed in the electrical characteristics section (V<sub>EN</sub>). The Enable pin must not be left floating because it is not internally pulled down/up.

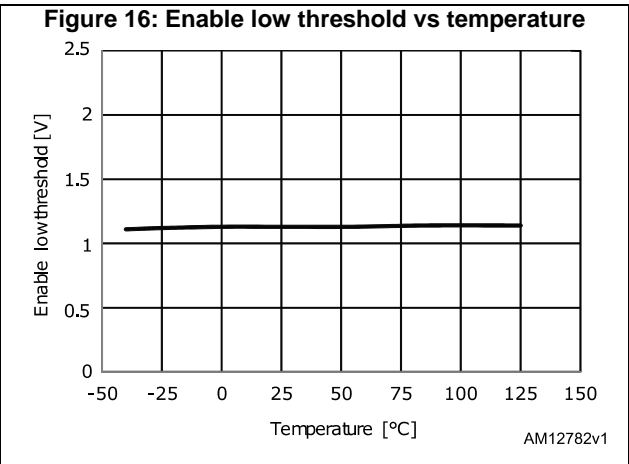
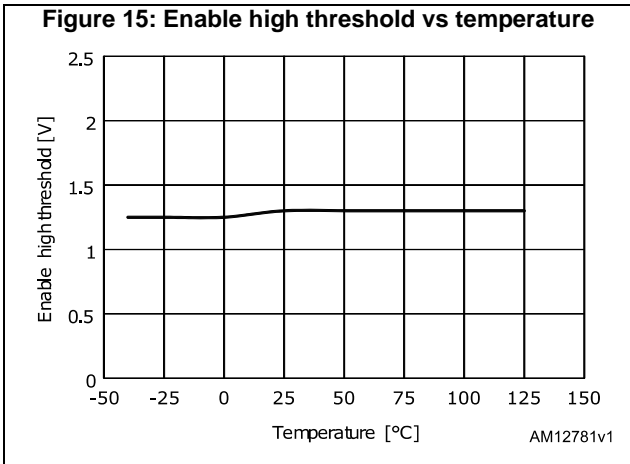
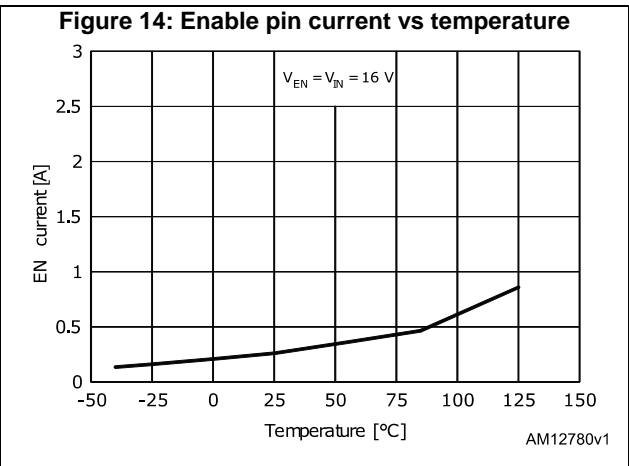
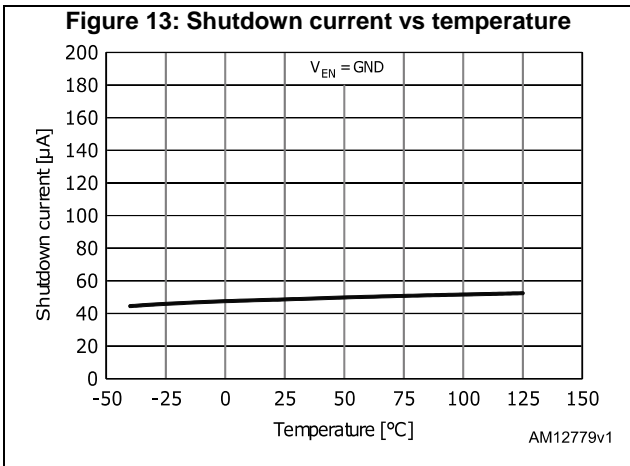
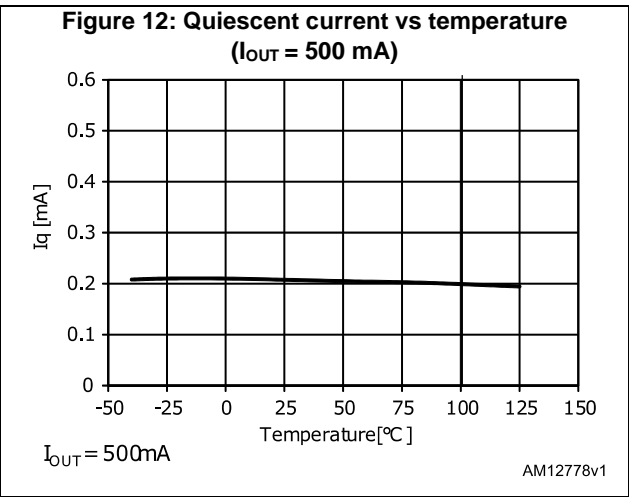
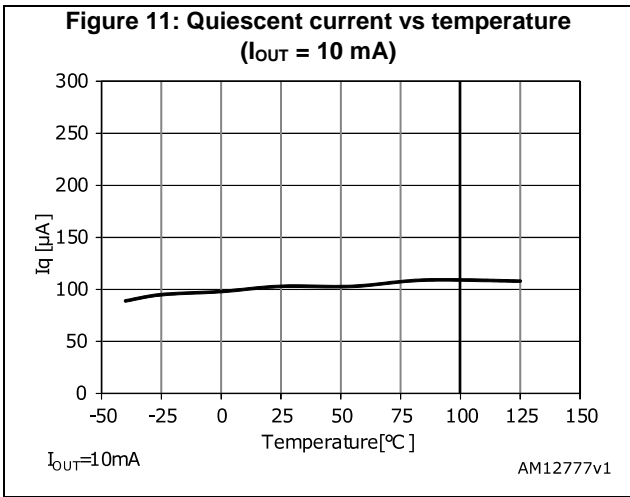
### 6.3 Power Good

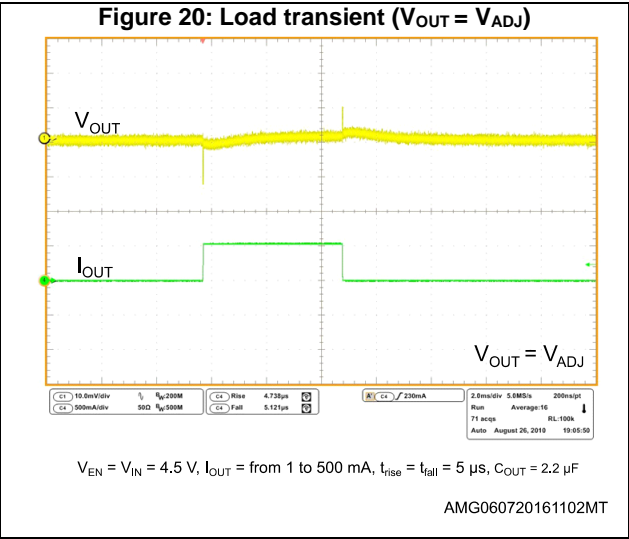
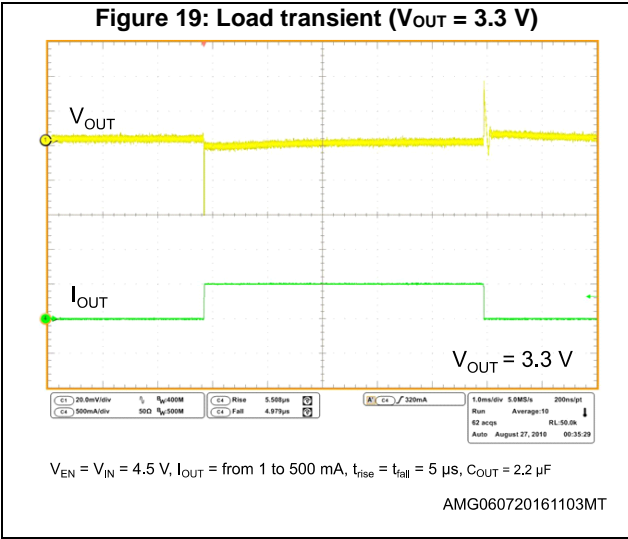
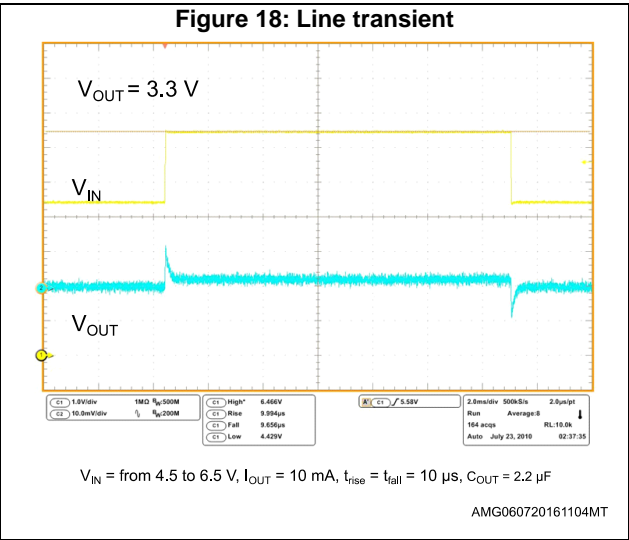
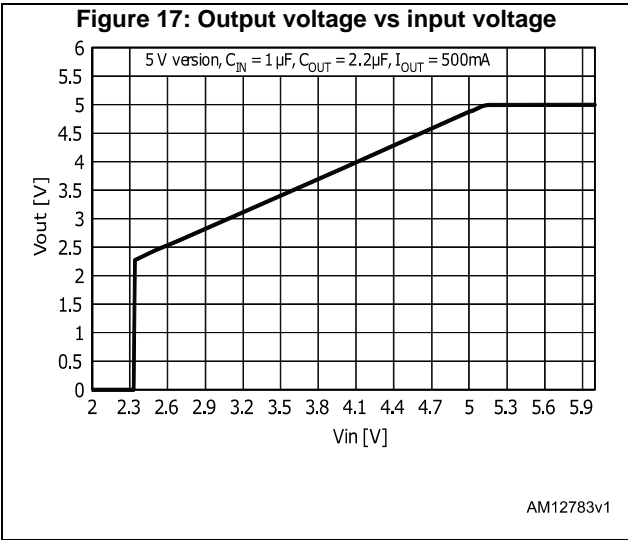
The LDFM features an open drain Power Good (PG) pin to sequence external supplies or loads and to provide fault detection. This pin requires an external resistor (R<sub>PG</sub>) to pull PG high when the output is within the PG tolerance window. Typical values for this resistor range from 10 k $\Omega$  to 100 k $\Omega$ .

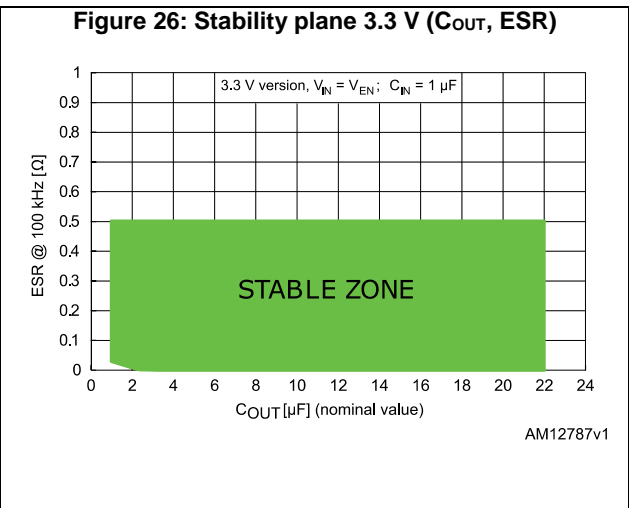
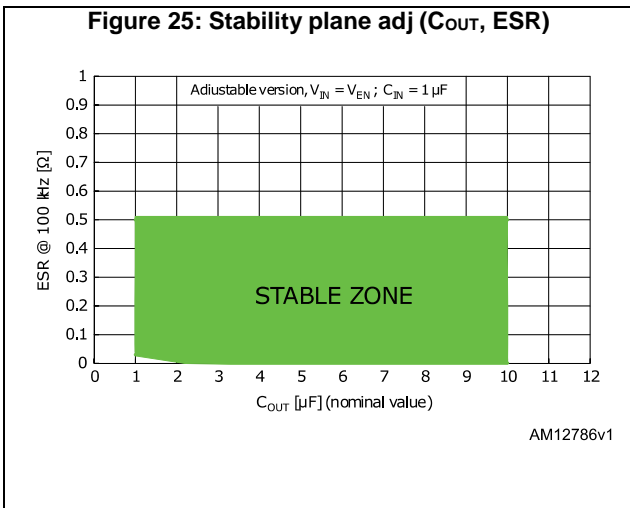
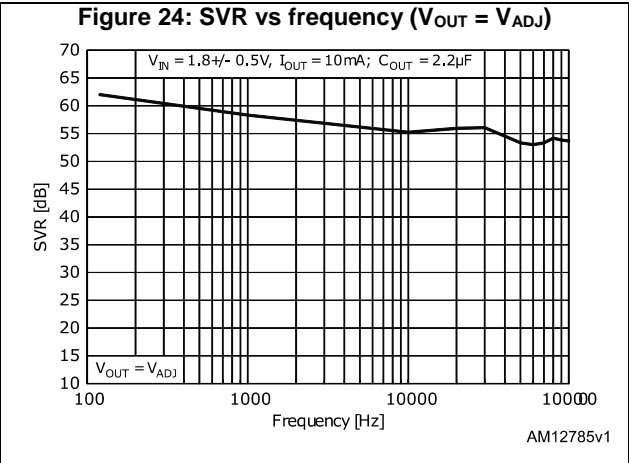
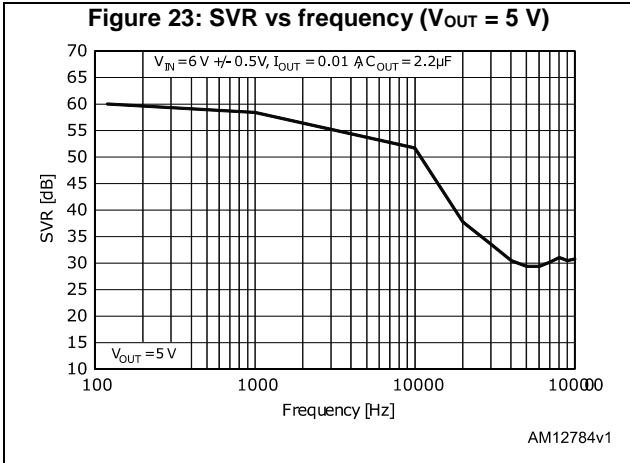
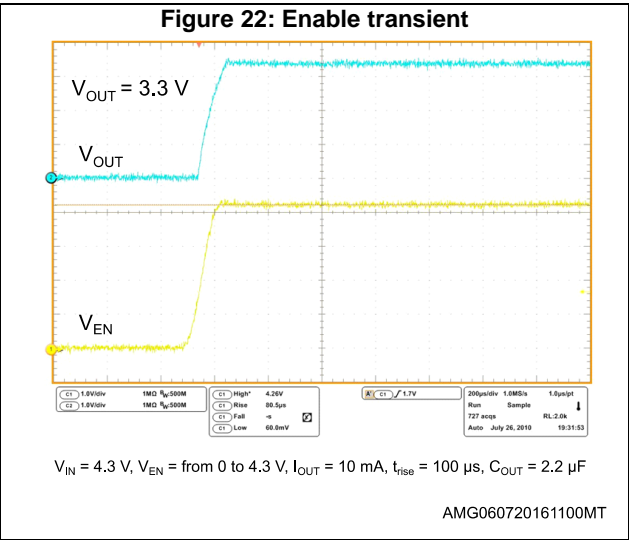
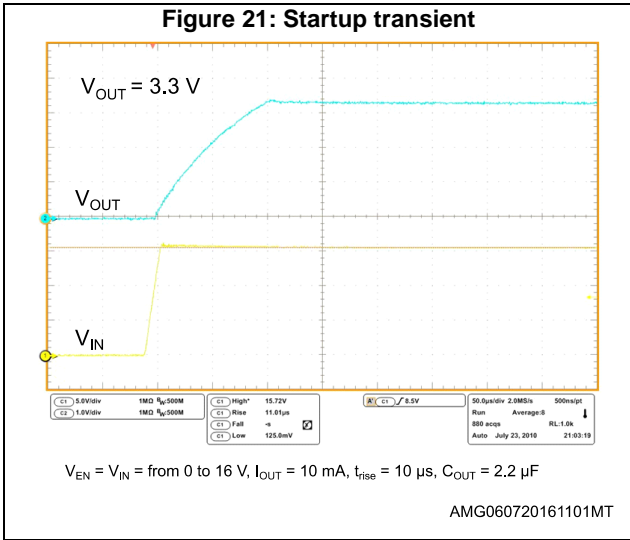
## 7 Typical performance characteristics

$C_{IN} = C_{OUT} = 1 \mu F$ ,  $V_{IN} = V_{OUT} + 1 V$ ,  $V_{EN}$  to  $V_{IN}$ ,  $I_{OUT} = 10 mA$ , unless otherwise specified.







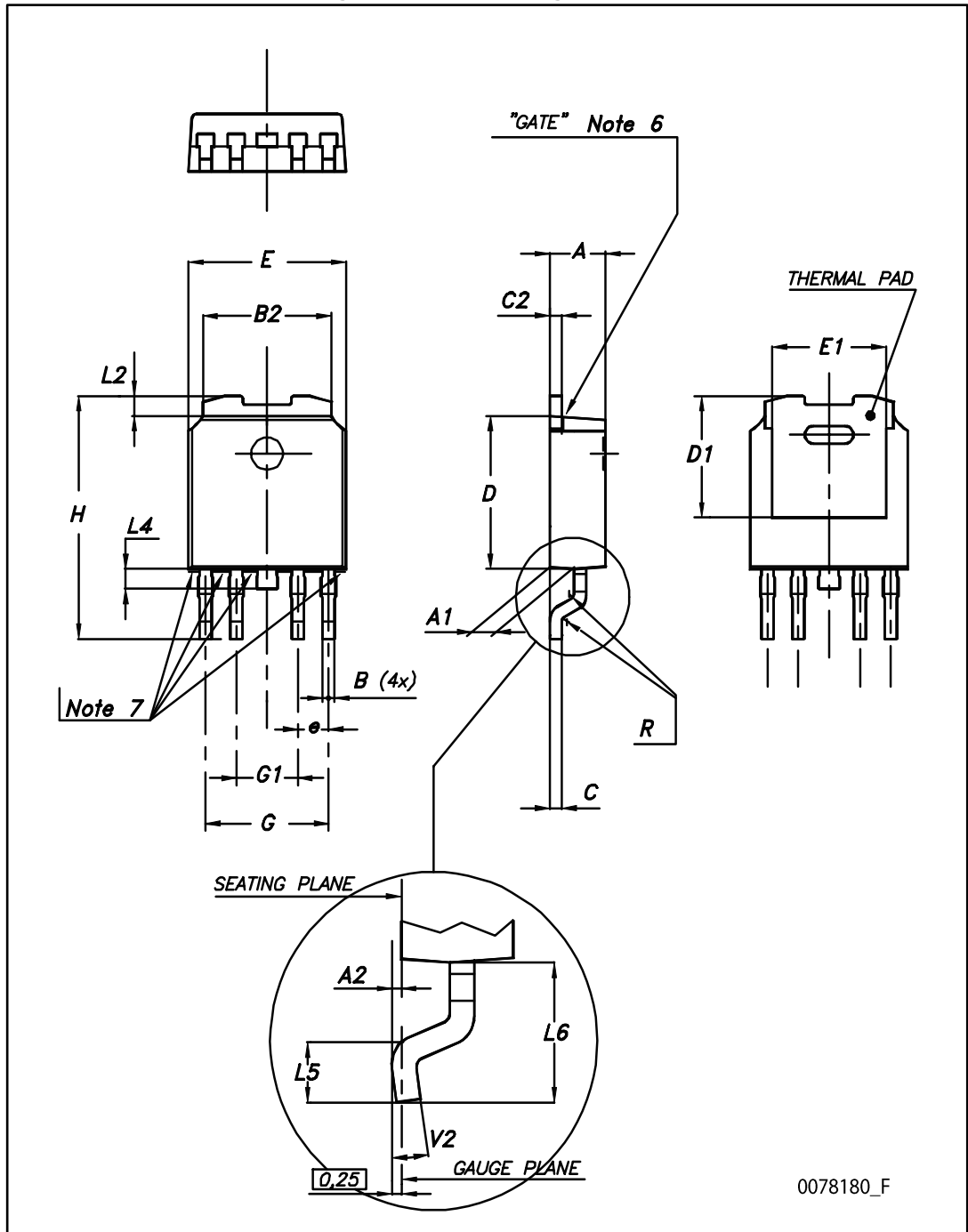


## 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

# 8.1 PPAK package information

Figure 27: PPAK package outline



0078180\_F

Table 7: PPAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.2		2.4
A1	0.9		1.1
A2	0.03		0.23
B	0.4		0.6
B2	5.2		5.4
C	0.45		0.6
C2	0.48		0.6
D	6		6.2
D1		5.1	
E	6.4		6.6
E1		4.7	
e		1.27	
G	4.9		5.25
G1	2.38		2.7
H	9.35		10.1
L2		0.8	1
L4	0.6		1
L5	1		
L6		2.8	
R		0.20	
V2	0°		8°

## 8.2 PPAK packing information

Figure 28: PPAK tape outline

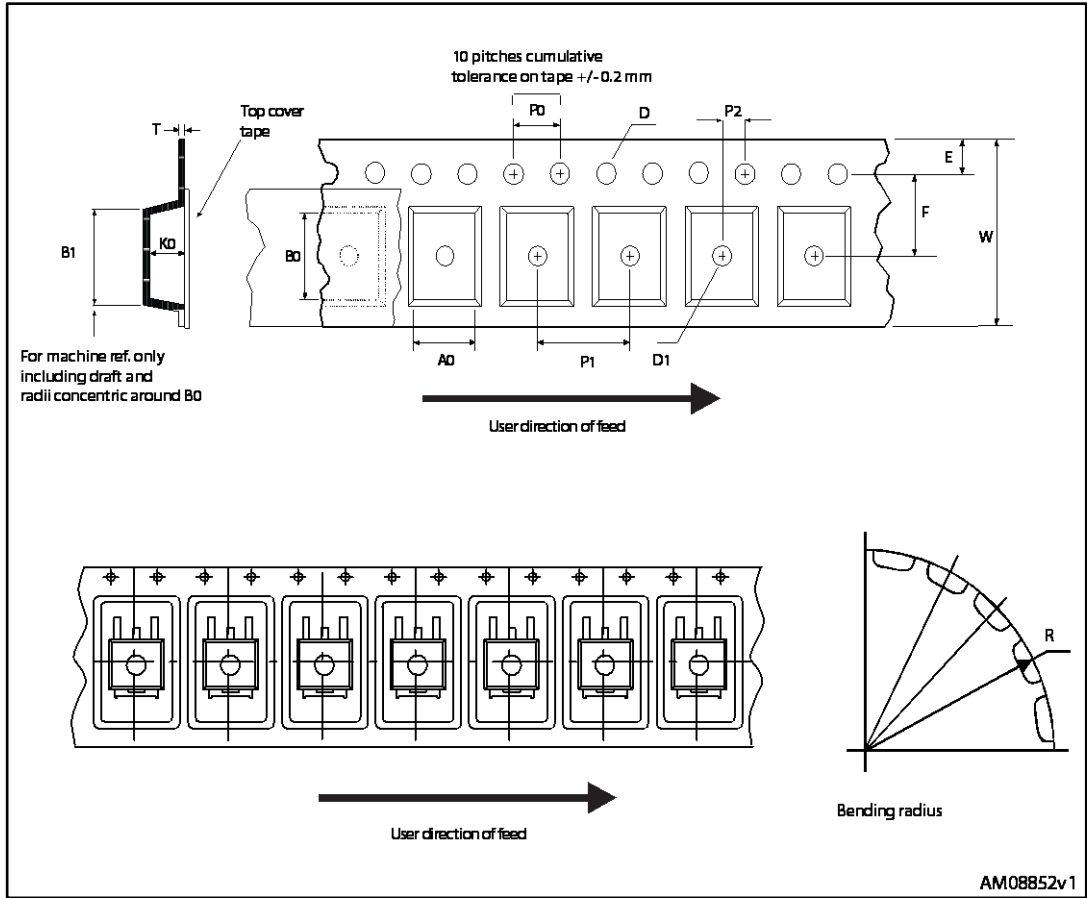


Figure 29: PPAK reel outline

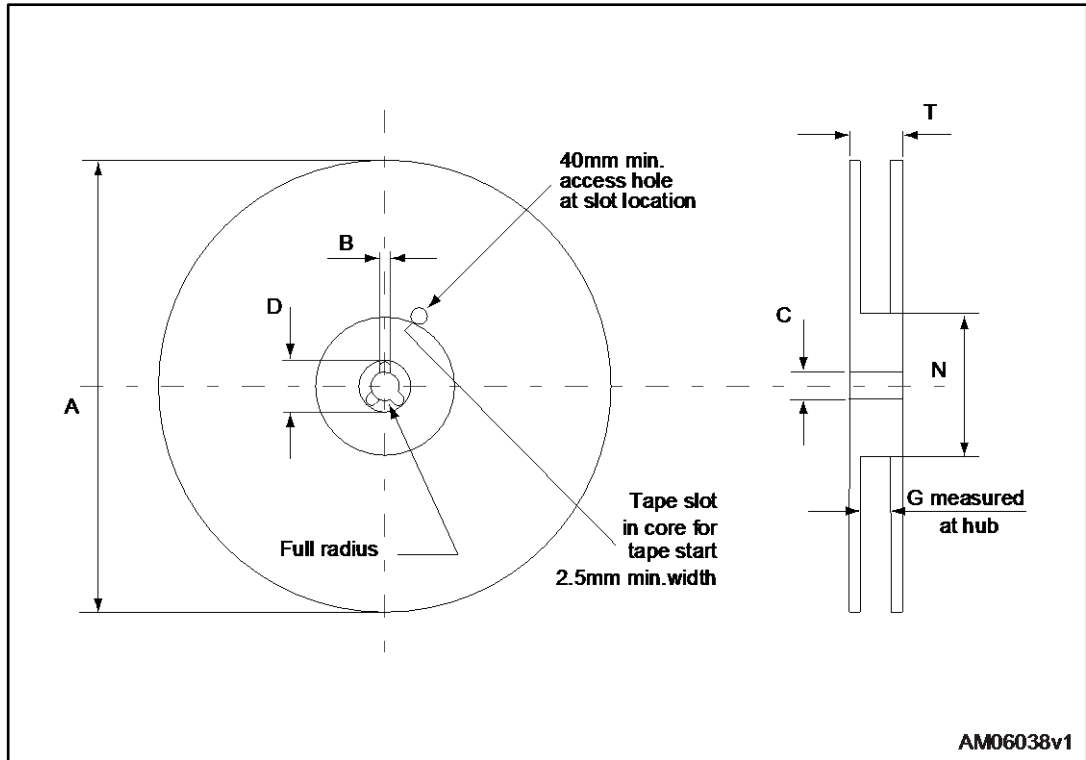


Table 8: PPAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

### 8.3 DPAK (TO-252) package information

Figure 30: DPAK (TO-252) package outline

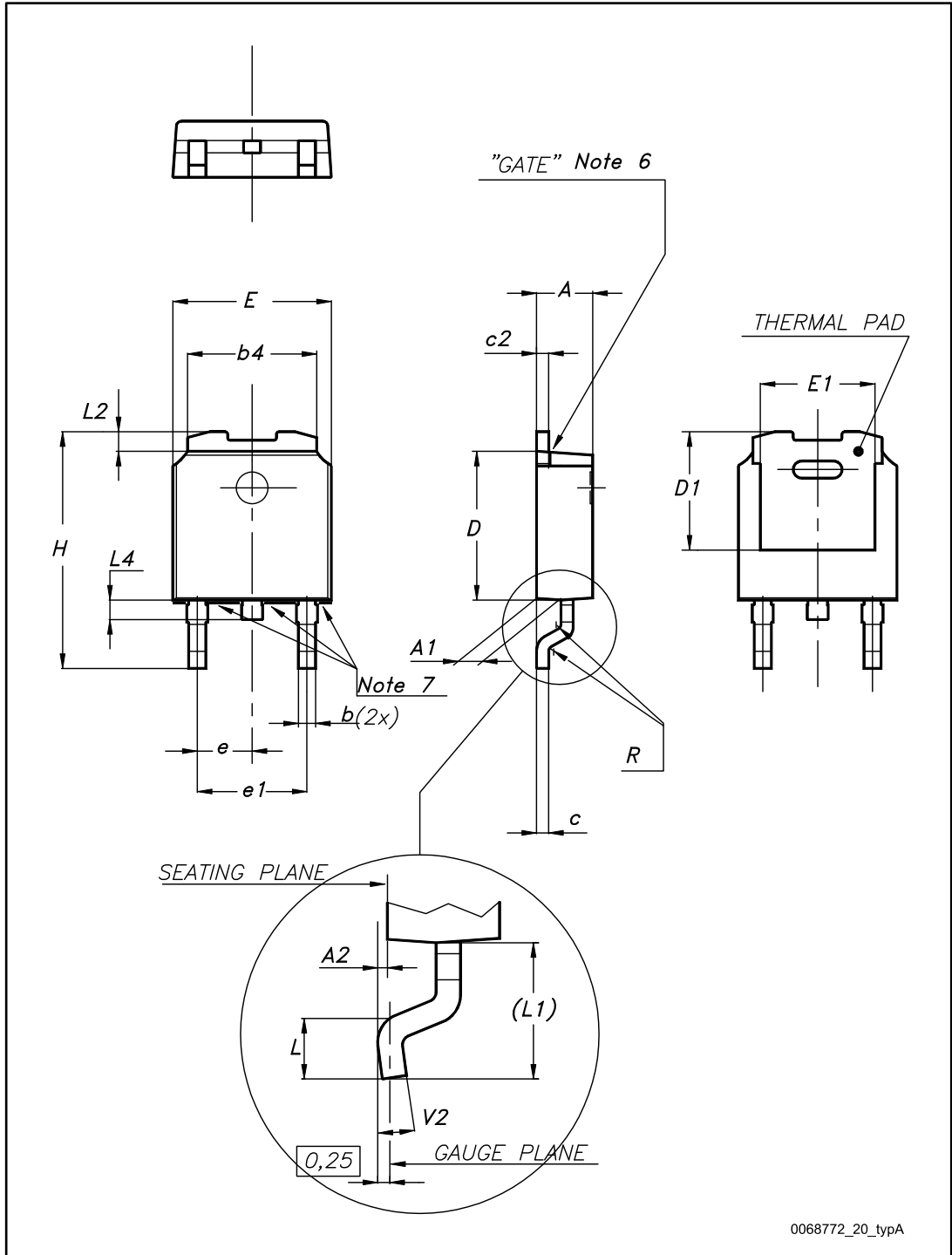


Table 9: DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		5.20	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°



### 8.4 DPAK (TO-252) packing information

Figure 32: DPAK (TO-252) tape outline

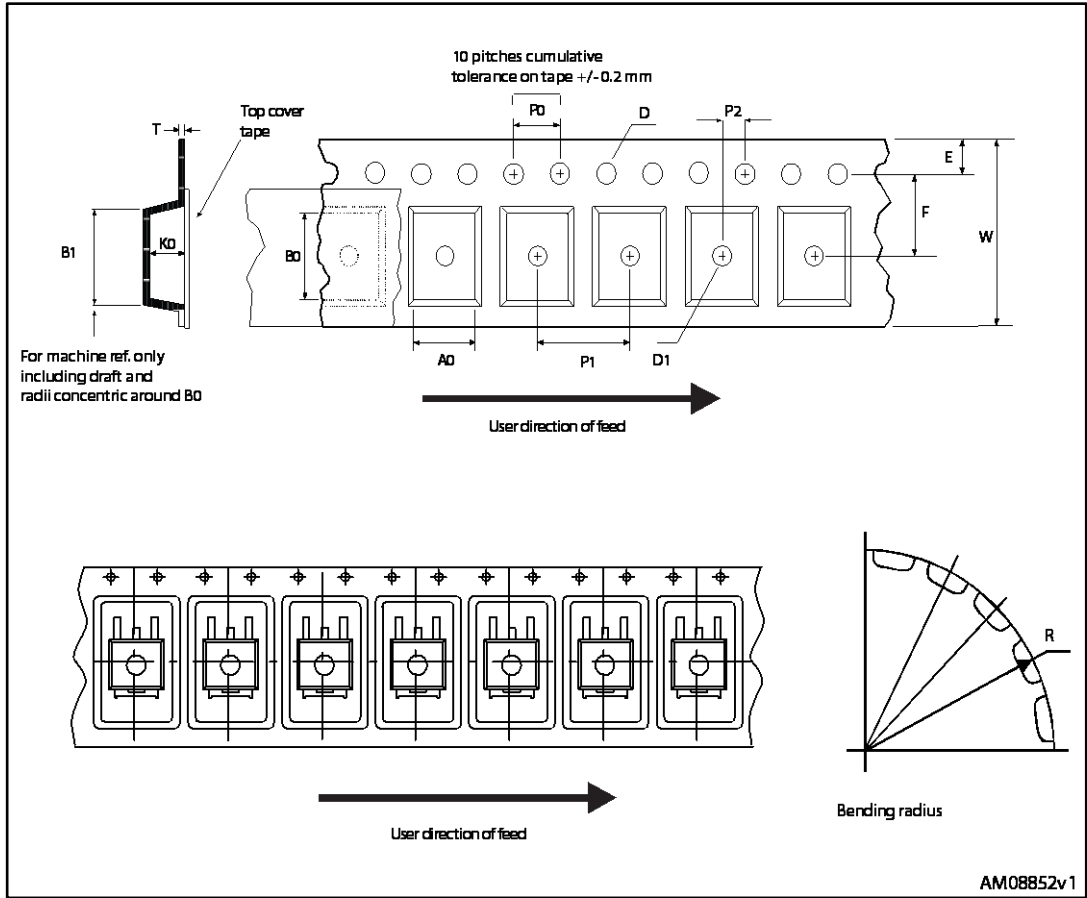


Figure 33: DPAK (TO-252) reel outline

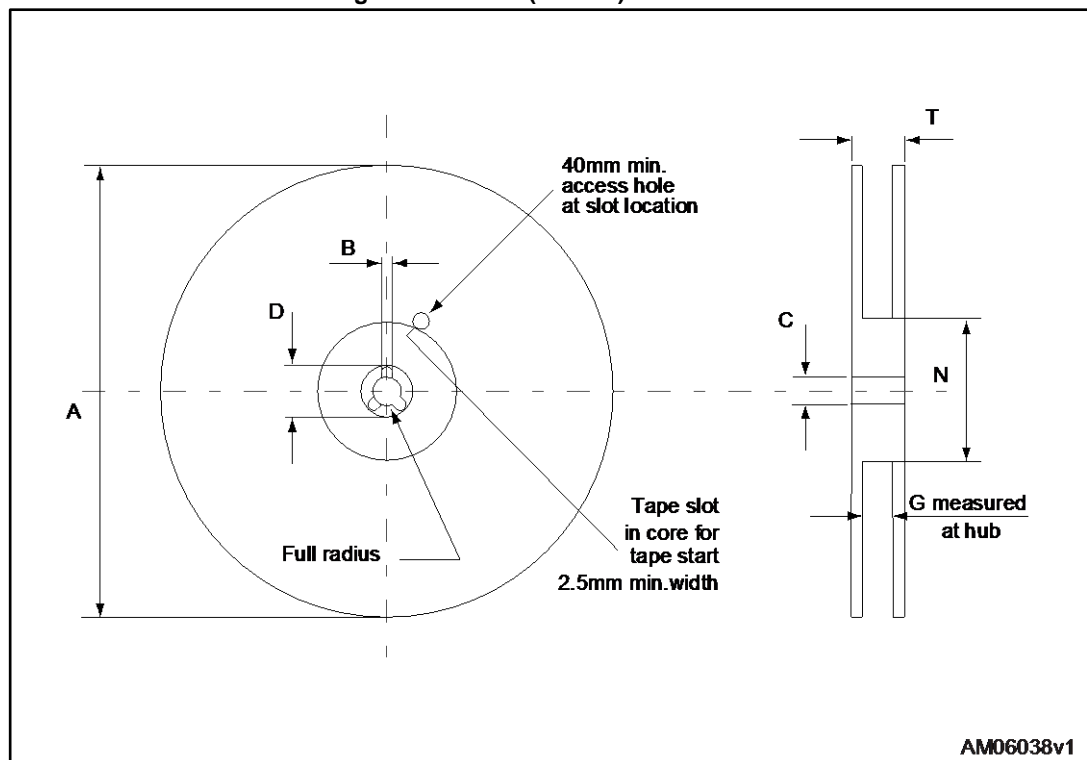


Table 10: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

### 8.5 DFN6 (2x2) package information

Figure 34: DFN6 (2x2) package outline

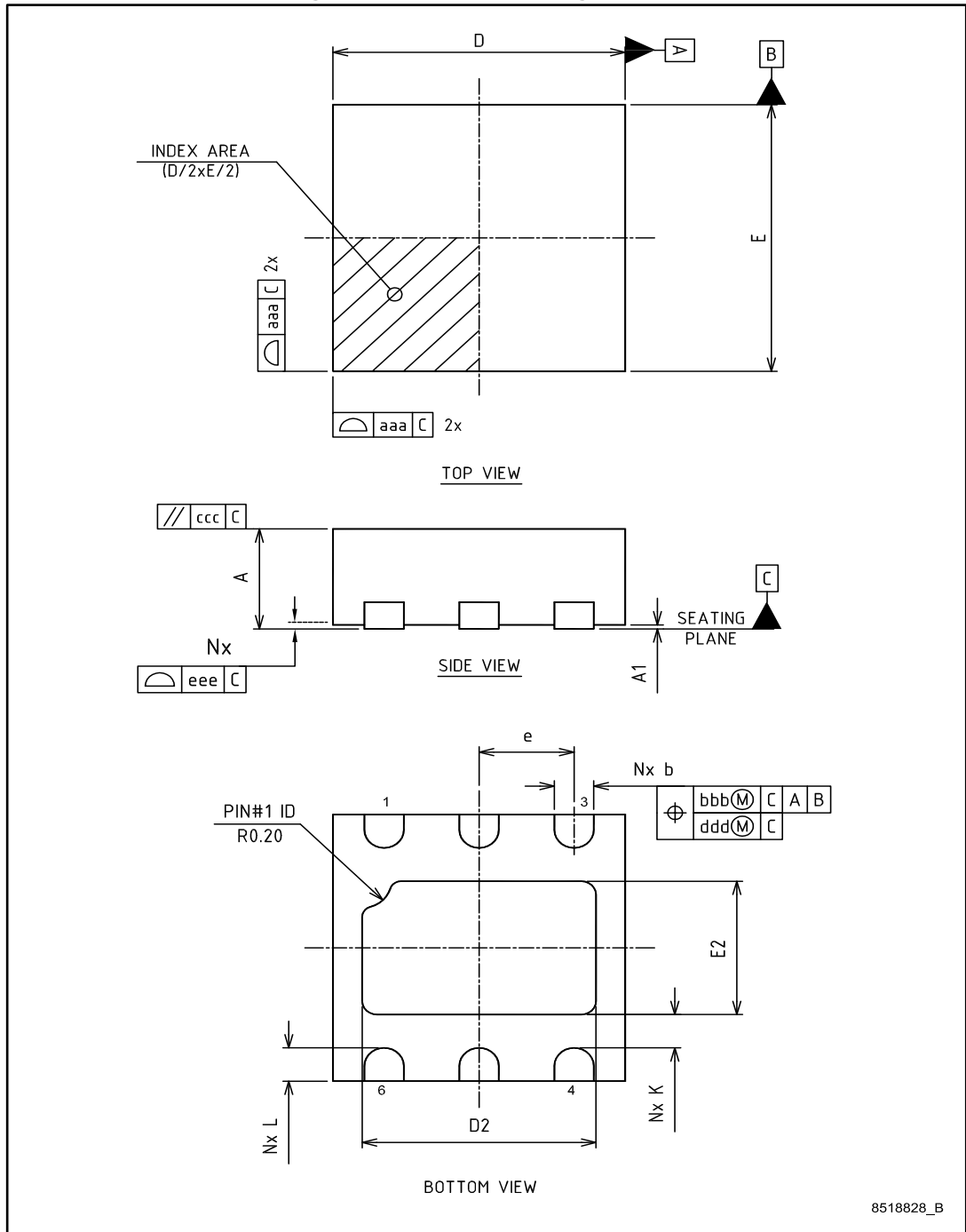
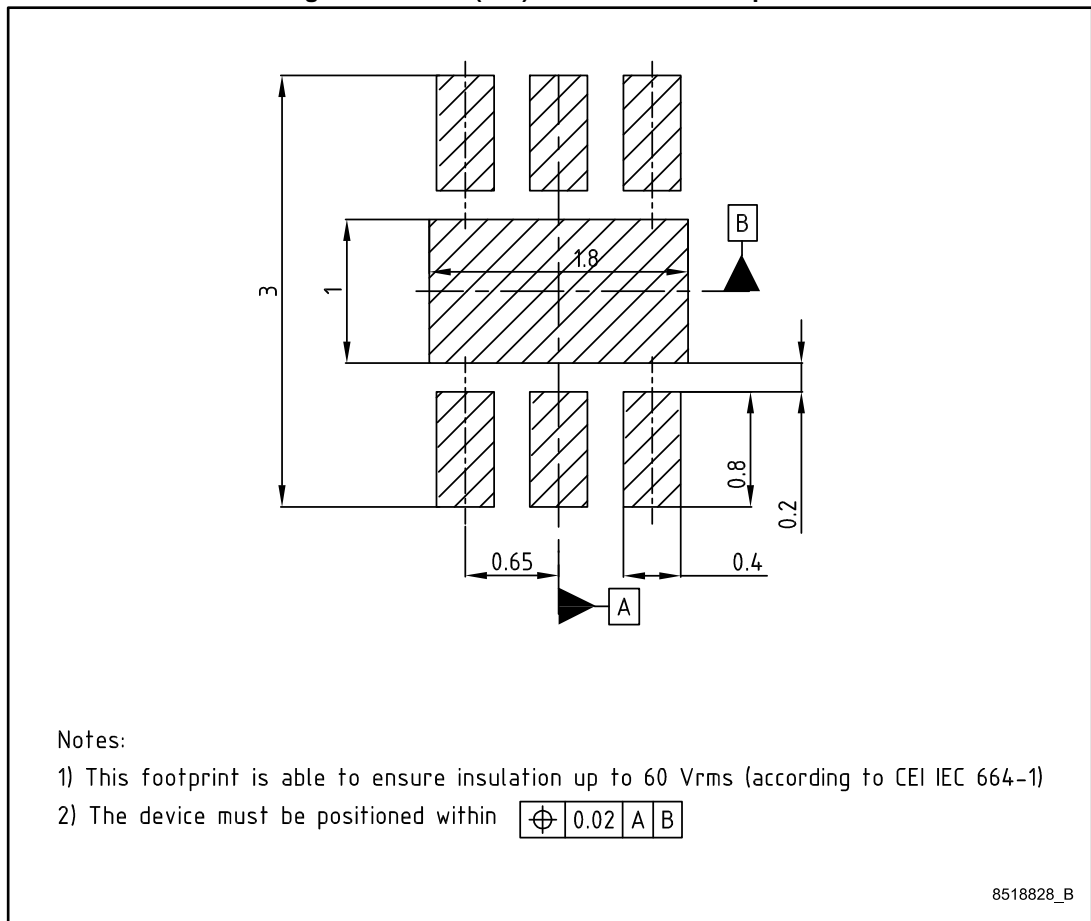


Table 11: DFN6 (2x2) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.25	0.30	0.35
D	2.00 BSC		
E	2.00 BSC		
e	0.65 BSC		
D2	1.45		1.70
E2	0.85		1.10
L	0.20		0.30
K	0.15		
aaa	0.05		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
N	6		

Figure 35: DFN6 (2x2) recommended footprint



## 8.6 DFN6 (2x2) packing information

Figure 36: DFN6 (2x2) reel outline

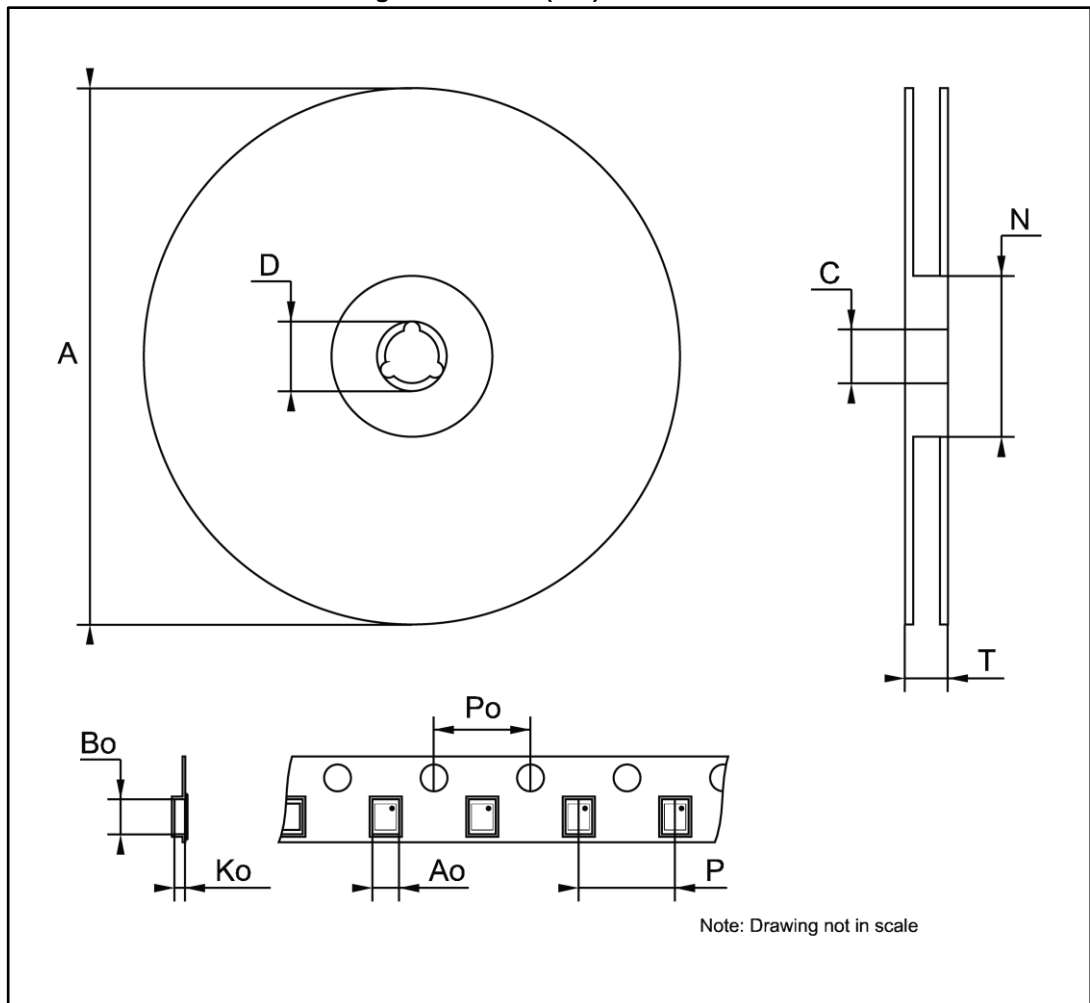


Table 12: DFN6 (2x2) tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			180
C	12.8		13.2
D	20.2		
N	60		
T			14.4
A0		2.4	
B0		2.4	
K0		1.3	
P0		4	
P		4	

### 8.7 DFN6 (3x3) package information

Figure 37: DFN6 (3x3) package outline

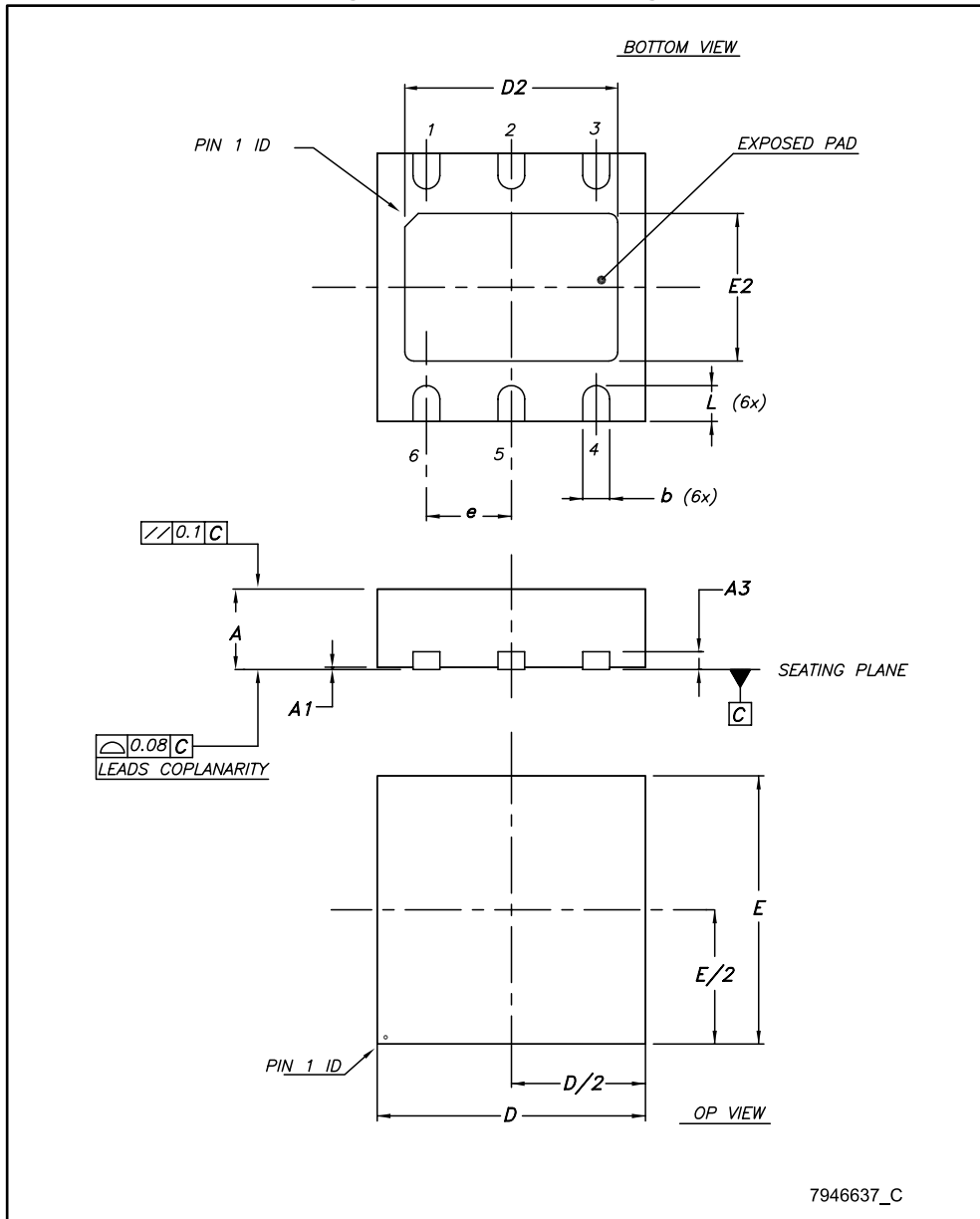


Table 13: DFN6 (3x3) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1
A1	0	0.02	0.05
A3		0.20	
b	0.23		0.45
D	2.90	3	3.10
D2	2.23		2.50
E	2.90	3	3.10
E2	1.50		1.75
e		0.95	
L	0.30	0.40	0.50

Figure 38: DFN6 (3x3) recommended footprint

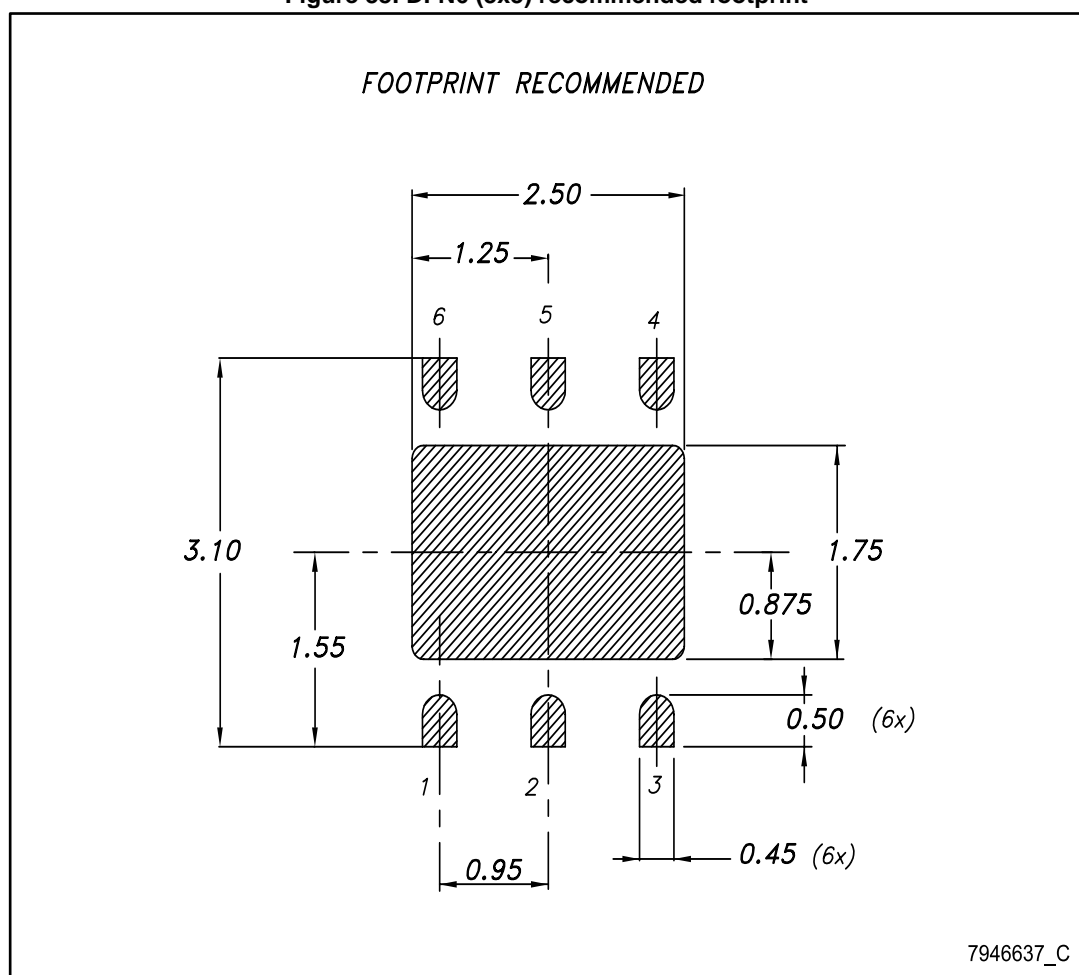




Figure 40: DFN6 (3x3) reel outline

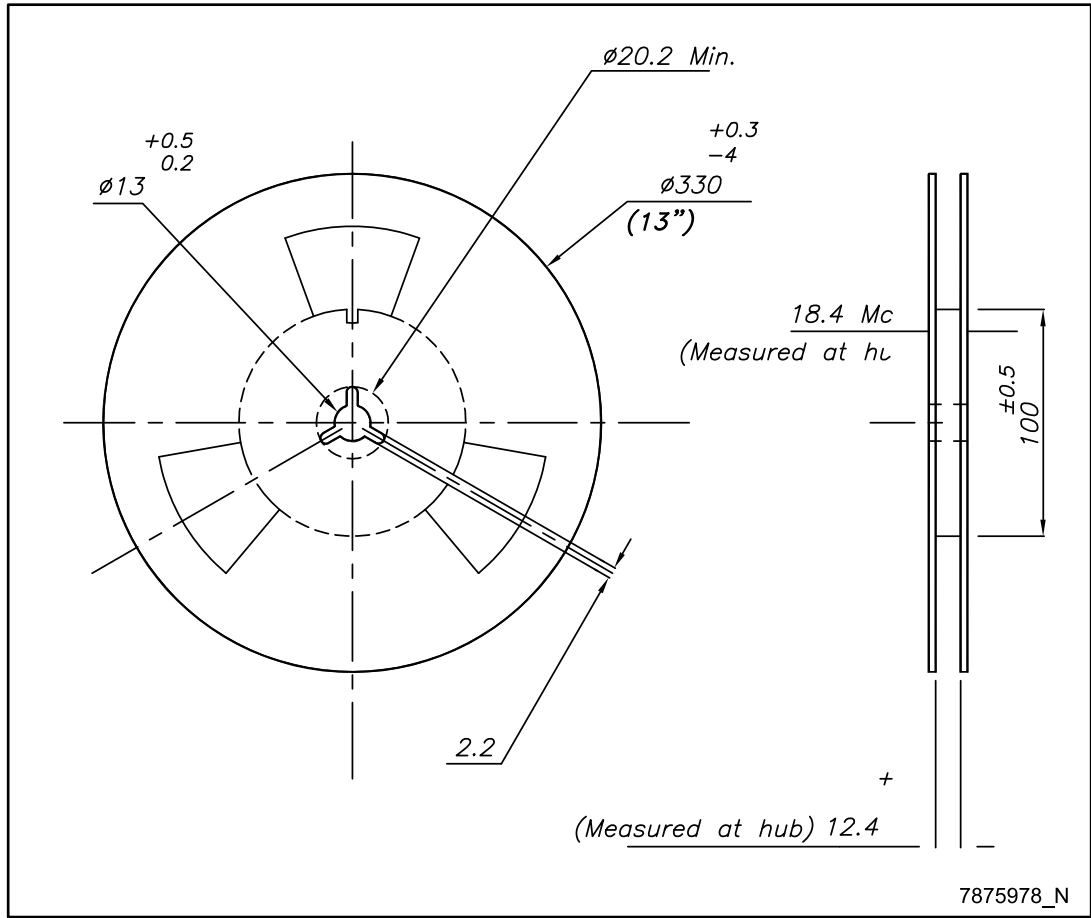


Table 14: DFN6 (3x3) tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A0	3.20	3.30	3.40
B0	3.20	3.30	3.40
K0	1	1.10	1.20

## 9 Ordering information

Table 15: Order code

DPAK	PPAK	DFN6-2x2	DFN6-3x3	Output voltage
LDFM33DT-TR	LDFM33PT-TR	LDFM33PVR	LDFM33PUR	3.3 V
LDFM50DT-TR	LDFM50PT-TR			5 V
	LDFMPT-TR	LDFMPVR	LDFMPUR	ADJ from 0.8 V

## 10 Revision history

**Table 16: Document revision history**

Date	Revision	Changes
28-Aug-2012	1	Initial release.
22-Nov-2013	2	Part numbers LDFM and LDFM50 have been unified under LDFM. Updated the Features and the Description in cover page. Cancelled <i>Table 1: Device summary</i> . Updated <i>Section 2: Pin configuration</i> , <i>Section 3: Typical application</i> , <i>Section 4: Absolute maximum ratings</i> , <i>Section 5: Electrical characteristics</i> and <i>Section 8: Package information</i> . Added <i>Section 8.7: DFN6 (3 x 3 mm) packing information</i> and <i>Section 9: Order code</i> . Minor text changes.
15-Jun-2015	3	Updated <i>Table 5: Electrical characteristics for LDFM (fixed versions)</i> and <i>Table 6: Electrical characteristics for LDFM (adjustable version)</i> . Minor text changes.
05-Sep-2016	4	Updated <i>Section 9: "Ordering information"</i> . Minor text changes.
05-Jul-2017	5	Updated <i>Section 9: "Ordering information"</i> . Minor text changes.

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