THE DATASHEET OF

LM3241TLX/NOPB

LM3241 6-MHz, 750-mA Miniature, Adjustable, Step-Down DC-DC Converter for RF Power Amplifiers

1 Features

- 6-MHz (typ.) PWM Switching Frequency
- Operates from a Single Li-Ion Cell (2.7 V to 5.5 V)
- Adjustable Output Voltage (0.6 V to 3.4 V)
- 750-mA Maximum Load Capability
- High Efficiency (95% typ. at 3.9 V_{IN}, 3.3 V_{OUT} at 500 mA)
- Automatic Eco-mode™ and PWM Mode Change
- 6-Bump DSBGA Package
- Current Overload Protection
- Thermal Overload Protection
- Soft Start Function
- C_{IN} and C_{OUT} are 0402 (1005) Case Size and 6.3 V of Rated-Voltage Ceramic Capacitor
- Small Chip Inductor in 0805 (2012) Case Size

2 Applications

- Battery-Powered 3G and 4G Power Amplifiers
- Hand-Held Radios
- RF PC Cards
- Battery-Powered RF Devices

3 Description

The LM3241 is a DC-DC converter optimized for powering RF power amplifiers (PAs) from a single Lithium-Ion cell. The device can also be used in many other applications. The device steps down an input voltage from 2.7 V to 5.5 V to an adjustable output voltage from 0.6 V to 3.4 V. The output voltage is set using a VCON analog input for controlling power levels and efficiency of the RF PA.

The LM3241 offers three modes of operation. In PWM mode the device operates at a fixed frequency of 6 MHz (typical) which minimizes RF interference when driving medium-to-heavy loads. At light-load conditions, the device enters into Eco-mode automatically and operates with reduced switching frequency. In Eco-mode, the quiescent current is reduced and extends the battery life. Shutdown mode turns the device off and reduces battery consumption to 0.1 µA (typical).

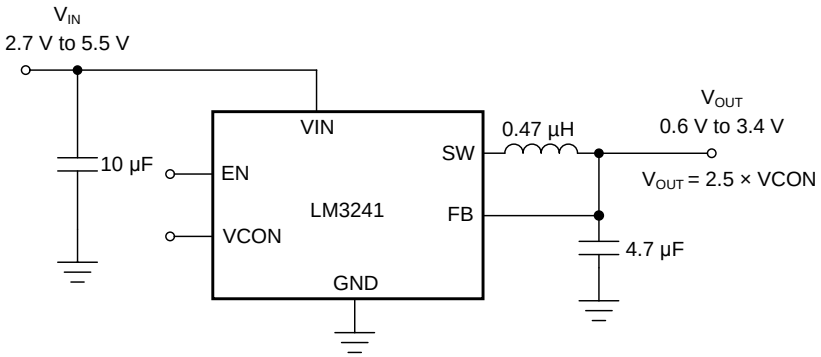
The LM3241 is available in a 6-bump lead-free DSBGA package. A high-switching frequency (6 MHz) allows use of tiny surface-mount components. Only three small external surface-mount components, an inductor and two ceramic capacitors are required.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM3241	DSBGA (6)	1.50 mm × 1.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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4 Revision History

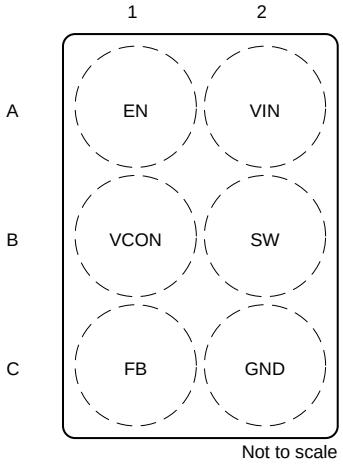
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2013) to Revision C **Page**

- Added the *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted the maximum lead temperature parameter from the *Absolute Maximum Ratings* table ... 4
- Changed the minimum T_J and T_A from –30°C to –40°C in the *Recommended Operating Conditions* table ... 4
- Added the *Thermal Information* table ... 4
- Added maximum values for VOUT step rise and fall times under –40°C to 85°C T_A range in the *System Characteristics* table ... 6
- Added maximum value for turnon time under –40°C to 85°C T_A range in the *System Characteristics* table ... 6

5 Pin Configuration and Functions

YZR Package With 0.5 mm Pitch
6-Pin DSBGA
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	EN	I	Enable Input. Set this digital input high for normal operation. For shutdown, set low. Do not leave EN pin floating.
A2	VIN	PWR	Power supply input. Connect to the input filter capacitor (see Figure 29).
B1	VCON	I	Voltage Control Analog input. VCON controls VOUT in PWM mode. Do not leave VCON pin floating. V_{OUT} = 2.5 × VCON.
B2	SW	PWR	Switching Node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the maximum Switch Peak Current Limit specification of the LM3241.
C1	FB	I	Feedback Analog Input. Connect to the output at the output inductor.
C2	GND	—	Ground

6 Specifications

6.1 Absolute Maximum Ratings

See (1) and (2).

		MIN	MAX	UNIT
Pin voltage	VIN to GND	–0.2	6	V
	EN, FB, VCON, SW	(GND − 0.2)	(VIN + 0.2) (3)	
Continuous power dissipation (4)		Internally limited		
Junction temperature, $T_{J\text{-}MAX}$			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pins.
(3) All pins are limited to the 6-V maximum stated for the VIN supply.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 125°C (typical).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) (2)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (3)	1250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. (MIL-STD-883 3015.7).
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See (1).

		MIN	NOM	MAX	UNIT
	Input voltage	2.7		5.5	V
	Recommended load current	0		750	mA
T_J	Junction temperature	–40		125	°C
T_A	Ambient temperature (2)	–40		85	°C

(1) All voltages are with respect to the potential at the GND pins.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})$.

6.4 Thermal Information

THERMAL METRIC (1)		LM3241 YZR (DSBGA) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	117	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

All voltages are with respect to the potential at the GND pins. Minimum (MIN) and maximum (MAX) limits are specified by design, test, or statistical analysis. For performance over the input voltage range and closed-loop results, see the curves in the *Typical Characteristics* section.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{FB,MIN}$	Feedback voltage at minimum setting	PWM mode, VCON = 0.24 V		0.6		V
		PWM mode, open loop conditions at V_{IN} = 3.6 V, VCON = 0.24 V	0.58		0.62	
$V_{FB,MAX}$	Feedback voltage at maximum setting	PWM mode, VCON = 1.36 V, V_{IN} = 3.9 V		3.4		V
		PWM mode, open loop conditions at V_{IN} = 3.6 V, VCON = 1.36 V, V_{IN} = 3.9 V	3.332		3.468	
I_{SHDN}	Shutdown supply current	EN = SW = VCON = 0 V(1)		0.1		µA
		open loop conditions at V_{IN} = 3.6 V, EN = SW = VCON = 0 V(1)			2	
I_Q_PWM	PWM mode quiescent current	PWM mode, No switching(2), VCON = 0 V, FB = 1 V		620		µA
		PWM mode, open loop conditions at V_{IN} = 3.6 V, No switching(2), VCON = 0 V, FB = 1 V			750	
I_Q_ECO	Eco-mode quiescent current	Eco-mode, No switching(2), VCON = 0.8 V, FB = 2.05 V		45		µA
		Eco-mode, open loop conditions at V_{IN} = 3.6 V, No switching(2), VCON = 0.8 V, FB = 2.05 V			60	
$R_{DSON\ (P)}$	Pin-pin resistance for PFET	V_{IN} = V_{GS} = 3.6 V, I_{SW} = 200 mA		160		mΩ
		Open loop conditions at V_{IN} = 3.6 V, V_{IN} = V_{GS} = 3.6 V, I_{SW} = 200 mA			250	
$R_{DSON\ (N)}$	Pin-pin resistance for NFET	V_{IN} = V_{GS} = 3.6 V, I_{SW} = −200 mA		110		mΩ
		Open loop conditions at V_{IN} = 3.6 V, V_{IN} = V_{GS} = 3.6 V, I_{SW} = −200 mA			200	
I_{LIM}	PFET switch peak current limit(3)			1450		mA
		Open loop conditions at V_{IN} = 3.6 V	1300		1600	
F_{OSC}	Internal oscillator frequency			6		MHz
		Open loop conditions at V_{IN} = 3.6 V	5.7		6.3	
V_{IH}	EN Logic high input threshold	Open loop conditions at V_{IN} = 3.6 V	1.2			V
V_{IL}	EN Logic low input threshold	Open loop conditions at V_{IN} = 3.6 V			0.4	V
Gain	VCON to V_{OUT} gain	0.24 V ≤ VCON ≤ 1.36 V		2.5		V/V
I_{CON}	VCON pin leakage current	Open-loop mode, VCON = 1 V			±1	µA

(1) Shutdown current includes leakage current of PFET.
(2) I_Q specified here is when the part is not switching under test mode conditions. For operating quiescent current at no load, see the curves in the *Typical Characteristics* section.
(3) Current limit is built-in, fixed, and not adjustable.

6.6 System Characteristics

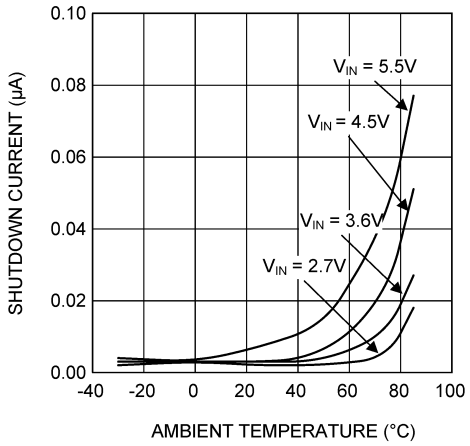
The following spec table entries are specified by design providing the component values in Figure 29 are used. These parameters are not verified by production testing. Minimum (MIN) and maximum (MAX) values apply over the full operating ambient temperature range (–40°C ≤ T_A ≤ 85°C) and over the V_{IN} range of 2.7 V to 5.5 V unless otherwise specified. L = 0.47 µH, DCR = 50 mΩ, C_{IN} = 10 µF, 6.3 V, 0603 (1608), C_{OUT} = 4.7 µF, 6.3 V, 0603 (1608).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{CON\ TR}$	V_{OUT} step rise time from 0.6 V to 3.4 V (to reach 3.26 V)	V_{IN} = 3.6 V, VCON = 0.24 V to 1.36 V, VCON T_R = 1 µs, R_{LOAD} = 10 Ω, –30°C ≤ T_A ≤ 85°C			25	µs
		V_{IN} = 3.6 V, VCON = 0.24 V to 1.36 V, VCON T_R = 1 µs, R_{LOAD} = 10 Ω			30	
	V_{OUT} step fall time from 3.4 V to 0.6 V (to reach 0.74 V)	V_{IN} = 3.6 V, VCON = 1.36 V to 0.24 V, VCON T_F = 1 µs, R_{LOAD} = 10 Ω, –30°C ≤ T_A ≤ 85°C			25	
		V_{IN} = 3.6 V, VCON = 1.36 V to 0.24 V, VCON T_F = 1 µs, R_{LOAD} = 10 Ω			30	
D	Maximum Duty cycle		100%			
I_{OUT}	Maximum output current capability	2.7 V ≤ V_{IN} ≤ 5.5 V, 0.24 V ≤ VCON ≤ 1.36 V	750			mA
C_{CON}	VCON input capacitance	VCON = 1 V, Test frequency = 100 KHz		5	10	pF
Linearity	Linearity in control range 0.24 V to 1.36 V	Monotronic in nature(1)	–3%		3%	
			–50		+50	mV
T_{ON}	Turnon time (time for output to reach 95% final value after Enable low-to-high transition)	EN = Low-to-High, V_{IN} = 4.2 V, V_{OUT} = 3.4 V, I_{OUT} = < 1 mA, C_{OUT} = 4.7 µF, –30°C ≤ T_A ≤ 85°C			50	µs
		EN = Low-to-High, V_{IN} = 4.2 V, V_{OUT} = 3.4 V, I_{OUT} = < 1 mA, C_{OUT} = 4.7 µF			55	
η	Efficiency	V_{IN} = 3.6 V, V_{OUT} = 0.8 V, I_{OUT} = 10 mA, Eco-mode		75%		
		V_{IN} = 3.6 V, V_{OUT} = 1.8 V, I_{OUT} = 200 mA, PWM mode		90%		
		V_{IN} = 3.9 V, V_{OUT} = 3.3 V, I_{OUT} = 500 mA, PWM mode		95%		
$LINE_{TR}$	Line transient response	V_{IN} = 3.6 V to 4.2 V, T_R = T_F = 10 µs, I_{OUT} = 100 mA, V_{OUT} = 0.8 V		50		mVpk
$LOAD_{TR}$	Load transient response	V_{IN} = 3.1 V/3.6 V/4.5 V, V_{OUT} = 0.8 V, I_{OUT} = 50 mA to 150 mA, T_R = T_F = 0.1 µs		50		

(1) Linearity limits are ±3% or ±50 mV whichever is larger.

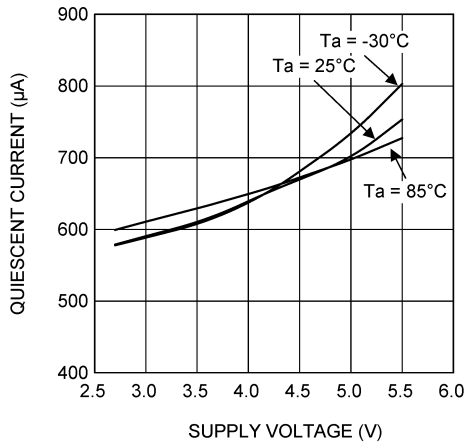
6.7 Typical Characteristics

V_{IN} = EN = 3.6 V and T_A = 25°C, unless otherwise noted.



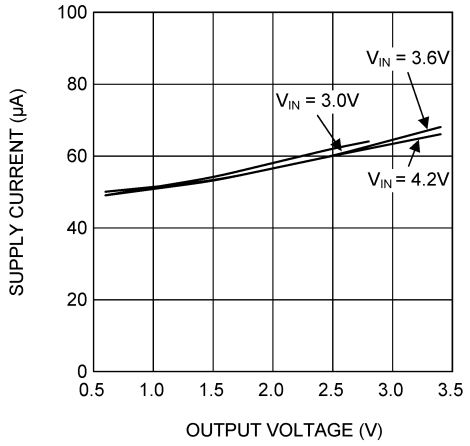
SW = VCON = EN = 0 V

Figure 1. Shutdown Current vs Temperature



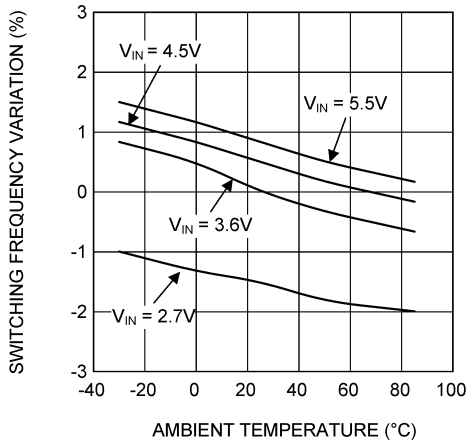
No switching FB = 1 V VCON = 0 V

Figure 2. Quiescent Current vs Supply Voltage



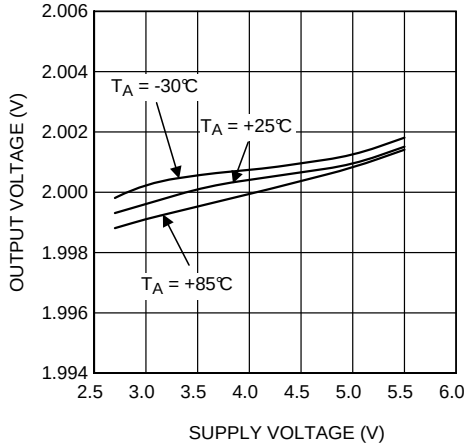
Closed loop Switching No load

Figure 3. Eco-mode Supply Current vs Output Voltage



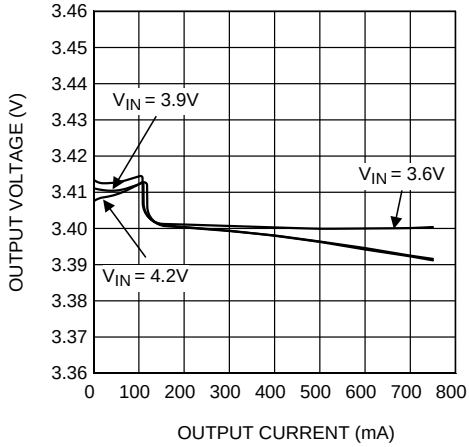
V_{OUT} = 2 V I_{OUT} = 200 mA

Figure 4. Switching Frequency vs Temperature



V_{OUT} = 2 V R_{LOAD} = 10 Ω

Figure 5. Output Voltage vs Supply Voltage

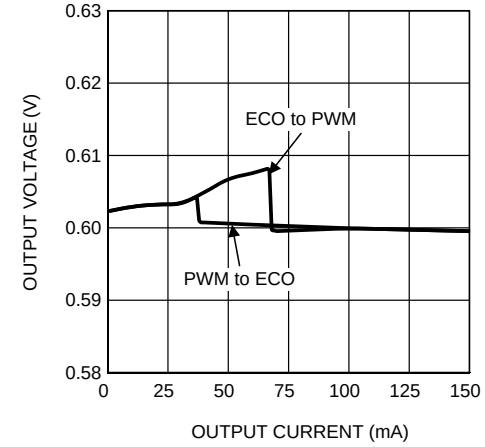


V_{OUT} = 3.4 V

Figure 6. Output Voltage vs Output Current

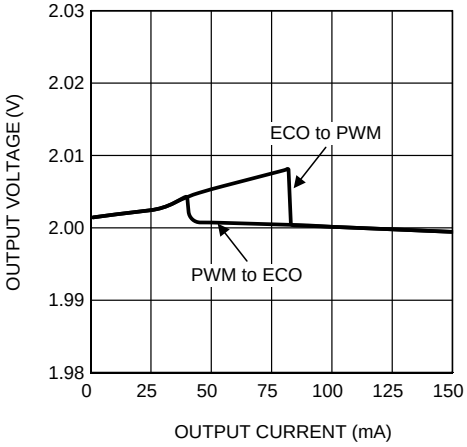
Typical Characteristics (continued)

V_{IN} = EN = 3.6 V and T_A = 25°C, unless otherwise noted.



V_{OUT} = 0.6 V

Figure 7. Output Voltage vs Output Current



V_{OUT} = 2 V

Figure 8. Output Voltage vs Output Current

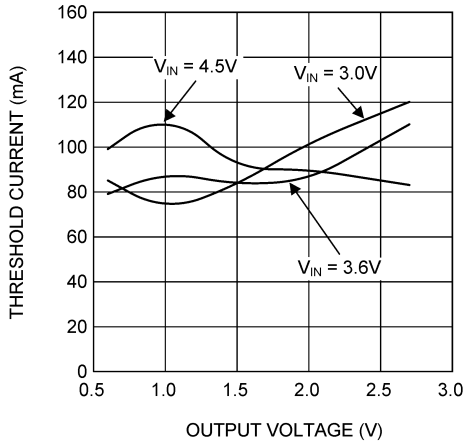


Figure 9. ECO-PWM Mode Threshold Current vs Output voltage

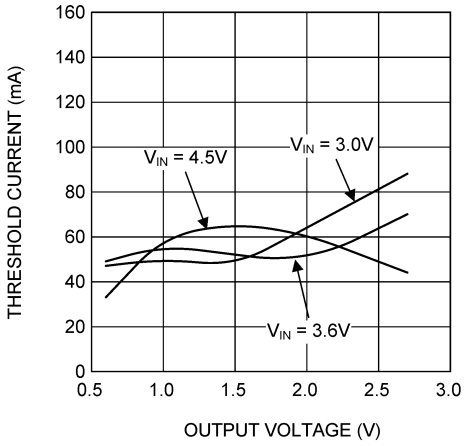
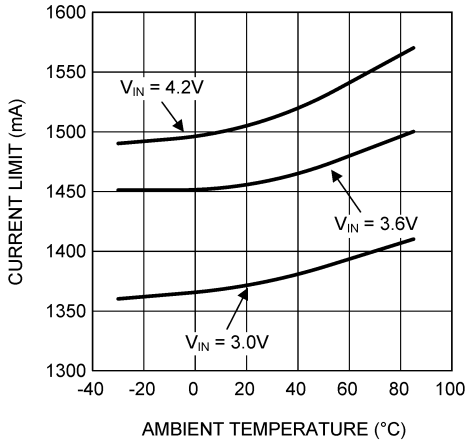
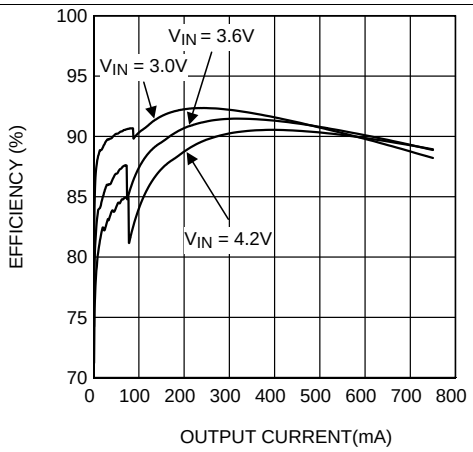


Figure 10. PWM-Eco-Mode Threshold Current vs Output voltage



V_{OUT} = 2 V

Figure 11. Closed-loop Current Limit vs Temperature

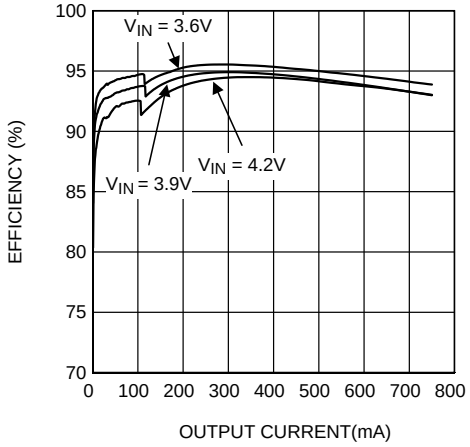


V_{OUT} = 2 V

Figure 12. Efficiency vs Output Current

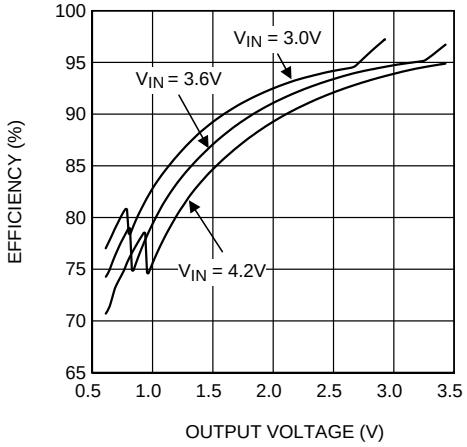
Typical Characteristics (continued)

V_{IN} = EN = 3.6 V and T_A = 25°C, unless otherwise noted.



V_{OUT} = 3.3 V

Figure 13. Efficiency vs Output Current



R_{LOAD} = 10 Ω

Figure 14. Efficiency vs Output Voltage

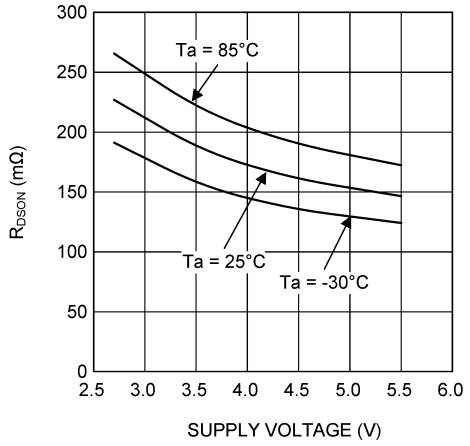


Figure 15. PFET R_{DSON} vs Supply Voltage

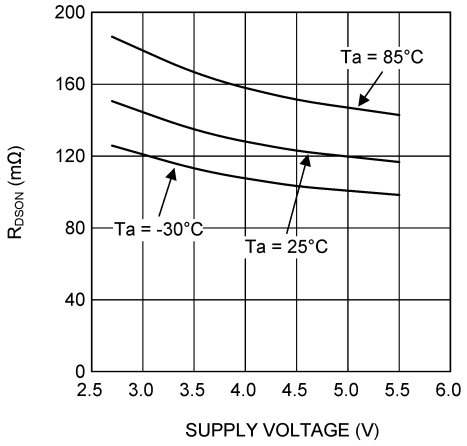
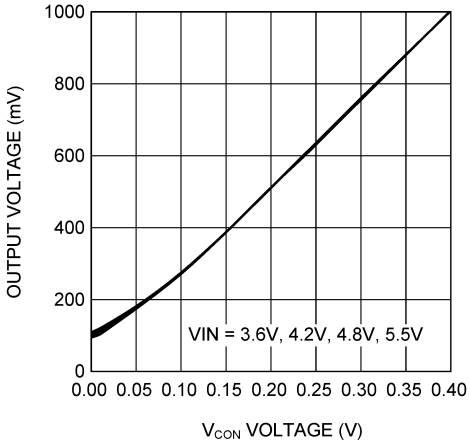
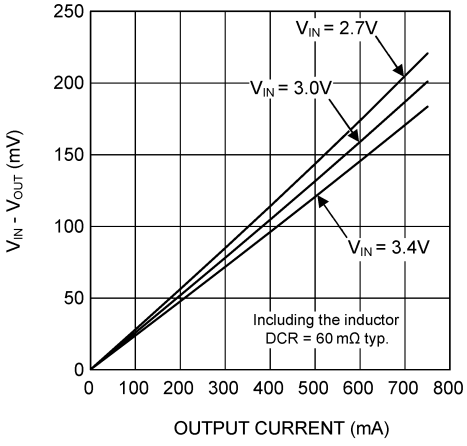


Figure 16. NFET R_{DSON} vs Supply Voltage



R_{LOAD} = 10 Ω

Figure 17. Low VCON Voltage vs Output Voltage



100% Duty Cycle

Figure 18. V_{IN}-V_{OUT} vs Output Current

Typical Characteristics (continued)

V_{IN} = EN = 3.6 V and T_A = 25°C, unless otherwise noted.

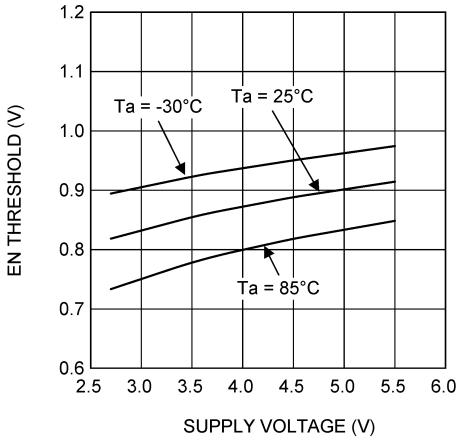
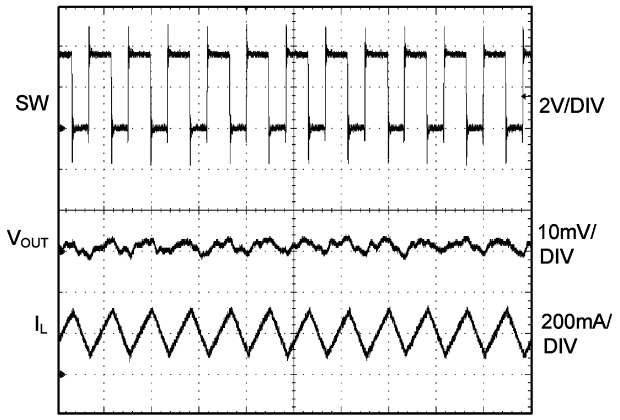
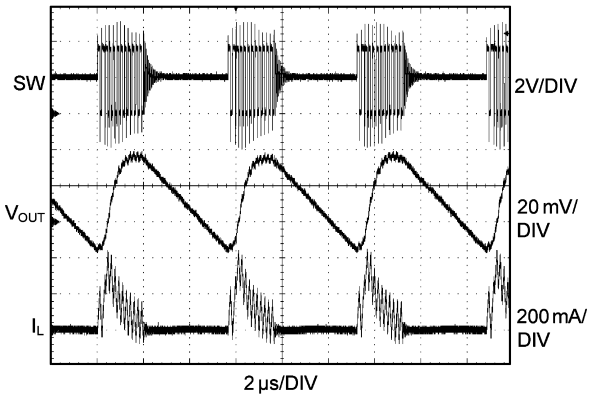


Figure 19. EN High Threshold vs Supply Voltage



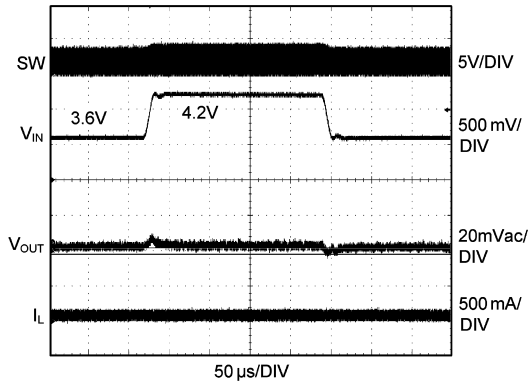
V_{OUT} = 2 V I_{OUT} = 200 mA

Figure 20. Output Voltage Ripple in PWM Mode



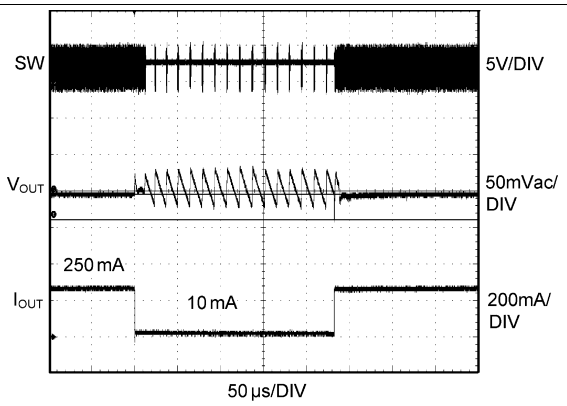
V_{OUT} = 2 V I_{OUT} = 50 mA

Figure 21. Output Voltage Ripple in Eco-Mode



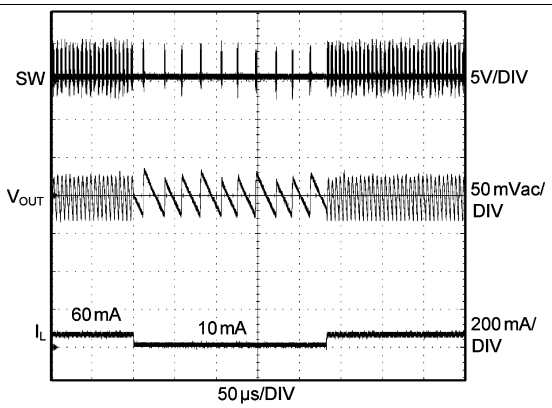
V_{IN} = 3.6 V/4.2 V V_{OUT} = 0.8 V R_{LOAD} = 8 Ω

Figure 22. Line Transient Response



V_{OUT} = 2.5 V I_{OUT} = 10 mA/250 mA

Figure 23. Load Transient Response

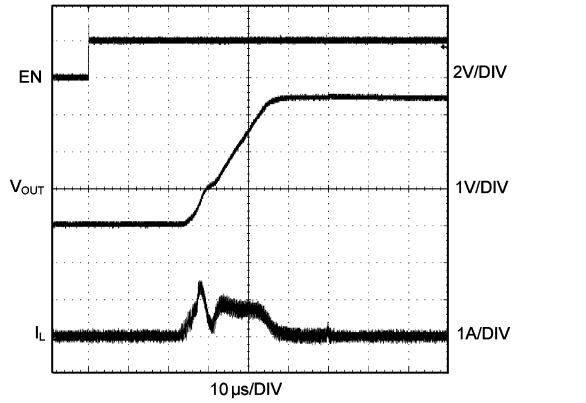


V_{OUT} = 0.6 V I_{OUT} = 10 mA/60 mA

Figure 24. Load Transient Response

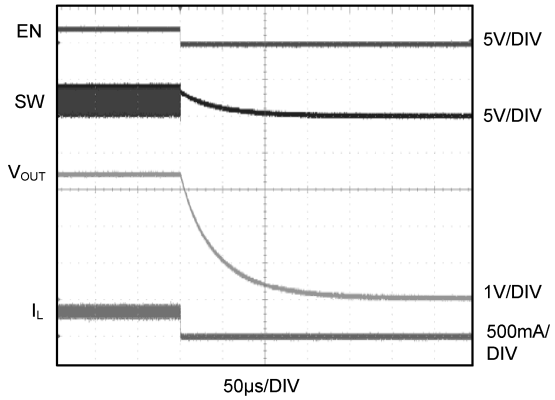
Typical Characteristics (continued)

V_{IN} = EN = 3.6 V and T_A = 25°C, unless otherwise noted.



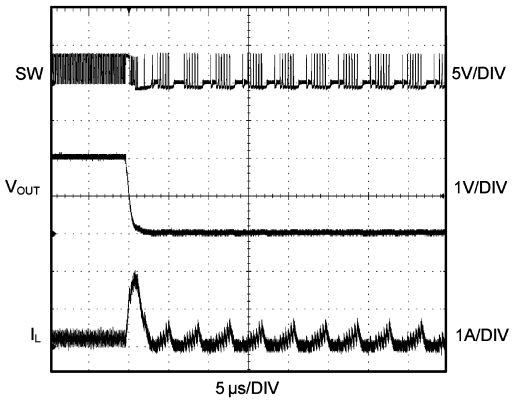
V_{IN} = 4.2 V V_{OUT} = 3.4 V R_{LOAD} = 3.6 kΩ

Figure 25. Startup



V_{IN} = 4.2 V V_{OUT} = 3.4 V R_{LOAD} = 10 kΩ

Figure 26. Shutdown



V_{OUT} = 2 V R_{LOAD} = 10 Ω

Figure 27. Timed Current Limit

7 Detailed Description

7.1 Overview

The LM3241 is a simple, step-down DC-DC converter optimized for powering RF power amplifiers (PAs) in mobile phones, portable communicators, and similar battery-powered RF devices. The device is designed to allow the RF PA to operate at maximum efficiency over a wide range of power levels from a single Li-Ion battery cell. The design is based on a voltage-mode buck architecture, with synchronous rectification for high efficiency. The device is designed for a maximum load capability of 750 mA in PWM mode. Maximum load range may vary from this depending on input voltage, output voltage, and the inductor chosen.

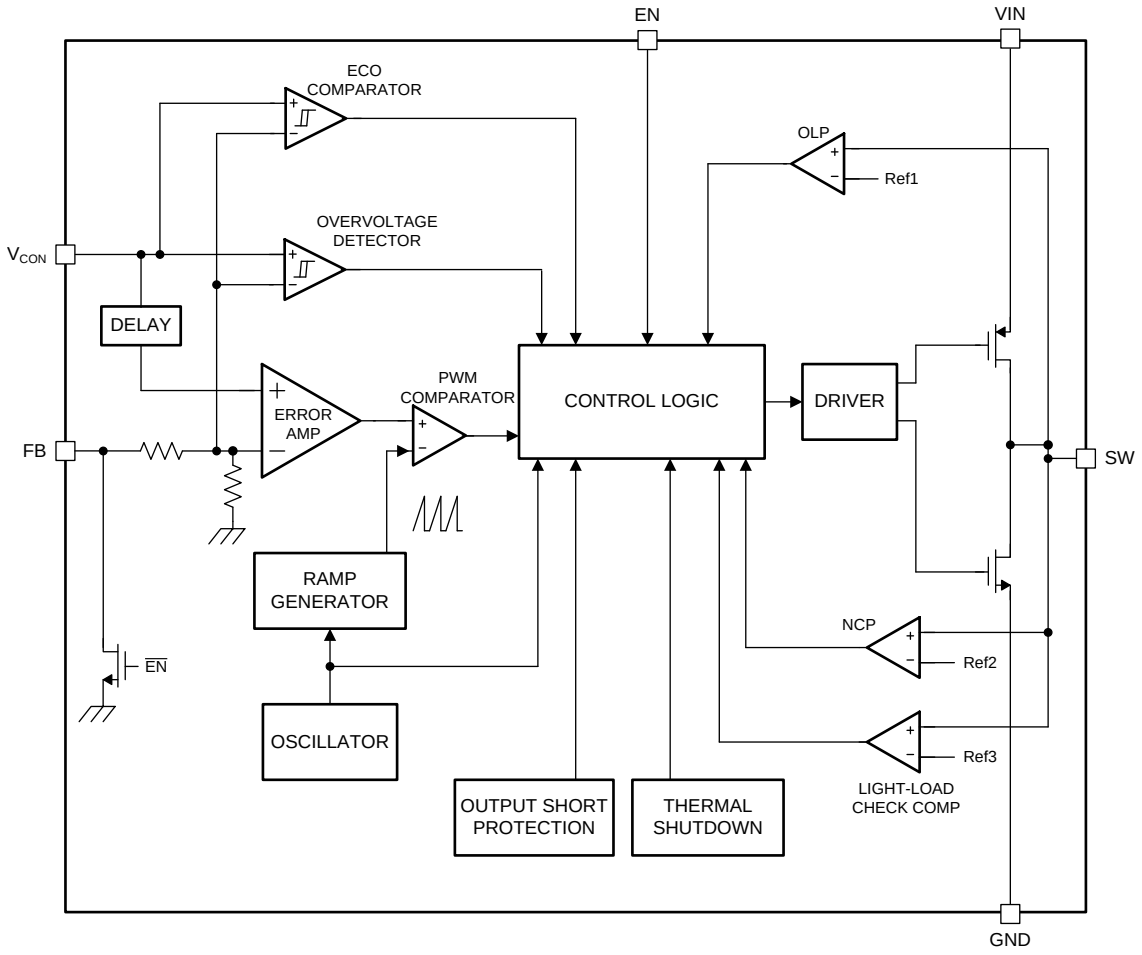
Three modes of operation are available depending on the current required: pulse width modulation (PWM), Eco-mode (economy mode), and shutdown. The LM3241 operates in PWM mode at higher load-current conditions. Lighter loads cause the device to automatically switch into Eco-mode. Shutdown mode turns off the device and reduces battery consumption to 0.1 µA (typical).

Precision of the DC PWM-mode output voltage is ±2% for 3.4 V_{OUT}. Efficiency is around 95% (typical) for a 500-mA load with a 3.3-V output and 3.9-V input. The output voltage is dynamically programmable from 0.6 V to 3.4 V by adjusting the voltage on the control pin (VCON) without the need for external feedback resistors. This feature ensures longer battery life by being able to change the PA supply voltage dynamically depending on its transmitting power.

Additional features include current overload protection and thermal overload shutdown.

The LM3241 is constructed using a chip-scale, 6-bump DSBGA package. This package offers the smallest possible size for space-critical applications, such as cell phones, where board area is an important design consideration. Use of a high switching frequency (6 MHz, typical) reduces the size of external components. As shown in Figure 29, only three external power components are required for implementation. Use of a DSBGA package requires special design considerations for implementation (for more information see the *DSBGA Package Assembly and Use* section.) The fine-bump pitch of the package requires careful board design and precision assembly equipment. Use of this package is best suited for opaque-case applications, where its edges are not subject to high-intensity ambient red or infrared light. Also, the system controller should set EN low during power-up and other low supply voltage conditions (see the *Shutdown Mode* section).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Circuit Operation

Referring to Figure 29 and the *Functional Block Diagram*, the LM3241 operates as follows. During the first part of each switching cycle, the control block in the LM3241 turns on the internal, top-side PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of around (V_{IN} – V_{OUT}) / L, by storing energy in a magnetic field. During the second part of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the bottom-side NFET synchronous rectifier on. In response, the magnetic field of the inductor collapses, generating a voltage that forces current from ground through the synchronous rectifier to the output filter capacitor and load. As the stored energy is transferred back into the circuit and depleted, the inductor current ramps down with a slope around V_{OUT} / L. The output filter capacitor stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch-on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at SW to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

Feature Description (continued)

7.3.2 Internal Synchronization Rectification

While in PWM mode, the LM3241 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

With medium and heavy loads, the NFET synchronous rectifier is turned on during the inductor current-down slope in the second part of each cycle. The synchronous rectifier is turned off prior to the next cycle. The NFET is designed to conduct through its intrinsic body diode during transient intervals before it turns on, eliminating the need for an external diode.

7.3.3 Current Limiting

The current limit feature allows the LM3241 to protect itself and external components during overload conditions. In PWM mode, the cycle-by-cycle current limit is 1450 mA (typical). If an excessive load pulls the output voltage down to less than 0.3 V (typical), the NFET synchronous rectifier is disabled, and the current limit is reduced to 530 mA (typical). Moreover, when the output voltage becomes less than 0.15 V (typical), the switching frequency decreases to 3 MHz, thereby preventing excess current and thermal stress.

7.3.4 Dynamically Adjustable Output Voltage

The LM3241 features dynamically adjustable output voltage to eliminate the need for external feedback resistors. The output voltage can be set from 0.6 V to 3.4 V by changing the voltage on the analog VCON pin. This feature is useful in PA applications where peak power is needed only when the handset is far away from the base station or when data is being transmitted. In other instances the transmitting power can be reduced. Therefore the supply voltage to the PA can be reduced, promoting longer battery life. For more information, see the *Setting the Output Voltage* in the *Application and Implementation* section. The LM3241 moves into Pulse Skipping mode when the duty cycle is over approximately 92% or less than approximately 15%, and the output voltage ripple increases slightly.

7.3.5 Thermal Overload Protection

The LM3241 has a thermal overload protection function that operates to protect itself from short-term misuse and overload conditions. When the junction temperature exceeds around 150°C, the device inhibits operation. Both the PFET and the NFET are turned off. When the temperature drops below 125°C, normal operation resumes. Prolonged operation in thermal overload conditions may damage the device and is considered bad practice.

7.3.6 Soft Start

The LM3241 has a soft-start circuit that limits in-rush current during startup. During startup the switch current limit is increased in steps. Soft start is activated if EN goes from low to high after V_{IN} reaches 2.7 V.

7.4 Device Functional Modes

7.4.1 PWM Mode Operation

While in PWM mode operation, the converter operates as a voltage-mode controller with input voltage feed forward. This operation allows the converter to achieve excellent load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward inversely proportional to the input voltage is introduced. While in PWM mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current-limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. Then the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.

7.4.2 Eco-mode™ Operation

At very light loads (50 mA to 100 mA), the LM3241 enters Eco-mode operation with reduced switching frequency and supply current to maintain high efficiency. During Eco-mode operation, the LM3241 positions the output voltage slightly higher (+7 mV typical) than the normal output voltage during PWM mode operation, allowing additional headroom for voltage drop during a load transient from light to heavy load.

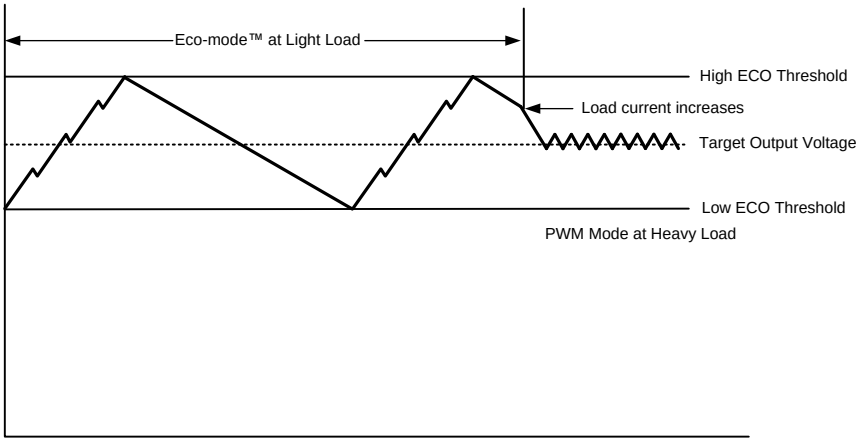


Figure 28. Operation in Eco-mode and Transfer to PWM Mode

7.4.3 Shutdown Mode

Setting the EN digital pin low (<0.4 V) places the LM3241 in shutdown mode (0.1 µA typical). During shutdown, the PFET switch, the NFET synchronous rectifier, reference voltage source, control and bias circuitry of the LM3241 are turned off. Setting the EN pin high (>1.2 V) enables normal operation. The EN pin should be set low to turn off the LM3241 during power-up and undervoltage conditions when the power supply is less than the 2.7-V minimum operating voltage. The LM3241 has an undervoltage-lockout (UVLO) comparator to turn off the power device in the case the input voltage or battery voltage is too low. The typical UVLO threshold is around 2.0 V for lock and 2.1 V for release.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM3241 is a synchronous step-down converter in which output voltage is adjusted by a controlled voltage. The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Application

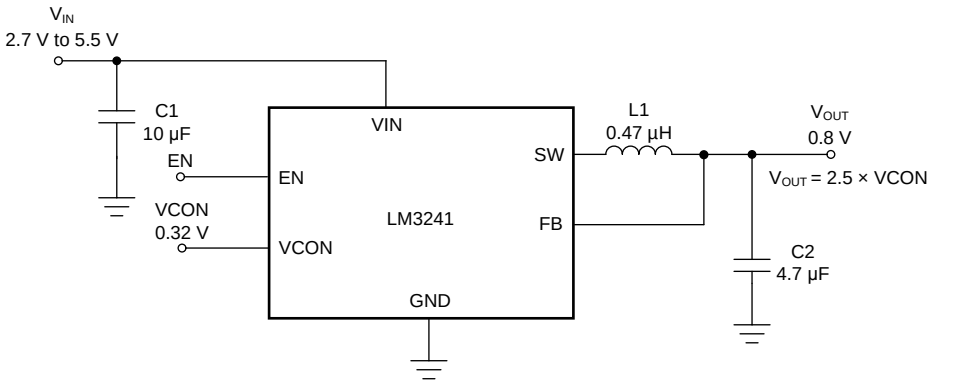


Figure 29. LM3241 Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.7 V to 5.5 V
Output voltage	0.8 V
Maximum current	750 mA

8.2.2 Detailed Design Procedure

Table 2 lists the component descriptions for Figure 29.

Table 2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
C1	10 µF, Ceramic capacitor, 6.3 V, X5R, size 0603, GRM188R60J106ME47D	Murata
C2	4.7 µF, Ceramic capacitor, 6.3 V, X5R, size 0603, GRM188R71H472KA01D	Murata
L1	0.47 µH, Fixed Inductor, 1.6 A, size 0806, LQM2MPNR47NG0L	Murata

8.2.2.1 Setting the Output Voltage

The LM3241 features a pin-controlled adjustable output voltage to eliminate the need for external feedback resistors. The output voltage can be programmed for an output voltage from 0.6 V to 3.4 V by setting the voltage on the VCON pin, as shown in Equation 1.

$$V_{OUT} = 2.5 \times VCON \quad (1)$$

When the VCON voltage is between 0.24 V and 1.36 V, the output voltage follows proportionally by 2.5 times of VCON.

If the VCON voltage is less than 0.24 V (V_{OUT} = 0.6 V), the output voltage may be regulated (for details see Figure 17). Figure 17 exhibits the characteristics of a typical part, and the performance cannot be ensured as a part-to-part variation could occur for output voltages less than 0.6 V. For V_{OUT} lower than 0.6 V, the converter could suffer from larger output ripple voltage and higher current limit operation.

8.2.2.2 Inductor Selection

Two main considerations must be considered when choosing an inductor: the inductor should not saturate, and the inductor current ripple should be small enough to achieve the desired output voltage ripple. Different manufacturers follow different saturation current rating specifications, so attention must be given to details. Saturation current ratings are typically specified at 25°C so ratings over the ambient temperature of application should be requested from manufacturer.

The minimum value of inductance to ensure good performance is 0.3 µH at bias current (I_{LIM}, typical) over the ambient temperature range. Shielded inductors radiate less noise and should be preferred. Two methods are avaialble to choose the inductor saturation current rating.

8.2.2.2.1 Method 1

The saturation current should be greater than the sum of the maximum load current and the worst case average to peak inductor current. Use Equation 2 to find the saturation current (I_{SAT}).

$$I_{SAT} > I_{OUT\_MAX} + I_{RIPPLE}$$

where

- I_{OUT_MAX} is the maximum load current (750 mA).
- I_{RIPPLE} is the average-to-peak inductor current. Use Equation 3 to calculate the I_{RIPPLE} value. (2)

$$I_{RIPPLE} = \left(\frac{V_{IN} - V_{OUT}}{2 \times L}\right) \times \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{f}\right)$$

where

- V_{IN} is the maximum input voltage in application.
- V_{OUT} is the output voltage
- L is the minimum inductor value including worst-case tolerances (30% drop can be considered for Method 1)
- f is the minimum switching frequency (5.7 MHz) (3)

8.2.2.2.2 Method 2

A more conservative and recommended approach is to choose an inductor that can support the maximum current limit of 1600 mA.

The resistance of the inductor should be less than approximately 0.1 Ω for good efficiency. Table 3 lists recommended inductors and suppliers.

Table 3. Recommended Inductors

Model	Size (W x L x H) (mm)	Vendor
MIPSZ2012D0R5	2.0 x 1.2 x 1.0	FDK
LQM21PNR54MG0	2.0 x 1.25 x 0.9	Murata
LQM2MPNR47NG0	2.0 x 1.6 x 0.9	Murata

8.2.2.3 Capacitor Selection

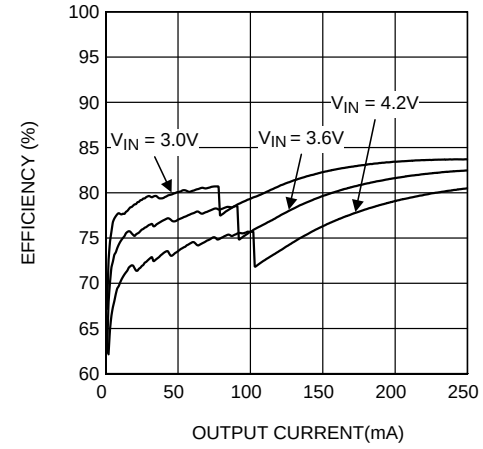
The LM3241 is designed for use with ceramic capacitors for its input and output filters. Use a 10-µF ceramic capacitor for the input and a 4.7-µF ceramic capacitor for the output. The capacitors should maintain at least 50% capacitance at DC bias and temperature conditions. Ceramic capacitors type such as X5R, X7R, and B are recommended for both filters. These types provide an optimal balance between small size, cost, reliability, and performance for cell phones and similar applications. Table 4 lists some recommended part numbers and suppliers. DC bias characteristics of the capacitors must be considered when selecting the voltage rating and case size of the capacitor. For C_{IN}, use of an 0805 (2012) size may also be considered if room is available on the system board.

Table 4. Recommended Capacitors

Capacitance, Voltage Rating, Case Size	Model	Vendor
4.7 µF, 6.3 V, 0603	C1608X5R0J475M	TDK
4.7 µF, 6.3 V, 0402	C1005X5R0J475M	TDK
4.7 µF, 6.3 V, 0402	CL05A475MQ5NRNC	Samsung
10 µF, 6.3 V, 0603	C1608X5R0J106M	TDK
10 µF, 6.3 V, 0402	CL05A106MQ5NUNC	Samsung

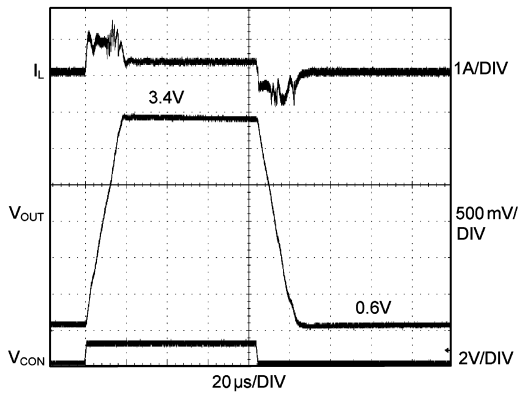
The input filter capacitor supplies AC current drawn by the PFET switch of the LM3241 in the first part of each cycle and reduces the voltage ripple imposed on the input power source. The output filter capacitor absorbs the AC inductor current, helps maintain a steady output voltage during transient load changes, and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low equivalent series resistance (ESR) to perform these functions. The ESR of the filter capacitors is generally a major factor in voltage ripple.

8.2.3 Application Curves



V_{OUT} = 0.8 V

Figure 30. Efficiency vs Output Current



V_{OUT} = 0.6 V/3.4 V R_{LOAD} = 10 Ω

Figure 31. VCON Transient Response

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.7 V to 5.5 V. Ensure that the input power supply has a sufficient current rating for the application.

10 Layout

10.1 Layout Guidelines

10.1.1 DSBGA Package Assembly and Use

Use of the DSBGA package requires specialized board layout, precision mounting and careful reflow techniques, as detailed in the *AN-1112 DSBGA Wafer Level Chip Scale Package* application report. For best results in assembly, alignment ordinals on the PC board should be used to facilitate placement of the device. The pad style used with DSBGA package must be the non-solder mask defined (NSMD) type. This pad type means that the solder-mask opening is larger than the pad size which prevents a lip that otherwise forms if the solder-mask and pad overlap when holding the device off the surface of the board causing interference with mounting. For specific instructions on how to do this, refer to the *AN-1112 DSBGA Wafer Level Chip Scale Package* application report.

The 6-bump package used for LM3241 has 300 micron solder balls and requires 10.82 mil pads for mounting on the circuit board. The trace to each pad should enter the pad with a 90° angle to prevent debris from being caught in deep corners. Initially, the trace to each pad should be 7 mil wide, for a section approximately 7 mil long, as a thermal relief. Then each trace should neck up or down to its optimal width. The important criterion is symmetry which ensures the solder bumps on the LM3241 reflow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps A2 and C2. Because the VIN and GND pins are typically connected to large copper planes, inadequate thermal relief can result in late or inadequate reflow of these bumps.

The DSBGA package is optimized for the smallest possible size in applications with red or infrared opaque cases. Because the DSBGA package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metallization and/or epoxy coating, along with front-side shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges. In particular, DSBGA devices are sensitive to light in the red and infrared range shining on the exposed die edges of the package.

TI recommends connecting a 10-nF capacitor between the VCON pin and ground for non-standard ESD events or environments and manufacturing processes. This capacitor prevents unexpected output voltage drift.

10.1.2 Board Layout Considerations

Printed-circuit board (PCB) layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These factors can send erroneous signals to the DC-DC converter device, resulting in poor regulation or instability. Poor layout can also result in reflow problems leading to poor solder joints between the DSBGA package and board pads—poor solder joints can result in erratic or degraded performance. Good layout for the LM3241 can be implemented by following a few simple design rules, as shown in Figure 33.

1. Place the LM3241 on 10.82 mil pads. As a thermal relief, connect each pad with a 7mil wide, approximately 7mil long trace, and then incrementally increase each trace to its optimal width. The V_{IN} and GND traces are especially recommended to be as wide as possible. The important criterion is symmetry to ensure the solder bumps reflow evenly (refer to the *AN-1112 DSBGA Wafer Level Chip Scale Package* application report).
2. Place the LM3241, inductor, and filter capacitors close together and make the traces short. The traces between these components carry relatively high switching current and act as antennae. Following this rule reduces radiated noise. **Special care must be given to place the input filter capacitor very close to the VIN and GND pads.**
3. Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor, through the LM3241 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground, through the LM3241 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.

Layout Guidelines (continued)

4. Connect the ground pads of the LM3241 and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then connect this to the ground-plane (if one is used) with several vias. This connection reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LM3241 by giving it a low impedance ground connection.
5. Use side traces between the power components and for power connections to the DC-DC converter circuit which reduces voltage errors caused by resistive losses across the traces.
6. Route noise sensitive traces such as the voltage feedback path away from noisy traces between the power components. The output voltage feedback point should be taken approximately 1.5 nH away from the output capacitor. The feedback trace also should be routed opposite to noise components. **The voltage feedback trace must remain close to the LM3241 circuit and should be routed directly from FB to VOUT at the inductor and should be routed opposite to noise components**. This trace placement allows fast feedback and reduces EMI radiated onto the voltage feedback trace of the DC-DC converter (see Figure 32).

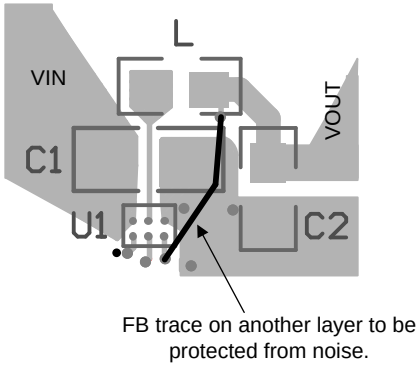


Figure 32. Feedback Trace

7. Place noise-sensitive circuitry, such as radio IF blocks, away from the DC-DC converter, CMOS digital blocks, and other noisy circuitry. Interference with noise-sensitive circuitry in the system can be reduce through distance.

In mobile phones, for example, a common practice is to place the DC-DC converter on one corner of the board, arrange the CMOS digital circuitry around it (because this also generates noise), and then place sensitive preamplifiers and IF stages on the diagonally opposing corner. Often, the sensitive circuitry is shielded with a metal pan and power to it is post-regulated to reduce conducted noise, using low-dropout linear regulators.

10.2 Layout Example

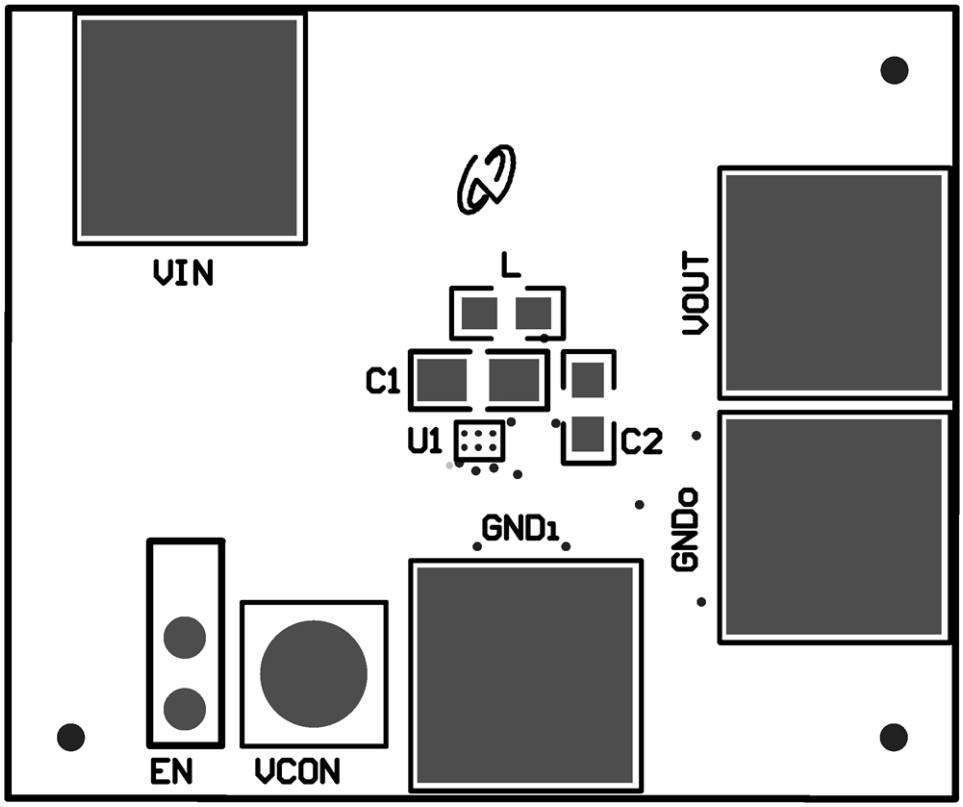


Figure 33. LM3241 Board Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:
Texas Instruments, *AN-1112 DSBGA Wafer Level Chip Scale Package* application report

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

Eco-mode, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3241TLE/NOPB	ACTIVE	DSBGA	YZR	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	H	Samples
LM3241TLX/NOPB	ACTIVE	DSBGA	YZR	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	H	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

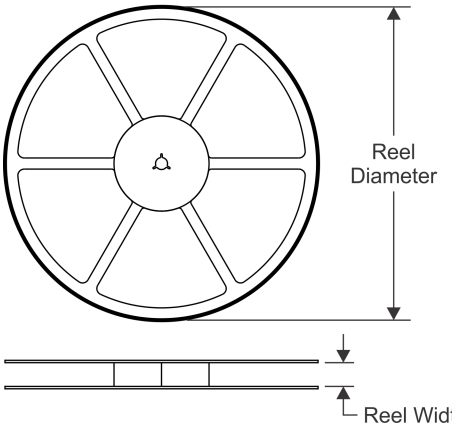
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

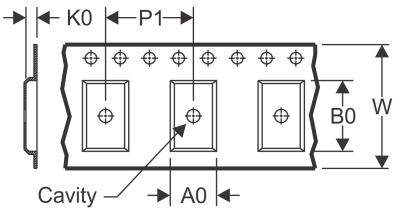
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

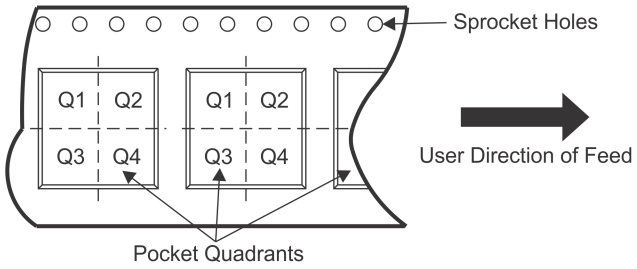


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

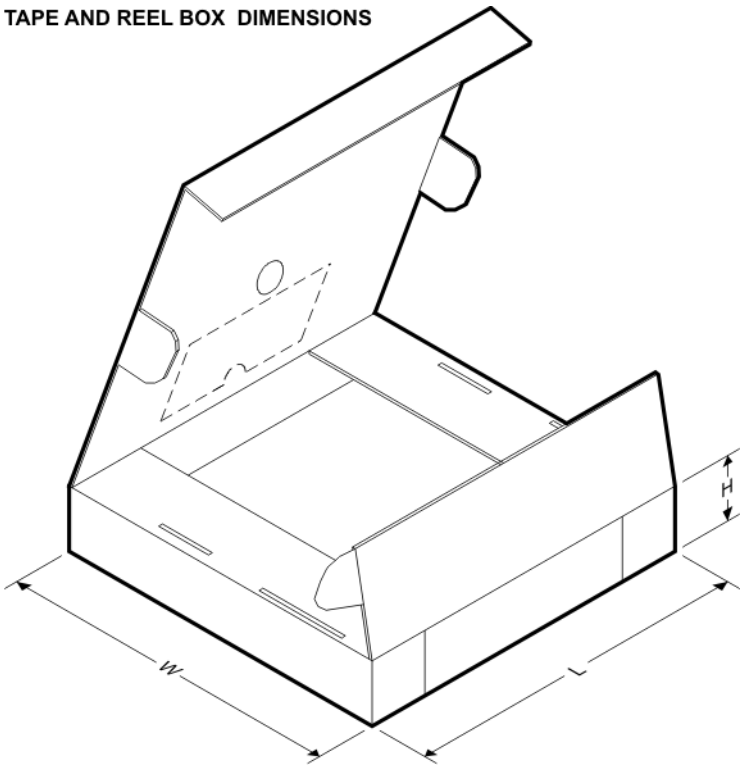
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3241TLE/NOPB	DSBGA	YZR	6	250	178.0	8.4	1.24	1.7	0.76	4.0	8.0	Q1
LM3241TLX/NOPB	DSBGA	YZR	6	3000	178.0	8.4	1.24	1.7	0.76	4.0	8.0	Q1

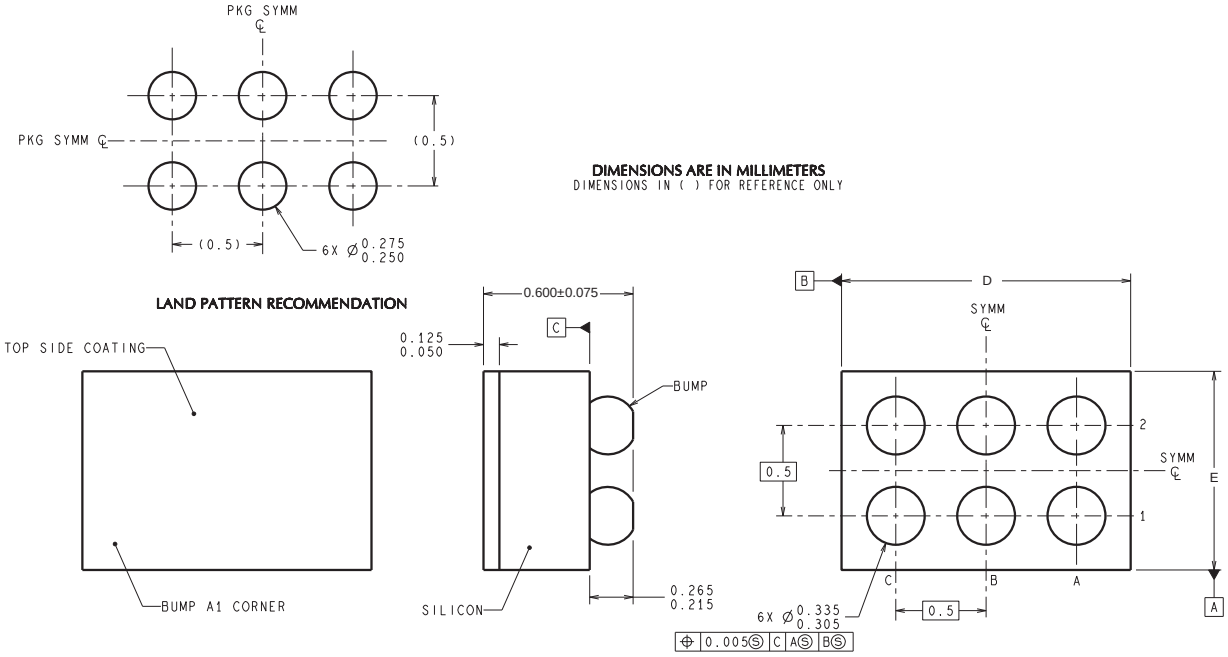
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3241TLE/NOPB	DSBGA	YZR	6	250	210.0	185.0	35.0
LM3241TLX/NOPB	DSBGA	YZR	6	3000	210.0	185.0	35.0

YZR0006



TLA06XXX (Rev C)

D: Max = 1.51 mm, Min = 1.45 mm

E: Max = 1.12 mm, Min = 1.06 mm

4215044/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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