



**THE DATASHEET OF  
LM3480IM3-5.0**





## LM3480 100-mA, SOT-23, Quasi Low-Dropout Linear Voltage Regulator

### 1 Features

- Input Voltage Range: up to 30 V
- 3.3-V, 5-V, 12-V, and 15-V Versions Available
- Packaged in the Tiny 3-Lead SOT-23 Package
- 30-V Maximum Input for Operation
- 1.2-V Ensured Maximum Dropout Over Full Load and Temperature Ranges
- 100-mA Ensured Minimum Load Current
- $\pm 5\%$  Ensured Output Voltage Tolerance Over Full Load and Temperature Ranges
- $-40$  to  $+125^\circ\text{C}$  Junction Temperature Range for Operation

### 2 Applications

- Tiny Alternative to LM78Lxx Series and Similar Devices
- Tiny 5-V  $\pm 5\%$  to 3.3-V, 100-mA Converter
- Post Regulator for Switching DC/DC Converter
- Bias Supply for Analog Circuits

### 3 Description

The LM3480 is an integrated linear voltage regulator. It features operation from an input as high as 30 V and an ensured maximum dropout of 1.2 V at the full 100-mA load. Standard packaging for the LM3480 is the 3-lead SOT-23 package.

The 5-V, 12-V, and 15-V members of the LM3480 series are intended as tiny alternatives to industry standard LM78Lxx series and similar devices. The 1.2-V quasi-low dropout of LM3480 series devices makes them a nice fit in many applications where the 2-V to 2.5-V dropout of LM78Lxx series devices precludes their (LM78Lxx series devices) use.

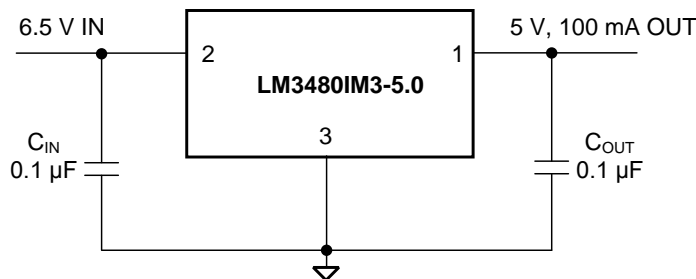
The LM3480 series also features a 3.3-V member. The SOT-23 packaging and quasi-low dropout features of the LM3480 series converge in this device to provide a very nice, very tiny, 3.3-V, 100-mA bias supply that regulates directly off the system 5-V  $\pm 5\%$  power supply.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM3480	SOT-23 (3)	2.92 mm x 1.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Typical Application Circuit



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision G (February 2015) to Revision H</b>	<b>Page</b>
• Replaced <i>Functional Block Diagram</i> .....	<b>10</b>
• Changed text of <i>External Capacitors</i> subsection .....	<b>11</b>
• Changed text of <i>Output Capacitor</i> subsection .....	<b>11</b>

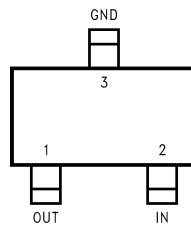
<b>Changes from Revision F (December 2014) to Revision G</b>	<b>Page</b>
• Changed pin numbers indicated in <i>Typical Application</i> drawing; fix typos.....	<b>1</b>
• Deleted soldering specs - found in POA .....	<b>4</b>
• Changed <i>Handling Ratings</i> to <i>ESD Ratings</i> format .....	<b>4</b>

<b>Changes from Revision E (March 2013) to Revision F</b>	<b>Page</b>
• Added <i>Pin Configuration and Functions</i> section, <i>Handling Rating</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section; add updated <i>Thermal Information</i> .....	<b>1</b>

<b>Changes from Revision D (March 2013) to Revision E</b>	<b>Page</b>
• Changed layout of National Data Sheet to TI format .....	<b>9</b>

## 5 Pin Configuration and Functions

**DBZ Package  
3-Pin SOT-23  
Top View**



**Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT	1	O	Output voltage
IN	2	I	Input voltage supply
GND	3	—	Common ground

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)(2)</sup>

	MIN	MAX	UNIT
Input voltage (IN to GND)	-0.3	35	V
Power dissipation <sup>(3)</sup>		Internally Limited	
Junction temperature <sup>(3)</sup>	-40	150	°C
Storage temperature, T <sub>stg</sub>	-65	150	°C

- (1) *Absolute Maximum Ratings* are limits beyond which damage to the device may occur. *Recommended Operating Conditions* are conditions under which operation of the device is ensured. Recommended operating ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the [Electrical Characteristics: LM3480-3.3, LM3480-5](#).
- (2) If Military- or Aerospace-specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (3) The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using  $P = (T_J - T_A) / R_{\theta JA}$  where  $T_J$  is the junction temperature,  $T_A$  is the ambient temperature, and  $R_{\theta JA}$  is the junction-to-ambient thermal resistance. The 370-mW rating results from substituting the Absolute Maximum junction temperature, 150°C for  $T_J$ , 50°C for  $T_A$ , and 269.6°C/W for  $R_{\theta JA}$ . More power can be safely dissipated at lower ambient temperatures. Less power can be safely dissipated at higher ambient temperatures. The Absolute Maximum power dissipation can be increased by 3.7 mW for each °C below 50°C ambient. It must be derated by 3.7 mW for each °C above 50°C ambient. Heat sinking enables the safe dissipation of more power. The LM3480 actively limits its junction temperature to about 150°C.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
Maximum input voltage (IN to GND)	0	30	V
Junction temperature (T <sub>J</sub> )	-40	125	°C

- (1) *Absolute Maximum Ratings* are limits beyond which damage to the device may occur. *Recommended Operating Conditions* are conditions under which operation of the device is ensured. Recommended operating ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the [Electrical Characteristics: LM3480-3.3, LM3480-5](#).

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LM3480	UNIT
		SOT-23 (DBZ)	
		3 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	269.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	141.1	
R <sub>θJB</sub>	Junction-to-board thermal resistance	63.1	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	24.2	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	62.1	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics: LM3480-3.3, LM3480-5

Typical and other limits apply for  $T_A = T_J = 25^\circ\text{C}$ , unless otherwise specified. Nominal output voltage ( $V_{\text{NOM}}$ ) = 3.3 V or 5 V. <sup>(1)(2)(3)</sup>

PARAMETER	TEST CONDITIONS	$V_{\text{NOM}} = 3.3 \text{ V}$			$V_{\text{NOM}} = 5 \text{ V}$			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$V_{\text{OUT}}$ Output voltage	$V_{\text{IN}} = V_{\text{NOM}} + 1.5 \text{ V}$ $1 \text{ mA} \leq I_{\text{OUT}} \leq 100 \text{ mA}$	3.17	3.3	3.43	4.8	5	5.2	V
	$V_{\text{IN}} = V_{\text{NOM}} + 1.5 \text{ V}$ $1 \text{ mA} \leq I_{\text{OUT}} \leq 100 \text{ mA}$ $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	3.14		3.46	4.75		5.25	
$\Delta V_{\text{OUT}}$ Line regulation	$V_{\text{NOM}} + 1.5 \text{ V} \leq V_{\text{IN}} \leq 30 \text{ V}$ $I_{\text{OUT}} = 1 \text{ mA}$		10			12		mV
	$V_{\text{NOM}} + 1.5 \text{ V} \leq V_{\text{IN}} \leq 30 \text{ V}$ $I_{\text{OUT}} = 1 \text{ mA}$ $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$			25			25	
$\Delta V_{\text{OUT}}$ Load regulation	$V_{\text{IN}} = V_{\text{NOM}} + 1.5 \text{ V}$ $10 \text{ mA} \leq I_{\text{OUT}} \leq 100 \text{ mA}$		20			20		mV
	$V_{\text{IN}} = V_{\text{NOM}} + 1.5 \text{ V}$ $10 \text{ mA} \leq I_{\text{OUT}} \leq 100 \text{ mA}$ $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$			40			40	
$I_{\text{GND}}$ Ground pin current	$V_{\text{NOM}} + 1.5 \text{ V} \leq V_{\text{IN}} \leq 30 \text{ V}$ No Load		2			2		mA
	$V_{\text{NOM}} + 1.5 \text{ V} \leq V_{\text{IN}} \leq 30 \text{ V}$ No Load, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$			4			4	
$V_{\text{IN}} - V_{\text{OUT}}$ Dropout voltage	$I_{\text{OUT}} = 10 \text{ mA}$		0.7	0.9		0.7	0.9	V
	$I_{\text{OUT}} = 10 \text{ mA}$ $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$			1			1	
	$I_{\text{OUT}} = 100 \text{ mA}$		0.9	1.1		0.9	1.1	V
	$I_{\text{OUT}} = 100 \text{ mA}$ $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$			1.2			1.2	
$e_n$ Output noise voltage	$V_{\text{IN}} = 10 \text{ V}$ Bandwidth: 10 Hz to 100 kHz		100			150		$\mu\text{V}_{\text{rms}}$

- (1) A typical is the center of characterization data taken with  $T_A = T_J = 25^\circ\text{C}$ . Typical values are not ensured.
- (2) All limits are ensured. All electrical characteristics having room-temperature limits are tested during production with  $T_A = T_J = 25^\circ\text{C}$ . All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
- (3) All voltages except dropout are with respect to the voltage at the GND pin.

## 6.6 Electrical Characteristics: LM3480-12, LM3480-15

Typical and other limits apply for  $T_A = T_J = 25^\circ\text{C}$ , unless otherwise specified. Nominal output voltage ( $V_{\text{NOM}}$ ) = 12 V or 15 V.<sup>(1)(2)(3)</sup>

PARAMETER	TEST CONDITIONS	$V_{\text{NOM}} = 12 \text{ V}$			$V_{\text{NOM}} = 15 \text{ V}$			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$V_{\text{OUT}}$ Output voltage	$V_{\text{IN}} = V_{\text{NOM}} + 1.5 \text{ V}$ $1 \text{ mA} \leq I_{\text{OUT}} \leq 100 \text{ mA}$	11.52	12	12.48	14.4	15	15.6	V
	$V_{\text{IN}} = V_{\text{NOM}} + 1.5 \text{ V}$ $1 \text{ mA} \leq I_{\text{OUT}} \leq 100 \text{ mA}$ $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	11.4		12.6	14.25		15.75	
$\Delta V_{\text{OUT}}$ Line regulation	$V_{\text{NOM}} + 1.5 \text{ V} \leq V_{\text{IN}} \leq 30 \text{ V}$ $I_{\text{OUT}} = 1 \text{ mA}$		14			16		mV
	$V_{\text{NOM}} + 1.5 \text{ V} \leq V_{\text{IN}} \leq 30 \text{ V}$ $I_{\text{OUT}} = 1 \text{ mA}$ $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$			40			40	
$\Delta V_{\text{OUT}}$ Load regulation	$V_{\text{IN}} = V_{\text{NOM}} + 1.5 \text{ V}$ $10 \text{ mA} \leq I_{\text{OUT}} \leq 100 \text{ mA}$		36			45		mV
	$V_{\text{IN}} = V_{\text{NOM}} + 1.5 \text{ V}$ $10 \text{ mA} \leq I_{\text{OUT}} \leq 100 \text{ mA}$ $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$			60			75	
$I_{\text{GND}}$ Ground pin current	$V_{\text{NOM}} + 1.5 \text{ V} \leq V_{\text{IN}} \leq 30 \text{ V}$ No Load		2			2		mA
	$V_{\text{NOM}} + 1.5 \text{ V} \leq V_{\text{IN}} \leq 30 \text{ V}$ No Load, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$			4			4	
$V_{\text{IN}} - V_{\text{OUT}}$ Dropout voltage	$I_{\text{OUT}} = 10 \text{ mA}$		0.7	0.9		0.7	0.9	V
	$I_{\text{OUT}} = 10 \text{ mA}$ , $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$			1			1	
	$I_{\text{OUT}} = 100 \text{ mA}$		0.9	1.1		0.9	1.1	V
	$I_{\text{OUT}} = 100 \text{ mA}$ , $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$			1.2			1.2	
$e_n$ Output noise voltage	$V_{\text{IN}} = 10 \text{ V}$ Bandwidth: 10 Hz to 100 kHz		360			450		$\mu\text{V}_{\text{rms}}$

- (1) A typical is the center of characterization data taken with  $T_A = T_J = 25^\circ\text{C}$ . Typical values are not ensured.
- (2) All limits are ensured. All electrical characteristics having room-temperature limits are tested during production with  $T_A = T_J = 25^\circ\text{C}$ . All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
- (3) All voltages except dropout are with respect to the voltage at the GND pin.

### 6.7 Typical Characteristics

Unless indicated otherwise,  $V_{IN} = V_{NOM} + 1.5\text{ V}$ ,  $C_{IN} = 0.1\ \mu\text{F}$ ,  $C_{OUT} = 0.1\ \mu\text{F}$ , and  $T_A = 25^\circ\text{C}$ .

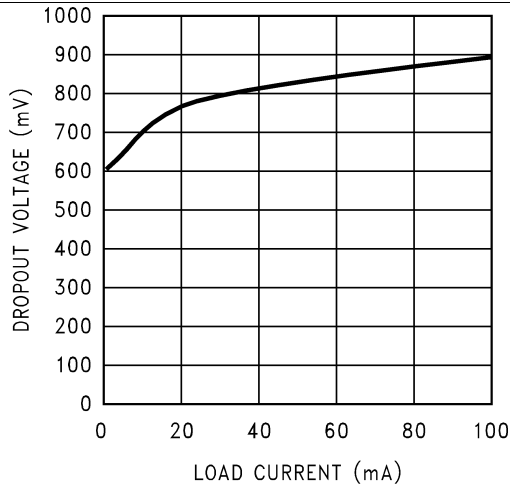


Figure 1. Dropout Voltage vs Load Current

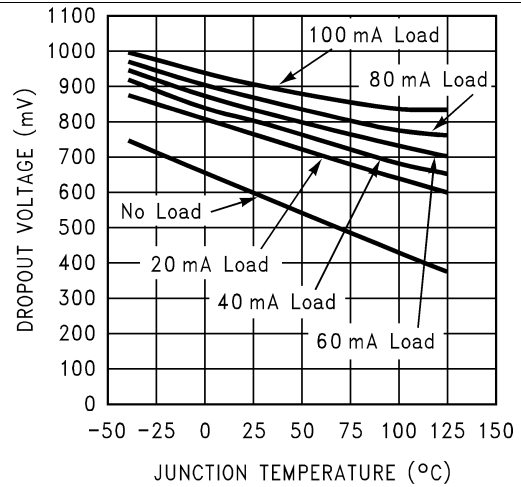


Figure 2. Dropout Voltage vs Junction Temperature

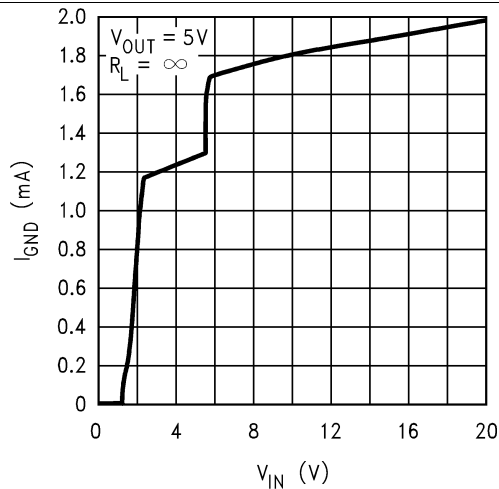


Figure 3. Ground Pin Current vs Input Voltage

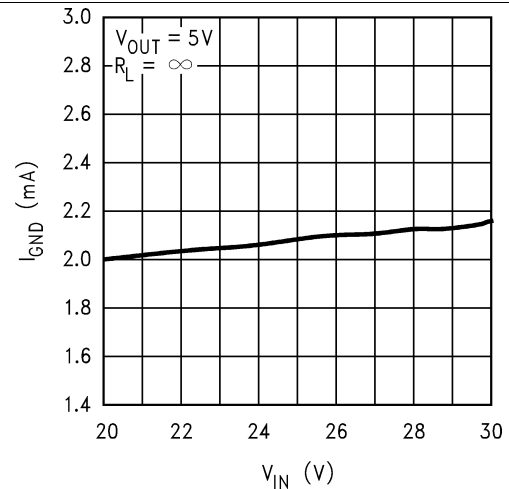


Figure 4. Ground Pin Current vs Input Voltage

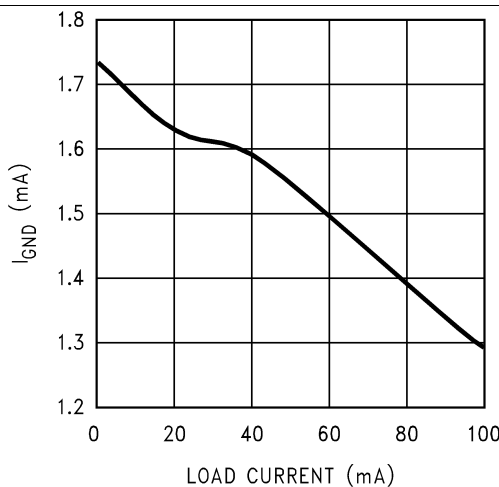


Figure 5. Ground Pin Current vs Load Current

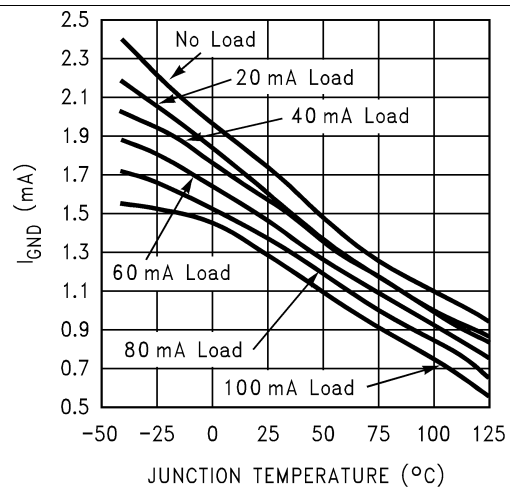


Figure 6. Ground Pin Current vs Junction Temperature

Typical Characteristics (continued)

Unless indicated otherwise,  $V_{IN} = V_{NOM} + 1.5\text{ V}$ ,  $C_{IN} = 0.1\ \mu\text{F}$ ,  $C_{OUT} = 0.1\ \mu\text{F}$ , and  $T_A = 25^\circ\text{C}$ .

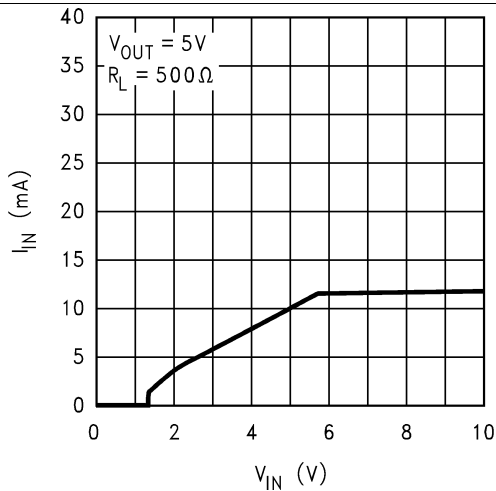


Figure 7. Input Current vs Input Voltage

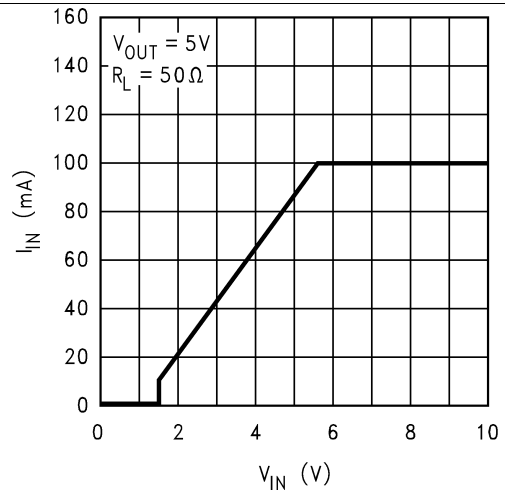


Figure 8. Input Current vs Input Voltage

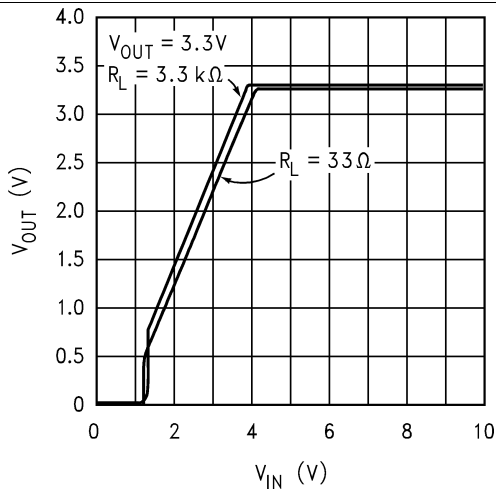


Figure 9. Output Voltage vs Input Voltage

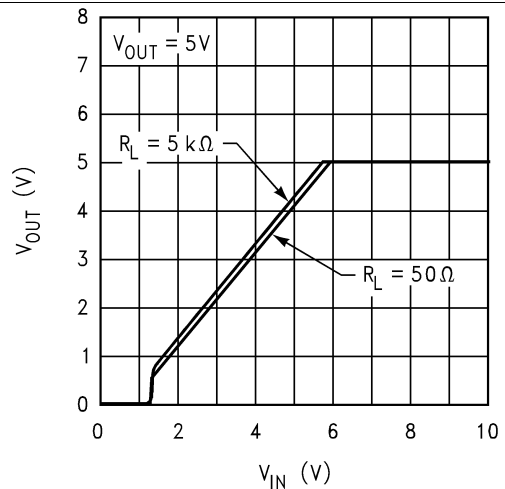


Figure 10. Output Voltage vs Input Voltage

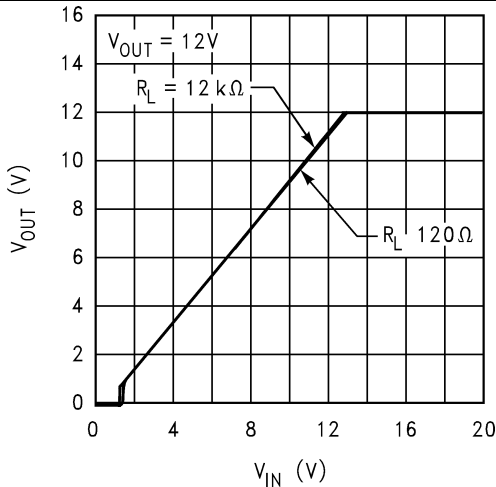


Figure 11. Output Voltage vs Input Voltage

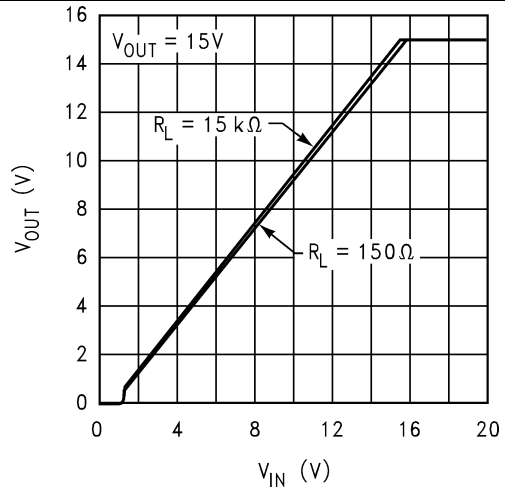


Figure 12. Output Voltage vs Input Voltage

Typical Characteristics (continued)

Unless indicated otherwise,  $V_{IN} = V_{NOM} + 1.5\text{ V}$ ,  $C_{IN} = 0.1\ \mu\text{F}$ ,  $C_{OUT} = 0.1\ \mu\text{F}$ , and  $T_A = 25^\circ\text{C}$ .

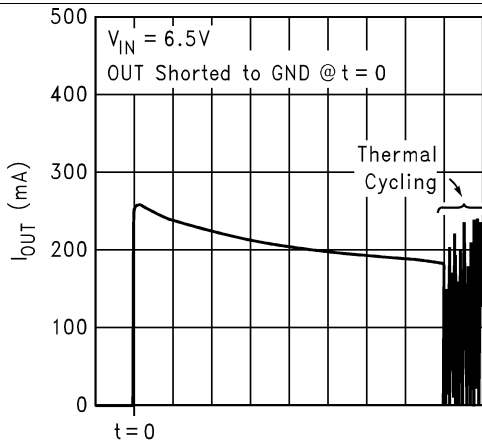


Figure 13. Output Short-Circuit Current

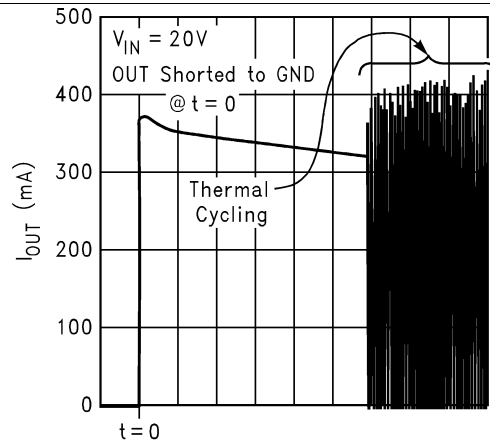


Figure 14. Output Short-Circuit Current

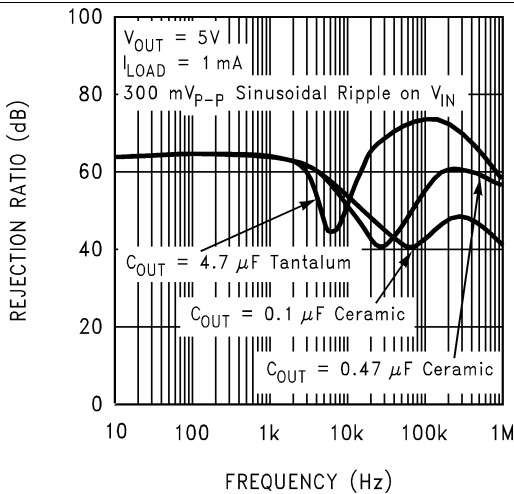


Figure 15. Power Supply Rejection Ratio

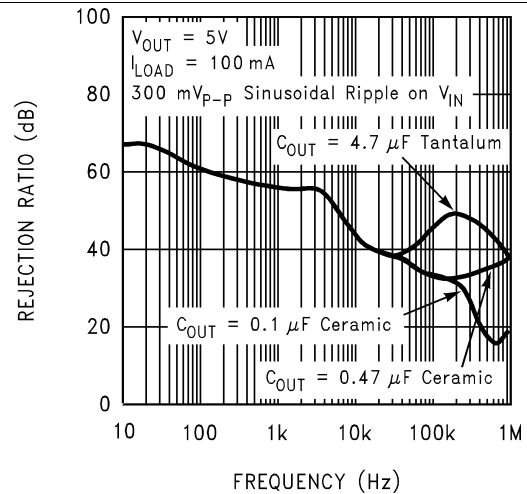


Figure 16. Power Supply Rejection Ratio

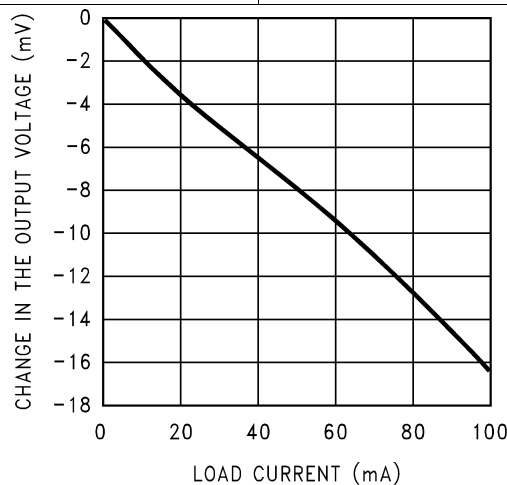


Figure 17. DC Load Regulation



## 8 Application and Implementation

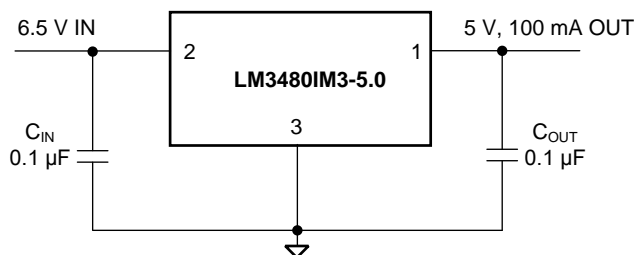
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The LM3480 is a linear voltage regulator with 1.2-V ensured maximum dropout and 100-mA ensured minimum load current. This device has 3.3-V, 5-V, 12-V, and 15-V versions. The implementation of LM3480 is discussed in this section.

### 8.2 Typical Application



#### 8.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	6.5 V
Output voltage	5 V
Output current	100 mA

#### 8.2.2 Detailed Design Procedure

##### 8.2.2.1 External Capacitors

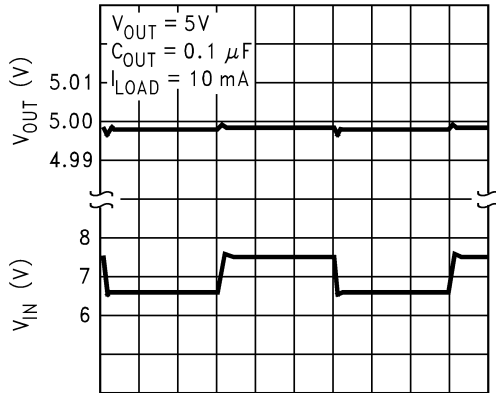
A minimum input and output capacitance value of 0.1  $\mu\text{F}$  is required for stability and adequate transient performance. There is no specific ESR limitation, although excessively high ESR will compromise transient performance. There is no specific limitation on a maximum capacitance value on the input or the output.

##### 8.2.2.1.1 Output Capacitor

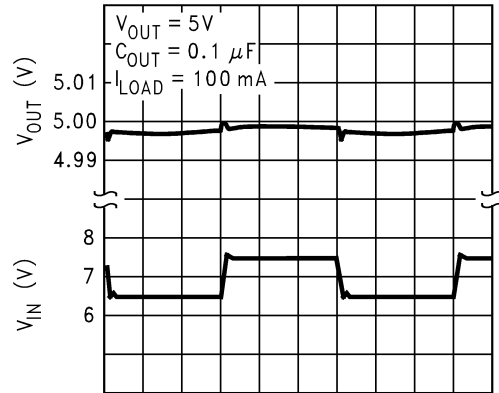
The minimum output capacitance required to maintain stability is 0.1  $\mu\text{F}$ . Larger values of output capacitance can be used to improve transient behavior.

### 8.2.3 Application Curves

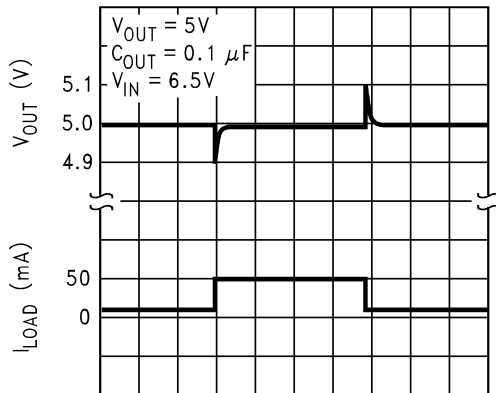
Unless indicated otherwise,  $V_{\text{IN}} = 6.5 \text{ V}$ ,  $V_{\text{OUT}} = 5 \text{ V}$ ,  $C_{\text{OUT}} = 0.1 \mu\text{F}$ , and  $T_{\text{A}} = 25^\circ\text{C}$



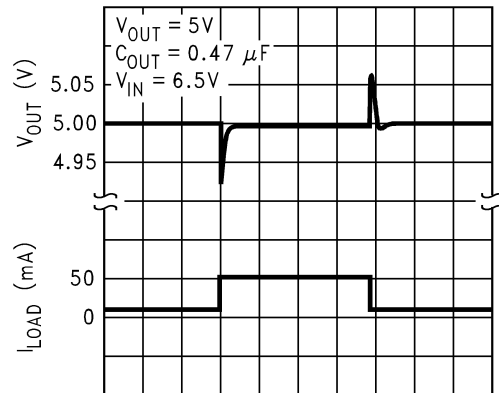
200  $\mu$ s/Div  
**Figure 18. Line Transient Response**



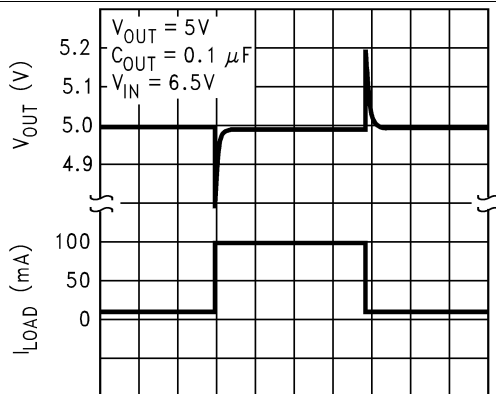
200  $\mu$ s/Div  
**Figure 19. Line Transient Response**



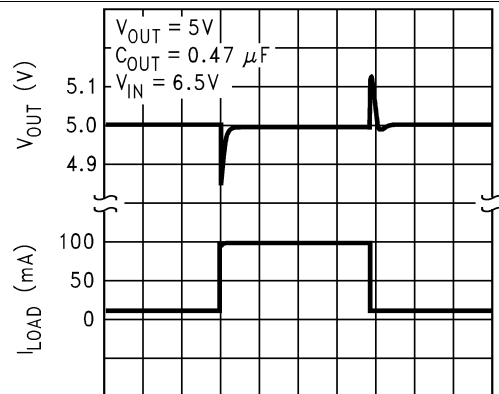
50  $\mu$ s/Div  
**Figure 20. Load Transient Response**



50  $\mu$ s/Div  
**Figure 21. Load Transient Response**



50  $\mu$ s/Div  
**Figure 22. Load Transient Response**



50  $\mu$ s/Div  
**Figure 23. Load Transient Response**

## 9 Power Supply Recommendations

The LM3480 is designed to operate from up to a 30-V input voltage supply. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help to improve the output noise performance.

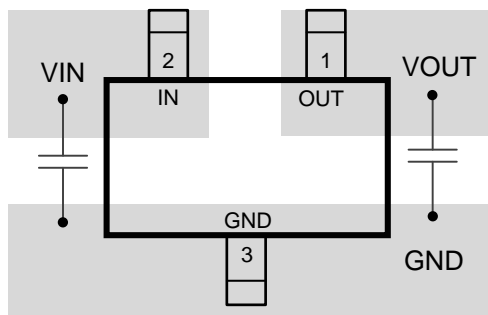
## 10 Layout

### 10.1 Layout Guidelines

For best overall performance, place all the circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitors, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes the inductive parasitic, and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread heat from the LDO device. In most applications, this ground plane is necessary to meet thermal requirements.

### 10.2 Layout Example



## 11 Device and Documentation Support

### 11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.2 Trademarks

E2E is a trademark of Texas Instruments.  
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### 11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3480IM3-12	NRND	SOT-23	DBZ	3	1000	TBD	Call TI	Call TI	-40 to 125	L0C	
LM3480IM3-12/NOPB	ACTIVE	SOT-23	DBZ	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0C	<a href="#">Samples</a>
LM3480IM3-15/NOPB	ACTIVE	SOT-23	DBZ	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0D	<a href="#">Samples</a>
LM3480IM3-3.3	NRND	SOT-23	DBZ	3	1000	TBD	Call TI	Call TI	-40 to 125	L0A	
LM3480IM3-3.3/NOPB	ACTIVE	SOT-23	DBZ	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0A	<a href="#">Samples</a>
LM3480IM3-5.0	NRND	SOT-23	DBZ	3	1000	TBD	Call TI	Call TI	-40 to 125	L0B	
LM3480IM3-5.0/NOPB	ACTIVE	SOT-23	DBZ	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0B	<a href="#">Samples</a>
LM3480IM3X-12/NOPB	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0C	<a href="#">Samples</a>
LM3480IM3X-15/NOPB	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0D	<a href="#">Samples</a>
LM3480IM3X-3.3	NRND	SOT-23	DBZ	3	3000	TBD	Call TI	Call TI	-40 to 125	L0A	
LM3480IM3X-3.3/NOPB	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0A	<a href="#">Samples</a>
LM3480IM3X-5.0/NOPB	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0B	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3480IM3-12	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM3480IM3-12/NOPB	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM3480IM3-15/NOPB	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM3480IM3-3.3	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM3480IM3-3.3/NOPB	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM3480IM3-5.0	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM3480IM3-5.0/NOPB	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM3480IM3X-12/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM3480IM3X-15/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM3480IM3X-3.3	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM3480IM3X-3.3/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM3480IM3X-5.0/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

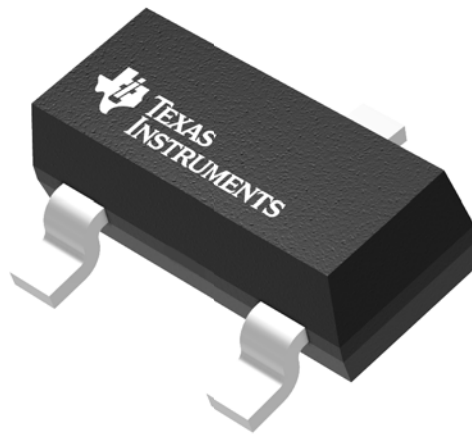
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3480IM3-12	SOT-23	DBZ	3	1000	210.0	185.0	35.0
LM3480IM3-12/NOPB	SOT-23	DBZ	3	1000	210.0	185.0	35.0
LM3480IM3-15/NOPB	SOT-23	DBZ	3	1000	210.0	185.0	35.0
LM3480IM3-3.3	SOT-23	DBZ	3	1000	210.0	185.0	35.0
LM3480IM3-3.3/NOPB	SOT-23	DBZ	3	1000	210.0	185.0	35.0
LM3480IM3-5.0	SOT-23	DBZ	3	1000	210.0	185.0	35.0
LM3480IM3-5.0/NOPB	SOT-23	DBZ	3	1000	210.0	185.0	35.0
LM3480IM3X-12/NOPB	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LM3480IM3X-15/NOPB	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LM3480IM3X-3.3	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LM3480IM3X-3.3/NOPB	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LM3480IM3X-5.0/NOPB	SOT-23	DBZ	3	3000	210.0	185.0	35.0

**GENERIC PACKAGE VIEW**

**DBZ 3**

**SOT-23 - 1.12 mm max height**

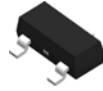
SMALL OUTLINE TRANSISTOR



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4203227/C

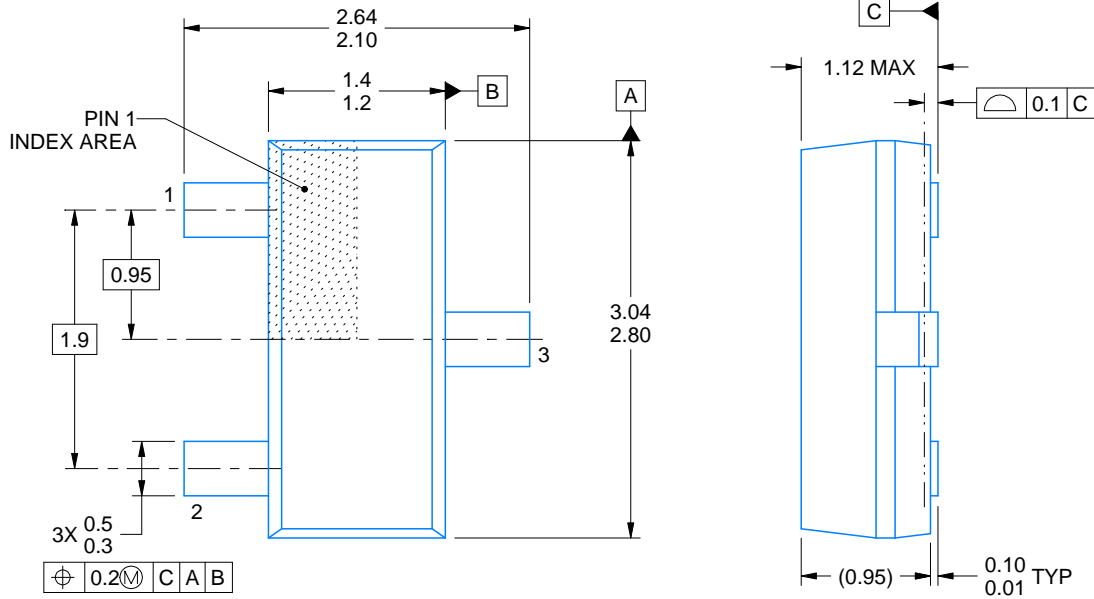
DBZ0003A



# PACKAGE OUTLINE

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



4214838/C 04/2017

NOTES:

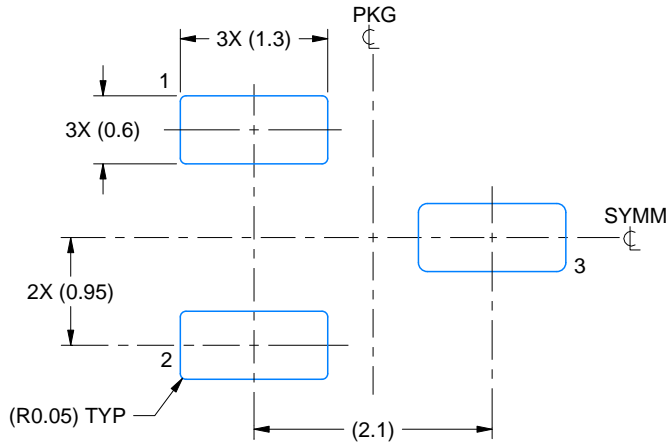
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.

# EXAMPLE BOARD LAYOUT

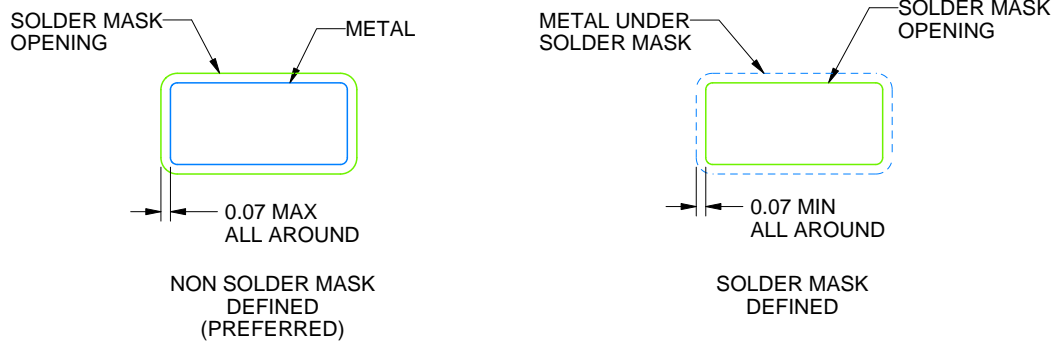
DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
SCALE:15X



SOLDER MASK DETAILS

4214838/C 04/2017

NOTES: (continued)

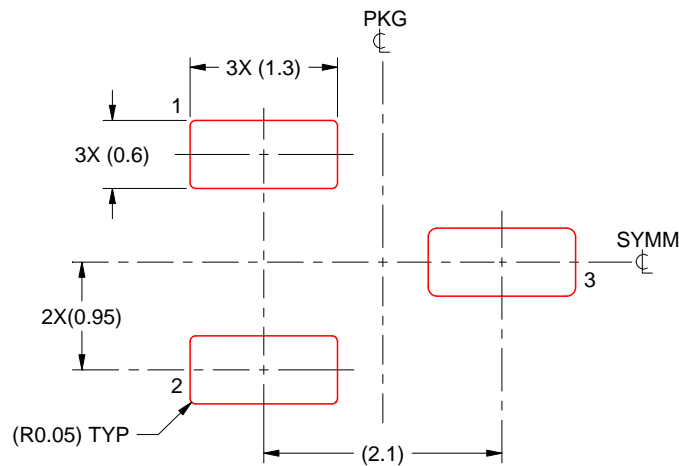
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:15X

4214838/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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