



**THE DATASHEET OF
LM3668SD-4550/NOPB**



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision N (August 2014) to Revision O Page

- Changed $R_{\theta JA}$ value from 34 to 47.3; change 20 PINS to 12 PINS in header; add additional thermal information..... 5

Changes from Revision M (May 2013) to Revision N Page

- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

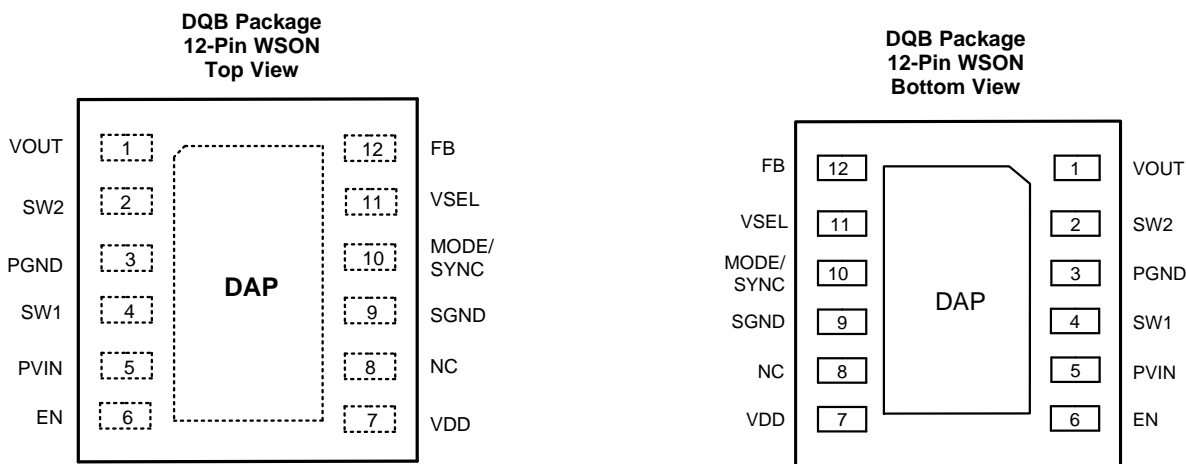
Changes from Revision L (April 2013) to Revision M Page

- Changed layout of National Data Sheet to TI format 23

5 Device Comparison Table

ORDER NUMBER	OUTPUT VOLTAGE (V)	PACKAGE	PACKAGE MARKING	SUPPLIED AS
LM3668SD-2833/NOPB	2.8, V _{SEL} = low 3.3, V _{SEL} = high	DQB (WSON)	S017B	1000 units, tape-and-reel
LM3668SDX-2833/NOPB				4500 units, tape-and-reel
LM3668SD-3034/NOPB	3, V _{SEL} = low 3.4, V _{SEL} = high		S018B	1000 units, tape-and-reel
LM3668SDX-3034/NOPB				4500 units, tape-and-reel
LM3668SD-4550/NOPB	4.5, V _{SEL} = low 5, V _{SEL} = high		S019B	1000 units, tape-and-reel
LM3668SDX-4550/NOPB				4500 units, tape-and-reel

6 Pin Configuration and Functions



Pin Functions⁽¹⁾

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VOUT	A	Connect to output capacitor.
2	SW2	A	Switching node connection to the internal PFET switch (P2) and NFET synchronous rectifier (N2).
3	PGND	G	Power ground.
4	SW1	A	Switching node connection to the internal PFET switch (P1) and NFET synchronous rectifier (N1).
5	PVIN	P	Supply to the power switch, connect to the input capacitor.
6	EN	I	Enable input. Set this digital input high for normal operation. For shutdown, set low.
7	VDD	P	Signal supply input. If board layout is not optimum an optional 1- μ F ceramic capacitor is suggested as close to this pin as possible.
8	NC	-	No connect. Connect this pin to SGND on PCB layout.
9	SGND	G	Analog and Control Ground.
10	MODE/SYNC	I	Mode = LOW, Automatic Mode. Mode= HI, forced PWM Mode. SYNC = external clock synchronization from 1.6 MHz to 2.7 MHz.(When SYNC function is used, device is forced in PWM mode).
11	VSEL	I	Voltage selection pin; (for example, 2.8-V-3.3-V option) logic input low (or GND) = 2.8 V and logic high = 3.3 V (or V _{IN}) to set output voltage.
12	FB	A	Feedback analog input. Connect to the output at the output filter.
DAP	DAP	-	Die Attach Pad, connect the DAP to SGND on PCB layout to enhance thermal performance. It should not be used as a primary ground connection.

(1) A: Analog Pin, G: Ground Pin, P: Power Pin, I: Digital Input Pin

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

	MIN	MAX	UNIT
PVIN, VDD, SW1, SW2 & VOUT pins: voltage to SGND & PGND	–0.2	6	V
FB, EN, and MODE/SYNC pins	(PGND and SGND–0.2)	(PV _{IN} + 0.2)	V
PGND to SGND	–0.2	0.2	V
Continuous power dissipation ⁽³⁾	Internally Limited		
Maximum junction temperature (T _{J-MAX})		125	°C
Maximum lead temperature (soldering, 10 sec)		260	°C
Storage temperature, T _{stg}	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (T_{J-MAX-OP} = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (R_{θJA}), as given by the following equation: T_{A-MAX} = T_{J-MAX-OP} – (R_{θJA} × P_{D-MAX}).

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Input voltage	2.5	5.5	V
Recommended load current	0	1	A
Junction temperature (T _J)	–40	125	°C
Ambient temperature (T _A) ⁽¹⁾	–40	85	°C

- (1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (T_{J-MAX-OP} = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (R_{θJA}), as given by the following equation: T_{A-MAX} = T_{J-MAX-OP} – (R_{θJA} × P_{D-MAX}).

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LM3668	UNIT
		DQB (WSON)	
		12 PINS	
R _{θJA}	Junction-to-ambient thermal resistance, WSON package ⁽²⁾	47.3	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	43.4	
R _{θJB}	Junction-to-board thermal resistance	21.6	
ψ _{JT}	Junction-to-top characterization parameter	0.4	
ψ _{JB}	Junction-to-board characterization parameter	21.7	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	3.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

(2) Junction-to-ambient thermal resistance (R_{θJA}) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. The test board is a 4-layer FR-4 board measuring 101.6 mm x 76.2 mm x 1.6 mm. Thickness of the copper layers are 2oz/1oz/1oz/2oz. The middle layer of the board is 60 mm x 60 mm. Ambient temperature in simulation is 22°C, still air. Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

7.5 Electrical Characteristics

Unless otherwise noted, specifications apply to the LM3668. V_{IN} = 3.6 V = EN, V_{OUT} = 3.3 V. For V_{OUT} = 4.5V-5 V, V_{IN} = 4 V.⁽¹⁾⁽²⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{FB}	Feedback voltage	-40°C ≤ T _A ≤ 85°C, see ⁽²⁾	-3%		3%	
I _{LIM}	Switch peak current limit	Open loop ⁽³⁾		1.85		A
	Switch peak current limit	Open loop ⁽³⁾ , -40°C ≤ T _A ≤ 85°C	1.6		2.05	
I _{SHDN}	Shutdown supply current	EN = 0 V		0.01		μA
	Shutdown supply current	EN = 0 V, -40°C ≤ T _A ≤ 85°C			1	
I _{Q_PFM}	DC bias current in PFM	No load, device is not switching (FB forced higher than programmed output voltage)		45		μA
	DC bias current in PFM	No load, device is not switching (FB forced higher than programmed output voltage) -40°C ≤ T _A ≤ 85°C			60	
I _{Q_PWM}	DC bias current in PWM	PWM mode, no switching		600		μA
	DC bias current in PWM	PWM mode, no switching -40°C ≤ T _A ≤ 85°C			750	
R _{DSON(P)}	Pin-pin resistance for PFET	Switches P1 and P2		130	180	mΩ
R _{DSON(N)}	Pin-pin resistance for NFET	Switches N1 and N2		100	150	mΩ
F _{OSC}	Internal oscillator frequency	PWM mode		2.2		MHz
		PWM mode, -40°C ≤ T _A ≤ 85°C	1.9		2.5	
F _{SYNC}	Sync frequency range	V _{IN} = 3.6 V	1.6		2.7	MHz
V _{IH}	Logic high input for EN, MODE/SYNC pins	-40°C ≤ T _A ≤ 85°C	1.1			V
V _{IL}	Logic low input for EN, MODE/SYNC pins	-40°C ≤ T _A ≤ 85°C			0.4	V
I _{EN, MODE, SYNC}	EN, MODE/SYNC pins input current			0.3		μA
		-40°C ≤ T _A ≤ 85°C			1	

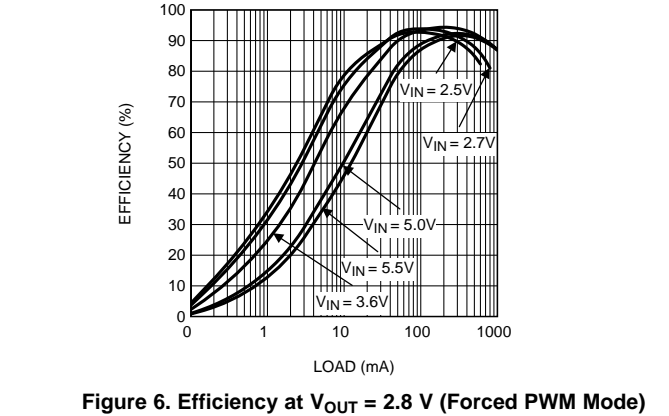
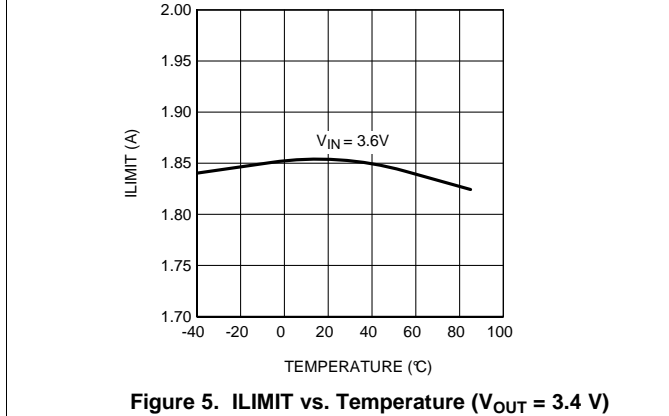
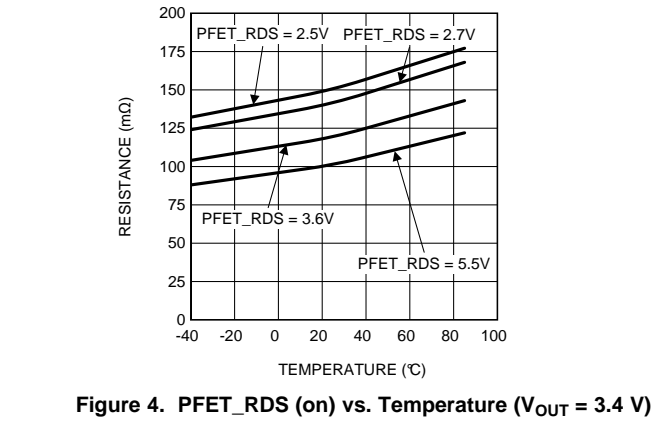
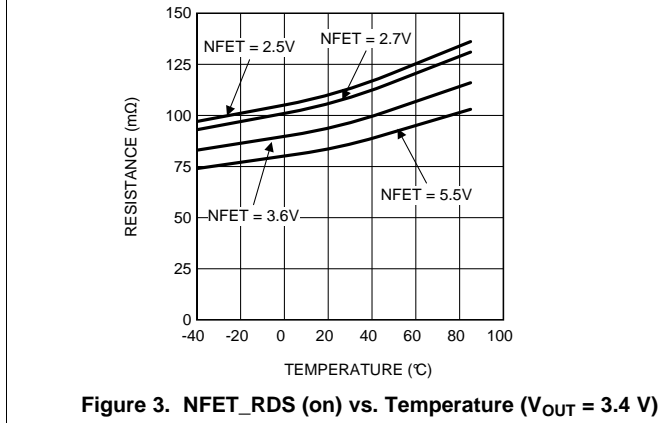
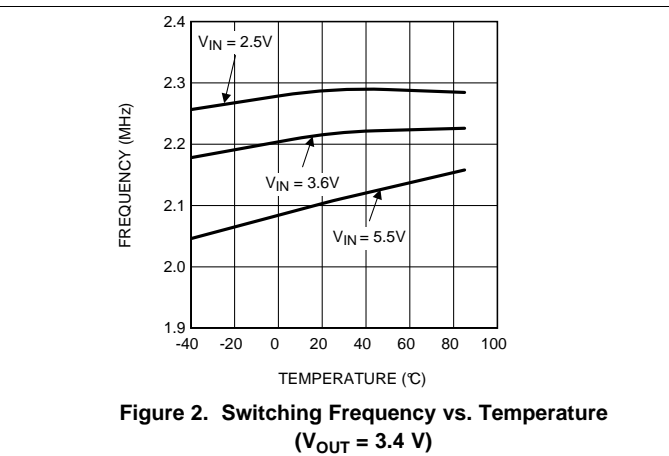
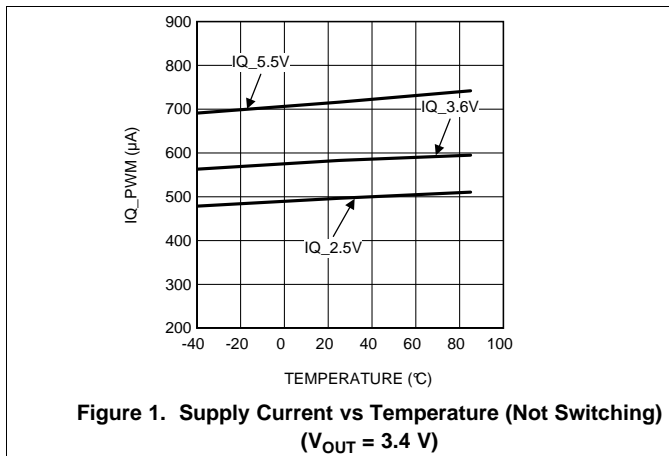
(1) All voltages with respect to SGND.

(2) Minimum and Maximum limits are specified by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.

(3) [Electrical Characteristics](#) table reflects open loop data (FB = 0 V and current drawn from SW pin ramped up until cycle-by-cycle current limits is activated). Closed loop current limit is the peak inductor current measured in the application circuit by increasing output current until output voltage drops by 10%.

7.6 Typical Characteristics

Typical Application Circuit (see [Figure 46](#)): $V_{IN} = 3.6\text{ V}$, $L = 2.2\ \mu\text{H}$, $C_{IN} = 10\ \mu\text{F}$, $C_{OUT} = 22\ \mu\text{F}^{(4)}$, $T_A = 25^\circ\text{C}$, unless otherwise stated.



(4) C_{IN} and C_{OUT} : Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics. C_{OUT_MIN} should not exceed -40% of suggested value. The preferable choice would be a type and make MLCC that issues -30% over the operating temperature and voltage range.

Typical Characteristics (continued)

Typical Application Circuit (see [Figure 46](#)): $V_{IN} = 3.6\text{ V}$, $L = 2.2\ \mu\text{H}$, $C_{IN} = 10\ \mu\text{F}$, $C_{OUT} = 22\ \mu\text{F}^{(4)}$, $T_A = 25^\circ\text{C}$, unless otherwise stated.

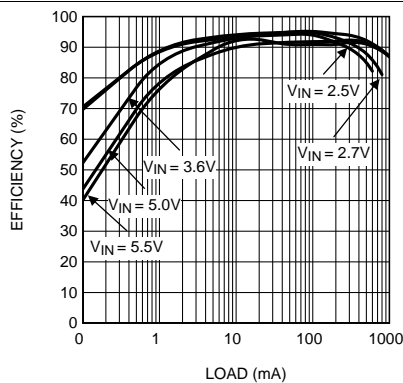


Figure 7. Efficiency at $V_{OUT} = 2.8\text{ V}$ (Auto Mode)

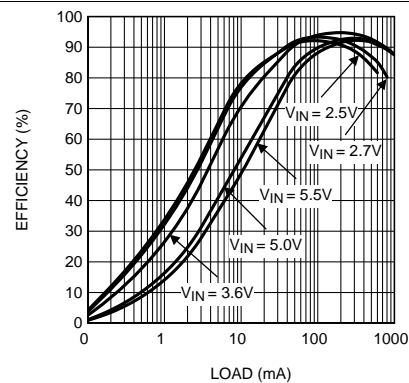


Figure 8. Efficiency at $V_{OUT} = 3\text{ V}$ (Forced PWM Mode)

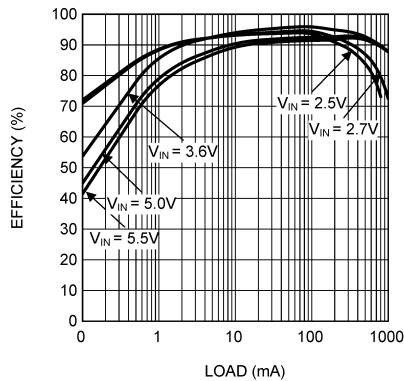


Figure 9. Efficiency at $V_{OUT} = 3\text{ V}$ (Auto Mode)

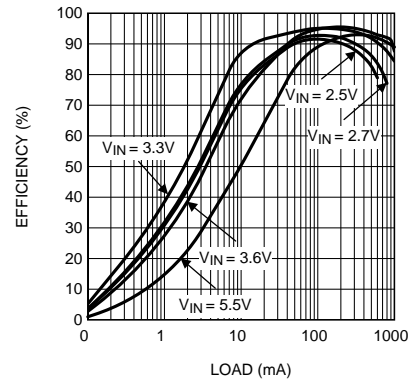


Figure 10. Efficiency at $V_{OUT} = 3.3\text{ V}$ (Forced PWM Mode)

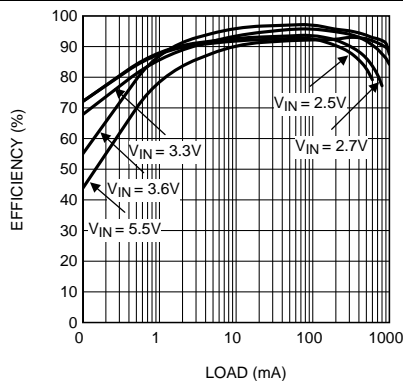


Figure 11. Efficiency at $V_{OUT} = 3.3\text{ V}$ (Auto Mode)

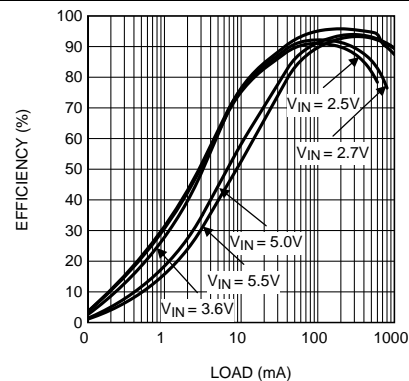


Figure 12. Efficiency at $V_{OUT} = 3.4\text{ V}$ (Forced PWM Mode)

Typical Characteristics (continued)

Typical Application Circuit (see [Figure 46](#)): $V_{IN} = 3.6\text{ V}$, $L = 2.2\ \mu\text{H}$, $C_{IN} = 10\ \mu\text{F}$, $C_{OUT} = 22\ \mu\text{F}^{(4)}$, $T_A = 25^\circ\text{C}$, unless otherwise stated.

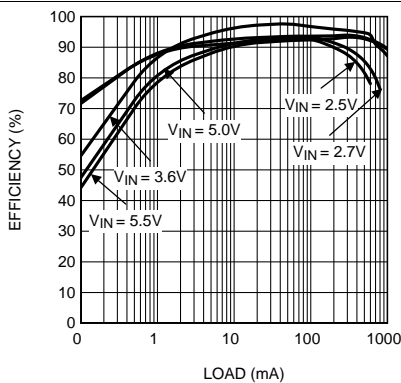


Figure 13. Efficiency at $V_{OUT} = 3.4\text{ V}$ (Auto Mode)

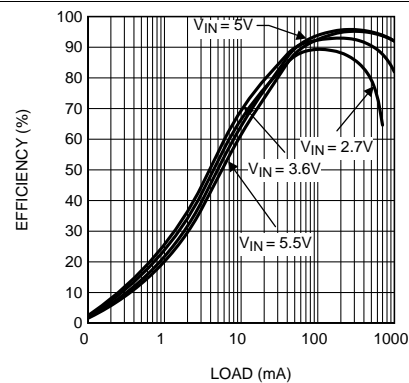


Figure 14. Efficiency at $V_{OUT} = 4.5\text{ V}$ (Forced PWM Mode)

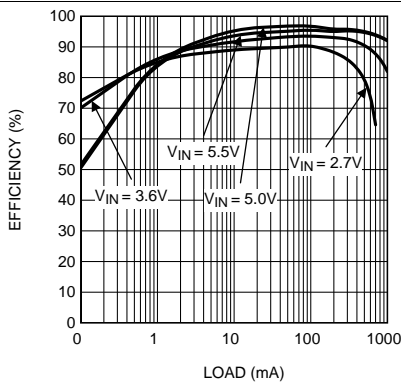


Figure 15. Efficiency at $V_{OUT} = 4.5\text{ V}$ (Auto Mode)

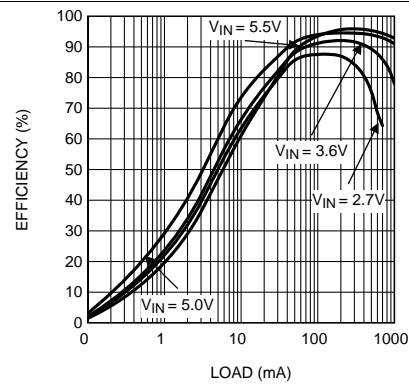


Figure 16. Efficiency at $V_{OUT} = 5\text{ V}$ (Forced PWM Mode)

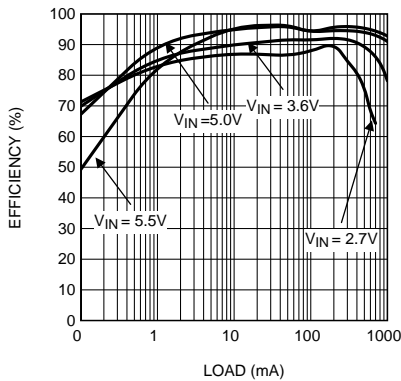


Figure 17. Efficiency at $V_{OUT} = 5\text{ V}$ (Auto Mode)

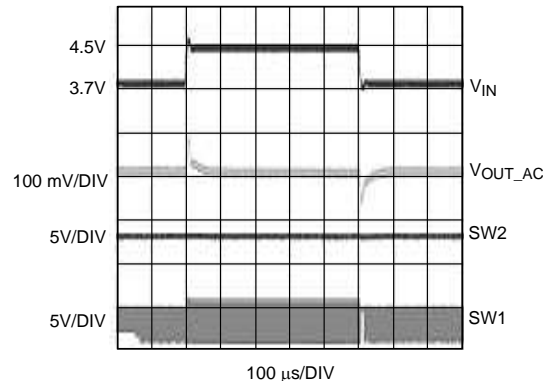


Figure 18. Line Transient in Buck Mode ($V_{OUT} = 3.4\text{ V}$, Load = 500 mA)

Typical Characteristics (continued)

Typical Application Circuit (see [Figure 46](#)): $V_{IN} = 3.6\text{ V}$, $L = 2.2\ \mu\text{H}$, $C_{IN} = 10\ \mu\text{F}$, $C_{OUT} = 22\ \mu\text{F}^{(4)}$, $T_A = 25^\circ\text{C}$, unless otherwise stated.

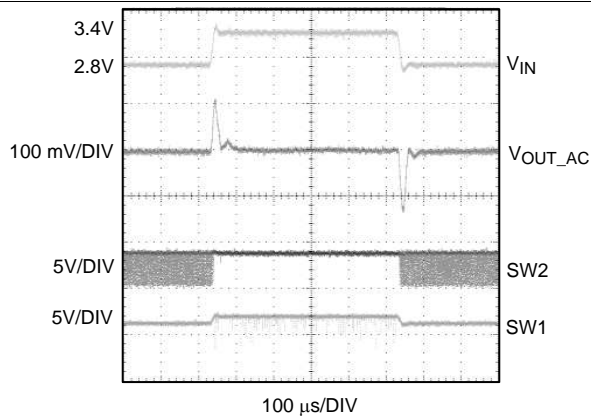


Figure 19. Line Transient in Boost Mode ($V_{OUT} = 3.4\text{ V}$, Load = 500 mA)

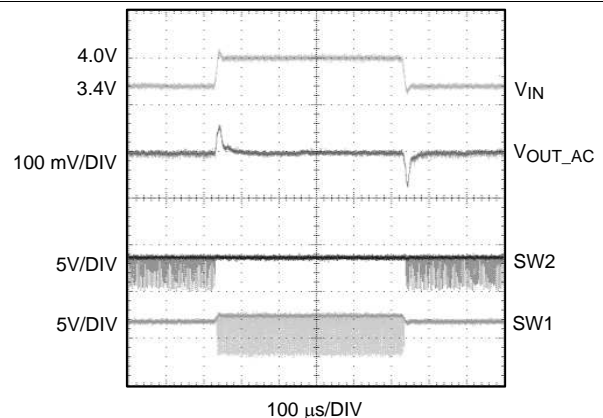


Figure 20. Line Transient in Buck-Boost Mode ($V_{OUT} = 3.4\text{ V}$, Load = 500 mA)

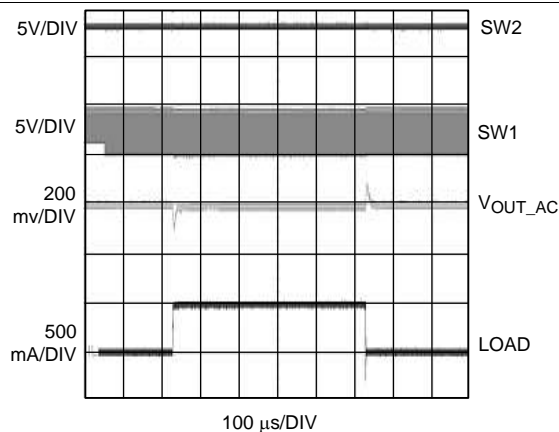


Figure 21. Load Transient in Buck Mode (Forced PWM Mode) $V_{IN} = 4.2\text{ V}$, $V_{OUT} = 3.4\text{ V}$, Load = 0 to 500 mA

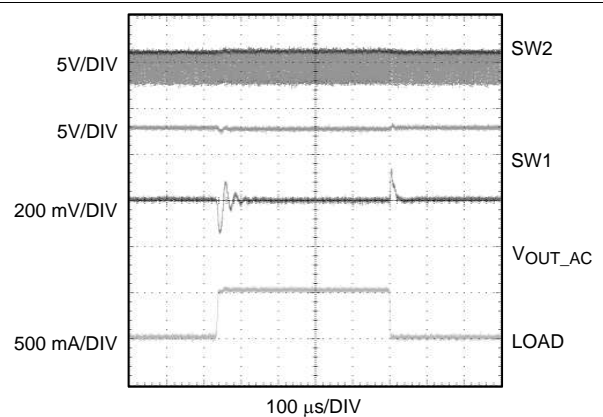


Figure 22. Load Transient in Boost Operation (Forced PWM Mode) $V_{IN} = 2.7\text{ V}$, $V_{OUT} = 3.4\text{ V}$, Load = 0 to 500 mA

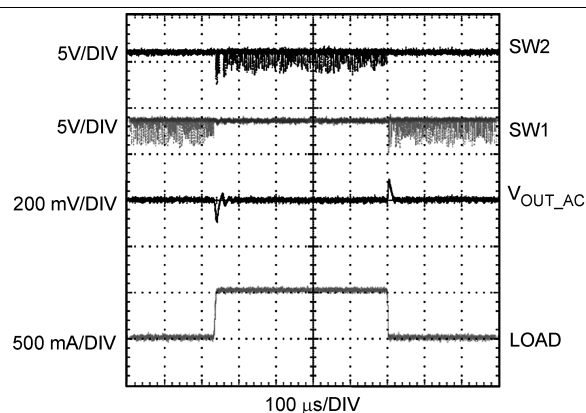


Figure 23. Load Transient in Buck-Boost Operation (Forced PWM Mode) $V_{IN} = 3.44\text{ V}$, $V_{OUT} = 3.4\text{ V}$, Load = 0 to 500 mA

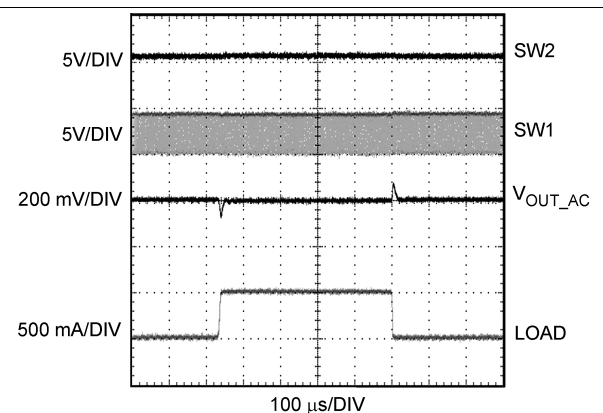
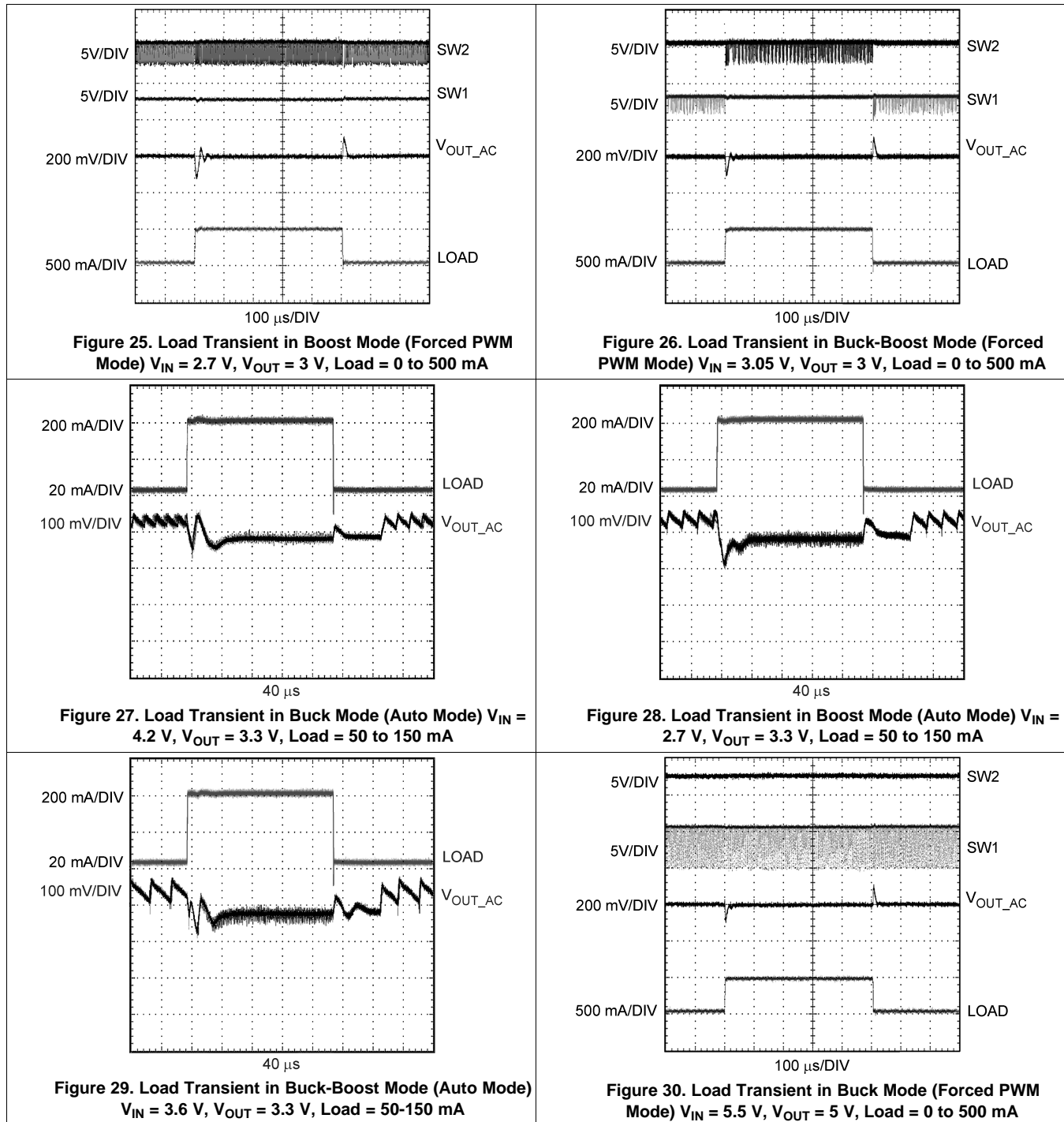


Figure 24. Load Transient in Buck Mode (Forced PWM Mode) $V_{IN} = 4.2\text{ V}$, $V_{OUT} = 3\text{ V}$, Load = 0 to 500 mA

Typical Characteristics (continued)

Typical Application Circuit (see [Figure 46](#)): $V_{IN} = 3.6\text{ V}$, $L = 2.2\ \mu\text{H}$, $C_{IN} = 10\ \mu\text{F}$, $C_{OUT} = 22\ \mu\text{F}^{(4)}$, $T_A = 25^\circ\text{C}$, unless otherwise stated.



Typical Characteristics (continued)

Typical Application Circuit (see [Figure 46](#)): $V_{IN} = 3.6\text{ V}$, $L = 2.2\text{ }\mu\text{H}$, $C_{IN} = 10\text{ }\mu\text{F}$, $C_{OUT} = 22\text{ }\mu\text{F}^{(4)}$, $T_A = 25^\circ\text{C}$, unless otherwise stated.

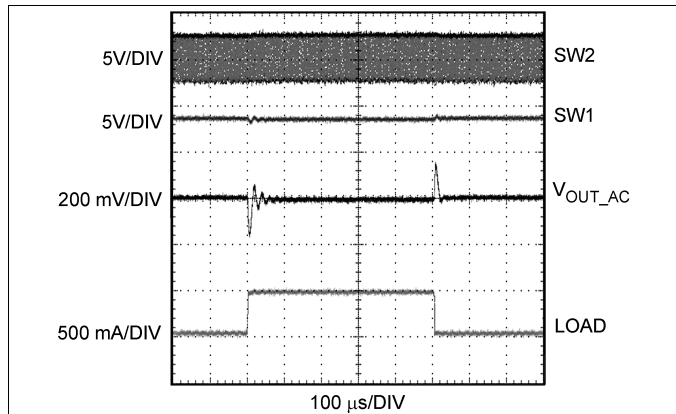


Figure 31. Load Transient in Boost Mode (Forced PWM Mode) $V_{IN} = 3.5\text{ V}$, $V_{OUT} = 5\text{ V}$, Load = 0 to 500 mA

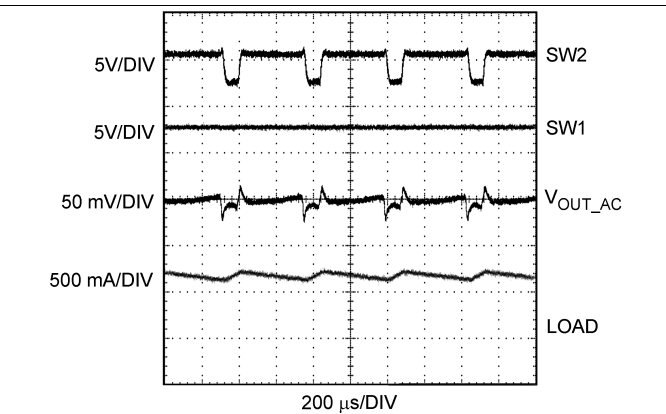


Figure 32. Typical Switching Waveform in Boost Mode (PWM Mode) $V_{IN} = 2.7\text{ V}$, $V_{OUT} = 3\text{ V}$, Load = 500 mA

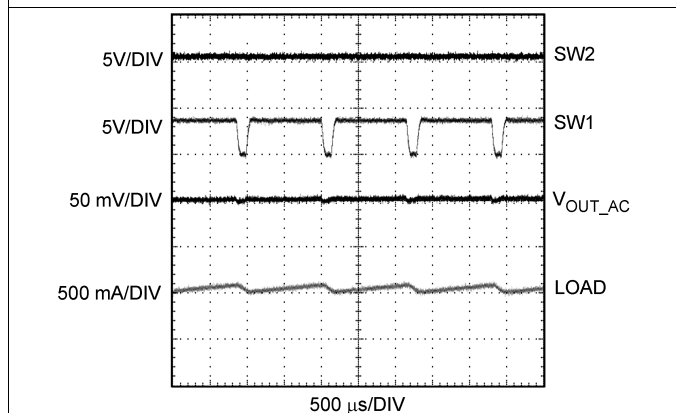


Figure 33. Typical Switching Waveform in Buck Mode (PWM Mode) $V_{IN} = 3.6\text{ V}$, $V_{OUT} = 3\text{ V}$, Load = 500 mA

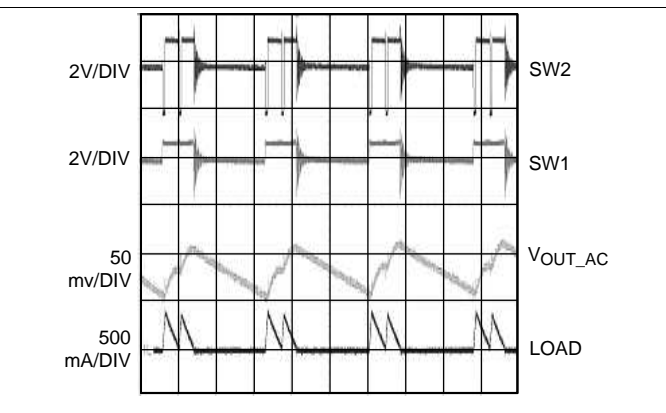


Figure 34. Typical Switching Waveform in Boost Mode (PFM Mode) $V_{IN} = 2.7\text{ V}$, $V_{OUT} = 3\text{ V}$, Load = 50 mA

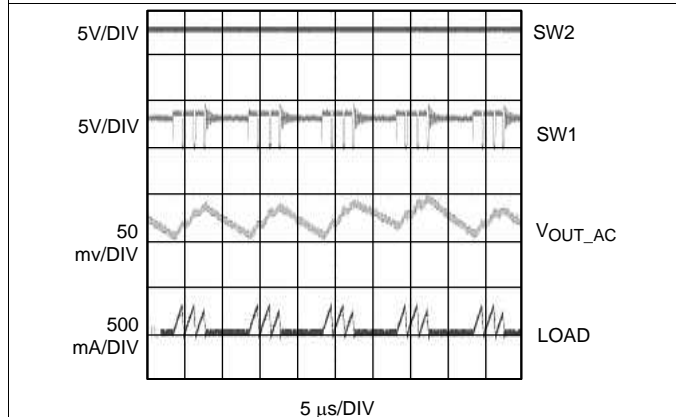


Figure 35. Typical Switching Waveform in Buck Mode (PFM Mode) $V_{IN} = 3.6\text{ V}$, $V_{OUT} = 3\text{ V}$, Load = 50 mA

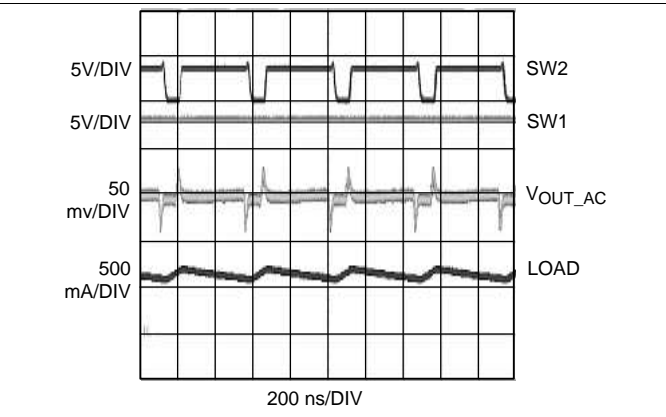
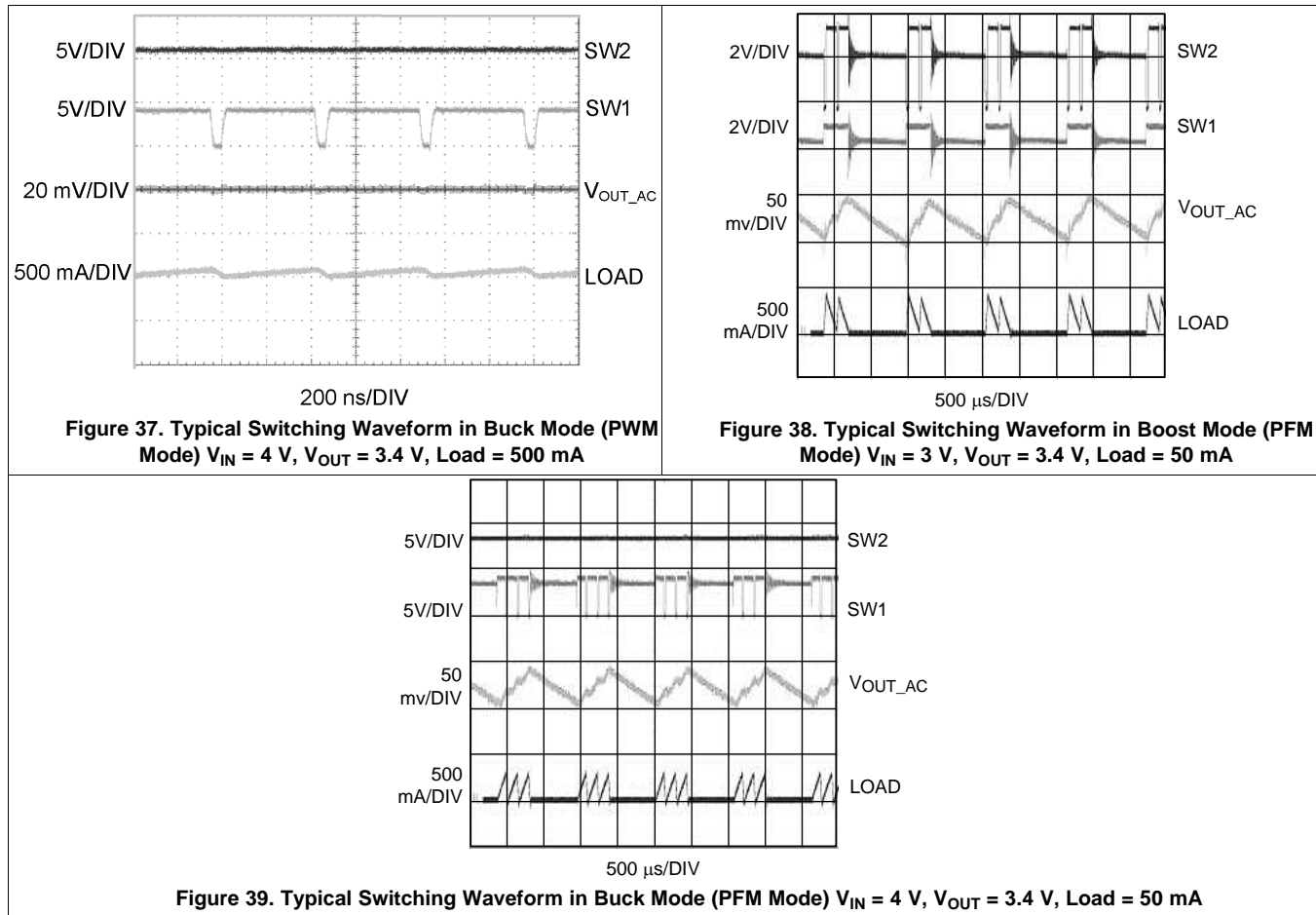


Figure 36. Typical Switching Waveform in Boost Mode (PWM Mode) $V_{IN} = 3\text{ V}$, $V_{OUT} = 3.4\text{ V}$, Load = 500 mA

Typical Characteristics (continued)

Typical Application Circuit (see [Figure 46](#)): $V_{IN} = 3.6\text{ V}$, $L = 2.2\ \mu\text{H}$, $C_{IN} = 10\ \mu\text{F}$, $C_{OUT} = 22\ \mu\text{F}^{(4)}$, $T_A = 25^\circ\text{C}$, unless otherwise stated.



8 Detailed Description

8.1 Overview

The LM3668, a high-efficiency buck or boost DC-DC converter, delivers a constant voltage from either a single Li-Ion or three cell NiMH/NiCd battery to portable devices such as mobile phones and PDAs. Using a voltage mode architecture with synchronous rectification, the device has the ability to deliver up to 1 A, depending on the input voltage, output voltage, ambient temperature and the chosen inductor.

In addition, the device incorporates a seamless transition from buck-to-boost or boost-to-buck mode. The internal error amplifier continuously monitors the output to determine the transition from buck-to-boost or boost-to-buck operation. Figure 40 shows the four switches network used for the buck and boost operation. Table 1 summarizes the state of the switches in different modes.

There are three modes of operation depending on the current required: Pulse Width Modulation (PWM), Pulse Frequency Modulation (PFM), and shutdown. The device operates in PWM mode at load currents of approximately 80 mA or higher to improve efficiency. Lighter load current causes the device to automatically switch into PFM mode to reduce current consumption and extend battery life. Shutdown mode turns off the device, offering the lowest current consumption.

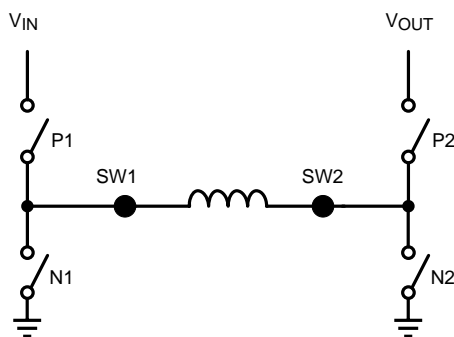
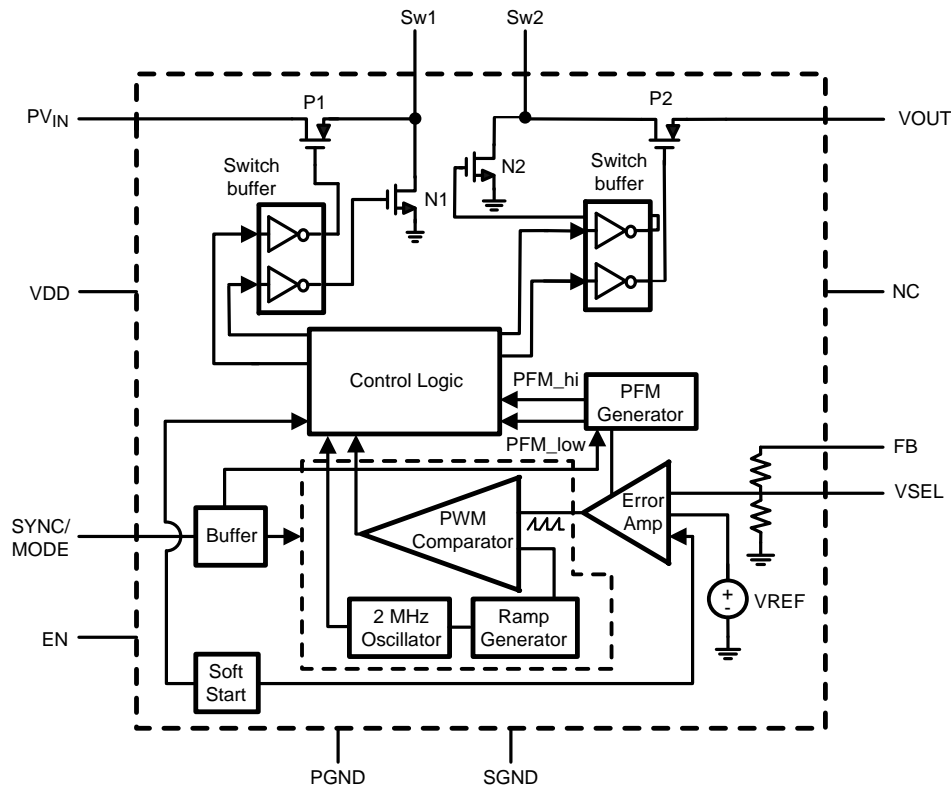


Figure 40. Simplified Diagram of Switches

Table 1. State of Switches in Different Modes

MODE	ALWAYS ON	ALWAYS OFF	SWITCHING
Buck	SW P2	SW N2	SW P1 & N1
Boost	SW P1	SW N1	SW N2 & P2

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Buck Operation

When the input voltage is greater than the output voltage, the device operates in buck mode where switch P2 is always ON and P1 and N1 control the output. [Figure 41](#) shows the simplified circuit for buck mode operation.

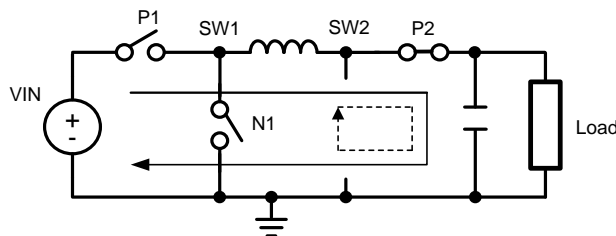


Figure 41. Simplified Circuit for Buck Operation

8.3.2 Boost Operation

When the input voltage is smaller than the output voltage, the device enters boost mode operation where P1 is always ON, while switches N2 and P2 control the output. [Figure 42](#) shows the simplified circuit for boost mode operation.

Feature Description (continued)

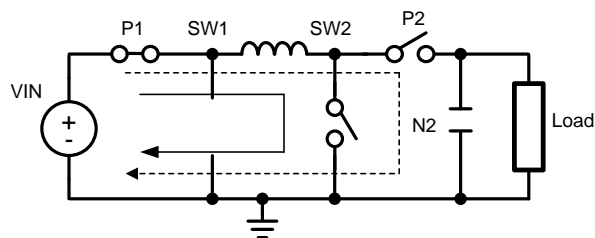


Figure 42. Simplified Circuit for Boost Operation

8.3.3 Internal Synchronous Rectification

While in PWM mode, the LM3668 uses an internal MOSFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compare to the voltage drop across an ordinary rectifier diode.

8.3.4 Current Limit Protection

The LM3668 has current limit protection to prevent excessive stress on itself and external components during overload conditions. The internal current limit comparator will disable the power device at a typical switch peak current limit of 1.85 A (typ.).

8.3.5 Undervoltage Protection

The LM3668 has an UVP comparator to turn the power device off in case the input voltage or battery voltage is too low. The typical UVP threshold is around 2 V.

8.3.6 Short Circuit Protection

When the output of the LM3668 is shorted to GND, the current limit is reduced to about half of the typical current limit value until the short is removed.

8.3.7 Shutdown

When the EN pin is pulled low, P1 and P2 are off; N1 and N2 are turned on to pull SW1 and SW2 to ground.

8.3.8 Thermal Shutdown

The LM3668 has an internal thermal shutdown function to protect the die from excessive temperatures. The thermal shutdown trip point is typically 150°C; normal operation resumes when the temperature drops below 125°C.

8.3.9 Start-Up

The LM3668 has a soft-start circuit that smooth the output voltage and ramp current during start-up. During start-up the bandgap reference is slowly ramped up and switch current limit is reduced to half the typical value. Soft start is activated only if EN goes from logic low to logic high after V_{IN} reaches 2.5 V. The start-up time thereby depends on the output capacitor and load current demanded at start-up. It is not recommended to start up the device at full load while in soft-start.

8.4 Device Functional Modes

8.4.1 PWM Operation

In PWM operation, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. In Normal operation, the internal error amplifier provides an error signal, V_c , from the feedback voltage and V_{ref} . The error amplifier signal, V_c , is compared with a voltage, V_{center} , and used to generate the PWM signals for both buck & boost modes. Signal V_{center} is a DC signal which sets the transition point of the buck and boost modes. Below are three regions of operation:

- Region I: If V_c is less than V_{center} , Buck mode.
- Region II: If V_c and V_{center} are equal, both PMOS switches (P1, P2) are on and both NMOS switches (N1, N2) are off. The power passes directly from input to output via P1 & P2
- Region III: If V_c is greater than V_{center} , Boost mode.

The Buck-Boost operation is avoided, to improve the efficiency across V_{IN} and load range.

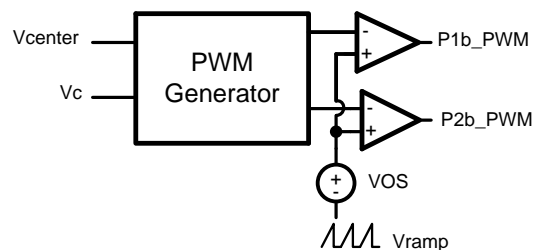


Figure 43. PWM Generator Block Diagram

8.4.2 PFM Operation

At very light loads, the converter enters PFM mode and operates with reduced switching frequency and supply current to maintain high efficiency. The part automatically transitions into PFM mode when either of two following conditions occur for a duration of 128 or more clock cycles:

- The inductor current reaches zero.
- The peak inductor current drops below the I_{MODE} level, (Typically $I_{MODE} < 45 \text{ mA} + V_{IN}/80 \Omega$).

In PFM operation, the compensation circuit in the error amplifier is turned off. The error amplifier works as a hysteretic comparator. The PFM comparator senses the output voltage via the feedback pin and controls the switching of the output FETs such that the output voltage ramps between $\sim 0.8\%$ and $\sim 1.6\%$ of the nominal PWM output voltage (Figure 44). If the output voltage is below the 'high' PFM comparator threshold, the P1 & P2 (Buck mode) or N2 & P1 (Boost mode) power switches are turned on. It remains on until the output voltage reaches the 'high' PFM threshold or the peak current exceeds the I_{PFM} level set for PFM mode. The typical peak current in PFM mode is: $I_{PFM} = 220 \text{ mA}$

Once the P1 (Buck mode) or N2 (Boost mode) power switch is turned off, the N1 & P2 (Buck mode) or P1 & P2 (Boost mode) power switches are turned on until the inductor current ramps to zero. When the zero inductor current condition is detected, the N1 (Buck mode) or P2 (Boost mode) power switches are turned off. If the output voltage is below the 'high' PFM comparator threshold, the P1 & P2 (Buck mode) or N2 & P1 (Boost mode) switches are again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the 'high' PFM threshold, the N1 & P2 (Buck mode) or P1 & P2 (Boost mode) switches are turned on briefly to ramp the inductor current to zero, then both output switches are turned off and the part enters an extremely low power mode. Quiescent supply current during this 'sleep' mode is $45 \mu\text{A}$ (typ), which allows the part to achieve high efficiency under extremely light load conditions.

Device Functional Modes (continued)

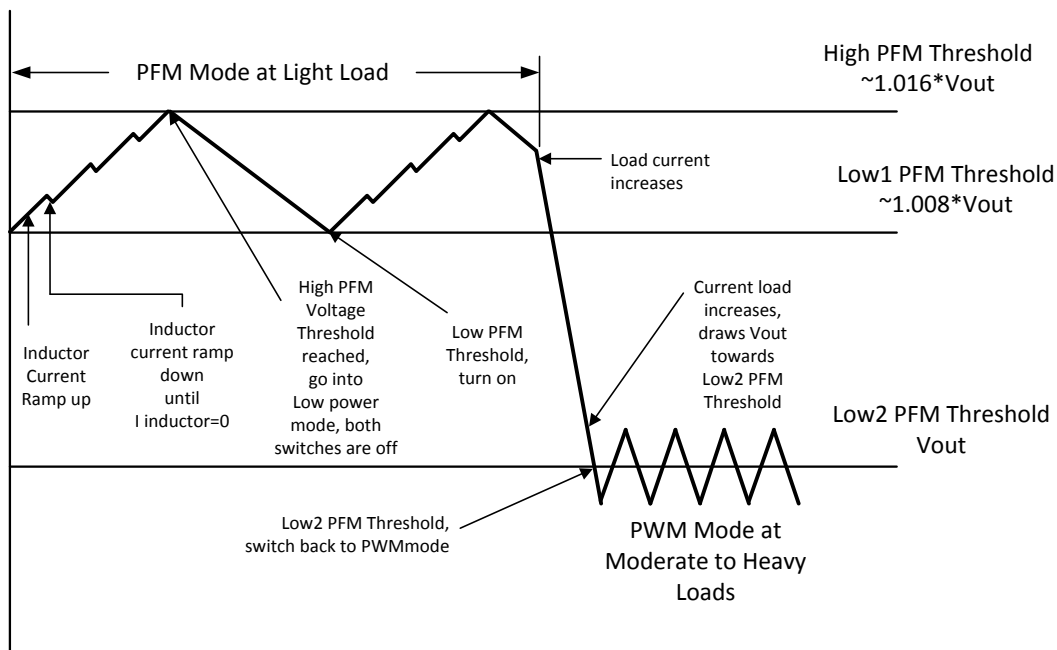


Figure 44. PFM to PWM Mode Transition

In addition to the auto mode transition, the LM3668 operates in PFM Buck or PFM Boost based on the following conditions. There is a small delta (approximately 500 mV) known as $dv1$ (approximately 200 mV) and $dv2$ (approximately 300 mV) when V_{OUT_TARGET} is very close to V_{IN} where the device can be in either Buck or Boost mode. For example, when $V_{OUT_TARGET} = 3.3$ V and V_{IN} is between 3.1 V and 3.6 V, the LM3668 can be in either mode depending on the V_{IN} vs V_{OUT_TARGET} .

- Region I: If $V_{IN} < V_{OUT_TARGET} - dv1$, the regulator operates in Boost mode.
- Region II: If $V_{OUT_TARGET} - dv1 < V_{IN} < V_{OUT_TARGET} + dv2$, the regulator operates in either Buck or Boost mode.
- Region III: If $V_{IN} > V_{OUT_TARGET} + dv2$, the regulator operates in Buck mode.

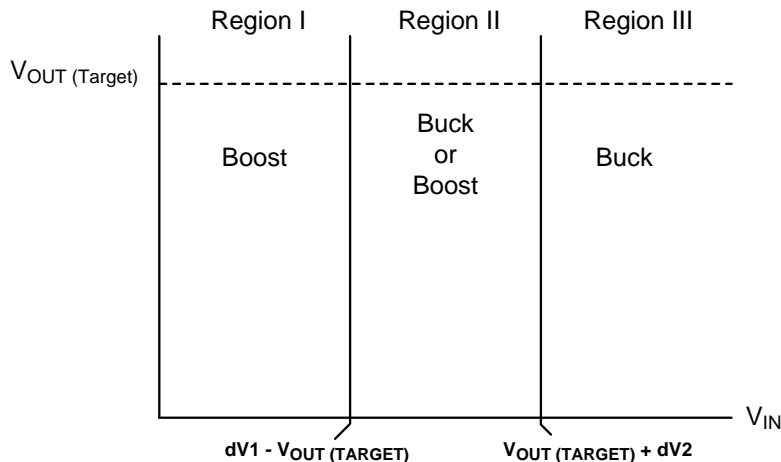


Figure 45. V_{OUT} vs V_{IN} Transition

Device Functional Modes (continued)

In the buck PFM operation, P2 is always turned on and N2 is always turned off, P1 and N1 power switches are switching. P1 and N1 are turned off to enter "sleep mode" when the output voltage reaches the "high" comparator threshold. In boost PFM operation, P2 and N2 are switching. P1 is turned on and N1 is turned off when the output voltage is below the "high" threshold. Unlike in buck mode, all four power switches are turned off to enter "sleep" mode when the output voltage reaches the "high" threshold in boost mode. In addition, the internal current sensing of the I_{PFM} is used to determine the precise condition to switch over to buck or boost mode via the PFM generator.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 MODE/SYNC Pin

If the MODE/SYNC pin is set high, the device is set to operate at PWM mode only. If MODE/SYNC pin is set low, the device is set to automatically transition from PFM to PWM or PWM to PFM depending on the load current. **Do not leave this pin floating.** The MODE/SYNC pin can also be driven by an external clock to set the desired switching frequency between 1.6 MHz to 2.7 MHz.

9.1.2 VSEL Pin

The LM3668 has built in logic for conveniently setting the output voltage, for example if V_{VSEL} high, the output is set to 3.3 V; with V_{VSEL} low the output is set to 2.8 V. It is not recommended to use this function for dynamically switching between 2.8 V and 3.3 V or switching at maximum load.

9.2 Typical Application

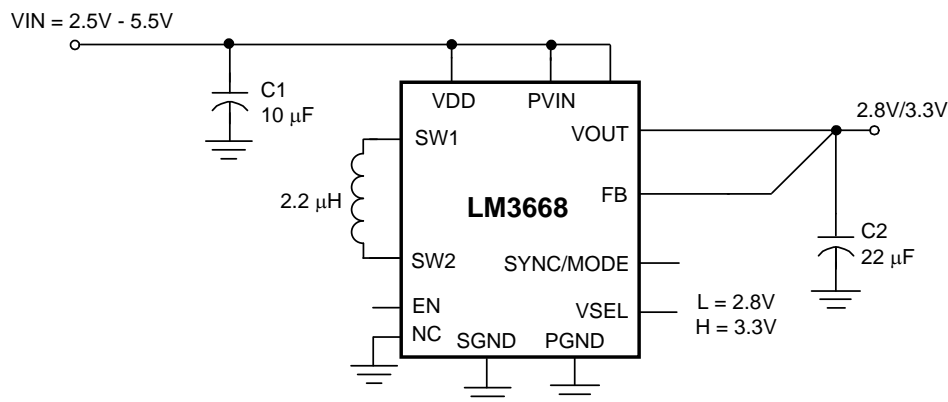


Figure 46. LM3668 Typical Application Circuit

9.2.1 Design Requirements

9.2.1.1 Maximum Current

The LM3668 is designed to operate up to 1 A. For input voltages at 2.5 V, the maximum operating current is 600 mA and 800 mA for 2.7 V input voltage. In any mode it is recommended to avoid starting up the device at minimum input voltage and maximum load. Special attention must be taken to avoid operating near thermal shutdown when operating in boost mode at maximum load (1 A). A simple calculation can be used to determine the power dissipation at the operating condition; $P_{D-MAX} = (T_{J-MAX-OP} - T_{A-MAX})/R_{\theta JA}$. The LM3668 has thermal resistance $R_{\theta JA} = 47.3^{\circ}\text{C/W}$ (see [Thermal Information](#)) and maximum operating ambient of 85°C. As a result, the maximum power dissipation using the above formula is around 845 mW.

Typical Application (continued)

9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection

There are two main considerations when choosing an inductor: the inductor should not saturate, and the inductor current ripple should be small enough to achieve the desired output voltage ripple. Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C. However, ratings at the maximum ambient temperature of application should be requested from the manufacturer. Shielded inductors radiate less noise and should be preferred.

In the case of the LM3668, there are two modes (Buck & Boost) of operation that must be considered when selecting an inductor with appropriate saturation current. The saturation current should be greater than the sum of the maximum load current and the worst case average to peak inductor current. Equation 1 shows the buck mode operation for worst case conditions and the second equation for boost condition.

$$I_{SAT} > I_{OUTMAX} + I_{RIPPLE} \quad \text{For Buck}$$

$$\text{Where } I_{RIPPLE} = \frac{(V_{IN} - V_{OUT})}{(2 \times L \times f)} \times \frac{V_{OUT}}{V_{IN}}$$

$$I_{SAT} > \frac{I_{OUTMAX}}{D'} + I_{RIPPLE} \quad \text{For Boost}$$

$$\text{Where } I_{RIPPLE} = \frac{(V_{OUT} - V_{IN})}{(2 \times L \times f)} \times \frac{V_{IN}}{V_{OUT}}$$

$$\text{Where } D = \frac{(V_{OUT} - V_{IN})}{(V_{OUT})} \quad \& \quad D' = (1-D)$$

where

- I_{RIPPLE} : Peak inductor current
- I_{OUTMAX} : Maximum load current
- V_{IN} : Maximum input voltage in application
- L : Min inductor value including worst case tolerances (30% drop can be considered)
- f : Minimum switching frequency
- V_{OUT} : Output voltage
- D : Duty Cycle for CCM Operation
- V_{OUT} : Output voltage
- V_{IN} : Input voltage

Example using above equations:

- $V_{IN} = 2.8 \text{ V to } 4 \text{ V}$
- $V_{OUT} = 3.3 \text{ V}$
- $I_{OUT} = 500 \text{ mA}$
- $L = 2.2 \mu\text{H}$
- $F = 2 \text{ MHz}$
- Buck: $I_{SAT} = 567 \text{ mA}$
- Boost: $I_{SAT} = 638 \text{ mA}$

(1)

As a result, the inductor should be selected according to the highest of the two I_{SAT} values.

A more conservative and recommended approach is to choose an inductor that has a saturation current rating greater than the maximum current limit of 2.05 A.

Typical Application (continued)

A 2.2- μ H inductor with a saturation current rating of at least 2.05 A is recommended for most applications. The inductor's resistance should be less than 100 m Ω for good efficiency. For low-cost applications, an unshielded bobbin inductor could be considered. For noise critical applications, a toroidal or shielded-bobbin inductor should be used. A good practice is to lay out the board with overlapping footprints of both types for design flexibility. This allows substitution of a low-noise shielded inductor, in the event that noise from low-cost bobbin model is unacceptable.

Table 2. Suggest Inductors and Suppliers

MODEL	VENDOR	DIMENSIONS LxWxH (mm)	D.C.R (m Ω)(MAX)	I _{SAT} (A)
LPS4012-222L	Coilcraft	4 x 4 x 1.2	100	2.1
LPS4018-222L	Coilcraft	4 x 4 x 1.8	70	2.5
1098AS-2R0M (2 μ H)	TOKO	3 x 2.8 x 1.2	67	1.8 (lower current applications)

9.2.2.2 Input Capacitor Selection

A ceramic input capacitor of at least 10 μ F, 6.3 V is sufficient for most applications. Place the input capacitor as close as possible to the PVIN pin of the device. A larger value may be used for improved input voltage filtering. Use X7R or X5R types; do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 or 0603. The input filter capacitor supplies current to the PFET switch of the LM3668 in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. For applications where input voltage is 4 V or higher, it is best to use a higher voltage rating capacitor to eliminate the DC bias affect over capacitance.

9.2.2.3 Output Capacitor Selection

A ceramic output capacitor of 22 μ F, 6.3 V (use 10 V or higher rating for 4.5 V-5 V output option) is sufficient for most applications. Multilayer ceramic capacitors such as X7R or X5R with low ESR is a good choice for this as well. These capacitors provide an ideal balance between small size, cost, reliability and performance. Do not use Y5V ceramic capacitors as they have temperature limitation and poor dielectric performance over temperature and poor voltage characteristic for a given value. In other words, ensure the minimum C_{OUT} value does not exceed -40% of the above-suggested value over the entire range of operating temperature and bias conditions.

Extra attention is required if a smaller case size capacitor is used in the application. Smaller case size capacitors typically have less capacitance for a given bias voltage as compared to a larger case size capacitor with the same bias voltage. Please contact the capacitor manufacturer for detailed information regarding capacitance verses case size. [Table 3](#) lists several capacitor suppliers.

The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

Note that the output voltage ripple is dependent on the inductor current ripple and the equivalent series resistance of the output capacitor (R_{ESR}).

The R_{ESR} is frequency dependent (as well as temperature dependent); make sure the value used for calculations is at the switching frequency of the part.

Table 3. Suggested Capacitors and Suppliers

MODEL	TYPE	VENDOR	VOLTAGE RATING (V)	CASE SIZE INCH (mm)
10 μF FOR C_{IN} (FOR 4.5/5 V OPTION, USE 10 V OR HIGHER RATING CAPACITOR)				
GRM21BR60J106K	Ceramic, X5R	Murata	6.3	0805 (2012)
JMK212BJ106K	Ceramic, X5R	Taiyo-Yuden	6.3	0805 (2012)
C2012X5R0J106K	Ceramic, X5R	TDK	6.3	0805 (2012)
LMK212 BJ106MG (\pm 20%)	Ceramic, X5R	Taiyon-Yuden	10	0806(2012)

Table 3. Suggested Capacitors and Suppliers (continued)

MODEL	TYPE	VENDOR	VOLTAGE RATING (V)	CASE SIZE INCH (mm)
LMK212 BJ106KG ($\pm 10\%$)	Ceramic, X5R	Taiyon-Yuden	10	0805(2012)
22 μF FOR C_{OUT} (FOR 4.5/5 V OPTION, USE 10 V OR HIGHER RATING CAPACITOR)				
JMK212BJ226MG	Ceramic, X5R	Taiyo-Yuden	6.3	0805 (2012)
LMK212BJ226MG	Ceramic, X5R	Taiyo-Yuden	10	0805 (2012)

9.2.3 Application Curves

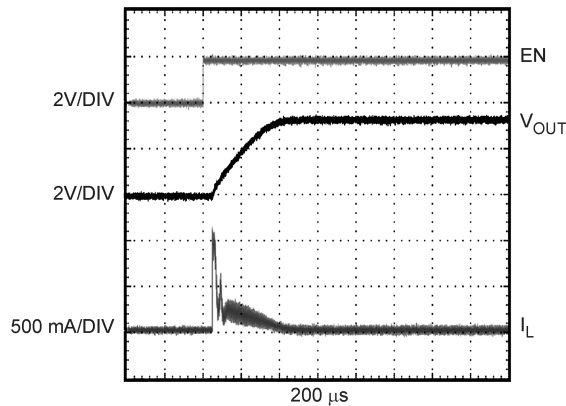


Figure 47. Start-Up in PWM Mode ($V_{\text{OUT}} = 3.4 \text{ V}$, Load = 1 mA)

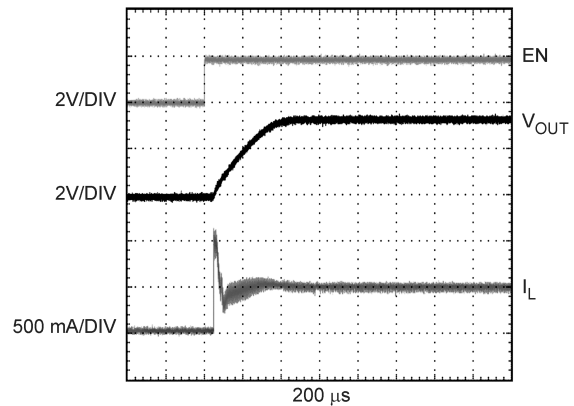


Figure 48. Start-Up in PWM Mode ($V_{\text{OUT}} = 3.4 \text{ V}$, Load = 500 mA)

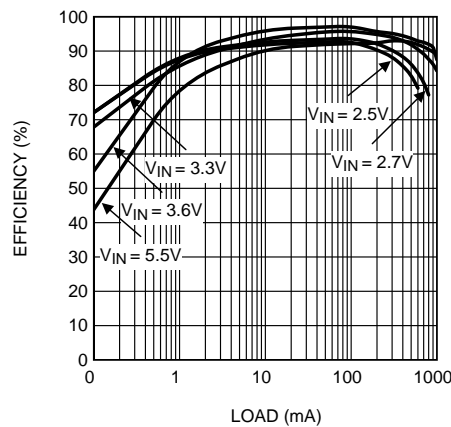


Figure 49. Efficiency at 3.3 V Output

10 Power Supply Recommendations

The power supply for the applications using the LM3668 device should be big enough considering output power and efficiency at given input voltage condition. Minimum current requirement condition is $(V_{OUT} \times I_{OUT}) / (V_{IN} \times \text{efficiency})$ and approximately 20 to 30% higher than this value is recommended.

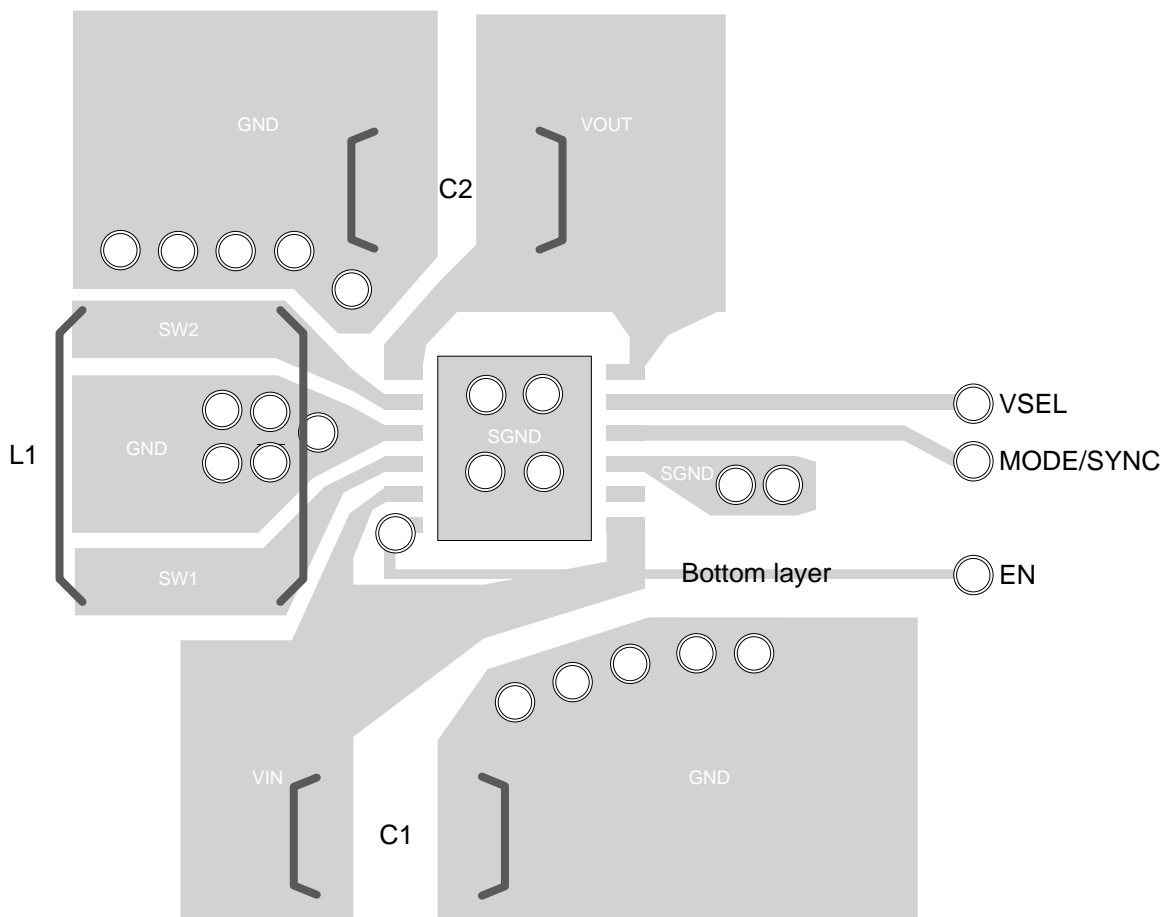
11 Layout

11.1 Layout Guidelines

As for any high frequency switcher, it is important to place the external components as close as possible to the IC to maximize device performance. Below are some layout recommendations:

1. Place input filter and output filter capacitors close to the IC to minimize copper trace resistance which will directly effect the overall ripple voltage.
2. Route noise sensitive trace away from noisy power components. Separate power GND (Noisy GND) and Signal GND (quiet GND) and star GND them at a single point on the PCB preferably close to device GND.
3. Connect the ground pins and filter capacitors together via a ground plane to prevent switching current circulating through the ground plane. Additional layout consideration regarding the WSON package can be found in AN-1187 *Leadless Leadframe Package (LLP)*, [SNOA401](#).

11.2 Layout Example



12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.1.2 Documentation Support

12.1.2.1 *Related Documentation*

TI Application Note AN-1187 *Leadless Leadframe Package (LLP) (SNOA401)*.

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3668SD-2833/NOPB	NRND	WSO	DQB	12	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		S017B	
LM3668SD-3034/NOPB	NRND	WSO	DQB	12	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	S018B	
LM3668SD-4550/NOPB	NRND	WSO	DQB	12	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	S019B	
LM3668SDX-2833/NOPB	NRND	WSO	DQB	12	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		S017B	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LM3668 :

- Automotive: [LM3668-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

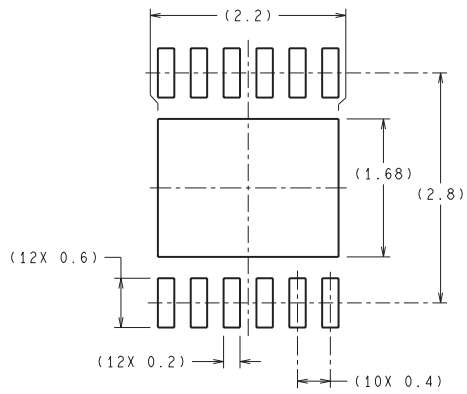
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3668SD-2833/NOPB	WSON	DQB	12	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM3668SD-3034/NOPB	WSON	DQB	12	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM3668SD-4550/NOPB	WSON	DQB	12	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM3668SDX-2833/NOPB	WSON	DQB	12	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

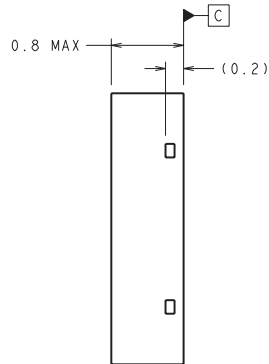
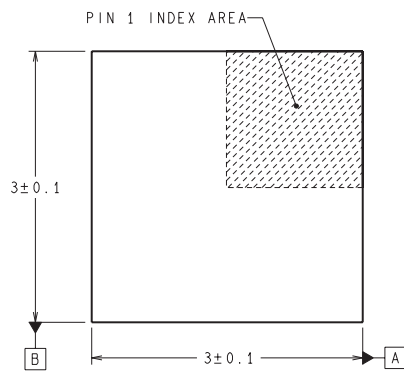

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3668SD-2833/NOPB	WSON	DQB	12	1000	210.0	185.0	35.0
LM3668SD-3034/NOPB	WSON	DQB	12	1000	210.0	185.0	35.0
LM3668SD-4550/NOPB	WSON	DQB	12	1000	210.0	185.0	35.0
LM3668SDX-2833/NOPB	WSON	DQB	12	4500	367.0	367.0	35.0

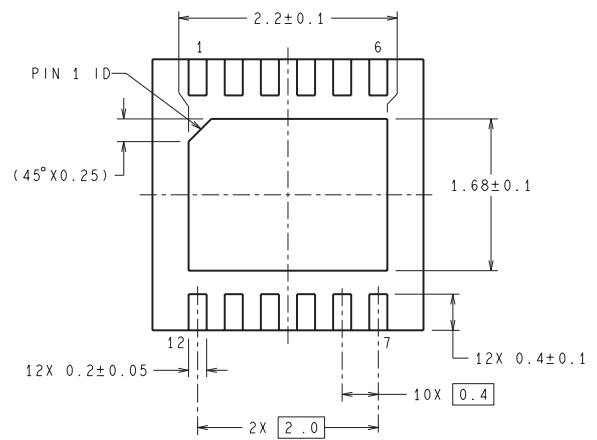
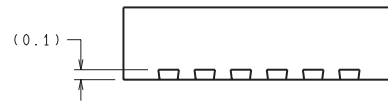
DQB0012A



RECOMMENDED LAND PATTERN



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY



SDF12A (Rev B)

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