THE DATASHEET OF

LM3670MFX-ADJ

LM3670 Miniature Step-Down DC-DC Converter for Ultralow Voltage Circuits

1 Features

- Input Voltage Range: 2.5 V to 5.5 V
- Adjustable Output Voltages (V_{OUT}): 0.7 V to 2.5 V
- Fixed Output Voltages: 1.2 V, 1.5 V, 1.6 V, 1.8 V, 1.875 V, 3.3V
- 15-µA Typical Quiescent Current
- 350-mA Maximum Load Capability
- 1-MHz PWM Fixed Switching Frequency (Typical)
- Automatic PFM and PWM Mode Switching
- Low Dropout Operation – 100% Duty Cycle Mode
- Internal Synchronous Rectification for High Efficiency
- Internal Soft Start
- 0.1-µA Typical Shutdown Current
- Current Overload Protection
- Operates from a Single Li-Ion Cell or Three-Cell NiMH/NiCd Batteries
- Only Three Tiny Surface-Mount External Components Required (One Inductor, Two Ceramic Capacitors)

2 Applications

- Mobile Phones and Handheld Devices
- PDAs
- Palm-Top PCs
- Portable Instruments
- Battery-Powered Devices

3 Description

The LM3670 step-down DC-DC converter is optimized for powering ultralow voltage circuits from a single Li-Ion cell or three-cell NiMH/NiCd batteries. It provides up to 350-mA load current, over an input voltage range from 2.5 V to 5.5 V. There are several different fixed voltage output options available as well as an adjustable output voltage version.

The device offers superior features and performance for mobile phones and similar portable applications with complex power management systems. Automatic intelligent switching between pulse width modulation (PWM) low-noise and pulse frequency modulation (PFM) low-current mode offers improved system control. During full-power operation, a fixed-frequency 1-MHz (typical) PWM mode drives loads from approximately 70 mA to 350 mA maximum, with up to 95% efficiency. Hysteretic PFM mode extends the battery life through reduction of the quiescent current to 15 µA (typical) during light current loads and system standby. Internal synchronous rectification provides high efficiency (90% to 95% typical at loads between 1 mA and 100 mA). In shutdown mode (enable (EN) pin pulled low) the device turns off and reduces battery consumption to 0.1 µA (typical).

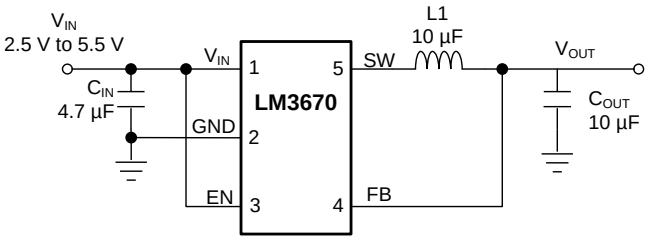
The LM3670 is available in a 5-pin SOT-23 package. A high switching frequency (1 MHz typical) allows use of tiny surface-mount components. Only three external surface-mount components, an inductor and two ceramic capacitors, are required.

Device Information(1)

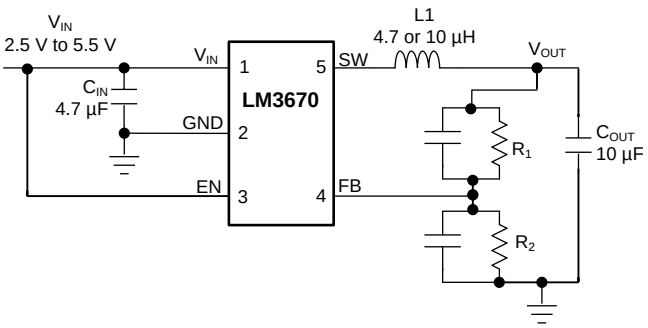
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM3670	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application: Fixed Output



Typical Application: Adjustable Output Voltage



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (February 2013) to Revision F — **Page**

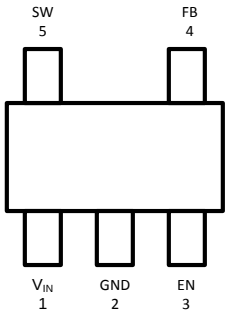
- Changed "(0.7V min) to "0.7 V to 2.5 V" ... 1
- Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* and *Thermal Information* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Deleted phone and fax numbers of manufacturers from suggested inductors table ... 15
- Deleted phone and fax numbers of manufacturers from suggested capacitors table ... 16
- Deleted rest of text from paragraph beginning "For any output voltages...." ... 17
- Deleted row beginning with "1.24... "from Table 3 ... 18

Changes from Revision D (February 2013) to Revision E — **Page**

- Changed layout of National Data Sheet to TI format ... 19

5 Connection Diagram

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
1	V_{IN}	Power	Power supply input. Connect to the input filter capacitor (*Typical Application: Fixed Output*).
2	GND	Ground	Ground pin.
3	EN	Digital	Enable input.
4	FB	Analog	Feedback analog input. Connect to the output filter capacitor (*Typical Application: Fixed Output*).
5	SW	Analog	Switching node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the 750-mA maximum switch peak current limit specification.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
V_{IN} pin: voltage to GND	–0.2	6	V
EN pin: voltage to GND	–0.2	6	V
FB, SW pins	(GND −0.2)	V_{IN} + 0.2	V
Junction temperature, $T_{J\text{-}MAX}$	–45	125	°C
Maximum lead temperature (soldering, 10 seconds)		260	°C
Storage temperature, T_{stg}	–45	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the TI Sales Office/Distributors for availability and specifications.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	NOM	MAX	UNIT
Input voltage	2.5		5.5	A
Recommended load current	0		350	mA
Junction temperature, T_J	–40		125	°C
Ambient temperature, T_A	–40		85	°C

(1) All voltages are with respect to the potential at the GND pin.

6.4 Thermal Information

THERMAL METRIC(1)		LM3670 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	163.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	114.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise specified, limits for typical values are T_J = 25°C, and minimum and maximum limits apply over the full operating junction temperature range (−40°C ≤ T_J ≤ +125°C); V_{IN} = 3.6 V, V_{OUT} = 1.8 V, I_{OUT} = 150 mA, EN = V_{IN}.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	See (1)	2.5		5.5	V
V_{OUT}	Fixed output voltage: 1.2 V	2.5 V ≤ V_{IN} ≤ 5.5 V I_{OUT} = 10 mA	–2%		4%	
		2.5 V ≤ V_{IN} ≤ 5.5 V 0 mA ≤ I_{OUT} ≤ 150 mA	–4.5%		4%	
	Fixed output voltage: 1.5 V	2.5 V ≤ V_{IN} ≤ 5.5 V I_{OUT} = 10 mA	–2.5%		4%	
		2.5 V ≤ V_{IN} ≤ 5.5 V 0 mA ≤ I_{OUT} ≤ 350 mA	–5%		4%	
	Fixed output voltage: 1.6 V, 1.875 V	2.5 V ≤ V_{IN} ≤ 5.5 V I_{OUT} = 10 mA	–2.5%		4%	
		2.5 V ≤ V_{IN} ≤ 5.5V 0 mA ≤ I_{OUT} ≤ 350 mA	–5.5%		4%	
	Fixed output voltage: 1.8 V	2.5 V ≤ V_{IN} ≤ 5.5 V I_{OUT} = 10 mA	–1.5%		3%	
		2.5 V ≤ V_{IN} ≤ 5.5 V 0 mA ≤ I_{OUT} ≤ 350 mA	–4.5%		3%	
	Fixed output voltage: 3.3 V	3.6 V ≤ V_{IN} ≤ 5.5 V I_{OUT} = 10 mA	–2%		4%	
		3.6V ≤ V_{IN} ≤ 5.5V 0 mA ≤ I_{OUT} ≤ 350 mA	–6%		4%	
	Adjustable output voltage (2)	2.5 V ≤ V_{IN} ≤ 5.5 V I_{OUT} = 10 mA	–2.5%		4.5%	
		2.5 V ≤ V_{IN} ≤ 5.5 V 0 mA ≤ I_{OUT} ≤ 150 mA	–4%		4.5%	
Line_reg	Line regulation	2.5 V ≤ V_{IN} ≤ 5.5 V I_{OUT} = 10 mA		0.26		%/V
Load_reg	Load regulation	150 mA ≤ I_{OUT} ≤ 350 mA		0.0014		%/mA
V_{REF}	Internal reference voltage			0.5		V
I_{Q_SHDN}	Shutdown supply current	T_A = 85ºC		0.1	1	µA
I_Q	DC bias current into V_{IN}	No load, device is not switching (V_{OUT} forced higher than programmed output voltage)		15	30	µA
V_{UVLO}	Minimum V_{IN} below which V_{OUT} is disabled	T_A = −40°C ≤ T_J ≤ 125°C		2.4		V
$R_{DSON\ (P)}$	Pin-pin resistance for PFET	V_{IN} = V_{GS}= 3.6V		360	690	mΩ
$R_{DSON\ (N)}$	Pin-pin resistance for NFET	V_{IN} = V_{GS}= 3.6 V		250	660	mΩ
$I_{LKG\ (P)}$	P channel leakage current	V_{DS} = 5.5 V, T_A = 25°C		0.1	1	µA
$I_{LKG\ (N)}$	N channel leakage current	V_{DS} = 5.5 V, T_A = 25°C		0.1	1.5	µA
I_{LIM}	Switch peak current limit		400	620	750	mA

(1) The input voltage range recommended for the specified output voltages are given below: V_{IN} = 2.5 V to 5.5 V for 0. 7 V ≤ V_{OUT} < 1.875 V, V_{IN} = (V_{OUT} + $V_{DROPOUT}$) to 5.5 for 1.875 ≤ V_{OUT} ≤ 3.3 V, where $V_{DROPOUT}$ = I_{LOAD} × ($R_{DSON\ (P)}$ + $R_{INDUCTOR}$).
(2) Output voltage specification for the adjustable version includes tolerance of the external resistor divider.

Electrical Characteristics (continued)

Unless otherwise specified, limits for typical values are T_J = 25°C, and minimum and maximum limits apply over the full operating junction temperature range (−40°C ≤ T_J ≤ +125°C); V_{IN} = 3.6 V, V_{OUT} = 1.8 V, I_{OUT} = 150 mA, EN = V_{IN}.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
η	Efficiency	V_{IN} = 3.6 V, V_{OUT} = 1.8 V I_{LOAD} = 1 mA		91%		
		V_{IN} = 3.6 V, V_{OUT} = 1.8 V I_{LOAD} = 10 mA		94%		
		V_{IN} = 3.6 V, V_{OUT} = 1.8 V I_{LOAD} = 100 mA		94%		
		V_{IN} = 3.6 V, V_{OUT} = 1.8 V I_{LOAD} = 200 mA		94%		
		V_{IN} = 3.6 V, V_{OUT} = 1.8 V I_{LOAD} = 300 mA		92%		
		V_{IN} = 3.6 V, V_{OUT} = 1.8 V I_{LOAD} = 350 mA		90%		
V_{IH}	Logic high input		1.3			V
V_{IL}	Logic low input				0.4	V
I_{EN}	Enable (EN) input current			0.01	1	µA
f_{OSC}	Internal oscillator frequency	PWM mode	550	1000	1300	kHz

6.6 Typical Characteristics

Unless otherwise stated, V_{IN} = 3.6 V and V_{OUT}= 1.8 V.

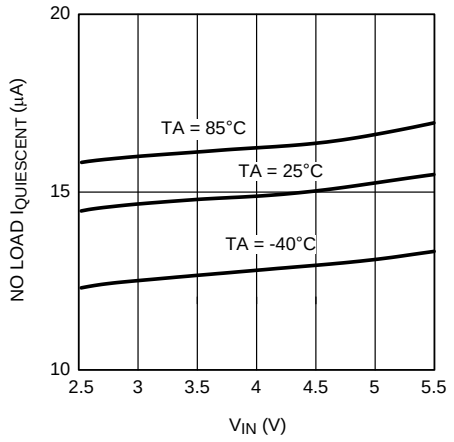


Figure 1. I_Q (Non-Switching) vs V_{IN}

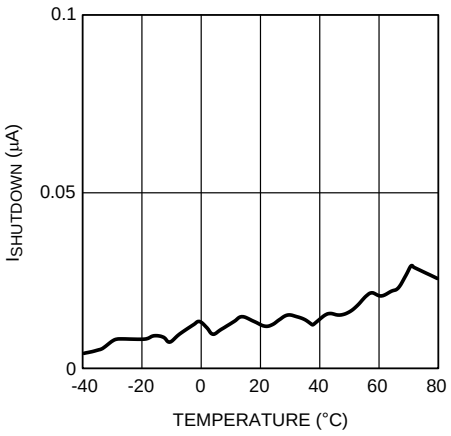


Figure 2. I_Q vs Temperature

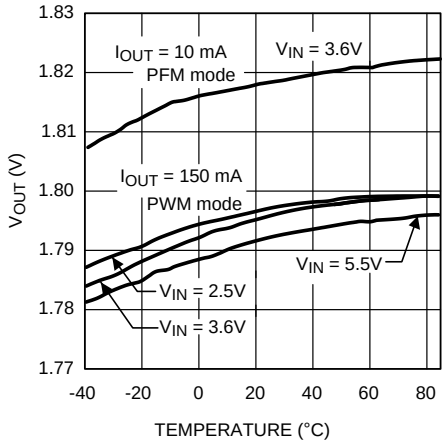


Figure 3. V_{OUT} vs V_{IN}

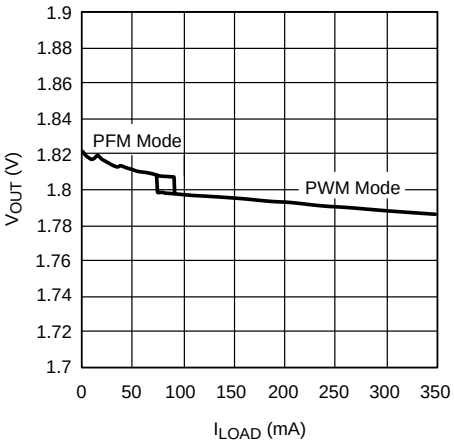


Figure 4. V_{OUT} vs I_{OUT}

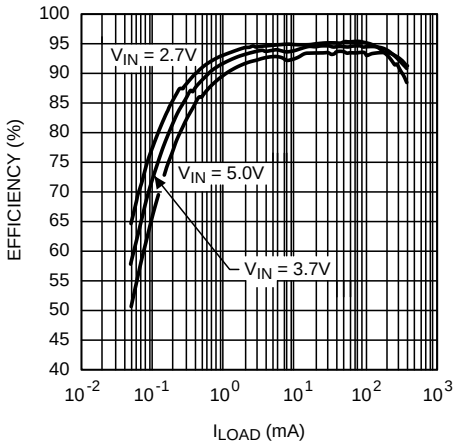


Figure 5. Efficiency vs I_{OUT}

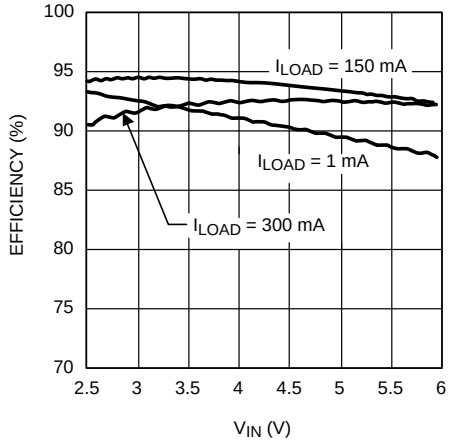


Figure 6. Efficiency vs V_{IN}

Typical Characteristics (continued)

Unless otherwise stated, V_{IN} = 3.6 V and V_{OUT}= 1.8 V.

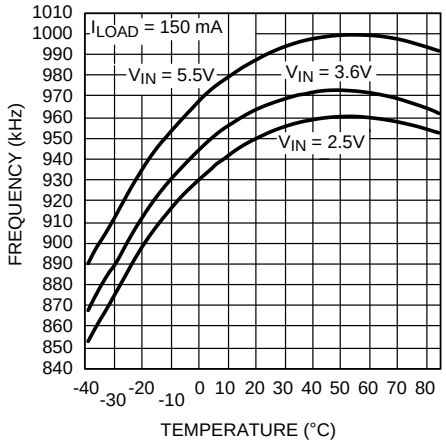


Figure 7. Frequency vs Temperature

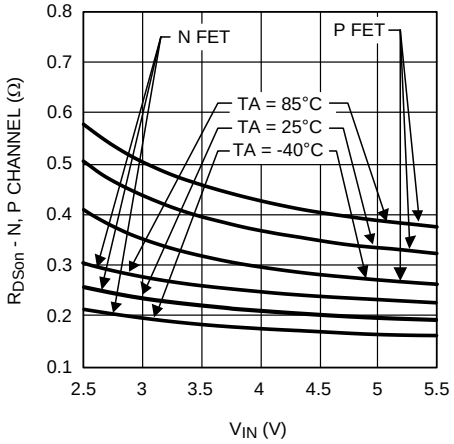
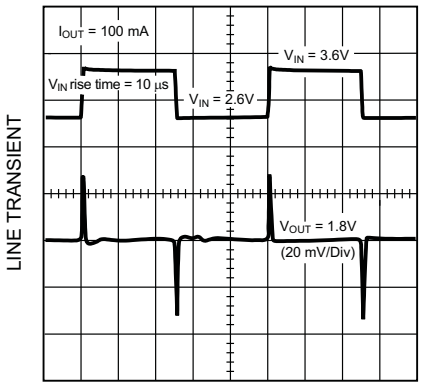
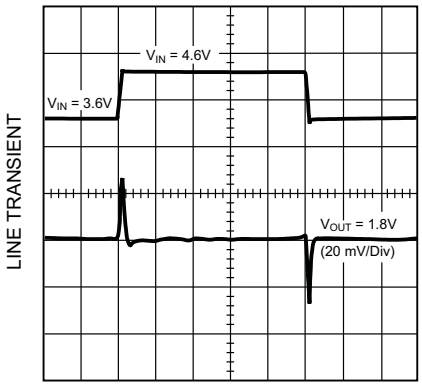


Figure 8. R_{DSON} vs. V_{IN} P and N Channels



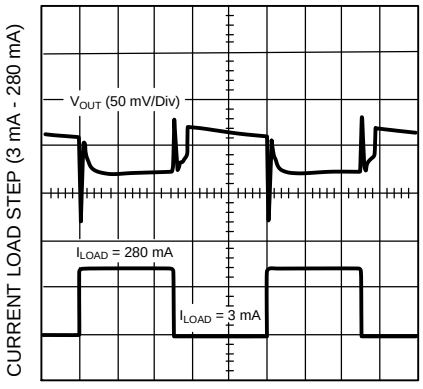
V_{IN} = 2.6 V to 3.6 V I_{LOAD} = 100 mA

Figure 9. Line Transient



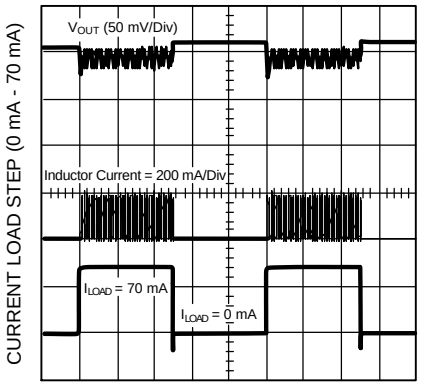
V_{IN} = 3.6 V to 4.6 V I_{LOAD} = 100 mA

Figure 10. Line Transient



I_{LOAD} = 3 mA to 280 mA

Figure 11. Load Transient



I_{LOAD} = 0 mA to 70 mA

Figure 12. Load Transient

Typical Characteristics (continued)

Unless otherwise stated, V_{IN} = 3.6 V and V_{OUT}= 1.8 V.

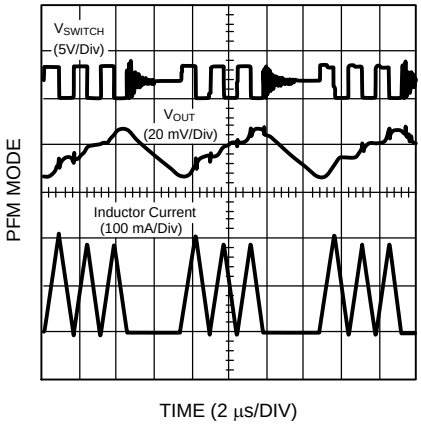


Figure 13. PFM Mode V_{SW}, V_{OUT}, $I_{INDUCTOR}$ vs Time

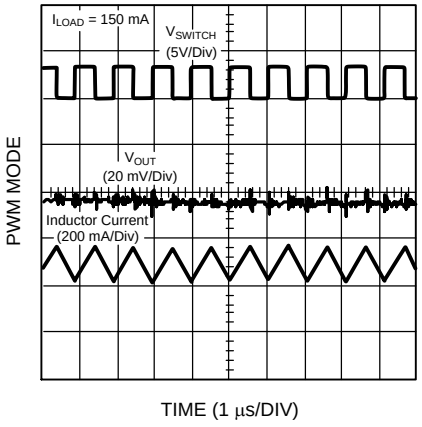
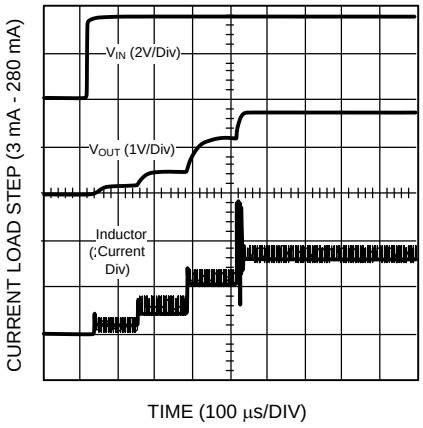


Figure 14. PWM Mode V_{SW}, V_{OUT}, $I_{INDUCTOR}$ vs Time



I_{LOAD} = 350 mA

Figure 15. Soft Start V_{IN}, V_{OUT}, $I_{INDUCTOR}$ vs Time

7 Detailed Description

7.1 Overview

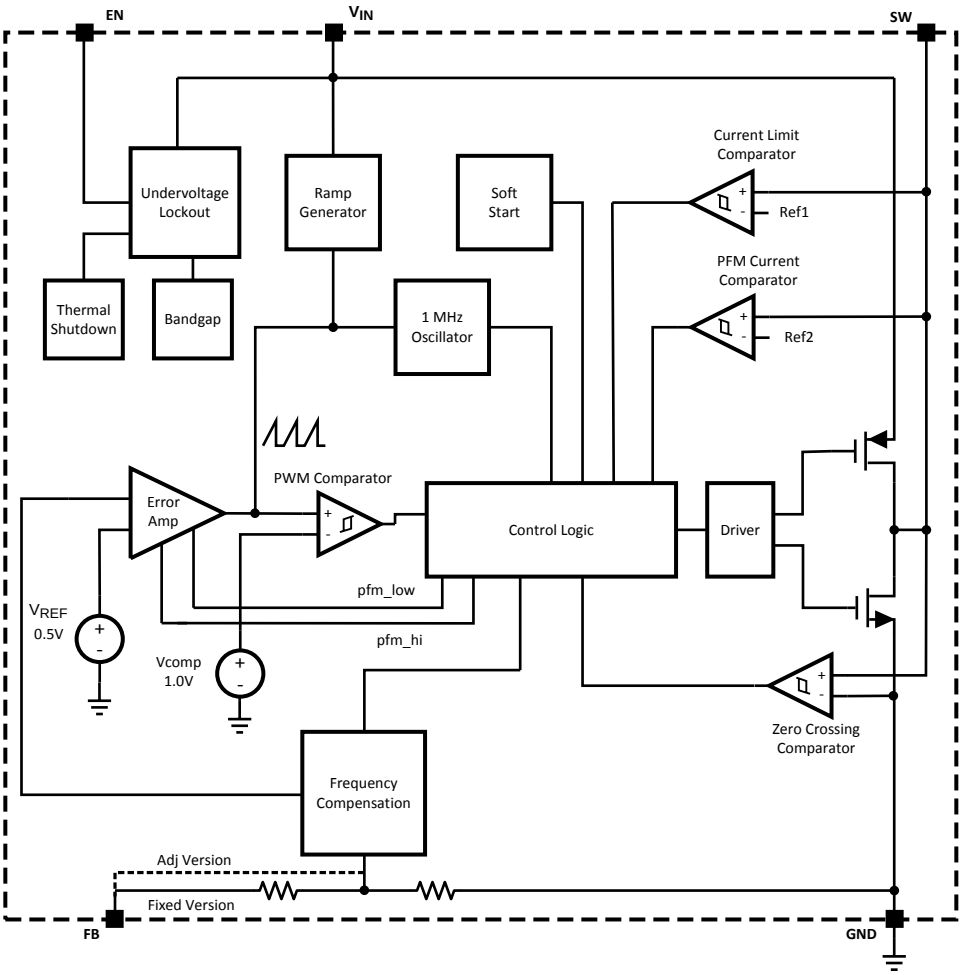
The LM3670, a high-efficiency step-down DC-DC switching buck converter, delivers a constant voltage from either a single Li-Ion or three-cell NiMH/NiCd battery to portable devices such as cell phones and PDAs. Using a voltage mode architecture with synchronous rectification, the LM3670 can deliver up to 350 mA depending on the input voltage and output voltage (voltage head room), and the inductor chosen (maximum current capability).

There are three modes of operation depending on the current required: pulse width modulation (PWM), pulse frequency modulation (PFM), and shutdown. PWM mode handles current loads of approximately 70 mA or higher. Lighter output current loads cause the device to automatically switch into PFM for reduced current consumption (I_Q = 15 µA typical) and a longer battery life. Shutdown mode turns off the device, offering the lowest current consumption ($I_{SHUTDOWN}$ = 0.1 µA typical).

The LM3670 can operate up to a 100% duty cycle (PMOS switch always on) for low dropout control of the output voltage. In this way the output voltage is controlled down to the lowest possible input voltage.

Additional features include soft-start, undervoltage lockout, current overload protection, and thermal overload protection. As shown in Figure 17, only three external power components are required for implementation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Circuit Operation

The LM3670 operates as follows. During the first portion of each switching cycle, the control block in the LM3670 turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of:

$$\frac{V_{IN}-V_{OUT}}{L} \quad (1)$$

by storing energy in a magnetic field. During the second portion of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of:

$$\frac{-V_{OUT}}{L} \quad (2)$$

The output filter stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

7.3.2 Soft Start

The LM3670 has a soft-start circuit that limits in-rush current during start-up. Typical start-up times with a 10-µF output capacitor and 350-mA load is 400 µs:

Table 1. Typical Start-Up Times for Soft Start

INRUSH CURRENT (mA)	DURATION (µs)
0	32
70	224
140	256
280	256
620	until soft start ends

7.3.3 LDO - Low Dropout Operation

The LM3670 can operate at 100% duty cycle (no switching, PMOS switch is completely on) for low dropout support of the output voltage. In this way the output voltage is controlled down to the lowest possible input voltage.

The minimum input voltage needed to support the output voltage is

$$V_{IN\_MIN} = I_{LOAD} \times (R_{DSON,PFET} + R_{INDUCTOR}) + V_{OUT} \quad (3)$$

where

- I_{LOAD} = load current
- $R_{DSON,\ PFET}$ = the drain to source resistance of PFET switch in the triode region
- $R_{INDUCTOR}$ = the inductor resistance

7.4 Device Functional Modes

7.4.1 PWM Operation

During PWM operation the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve excellent load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward inversely proportional to the input voltage is introduced.

7.4.1.1 Internal Synchronous Rectification

While in PWM mode, the LM3670 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

7.4.1.2 Current Limiting

A current limit feature allows the LM3670 to protect itself and external components during overload conditions PWM mode implements cycle-by-cycle current limiting using an internal comparator that trips at 620 mA (typical).

7.4.2 PFM Operation

At very light load, the converter enters PFM mode and operates with reduced switching frequency and supply current to maintain high efficiency.

The part automatically transition into PFM mode when either of two conditions occurs for a duration of 32 or more clock cycles:

1. The inductor current becomes discontinuous
2. The peak PMOS switch current drops below the I_{MODE} level:

$$I_{MODE} < 26\ mA + \frac{V_{IN}}{50\Omega}\ (typ) \tag{4}$$

During PFM operation, the converter positions the output voltage slightly higher than the nominal output voltage in PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparator senses the output voltage via the feedback pin and control the switching of the output FETs such that the output voltage ramps between 0.8% and 1.6% (typical) above the nominal PWM output voltage. If the output voltage is below the *high* PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage exceeds the 'high' PFM threshold or the peak current exceeds the I_{PFM} level set for PFM mode. The peak current in PFM mode is:

$$I_{PFM\ Peak} = 117\ mA + \frac{V_{IN}}{64\Omega}\ (typ) \tag{5}$$

Once the PMOS power switch is turned off, the NMOS power switch is turned on until the inductor current ramps to zero. When the NMOS zero-current condition is detected, the NMOS power switch is turned off. If the output voltage is below the *high* PFM comparator threshold (see Figure 16), the PMOS switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the *high* PFM threshold, the NMOS switch is turned on briefly to ramp the inductor current to zero and then both output switches are turned off and the part enters an extremely low power mode. Quiescent supply current during this sleep mode is less than 30 µA, which allows the part to achieve high efficiencies under extremely light load conditions. When the output drops below the low PFM threshold, the cycle repeats to restore the output voltage to approximately 1.6% above the nominal PWM output voltage.

If the load current increases during PFM mode (see Figure 16) causing the output voltage to fall below the 'low2' PFM threshold, the part automatically transitions into fixed-frequency PWM mode.

Device Functional Modes (continued)

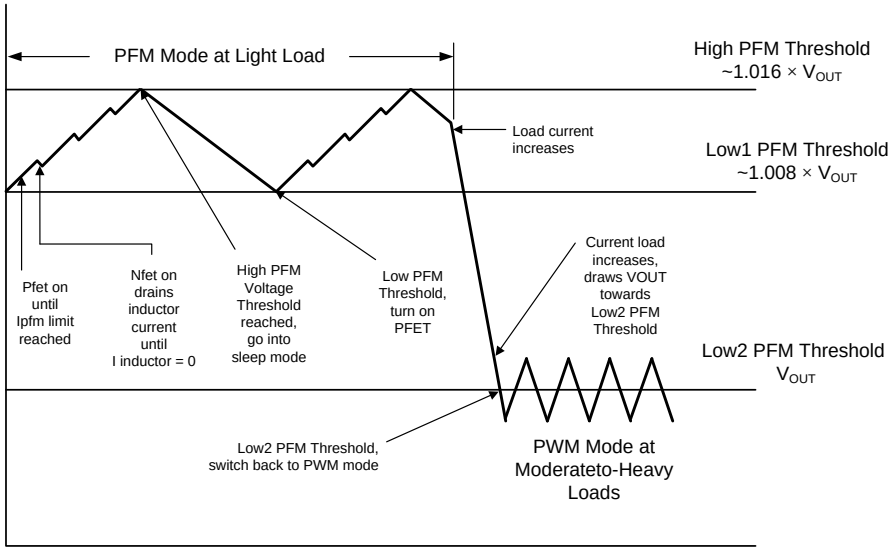


Figure 16. Operation in PFM Mode and Transition to PWM Mode

7.4.3 Shutdown

Setting the EN input pin low (< 0.4 V) places the LM3670 in shutdown mode. During shutdown the PFET switch, NFET switch, reference, control and bias circuitry of the LM3671 are turned off. Setting EN high (> 1.3 V) enables normal operation. It is recommended to set EN pin low to turn off the LM3671 during system power up and undervoltage conditions when the supply is less than 2.5 V. Do not leave the EN pin floating.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The external control of this device is very easy. First make sure the correct voltage been applied at V_{IN} pin, then simply apply the voltage at EN pin according to the *Electrical Characteristics* to enable or disable the output voltage.

8.2 Typical Application

8.2.1 Typical Application: Fixed Output

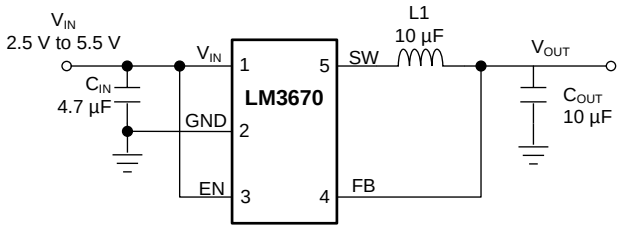


Figure 17. LM3670 Typical Application, Fixed Output

8.2.1.1 Design Requirements

For typical CMOS voltage regulator applications, use the parameters listed in Table 2.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	2.5 V
Minimum output voltage	1.2 V
Maximum load current	350 mA

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Inductor Selection

There are two main considerations when choosing an inductor: the inductor current must not saturate, and the inductor current ripple is small enough to achieve the desired output voltage ripple.

There are two methods to choose the inductor current rating.

8.2.1.2.1.1 Method 1

The total current is the sum of the load and the inductor ripple current. This can be written as

$$I_{MAX} = I_{LOAD} + \frac{I_{RIPPLE}}{2} \tag{6}$$

$$V_{OUT} = I_{LOAD} + \left(\frac{V_{IN}-V_{OUT}}{2*L}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{1}{f}\right)$$

where

- I_{LOAD} = load current
- V_{IN} = input voltage

- L = inductor
- f = switching frequency
- I_{RIPPLE} = peak-to-peak current (7)

8.2.1.2.1.2 Method 2

A more conservative approach is to choose an inductor that can handle the current limit of 700 mA.

Given a peak-to-peak current ripple (I_{PP}) the inductor needs to be at least

$$L >= \left(\frac{V_{IN} - V_{OUT}}{I_{PP}}\right) * \left(\frac{V_{OUT}}{V_{IN}}\right) * \left(\frac{1}{f}\right) \quad (8)$$

A 10-µH inductor with a saturation current rating of at least 800 mA is recommended for most applications. Resistance of the inductor resistance must be less than around 0.3 Ω for good efficiency. Table 3 lists suggested inductors and suppliers. For low-cost applications, an unshielded bobbin inductor is suggested. For noise critical applications, a toroidal or shielded-bobbin inductor must be used. A good practice is to lay out the board with overlapping footprints of both types for design flexibility. This allows substitution of a low-noise toroidal inductor, in the event that noise from low-cost bobbin models is unacceptable.

8.2.1.2.2 Input Capacitor Selection

A ceramic input capacitor of 4.7 µF is sufficient for most applications. A larger value may be used for improved input voltage filtering. The input filter capacitor supplies current to the PFET switch of the LM3670 in the first half of each cycle and reduces voltage ripple imposed on the input power source. The low equivalent series resistance (ESR) of a ceramic capacitor provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select an input filter capacitor with a surge current rating sufficient for the power-up surge from the input power source. The power-up surge current is approximately the value of the capacitor (µF) times the voltage rise rate (V/µs). The input current ripple can be calculated by :

$$I_{RMS} = I_{OUTMAX} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst case IRMS is:

$$IRMS = \frac{IRMS}{2} \qquad \text{(duty cycle = 50\%)} \quad (9)$$

Table 3. Suggested Inductors and Their Suppliers

MODEL	VENDOR
IDC2512NB100M	Vishay
DO1608C-103	Coilcraft
ELL6RH100M	Panasonic
CDRH5D18-100	Sumida

8.2.1.2.3 Output Capacitor Selection

The output filter capacitor smooths out current flow from the inductor to the load, maintaining a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

The output ripple current can be calculated as:

Voltage peak-to-peak ripple due to capacitance = $V_{PP\text{-}C} = \frac{I_{PP}}{f*8*C}$

Voltage peak-to-peak ripple due to ESR = $V_{OUT} = V_{PP\text{-}ESR} = I_{PP} * R_{ESR}$

Voltage peak-to-peak ripple, root mean squared = $V_{PP\text{-}RMS} = \sqrt{V_{PP\text{-}C}^2 + V_{PP\text{-}ESR}^2}$

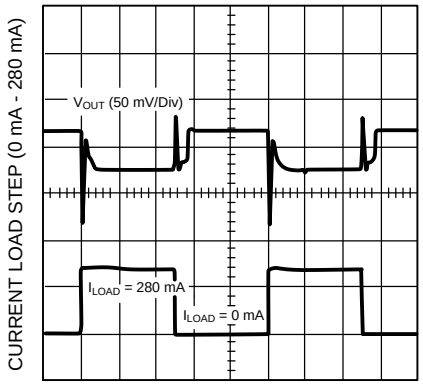
Note that the output ripple is dependent on the current ripple and the equivalent series resistance of the output capacitor (R_{ESR}).

Because these two components are out-of-phase the RMS value is used. The R_{ESR} is frequency dependent (as well as temperature dependent); make sure the frequency of the R_{ESR} given is the same order of magnitude as the switching frequency.

Table 4. Suggested Capacitors And Their Suppliers

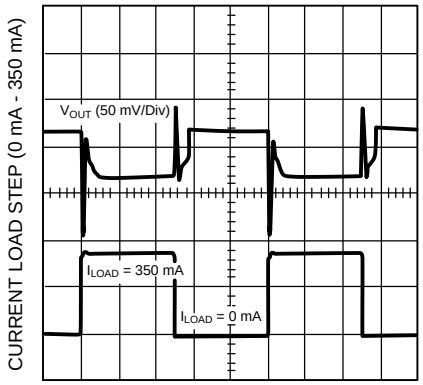
MODEL	TYPE	VENDOR
10 µF for C_{OUT}		
VJ1812V106MXJAT	Ceramic	Vishay
LMK432BJ106MM	Ceramic	Taiyo-Yuden
JMK325BJ106MM	Ceramic	Taiyo-Yuden
4.7 µF for C_{IN}		
VJ1812V475MXJAT	Ceramic	Vishay
EMK325BJ475MN	Ceramic	Taiyo-Yuden
C3216X5R0J475M	Ceramic	TDK

8.2.1.3 Application Curves



I_{LOAD} = 0 mA to 280 mA

Figure 18. Load Transient



I_{LOAD} = 0 mA to 350 mA

Figure 19. Load Transient

8.2.2 Typical Application: Adjustable Output

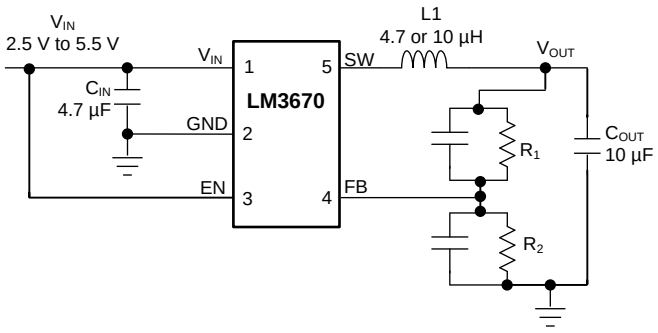


Figure 20. LM3670 Typical Application: Adjustable Output

8.2.2.1 Design Requirements

For adjustable LM3670 option, use the design parameters in Table 5

Table 5. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.5 V to 5.5
Input capacitor	4.7 µF
Output capacitor	10 µF
Inductor	4.7 µH or 10 µH
ADJ programmable output voltage	0.7 V to 2.5 V

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Output Voltage Selection for Adjustable LM3670

The output voltage of the adjustable parts can be programmed through the resistor network connected from V_{OUT} to V_{FB} then to GND. V_{OUT} is adjusted to make V_{FB} equal to 0.5 V. The resistor from V_{FB} to GND (R_2) must be at least 100 KΩ to keep the current sunk through this network well below the 15-µA quiescent current level (PFM mode with no switching) but large enough that it is not susceptible to noise. If R_2 is 200 KΩ, and V_{FB} is 0.5 V, then the current through the resistor feedback network is 2.5 µA (I_{FB} = 0.5 V / R_2). The output voltage formula is:

$$V_{OUT} = V_{FB} * \left(\frac{R_1}{R_2} + 1\right) \quad (10)$$

where

- V_{OUT} = output voltage (V)
- V_{FB} = feedback voltage (0.5 V typical)
- R_1 Resistor from V_{OUT} to V_{FB} (Ω)
- R_2 Resistor from V_{OUT} to GND (Ω)

For output voltage greater than or equal to 0.7 V a frequency zero must be added at 10 kHz for stability.

$$C_1 = \frac{1}{2 * \pi * R_1 * 10\ \text{kHz}} \quad (11)$$

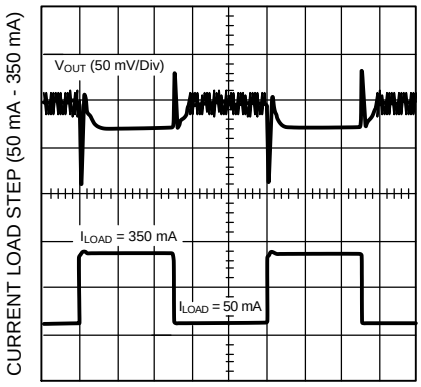
For any output voltages equal to 0.7 V or 2.5 V, a pole must also be placed at 10 kHz (see Table 6).

Table 6. Adjustable LM3670 Configurations for Various V_{OUT}

VOUT (V)	R1 (KΩ)	R2 (KΩ)	C1 (pF)	C2 (pF)	L (µH)	C_{IN} (µF)	C_{OUT} (µF)
0.7	80.6	200	200	150	4.7	4.7	10
0.8	120	200	130	none	4.7	4.7	10
0.9	160	200	100	none	4.7	4.7	10
1.0	200	200	82	none	4.7	4.7	10
1.1	240	200	68	none	4.7	4.7	10
1.2	280	200	56	none	4.7	4.7	10
1.24	221	150	75	120	4.7	4.7	10
1.5	402	200	39	none	10	4.7	10
1.6	442	200	39	none	10	4.7	10
1.7	487	200	33	none	10	4.7	10
1.875	549	200	30	none	10	4.7	14.7(1)
2.5	806	200	22	82	10	4.7	22

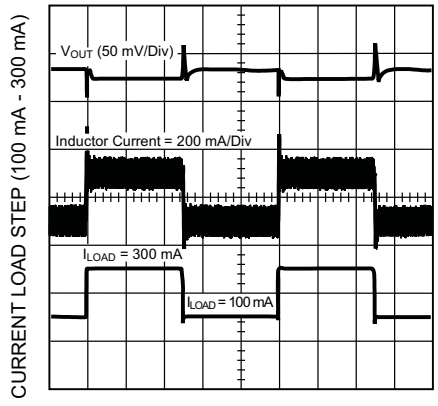
(1) (10 || 4.7)

8.2.2.3 Application Curves



I_{LOAD} = 50 mA to 350 mA

Figure 21. Load Transient



I_{LOAD} = 100 mA to 300 mA

Figure 22. Load Transient

9 Power Supply Recommendations

The LM3670 is designed to operate from a stable input supply range of 2.5 V to 5.5 V.

10 Layout

10.1 Layout Guidelines

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces, which can send erroneous signals to the DC-DC converter device, resulting in poor regulation or instability.

Good layout for the LM3670 can be implemented by following a few simple design rules, as shown in Figure 23.

- *Place the LM3670, inductor and filter capacitors close together and make the traces short.* The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Place the capacitors and inductor within 0.2 in. (5 mm) of the LM3670.
- *Arrange the components so that the switching current loops curl in the same direction.* During the first half of each cycle, current flows from the input filter capacitor, through the LM3670 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground, through the LM3670 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
- *Connect the ground pins of the LM3670, and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then, connect this to the ground-plane (if one is used) with several vias.* This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LM3670 by giving it a low-impedance ground connection.
- *Use wide traces between the power components and for power connections to the DC-DC converter circuit.* This reduces voltage errors caused by resistive losses across the traces.
- *Route noise sensitive traces, such as the voltage feedback path, away from noisy traces between the power components.* The voltage feedback trace must remain close to the LM3670 circuit, and be direct but must be routed opposite to noisy components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace.
- *Place noise sensitive circuitry, such as radio IF blocks, away from the DC-DC converter, CMOS digital blocks and other noisy circuitry.* Interference with noise-sensitive circuitry in the system can be reduced through distance.

In mobile phones, for example, a common practice is to place the DC-DC converter on one corner of the board, arrange the CMOS digital circuitry around it (because this also generates noise), and then place sensitive pre-amplifiers and IF stages on the diagonally opposing corner. Often, the sensitive circuitry is shielded with a metal pan and, by using low-dropout linear regulators, power to the circuit is post-regulated to reduce conducted noise.

10.2 Layout Example

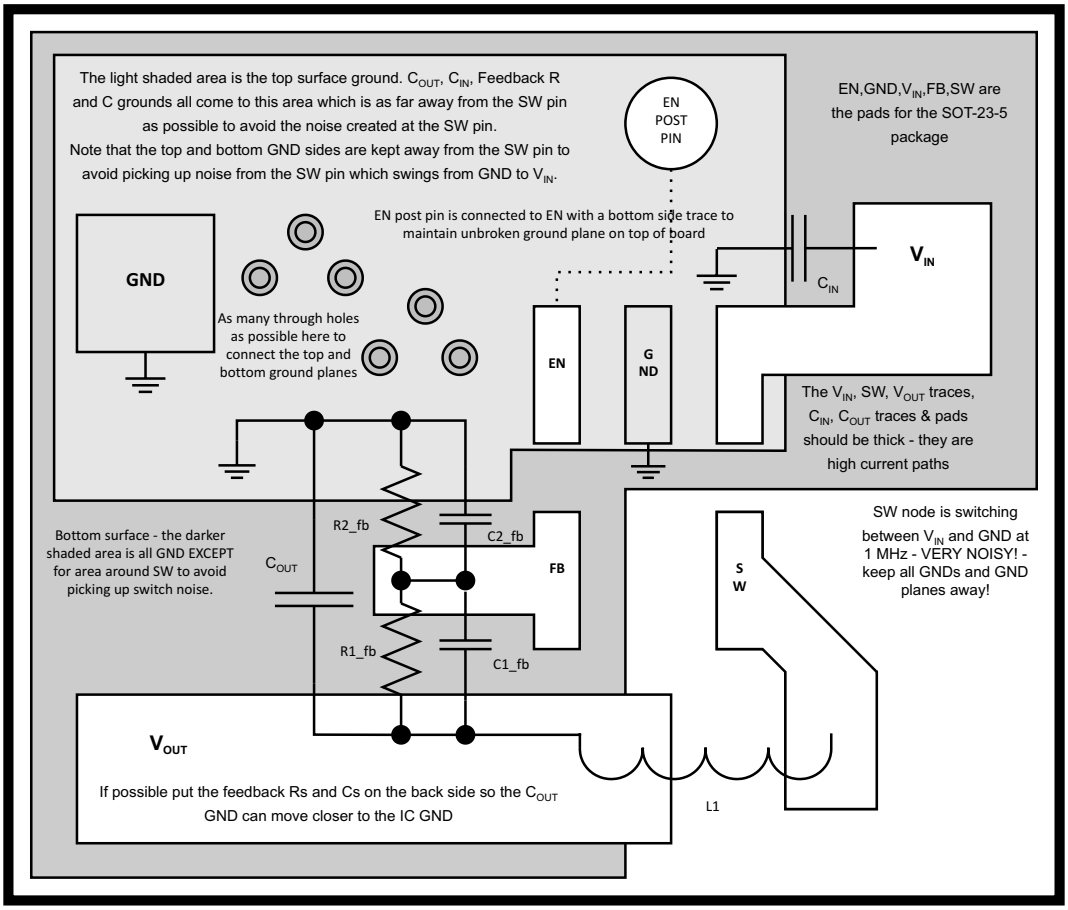


Figure 23. LM3670 Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3670MF-1.2/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	SCZB	Samples
LM3670MF-1.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	S82B	Samples
LM3670MF-1.6/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	SDBB	Samples
LM3670MF-1.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	SDCB	Samples
LM3670MF-1.875/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	SEFB	Samples
LM3670MF-3.3/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	SDEB	Samples
LM3670MF-ADJ/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	SDFB	Samples
LM3670MFX-1.2/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	SCZB	Samples
LM3670MFX-1.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	SDCB	Samples
LM3670MFX-ADJ/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	SDFB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

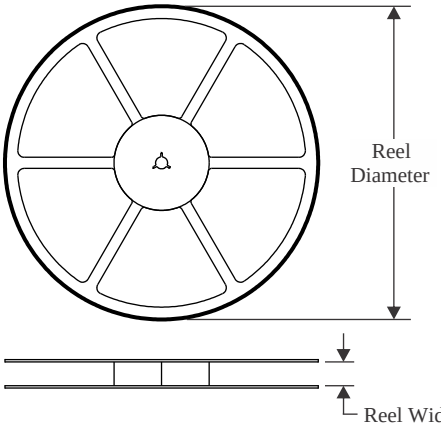
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

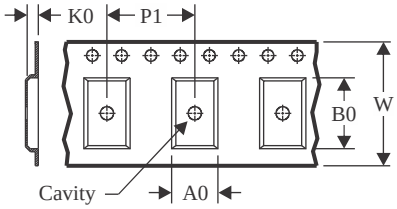
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

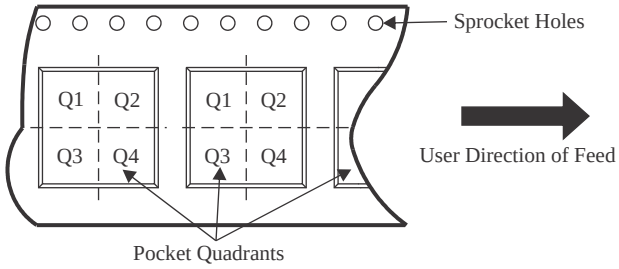


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

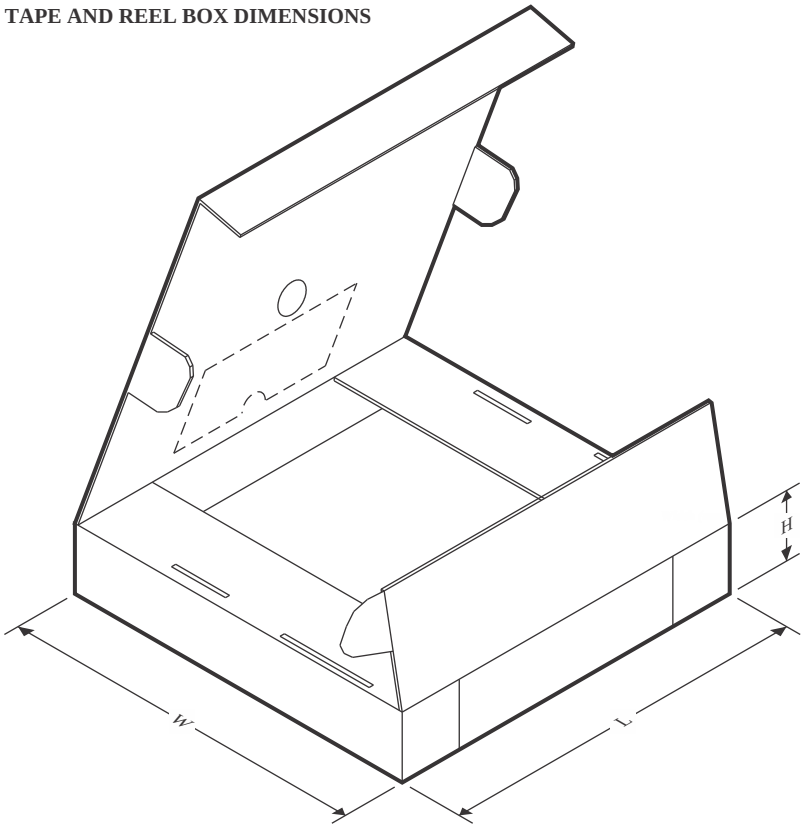
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3670MF-1.2/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3670MF-1.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3670MF-1.6/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3670MF-1.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3670MF-1.875/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3670MF-3.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3670MF-ADJ/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3670MFX-1.2/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3670MFX-1.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3670MFX-ADJ/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

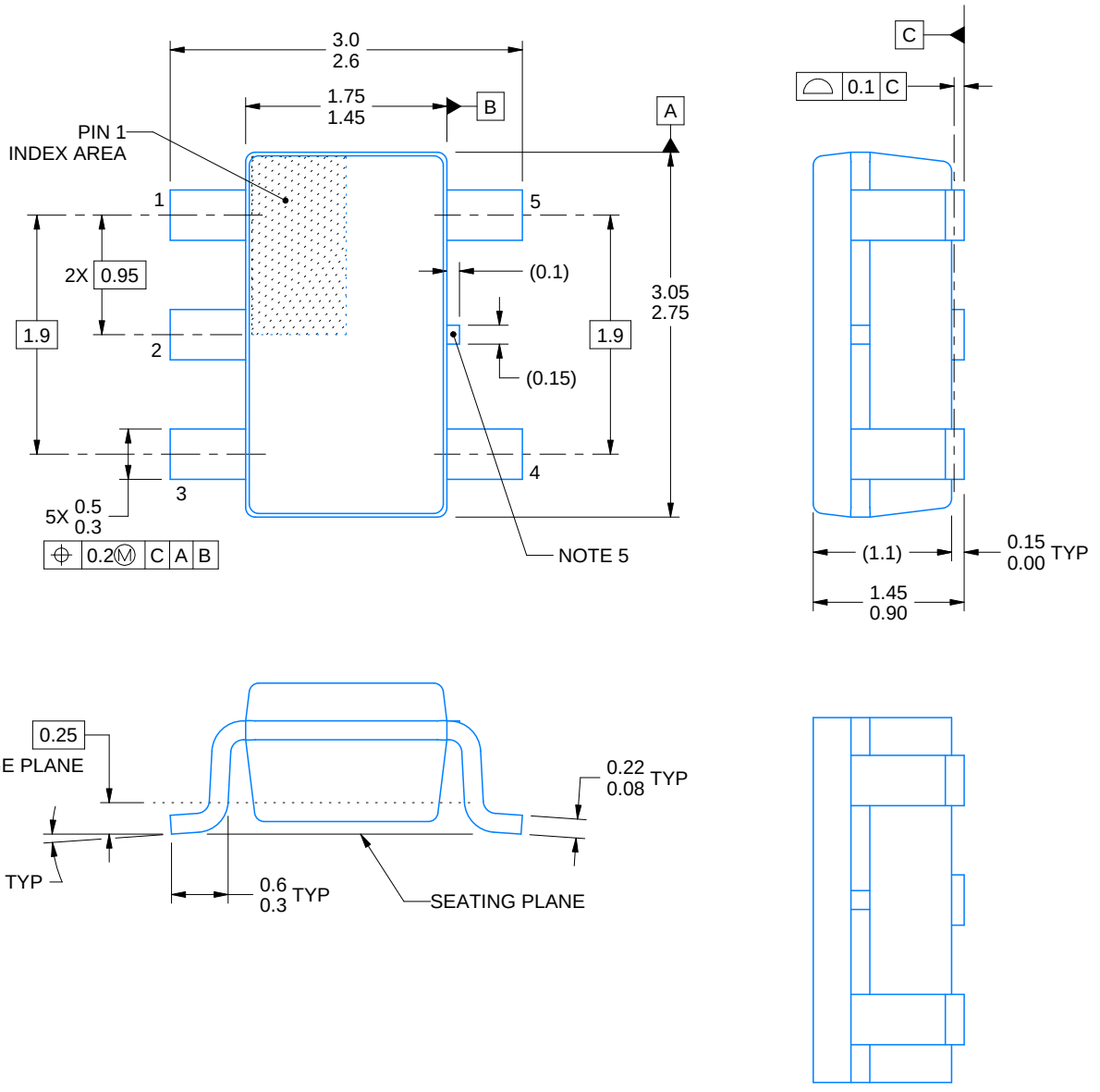
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3670MF-1.2/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LM3670MF-1.5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LM3670MF-1.6/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LM3670MF-1.8/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LM3670MF-1.875/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LM3670MF-3.3/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LM3670MF-ADJ/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LM3670MFX-1.2/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LM3670MFX-1.8/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LM3670MFX-ADJ/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

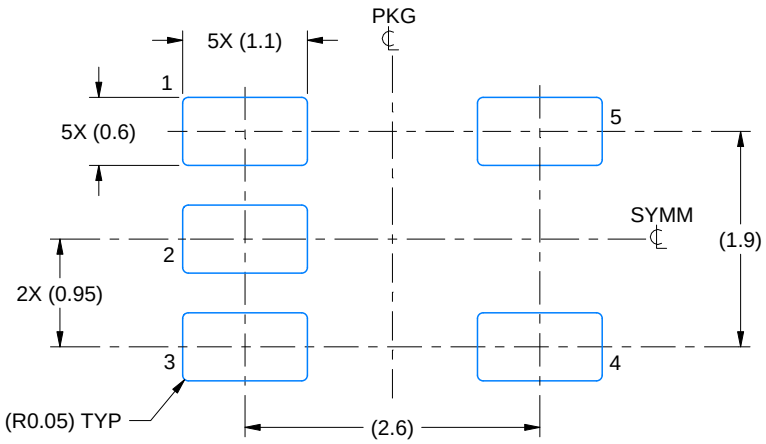


ALTERNATIVE PACKAGE SINGULATION VIEW

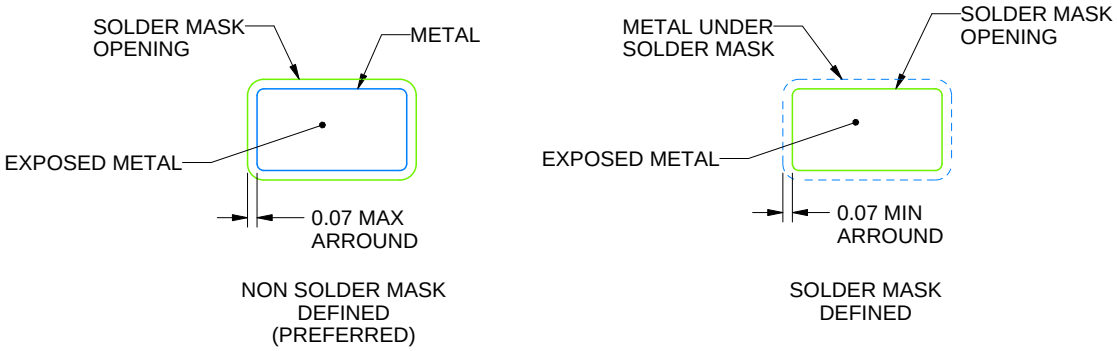
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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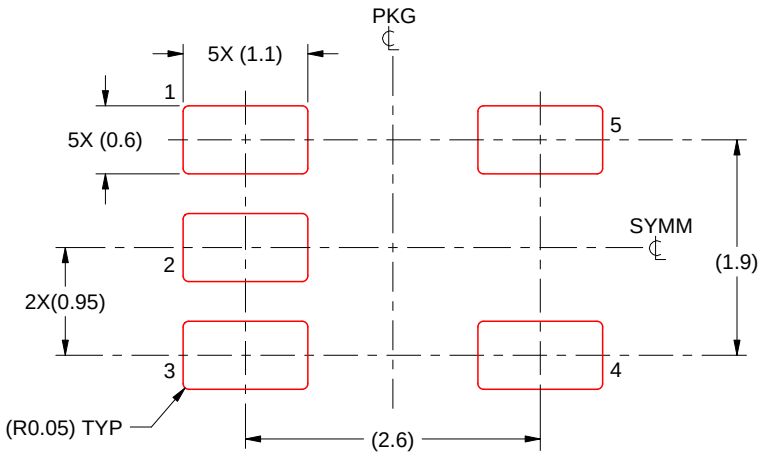
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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