THE DATASHEET OF

LM4140ACMX-4.1/NOPB

LM4140 High Precision Low Noise Low Dropout Voltage Reference

1 Features

- High Initial Accuracy: 0.1%
- Ultra-Low Noise
- Low Temperature Coefficient: 3 ppm/°C (A Grade)
- Low Voltage Operation: 1.8V
- Low Dropout Voltage: 20 mV (Typical) at 1mA
- Supply Current: 230 µA (Typical), ≤ 1 µA Disable Mode
- Enable Pin
- Output Voltage Options: 1.024 V, 1.25 V, 2.048 V, 2.5 V, and 4.096 V
- Custom Voltages From 0.5 V to 4.5 V
- Temperature Range: 0°C to 70°C

2 Applications

- Portable, Battery-Powered Equipment
- Instrumentation and Test Equipment
- Automotive
- Industrial Process Control
- Data Acquisition Systems
- Medical Equipment
- Precision Scales
- Servo Systems
- Battery Charging

3 Description

The LM4140 series of precision references are designed to combine high accuracy, low drift, and noise with low power dissipation in a small package.

The LM4140 is the industry's first reference with output voltage options lower than the bandgap voltage.

The key to the advance performance of the LM4140 is the use of EEPROM registers and CMOS DACs for temperature coefficient curvature correction and trimming of the output voltage accuracy of the device during the final production testing.

The major advantage of this method is the much higher resolution available with DACs than is available economically with most methods used by other bandgap references.

The low input and dropout voltage, low supply current, and output drive capability of the LM4140 makes this product an ideal choice for battery powered and portable applications.

The LM4140 is available in three grades (A, B, C) with 0.1% initial accuracy and 3, 6, and 10 ppm/°C temperature coefficients. For even lower temperature coefficients, contact Texas Instruments.

The device performance is specified over the temperature range 0°C to 70°C, and is available in compact 8-pin package.

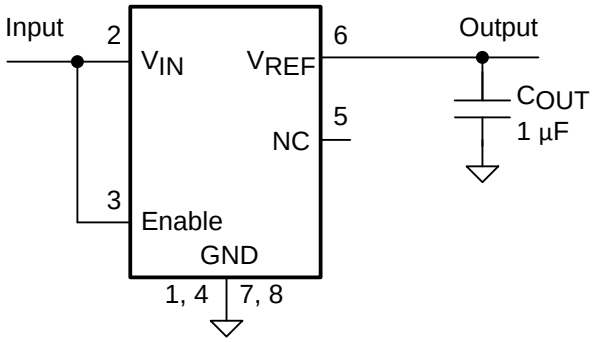
For other output voltage options from 0.5 V to 4.5 V, contact Texas Instruments.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM4140	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April 2013) to Revision F **Page**

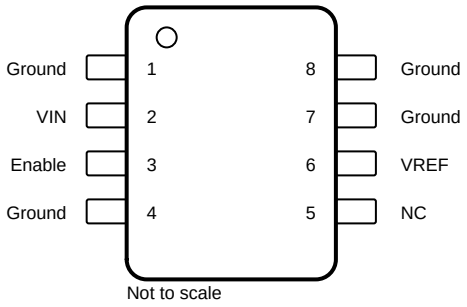
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added *Thermal Information* table ... 4

Changes from Revision D (April 2005) to Revision E **Page**

- Changed layout of National Semiconductor Data Sheet to TI format ... 1

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Not to scale

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
Enable	3	I	Pulled to input for normal operation. Forcing this pin to ground turns off the output.
Ground	1, 4, 7, 8	G	Negative supply or ground connection. These pins must be connected to ground.
NC	5	—	This pin must be left open.
V_{IN}	2	I	Positive supply.
V_{REF}	6	O	Reference output. Capable of sourcing up to 8 mA.

(1) G = Ground, I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Maximum voltage on any input pin	–0.3	5.6	V
Output short-circuit duration	Indefinite		
Power dissipation (T_A = 25°C)(2)		345	mW
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Without PCB copper enhancements. The maximum power dissipation must be derated at elevated temperatures and is limited by T_{JMAX} (maximum junction temperature), $R_{\theta JA}$ (junction to ambient thermal resistance) and T_A (ambient temperature). The maximum power dissipation at any temperature is: $PDiss_{MAX} = (T_{JMAX} - T_A)/R_{\theta JA}$ up to the value listed in the *Absolute Maximum Ratings*. The $R_{\theta JA}$ for the 8-pin SOIC package is 160°C/W.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Ambient temperature	0		70	°C
Junction temperature	0		80	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM4140 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	59.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_{IN} = 3 V for the 1.024-V and 1.25-V, V_{IN} = 5 V for all other voltage options, $V_{EN} = V_{IN}$, C_{OUT} = 1 µF(1), I_{LOAD} = 1 mA, and $T_A = T_J$ = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN(2)	TYP(3)	MAX(2)	UNIT
V_{REF}	Output voltage initial accuracy(4)	All versions					±0.1%	
TCV_{REF}/°C	Temperature coefficient	0°C ≤ T_A ≤ 70°C		A grade			3	ppm/°C
				B grade			6	
				C grade			10	
$\Delta V_{REF}/\Delta V_{IN}$	Line regulation	1.024-V and 1.25-V options, 1.8 V ≤ V_{IN} ≤ 5.5 V		T_A = 25°C		50	300	ppm/V
				0°C ≤ T_A ≤ 70°C			350	
		All other voltage options, V_{ref} + 200 mV ≤ V_{IN} ≤ 5.5 V		T_A = 25°C		20	200	
				0°C ≤ T_A ≤ 70°C			250	
$\Delta V_{REF}/\Delta I_{LOAD}$	Load regulation	1 mA ≤ I_{LOAD} ≤ 8 mA	All other voltage options	T_A = 25°C		1	20	ppm/mA
				0°C ≤ T_A ≤ 70°C			150	
			4.096-V option	T_A = 25°C		5	35	
				0°C ≤ T_A ≤ 70°C			150	
ΔV_{REF}	Long-term stability	1000 hours				60		ppm
ΔV_{REF}	Thermal hysteresis(5)	0°C ≤ T_A ≤ + 70°C				20		ppm
	Operating voltage	1.024-V and 1.25-V options, I_L = 1 mA to 8 mA, 0°C ≤ T_A ≤ 70°C			1.8		5.5	V
V_{IN}-V_{REF}	Dropout voltage(6)	2.048-V and 2.5-V options	I_L = 1 mA	T_A = 25°C		20	40	mV
				0°C ≤ T_A ≤ 70°C			45	
			I_L = 8 mA	T_A = 25°C		160	235	
				0°C ≤ T_A ≤ 70°C			400	
		4.096-V option	I_L = 1 mA	T_A = 25°C		20	40	
				0°C ≤ T_A ≤ 70°C			45	
			I_L = 8 mA	T_A = 25°C		195	270	
				0°C ≤ T_A ≤ 70°C			490	
V_N	Output noise voltage(7)	0.1 Hz to 10 Hz				2.2		μV_{PP}
$I_{S(ON)}$	Supply current	I_{LOAD} = 0 mA	All other voltage options	T_A = 25°C		230	320	µA
				0°C ≤ T_A ≤ 70°C			375	
			4.096-V option	T_A = 25°C		265	350	
				0°C ≤ T_A ≤ 70°C			400	
$I_{S(OFF)}$	Supply current	V_{Enable} < 0.4 V		T_A = 25°C		0.01		µA
				0°C ≤ T_A ≤ 70°C			1	
V_H	Logic high input voltage	0°C ≤ T_A ≤ 70°C			0.8 × V_{IN}			V
I_H	Logic high input current					2		nA
V_L	Logic low input voltage	0°C ≤ T_A ≤ 70°C					0.4	V
I_L	Logic low input current					1		nA
I_{SC}	Short-circuit current	T_A = 25°C			8.5	20	35	mA
		0°C ≤ T_A ≤ 70°C					40	

(1) For proper operation, a 1-µF capacitor is required between the output pin and the GND pin of the device.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL).
(3) Typical numbers are at 25°C and represent the most likely parametric norm.
(4) High temperature and mechanical stress associated with PCB assembly can have significant impact on the initial accuracy of the LM4140 and may create significant shifts in V_{REF}.
(5) Thermal hysteresis is defined as the changes in 25°C output voltage before and after the cycling of the device from 0°C to 70°C.
(6) Dropout voltage is defined as the minimum input to output differential voltage at which the output voltage drops by 0.5% below the value measured with V_{IN} = 3 V for the 1.024-V and 1.25-V, V_{IN} = 5 V for all other voltage options.
(7) The output noise is based on 1.024 V option. Output noise is linearly proportional to V_{REF}.

6.6 Typical Characteristics

T_A = 25°C, no load, C_{OUT} = 1 µF, V_{IN} = 3 V for 1.024-V and 1.25-V, and 5 V for all other voltage options, and V_{IN} = V_{EN} (unless otherwise noted). The 1-µF output capacitor is actively discharged to ground (see *ON/OFF Operation* for more details).

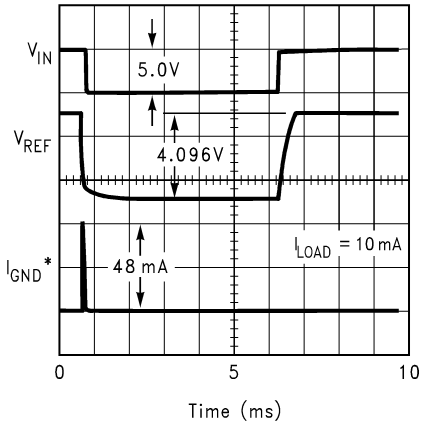


Figure 1. Power Up and Down Ground Current

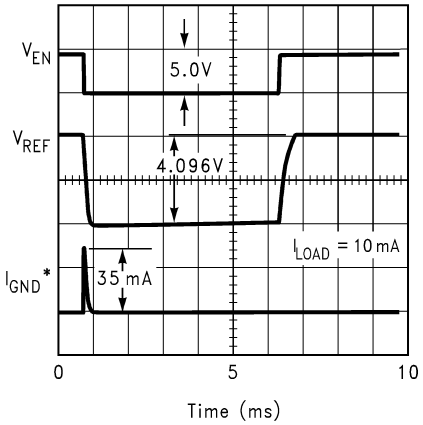


Figure 2. Enable Response

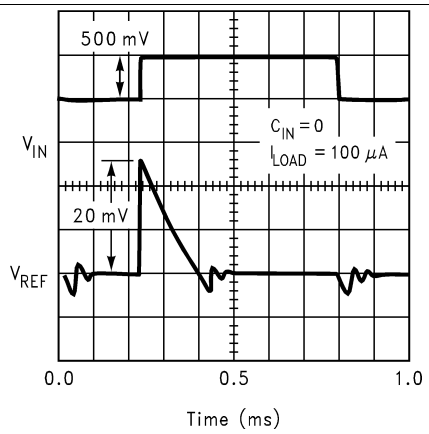


Figure 3. Line Transient Response

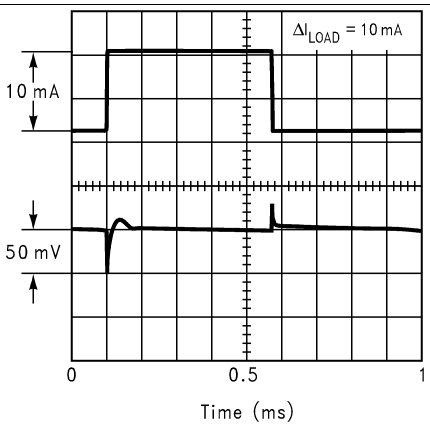


Figure 4. Load Transient Response

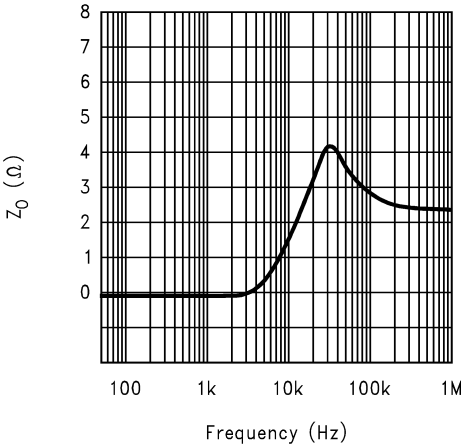


Figure 5. Output Impedance

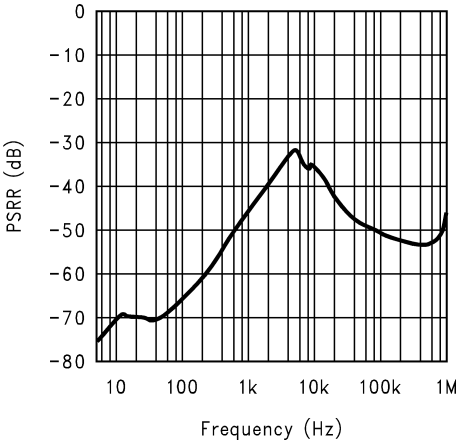
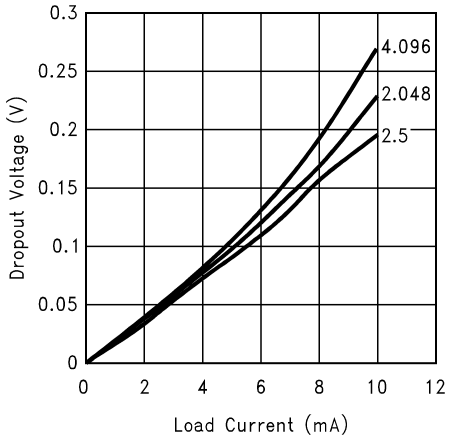


Figure 6. Power Supply Rejection Ratio

Typical Characteristics (continued)

T_A = 25°C, no load, C_{OUT} = 1 µF, V_{IN} = 3 V for 1.024-V and 1.25-V, and 5 V for all other voltage options, and V_{IN} = V_{EN} (unless otherwise noted). The 1-µF output capacitor is actively discharged to ground (see *ON/OFF Operation* for more details).



1.024-V and 1.25-V options require 1.8-V supply

Figure 7. Dropout Voltage vs Load Current

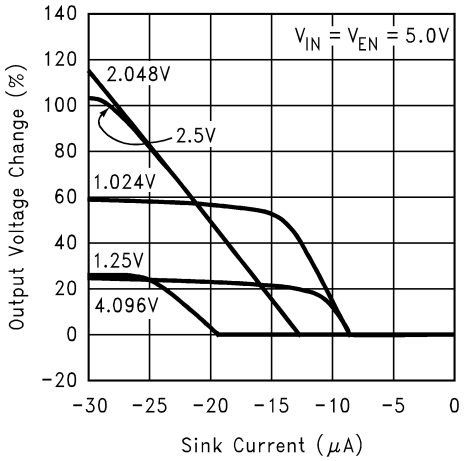


Figure 8. Output Voltage Change vs Sink Current (I_{SINK})

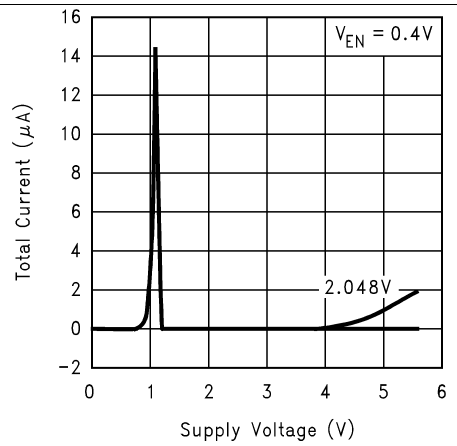


Figure 9. Total Current ($I_{S(OFF)}$) vs Supply Voltage

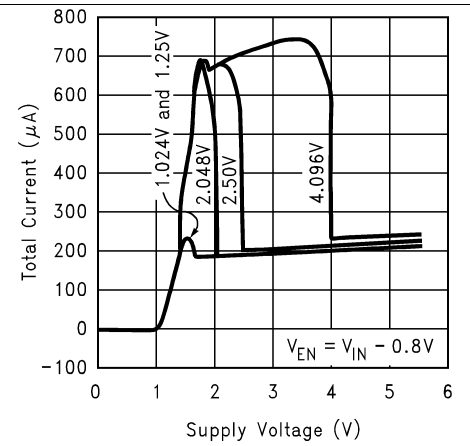


Figure 10. Total Current ($I_{S(ON)}$) vs Supply Voltage

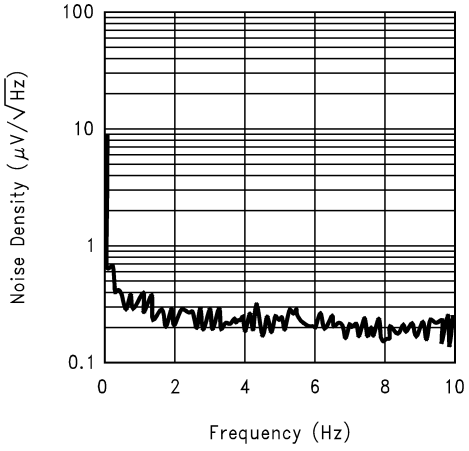


Figure 11. Spectral Noise Density (0.1 Hz to 10 Hz)

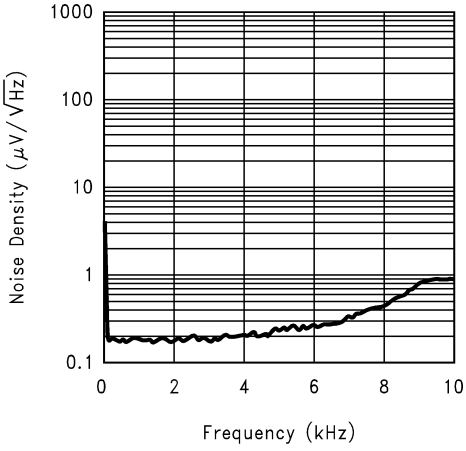


Figure 12. Spectral Noise Density (10 Hz to 100 kHz)

Typical Characteristics (continued)

T_A = 25°C, no load, C_{OUT} = 1 µF, V_{IN} = 3 V for 1.024-V and 1.25-V, and 5 V for all other voltage options, and V_{IN} = V_{EN} (unless otherwise noted). The 1-µF output capacitor is actively discharged to ground (see *ON/OFF Operation* for more details).

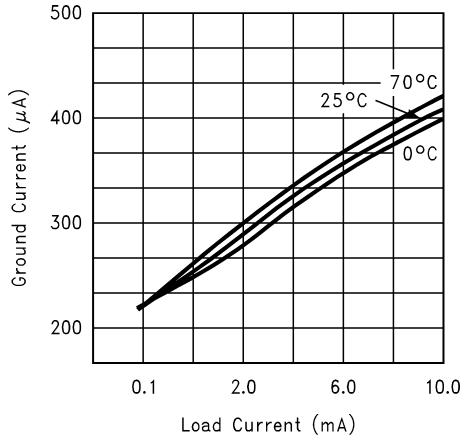


Figure 13. Ground Current vs Load Current

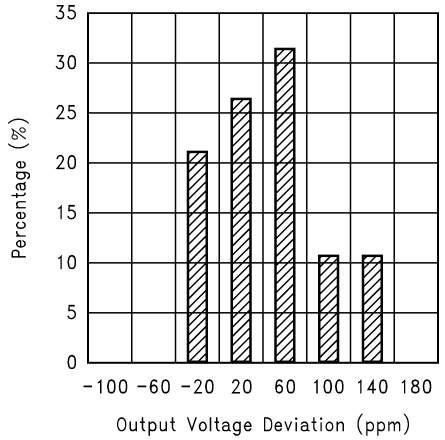


Figure 14. Long-Term Drift

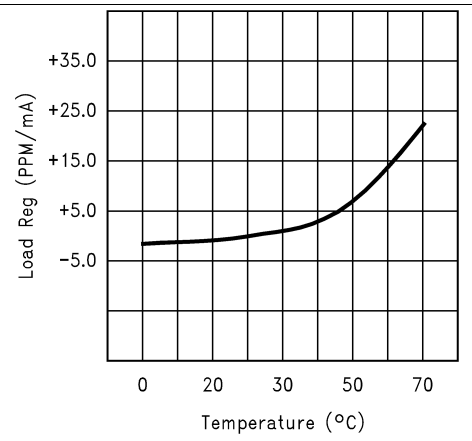


Figure 15. Load Regulation vs Temperature

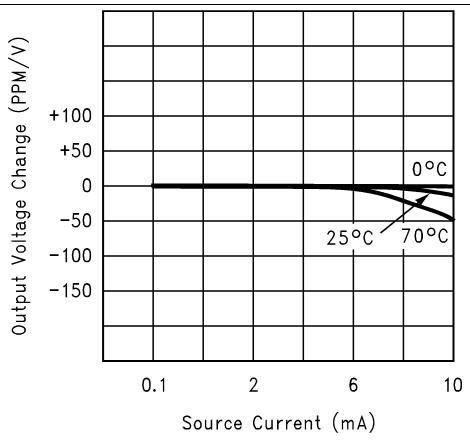


Figure 16. Output Voltage vs Load Current

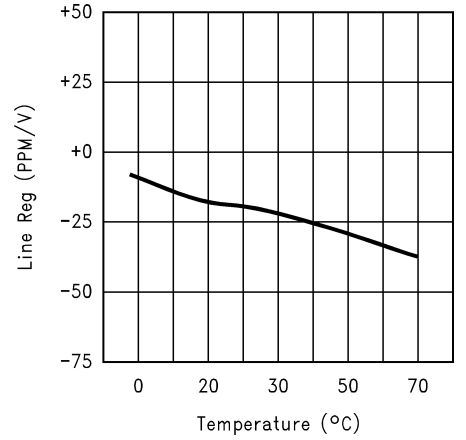


Figure 17. Line Regulation vs Temperature

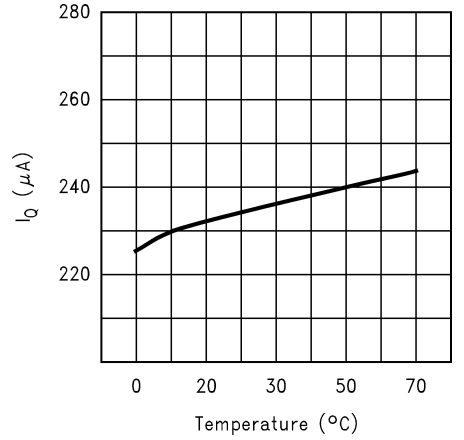


Figure 18. I_Q vs Temperature

Typical Characteristics (continued)

T_A = 25°C, no load, C_{OUT} = 1 µF, V_{IN} = 3 V for 1.024-V and 1.25-V, and 5 V for all other voltage options, and V_{IN} = V_{EN} (unless otherwise noted). The 1-µF output capacitor is actively discharged to ground (see *ON/OFF Operation* for more details).

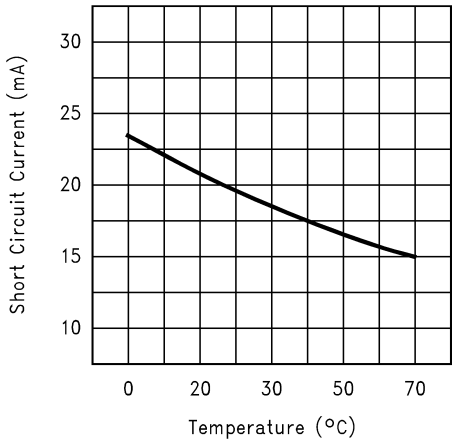


Figure 19. Short-Circuit Current vs Temperature

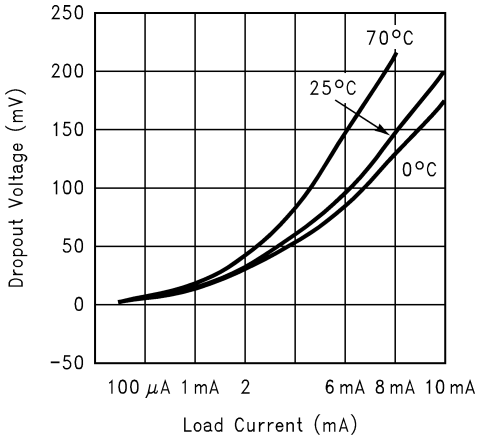


Figure 20. Dropout Voltage vs Load Current (V_{OUT}) = 2 V

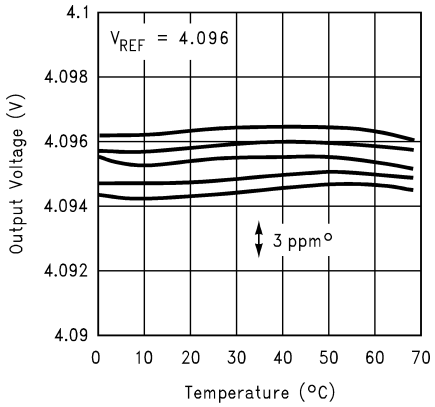


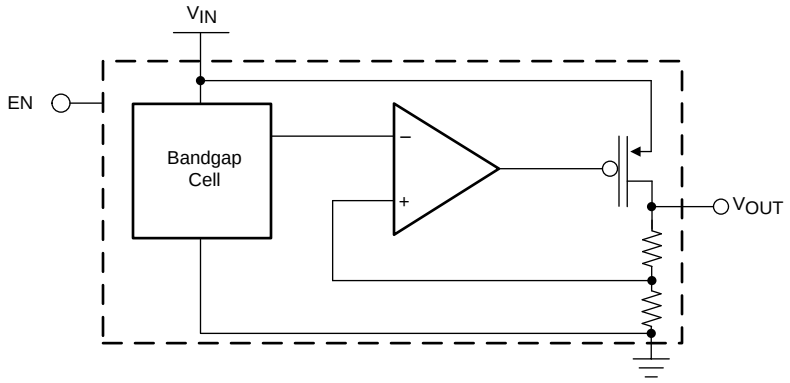
Figure 21. Typical Temperature Coefficient (Sample of 5 Parts)

7 Detailed Description

7.1 Overview

The LM4140 device is a high-precision series voltage reference available in 5 difference output voltage options, including the 1.024-V option below the bandgap voltage. The series reference can operate with input voltage as low as VREF + 400 mV over temperature, consuming 400 µA or less over temperature depending on voltage option. While in shutdown, the device consumes 10 nA (typical).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 ON/OFF Operation

The LM4140 is designed to quickly reduce both V_{REF} and I_Q to zero when turned off. V_{REF} is restored in less than 200 µs when turned on. During the turnoff, the charge across the output capacitor is discharged to ground through internal circuitry.

The LM4140 is turned off by pulling the enable input low, and turned on by driving the input high. If this feature is not to be used, the enable pin must be tied to the V_{IN} to keep the reference on at all times (the enable pin must not be left floating).

To ensure proper operation, the signal source used to drive the enable pin must be able to swing above and below the specified high and low voltage thresholds which ensure an ON or OFF state (see *Electrical Characteristics*).

The ON/OFF signal may come from either a totem-pole output, or an open-collector output with pullup resistor to the LM4140 input voltage. This high-level voltage may exceed the LM4140 input voltage, but must remain within the absolute maximum rating for the enable pin.

7.4 Device Functional Modes

Table 1 lists the operational modes of the LM4140.

Table 1. Operational Modes

ENABLE PIN	LOGIC STATE	DESCRIPTION
EN = V_{IN}	1	Normal operation, device powered up
EN = Ground	0	Device in shutdown

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input Capacitors

Although not always required, TI recommends an input capacitor. A supply bypass capacitor on the input assures that the reference is working from a source with low impedance, which improves stability. A bypass capacitor can also improve transient response by providing a reservoir of stored energy that the reference can use in case where the load current demand suddenly increases. The value used for C_{IN} may be used without limit.

8.1.2 Output Capacitors

The LM4140 requires a 1-µF (nominally) output capacitor for loop stability (compensation) as well as transient response. During the sudden changes in load current demand, the output capacitor must source or sink current during the time it takes the control loop of the LM4140 to respond.

This capacitor must be selected to meet the requirements of minimum capacitance and equivalent series resistance (ESR) range.

In general, the capacitor value must be at least 0.2 µF (over the actual ambient operating temperature), and the ESR must be within the range indicated in Figure 22, Figure 23, and Figure 24.

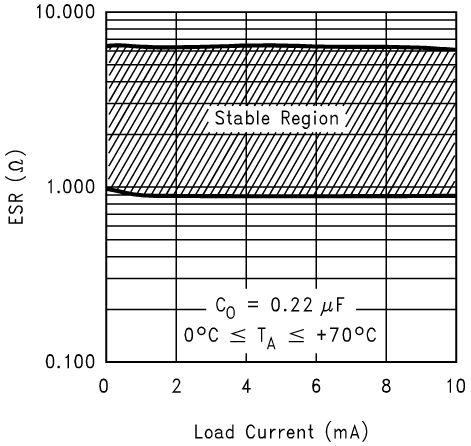


Figure 22. 0.22-µF ESR Range

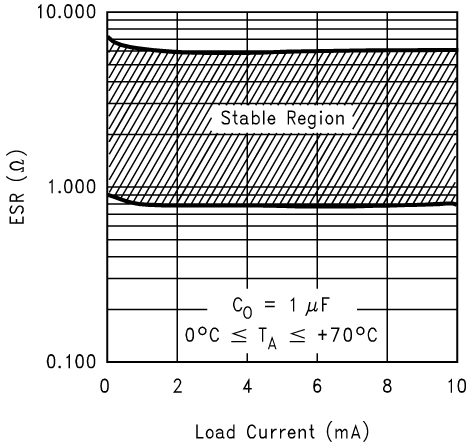


Figure 23. 1-µF ESR Range

Application Information (continued)

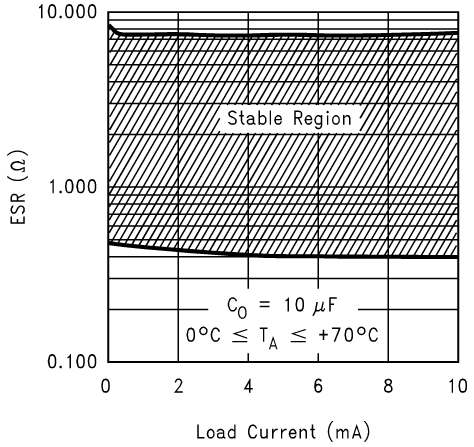


Figure 24. 10-µF ESR Range

8.1.3 Tantalum Capacitors

Surface-mountable solid tantalum capacitors offer a good combination of small physical size for the capacitance value, and ESR in the range required by the LM4140. The results of testing the LM4140 stability with surface mount solid tantalum capacitors show good stability with values in the range of 0.1 µF. However, optimum performance is achieved with a 1-µF capacitor.

Table 2 shows tantalum capacitors that have been verified as suitable for use with the LM4140.

Table 2. 1-µF Surface-Mount Tantalum Capacitor Selection Guide

MANUFACTURER	PART NUMBER
Kemet	T491A105M010AS
NEC	NRU105N10
Siemens	B45196-E3105-K
Nichicon	F931C105MA
Sprague	293D105X0016A2T

Table 3. 2.2-µF Surface-Mount Tantalum Capacitor Selection Guide

MANUFACTURER	PART NUMBER
Kemet	T491A225M010AS
NEC	NRU225M06
Siemens	B45196/2.2/10/10
Nichicon	F930J225MA
Sprague	293D225X0010A2T

8.1.4 Aluminum Electrolytic Capacitors

Although probably not a good choice for a production design, because of relatively large physical size, an aluminium electrolytic capacitor can be used in the design prototype for an LM4140 reference. A 1-µF capacitor meeting the ESR conditions can be used. If the operating temperature drops below 0°C, the reference may not remain stable, as the ESR of the aluminium electrolytic capacitor increases, and may exceed the limits indicated in the figures.

8.1.5 Multilayer Ceramic Capacitors

Surface-mountable multilayer ceramic capacitors may be an attractive choice because of their relatively small physical size and excellent RF characteristics.

However, they sometimes have an ESR values lower than the minimum required by the LM4140, and relatively large capacitance change with temperature. The manufacturer's datasheet for the capacitor must be consulted before selecting a value. Test results of LM4140 stability using multilayer ceramic capacitors show that a minimum of 0.2 µF is usually required.

Table 4 shows the multilayer ceramic capacitors that have been verified as suitable for use with the LM4140.

Table 4. Surface-Mount Ceramic Capacitors Selection Guide

CAPACITOR (µF)	MANUFACTURER	PART NUMBER
2.2	Tokin	1E225ZY5U-C203
2.2	Murata	GRM42-6Y5V225Z16
4.7	Tokin	1E475ZY5U-C304

8.1.6 Reverse Current Path

The P-channel Pass transistor used in the LM4140 has an inherent diode connected between the V_{IN} and V_{REF} pins (see Figure 25).

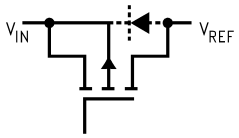


Figure 25. Internal P-Channel Pass Transistor

Forcing the output to voltages higher than the input, or pulling V_{IN} below voltage stored on the output capacitor by more than a V_{be}, forward biases this diode and current flows from the V_{REF} terminal to V_{IN}. No damage to the LM4140 occurs under these conditions as long as the current flowing into the output pin does not exceed 50 mA.

8.1.7 Output Accuracy

Like all references, either series or shunt, the after assembly accuracy is made up of primarily three components: initial accuracy itself, thermal hysteresis, and effects of the PCB assembly stress.

LM4140 provides an excellent output initial accuracy of 0.1% and temperature coefficient of 6ppm/°C (B Grade).

For best accuracy and precision, the LM4140 junction temperature must not exceed 70°C.

The thermal hysteresis curve on this datasheet are performance characteristics of three typical parts selected at random from a sample of 40 parts.

Parts are mounted in a socket to minimize the effect of PCB's mechnical expansion and contraction. Readings are taken at 25°C following multiple temperature cycles to 0°C and 70°C. The labels on the X axis of Figure 26 indicate the device temperature cycle prior to measurement at 25°C.

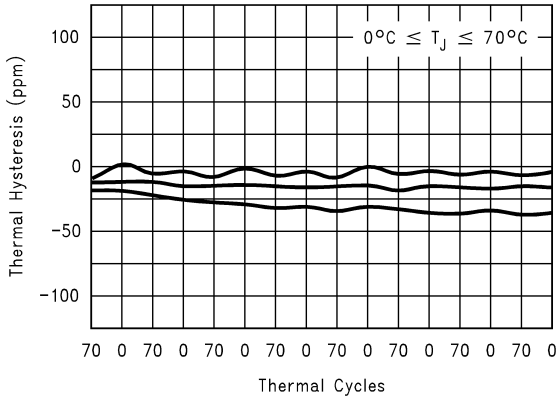


Figure 26. Typical Thermal Hysteresis

The mechanical stress due to the PCB's mechanical and thermal stress can cause an output voltage shift more than the true thermal coefficient of the device. References in surface mount packages are more susceptible to these stresses because of the small amount of plastic molding which support the leads.

Following the recommendations on *Layout* can minimize the mechanical stress on the device.

8.2 Typical Applications

8.2.1 Precision DAC Reference

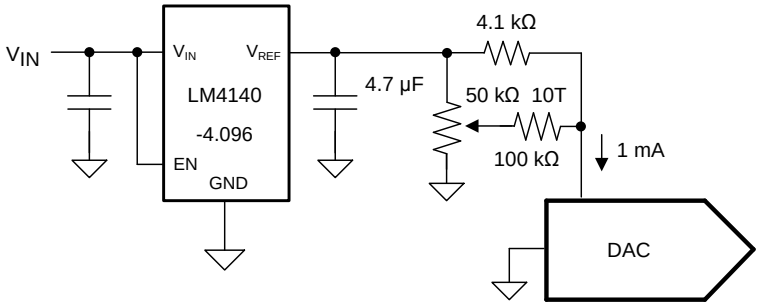


Figure 27. Precision DAC Reference Schematic

8.2.1.1 Design Requirements

Generate a precision, temperature-stable voltage reference for use in digital-to-analog converter applications.

8.2.1.2 Detailed Design Procedure

Use LM4140-4.096 to generate a 4.096-V reference voltage. Use an adjustable resistor network to fine tune the reference.

Typical Applications (continued)

8.2.1.3 Application Curves

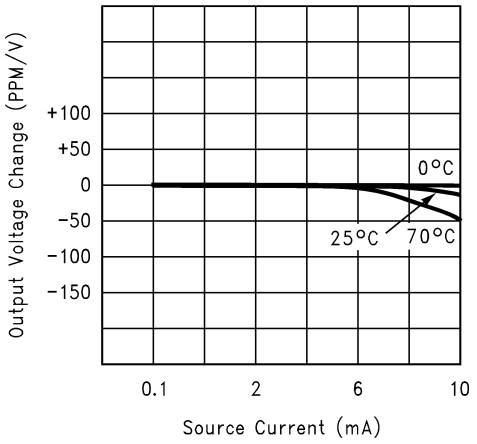


Figure 28. Output Voltage vs Load Current

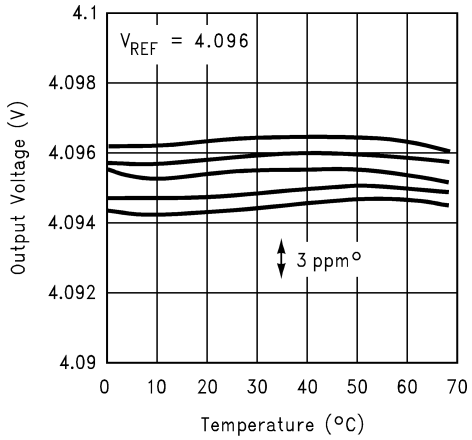


Figure 29. Typical Temperature Coefficient (Sample of 5 Parts)

8.2.2 Boosted Output Current

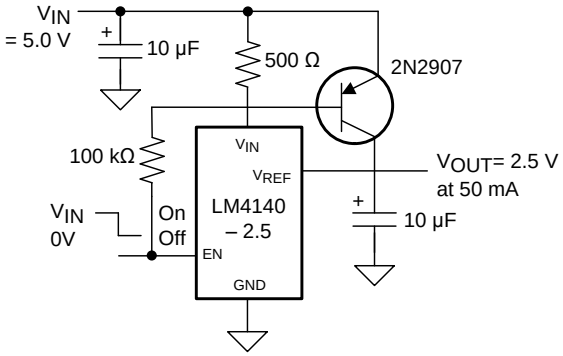


Figure 30. Boosted Output Current Schematic

8.2.2.1 Design Requirements

Generate a reference voltage that can support 50 mA.

8.2.2.2 Detailed Design Procedure

The LM4140-2.5 sets the reference level at 2.5 V. A 2N2907 PNP transistor is added, where the base is tied to V_{IN} through a 500-Ω resistor. The input current into the LM4140 increases with load current, which increases the voltage drop across the 500-Ω resistor until the PNP transistor turns on and supplements the load current. See Figure 30 for the circuit diagram.

Typical Applications (continued)

8.2.3 Boosted Output Current With Current Limiter

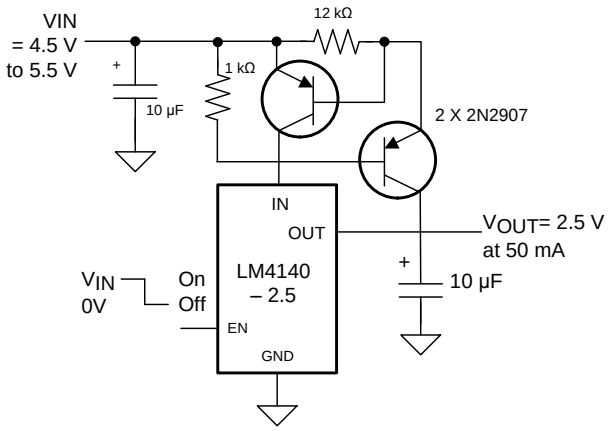


Figure 31. Boosted Output Current With Current Limiter Schematic

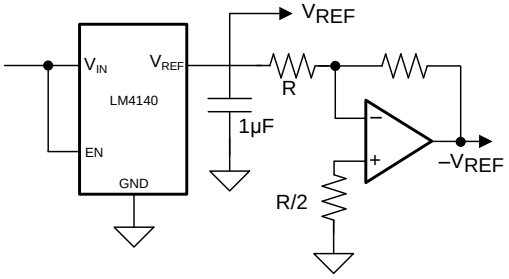
8.2.3.1 Design Requirements

Generate a reference voltage that can support 50 mA with current limiter.

8.2.3.2 Detailed Design Procedure

The LM4140-2.5 sets the reference level at 2.5 V. Similar to *Boosted Output Current*, a PNP transistor is added between V_{IN} and the output. Another PNP transistor is added to sense the current between V_{IN} and the load. This additional transistor turns on above 50 mA, which turns off the pass transistor to the load.

8.2.4 Complimentary Outputs



* Low Noise Op Amp such as OP-27

Figure 32. Complimentary Outputs Schematic

8.2.4.1 Design Requirements

Generate a positive and negative voltage reference.

8.2.4.2 Detailed Design Procedure

Use the LM4140 to generate the positive reference. Pass the reference into a unity gain inverting amplifier for a negative reference output.

Typical Applications (continued)

8.2.5 Voltage Reference With Force and Sense Output

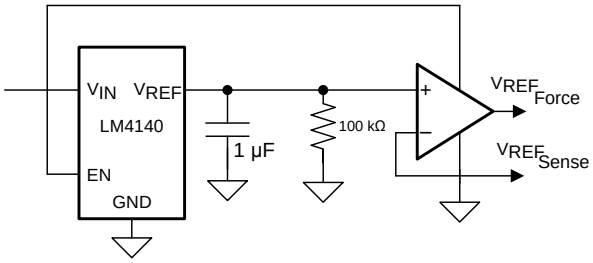


Figure 33. Voltage Reference With Force and Sense Output Schematic

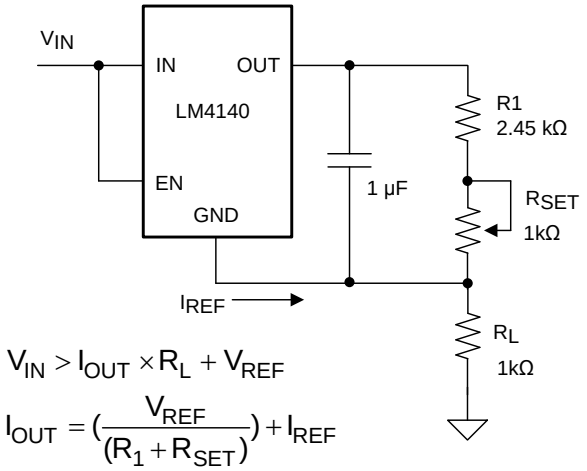
8.2.5.1 Design Requirements

Design a voltage reference source that has a force and sense output.

8.2.5.2 Detailed Design Procedure

Use the LM4140 to generate a reference voltage. Pass this into the positive input terminal of an operation amplifier, and use the negative input as the sense input from the load.

8.2.6 Precision Programmable Current Source



$$V_{IN} > I_{OUT} \times R_L + V_{REF}$$

$$I_{OUT} = \left(\frac{V_{REF}}{(R_1 + R_{SET})}\right) + I_{REF}$$

$R1 = 2.45\ k\Omega$ for

$I_L = 1\ mA$ using LM4120 – 2.5

Figure 34. Precision Programmable Current Source Schematic

8.2.6.1 Design Requirements

Create a precision, adjustable current source.

8.2.6.2 Detailed Design Procedure

Use LM4140 to create reference voltage across an adjustable resistor, R1 + RSET. The voltage reference creates a constant voltage source, and the adjustable resistor generates a proportional current.

Typical Applications (continued)

8.2.7 Strain Gauge Conditioner for 350-Ω Bridge

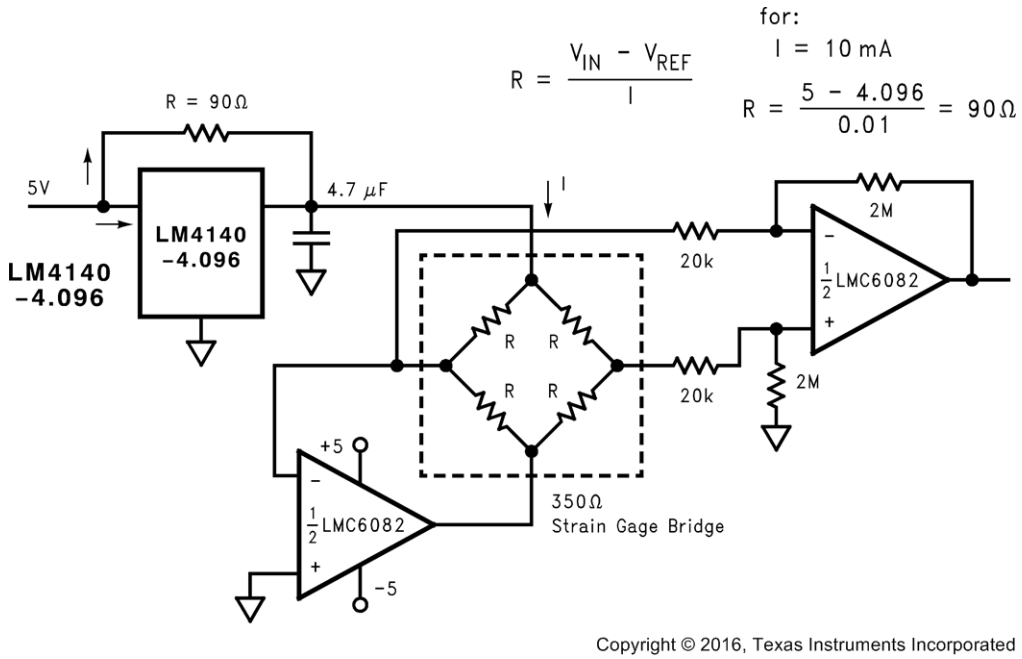


Figure 35. Strain Gauge Conditioner for 350-Ω Bridge Schematic

8.2.7.1 Design Requirements

Supply a strain gage with a precision reference voltage.

8.2.7.2 Detailed Design Procedure

Use LM4140 to generate 4.096-V reference voltage. Use the reference to drive the strain gage bridge.

8.2.8 Bipolar Voltage References for Low Power ADC

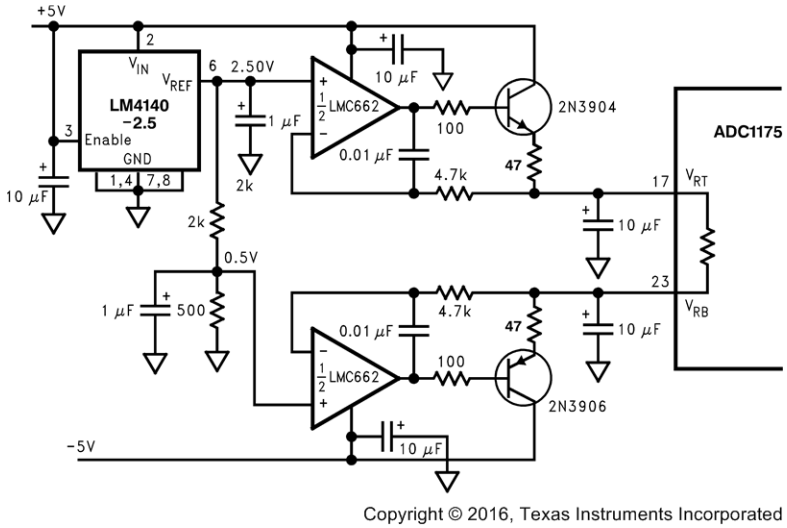


Figure 36. Bipolar Voltage References for Low Power ADC Schematic

Typical Applications (continued)

8.2.8.1 Design Requirements

Provide positive and negative reference voltages for the ADC1175 low power ADC.

8.2.8.2 Detailed Design Procedure

Use LM4140 to generate a 2.5-V positive reference voltage. The reference voltage is passed into an opamp to act as a buffer and inverter, which yields a positive and negative reference. Transistors are used to drive the low impedance inputs of the ADC1175.

8.2.9 Self-Biased Low Power ADC Reference With Trim Current Sources

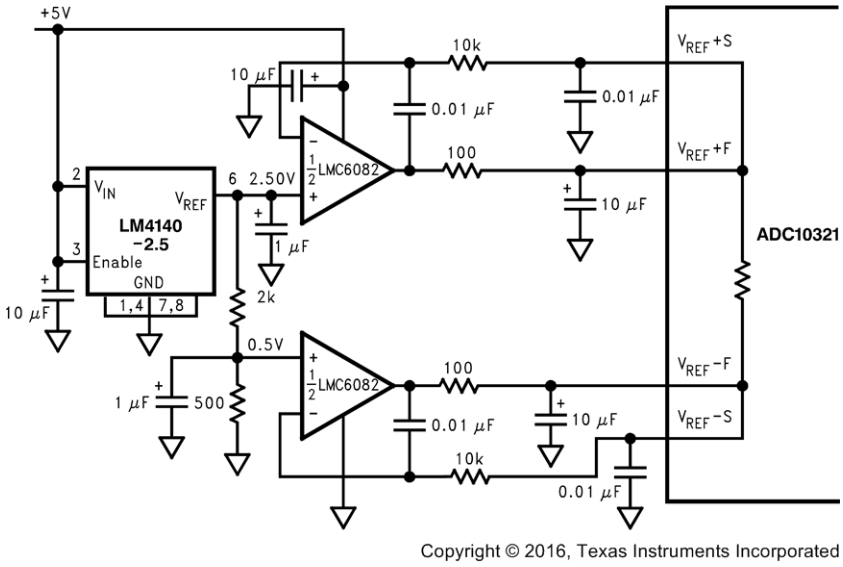


Figure 37. Self-Biased Low Power ADC Reference With Trim Current Sources Schematic

8.2.9.1 Design Requirements

Use ADC1175 internal reference, but increase accuracy with trimming currents.

8.2.9.2 Detailed Design Procedure

The LM4140-2.5 sets a stable voltage source which is buffered and inverted, and the opamps are used as force and sense amplifiers. This application does not require the transistor to drive low impedance nodes as the internal reference voltages are still being used. The external circuitry is to increase the accuracy of the internal reference.

9 Power Supply Recommendations

While an input capacitor is not required, TI recommends using a 0.1 µF or larger capacitor to reduce noise on the input and improve transient response.

10 Layout

10.1 Layout Guidelines

The simplest ways to reduce the stress related shifts are:

1. Mounting the device near the edges or the corners of the board where mechanical stress is at its minimum. The center of the board generally has the highest mechanical and thermal expansion stress.
2. Mechanical isolation of the device by creating an island by cutting a U shape slot on the PCB for mounting the device. This approach would also provide some thermal isolation from the rest of the circuit.

Figure 39 is a recommended printed-circuit board layout with a slot cut on three sides of the circuit layout to serve as a strain relief.

10.2 Layout Example

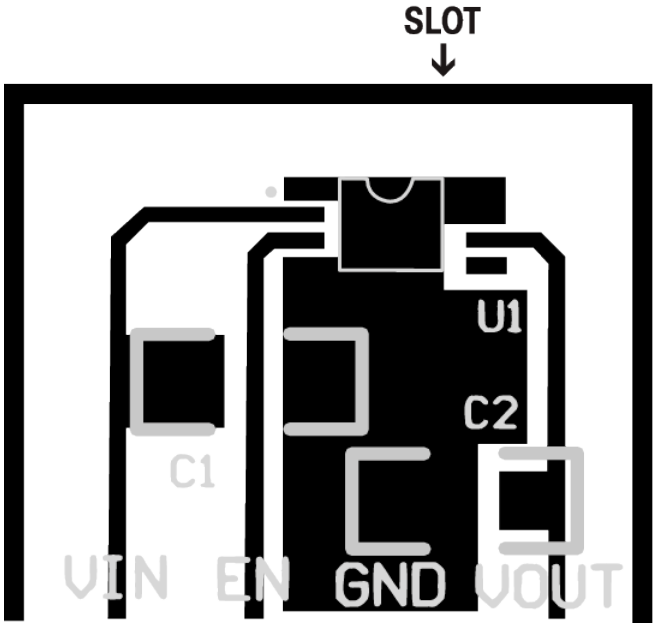


Figure 38. Suggested Schematic and External Components

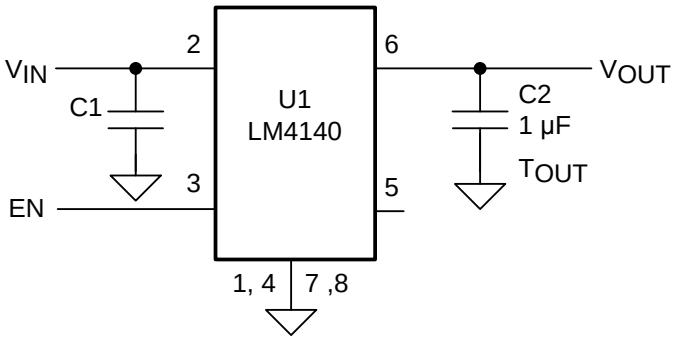


Figure 39. Suggested PCB Layout With Slot

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM4140ACM-1.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140A CM1.0	Samples
LM4140ACM-1.2/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140A CM1.2	Samples
LM4140ACM-2.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140A CM2.0	Samples
LM4140ACM-2.5/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140A CM2.5	Samples
LM4140ACM-4.1/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140A CM4.1	Samples
LM4140ACMX-2.5/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140A CM2.5	Samples
LM4140ACMX-4.1/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140A CM4.1	Samples
LM4140BCM-1.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140B CM1.0	Samples
LM4140BCM-1.2/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140B CM1.2	Samples
LM4140BCM-2.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140B CM2.0	Samples
LM4140BCM-2.5/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140B CM2.5	Samples
LM4140BCM-4.1/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140B CM4.1	Samples
LM4140BCMX-1.0/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140B CM1.0	Samples
LM4140BCMX-2.5/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140B CM2.5	Samples
LM4140BCMX-4.1/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140B CM4.1	Samples
LM4140CCM-1.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140C CM1.0	Samples
LM4140CCM-1.2/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140C CM1.2	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM4140CCM-2.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140C CM2.0	Samples
LM4140CCM-2.5/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140C CM2.5	Samples
LM4140CCM-4.1/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140C CM4.1	Samples
LM4140CCMX-1.0/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140C CM1.0	Samples
LM4140CCMX-1.2/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140C CM1.2	Samples
LM4140CCMX-2.5/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140C CM2.5	Samples
LM4140CCMX-4.1/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140C CM4.1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

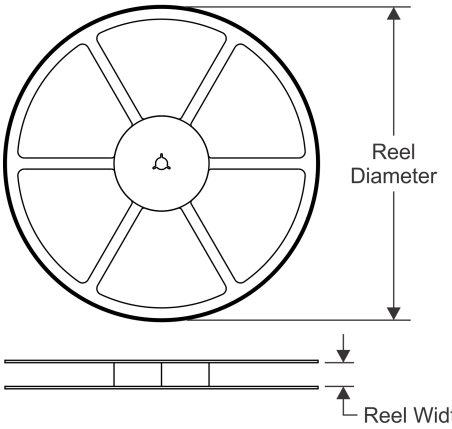
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

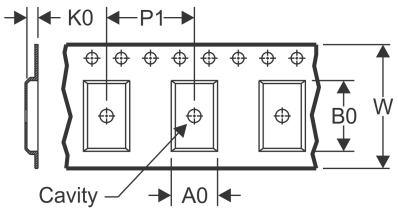
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

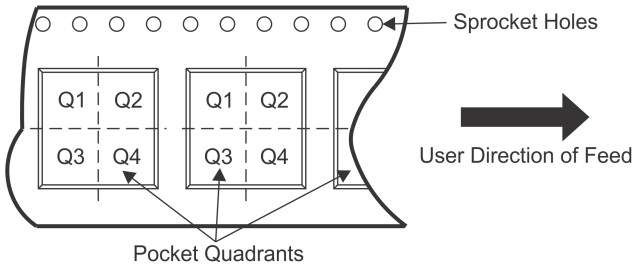


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

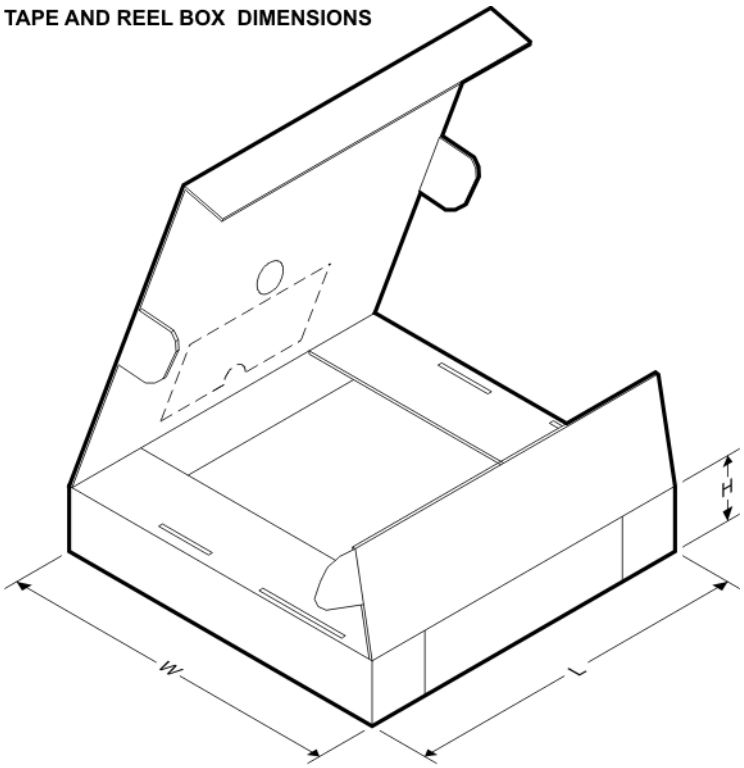
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

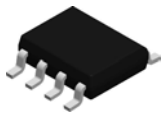
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4140ACMX-2.5/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4140ACMX-4.1/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4140BCMX-1.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4140BCMX-2.5/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4140BCMX-4.1/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4140CCMX-1.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4140CCMX-1.2/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4140CCMX-2.5/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4140CCMX-4.1/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4140ACMX-2.5/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM4140ACMX-4.1/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM4140BCMX-1.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM4140BCMX-2.5/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM4140BCMX-4.1/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM4140CCMX-1.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM4140CCMX-1.2/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM4140CCMX-2.5/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM4140CCMX-4.1/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

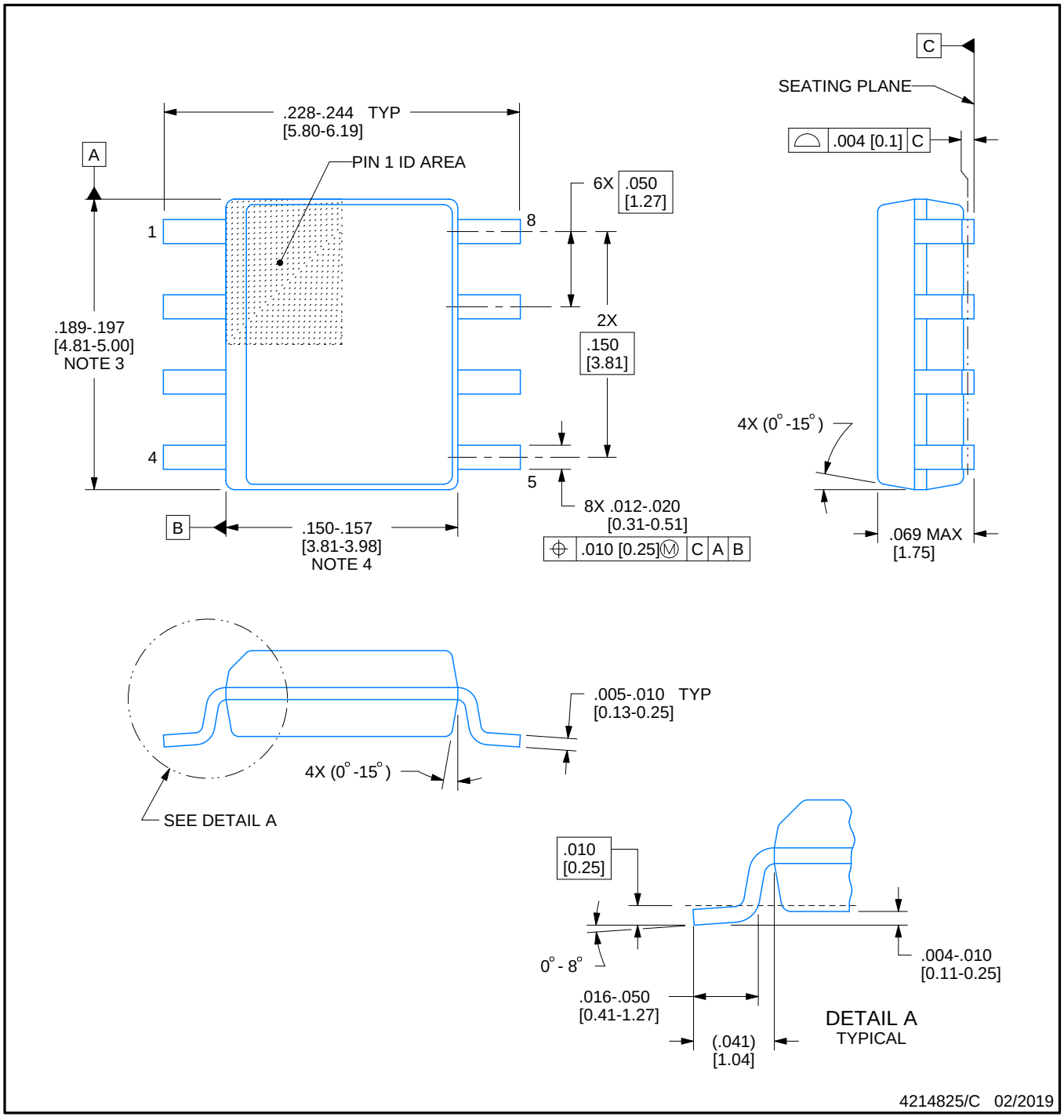


PACKAGE OUTLINE

D0008A

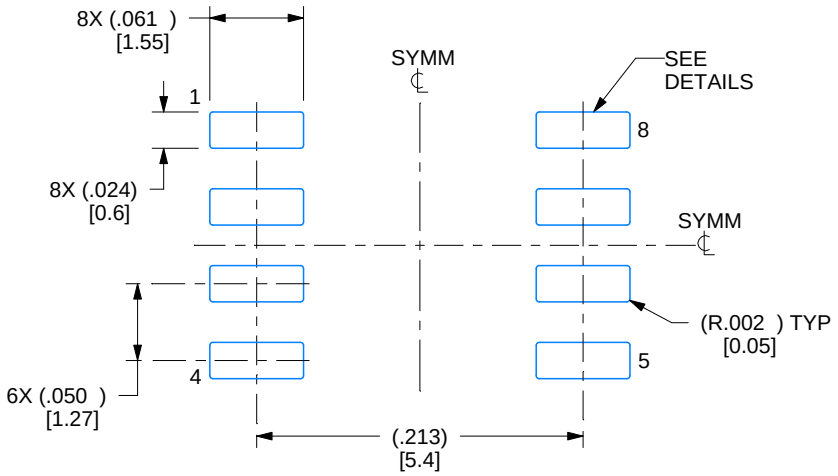
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

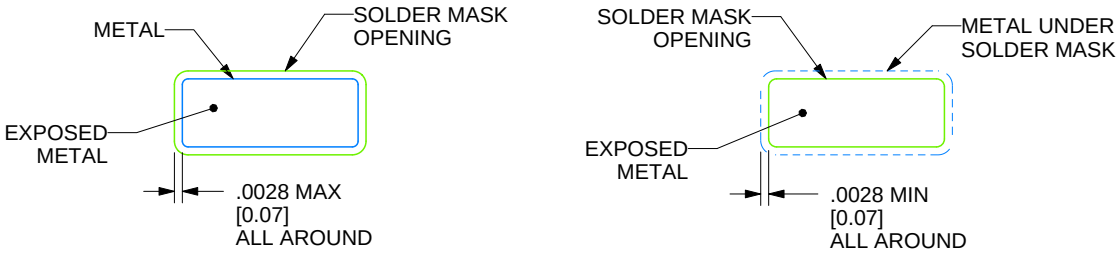


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

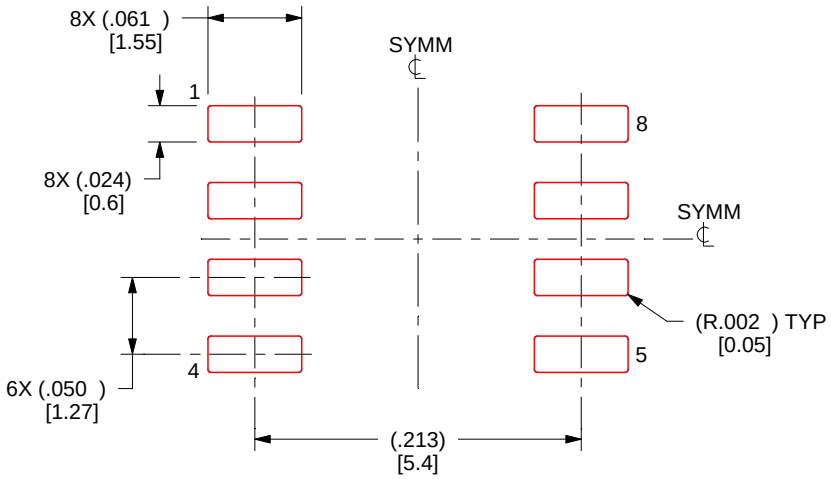
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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