



THE DATASHEET OF LM5030MM/NOPB



LM5030 100-V Push-Pull Current Mode PWM Controller

1 Features

- Internal High-Voltage Start-Up Regulator
- Single Resistor Oscillator Setting
- Synchronizable
- Error Amplifier
- Precision Reference
- Adjustable Softstart
- Dual Mode Overcurrent Protection
- Slope Compensation
- Direct Optocoupler Interface
- 1.5-A Peak Gate Drivers
- Thermal Shutdown

2 Applications

- Telecommunication Power Converters
- Industrial Power Converters
- +42-V Automotive Systems

3 Description

The LM5030 high-voltage PWM controller contains all of the features needed to implement push-pull and bridge topologies, using current-mode control in a small 10-pin package. This device provides two alternating gate driver outputs. The LM5030 includes a high-voltage start-up regulator that operates over a wide input range of 14 V to 100 V. Additional features include: error amplifier, precision reference, dual mode current limit, slope compensation, softstart, sync capability, and thermal shutdown. This high speed IC has total propagation delays less than 100 ns and a 1-MHz capable single-resistor adjustable oscillator.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|------------|-------------------|
| LM5030 | VSSOP (10) | 3.00 mm x 3.00 mm |
| | WSON (10) | 4.00 mm x 4.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Diagram

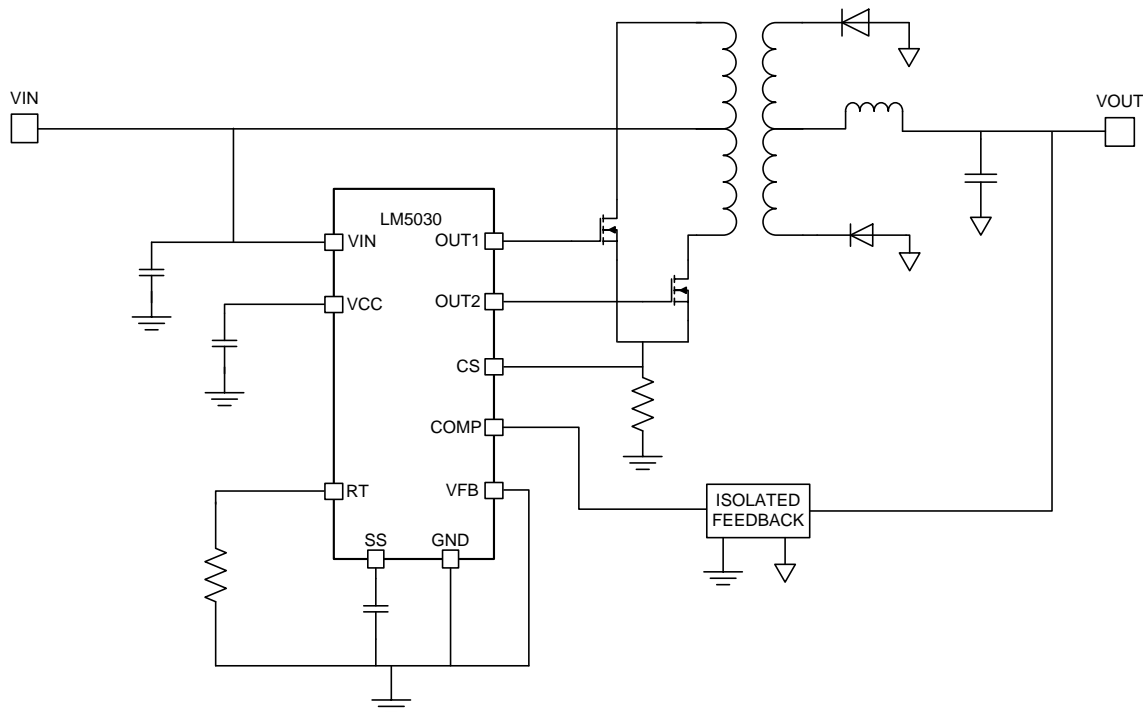


Table of Contents

| | | | |
|--|-----------|--|-----------|
| 1 Features | 1 | 7.4 Device Functional Modes..... | 13 |
| 2 Applications | 1 | 8 Application and Implementation | 14 |
| 3 Description | 1 | 8.1 Application Information..... | 14 |
| 4 Revision History | 2 | 8.2 Typical Application | 14 |
| 5 Pin Configuration and Functions | 3 | 9 Power Supply Recommendations | 20 |
| 6 Specifications | 4 | 10 Layout | 20 |
| 6.1 Absolute Maximum Ratings | 4 | 10.1 Layout Guidelines | 20 |
| 6.2 ESD Ratings..... | 4 | 10.2 Layout Example | 20 |
| 6.3 Recommended Operating Conditions..... | 4 | 11 Device and Documentation Support | 21 |
| 6.4 Thermal Information | 4 | 11.1 Device Support..... | 21 |
| 6.5 Electrical Characteristics..... | 5 | 11.2 Documentation Support | 21 |
| 6.6 Typical Characteristics..... | 8 | 11.3 Community Resources..... | 21 |
| 7 Detailed Description | 10 | 11.4 Trademarks | 21 |
| 7.1 Overview | 10 | 11.5 Electrostatic Discharge Caution..... | 21 |
| 7.2 Functional Block Diagram | 10 | 11.6 Glossary | 21 |
| 7.3 Feature Description..... | 11 | 12 Mechanical, Packaging, and Orderable Information | 21 |

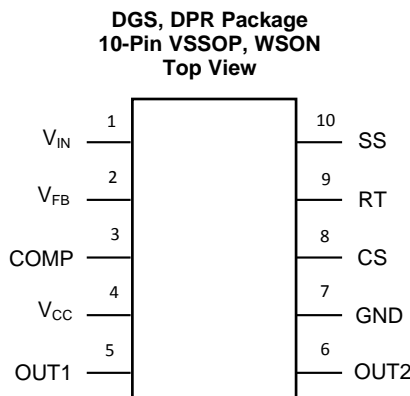
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision C (March 2013) to Revision D | Page |
|--|-------------|
| <ul style="list-style-type: none"> Added <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section..... | 1 |

| Changes from Revision B (March 2013) to Revision C | Page |
|--|-------------|
| <ul style="list-style-type: none"> Changed layout of National Data Sheet to TI format | 16 |

5 Pin Configuration and Functions



Pin Functions

| PIN | | I/O | DESCRIPTION | APPLICATION INFORMATION |
|-----------------|-----|-----|--|---|
| NAME | NO. | | | |
| COMP | 3 | O | Output to the error amplifier | There is an internal 5-kΩ pullup resistor on this pin. The error amplifier provides an active sink. |
| CS | 8 | I | Current sense input | Current sense input for current mode control and current limit sensing. Using separate dedicated comparators, if CS exceeds 0.5 V, the outputs will go into cycle-by-cycle current limit. If CS exceeds 0.625 V the outputs will be disabled and a softstart commenced. |
| GND | 7 | — | Return | Ground |
| OUT1 | 5 | O | Output of the PWM controller | Alternating PWM output gate driver |
| OUT2 | 6 | O | Output of the PWM controller | Alternating PWM output gate driver |
| RT | 9 | I | Oscillator timing resistor pin and synchronization input | An external resistor sets the oscillator frequency. This pin will also accept synchronization pulses from an external oscillator. |
| SS | 10 | I | Dual purpose soft start and shutdown pin | A 10-μA current source and an external capacitor set the softstart timing length. The controller will enter a low power state if the SS pin is pulled below the typical shutdown threshold of 0.45 V. |
| V _{IN} | 1 | I | Source input voltage | Input to start-up regulator. Input range 14 to 100 V. |
| V _{FB} | 2 | I | Inverting input to the error amplifier | The non-inverting input is internally connected to a 1.25-V reference. |
| V _{CC} | 4 | I/O | Output from the internal high-voltage series pass regulator. The regulation setpoint is 7.7 V. | If an auxiliary winding raises the voltage on this pin above the regulation setpoint, the internal series pass regulator will shutdown, reducing the IC power dissipation. |
| WSON DAP | SUB | — | Die substrate | The exposed die attach pad on the WSON package should be connected to a PCB thermal pad at ground potential. For additional information on using TI's No Pull Back WSON package, refer to WSON Application Note AN-1187 (SNOA401). |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

| | MIN | MAX | UNIT |
|--|--------------------|-----|------|
| V _{IN} to GND (Survival) | –0.3 | 100 | V |
| V _{CC} to GND (Survival) | –0.3 | 16 | V |
| RT to GND (Survival) | –0.3 | 5.5 | V |
| All other pins to GND (Survival) | –0.3 | 7 | V |
| Power dissipation | Internally Limited | | |
| Lead temperature (soldering 4 seconds) | | 260 | °C |
| Operating junction temperature | | 150 | °C |
| Storage temperature, T _{stg} | –55 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

| | | VALUE | UNIT |
|--|---|-------|------|
| V _(ESD) Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V |
| | Machine model (MM) | ±200 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|---|-----|-----|-----|------|
| V _{IN} | 14 | | 90 | V |
| T _J Operating junction temperature | –40 | | 105 | °C |

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | LM5030 | | UNIT |
|-------------------------------|--|-------------|------------|------|
| | | DGS (VSSOP) | DPR (WSON) | |
| | | 10 PINS | 10 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 158.8 | 38.1 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 53.6 | 137.1 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 74.8 | 15.2 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 5.3 | 0.4 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 77.6 | 15.4 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | — | 4.6 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

Specifications are for $T_J = 25^\circ\text{C}$. Unless otherwise specified: $V_{IN} = 48\text{ V}$, $V_{CC} = 10\text{ V}$, and $R_T = 26.7\text{ k}\Omega$

| PARAMETER | | TEST CONDITIONS | | MIN ⁽¹⁾ | TYP ⁽²⁾ | MAX ⁽¹⁾ | UNIT |
|-----------------------------------|---|--|---|------------------------------------|--------------------|------------------------------------|---------------|
| START-UP REGULATOR | | | | | | | |
| $V_{CC\text{Reg}}$ | V_{CC} Regulation | Open ckt | $T_J = 25^\circ\text{C}$ | 7.7 | | 8.0 | V |
| | | | full operating junction temperature range | 7.4 | | | |
| V_{CC} | Current limit | See Figure 2 | $T_J = 25^\circ\text{C}$ | 17 | | 10 | mA |
| | | | full operating junction temperature range | | | | |
| $I_{-V_{IN}}$ | Start-up regulator leakage (external V_{CC} supply) | $V_{IN} = 90\text{ V}$ | $T_J = 25^\circ\text{C}$ | 150 | | 500 | μA |
| | | | full operating junction temperature range | | | | |
| I_{IN} | Shutdown current | SS = 0 V, $V_{CC} =$ open | $T_J = 25^\circ\text{C}$ | 250 | | 350 | μA |
| | | | full operating junction temperature range | | | | |
| V_{CC} SUPPLY | | | | | | | |
| V_{CC} | Undervoltage lockout voltage | $T_J = 25^\circ\text{C}$ | | $V_{CC\text{Reg}} - 100\text{ mV}$ | | $V_{CC\text{Reg}} - 300\text{ mV}$ | V |
| | | | full operating junction temperature range | | | | |
| | Undervoltage hysteresis | $T_J = 25^\circ\text{C}$ | | 1.6 | | 2.1 | V |
| | | | full operating junction temperature range | 1.2 | | | |
| I_{CC} | Supply current | $C_{\text{load}} = 0$ | $T_J = 25^\circ\text{C}$ | 2 | | 3 | mA |
| | | | full operating junction temperature range | | | | |
| ERROR AMPLIFIER | | | | | | | |
| GBW | Gain bandwidth | | | 4 | | | MHz |
| | DC gain | | | 75 | | | dB |
| Input voltage | $V_{FB} = \text{COMP}$ | $T_J = 25^\circ\text{C}$ | | 1.245 | | 1.270 | V |
| | | | full operating junction temperature range | 1.220 | | | |
| COMP sink capability | $V_{FB} = 1.5\text{ V COMP} = 1\text{ V}$ | $T_J = 25^\circ\text{C}$ | | 13 | | 5 | mA |
| | | | full operating junction temperature range | | | | |
| CURRENT LIMIT | | | | | | | |
| CS1 | Cycle-by-cyble CS threshold voltage | $T_J = 25^\circ\text{C}$ | | 0.5 | | 0.55 | V |
| | | | full operating junction temperature range | 0.45 | | | |
| CS2 | Restart CS threshold voltage | Resets SS capacitor; auto restart | $T_J = 25^\circ\text{C}$ | 0.625 | | 0.675 | V |
| | | | full operating junction temperature range | 0.575 | | | |
| | ILIM delay to output | CS step from 0-V to 0.6-V time-to-onset of OUT transition (90%) $C_{\text{load}} = 0$ | | 30 | | | ns |
| CS sink current (clocked) | CS = 0.3 V | $T_J = 25^\circ\text{C}$ | | 6 | | 3 | mA |
| | | | full operating junction temperature range | | | | |

- (1) Limits are 100% production tested at 25°C . Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL).
- (2) Typical numbers represent the most likely parametric norm for 25°C operation.

Electrical Characteristics (continued)

 Specifications are for $T_J = 25^\circ\text{C}$. Unless otherwise specified: $V_{IN} = 48\text{ V}$, $V_{CC} = 10\text{ V}$, and $R_T = 26.7\text{ k}\Omega$

| PARAMETER | TEST CONDITIONS | | MIN ⁽¹⁾ | TYP ⁽²⁾ | MAX ⁽¹⁾ | UNIT |
|--------------------------------|--|---|--------------------|--------------------|--------------------|---------------|
| SOFT START AND SHUTDOWN | | | | | | |
| Softstart current source | $T_J = 25^\circ\text{C}$ | | 10 | | | μA |
| | full operating junction temperature range | | 7 | | 13 | |
| Softstart to COMP offset | $T_J = 25^\circ\text{C}$ | | 0.5 | | | V |
| | full operating junction temperature range | | 0.25 | | 0.75 | |
| Shutdown threshold | $T_J = 25^\circ\text{C}$ | | 0.45 | | | V |
| | full operating junction temperature range | | 0.2 | | 0.7 | |
| OSCILLATOR | | | | | | |
| Frequency1 (RT = 26.7K) | $T_J = 25^\circ\text{C}$ | | 200 | | | kHz |
| | full operating junction temperature range | | 175 | | 225 | |
| Frequency2 (RT = 8.2K) | $T_J = 25^\circ\text{C}$ | | 600 | | | kHz |
| | full operating junction temperature range | | 510 | | 690 | |
| Sync threshold | $T_J = 25^\circ\text{C}$ | | 3.2 | | | V |
| | full operating junction temperature range | | | | 3.8 | |
| PWM COMPARATOR | | | | | | |
| Delay to output | COMP set to 2-V CS stepped 0 to 0.4 V, time-to-onset of OUT transition low | | 30 | | | ns |
| Max duty cycle | Inferred from deadtime | $T_J = 25^\circ\text{C}$ | 49% | | | |
| | | full operating junction temperature range | 47.5% | | 50% | |
| Min duty cycle | COMP = 0 V | full operating junction temperature range | 0% | | | |
| COMP to PWM comparator gain | | | 0.34 | | | V / V |
| COMP open circuit voltage | $V_{FB} = 0\text{ V}$ | $T_J = 25^\circ\text{C}$ | 5.2 | | | V |
| | | full operating junction temperature range | 4.3 | | 6.1 | |
| COMP short circuit current | $V_{FB} = 0\text{ V}$, COMP = 0 V | $T_J = 25^\circ\text{C}$ | 1.1 | | | mA |
| | | full operating junction temperature range | 0.6 | | 1.5 | |
| SLOPE COMPENSATION | | | | | | |
| Slope comp amplitude | Delta increase at PWM Comparator to CS | $T_J = 25^\circ\text{C}$ | 105 | | | mV |
| | | full operating junction temperature range | 80 | | 130 | |
| OUTPUT SECTION | | | | | | |
| Deadtime | $C_{load} = 0, 10\% \text{ to } 10\%$ | $T_J = 25^\circ\text{C}$ | 135 | | | ns |
| | | full operating junction temperature range | 85 | | 185 | |
| Output high saturation | $I_{out} = 50\text{ mA}$, $V_{CC} - V_{OUT}$ | $T_J = 25^\circ\text{C}$ | 0.25 | | | V |
| | | full operating junction temperature range | | | 0.75 | |
| Output low saturation | $I_{OUT} = 100\text{ mA}$ | $T_J = 25^\circ\text{C}$ | 0.25 | | | V |
| | | full operating junction temperature range | | | 0.75 | |
| Rise time | $C_{load} = 1\text{ nF}$ | 16 | | | ns | |
| Fall time | $C_{load} = 1\text{ nF}$ | 16 | | | ns | |

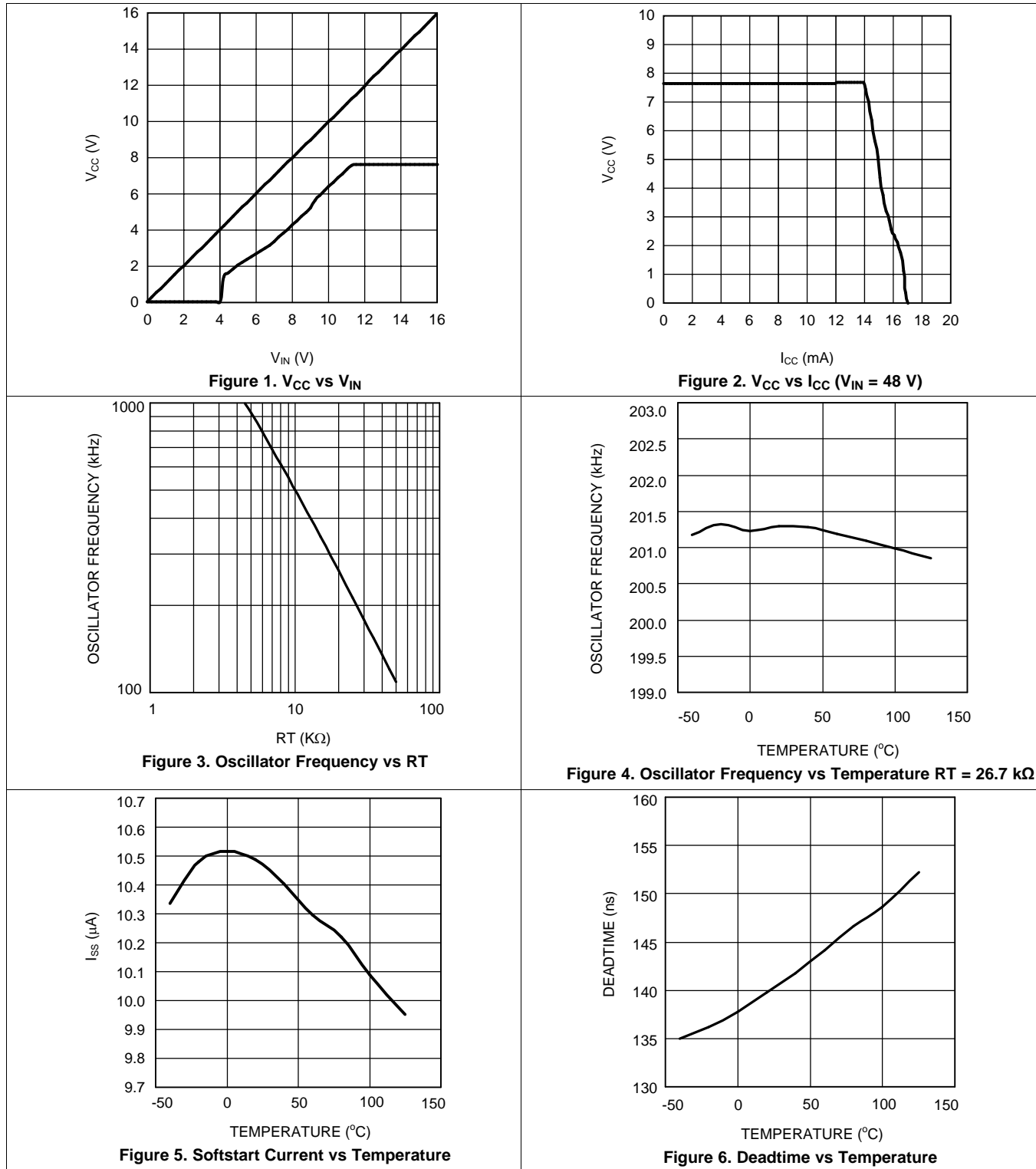
Electrical Characteristics (continued)

 Specifications are for $T_J = 25^\circ\text{C}$. Unless otherwise specified: $V_{IN} = 48\text{ V}$, $V_{CC} = 10\text{ V}$, and $R_T = 26.7\text{ k}\Omega$

| PARAMETER | | TEST CONDITIONS | MIN ⁽¹⁾ | TYP ⁽²⁾ | MAX ⁽¹⁾ | UNIT |
|-------------------------|------------------------------|-----------------|--------------------|--------------------|--------------------|------------------|
| THERMAL SHUTDOWN | | | | | | |
| T_{sd} | Thermal shutdown temperature | | | 165 | | $^\circ\text{C}$ |
| | Thermal shutdown hysteresis | | | 15 | | $^\circ\text{C}$ |

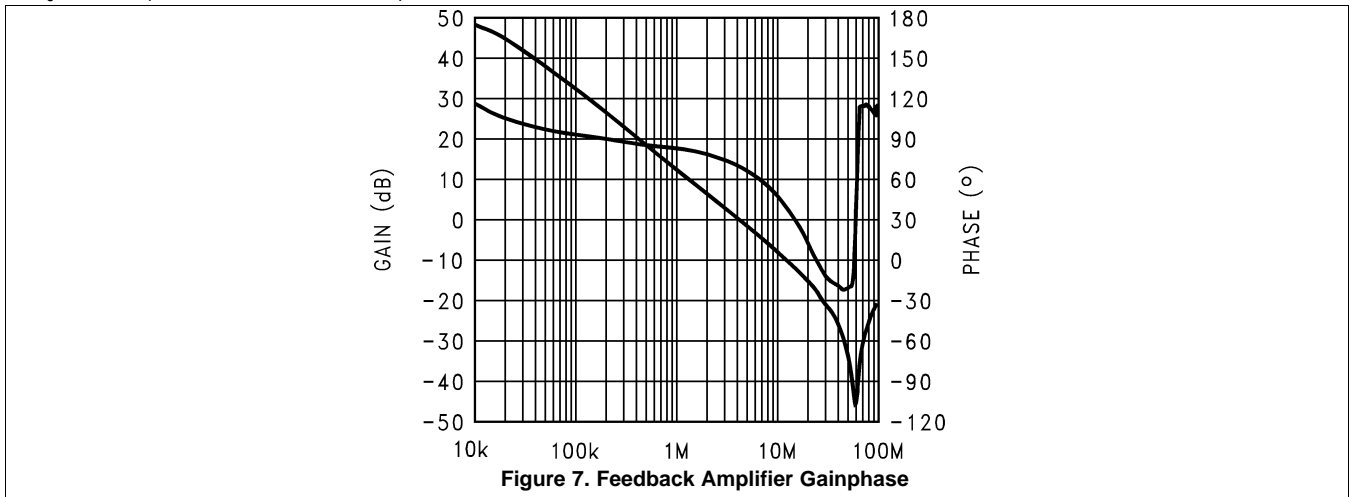
6.6 Typical Characteristics

at $T_J = 25^\circ\text{C}$ (unless otherwise noted)



Typical Characteristics (continued)

at $T_J = 25^\circ\text{C}$ (unless otherwise noted)



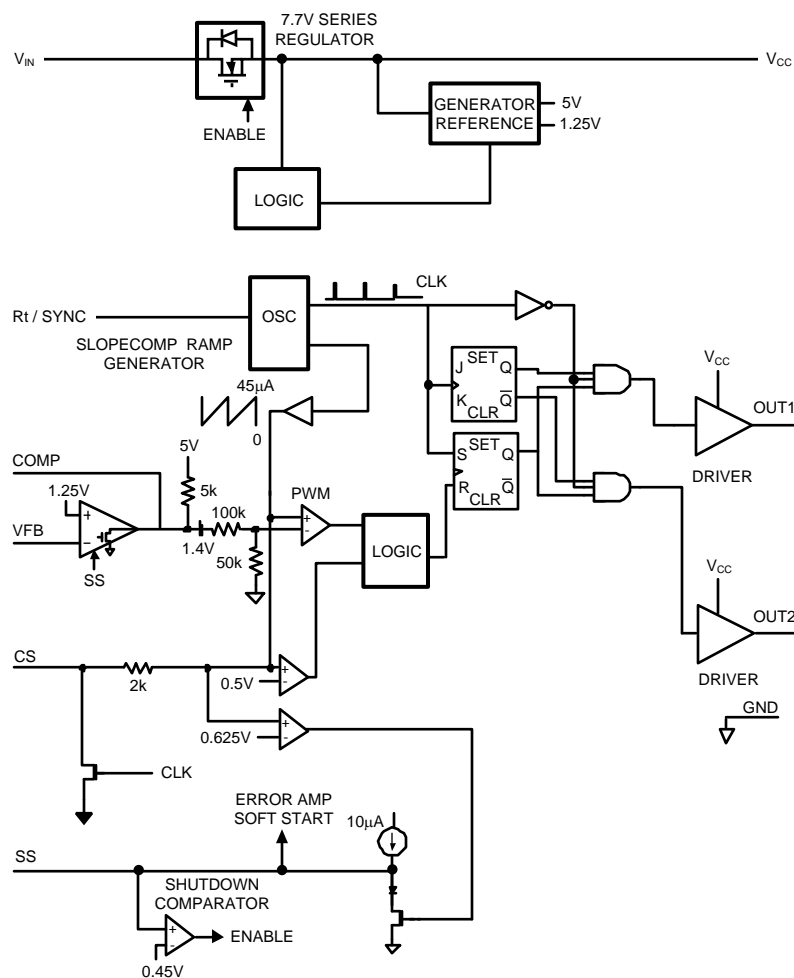
7 Detailed Description

7.1 Overview

The LM5030 high-voltage PWM controller contains all of the features needed to implement push-pull and bridge topologies, using current-mode control in a small 10-pin package. Features included are, start-up regulator, dual mode current limit, dual alternating gate drivers, thermal shutdown, softstart, and slope compensation. This high speed IC has total propagation delays < 100 ns. The functional block diagram of the LM5030 is shown in [Functional Block Diagram](#).

The LM5030 is designed for current-mode control converters that require alternating outputs, such as push-pull and half- and full-bridge topologies. The features included in the LM5030 enable all of the advantages of current-mode control, line feed-forward, cycle-by-cycle current limit, and simplified loop compensation. The oscillator ramp is internally buffered and added to the PWM comparator input to provide the necessary slope compensation for current-mode control at higher duty cycles.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 High-Voltage Start-Up Regulator

The LM5030 contains an internal high-voltage start-up regulator. The input pin (V_{IN}) can be connected directly to line voltages as high as 100 V. The regulator output is internally current limited to 10 mA. Upon power up, the regulator is enabled and sources current into an external capacitor connected to the V_{CC} pin. The recommended capacitance range for the V_{CC} regulator is 0.1 μF to 50 μF . When the voltage on the V_{CC} pin reaches the regulation point of 7.7 V, the controller outputs are enabled. The outputs will remain enabled unless, V_{CC} falls below 6.1 V or if the SS/SHUTDOWN pin is pulled to ground or an over temperature condition occurs. In typical applications, an auxiliary transformer winding is diode connected to the V_{CC} pin. This winding raises the V_{CC} voltage greater than 8 V, effectively shutting off the internal start-up regulator and saving power while reducing the controller dissipation. The external V_{CC} capacitor must be sized such that the self-bias will maintain a V_{CC} voltage greater than 6.1 V during the initial start-up. During a fault mode when the converter self bias winding is inactive, external current draw on the V_{CC} line should be limited as to not exceed the maximum power dissipation of the controller. An external start-up or other bias rail can be used instead of the internal start-up regulator by connecting the V_{CC} and the V_{in} pins and feeding the external bias voltage (8 V to 15 V) to that node.

7.3.2 Error Amplifier

An internal high gain error amplifier is provided within the LM5030. The noninverting reference of the amplifier is tied to 1.25 V. In nonisolated applications the power converter output is connected to the VFB pin via the voltage setting resistors and loop compensation is connected between the COMP and VFB pins.

For most isolated applications the error amplifier function is implemented on the secondary side ground. Because the internal error amplifier is configured as an open drain output it can be disabled by connecting VFB to ground. The internal 5-k Ω pullup resistor, connected between the 5-V reference and COMP, can be used as the pullup for an optocoupler or other isolation device.

7.3.3 PWM Comparator

The PWM comparator compares the compensated current ramp signal to the loop error voltage from the internal error amplifier (COMP pin). This comparator is optimized for speed in order to achieve minimum discernable duty cycles. The comparator polarity is such that 0 V on the COMP pin will cause a zero duty cycle.

7.3.4 Current Limit and Current Sense

The LM5030 contains two levels of over-current protection. If the voltage on the current sense comparator exceeds 0.5 V the present cycle is terminated (cycle-by-cycle current limit). If the voltage on the current sense comparator exceeds 0.625 V, the controller will terminate the present cycle and discharge the softstart capacitor. A small RC filter, located near the controller, is recommended for the CS pin. An internal MOSFET discharges the current sense filter capacitor at the conclusion of every cycle, to improve dynamic performance.

The LM5030 CS and PWM comparators are very fast, and as such will respond to short duration noise pulses. Layout considerations are critical for the current sense filter and sense resistor. The capacitor associated with the CS filter must be placed very close to the device and connected directly to the pins of the IC (CS and RTN). Also if a current sense transformer is used, both leads of the transformer secondary should be routed to the sense resistor, which should also be located close to the IC. If a current sense resistor located in the drive transistor sources is used, for current sense, a low inductance resistor should be chosen. In this case all of the noise sensitive low power grounds should be commoned together around the IC and then a single connection should be made to the power ground (sense resistor ground point).

The second level threshold is intended to protect the power converter by initiating a low duty cycle hiccup mode when abnormally high, fast rising currents occur. During excessive loading, the first level threshold will always be reached and the output characteristic of the converter will be that of a current source but this sustained current level can cause excessive temperatures in the power train especially the output rectifiers. If the second level threshold is reached, the softstart capacitor will be fully discharged, a retry will commence following the discharge detection. The second level threshold will only be reached when a high dV/dt is present at the current sense pin. The signal must be fast enough to reach the second level threshold before the first threshold detector turns off the driver. This can usually happen for a saturated power inductor or shorted load. Excessive filtering on the CS pin, extremely low value current sense resistor or an inductor that does not saturate with excessive loading may prevent the second level threshold from ever being reached.

Feature Description (continued)

7.3.5 Oscillator, Shutdown and Sync Capability

The LM5030 oscillator is set by a single external resistor connected between the RT pin and return. To set a desired oscillator frequency, the necessary RT resistor can be calculated in [Equation 1](#):

$$RT = \frac{(1/F) - 172 \times 10^{-9}}{182 \times 10^{-12}} \quad (1)$$

Each output switches at half the oscillator frequency in a push-pull configuration. The LM5030 can also be synchronized to an external clock. The external clock must be of higher frequency than the free running frequency set by the RT resistor. The clock signal should be capacitively coupled into the RT pin with a 100-pF capacitor. A peak voltage level greater than 3 V with respect to ground is required for detection of the sync pulse. The sync pulse width should be set in the 15- to 150-ns range by the external components. The RT resistor is always required, whether the oscillator is free running or externally synchronized. The voltage at the RT pin is internally regulated to a nominal 2 V.

Locate the RT resistor close to the device and connected directly to the pins of the IC (RT and GND).

7.3.6 Slope Compensation

The PWM comparator compares the current sense signal to the voltage derived from the COMP pin. The COMP voltage is set by either the internal error amplifier or an external error amplifier through an optocoupler. At duty cycles greater than 50% (composite of alternating outputs) current mode control circuits are prone to subharmonic oscillation. By adding an additional ramp signal to the current sense ramp signal this condition can be avoided. The LM5030 integrates this slope compensation by buffering the internal oscillator ramp and summing it internally to the current sense (CS) signal. Additional slope compensation may be added by increasing the source impedance of the current sense signal.

7.3.7 Soft Start and Shutdown

The soft-start feature allows the converter to gradually reach the initial steady state operating point, thus reducing start-up stresses and surges. An internal 10-μA current source and an external capacitor generate a ramping voltage signal that limits the error amplifier output during start-up. In the event of a second level current limit fault, the soft-start capacitor will be fully discharged which disables the output drivers. When the fault condition is no longer present, the soft-start capacitor is released to ramp and gradually restart the converter. The SS pin can also be used to disable the controller. If the SS pin voltage is pulled down below 0.45 V (nominal) the controller will disable the outputs and enter a low power state.

7.3.8 OUT1, OUT2, and Time Delay

The LM5030 provides two alternating outputs, OUT1 and OUT2. The internal gate drivers can each sink 1.5-A peak each. The maximum duty cycle for each output is inherently limited to less than 50%. The typical deadtime between the falling edge of one gate driver output and the rising edge of the other gate driver output is 135 ns.

7.3.9 Thermal Protection

Internal thermal-shutdown circuitry is provided to protect the integrated circuit in the event the excessive junction temperature. When activated, typically at 165°C, the controller is forced into a low-power reset state, disabling the output drivers and the bias regulator. This feature is provided to prevent catastrophic failures from accidental device overheating.

7.4 Device Functional Modes

The LM5030 is a versatile PWM controller that can be used in the following functional modes:

- The LM5030 provides a complete push-pull current mode controller.
- The LM5030 driver outputs can be configured to drive high side MOSFETs through a gate driver chip to implement half and full bridge topologies.
- The LM5030 can be configured in single ended outputs such as a flyback converter or boost.
- The LM5030 can also operate in conjunction with a high side driver chip to implement a synchronous buck converter.

Details of these circuits can be found in *Versatility of the LM5030 PWM Push-Pull Controller*, [SNVA548](#).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM5030 is a highly integrated PWM controller that contains all of the features necessary for implementing push-pull topology power converters. The device targets DC-DC converter applications with input voltages of up to 100 VDC and output power in the range 15 W to 150 W.

8.2 Typical Application

The schematic in [Figure 8](#) shows an example of a 33-W push-pull converter controlled by a LM5030. The operating input range is 36 V to 75 V, and the output voltage is 3.3 V. The output current capability is 10 A. The converter is configured for input current protection with cycle-by-cycle current limit. An auxiliary winding is used to raise the VCC voltage to reduce the controller power dissipation.



Figure 8. Typical Application Circuit, 36-V to 75-V IN and 3.3-V, 10-A OUT

Typical Application (continued)

8.2.1 Design Requirements

For this design example, use the input parameters listed in [Table 1](#).

Table 1. Design Parameters

| PARAMETER | MIN | NOM | MAX | UNIT |
|------------------------|-----|-------|-----|------|
| Input Voltage | 36 | | 75 | V |
| Output Voltage | | 3.3 | | V |
| Output Current | 0 | | 10 | A |
| Efficiency (Full Load) | | 82.5% | | |
| Efficiency (Half Load) | | 84.5% | | |
| Load Regulation | | 1% | | |
| Line Regulation | | 0.15% | | |
| Output Current Limit | | 11 | | A |

8.2.2 Detailed Design Procedure

8.2.2.1 V_{CC}

While the LM5030 internally generates a voltage at V_{CC} (7.7 V), the internal regulator is used mainly during the start-up sequence. Once the load current begins flowing through L2, which is both an inductor for the output filter and a transformer, a voltage is generated at the secondary of L2, which powers the V_{CC} pin. When the externally applied voltage exceeds the internal value (7.7 V), the internal regulator shuts off, thereby reducing internal power dissipation in the LM5030. L2 is constructed such that the voltage supplied to V_{CC} ranges from approximately 10.6 V to approximately 11.3 V, depending on the load current (see [Figure 9](#)).

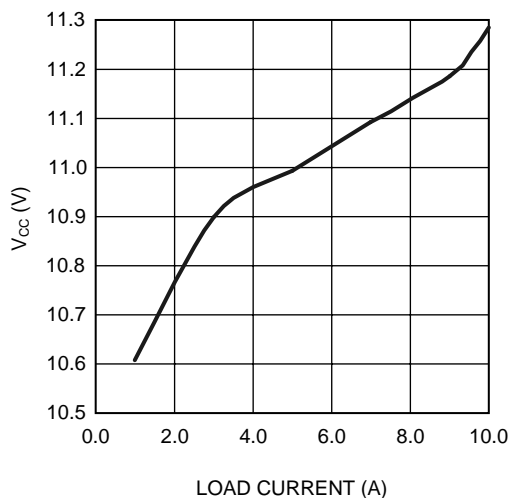
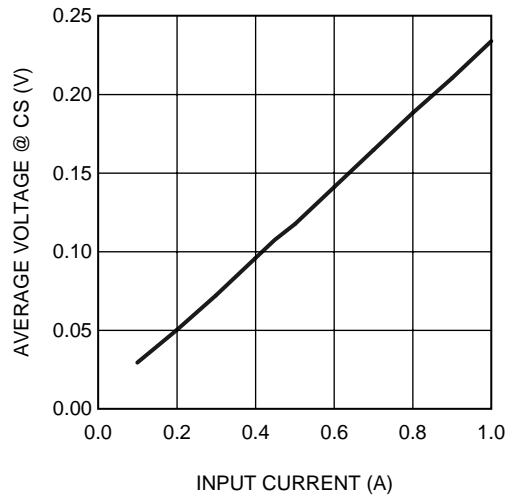


Figure 9. V_{CC} Voltage vs Load Current

8.2.2.2 Current Sense

Monitoring the input current provides a good indication of the operation of the circuit. If an overload condition should exist at the output (a partial overload or a short circuit), the input current would rise above the nominal value shown in [Figure 12](#). Transformer T2, in conjunction with D3, R9, R12 and C10, provides a voltage to pin 8 on the LM5030 (CS) which is representative of the input current flowing through its primary. The average voltage seen at pin 8 is plotted in [Figure 10](#). If the voltage at the first current sense comparator exceeds 0.5 V, the LM5030 disables its outputs, and the circuit enters a cycle-by-cycle current limit mode. If the second level threshold (0.625 V) is exceeded due to a severe overload and transformer saturation, the LM5030 will disable its outputs and initiate a softstart sequence. However, the very short propagation delay of the cycle-by-cycle current limiter (CS1), the design of the CS filter (R9, R12, and C10), and the conservative design of the output inductor (L2), may prevent the second level current threshold from being realized on this evaluation board.


Figure 10. Average Voltage at the CS Pin vs Input Current

8.2.2.3 Shutdown

The Shutdown pad (SD) on the board connects to the SoftStart pin on the LM5030 (pin 10), and permits on/off control of the converter by an external switch. SD should be pulled below 0.45 V, with an open collector or open drain device, to shut down the LM5030 outputs and the VCC regulator. If the voltage at the SD pad is between 1.0 and 1.5 V, a partial-on condition results, which could be disruptive to the system. Therefore, the voltage at the SD pad should transition quickly between its open circuit voltage (4.9 V) and ground.

8.2.2.4 External Sync

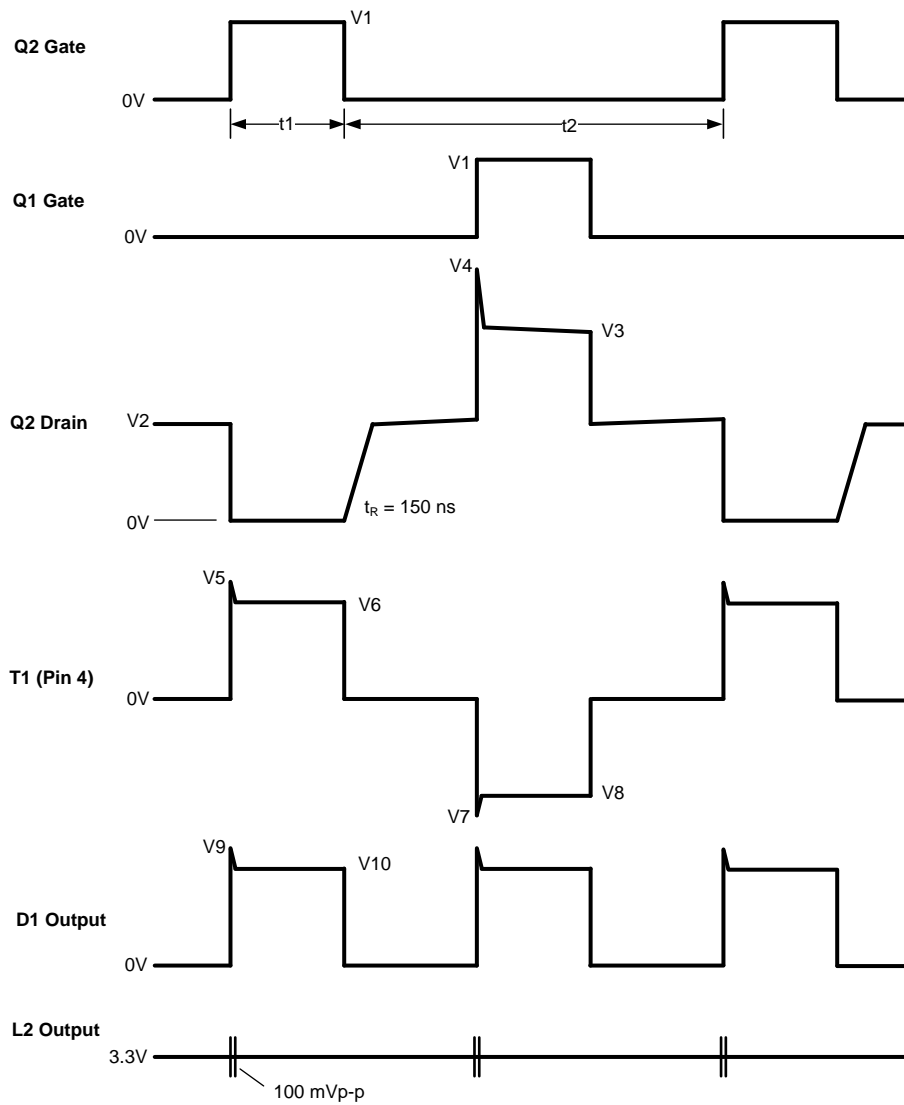
Although the LM5030 includes an internal oscillator, its operating frequency can be synchronized to an external signal if desired. The external source frequency must be higher than the internal frequency set with the RT resistor (262 kHz with $R_T = 20$ k Ω). The sync input pulse width must be between 15 and 150 ns, and have an amplitude of 1.5 to 3.0 V at the Sync pad on the board. The pulses are coupled to the LM5030 through a 100-pF capacitor (C16) as specified in the data sheet.

Table 2. Bill of Materials

| ITEM | PART NUMBER | DESCRIPTION | VALUE |
|------|--------------------|------------------------|-----------------------|
| C 1 | C0805C472K5RAC | Capacitor, CER, KEMET | 4700 p, 50 V |
| C 2 | C0805C103K5RAC | Capacitor, CER, KEMET | 0.01 μ , 50 V |
| C 3 | C4532X7S0G686M | Capacitor, CER, TDK | 68 μ , 4 V |
| C 4 | T520D337M006AS4350 | Capacitor, TANT, KEMET | 330 μ , 6.3 V |
| C 5 | T520D337M006AS4350 | Capacitor, TANT, KEMET | 330 μ , 6.3 V |
| C 6 | C4532X7R3A103K | Capacitor, CER, TDK | 0.01 μ , 1000 V |
| C 7 | C3216X7R2A104K | Capacitor, CER, TDK | 0.1 μ , 100 V |
| C 8 | C4532X7R2A105M | Capacitor, CER, TDK | 1 μ , 100 V |
| C 9 | C4532X7R2A105M | Capacitor, CER, TDK | 1 μ , 100 V |
| C 10 | C0805C102K1RAC | Capacitor, CER, KEMET | 1000 p, 100 V |
| C 11 | C1206C223K5RAC | Capacitor, CER, KEMET | 0.022 μ , 50 V |
| C 12 | C3216X7R1E105M | Capacitor, CER, TDK | 1 μ , 25 V |
| C 13 | C3216COG2J221J | Capacitor, CER, TDK | 220 p, 630 V |
| C 14 | C3216COG2J221J | Capacitor, CER, TDK | 220 p, 630 V |
| C 15 | C1206C104K5RAC | Capacitor, CER, KEMET | 0.1 μ , 50 V |
| C 16 | C0805C101J1GAC | Capacitor, CER, KEMET | 100 p, 100 V |
| C 17 | C0805C101J1GAC | Capacitor, CER, KEMET | 100 p, 100 V |
| C 18 | C3216X7R1H334K | Capacitor, CER, TDK | 0.33 μ , 50 μ |

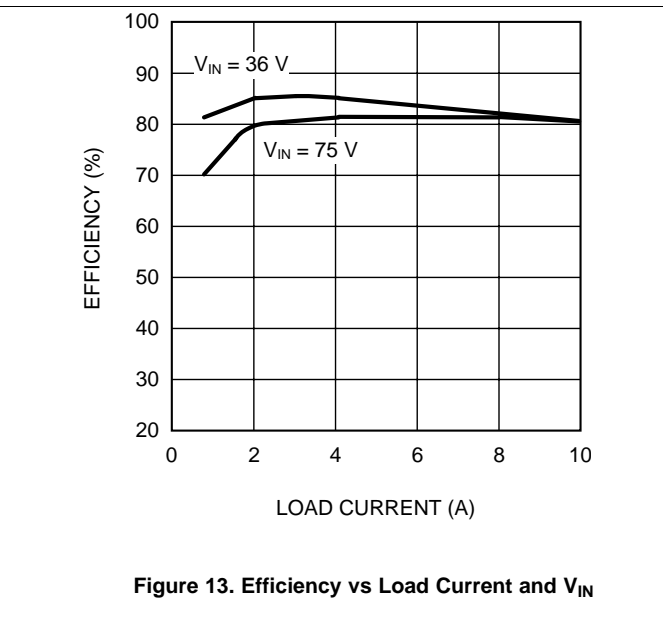
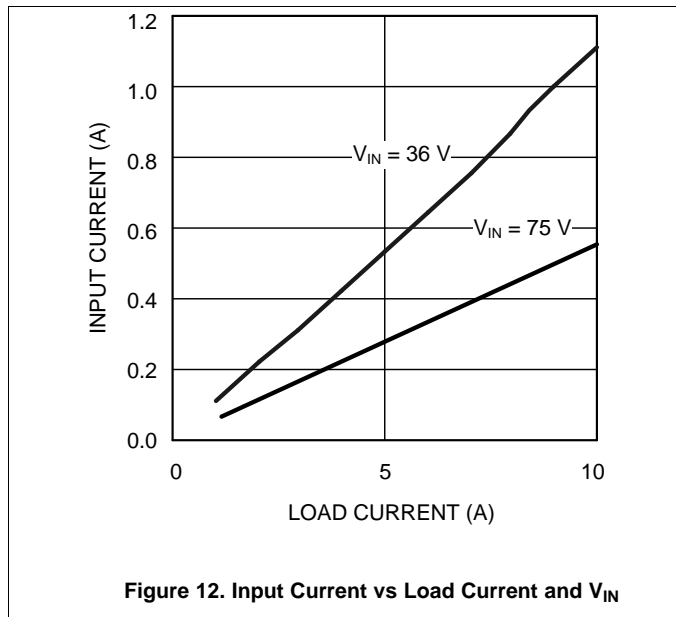
Table 2. Bill of Materials (continued)

| ITEM | | PART NUMBER | DESCRIPTION | VALUE |
|------|----|---------------|----------------------------------|-------------------|
| D | 1 | MBRB3030CTL | Diode, Schottky, ON | |
| D | 2 | CMPD2838-NSA | Diode, Signal, Central | |
| D | 3 | CMPD2838-NSA | Diode, Signal, Central | |
| D | 4 | CMPD2838-NSA | Diode, Signal, Central | |
| D | 5 | CMPD2838-NSA | Diode, Signal, Central | |
| L | 1 | MSS6132-103 | Input Choke, Coilcraft | 10 μ H, 1.5 A |
| L | 2 | A9785-B | Output Choke, Coilcraft | 7 μ H |
| R | 1 | CRCW12061R00F | Resistor | 1 |
| R | 2 | CRCW12064990F | Resistor | 499 |
| R | 3 | CRCW2512101J | Resistor | 100, 1 W |
| R | 4 | CRCW2512101J | Resistor | 100, 1 W |
| R | 5 | CRCW12064022F | Resistor | 40.2K |
| R | 6 | CRCW120610R0F | Resistor | 10 |
| R | 7 | CRCW120610R0F | Resistor | 10 |
| R | 8 | CRCW12061002F | Resistor | 10K |
| R | 9 | CRCW120623R7F | Resistor | 23.7 |
| R | 10 | CRCW12062002F | Resistor | 20K |
| R | 11 | CRCW120610R0F | Resistor | 10 |
| R | 12 | CRCW12063010F | Resistor | 301 |
| R | 13 | CRCW120610R0F | Resistor | 10 |
| R | 14 | CRCW12061001F | Resistor | 1K |
| TX | 1 | A9784-B | POWER XFR, COILCRAFT | |
| TX | 2 | P8208T | CURRENT XFR, Pulse | 100:1 |
| U1 | 1 | LM5030 | REGULATOR, TI | |
| U2 | 2 | MOCD207M | OPTO-COUPLER, QT OPTOELECTRONICS | |
| U3 | 3 | LM3411AM5-3.3 | REFERENCE, TI | |
| | | 651-1727010 | DUAL TERMINALS, MOUSER | 3 per ASSY |
| X | 1 | SUD19N20-90 | FET, N, 200 V, SILICONIX | |
| X | 2 | SUD19N20-90 | FET, N, 200 V, SILICONIX | |


Figure 11. Representative Waveforms
Table 3. Test Data

| V_{IN} | I_{OUT} | t_1 | t_2 | F_s | V_1 | V_2 | V_3 | V_4 | V_5 | V_6 | V_7 | V_8 | V_9 | V_{10} |
|----------|-----------|-------------|-------------|-------|--------|-------|-------|-------|-------|-------|-------|-------|-------|----------|
| 36 V | 1.0 A | 2.2 μ S | 5.3 μ S | 266.7 | 10.5 V | 36 V | 72 V | 90 V | 10 V | 6 V | -10 V | -6 V | 10 V | 6 V |
| 48 V | 10 A | 1.9 μ S | 5.5 μ S | 270.3 | 11.5 V | 48 V | 96 V | 130 V | 18 V | 8 V | -18 V | -8 V | 13 V | 8 V |
| 75 V | 1.0 A | 1.2 μ S | 6.2 μ S | 270.3 | 10.5 V | 75 V | 150 V | 200 V | 20 V | 13 V | -20 V | -13 V | 20 V | 13 V |

8.2.3 Application Curves



9 Power Supply Recommendations

The LM5030 can be used as a controller for push-pull, full bridge or half bridge power supplies. Typical applications are for input voltages up to 100 V and output power around 30 W with switching frequency up to 1 MHz.

Care should be taken that components with the correct current rating are chosen. This includes magnetic components, power MOSFETs and diodes, connectors and wire sizes. Input and output capacitors should have the correct ripple current rating.

The VCC pin requires a local decoupling capacitor that is connected to GND. This capacitor ensures stability of the internal regulator from the VIN pin. The decoupling capacitor also provides the current pulses to drive the gates of the external MOSFETs through the driver output pins.

Place the decoupling capacitor close to the VCC and GND pins and track it directly to these pins.

10 Layout

10.1 Layout Guidelines

As in all high frequency switching power supplies, it is important to separate the high current return trace from the low level GND signal of the controller. These signals should be connected together at a single point, usually the negative side of the DC input filter capacitor.

Layout considerations are critical for the current sense filter. If a current sense transformer is used, both leads of the transformer secondary should be routed to the sense filter components and to the device pins. If the current sense circuit employs a sense resistor in the power MOSFET source, a low inductance resistor should be used and all the low current traces should be connected in common near the device with a single connection made to the GND pin.

The gate drive outputs of the device should have short, direct paths to the power MOSFETs in order to minimize inductance in the gate path.

If the internal dissipation of the device produces a high junction temperature during normal operation, the use of multiple vias under the device to a ground plane can help conduct heat away from the device.

10.2 Layout Example

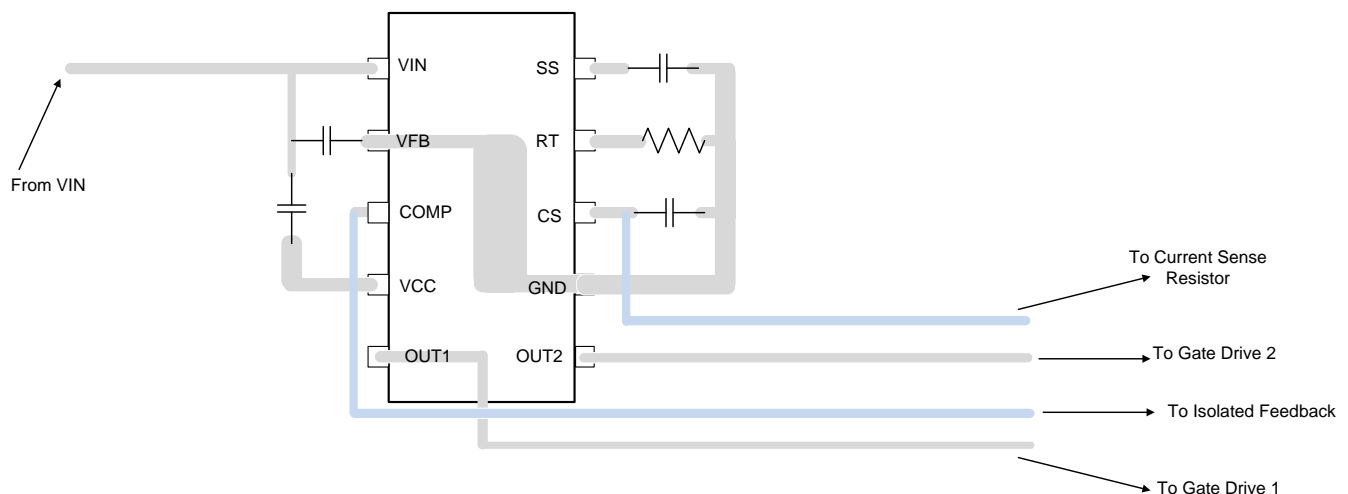


Figure 14. LM5030 Board Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

[SNOA401](#): *AN-1187 Leadless Leadframe Package (LLP)*

[SNVA548](#): *Versatility of the LM5030 PWM Push-Pull Controller*

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
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11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary


[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|---|
| LM5030MM | NRND | VSSOP | DGS | 10 | 1000 | TBD | Call TI | Call TI | -40 to 125 | S73B | |
| LM5030MM/NOPB | ACTIVE | VSSOP | DGS | 10 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | S73B |  |
| LM5030MMX/NOPB | ACTIVE | VSSOP | DGS | 10 | 3500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | S73B |  |
| LM5030SD/NOPB | ACTIVE | WSO | DPR | 10 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | 5030SD |  |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

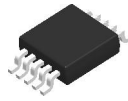
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LM5030MM | VSSOP | DGS | 10 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LM5030MM/NOPB | VSSOP | DGS | 10 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LM5030MMX/NOPB | VSSOP | DGS | 10 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LM5030SD/NOPB | WSOP | DPR | 10 | 1000 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LM5030MM | VSSOP | DGS | 10 | 1000 | 210.0 | 185.0 | 35.0 |
| LM5030MM/NOPB | VSSOP | DGS | 10 | 1000 | 210.0 | 185.0 | 35.0 |
| LM5030MMX/NOPB | VSSOP | DGS | 10 | 3500 | 367.0 | 367.0 | 35.0 |
| LM5030SD/NOPB | WSON | DPR | 10 | 1000 | 210.0 | 185.0 | 35.0 |

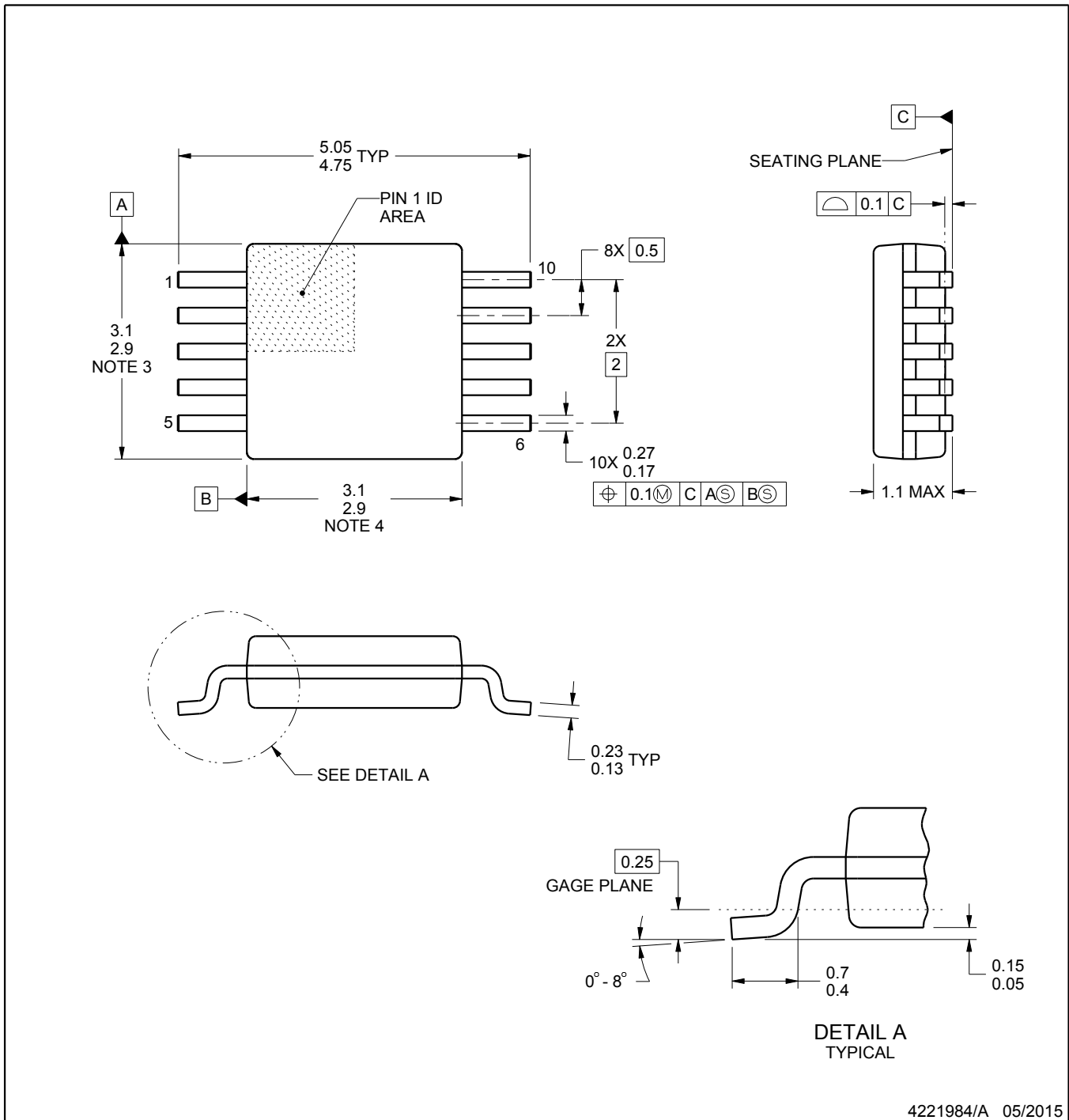
DGS0010A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4221984/A 05/2015

NOTES:

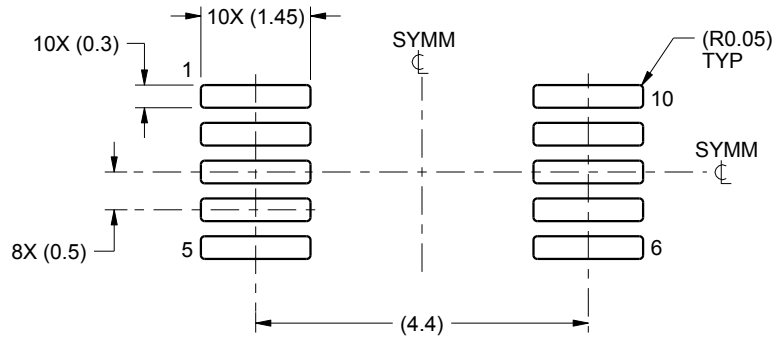
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

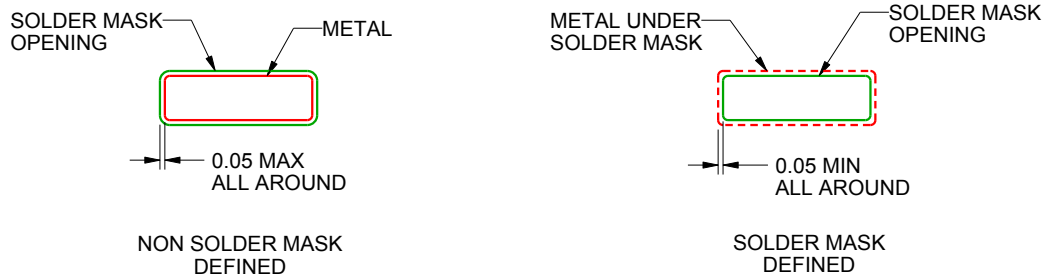
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



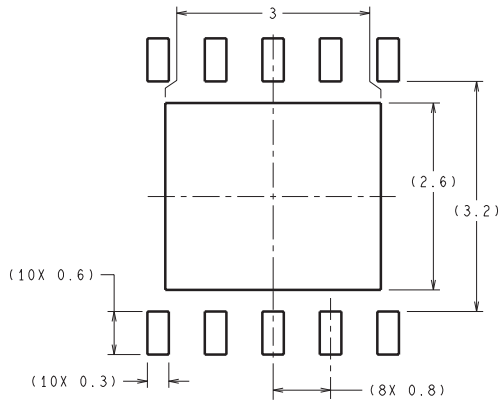
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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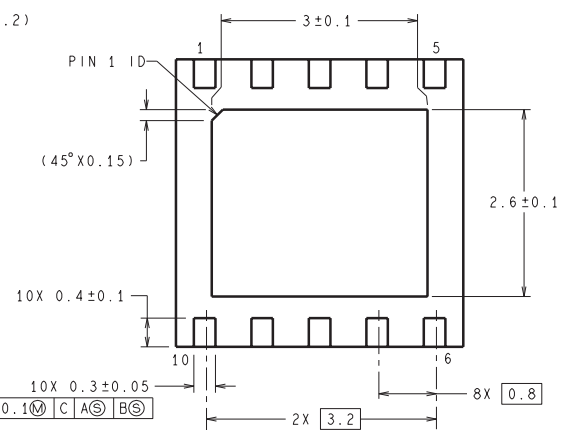
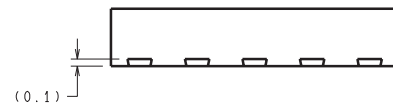
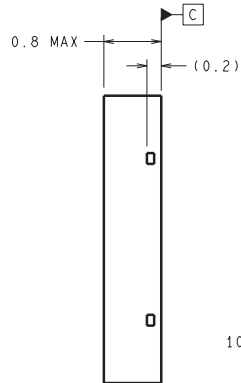
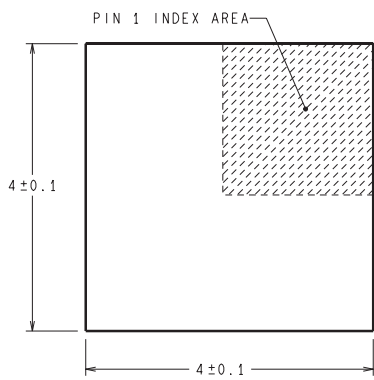
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DPR0010A



RECOMMENDED LAND PATTERN



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SDC10A (Rev A)

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