THE DATASHEET OF

LM5035SQ/NOPB

www.win-source.net 0086-755-83957316

LM5035 PWM Controller With Integrated Half-Bridge and SyncFET Drivers

1 Features

- 105-V, 2-A Half-Bridge Gate Drivers
- Synchronous Rectifier-Control Outputs With Programmable Delays
- High-Voltage (105-V) Start-up Regulator
- Voltage Mode Control With Line Feedforward and Volt-Second Limiting
- Resistor Programmed, 2-MHz Capable Oscillator
- Patent Pending Oscillator Synchronization
- Programmable Line Undervoltage Lockout
- Line Overvoltage Protection
- Internal Thermal Shutdown Protection
- Adjustable Soft-Start
- Versatile Dual Mode Overcurrent Protection With Hiccup Delay Timer
- Cycle-by-Cycle Overcurrent Protection
- Direct Optocoupler Interface
- 5-V Reference Output

2 Applications

- Industrial Power Converters
- Telecom Power Converters

3 Description

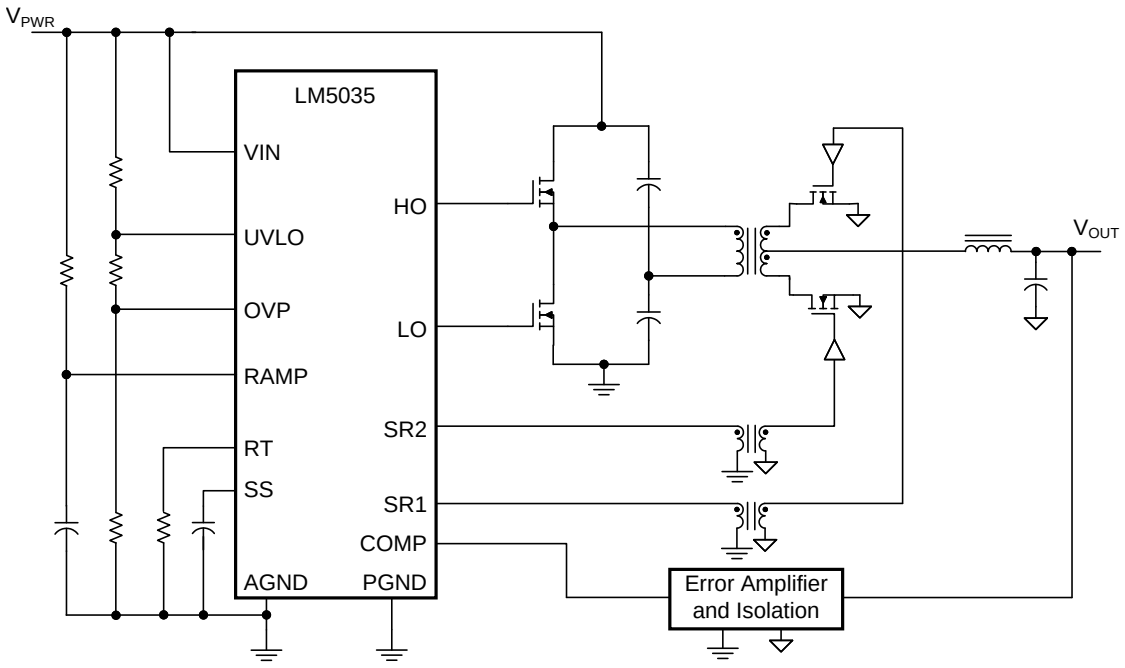
The LM5035 half-bridge controller-gate driver contains all of the features necessary to implement half-bridge topology power converters using voltage mode control with line voltage feedforward. The floating high-side gate driver is capable of operating with supply voltages up to 105 V. Both the high-side and low-side gate drivers are capable of 2-A peak. An internal high voltage start-up regulator is included, along with programmable line undervoltage lockout (UVLO) and overvoltage protection (OVP). The oscillator is programmed with a single resistor to frequencies up to 2 MHz. The oscillator can also be synchronized to an external clock. A current sense input and a programmable timer provide cycle-by-cycle current limit and adjustable hiccup mode overload protection.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5035	HTSSOP PowerPAD™ (20)	6.50 mm × 4.40 mm
	WQFN (24)	5.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplied Application Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (March 2013) to Revision H **Page**

- Added *ESD Rating* table, *Feature Description* section, *Device Functional Modes, Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Deleted Thermal Resistance section from *Electrical Characteristics* table. ... 5

Changes from Revision F (March 2013) to Revision G **Page**

- Changed layout of National Data Sheet to TI format ... 21

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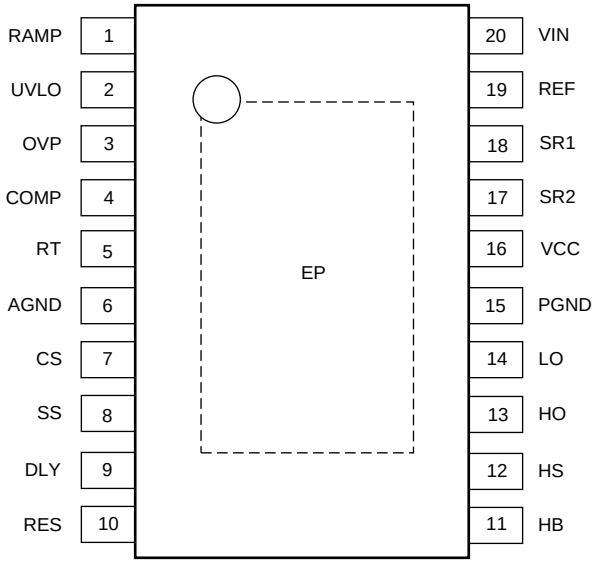
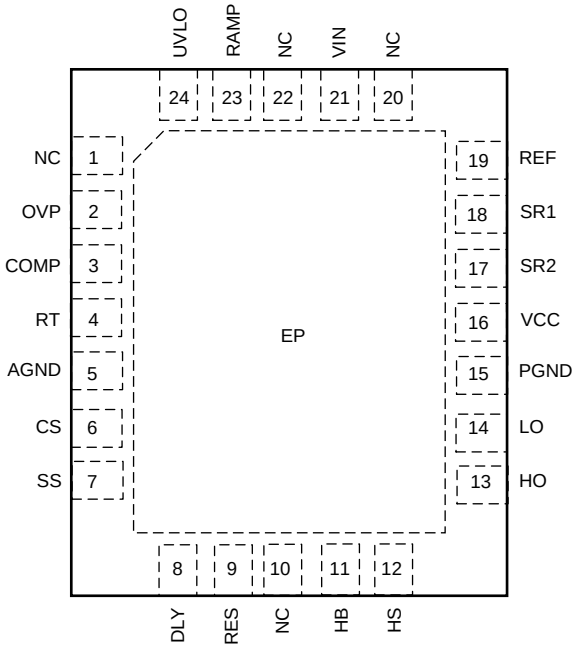
5 Pin Configuration and Functions

PWP Package
20-Pin HTSSOP With PowerPAD
Top View



NHZ Package
24-Pin WQFN
Top View



Pin Functions

PIN			TYPE	DESCRIPTION	APPLICATION INFORMATION
NAME	NO.				
	HTSSOP	WQFN			
AGND	6	5	GND	Analog ground	Connect directly to Power Ground.
COMP	4	3	I/O	Input to the pulse width modulator	An external optocoupler connected to the COMP pin sources current into an internal NPN current mirror. The PWM duty cycle is maximum with zero input current, while 1mA reduces the duty cycle to zero. The current mirror improves the frequency response by reducing the AC voltage across the optocoupler detector.
CS	7	6	I	Current sense input for current limit	If CS exceeds 0.25 V, the output pulse will be terminated, entering cycle-by-cycle current limit. An internal switch holds CS low for 50 ns after HO or LO switches high to blank leading edge transients.
DLY	9	8	I	Timing programming pin for the LO and HO to SR1 and SR2 outputs	An external resistor to ground sets the timing for the nonoverlap time of HO to SR1 and LO to SR2.
HB	11	11	I/O	Boost voltage for the HO driver	An external diode is required from VCC to HB and an external capacitor is required from HS to HB to power the HO gate driver.
HO	13	13	O	High side gate drive output	Output of the high side PWM gate driver. Capable of sinking 2-A peak current.
HS	12	12	I/O	Switch node	Connection common to the transformer and both power switches. Provides a return path for the HO gate driver.
LO	14	14	O	Low side gate drive output	Output of the low side PWM gate driver. Capable of sinking 2-A peak current.
NC		1, 10, 20, 22	—	No connection	No electrical contact.
OVP	3	2	I	Line overvoltage protection	An external voltage divider from the power source sets the shutdown levels. The threshold is 1.25 V. Hysteresis is set by an internal current source that sources 23 µA into the external resistor divider.
PGND	15	15	GND	Power ground	Connect directly to Analog Ground.
RAMP	1	23	I	Modulator ramp signal	An external RC circuit from VIN sets the ramp slope. This pin is discharged at the conclusion of every cycle by an internal FET. Discharge is initiated by either the internal clock or the Volt Second clamp comparator.
REF	19	19	O	Output of 5-V reference	Maximum output current is 20 mA. Locally decoupled with a 0.1-µF capacitor.
RT	5	4	I	Oscillator frequency control and sync clock input	Normally biased at 2 V. An external resistor connected between RT and AGND sets the internal oscillator frequency. The internal oscillator can be synchronized to an external clock with a frequency higher than the free running frequency set by the RT resistor.

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Pin Functions (continued)

PIN			TYPE	DESCRIPTION	APPLICATION INFORMATION
NAME	NO.				
	HTSSOP	WQFN			
RES	10	9	I	Restart timer	If cycle-by-cycle current limit is exceeded during any cycle, a 22-µA current is sourced to the RES pin capacitor. If the RES capacitor voltage reaches 2.5 V, the soft-start capacitor will be fully discharged and then released with a pull-up current of 1.2 µA. After the first output pulse at LO (when SS > COMP offset, typically 1 V), the SS pin charging current will revert to 55 µA.
SR1	18	18	O	Synchronous rectifier driver output	Control output of the synchronous FET gate. Capable of 0.5-A peak current.
SR2	17	17	O	Synchronous rectifier driver output	Control output of the synchronous FET gate. Capable of 0.5-A peak current.
SS	8	7	I	Soft-start input	An internal 55-µA current source charges an external capacitor to set the soft-start rate. During a current limit restart sequence, the internal current source is reduced to 1.2 µA to increase the delay before retry.
UVLO	2	24	I	Line undervoltage lockout	An external voltage divider from the power source sets the shutdown and standby comparator levels. When UVLO reaches the 0.4-V threshold the VCC and REF regulators are enabled. When UVLO reaches the 1.25-V threshold, the SS pin is released and the device enters the active mode. Hysteresis is set by an internal current sink that pulls 23 µA from the external resistor divider.
VCC	16	16	I/O	Output of the high voltage start-up regulator. The VCC voltage is regulated to 7.6 V	If an auxiliary winding raises the voltage on this pin above the regulation set-point, the start-up regulator will shutdown, thus reducing the internal power dissipation.
VIN	20	21	I	Input voltage source	Input to the Start-up Regulator. Operating input range is 13 V to 100 V with transient capability to 105 V. For power sources outside of this range, the LM5035 can be biased directly at VCC by an external regulator.
EP			GND	Exposed pad, underside of package (WQFN)	No electrical contact. Connect to system ground plane for reduced thermal resistance.
				PowerPAD (HTSSOP)	

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
VIN to GND	–0.3	105	V
HS to GND	–1	105	V
HB to GND	–0.3	118	V
HB to HS	–0.3	18	V
VCC to GND	–0.3	16	V
CS, RT, DLY to GND	–0.3	5.5	V
COMP input current		10	mA
All other inputs to GND	–0.3	7	V
Junction temperature		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office or Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$(1)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±1000	

(1) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. 2 kV for all pins except HB, HO, and HS, which are rated at 1.5 kV.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	NOM	MAX	UNIT
VIN voltage	13		105	V
External voltage applied to VCC	8		15	V
Operating Junction Temperature	–40		125	°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the *Electrical Characteristics*.

6.4 Thermal Information

THERMAL METRIC(1)		LM5035		UNIT
		PWP (HTSSOP)	NHZ (WQFN)	
		20 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.2	30	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.6	20.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.4	5.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.2	5.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.6	1.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{VIN} = 48 V, V_{VCC} = 10 V externally applied, R_{RT} = 15.0 kΩ, R_{DLY} = 27.4 kΩ, V_{UVLO} = 3 V, V_{OVP} = 0 V unless otherwise stated(1)(2).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
START-UP REGULATOR (VCC PIN)							
V_{VCC}	VCC voltage	I_{VCC} = 10 mA	T_J = 25°C		7.6		V
			T_J = –40°C to 125°C	7.3		7.9	
$I_{VCC(LIM)}$	VCC current limit	V_{VCC} = 7 V	T_J = 25°C		25		mA
			T_J = –40°C to 125°C	20			
V_{VCCUV}	VCC undervoltage threshold (VCC increasing)	VIN = VCC, ΔV_{VCC} from the regulation set point	T_J = 25°C		0.1		V
			T_J = –40°C to 125°C	0.2			
	VCC decreasing	VCC – PGND	T_J = 25°C		6.2		V
			T_J = –40°C to 125°C	5.5		6.9	
I_{VIN}	Start-up regulator current	VIN = 90 V, UVLO = 0 V	T_J = 25°C		30		µA
			T_J = –40°C to 125°C			70	
	Supply current into VCC from external source	Outputs and COMP open, V_{VCC} = 10 V, outputs switching	T_J = 25°C		4		mA
			T_J = –40°C to 125°C			6	
VOLTAGE REFERENCE REGULATOR (REF PIN)							
V_{REF}	REF voltage	I_{REF} = 0 mA	T_J = 25°C		5		V
			T_J = –40°C to 125°C	4.85		5.15	
	REF voltage regulation	I_{REF} = 0 to 10 mA	T_J = 25°C		25		mV
			T_J = –40°C to 125°C			50	
	REF current limit	REF = 4.5 V	T_J = 25°C		20		mA
			T_J = –40°C to 125°C	15			

(1) All limits are ensured. All electrical characteristics having room temperature limits are tested during production with T_A = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Typical specifications represent the most likely parametric norm at 25°C operation.

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Electrical Characteristics (continued)

V_{VIN} = 48 V, V_{VCC} = 10 V externally applied, R_{RT} = 15.0 kΩ, R_{DLY} = 27.4 kΩ, V_{UVLO} = 3 V, V_{OVP} = 0 V unless otherwise stated[1][2].

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
UVLO AND SHUTDOWN (UVLO PIN)							
V_{UVLO}	Undervoltage threshold	T_J = 25°C			1.25		V
		T_J = –40°C to 125°C		1.212		1.288	
I_{UVLO}	Hysteresis current	UVLO pin sinking	T_J = 25°C		23		µA
			T_J = –40°C to 125°C	19		27	
	Undervoltage shutdown threshold	UVLO voltage falling, T_J = 25°C			0.3		V
	Undervoltage standby enable threshold	UVLO voltage rising, T_J = 25°C			0.4		V
OVERVOLTAGE PROTECTION (OVP PIN)							
V_{OVP}	Overvoltage threshold	T_J = 25°C			1.25		V
		T_J = –40°C to 125°C		1.212		1.288	
I_{OVP}	Hysteresis current	OVP pin sourcing	T_J = 25°C		23		µA
			T_J = –40°C to 125°C	19		27	
CURRENT SENSE INPUT (CS PIN)							
V_{CS}	Current limit threshold	T_J = 25°C			0.25		V
		T_J = –40°C to 125°C		0.228		0.272	
	CS delay to output	T_J = 25°C, CS from zero to 1 V, Time for HO and LO to fall to 90% of VCC Output load = 0 pF			80		ns
	Leading edge blanking time at CS	T_J = 25°C			50		ns
	CS sink impedance (clocked)	Internal FET sink impedance	T_J = 25°C		32		Ω
			T_J = –40°C to 125°C			60	
CURRENT LIMIT RESTART (RES PIN)							
V_{RES}	RES threshold	T_J = 25°C			2.5		V
		T_J = –40°C to 125°C		2.4		2.6	
	Charge source current	V_{RES} = 1.5 V	T_J = 25°C		22		µA
			T_J = –40°C to 125°C	16		28	
	Discharge sink current	V_{RES} = 1 V	T_J = 25°C		12		µA
			T_J = –40°C to 125°C	8		16	
SOFT-START (SS PIN)							
I_{SS}	Charging current in normal operation	V_{SS} = 0	T_J = 25°C		55		µA
			T_J = –40°C to 125°C	40		70	
	Charging current during a hiccup mode restart	V_{SS} = 0	T_J = 25°C		1.2		µA
			T_J = –40°C to 125°C	0.6		1.8	
	Soft-stop current sink	V_{SS} = 2.5 V	T_J = 25°C		55		µA
			T_J = –40°C to 125°C	40		70	
OSCILLATOR (RT PIN)							
F_{SW1}	Frequency 1 (at HO, half oscillator frequency)	R_{RT} = 15 kΩ,	T_J = 25°C	185	200	215	kHz
			T_J = –40°C to 125°C	180		220	
F_{SW2}	Frequency 2 (at HO, half oscillator frequency)	R_{RT} = 5.49 kΩ	T_J = 25°C		500		kHz
			T_J = –40°C to 125°C	430		570	
	DC level	T_J = 25°C			2		V
	Input Sync threshold	T_J = 25°C			3		V
		T_J = –40°C to 125°C		2.5		3.4	

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Electrical Characteristics (continued)

V_{VIN} = 48 V, V_{VCC} = 10 V externally applied, R_{RT} = 15.0 kΩ, R_{DLY} = 27.4 kΩ, V_{UVLO} = 3 V, V_{OVP} = 0 V unless otherwise stated[1][2].

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PWM CONTROLLER (COMP PIN)							
	Delay to output	T_J = 25°C			80		ns
V_{PWM-OS}	SS to RAMP offset	T_J = 25°C			1		V
		T_J = –40°C to 125°C		0.7		1.2	
	Minimum duty cycle	SS = 0 V, T_J = 25°C				0%	
	Small signal impedance	I_{COMP} = 600 µA, COMP current to PWM voltage, T_J = 25°C			5000		Ω
MAIN OUTPUT DRIVERS (HO and LO PINS)							
	Output high voltage	I_{OUT} = 50 mA, $V_{HB} – V_{HO}$, $V_{VCC} – V_{LO}$	T_J = 25°C		0.25		V
			T_J = –40°C to 125°C	0.5			
	Output low voltage	I_{OUT} = 100 mA	T_J = 25°C		0.2		V
			T_J = –40°C to 125°C			0.5	
	Rise time	C_{LOAD} = 1 nF, T_J = 25°C			15		ns
	Fall time	C_{LOAD} = 1 nF, T_J = 25°C			13		ns
	Dead time, HO to LO, LO to HO	$V_{DLY} = V_{REF}$, I_{COMP} = 0 mA	T_J = 25°C		70		ns
			T_J = –40°C to 125°C	45		100	
	Peak source current	$V_{HO,LO}$ = 0 V, V_{VCC} = 10 V , T_J = 25°C			1.25		A
	Peak sink current	$V_{HO,LO}$ = 10 V, V_{VCC} = 10 V, T_J = 25°C			2		A
VOLTAGE FEEDFORWARD (RAMP PIN)							
	RAMP comparator threshold	COMP current = 0	T_J = 25°C		2.5		V
			T_J = –40°C to 125°C	2.4		2.6	
SYNCHRONOUS RECTIFIER DRIVERS (SR1, SR2)							
	Output high voltage	I_{OUT} = 10 mA, $V_{VCC} – V_{SR1}$, $V_{VCC} – V_{SR2}$	T_J = 25°C		0.1		V
			T_J = –40°C to 125°C	0.25			
	Output low voltage	I_{OUT} = 20 mA (sink)	T_J = 25°C		0.08		V
			T_J = –40°C to 125°C			0.2	
	Rise time	C_{LOAD} = 1 nF, T_J = 25°C			40		ns
	Fall time	C_{LOAD} = 1 nF, T_J = 25°C			20		ns
	Peak source current	V_{SR} = 0, V_{VCC} = 10 V, T_J = 25°C			0.5		A
	Peak sink current	$V_{SR} = V_{VCC}$, V_{VCC} = 10 V, T_J = 25°C			0.5		A
T1	Dead time, SR1 falling to HO rising, SR2 falling to LO rising	R_{DLY} = 10 kΩ, T_J = 25°C			40		ns
		R_{DLY} = 27.4 kΩ	T_J = 25°C		100		
			T_J = –40°C to 125°C	75		125	
		R_{DLY} = 100 kΩ, T_J = 25°C			300		
T2	Dead time, HO falling to SR1 rising, LO falling to SR2 rising	R_{DLY} = 10 kΩ, T_J = 25°C			20		ns
		R_{DLY} = 27.4 kΩ	T_J = 25°C		45		
			T_J = –40°C to 125°C	30		65	
		R_{DLY} = 100 kΩ, T_J = 25°C			140		
THERMAL SHUTDOWN							
T_{SD}	Shutdown temperature	T_J = 25°C			165		°C
	Hysteresis	T_J = 25°C			20		°C

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6.6 Typical Characteristics

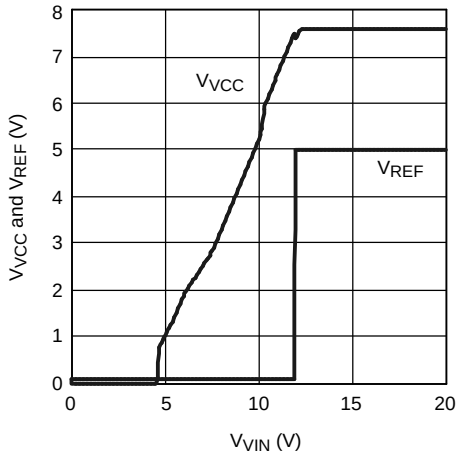

Figure 1. V_{VCC} and V_{REF} vs V_{VIN}

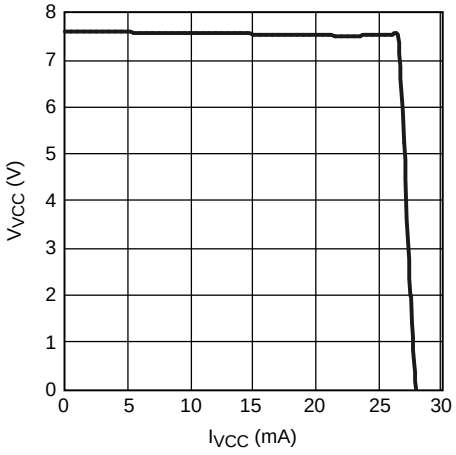

Figure 2. V_{VCC} vs I_{VCC}

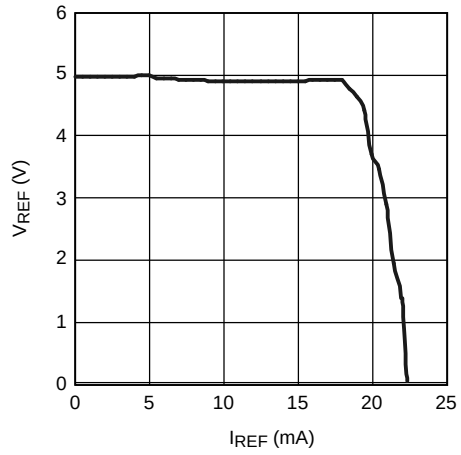

Figure 3. V_{REF} vs I_{REF}

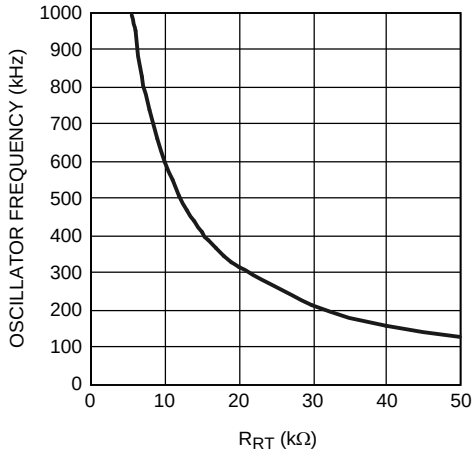

Figure 4. Frequency vs RT

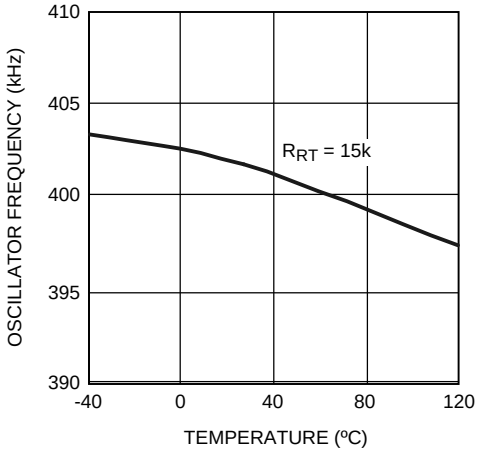

Figure 5. Oscillator Frequency vs Temperature

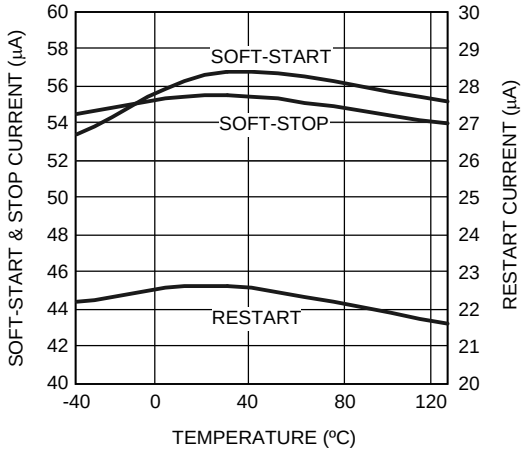

Figure 6. Soft-Start and Stop Current vs Temperature

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Typical Characteristics (continued)

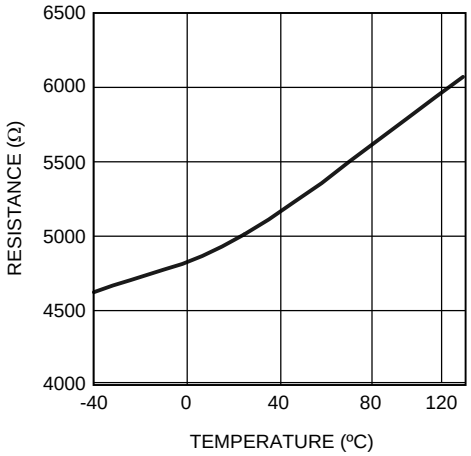

Figure 7. Effective Comp Input Impedance

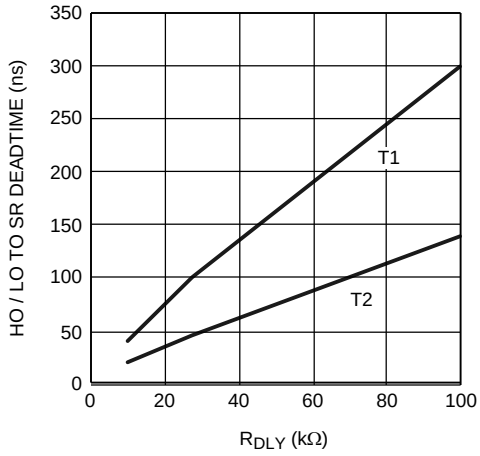

Figure 8. R_{DLY} vs Dead Time

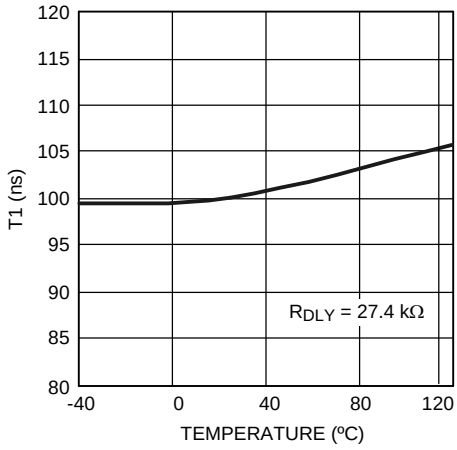

Figure 9. SR *T1* Parameter vs Temperature

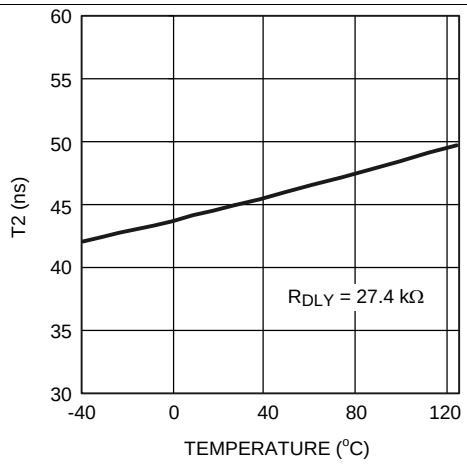

Figure 10. SR *T2* Parameter vs Temperature

7 Detailed Description

7.1 Overview

The LM5035 PWM controller contains all of the features necessary to implement half-bridge voltage-mode controlled power converters. The LM5035 provides two gate driver outputs to directly drive the primary side power MOSFETs and two signal level outputs to control secondary synchronous rectifiers through an isolation interface. Secondary side drivers, such as the LM5110, are typically used to provide the necessary gate drive current to control the sync MOSFETs. Synchronous rectification allows higher conversion efficiency and greater power density than conventional PN or Schottky rectifier techniques. The LM5035 can be configured to operate with bias voltages ranging from 8 V to 105 V. Additional features include line undervoltage lockout, cycle-by-cycle current limit, voltage feedforward compensation, hiccup mode fault protection with adjustable delays, soft-start, a 2-MHz capable oscillator with synchronization capability, precision reference, thermal shutdown and programmable volt-second clamping. These features simplify the design of voltage-mode half-bridge DC-DC power converters. See the *Functional Block Diagram*.

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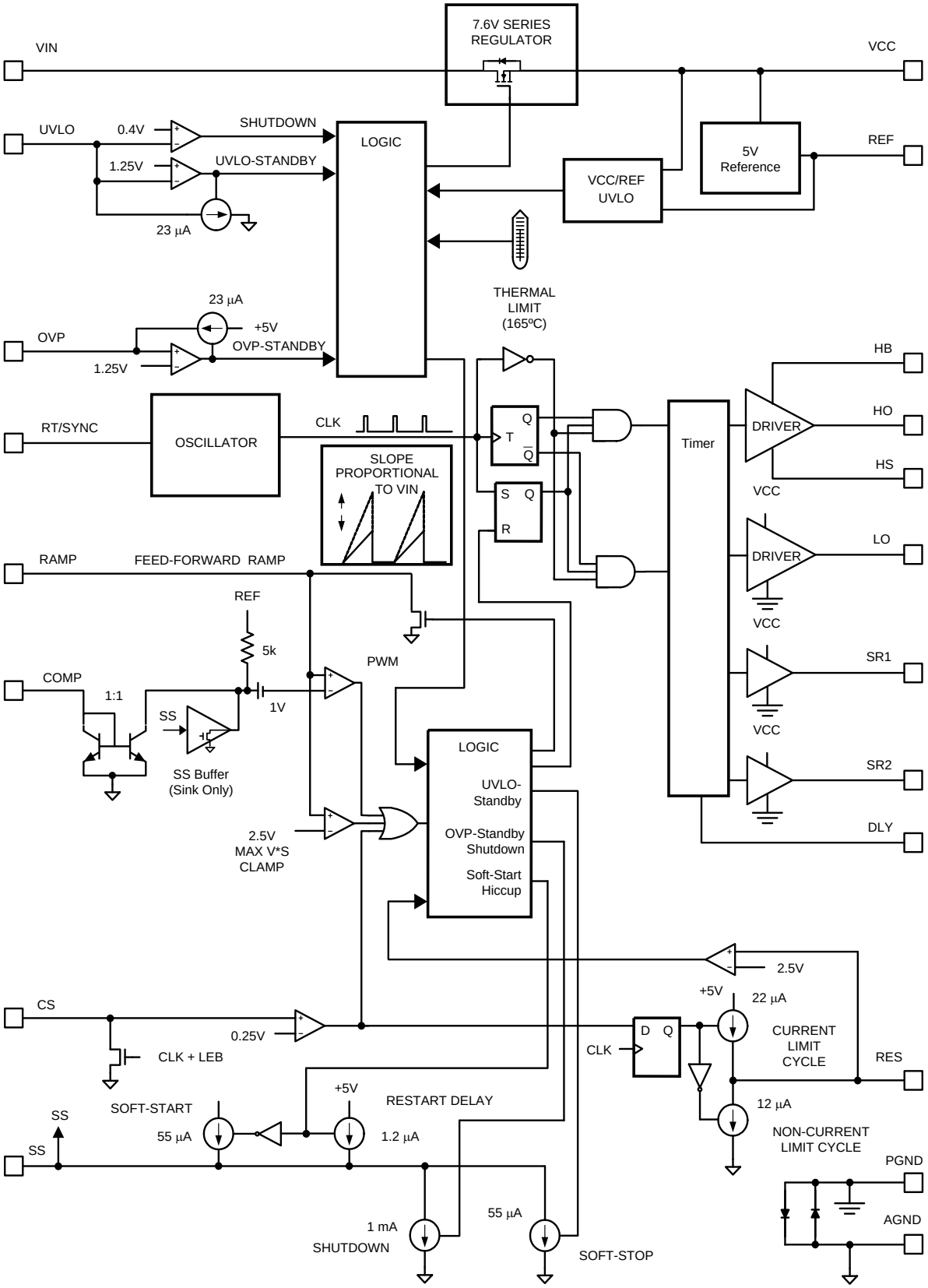
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 High-Voltage Start-Up Regulator

The LM5035 contains an internal high voltage start-up regulator that allows the input pin (VIN) to be connected directly to a nominal 48-V DC input voltage. The regulator input can withstand transients up to 105 V. The regulator output at VCC (7.6-V) is internally current limited to 25-mA typical. When the UVLO pin potential is greater than 0.4 V, the VCC regulator is enabled to charge an external capacitor connected to the VCC pin. The VCC regulator provides power to the voltage reference (REF) and the output drivers (LO, SR1, and SR2). When the voltage on the VCC pin exceeds the UVLO threshold of 7.6 V, the internal voltage reference (REF) reaches its regulation set-point of 5 V and the UVLO voltage is greater than 1.25 V, the controller outputs are enabled. The value of the VCC capacitor depends on the total system design, and its start-up characteristics. The recommended range of values for the VCC capacitor is 0.1 µF to 100 µF.

The VCC undervoltage comparator threshold is lowered to 6.2-V (typical) after VCC reaches the regulation set-point. If VCC falls below this value, the outputs are disabled, and the soft-start capacitor is discharged. If VCC increases above 7.6 V, the outputs will be enabled and a soft-start sequence will commence.

The internal power dissipation of the LM5035 can be reduced by powering VCC from an external supply. In typical applications, an auxiliary transformer winding is connected through a diode to the VCC pin. This winding must raise the VCC voltage above 8.3 V to shut off the internal start-up regulator. Powering VCC from an auxiliary winding improves efficiency while reducing the power dissipation of the controller. The undervoltage comparator circuit will still function in this mode, requiring that VCC never falls below 6.2 V during the start-up sequence.

During a fault mode, when the converter auxiliary winding is inactive, external current draw on the VCC line must be limited such that the power dissipated in the start-up regulator does not exceed the maximum power dissipation of the IC package.

An external DC bias voltage can be used instead of the internal regulator by connecting the external bias voltage to both the VCC and the VIN pins. The external bias must be greater than 8.3 V to exceed the VCC UVLO threshold and less than the VCC maximum operating voltage rating (15 V).

7.3.2 Line Undervoltage Detector

The LM5035 contains a dual level undervoltage Lockout (UVLO) circuit. When the UVLO pin voltage is below 0.4 V, the controller is in a low current shutdown mode. When the UVLO pin voltage is greater than 0.4 V but less than 1.25 V, the controller is in standby mode. In standby mode, the VCC and REF bias regulators are active while the controller outputs are disabled. When the VCC and REF outputs exceed the VCC and REF undervoltage thresholds and the UVLO pin voltage is greater than 1.25 V, the outputs are enabled and normal operation begins. An external set-point voltage divider from VIN to GND can be used to set the minimum operating voltage of the converter. The divider must be designed such that the voltage at the UVLO pin will be greater than 1.25 V when VIN enters the desired operating range. UVLO hysteresis is accomplished with an internal 23-µA current sink that is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current sink is deactivated to quickly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 1.25-V threshold, the current sink is enabled causing the voltage at the UVLO pin to quickly fall. The hysteresis of the 0.4-V shutdown comparator is internally fixed at 100 mV.

The UVLO pin can also be used to implement various remote enable and disable functions. Turning off a converter by forcing the UVLO pin to the standby condition provides a controlled soft-stop. See the *Soft-Start* section for more details.

7.3.3 Line Overvoltage, Load Overvoltage, Remote Thermal Protection

The LM5035 provides a multipurpose OVP pin that supports several fault protection functions. When the OVP pin voltage exceeds 1.25 V, the controller is held in standby mode, which immediately halts the PWM pulses at the HO and LO pins. In standby mode, the VCC and REF bias regulators are active while the controller outputs are disabled. When the OVP pin voltage falls below the 1.25-V OVP threshold, the outputs are enabled and normal soft-start sequence begins. Hysteresis is accomplished with an internal 23-µA current source that is switched on or off into the impedance of the OVP pin set-point divider. When the OVP threshold is exceeded, the current source is enabled to quickly raise the voltage at the OVP pin. When the OVP pin voltage falls below the 1.25-V threshold, the current source is disabled causing the voltage at the OVP pin to quickly fall.

See the *Application Information* section for several examples of how to use the OVP pin.

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Feature Description (continued)

7.3.4 Reference

The REF pin is the output of a 5-V linear regulator that can be used to bias an optocoupler transistor and external housekeeping circuits. The regulator output is internally current limited to 20-mA (typical).

7.3.5 Cycle-by-Cycle Current Limit

The CS pin is driven by a signal representative of the transformer primary current. If the voltage sensed at CS pin exceeds 0.25 V, the current sense comparator terminates the HO or LO output driver pulse. If the high-current condition persists, the controller operates in a cycle-by-cycle current-limit mode with duty cycle determined by the current sense comparator instead of the PWM comparator. Cycle-by-cycle current limiting may trigger the hiccup mode restart cycle, depending on the configuration of the RES pin (see the *Overload Protection Timer* section).

TI recommends placing a small R-C filter connected to the CS pin and located near the controller to suppress noise. An internal 32-Ω MOSFET connected to the CS input discharges the external current sense filter capacitor at the conclusion of every cycle. The discharge MOSFET remains on for an additional 50 ns after the HO or LO driver switches high to blank leading edge transients in the current sensing circuit. Discharging the CS pin filter each cycle and blanking leading edge spikes reduces the filtering requirements and improves the current sense response time.

The current sense comparator is very fast and responds to short duration noise pulses. Layout considerations are critical for the current sense filter and sense resistor. The capacitor associated with the CS filter must be placed very close to the device and must be connected directly to the CS and AGND pins. If a current sense transformer is used, both leads of the transformer secondary must be routed to the filter network, which must be located close to the IC. If a sense resistor located in the source of the main MOSFET switch is used for current sensing, a low-inductance type of resistor is required. When designing with a current sense resistor, all of the noise sensitive low-power ground connections must be connected together near the AGND pin, and a single connection must be made to the power ground (sense resistor ground point).

7.3.6 Overload Protection Timer

The LM5035 provides a current-limit restart timer (see Figure 11) to disable the outputs and force a delayed restart (hiccup mode) if a current limit condition is repeatedly sensed. The number of cycle-by-cycle current-limit events required to trigger the restart is programmable by the external capacitor at the RES pin. During each PWM cycle, the LM5035 either sources or sinks current from the RES pin capacitor. If no current limit is detected during a cycle, an 12-µA discharge current sink is enabled to pull the RES pin to ground. If a current limit is detected, the 12-µA sink current is disabled and a 22-µA current source causes the voltage at the RES pin to gradually increase. The LM5035 protects the converter with cycle-by-cycle current limiting while the voltage at RES pin increases. If the RES voltage reaches the 2.5-V threshold, the following restart sequence occurs (also see Figure 11):

1. The RES capacitor and SS capacitors are fully discharged.
2. The soft-start current source is reduced from 55 µA to 1 µA.
3. The SS capacitor voltage slowly increases. When the SS voltage reaches ≅1 V, the PWM comparator will produce the first narrow output pulse. After the first pulse occurs, the SS source current reverts to the normal 55-µA level. The SS voltage increases at its normal rate, gradually increasing the duty cycle of the output drivers.
4. If the overload condition persists after restart, cycle-by-cycle current limiting will begin to increase the voltage on the RES capacitor again, repeating the hiccup mode sequence.
5. If the overload condition no longer exists after restart, the RES pin will be held at ground by the 12-µA current sink and normal operation resumes.

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Feature Description (continued)

The overload-timer function is very versatile and can be configured for the following modes of protection:

Cycle-by-cycle only The hiccup mode can be completely disabled by connecting a zero to 50-kΩ resistor from the RES pin to AGND. In this configuration, the cycle-by-cycle protection will limit the output current indefinitely and no hiccup sequences will occur.

Hiccup only The timer can be configured for immediate activation of a hiccup sequence upon detection of an overload by leaving the RES pin open circuit.

Delayed Hiccup Connecting a capacitor to the RES pin provides a programmed interval of cycle-by-cycle limiting before initiating a hiccup mode restart, as previously described. The dual advantages of this configuration are that a short term overload will not cause a hiccup mode restart but during extended overload conditions, the average dissipation of the power converter will be very low.

Externally Controlled Hiccup The RES pin can also be used as an input. By externally driving the pin to a level greater than the 2.5-V hiccup threshold, the controller will be forced into the delayed restart sequence. For example, the external trigger for a delayed restart sequence could come from an overtemperature protection circuit or an output overvoltage sensor.

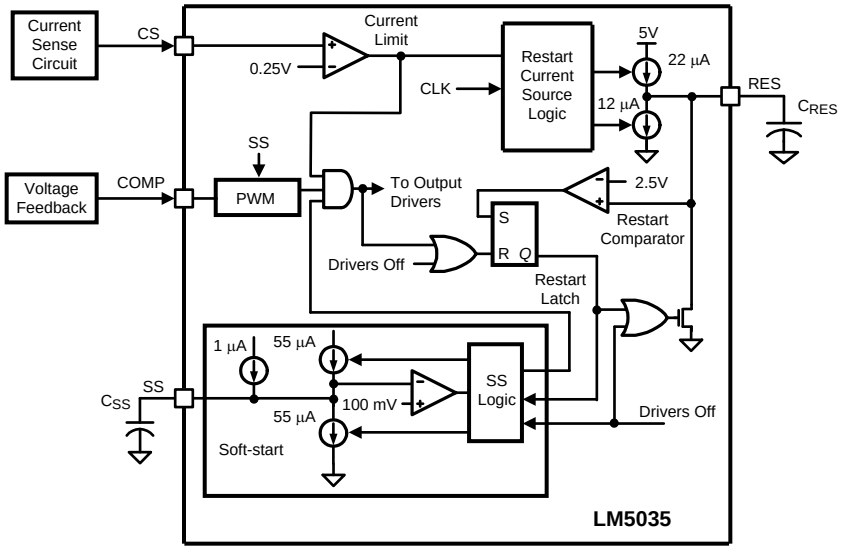

Figure 11. Current-Limit Restart Circuit

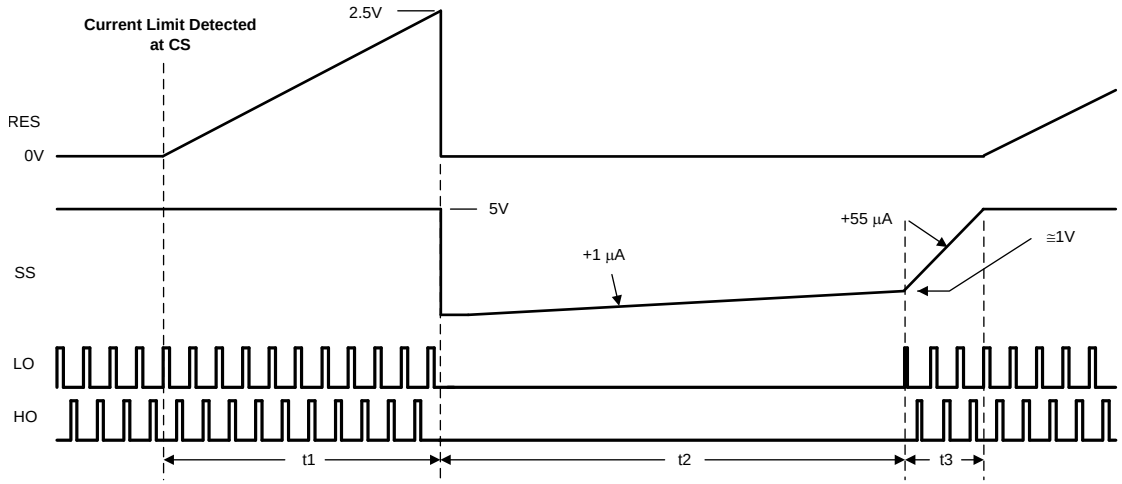

Figure 12. Current-Limit Restart Timing

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Feature Description (continued)

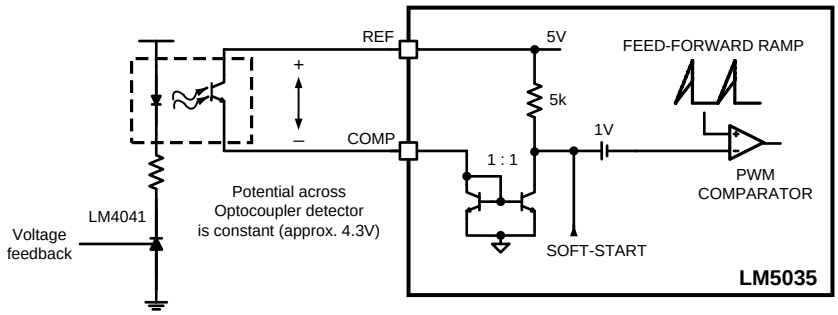

Figure 13. Optocoupler-to-COMP Interface

7.3.7 Soft-Start

The soft-start circuit allows the regulator to gradually reach a steady state operating point, thereby reducing start-up stresses and current surges. When bias is supplied to the LM5035, the SS pin capacitor is discharged by an internal MOSFET. When the UVLO, VCC, and REF pins reach their operating thresholds, the SS capacitor is released and charged with a 55-µA current source. The PWM comparator control voltage is clamped to the SS pin voltage by an internal amplifier. When the PWM comparator input reaches 1 V, output pulses commence with slowly increasing duty cycle. The voltage at the SS pin eventually increases to 5 V, while the voltage at the PWM comparator increases to the value required for regulation, as determined by the voltage feedback loop.

One method to shutdown the regulator is to ground the SS pin, which forces the internal PWM control signal to ground, thus quickly reducing the output duty cycle to zero. Releasing the SS pin begins a soft-start cycle, and normal operation resumes. A second shutdown method is discussed in the *UVLO* section.

7.3.8 Soft-Stop

If the UVLO pin voltage falls below the 1.25-V standby threshold but above the 0.4-V shutdown threshold, the 55-µA SS pin source current is disabled and a 55-µA sink current discharges the soft-start capacitor. As SS voltage falls and clamps the PWM comparator input, the PWM duty cycle will gradually fall to zero. The soft-stop feature produces a gradual reduction of the power converter output voltage. This soft-stop method of turning off the converter reduces energy in the output capacitor before control of the main and synchronous rectification MOSFETs is disabled. The PWM pulses may cease before the SS voltage reduces the duty cycle if the VCC or REF voltage drops below the respective undervoltage thresholds during the soft-stop process.

7.3.9 PWM Comparator

The pulse width modulation (PWM) comparator compares the voltage ramp signal at the RAMP pin to the loop-error signal. This comparator is optimized for speed in order to achieve minimum controllable duty cycles. The loop-error signal is received from the external feedback, and the isolation circuit is in the form of a control current into the COMP pin. The COMP pin current is internally mirrored by a matched pair of NPN transistors that sink current through a 5-kΩ resistor connected to the 5-V reference. The resulting control voltage passes through a 1-V level shift before being applied to the PWM comparator.

An optocoupler detector can be connected between the REF pin and the COMP pin (see Figure 13). Because the COMP pin is controlled by a current input, the potential difference across the optocoupler detector is nearly constant. The bandwidth-limiting phase delay, which is normally introduced by the significant capacitance of the optocoupler, is thereby greatly reduced. Higher loop bandwidths can be realized because the bandwidth-limiting pole associated with the optocoupler is now at a much higher frequency. The PWM comparator polarity is configured such that, with no current into the COMP pin, the controller produces the maximum duty cycle at the main gate driver outputs, HO and LO.

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Feature Description (continued)

7.3.10 Feedforward Ramp and Volt-Second Clamp

An external resistor (R_{FF}) and capacitor (C_{FF}) connected to VIN, AGND, and the RAMP pin are required to create the PWM ramp signal. The slope of the signal at RAMP will vary in proportion to the input line voltage. This varying slope provides line feedforward information necessary to improve line transient response with voltage mode control. The RAMP signal is compared to the error signal by the pulse width modulator comparator to control the duty cycle of the HO and LO outputs. With a constant error signal, the on-time (T_{ON}) varies inversely with the input voltage (VIN) to stabilize the volt-second product of the transformer primary signal. The power path gain of conventional voltage-mode pulse-width modulators (oscillator generated ramp) varies directly with input voltage. The use of a line generated ramp (input voltage feedforward) nearly eliminates this gain variation. As a result, the feedback loop is only required to make very small corrections for large changes in input voltage.

In addition to the PWM comparator, a volt-second clamp comparator also monitors the RAMP pin. If the ramp amplitude exceeds the 2.5-V threshold of the volt-second clamp comparator, the on-time is terminated. The C_{FF} ramp capacitor is discharged by an internal 32-Ω discharge MOSFET controlled by the volt-second clamp comparator. If the RAMP signal does not exceed 2.5 V before the end of the clock period, the internal clock will enable the discharge MOSFET to reset capacitor C_{FF}.

By proper selection of R_{FF} and C_{FF} values, the maximum on-time of HO and LO can be set to the desired duration. The on-time set by the volt-second clamp varies inversely to the line voltage because the RAMP capacitor is charged by a resistor (R_{FF}) connected to VIN, while the threshold of the clamp is a fixed voltage (2.5 V). An example will illustrate the use of the volt-second clamp comparator to achieve a 50% duty cycle limit at 200 kHz with a 48-V line input. A 50% duty cycle at a 200 kHz requires a 2.5-µs on-time. To achieve this maximum on-time clamp level, use Equation 1:

$$R_{FF} \times C_{FF} = \frac{T_{ON} + 10\%}{\ln\left[\left(1 - \frac{2.5V}{VIN}\right)^{-1}\right]} = \frac{2.5\ \mu s + 0.25\ \mu s}{\ln\left[\left(1 - \frac{2.5V}{48V}\right)^{-1}\right]} = 51.4\ \mu s \quad (1)$$

The recommended capacitor value range for C_{FF} is 100 pF to 1000 pF. A standard value of 470 pF can be paired with 110 kΩ to approximate the desired 51.4-µs time constant. If load-transient response is slowed by the 10% margin, the R_{FF} value can be increased. The system signal-to-noise will be slightly decreased by increasing $R_{FF} \times C_{FF}$.

7.3.11 Oscillator, Sync Capability

The LM5035 oscillator frequency is set by a single external resistor connected between the RT and AGND pins. To set a desired oscillator frequency, the necessary RT resistor is calculated from Equation 2:

$$RT = \left(\frac{1}{F_{OSC}} - 110\ ns\right) \times 6.25 \times 10^{9} \quad (2)$$

For example, if the desired oscillator frequency is 400 kHz (HO and LO each switching at 200 kHz) a 15-kΩ resistor would be the nearest standard one percent value.

Each output (HO, LO, SR1 and SR2) switches at half the oscillator frequency. The voltage at the RT pin is internally regulated to a nominal 2 V. The RT resistor must be located as close as possible to the IC and connected directly to the pins (RT and AGND). The tolerance of the external resistor and the frequency tolerance indicated in the *Electrical Characteristics* must be taken into account when determining the worst-case frequency range.

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Feature Description (continued)

The LM5035 can be synchronized to an external clock by applying a narrow pulse to the RT pin. The external clock must be at least 10% higher than the free-running oscillator frequency set by the RT resistor. If the external clock frequency is less than the RT resistor programmed frequency, the LM5035 will ignore the synchronizing pulses. The synchronization pulse width at the RT pin must be a minimum of 15-ns wide. The clock signal must be coupled into the RT pin through a 100-pF capacitor or a value small enough to ensure the pulse width at RT is less than 60% of the clock period under all conditions. When the synchronizing pulse transitions low-to-high (rising edge), the voltage at the RT pin must be driven to exceed 3.2 V from its nominal 2-V DC level. During the low time of the clock signal, the voltage at the RT pin will be clamped at 2-V DC by an internal regulator. The output impedance of the RT regulator is approximately 100 Ω. The RT resistor is always required, whether the oscillator is free running or externally synchronized.

7.3.12 Gate-Driver Outputs (HO and LO)

The LM5035 provides two alternating gate-driver outputs, the floating high-side gate driver HO and the ground referenced low-side driver LO. Each driver can source 1.25 A and sink 2-A peak. The HO and LO outputs operate in an alternating manner at one-half of the internal oscillator frequency. The LO driver is powered directly by the VCC regulator. The HO gate driver is powered from a bootstrap capacitor connected between HB and HS. An external diode connected between VCC (anode pin) and HB (cathode pin) provides the high-side gate driver power by charging the bootstrap capacitor from VCC when the switch node (HS pin) is low. When the high-side MOSFET is turned on, HB rises to a peak voltage equal to $V_{VCC} + V_{HS}$ where V_{HS} is the switch-node voltage.

The HB and VCC capacitors must be placed close to the pins of the LM5035 to minimize voltage transients due to parasitic inductances because the peak current sourced to the MOSFET gates can exceed 1.25 A. The recommended value of the HB capacitor is 0.01 µF or greater. A low-ESR or low-ESL capacitor, such as a surface-mount ceramic, must be used to prevent voltage droop during the HO transitions.

The maximum duty cycle for each output is limited to slightly less than 50%, due to the internally fixed dead time and any programmed sync rectifier delay. The typical dead time in this condition is 70 ns. The programmed sync rectifier delay is determined by the DLY pin resistor. If the COMP pin is open circuit, the outputs will operate at maximum duty cycle. The maximum duty cycle for each output can be calculated with Equation 3:

$$\text{Maximum Duty Cycle} = \frac{\frac{1}{2}T_S - T_D - T1}{T_S} \quad (3)$$

where

- T_S is the period of one complete cycle for either the HO or LO outputs
- T_D is the internally fixed dead time
- and T1 is the programmed sync rectifier delay

For example, if the oscillator frequency is 200 kHz, each output will cycle at 100 kHz (T_S = 10 µs). Using the nominal dead time of 70 ns and no programmed delay, the maximum duty cycle at this frequency is calculated to be 49.3%. Using a programmed sync rectifier delay of 100 ns, the maximum duty cycle is reduced to 48.3%.

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Feature Description (continued)

7.3.13 Synchronous Rectifier Control Outputs (SR1 and SR2)

Synchronous rectification (SR) of the transformer secondary provides higher efficiency, especially for low-output voltage converters. The reduction of rectifier forward-voltage drop (0.5 V – 1.5 V) to 10 mV – 200 mV V_{DS} voltage for a MOSFET, significantly reduces rectification losses. In a typical application, the transformer secondary winding is center tapped, with the output-power inductor in series with the center tap. The SR MOSFETs provide the ground path for the energized secondary winding and the inductor current. Figure 14 shows that the SR2 MOSFET is conducting while HO enables power transfer from the primary. The SR1 MOSFET must be disabled during this period, because the secondary winding connected to the SR1 MOSFET drain is twice the voltage of the center tap. At the conclusion of the HO pulse, the inductor current continues to flow through the SR1 MOSFET body diode. Because the body diode causes more loss than the SR MOSFET, efficiency can be improved by minimizing the T2 period, while maintaining sufficient timing margin over all conditions (component tolerances, and so on) to prevent shoot-through current. When LO enables power transfer from the primary, the SR1 MOSFET is enabled, and the SR2 MOSFET is off.

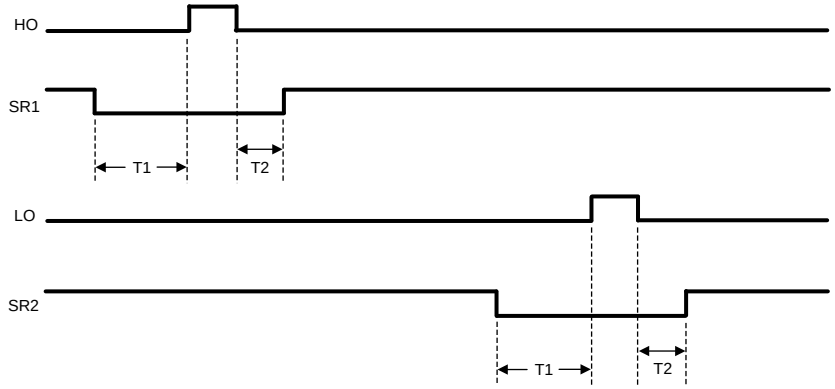

Figure 14. HO, LO, SR1 and SR2 Timing Diagram

During the time that neither HO nor LO is active, the inductor current is shared between both the SR1 and SR2 MOSFETs, which effectively shorts the transformer secondary and cancels the inductance in the windings. The SR2 MOSFET is disabled before LO delivers power to the secondary to prevent power being shunted to ground. The SR2 MOSFET body diode continues to carry about half the inductor current until the primary power raises the SR2 MOSFET drain voltage and reverse biases the body diode. Ideally, dead-time T1 would be set to the minimum time that allows the SR MOSFET to turn off before the SR MOSFET body diode starts conducting.

The SR1 and SR2 outputs are powered directly by the VCC regulator. Each output is capable of sourcing and sinking 0.5-A peak. Typically, the SR1 and SR2 signals control SR MOSFET gate drivers through a pulse transformer. The actual gate sourcing and sinking currents are provided by the secondary-side bias supply and gate drivers.

The timing of SR1 and SR2 with respect to HO and LO is shown in Figure 14. SR1 is configured out-of-phase with HO, and SR2 is configured out-of-phase with LO. The dead time between transitions is programmable by a resistor connected from the DLY pin to the AGND pin. Typically, R_{DLY} is set in the range of 10 kΩ to 100 kΩ. The dead-time periods can be calculated using Equation 4 and Equation 5:

$$T1 = [R_{DLY} \times 2.8\ ps] + 20\ ns \quad (4)$$

$$T2 = [R_{DLY} \times 1.35\ ps] + 6\ ns \quad (5)$$

To set the minimum dead time (propagation delays only), the DLY pin must be left open or connected to the REF pin. Any resistor value above 300 kΩ connected between the DLY pin and AGND will also provide the minimum period (approximately 5 ns).

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Feature Description (continued)

7.3.14 Thermal Protection

Internal thermal-shutdown circuitry is provided to protect the integrated circuit in the event that the maximum-rated junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low-power standby state with the output drivers (HO, LO, SR1, and SR2) and the bias regulators (VCC and REF) disabled. This helps prevent catastrophic failures from accidental device overheating. During thermal shutdown, the soft-start capacitor is fully discharged, and the controller follows a normal start-up sequence after the junction temperature falls to the operating level (145°C).

7.4 Device Functional Modes

The LM5035 can be used as a half-bridge PWM controller or as a push-pull PWM controller.

To implement the LM5035 in a push-pull application, the HB pin is connected to VCC and the HS pin is connected to PGND. The LM5035 will deliver 180º out-of-phase ground-referenced PWM signals to the gates of the power MOSFETS.

The high-side driver has an HS-to-GND maximum voltage rating of 105 V, but in higher-voltage applications the high-side MOSFET can be driven with a gate-drive transformer.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

8.1 Application Information

The following information is intended to provide guidelines for the power-supply designer using the LM5035.

8.2 Typical Application

Figure 15 shows an example of a 100-W half-bridge power converter controlled by the LM5035. The operating input-voltage range (V_{PWR}) is 36 V to 75 V, and the output voltage is 3.3 V. The output-current capability is 30 A. Current sense transformer T2 provides information to the CS pin for current-limit protection. The error amplifier and reference, U3 and U5 respectively, provide voltage feedback through optocoupler U4. Synchronous rectifiers (Q4, Q5, Q6, and Q7) minimize rectification losses in the secondary. An auxiliary winding on transformer T1 provides power to the LM5035 VCC pin when the output is in regulation. The input voltage UVLO thresholds are ≅ 34 V for increasing V_{PWR}, and ≅ 32 V for decreasing V_{PWR}. The circuit can be shut down by driving the ON/OFF input (J2) below 1.25 V with an open-collector or open-drain circuit. An external synchronizing frequency can be applied through a 100-pF capacitor to the RT input (U1 pin 5). The regulator output is current limited at ≅ 34 A.

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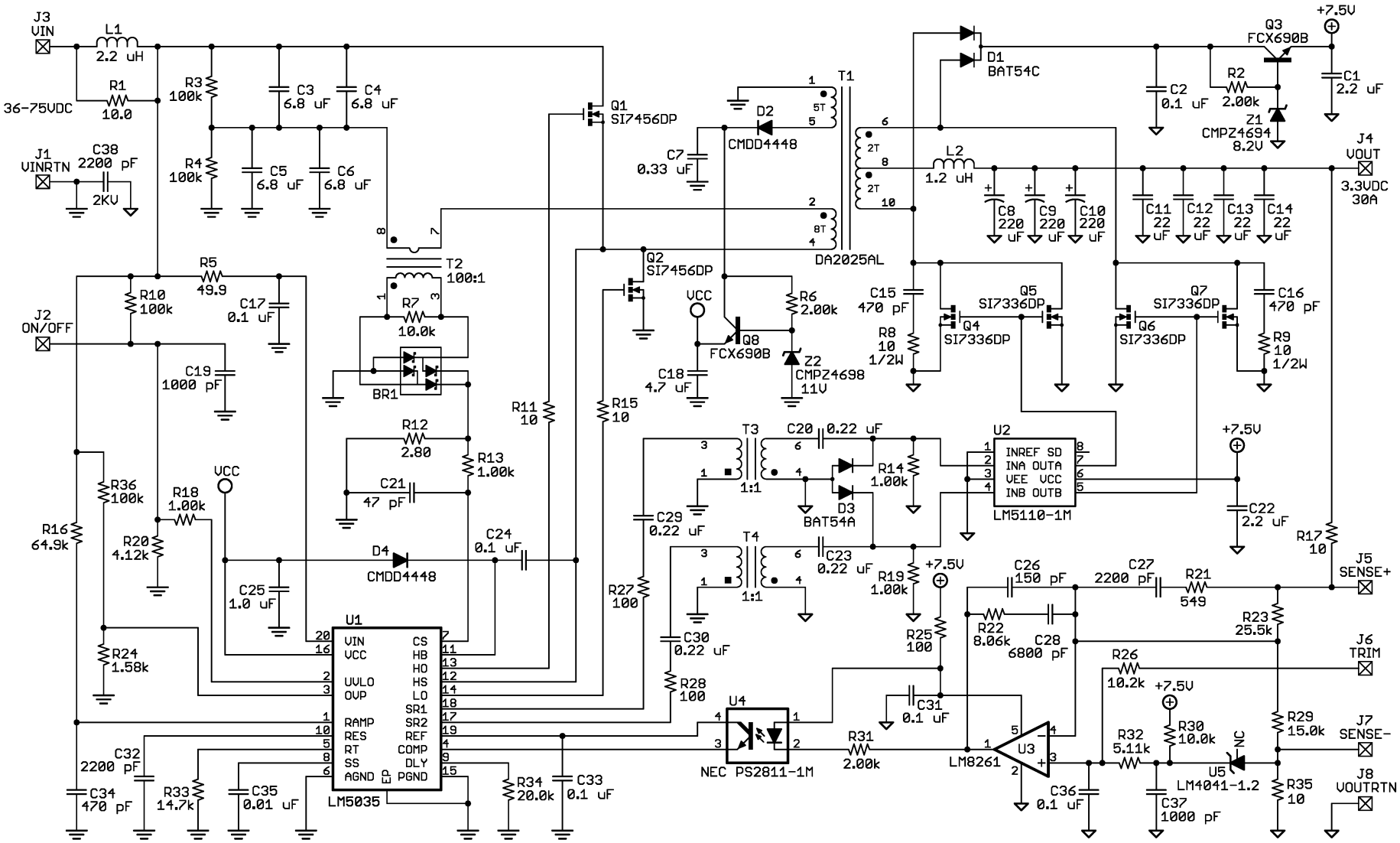

Figure 15. Application Circuit

8.2.1 Design Requirements

Table 1 lists example design parameters for the application circuit layout in Figure 15.

Table 1. Design Parameters

PARAMETER	MIN	NOM	MAX	UNIT
Input voltage (VIN)	36		72	V
Output voltage (V_{OUT})		3.3		V
Output current (I_{OUT})	0		30	A
Switching frequency		400		kHz
Efficiency (full load)		89%		
Efficiency (half load)		92%		
Load regulation		0.2%		
Line regulation		0.1%		
undervoltage lock-out (ON)		33.9		V
undervoltage lock-out (OFF)		31.9		V
Line overvoltage protection (ON)		79.4		V
Line overvoltage protection (OFF)		78.3		V

8.2.2 Detailed Design Procedure

8.2.2.1 VIN

The voltage applied to the VIN pin, which may be the same as the system voltage applied to the power transformer primary (V_{PWR}), can vary in the range from 13 V to 105 V. The current into VIN depends primarily on the gate charge provided to the output drivers, the switching frequency, and any external loads on the VCC and REF pins. It is recommended the filter shown in Figure 16 be used to suppress transients which may occur at the input supply. This is particularly important when VIN is operated close to the maximum operating rating of the LM5035.

When power is applied to VIN and the UVLO pin voltage is greater than 0.4 V, the VCC regulator is enabled and supplies current into an external capacitor connected to the VCC pin. When the voltage on the VCC pin reaches the regulation point of 7.6 V, the voltage reference (REF) is enabled. The reference regulation set point is 5 V. The HO, LO, SR1, and SR2 outputs are enabled when the two bias regulators reach their set point and the UVLO pin potential is greater than 1.25 V. In typical applications, an auxiliary transformer winding is connected through a diode to the VCC pin. This winding must raise the VCC voltage above 8.3 V to shut off the internal start-up regulator.

After the outputs are enabled and the external VCC supply voltage has begun supplying power to the IC, the current into VIN drops below 1 mA. VIN must remain at a voltage equal to or above the VCC voltage to avoid reverse current through protection diodes.

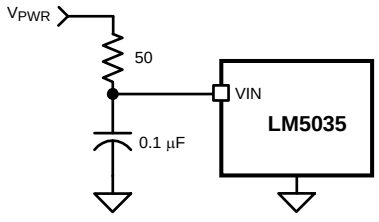

Figure 16. Input-Transient Protection

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8.2.2.2 For Applications >100 V

For applications where the system input voltage exceeds 100 V or the IC power dissipation is of concern, the LM5035 can be powered from an external start-up regulator as shown in Figure 17. In this configuration, the VIN and the VCC pins must be connected together, which allows the LM5035 to be operated below 13 V. The voltage at the VCC pin must be greater than 8.3 V, yet not exceed 15 V. An auxiliary winding can be used to reduce the power dissipation in the external regulator once the power converter is active. The NPN base-emitter reverse breakdown voltage, which can be as low as 5 V for some transistors, must be considered when selecting the transistor.

8.2.2.3 Current Sense

The CS pin needs to receive an input signal representative of the primary current of the transformer, either from a current sense transformer or from a resistor in series with the source of the LO switch, as shown in Figure 18 and Figure 19. In both cases, the sensed current creates a ramping voltage across R1, and the R_F / C_F filter suppresses noise and transients. R1, R_F and C_F must be located as close to the LM5035 as possible, and the ground connection from the current sense transformer, or R1, must be a dedicated track to the AGND pin. The current sense components must provide greater than 0.25 V at the CS pin when an overcurrent condition exists.

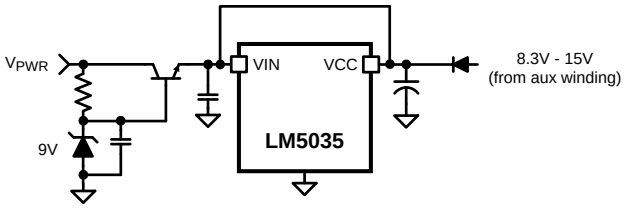

Figure 17. Start-Up Regulator for V_{PWR} >100 V

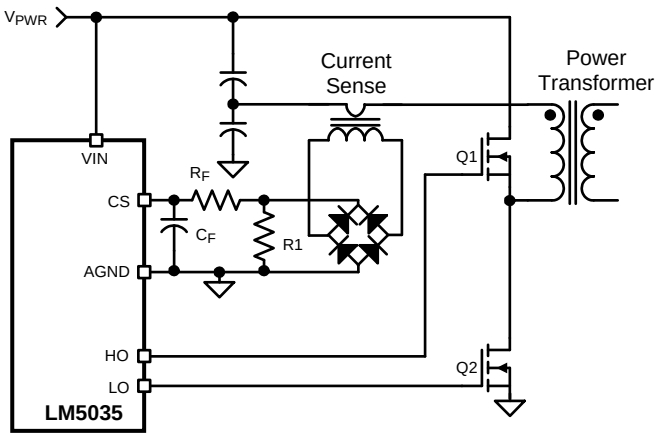

Figure 18. Current Sense Using Current Sense Transformer

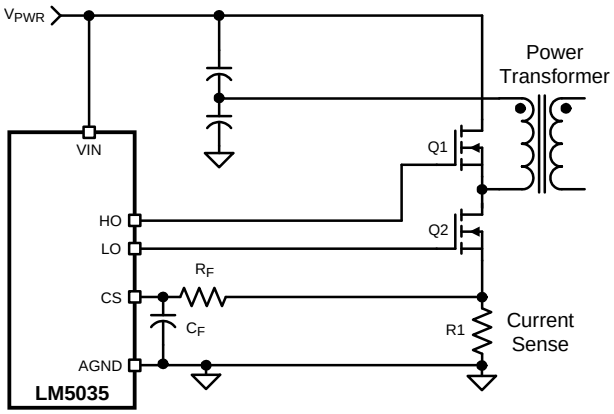

Figure 19. Current Sense Using Current Sense Resistor (R1)

If the current sense resistor method is used, the overcurrent condition will only be sensed while LO is driving the low-side MOSFET. Overcurrent while HO is driving the high-side MOSFET will not be detected. In this configuration, it will take 4 times as long for continuous cycle-by-cycle current limiting to initiate a restart event since each overcurrent event during LO enables the 22-µA RES pin current source for one oscillator period, and then the lack of an overcurrent event during HO enables the 12-µA RES pin current sink for one oscillator period. The time average of this toggling is equivalent to a continuous 5-µA current source into the RES capacitor, increasing the delay by a factor of four. The value of the RES capacitor can be reduced to decrease the time before restart cycle is initiated.

When using the resistor current sense method, an imbalance in the input capacitor voltages may develop when operating in cycle-by-cycle current limiting mode. If the imbalance persists for an extended period, excessive currents in the non-sensed MOSFET, and possible transformer saturation may result. This condition is inherent to the half-bridge topology operated with cycle-by-cycle current limiting and is compounded by only sensing in one leg of the half-bridge circuit. The imbalance is greatest at large duty cycles (low input voltages). If using this method, it is recommended that the capacitor on the RES pin be no larger than 220 pF. Check the final circuit and reduce the RES capacitor further, or omit the capacitor completely to ensure the voltages across the bridge capacitors remain balanced. The current limit value may decrease slightly as the RES capacitor is reduced.

8.2.2.4 HO, HB, HS, and LO

Attention must be given to the PC board layout for the low-side driver and the floating high-side driver pins HO, HB and HS. A low ESR or ESL capacitor (such as a ceramic surface mount capacitor) must be connected close to the LM5035, between HB and HS to provide high peak currents during turnon of the high-side MOSFET. The capacitor must be large enough to supply the MOSFET gate charge (Q_g) without discharging to the point where the drop in gate voltage affects the MOSFET $R_{DS(ON)}$. Use Equation 6 to calculate the value for C_{BOOST}. A value that is ten to 20 times Q_g is recommended.

$$C_{BOOST} = 20 \times \frac{Q_g}{VCC} \tag{6}$$

The diode (D_{BOOST}) that charges C_{BOOST} from VCC when the low-side MOSFET is conducting must be capable of withstanding the full converter input voltage range. When the high-side MOSFET is conducting, the reverse voltage at the diode is approximately the same as the MOSFET drain voltage because the high-side driver is boosted up to the converter input voltage by the HS pin, and the high side MOSFET gate is driven to the HS voltage plus VCC. Since the anode of D_{BOOST} is connected to VCC, the reverse potential across the diode is equal to the input voltage minus the VCC voltage. D_{BOOST} average current is less than 20 mA in most applications, so a low current ultra-fast recovery diode is recommended to limit the loss due to diode junction capacitance. Schottky diodes are also a viable option, particularly for lower input voltage applications, but attention must be paid to leakage currents at high temperatures.

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The internal gate drivers need a very low impedance path to the respective decoupling capacitors; the VCC cap for the LO driver and C_{BOOST} for the HO driver. These connections must be as short as possible to reduce inductance and as wide as possible to reduce resistance. The loop area, defined by the gate connection and its respective return path, must be minimized.

The high-side gate driver can also be used with HS connected to PGND for applications other than a half bridge converter (for example, push-pull). The HB pin is then connected to VCC, or any supply greater than the high-side driver undervoltage lockout (approximately 6.5 V). In addition, the high-side driver can be configured for high voltage offline applications where the high-side MOSFET gate is driven via a gate drive transformer.

8.2.2.5 Programmable Delay (DLY)

The R_{DLY} resistor programs the delays between the SR1 and SR2 signals and the HO and LO driver outputs. Figure 14 shows the relationship between these outputs. The DLY pin is nominally set at 2.5 V and the current is sensed through R_{DLY} to ground. This current is used to adjust the amount of dead time before the HO and LO pulse (T1) and after the HO and LO pulse (T2). Typically R_{DLY} is in the range of 10 kΩ to 100 kΩ. The dead-time periods can be calculated using Equation 7 and Equation 8:

$$T1 = [R_{DLY} \times 2.8\ ps] + 20\ ns \quad (7)$$

$$T2 = [R_{DLY} \times 1.35\ ps] + 6\ ns \quad (8)$$

T1 and T2 can be set to minimum by not connecting a resistor to DLY, connecting a resistor greater than 300 kΩ from DLY to ground, or connecting DLY to the REF pin. This may cause lower than optimal system efficiency if the delays through the SR signal transformer network, the secondary gate drivers and the SR MOSFETs are greater than the delay to turn on the HO or LO MOSFETs. must an SR MOSFET remain on while the opposing primary MOSFET is supplying power through the power transformer, the secondary winding will experience a momentary short circuit, causing a significant power loss to occur.

When choosing the R_{DLY} value, worst case propagation delays and component tolerances must be considered to assure that there is never a time where both SR MOSFETs are enabled AND one of the primary side MOSFETs is enabled. The time period T1 must be set so that the SR MOSFET has turned off before the primary MOSFET is enabled. Conversely, T1 and T2 must be kept as low as tolerances allow to optimize efficiency. The SR body diode conducts during the time between the SR MOSFET turns off and the power transformer begins supplying energy. Power losses increase when this happens since the body diode voltage drop is many times higher than the MOSFET channel voltage drop. The interval of body diode conduction can be observed with an oscilloscope as a negative 0.7 V to 1.5 V pulse at the SR MOSFET drain.

8.2.2.6 UVLO and OVP Voltage Divider Selection for R1, R2, and R3

Two dedicated comparators connected to the UVLO and OVP pins are used to detect undervoltage and overvoltage conditions. The threshold value of these comparators, V_{UVLO} and V_{OVP}, is 1.25 V (typical). The two functions can be programmed independently with two voltage dividers from VIN to AGND as shown in Figure 20 and Figure 21, or with a three-resistor divider as shown in Figure 22. Independent UVLO and OVP pins provide greater flexibility for the user to select the operational voltage range of the system. Hysteresis is accomplished by 23-µA current sources (I_{UVLO} and I_{OVP}), which are switched on or off into the sense pin resistor dividers as the comparators change state.

When the UVLO pin voltage is below 0.4 V, the controller is in a low current shutdown mode. For a UVLO pin voltage greater than 0.4 V but less than 1.25 V the controller is in standby mode. Once the UVLO pin voltage is greater than 1.25 V, the controller is fully enabled. Two external resistors can be used to program the minimum operational voltage for the power converter as shown in Figure 20. When the UVLO pin voltage falls below the 1.25-V threshold, an internal 23-µA current sink is enabled to lower the voltage at the UVLO pin, thus providing threshold hysteresis. Resistance values for R1 and R2 can be determined from Equation 9 and Equation 10.

$$R_1 = \frac{V_{HYS}}{23\ \mu A} \quad (9)$$

$$R_2 = \frac{1.25V \times R_1}{V_{PWR} - 1.25V - (23\ \mu A \times R_1)}$$

where

- V_{PWR} is the desired turnon voltage
- V_{HYS} is the desired UVLO hysteresis at V_{PWR} (10)

For example, if the LM5035 is to be enabled when V_{PWR} reaches 34 V, and disabled when VPWR is decreased to 32 V, R1 must be 87 kΩ, and R2 must be 3.54 kΩ. The voltage at the UVLO pin must not exceed 7 V at any time. Be sure to check both the power and voltage rating (0603 resistors can be rated as low as 50 V) for the selected R1 resistor.

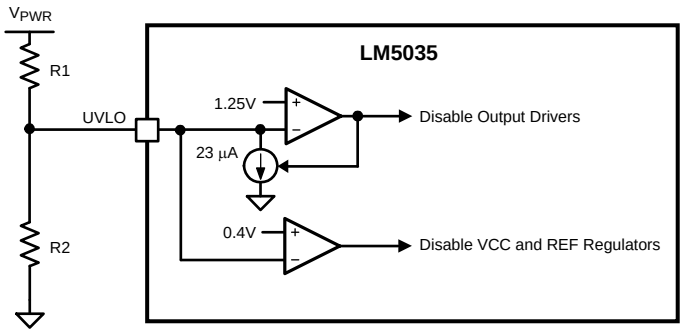

Figure 20. Basic UVLO Configuration

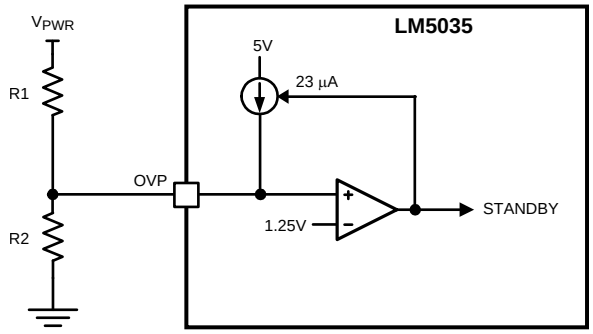

Figure 21. Basic Overvoltage Protection

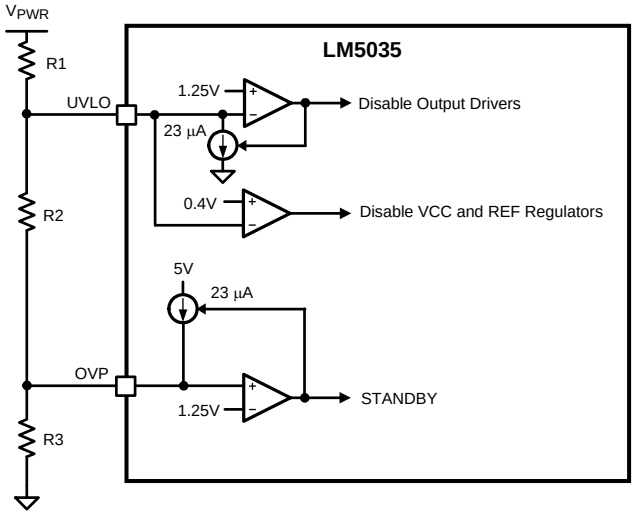

Figure 22. UVLO and OVP Divider

The impedance seen looking into the resistor divider from the UVLO and OVP pins determines the hysteresis level. UVLO and OVP enable and disable thresholds are calculated using the equations in Table 2 for the three-resistor divider listed in Figure 22.

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Table 2. UVO and OVP Divider Formulas

THRESHOLD	EQUATION
Outputs disabled due to VIN falling below UVLO threshold	$UVLO_{off} = 1.25V \times \left(\frac{R_1 + R_2 + R_3}{R_2 + R_3}\right)$ (11)
Outputs enabled due to VIN rising above UVLO threshold	$UVLO_{on} = UVLO_{off} + (23\ \mu A \times R_1)$
Outputs disabled due to VIN rising above OVP threshold	$OVP_{off} = 1.25V \times \left(\frac{R_1 + R_2 + R_3}{R_3}\right)$ (12)
Outputs enabled due to VIN falling below OVP threshold	$OVP_{on} = OVP_{off} – [23\ \mu A \times (R1 + R2)]$

The equations listed in Table 2 calculate the typical operating ranges of undervoltage and overvoltage thresholds. For example, for resistor values R_1 = 86.6 kΩ, R_2 = 2.1 kΩ and R_3 = 1.4 kΩ the calculated thresholds are as follows:

- UVLO turnoff = 32.2 V
- UVLO turnon = 34.2 V
- OVP turnon = 78.4 V
- OVP turnoff = 80.5 V

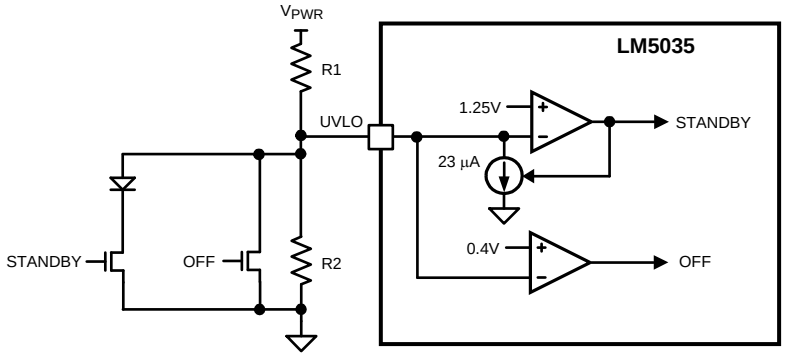

Figure 23. Remote Standby and Disable Control

To maintain the accuracy of the threshold, a resistor tolerance of 1% or better is recommended.

The design process begins with the selection of the voltage difference between the UVLO enabling and disabling thresholds. This selection also sets the approximate difference between OVP enabling and disabling regulation. Use Equation 13 to calculate the value of R_1.

$$R_1 = \frac{UVLO_{on} - UVLO_{off}}{23\ \mu A} \quad (13)$$

Next, the combined resistance of R_2 and R_3 is calculated by selecting the threshold for the UVLO disabling threshold. Use Equation 14 to calculate the value of $R_{COMBINED}$.

$$R_{COMBINED} = \frac{1.25V \times R_1}{UVLO_{off} – 1.25V} \quad (14)$$

The value of R_3 is then determined by selecting the OVP disabling threshold. Use Equation 15 to calculate the value of R_3.

$$R_3 = \frac{1.25V \times (R_1 + R_{COMBINED})}{OVP_{off}} \quad (15)$$

Finally, subtract the value of R_3 from the value of $R_{COMBINED}$ calculate the value of R_2 as shown in Equation 16.

$$R_2 = R_{COMBINED} — R_3 \quad (16)$$

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Remote configuration of the operational modes of the controller can be accomplished with open drain devices connected to the UVLO pin as shown in Figure 23.

8.2.2.7 Fault Protection

The overvoltage protection (OVP) comparator of the LM5035 can be configured for line or load fault protection or thermal protection using an external temperature sensor or thermistor. Figure 21 shows a line over voltage shutdown application using a voltage divider between the input power supply, V_{PWR}, and AGND to monitor the line voltage.

Figure 24 demonstrates the use of the OVP pin for latched output overvoltage fault protection, using a zener and optocoupler. When V_{OUT} exceeds the conduction threshold of the optocoupler diode and zener, the optocoupler momentarily turns on Q1 and the LM5035 enters standby mode, disabling the drivers and enabling the hysteresis current source on the OVP pin. When the current source is enabled, the OVP voltage will remain at 2.3 V (23 µA × 100 kΩ) without additional drive from the external circuit. If the optocoupler transistor emitter were directly connected to the OVP pin, then leakage current in the zener diode amplified by the gain of the optocoupler could falsely trip the protection latch. R1 and Q1 are added reduce the sensitivity to low level currents in the optocoupler. Using the values of Figure 24, the optocoupler collector current must equal $V_{BE(Q1)}$ / R1 = 350 µA before OVP latches. Once the controller has switched to standby mode, the outputs no longer switch but the VCC and REF regulators continue functioning and supply bias to the external circuitry. VCC must fall below 6.2 V or the UVLO pin must fall below 0.4 V to clear the OVP latch.

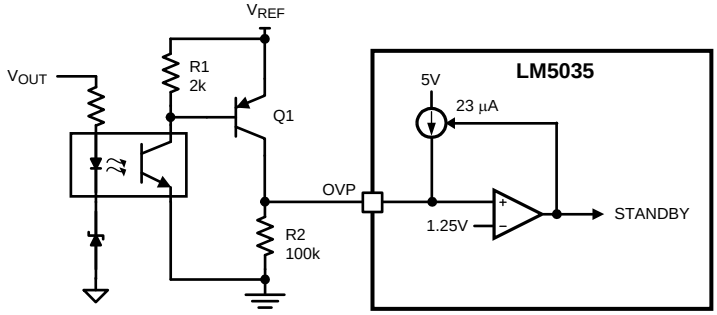

Figure 24. Latched Load Overvoltage Protection

Figure 25 shows an application of the OVP comparator for Remote Thermal Protection using a thermistor (or multiple thermistors) which may be located near the main heat sources of the power supply. The negative temperature coefficient (NTC) thermistor is nearly logarithmic, and in this example a 100kΩ thermistor with the β material constant of 4500 kelvins changes to approximately 2 kΩ at 130°C. Setting R1 to one-third of this resistance (665 Ω) establishes 130°C as the desired trip point (for V_{REF} = 5 V). In a temperature band from 20°C below to 20°C above the OVP threshold, the voltage divider is nearly linear with 25 mV per°C sensitivity.

R2 provides temperature hysteresis by raising the OVP comparator input by R2 × 23 µA. For example, if a 22-kΩ resistor is selected for R2, then the OVP pin voltage will increase by 22 kΩ × 23 µA = 506 mV. The NTC temperature must therefore fall by 506 mV / 25 mV per°C = 20°C before the LM5035 switches from the standby mode to the normal mode.

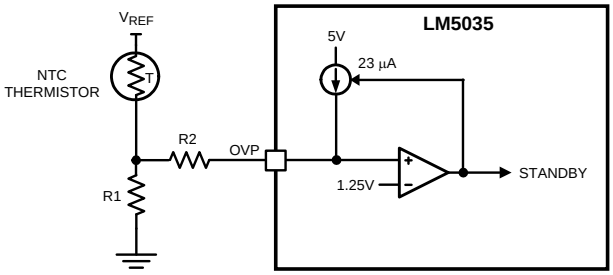

Figure 25. Remote Thermal Protection

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8.2.2.8 HICCUP Mode Current-Limit Restart (RES)

The basic operation of the hiccup mode current limit restart is described in the functional description. The delay time to restart is programmed with the selection of the RES pin capacitor C_{RES} as shown in Figure 25.

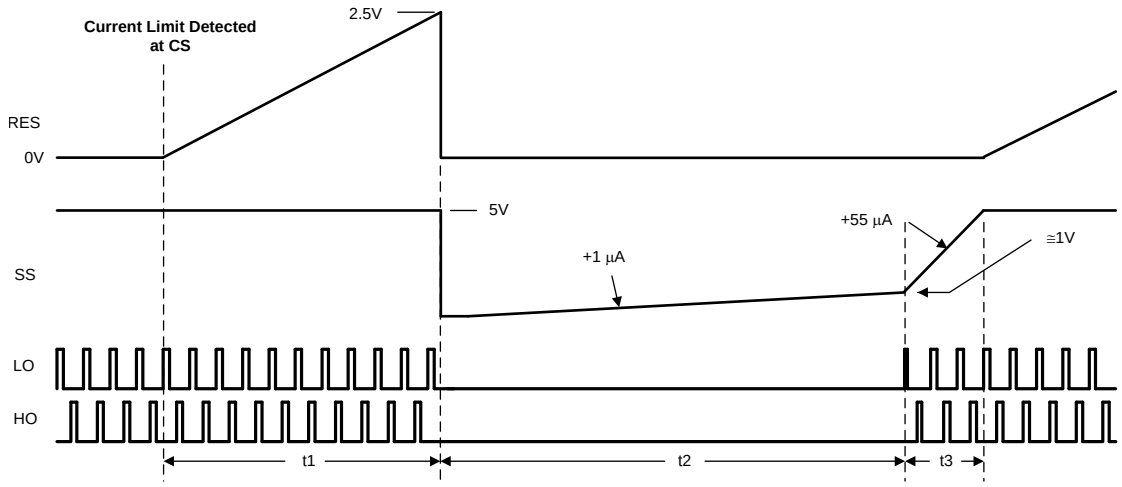

Figure 26. Hiccup Overload Restart Timing

In the case of continuous cycle-by-cycle current-limit detection at the CS pin, refer to Figure 26 and use Equation 17 to calculate the time required for C_{RES} to reach the 2.5-V hiccup mode threshold.

$$t1 = \frac{C_{RES} \times 2.5V}{22\ \mu A} = 114\ k\Omega \times C_{RES} \quad (17)$$

For example, if C_{RES} = 0.01 µF the time, t1, is approximately 1.14 ms.

The cool down time, t2 is set by the soft-start capacitor (C_{SS}) and the internal 1-µA SS current source. Use Equation 18 to calculate the value of t2.

$$t2 = \frac{C_{SS} \times 1V}{1\ \mu A} = 1\ M\Omega \times C_{SS} \quad (18)$$

If C_{SS} = 0.01 µF, the value of t2 is ≅ 10 ms.

The soft-start time t3 is set by the internal 55-µA current source. Use Equation 19 to calculate the value of t3.

$$t3 = \frac{C_{SS} \times 4V}{55\ \mu A} = 73\ k\Omega \times C_{SS} \quad (19)$$

If C_{SS} = 0.01 µF, the value of t3 is ≅ 730 µs.

The time t2 provides a periodic cool-down time for the power converter in the event of a sustained overload or short circuit. This off time results in lower average input current and lower power dissipation within the power components. It is recommended that the ratio of t2 / (t1 + t3) be in the range of 5 to 10 to take advantage of this feature.

If the application requires no delay from the first detection of a current limit condition to the onset of the hiccup mode (t1 = 0), the RES pin can be left open (no external capacitor). If it is desired to disable the hiccup mode entirely, the RES pin must be connected to ground (AGND).

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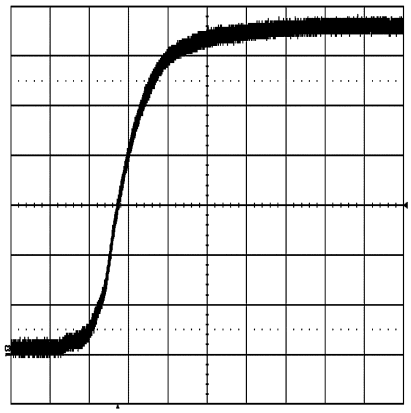
8.2.3 Application Curves

Figure 29 shows typical output ripple seen across the output terminals (with standard 10-µF and 1-µF ceramic capacitors) for an input voltage of 48 V and a load of 30 A. This waveform is typical of most loads and input voltages.

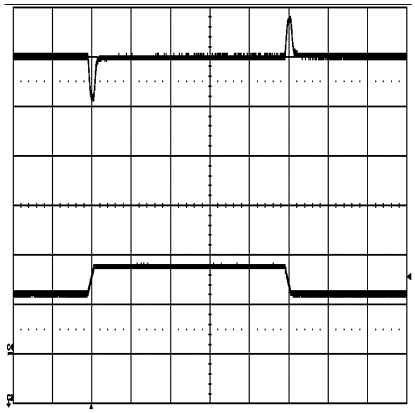
Figure 30 and Figure 31 show the drain voltage of Q1 with a 5-A load. Figure 30 represents an input voltage of 36 V and Figure 29 represents an input voltage of 72 V.

Figure 32 shows the gate voltages of the synchronous rectifiers. The dead time provided by the 20-kΩ DLY resistor is difficult to see at this timescale.



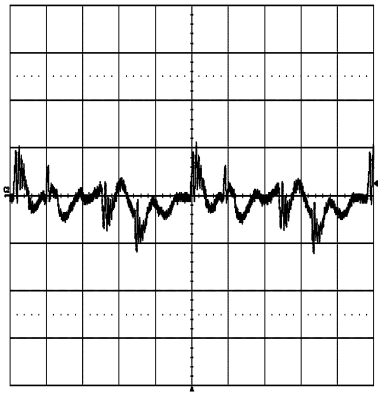
VIN = 48 VDC
I_{OUT} = 5 A
Horizontal resolution = 0.5 ms/div
Trace 1: output voltage V/div = 500 mV

Figure 27. Output Voltage During a Typical Start-Up



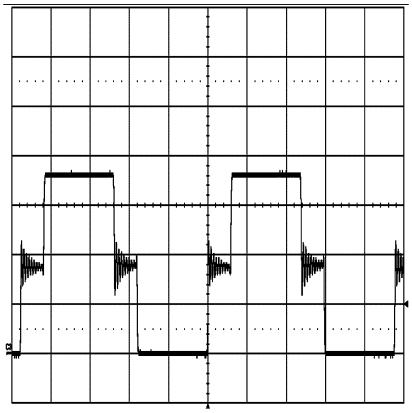
VIN = 48 VDC
I_{OUT} = 15 A to 22.5 A
Horizontal resolution = 0.5 ms/div
Upper trace: V_{OUT} V/div = 50 mV
Lower trace: I_{OUT} = 15 A to 22.5 A to 15 A

Figure 28. Transient Response for a Load Change From 15 A to 22.5 A



VIN = 48 VDC
I_{OUT} = 30 A
Trace 1: output ripple voltage V/div = 20 mV
Horizontal resolution = 1 µs/div
Bandwidth limit = 20 MHz

Figure 29. Typical Output Ripple Across the Output Terminals



VIN = 36 VDC
I_{OUT} = 5 A
Trace 1: Q1 drain voltage V/div = 10 V
Horizontal resolution = 1 µs/div

Figure 30. Drain Voltage of Q1 With a 5-A Load

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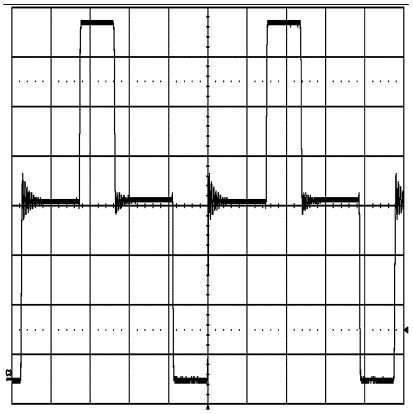
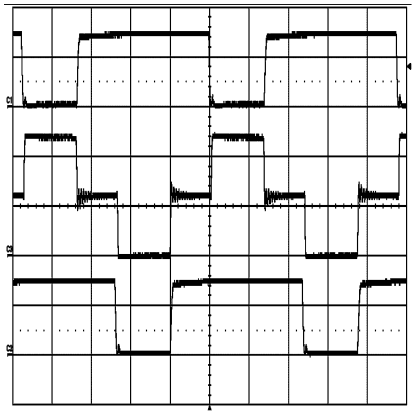


VIN = 72 VDC
I_{OUT} = 5 A
Trace 1: Q2 drain voltage V/div = 10 V
Horizontal resolution = 1 µs/div

Figure 31. Drain Voltage of Q1 With a 5-A Load



VIN = 48 VDC
I_{OUT} = 5 A
Upper trace: SR1, Q4 gate V/div = 5 V
Middle trace: HS, Q2 drain V/div = 20 V
Lower trace: SR2, Q6 gate V/div = 5 V
Horizontal resolution = 1 µs/div

Figure 32. Gate Voltages of the Synchronous Rectifiers

9 Power Supply Recommendations

The LM5035 can be used to control power levels up to 500 W; therefore, the current levels can be considerable. Care must be taken in choosing components with the correct current rating which includes: magnetic components, power MOSFETS and diodes, connectors, and wire sizes. Input and output capacitors must have the correct ripple current rating. The use of a multilayer PCB is recommended with a copper area chosen to ensure the LM5035 operates below the maximum junction temperature.

Full power loading must never be attempted without providing for adequate cooling.

10 Layout

10.1 Layout Guidelines

The LM5035 current sense and PWM comparators are very fast, and they respond to short duration noise pulses. The components at the CS, COMP, SS, OVP, UVLO, DLY, and the RT pins must be as physically close to the device as possible, thereby minimizing noise pickup on the PC board tracks.

Layout considerations are critical for the current sense filter. If a current sense transformer is used, both leads of the transformer secondary must be routed to the sense filter components and to the IC pins. The ground side of the transformer must be connected through a dedicated PC board track to the AGND pin rather than through the ground plane.

If the current sense circuit employs a sense resistor in the drive transistor source, low inductance resistors must be used. In this case, all the noise sensitive, low-current ground tracks must be connected in common near the device, and then a single connection made to the power ground (sense resistor ground point).

The gate drive outputs of the LM5035 must have short, direct paths to the power MOSFETs to minimize inductance in the PC board traces. The SR control outputs must also have minimum routing distance through the pulse transformers and through the secondary gate drivers to the sync FETs.

The two ground pins (AGND, PGND) must be connected together with a short, direct connection, to avoid jitter due to relative ground bounce.

If the internal dissipation of the LM5035 produces high junction temperatures during normal operation, the use of multiple vias under the IC to a ground plane can help conduct heat away from the IC. Judicious positioning of the PC board within the end product, along with use of any available air flow (forced or natural convection) will help reduce the junction temperatures. If using forced air cooling, avoid placing the LM5035 in the airflow shadow of tall components, such as input capacitors.

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10.2 Layout Example

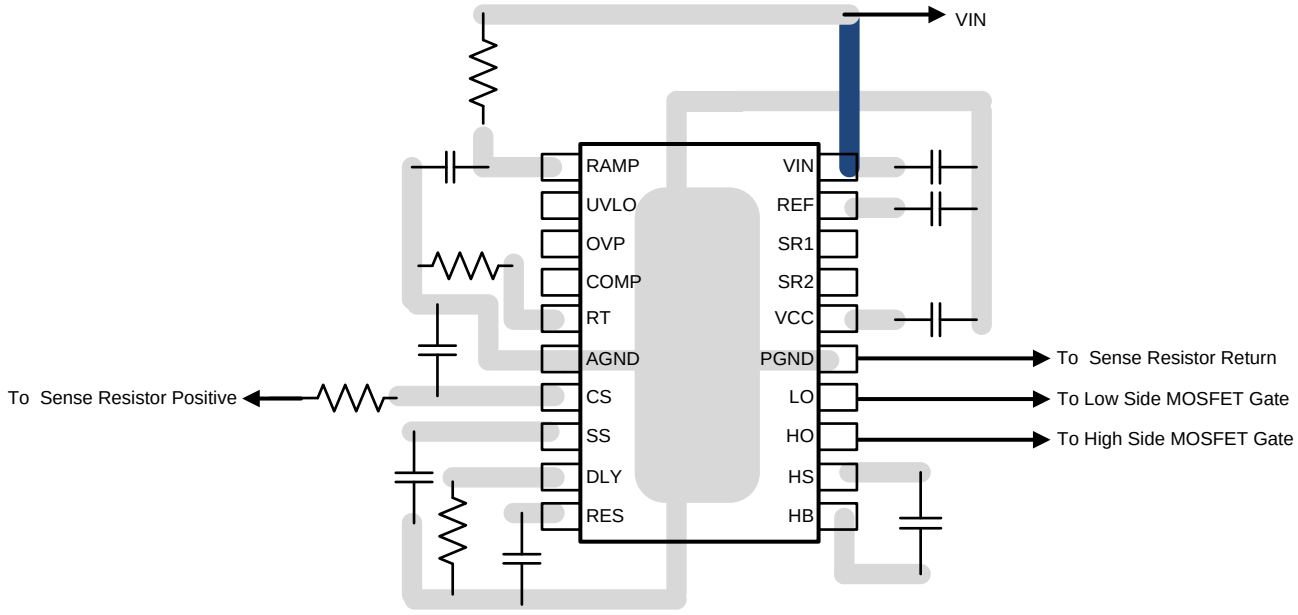

Figure 33. LM5035 Board Layout

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

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11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5035MH/NOPB	ACTIVE	HTSSOP	PWP	20	73	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM5035 MH	Samples
LM5035MHX/NOPB	ACTIVE	HTSSOP	PWP	20	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM5035 MH	Samples
LM5035SQ/NOPB	ACTIVE	WQFN	NHZ	24	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5035SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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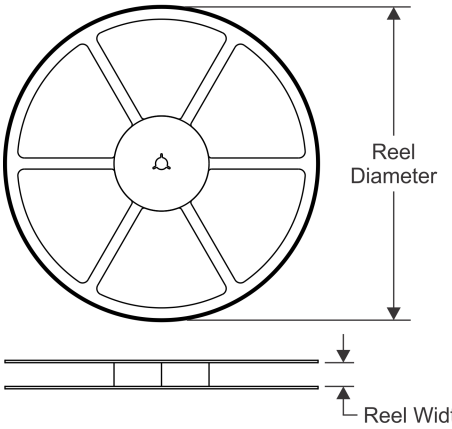
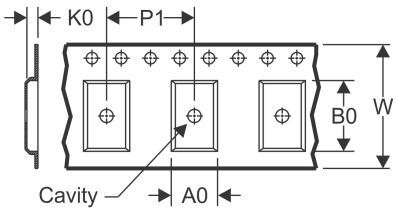
TAPE AND REEL INFORMATION

REEL DIMENSIONS

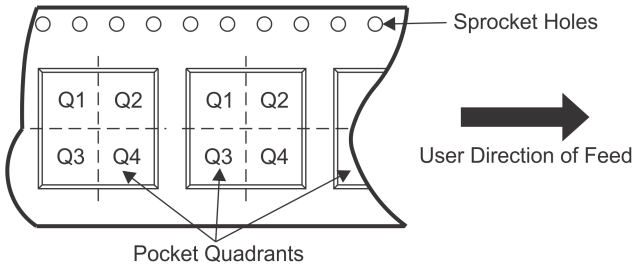


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

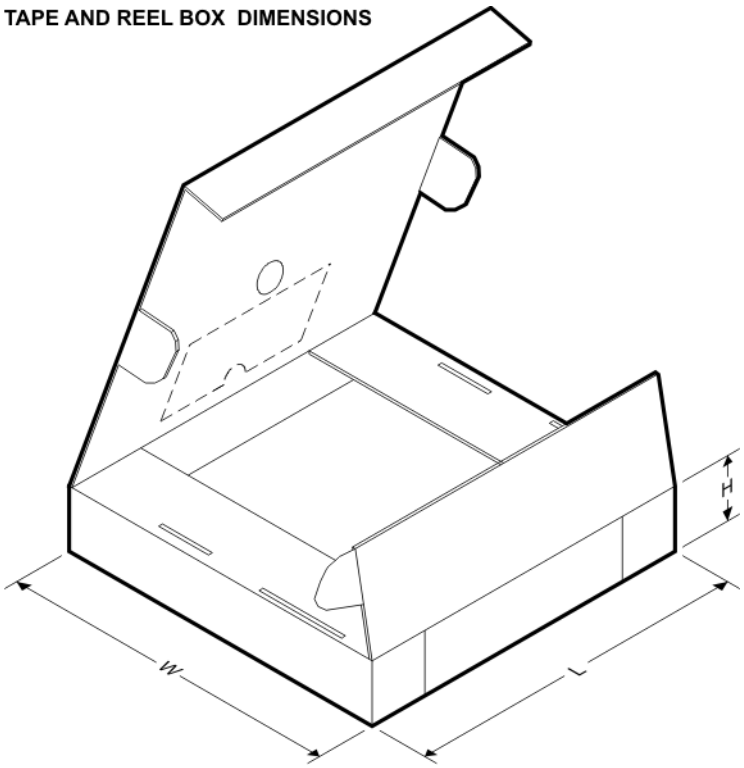
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5035MHX/NOPB	HTSSOP	PWP	20	2500	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
LM5035SQ/NOPB	WQFN	NHZ	24	1000	178.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

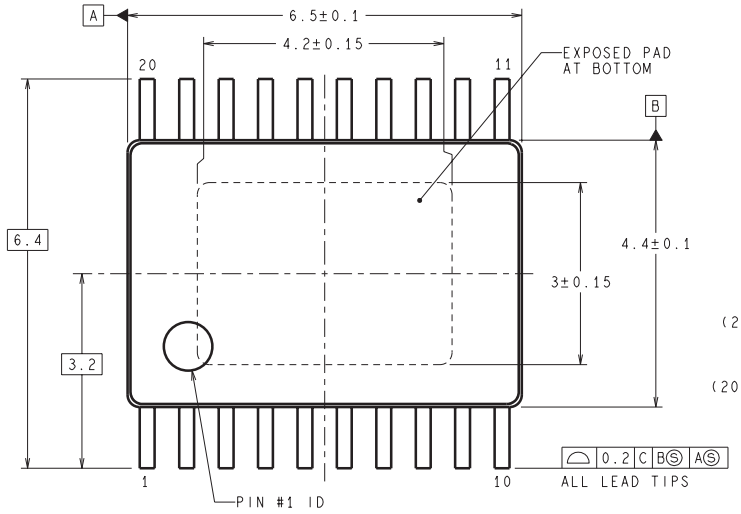
TAPE AND REEL BOX DIMENSIONS

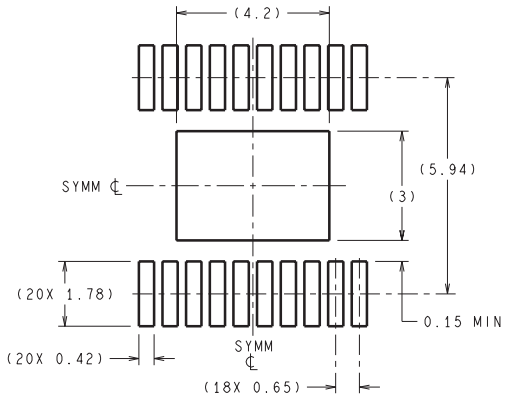


*All dimensions are nominal

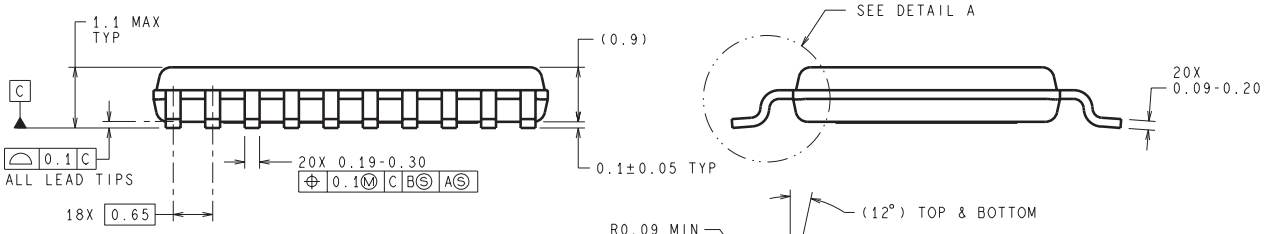
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5035MHX/NOPB	HTSSOP	PWP	20	2500	367.0	367.0	35.0
LM5035SQ/NOPB	WQFN	NHZ	24	1000	210.0	185.0	35.0

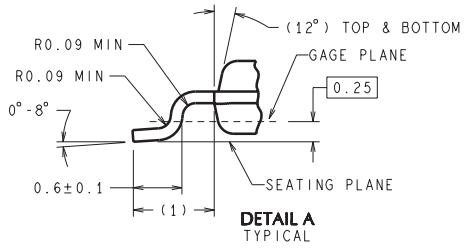
PWP0020A





RECOMMENDED LAND PATTERN





DETAIL A
TYPICAL

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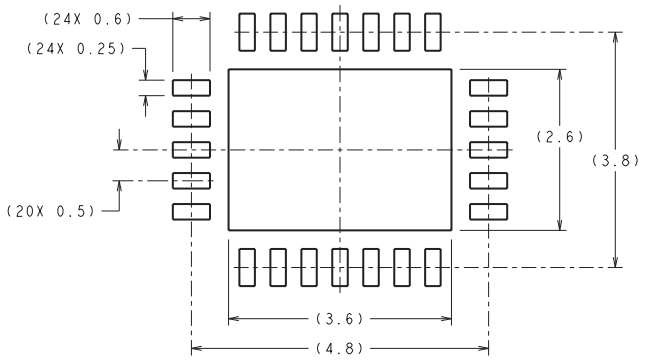
MXA20A (Rev C)

NHZ0024B



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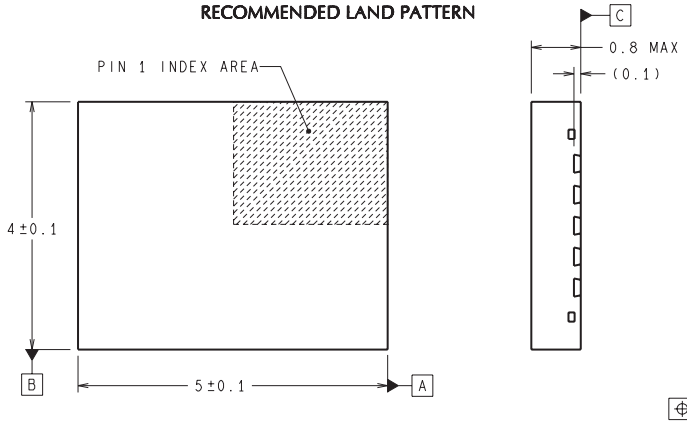

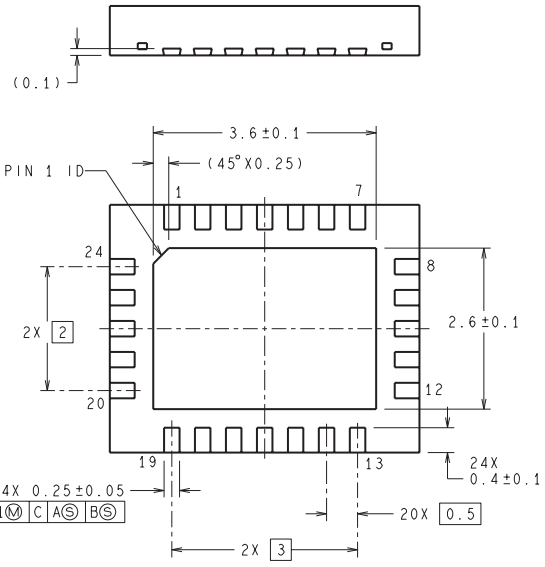

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