



THE DATASHEET OF LM83CIMQAX/NOPB



LM83

LM83 Triple-Diode Input and Local Digital Temperature Sensor with Two-Wire Interface



Literature Number: SNIS111A

LM83 Triple-Diode Input and Local Digital Temperature Sensor with Two-Wire Interface

General Description

The LM83 is a digital temperature sensor with a 2 wire serial interface that senses the voltage and thus the temperature of three remote diodes using a Delta-Sigma analog-to-digital converter with a digital over-temperature detector. The LM83 accurately senses its own temperature as well as the temperature of three external devices, such as Pentium II® Processors or diode connected 2N3904s. The temperature of any ASIC can be detected using the LM83 as long as a dedicated diode (semiconductor junction) is available on the die. Using the SMBus interface a host can access the LM83's registers at any time. Activation of a $\overline{T_CRIT_A}$ output occurs when any temperature is greater than a programmable comparator limit, T_CRIT . Activation of an \overline{INT} output occurs when any temperature is greater than its corresponding programmable comparator HIGH limit.

The host can program as well as read back the state of the T_CRIT register and the four T_HIGH registers. Three state logic inputs allow two pins (ADD0, ADD1) to select up to 9 SMBus address locations for the LM83. The sensor powers up with default thresholds of 127°C for T_CRIT and all T_HIGH s. The LM83 is pin for pin and register compatible with the LM84 as well as the Maxim MAX1617 and the Analog Devices ADM1021.

Features

- Accurately senses die temperature of 3 remote ICs, or diode junctions

- On-board local temperature sensing
- SMBus and I²C compatible interface, supports SMBus 1.1 TIMEOUT
- Two interrupt outputs: \overline{INT} and $\overline{T_CRIT_A}$
- Register readback capability
- 7 bit plus sign temperature data format, 1 °C resolution
- 2 address select pins allow connection of 9 LM83s on a single bus

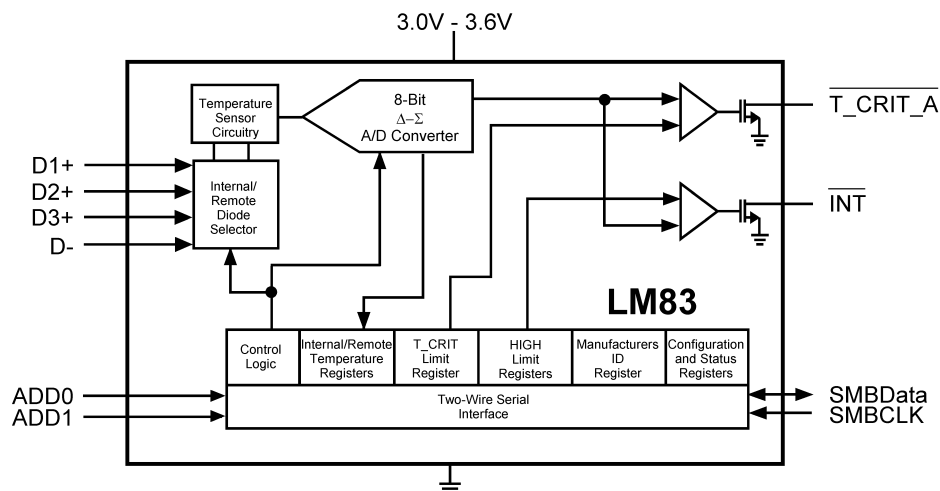
Key Specifications

- | | |
|--|----------------------------|
| ■ Supply Voltage | 3.0V to 3.6V |
| ■ Supply Current | 0.8mA (max) |
| ■ Local Temp Accuracy (includes quantization error) | 0°C to +85°C ±3.0°C (max) |
| ■ Remote Diode Temp Accuracy (includes quantization error) | +25°C to +100°C ±3°C (max) |
| | 0°C to +125°C ±4°C (max) |

Applications

- System Thermal Management
- Computers
- Electronic Test Equipment
- Office Electronics
- HVAC

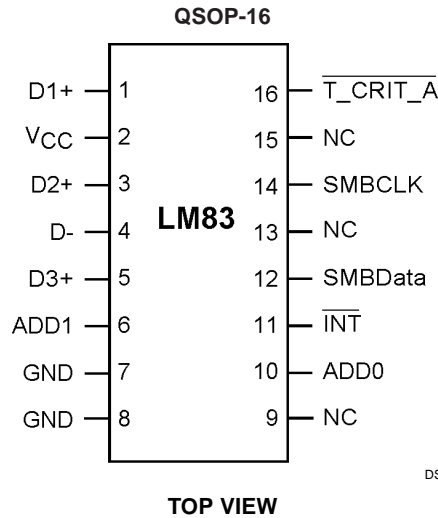
Simplified Block Diagram



DS101058-1

SMBus™ is a trademark of the Intel Corporation.
Pentium II® is a registered trademark of the Intel Corporation.
I²C® is a registered trademark of the Philips Corporation.

Connection Diagram

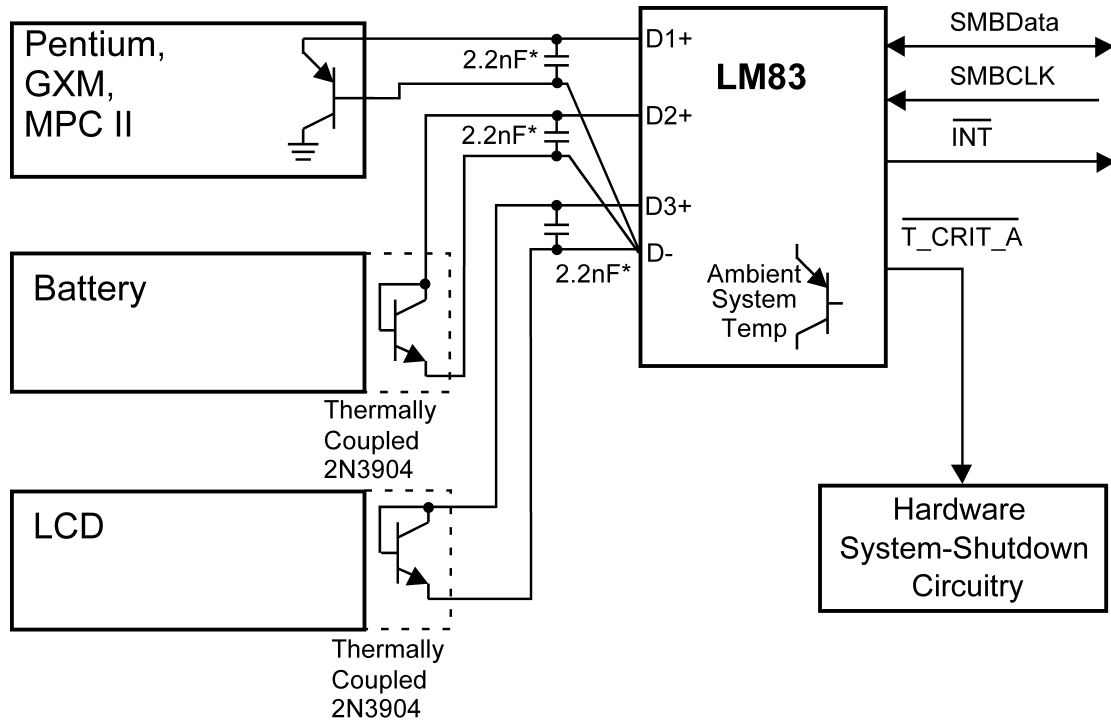


DS101058-2

Ordering Information

Order Number	NS Package Number	Transport Media
LM83CIMQA	MQA16A (QSOP-16)	95 Units in Rail
LM83CIMQAX	MQA16A (QSOP-16)	2500 Units on Tape and Reel

Typical Application



*Note: 2.2nF Capacitors must be placed as close as possible to D+ and D- pins of the LM83.

DS101058-3

Pin Description

Label	Pin #	Function	Typical Connection
D1+, D2+, D3+	1, 3, 5	Diode Current Source	To Diode Anode. Connected to remote discrete diode junction or to the diode junction on a remote IC whose die temperature is being sensed. When not used they should be left floating.
V _{CC}	2	Positive Supply Voltage Input	DC Voltage from 3.0 V to 3.6 V

Pin Description (Continued)

Label	Pin #	Function	Typical Connection
D-	4	Diode Return Current Sink	To all Diode Junction Cathodes using a star connection to pin. Must float when not used.
ADD0-ADD1	10, 6	User-Set SMBus (I ² C) Address Inputs	Ground (Low, "0"), V _{CC} (High, "1") or open ("TRI-LEVEL")
GND	7, 8	Power Supply Ground	Ground
NC	9, 13, 15	Manufacturing test pins.	Left floating. PC board traces may be routed through the pads for these pins, although the components that drive these traces should share the same supply as the LM83 so that the Absolute Maximum Rating, Voltage at Any Pin, is not violated.
$\overline{\text{INT}}$	11	Interrupt Output, open-drain	Pull Up Resistor, Controller Interrupt or Alert Line
SMBData	12	SMBus (I ² C) Serial Bi-Directional Data Line, open-drain output	From and to Controller, Pull-Up Resistor
SMBCLK	14	SMBus (I ² C) Clock Input	From Controller, Pull-Up Resistor
$\overline{\text{T_CRIT_A}}$	16	Critical Temperature Alarm, open-drain output	Pull Up Resistor, Controller Interrupt Line or System Shutdown

Absolute Maximum Ratings (Note 1)

Supply Voltage	-0.3 V to 6.0 V
Voltage at Any Pin	-0.3 V to ($V_{CC} + 0.3$ V)
D- Input Current	± 1 mA
Input Current at All Other Pins (Note 2)	5 mA
Package Input Current (Note 2)	20 mA
SMBData, $\overline{T_CRIT_A}$, \overline{INT} Output Sink Current	10 mA
SMBCLK, SMBData, $\overline{T_CRIT_A}$, \overline{INT} Output Voltage	6.0 V
Storage Temperature	-65°C to +150°C
Soldering Information, Lead Temperature	

QSOP Package (Note 3)

Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 4)	
Human Body Model	2000 V
Machine Model	200 V

Operating Ratings

(Notes 1, 5)

Specified Temperature Range	T_{MIN} to T_{MAX}
LM83	-40°C to +125°C
Supply Voltage Range (V_{CC})	+3.0V to +3.6V

Temperature-to-Digital Converter Characteristics

Unless otherwise noted, these specifications apply for $V_{CC}=+3.0$ Vdc to 3.6Vdc. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = T_J = +25^\circ\text{C}$, unless otherwise noted.

Parameter	Conditions	Typical (Note 6)	Limits (Note 7)	Units (Limit)
Temperature Error using Local Diode ((Note 8))	$T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC}=+3.3\text{V}$	± 1	± 3	$^\circ\text{C}$ (max)
	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC}=+3.3\text{V}$		± 4	$^\circ\text{C}$ (max)
Temperature Error using Remote Diode ((Note 8))	$T_A = +60^\circ\text{C}$ to $+100^\circ\text{C}$, $V_{CC}=+3.3\text{V}$		± 3	$^\circ\text{C}$ (max)
	$T_A = 25^\circ\text{C}$ to $+100^\circ\text{C}$, $V_{CC}=+3.3\text{V}$		± 3	$^\circ\text{C}$ (max)
	$T_A = 0^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC}=+3.3\text{V}$		± 4	$^\circ\text{C}$ (max)
Diode Channel to Channel Matching		0		$^\circ\text{C}$
Resolution		8		Bits
		1		$^\circ\text{C}$
Conversion Time of All Temperatures	(Note 10)	460	600	ms (max)
Quiescent Current (Note 9)	SMBus (I ² C) Inactive	0.500	0.80	mA (max)
D- Source Voltage		0.7		V
Diode Source Current	(D+ - D-)=+ 0.65V; high level		125	μA (max)
			60	μA (min)
	Low level		15	μA (max)
			5	μA (min)
$\overline{T_CRIT_A}$ and \overline{INT} Output Saturation Voltage	$I_{OUT} = 3.0$ mA		0.4	V (max)
Power-On Reset Threshold	On V_{CC} input, falling edge		2.3	V (max)
			1.8	V (min)
Local and Remote T_CRIT and HIGH Default Temperature settings	(Note 11)	+127		$^\circ\text{C}$

Logic Electrical Characteristics

DIGITAL DC CHARACTERISTICS

Unless otherwise noted, these specifications apply for $V_{CC}=+3.0$ to 3.6 Vdc. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = T_J = +25^\circ\text{C}$, unless otherwise noted.

Symbol	Parameter	Conditions	Typical (Note 6)	Limits (Note 7)	Units (Limit)
SMBData, SMBCLK					
$V_{IN(1)}$	Logical "1" Input Voltage			2.1	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage			0.8	V (max)
$V_{IN(HYST)}$	SMBData and SMBCLK Digital Input Hysteresis		300		mV
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = V_{CC}$	0.005	1.5	μA (max)
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0$ V	-0.005	1.5	μA (max)
ADD0, ADD1					
$V_{IN(1)}$	Logical "1" Input Voltage		V_{CC}	1.5	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage		GND	0.6	V (max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = V_{CC}$		2	μA (max)
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0$ V		-2	μA (max)
ALL DIGITAL INPUTS					
C_{IN}	Input Capacitance		20		pF
ALL DIGITAL OUTPUTS					
I_{OH}	High Level Output Current	$V_{OH} = V_{CC}$		100	μA (max)
V_{OL}	SMBus Low Level Output Voltage	$I_{OL} = 3$ mA $I_{OL} = 6$ mA		0.4 0.6	V (max)

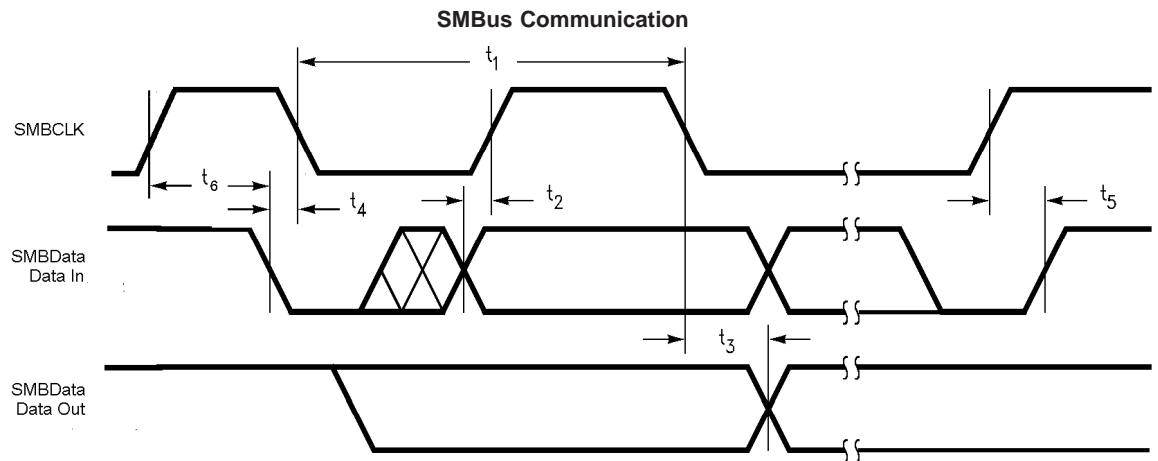
Logic Electrical Characteristics (Continued)

SMBus DIGITAL SWITCHING CHARACTERISTICS

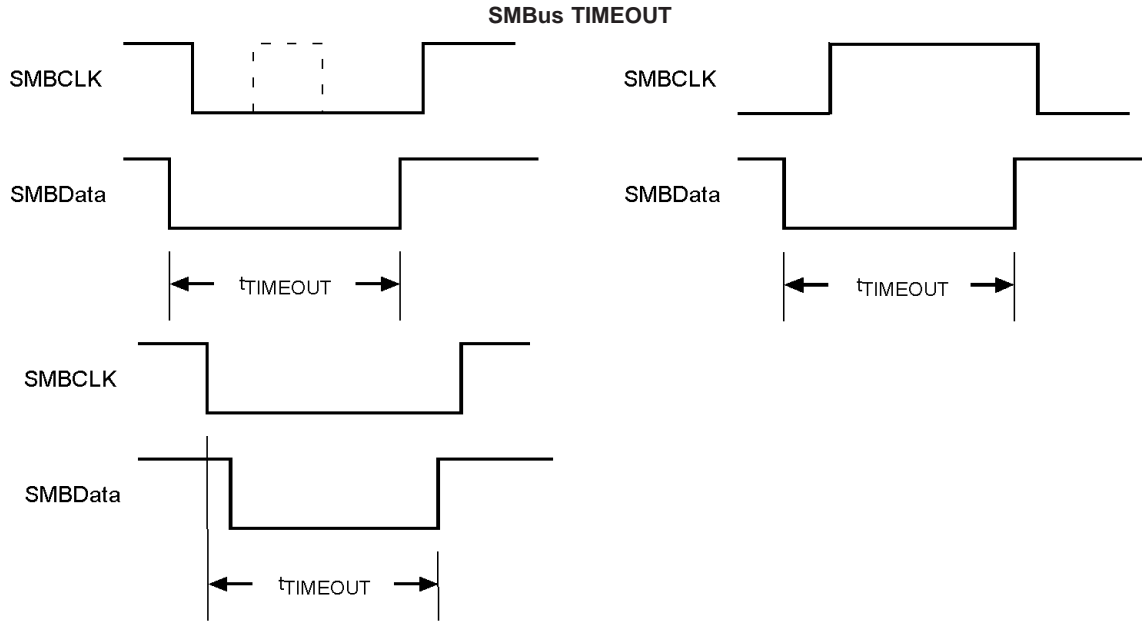
Unless otherwise noted, these specifications apply for $V_{CC}=+3.0$ Vdc to $+3.6$ Vdc, C_L (load capacitance) on output lines = 80 pF. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = T_J = +25^\circ\text{C}$, unless otherwise noted.

The switching characteristics of the LM83 fully meet or exceed the published specifications of the SMBus or I²C bus. The following parameters are the timing relationships between SMBCLK and SMBData signals related to the LM83. They are not the I²C or SMBus bus specifications.

Symbol	Parameter	Conditions	Typical (Note 6)	Limits (Note 7)	Units (Limit)
f_{SMB}	SMBus Clock Frequency			100 10	kHz (max) kHz (min)
t_{LOW}	SMBus Clock Low Time	10 % to 10 %		1.3 25	μs (min) ms (max)
$t_{LOWMEXT}$	Cumulative Clock Low Extend Time			10	ms (max)
t_{HIGH}	SMBus Clock High Time	90 % to 90%		0.6	μs (min)
$t_{R,SMB}$	SMBus Rise Time	10% to 90%	1		μs (max)
$t_{F,SMB}$	SMBus Fall Time	90% to 10%	0.3		ns (max)
t_{OF}	Output Fall Time	$C_L = 400$ pF, $I_O = 3$ mA		250	ns (max)
$t_{TIMEOUT}$	SMBData and SMBCLK Time Low for Reset of Serial Interface (Note 12)			25 40	ms (min) ms (max)
t_1	SMBCLK (Clock) Period			10	μs (min)
t_2 , $t_{SU,DAT}$	Data In Setup Time to SMBCLK High			100	ns (min)
t_3 , $t_{HD,DAT}$	Data Out Stable after SMBCLK Low			300 TBD	ns (min) ns (max)
t_4 , $t_{HD,STA}$	SMBData Low Setup Time to SMBCLK Low			100	ns (min)
t_5 , $t_{SU,STO}$	SMBData High Delay Time after SMBCLK High (Stop Condition Setup)			100	ns (min)
t_6 , $t_{SU,STA}$	SMBus Start-Condition Setup Time			0.6	μs (min)
t_{BUF}	SMBus Free Time			1.3	μs (min)



Logic Electrical Characteristics (Continued)



DS101058-7

See drawing DS10105807

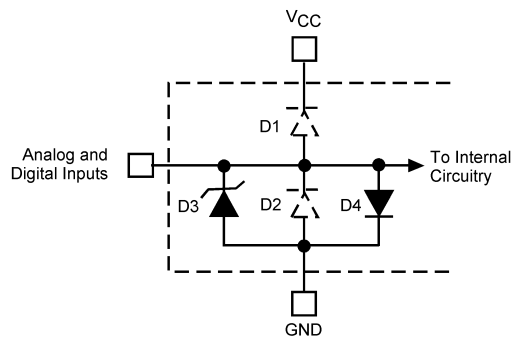
Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: When the input voltage (V_I) at any pin exceeds the power supplies ($V_I < GND$ or $V_I > V_{CC}$), the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four.

Parasitic components and or ESD protection circuitry are shown in the figure below for the LM83's pins. The nominal breakdown voltage of the zener D3 is 6.5 V. Care should be taken not to forward bias the parasitic diode, D1, present on pins: D+, D-, ADD1 and ADD0. Doing so by more than 50 mV may corrupt a temperature or voltage measurement.

Pin Name	D1	D2	D3	D4	Pin Name	D1	D2	D3	D4
					$\overline{T_CRIT_A}$ & \overline{INT}		x		
V_{CC}			x		SMBData		x	x	
D+	x	x	x		NC (pins 9 & 15)	x	x	x	
D-	x	x	x	x	SMBCLK		x	x	
ADD0, ADD1	x	x	x		NC (pin 13)		x	x	

Note: An x indicates that the diode exists.



DS101058-13

FIGURE 1. ESD Protection Input Structure

Note 3: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Note 4: Human body model, 100 pF discharged through a 1.5 k Ω resistor. Machine model, 200 pF discharged directly into each pin.

Note 5: Thermal resistance of the QSOP-16 package is xyz°C/W, junction-to-ambient when attached to a printed circuit board with 2 oz. foil as shown in Figure 3

Logic Electrical Characteristics (Continued)

Note 6: Typicals are at $T_A = 25^\circ\text{C}$ and represent most likely parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: The Temperature Error will vary less than $\pm 1.0^\circ\text{C}$ for a variation in V_{CC} of 3 V to 3.6 V from the nominal of 3.3 V.

Note 9: Quiescent current will not increase substantially with an active SMBus.

Note 10: This specification is provided only to indicate how often temperature data is updated. The LM83 can be read at any time without regard to conversion state (and will yield last conversion result).

Note 11: Default values set at power up.

Note 12: Holding the SMBData and/or SMBCLK lines Low for a time interval greater than t_{TIMEOUT} will cause the LM83 to reset SMBData and SMBCLK to the IDLE state of an SMBus communication (SMBCLK and SMBData set High).

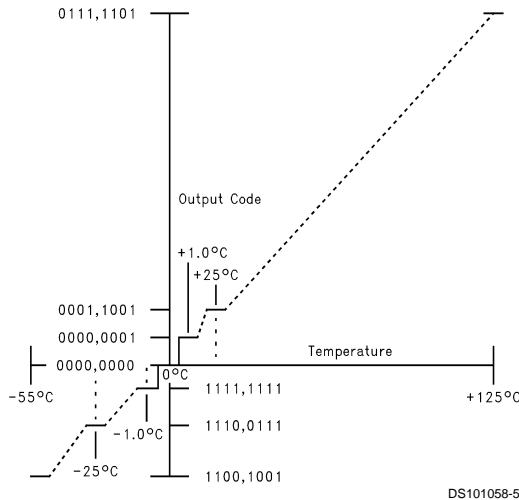


FIGURE 2. Temperature-to-Digital Transfer Function (Non-linear scale for clarity)

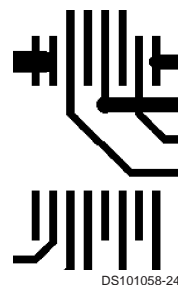


FIGURE 3. Printed Circuit Board Used for Thermal Resistance Specifications

1.0 Functional Description

The LM83 temperature sensor incorporates a band-gap type temperature sensor using a Local or three Remote diodes and an 8-bit ADC (Delta-Sigma Analog-to-Digital Converter). The LM83 is compatible with the serial SMBus and I²C two wire interfaces. Digital comparators compare Local (LT) and Remote (D1RT, D2RT and D3RT) temperature readings to user-programmable setpoints (LHS, D1RHS, D2RHS, D3RHS and TCS). Activation of the $\overline{\text{INT}}$ output indicates that a comparison is greater than the limit preset in a HIGH register. The T_{CRIT} setpoint (TCS) interacts with all the temperature readings. Activation of the $\overline{\text{T_CRIT_A}}$ output indicates that any or all of the temperature readings have exceeded the T_{CRIT} setpoint.

1.1 CONVERSION SEQUENCE

The LM83 converts its own temperature as well as 3 remote diode temperatures in the following sequence:

1. Local Temperature (LT)

2. Remote Diode 2 (D2RT)
3. Remote Diode 1 (D1RT)
4. Remote Diode 3 (D3RT)

This round robin sequence takes approximately 480 ms to complete as each temperature is digitized in approximately 120 ms.

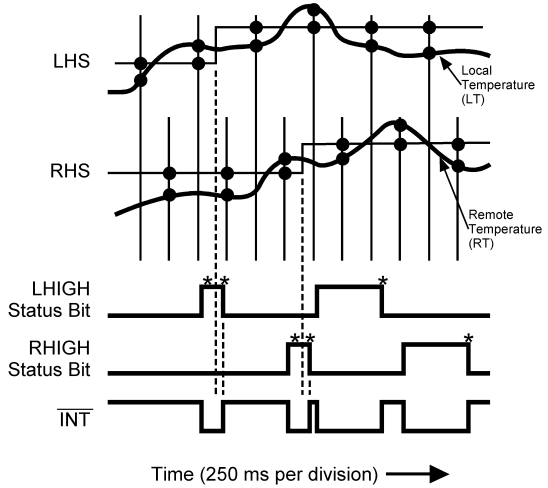
1.2 $\overline{\text{INT}}$ OUTPUT and T_{HIGH} LIMITS

Each temperature reading (LT, D1RT, D2RT, and D3RT) is associated with a T_{HIGH} setpoint register (LHS, D1RHS, D2RHS, D3RHS). At the end of a temperature reading a digital comparison determines whether that reading has exceeded its HIGH setpoint. If the temperature reading is greater than the HIGH setpoint, a bit is set in one of the Status Registers, to indicate which temperature reading, and the $\overline{\text{INT}}$ output is activated.

Local and remote temperature diodes are sampled in sequence by the A/D converter. The $\overline{\text{INT}}$ output and the Status

1.0 Functional Description (Continued)

Register flags are updated at the completion of a conversion, which occurs approximately 60 ms after a temperature diode is sampled. \overline{INT} is deactivated when the Status Register, containing the set bit, is read and a temperature reading is less than or equal to its corresponding HIGH setpoint, as shown in Figure 4. Figure 5 shows a simplified logic diagram for the \overline{INT} output and related circuitry.



* Note: Status Register Bits are reset by a read of Status Register where bit is located.

FIGURE 4. \overline{INT} Temperature Response Diagram with D2RHS and D3RHS set to 127°C.

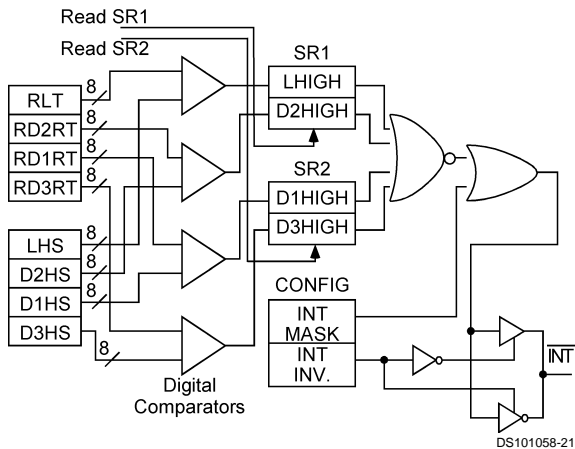


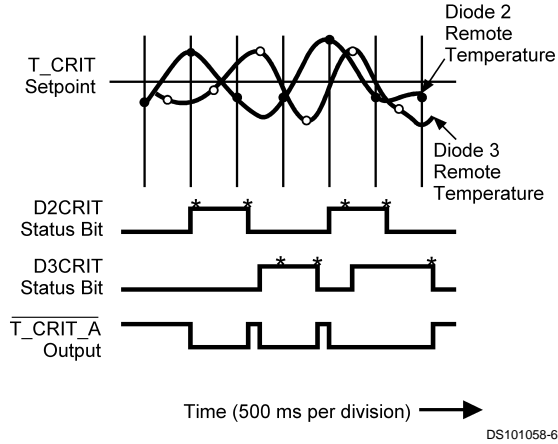
FIGURE 5. \overline{INT} output related circuitry logic diagram

The \overline{INT} output can be disabled by setting the \overline{INT} mask bit, D7, of the configuration register. \overline{INT} can be programmed to be active high or low by the state of the \overline{INT} inversion bit, D1, in the configuration register. A "0" would program \overline{INT} to be active low. \overline{INT} is an open-drain output.

1.3 $\overline{T_CRIT_A}$ OUTPUT and T_CRIT LIMIT

$\overline{T_CRIT_A}$ is activated when any temperature reading is greater than the limit preset in the critical temperature setpoint register (T_CRIT), as shown in Figure 6. The Status Registers can be read to determine which event caused the alarm. A bit in the Status Registers is set high to indicate which temperature reading exceeded the T_CRIT setpoint and caused the alarm, see Section 2.3.

Local and remote temperature diodes are sampled in sequence by the A/D converter. The $\overline{T_CRIT_A}$ output and the Status Register flags are updated at the completion of a conversion. $\overline{T_CRIT_A}$ and the Status Register flags are reset only after the Status Register is read and if a temperature conversion is below the T_CRIT setpoint, as shown in Figure 6. Figure 7 shows a simplified logic diagram of the $\overline{T_CRIT_A}$ and related circuitry.



* Note: Status Register Bits are reset by a read of Status Register where bit is located.

FIGURE 6. $\overline{T_CRIT_A}$ Temperature Response Diagram with remote diode 1 and local temperature masked.

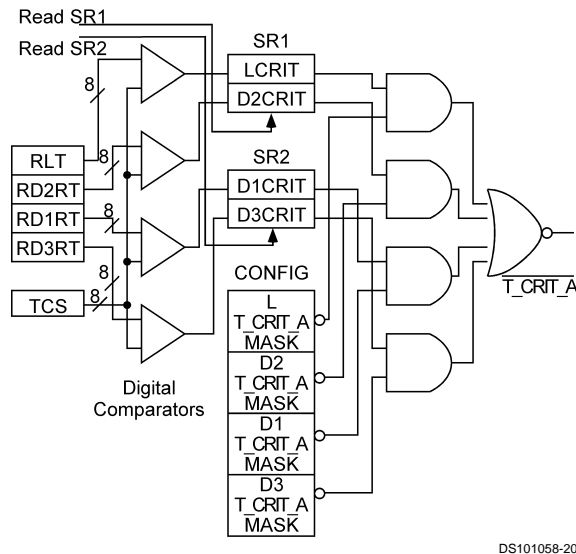


FIGURE 7. $\overline{T_CRIT_A}$ output related circuitry logic diagram

Located in the Configuration Register are the mask bits for each temperature reading, see Section 2.5. When a mask bit is set, its corresponding status flag will not propagate to the $\overline{T_CRIT_A}$ output, but will still be set in the Status Registers. Setting all four mask bits or programming the T_CRIT setpoint to 127°C will disable the $\overline{T_CRIT_A}$ output.

1.4 POWER ON RESET DEFAULT STATES

LM83 always powers up to these known default states:

1. Command Register set to 00h
2. Local Temperature set to 0°C

1.0 Functional Description (Continued)

- Diode 1, Diode 2, and Diode 3 Remote Temperature set to 0°C until the LM83 senses a diode present between the D+ and D- input pins.
- Status Registers 1 and 2 set to 00h.
- Configuration Register set to 00h; $\overline{\text{INT}}$ enabled and all T_CRIT setpoints enabled to activate $\overline{\text{T_CRIT_A}}$.
- Local and all Remote T_CRIT set to 127°C

1.5 SMBus INTERFACE

The LM83 operates as a slave on the SMBus, so the SMBCLK line is an input (no clock is generated by the LM83) and the SMBData line is bi-directional. According to SMBus specifications, the LM83 has a 7-bit slave address. Bit 4 (A3) of the slave address is hard wired inside the LM83 to a 1. The remainder of the address bits are controlled by the state of the address select pins ADD1 and ADD0, and are set by connecting these pins to ground for a low, (0) , to V_{CC} for a high, (1), or left floating (TRI-LEVEL).

Therefore, the complete slave address is:

A6	A5	A4	1	A2	A1	A0
MSB						LSB

and is selected as follows:

Address Select Pin State		LM83 SMBus Slave Address
ADD0	ADD1	A6:A0 binary
0	0	001 1000
0	TRI-LEVEL	001 1001
0	1	001 1010
TRI-LEVEL	0	010 1001
TRI-LEVEL	TRI-LEVEL	010 1010
TRI-LEVEL	1	010 1011
1	0	100 1100
1	TRI-LEVEL	100 1101
1	1	100 1110

The LM83 latches the state of the address select pins during the first read or write on the SMBus. Changing the state of the address select pins after the first read or write to any device on the SMBus will not change the slave address of the LM83.

1.6 TEMPERATURE DATA FORMAT

Temperature data can be read from the Local and Remote Temperature, T_CRIT, and HIGH setpoint registers; and written to the T_CRIT and HIGH setpoint registers. Temperature data is represented by an 8-bit, two's complement byte with an LSB (Least Significant Bit) equal to 1°C:

Temperature	Digital Output	
	Binary	Hex
+125°C	0111 1101	7Dh
+25°C	0001 1001	19h
+1°C	0000 0001	01h
0°C	0000 0000	00h
-1°C	1111 1111	FFh
-25°C	1110 0111	E7h
-55°C	1100 1001	C9h

1.7 OPEN-DRAIN OUTPUTS

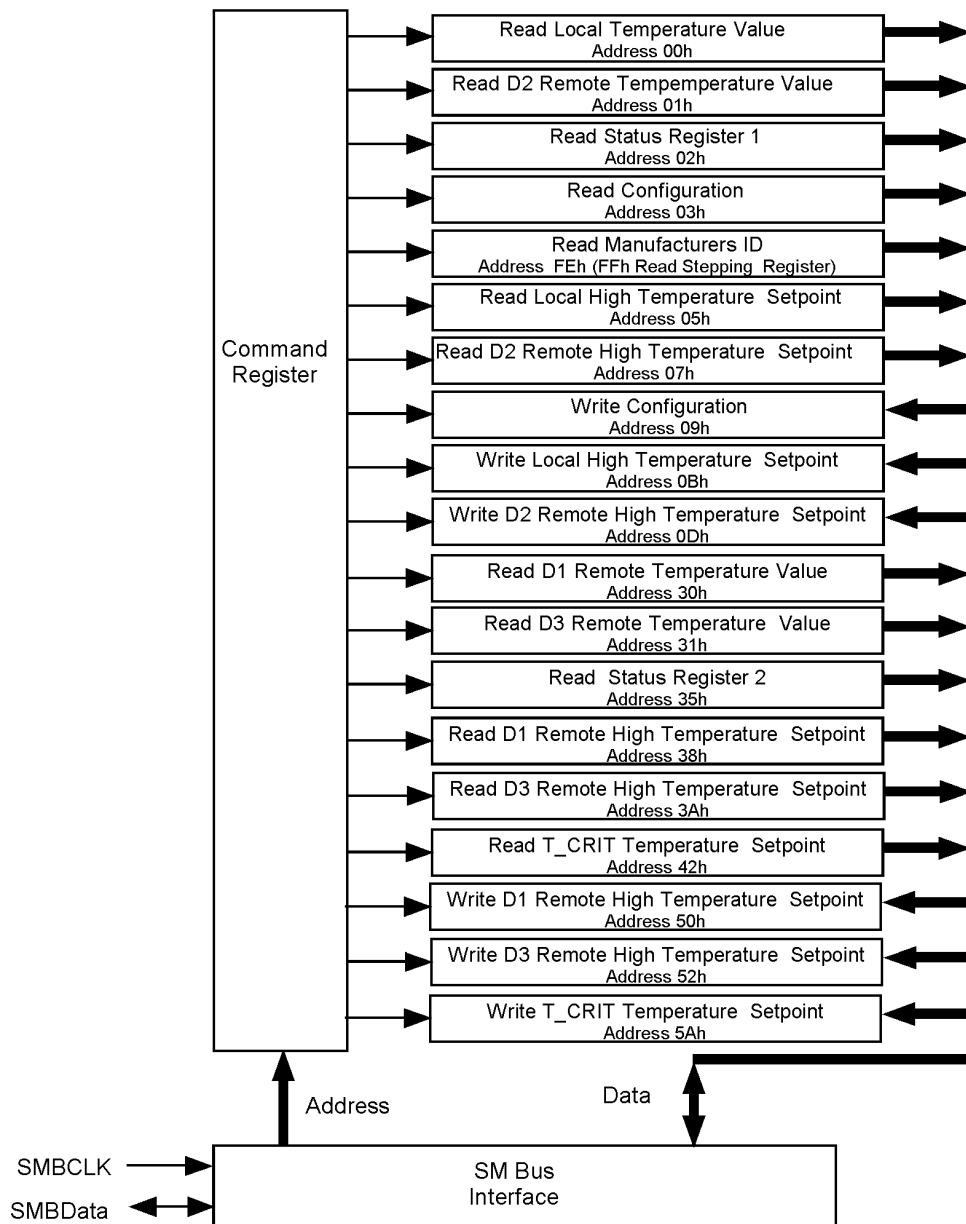
The SMBData, $\overline{\text{INT}}$ and $\overline{\text{T_CRIT_A}}$ outputs are open-drain outputs and do not have internal pull-ups. A "high" level will not be observed on these pins until pull-up current is provided from some external source, typically a pull-up resistor. Choice of resistor value depends on many system factors but, in general, the pull-up resistor should be as large as possible. This will minimize any internal temperature reading errors due to internal heating of the LM83. The maximum resistance of the pull up, based on LM83 specification for High Level Output Current, to provide a 2.1V high level, is 30kΩ.

1.8 DIODE FAULT DETECTION

Before each external conversion the LM83 goes through an external diode fault detection sequence. If a D+ input is shorted to V_{CC} or floating then the temperature reading will be +127 °C, and its OPEN bit in the Status Register will be set. If the T_CRIT setpoint is set to less than +127 °C then the D+ inputs RTCRIT bit in the Status Register will be set which will activate the $\overline{\text{T_CRIT_A}}$ output, if enabled. If a D+ is shorted to GND or D-, its temperature reading will be 0 °C and its OPEN bit in the Status Register will not be set.

1.0 Functional Description (Continued)

1.9 COMMUNICATING with the LM83



DS101058-9

There are 19 data registers in the LM83, selected by the Command Register. At power-up the Command Register is set to "00", the location for the Read Local Temperature Register. The Command Register latches the last location it was set to. Reading the Status Register resets $\overline{T_CRIT_A}$ and \overline{INT} , so long as a temperature comparison does not signal a fault (see *Sections 1.2 and 1.3*). All other registers are pre-defined as read only or write only. Read and write registers with the same function contain mirrored data.

A **Write** to the LM83 will always include the address byte and the command byte. A write to any register requires one data byte.

Reading the LM83 can take place either of two ways:

1. If the location latched in the Command Register is correct (most of the time it is expected that the Command Register will point to one of the Read Temperature Reg-

isters because that will be the data most frequently read from the LM83), then the read can simply consist of an address byte, followed by retrieving the data byte.

2. If the Command Register needs to be set, then an address byte, command byte, repeat start, and another address byte will accomplish a read.

The data byte has the most significant bit first. At the end of a read, the LM83 can accept either Acknowledge or No Acknowledge from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte).

1.10 SERIAL INTERFACE ERROR RECOVERY

The LM83 SMBus lines will be reset to the SMBus idle state if the SMBData or SMBCLK lines are held low for 40 ms or more ($t_{TIMEOUT}$). The LM83 may or may not reset the state of

1.0 Functional Description (Continued)

the serial interface logic if either of the SMBData or SMBCLK lines are held low between 25 ms and 40 ms. TIMEOUT allows a clean recovery in cases where the master may be reset while the LM83 is transmitting a low bit thus preventing possible bus lock up.

Whenever the LM83 sees the start condition its serial interface will reset to the beginning of the communication, thus the LM83 will expect to see an address byte next. This simplifies recovery when the master is reset while the LM83 is transmitting a high.

1.0 Functional Description (Continued)

2.0 LM83 REGISTERS

2.1 COMMAND REGISTER

Selects which registers will be read from or written to. Data for this register should be transmitted during the Command Byte of the SMBus write communication.

P7	P6	P5	P4	P3	P2	P1	P0
0	Command Select						

P0-P7: Command Select

Command Select Address	Power On Default State		Register Name	Register Function
	<P7:P0> hex	<D7:D0> binary		
00h	0000 0000	0	RLT	Read Local Temperature
01h	0000 0000	0	RD2RT	Read D2 Remote Temperature
02h	0000 0000	0	RSR1	Read Status Register 1
03h	0000 0000	0	RC	Read Configuration
04h	0000 0000	0		Reserved
05h	0111 1111	127	RLHS	Read Local HIGH Setpoint
06h				Reserved
07h	0111 1111	127	RD2RHS	Read D2 Remote HIGH Setpoint
08h				Reserved
09h	0000 0000		WC	Write Configuration
0Ah				Reserved
0Bh	0111 1111	127	WD2LHS	Write Local HIGH Setpoint
0Ch				Reserved
0Dh	0111 1111	127	WD2RHS	Write D2 Remote HIGH Setpoint
0Eh-2Fh				Reserved for Future Use
30h	0000 0000	0	RD1RT	Read D1 Remote Temperature
31h	0000 0000	0	RD3RT	Read D3 Remote Temperature
32h-34h				Reserved for Future Use
35h	0000 0000	0	RSR2	Read Status Register 2
36h-37h				Reserved for Future Use
38h	0111 1111	127	RD1RHS	Read D1 Remote HIGH Setpoint
39h				Reserved for Future Use
3Ah	0111 1111	127	RD3RHS	Read D3 Remote HIGH Setpoint
3Bh-41h				Reserved for Future Use
42h	0111 1111	127	RTCS	Read T_CRIT Setpoint
43h-4Fh				Reserved for Future Use
50h	0111 1111	127	WD1RHS	Write D1 Remote HIGH Setpoint
51h				Reserved for Future Use
52h	0111 1111	127	WD3RHS	Write D3 Remote HIGH Setpoint
53h-59h				Reserved for Future Use
5Ah	0111 1111	127	WTCS	Write T_CRIT Setpoint

1.0 Functional Description (Continued)

Command Select Address	Power On Default State		Register Name	Register Function
	<D7:D0> binary	<D7:D0> decimal		
5Ch-6Fh and F0h-FDh				Reserved for Future Use
FEh	0000 0001	1	RMID	Read Manufacturers ID
FFh			RSR	Read Stepping or Die Revision Code

2.2 LOCAL and D1, D2 and D3 REMOTE TEMPERATURE REGISTERS (LT, D1RT, D2RT, and D3RT)

(Read Only Address 00h, 01h, 30h and 31h):

D7	D6	D5	D4	D3	D2	D1	D0
MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB

D7–D0: Temperature Data. One LSB = 1°C. Two's complement format.

2.3 STATUS REGISTERS 1 and 2

2.3.1 Status Register 1 (SR1) (Read Only Address 02h):

D7	D6	D5	D4	D3	D2	D1	D0
0	LHIGH	0	D2RHIGH	0	D2OPEN	D2CRIT	LCRIT

Power up default is with all bits "0" (zero).

D0: LCRIT: When set to a 1 indicates an Local Critical Temperature alarm.

D1: D2CRIT: When set to a 1 indicates a Remote Diode 2 Critical Temperature alarm.

D2: D2OPEN: When set to 1 indicates a Remote Diode 2 disconnect.

D4: D2RHIGH: When set to 1 indicates a Remote Diode 2 HIGH Temperature alarm.

D6: LHIGH: When set to 1 indicates a Local HIGH Temperature alarm.

D7, D5, and D3: These bits are always set to 0 and reserved for future use.

Status Register 2

2.3.2 Status Register 2 (SR2) (Read Only Address 35h):

D7	D6	D5	D4	D3	D2	D1	D0
D1RHIGH	0	D1OPEN	D3RHIGH	0	D3OPEN	D3CRIT	D1CRIT

Power up default is with all bits "0" (zero).

D0: D1CRIT, when set to 1 indicates a Remote Diode 1 Critical Temperature alarm.

D1: D3CRIT, when set to 1 indicates a Remote Diode 3 Critical Temperature alarm.

D2: D3OPEN, when set to 1 indicates a Remote Diode 3 disconnect.

D4: D3RHIGH, when set to 1 indicates a Remote Diode 3 HIGH Temperature alarm.

D5: D1OPEN, when set to 1 indicates a Remote Diode 1 disconnect.

D7: D1RHIGH, when set to 1 indicates a Remote Diode 1 HIGH Temperature alarm.

D6, and D3: These bits are always set to 0 and reserved for future use.

2.4 MANUFACTURERS ID REGISTER

(Read Address FEh) Default value 01h.

2.5 CONFIGURATION REGISTER

(Read Address 03h/Write Address 09h):

D7	D6	D5	D4	D3	D2	D1	D0
$\overline{\text{INT}}$ mask	0	D1 $\overline{\text{T_CRIT_A}}$ mask	D2 $\overline{\text{T_CRIT_A}}$ mask	D3 $\overline{\text{T_CRIT_A}}$ mask	Local $\overline{\text{T_CRIT_A}}$ mask	$\overline{\text{INT}}$ Inversion	0

Power up default is with all bits "0" (zero).

D7: $\overline{\text{INT}}$ mask: When set to 1 $\overline{\text{INT}}$ interrupts are masked.

1.0 Functional Description (Continued)

D5: T_CRIT mask for Diode 1, when set to 1 a Diode 1 temperature reading that exceeds T_CRIT setpoint will not activate the $\overline{T_CRIT_A}$ pin.

D4: T_CRIT mask for Diode 2, when set to 1 a Diode 2 temperature reading that exceeds T_CRIT setpoint will not activate the $\overline{T_CRIT_A}$ pin.

D3: T_CRIT mask for Diode 3, when set to 1 a Diode 3 temperature reading that exceeds T_CRIT setpoint will not activate the $\overline{T_CRIT_A}$ pin.

D2: T_CRIT mask for Local reading, when set to 1 a Local temperature reading that exceeds T_CRIT setpoint will not activate the $\overline{T_CRIT_A}$ pin.

D1: \overline{INT} active state inversion. When \overline{INT} Inversion is set to a 1 the active state of the \overline{INT} output will be a logical high. A low would then select an active state of a logical low.

D6 and D0: These bits are always set to 0 and reserved for future use. A write of 1 will return a 0 when read.

2.6 LOCAL, DIODE 1, DIODE 2 and DIODE 3 HIGH SETPOINT REGISTERS (LHS, D1RHS, D2RHS and D3RHS)

(Read Address 05h, 07h, 38h, 3Ah /Write Address 0Bh, 0Dh, 50h, 52h):

D7	D6	D5	D4	D3	D2	D1	D0
MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB

D7–D0: HIGH setpoint temperature data. Power up default is LHIGH = RD1HIGH=RD2HIGH=RD3HIGH = 127°C.

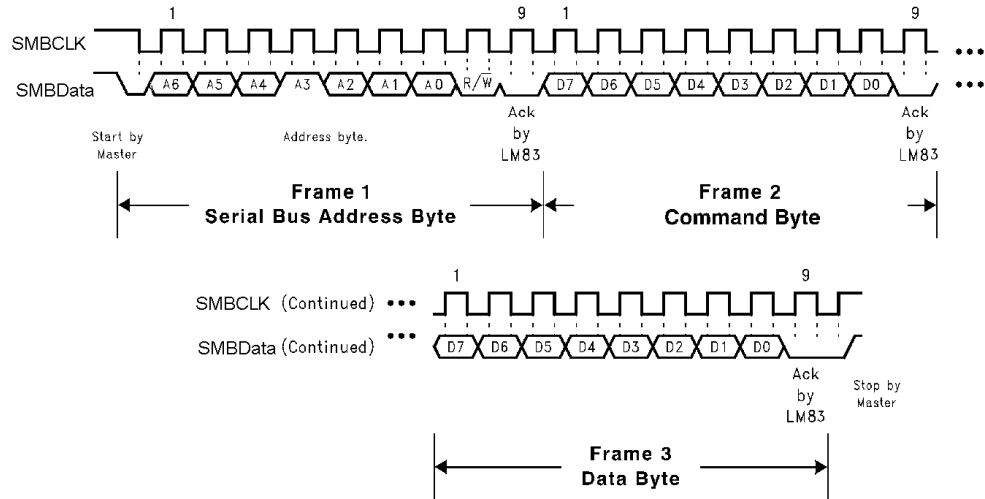
2.7 T_CRIT REGISTER (TCS)

(Read Address 42h/Write Address 5Ah):

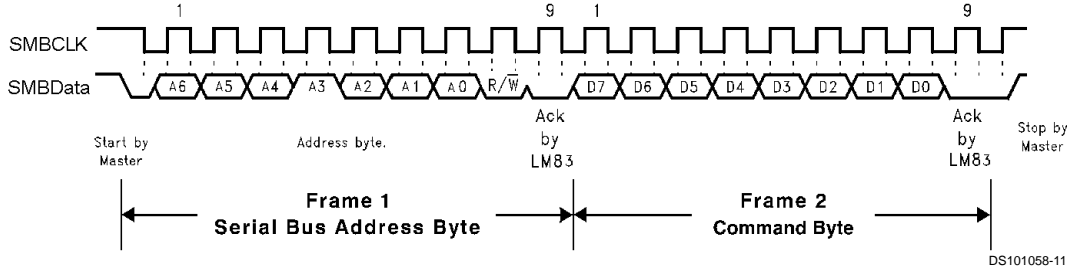
D7	D6	D5	D4	D3	D2	D1	D0
MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB

D7–D0: T_CRIT setpoint temperature data. Power up default is T_CRIT = 127°C.

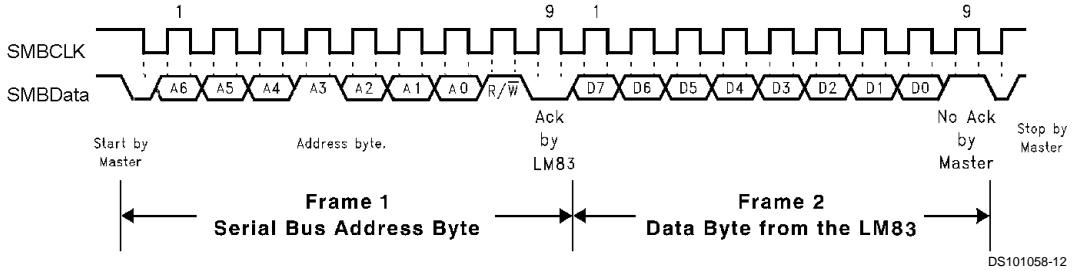
3.0 SMBus Timing Diagrams



(a) Serial Bus Write to the internal Command Register followed by a the Data Byte



(b) Serial Bus Write to the internal Command Register



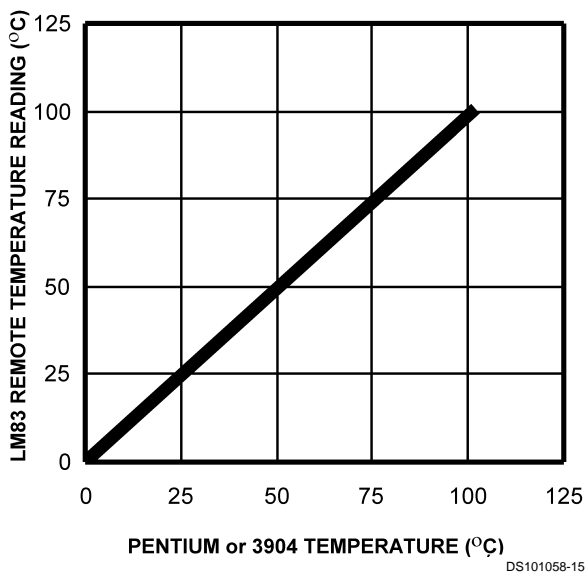
(c) Serial Bus Read from a Register with the internal Command Register preset to desired value.

FIGURE 8. Serial Bus Timing Diagrams

4.0 Application Hints

The LM83 can be applied easily in the same way as other integrated-circuit temperature sensors, and its remote diode sensing capability allows it to be used in new ways as well. It can be soldered to a printed circuit board, and because the path of best thermal conductivity is between the die and the pins, its temperature will effectively be that of the printed circuit board lands and traces soldered to the LM83's pins. This presumes that the ambient air temperature is almost the same as the surface temperature of the printed circuit board; if the air temperature is much higher or lower than the surface temperature, the actual temperature of the of the LM83 die will be at an intermediate temperature between the surface and air temperatures. Again, the primary thermal conduction path is through the leads, so the circuit board temperature will contribute to the die temperature much more strongly than will the air temperature.

To measure temperature external to the LM83's die, use a remote diode. This diode can be located on the die of a target IC, allowing measurement of the IC's temperature, independent of the LM83's temperature. The LM83 has been optimized to measure the remote diode of a Pentium II processor as shown in *Figure 9*. A discrete diode can also be used to sense the temperature of external objects or ambient air. Remember that a discrete diode's temperature will be affected, and often dominated, by the temperature of its leads.



DS101058-15

Pentium or 3904 Temperature vs LM83 Temperature Reading

Most silicon diodes do not lend themselves well to this application. It is recommended that a 2N3904 transistor base emitter junction be used with the collector tied to the base.

A diode connected 2N3904 approximates the junction available on a Pentium microprocessor for temperature measurement. Therefore, the LM83 can sense the temperature of this diode effectively.

3.1 ACCURACY EFFECTS OF DIODE NON-IDEALITY FACTOR

The technique used in today's remote temperature sensors is to measure the change in V_{BE} at two different operating points of a diode. For a bias current ratio of $N:1$, this difference is given as:

$$\Delta V_{BE} = \eta \frac{kT}{q} \ln(N)$$

where:

- η is the non-ideality factor of the process the diode is manufactured on,
- q is the electron charge,
- k is the Boltzmann's constant,
- N is the current ratio,
- T is the absolute temperature in °K.

The temperature sensor then measures ΔV_{BE} and converts to digital data. In this equation, k and q are well defined universal constants, and N is a parameter controlled by the temperature sensor. The only other parameter is η , which depends on the diode that is used for measurement. Since ΔV_{BE} is proportional to both η and T , the variations in η cannot be distinguished from variations in temperature. Since the non-ideality factor is not controlled by the temperature sensor, it will directly add to the inaccuracy of the sensor. For the Pentium II Intel specifies a $\pm 1\%$ variation in η from part to part. As an example, assume a temperature sensor has an accuracy specification of $\pm 3^\circ\text{C}$ at room temperature of 25°C and the process used to manufacture the diode has a non-ideality variation of $\pm 1\%$. The resulting accuracy of the temperature sensor at room temperature will be:

$$T_{ACC} = \pm 3^\circ\text{C} + (\pm 1\% \text{ of } 298^\circ\text{K}) = \pm 6^\circ\text{C}.$$

The additional inaccuracy in the temperature measurement caused by η , can be eliminated if each temperature sensor is calibrated with the remote diode that it will be paired with.

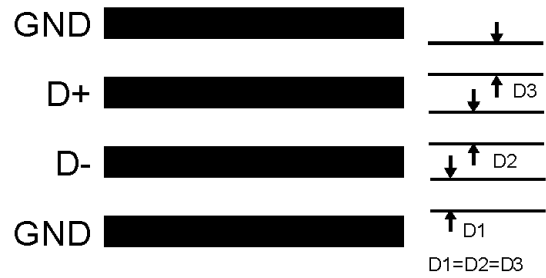
3.2 PCB LAYOUT for MINIMIZING NOISE

In a noisy environment, such as a processor mother board, layout considerations are very critical. Noise induced on traces running between the remote temperature diode sensor and the LM83 can cause temperature conversion errors. The following guidelines should be followed:

1. Place a $0.1 \mu\text{F}$ power supply bypass capacitor as close as possible to the V_{CC} pin and the recommended 2.2 nF capacitor as close as possible to the D+ and D- pins. Make sure the traces to the 2.2 nF capacitor are matched.
2. The recommended 2.2 nF diode bypass capacitor actually has a range of 200 pF to 3.3 nF . The average temperature accuracy will not degrade. Increasing the capacitance will lower the corner frequency where differential noise error affects the temperature reading thus producing a reading that is more stable. Conversely, lowering the capacitance will increase the corner frequency where differential noise error affects the temperature reading thus producing a reading that is less stable.
3. Ideally, the LM83 should be placed within 10 cm of the Processor diode pins with the traces being as straight, short and identical as possible. Trace resistance of 1Ω can cause as much as 1°C of error.
4. Diode traces should be surrounded by a GND guard ring to either side, above and below if possible. This GND guard should not be between the D+ and D- lines. In the event that noise does couple to the diode lines it would be ideal if it is coupled common mode. That is equally to the D+ and D- lines. (See *Figure 10*)
5. Avoid routing diode traces in close proximity to power supply switching or filtering inductors.

4.0 Application Hints (Continued)

6. Avoid running diode traces close to or parallel to high speed digital and bus lines. Diode traces should be kept at least 2cm. apart from the high speed digital traces.
7. If it is necessary to cross high speed digital traces, the diode traces and the high speed digital traces should cross at a 90 degree angle.
8. The ideal place to connect the LM83's GND pin is as close as possible to the Processors GND associated with the sense diode. For the Pentium II this would be pin A14.
9. Leakage current between D+ and GND should be kept to a minimum. One nano-ampere of leakage can cause as much as 1°C of error in the diode temperature reading. Keeping the printed circuit board as clean as possible will minimize leakage current.

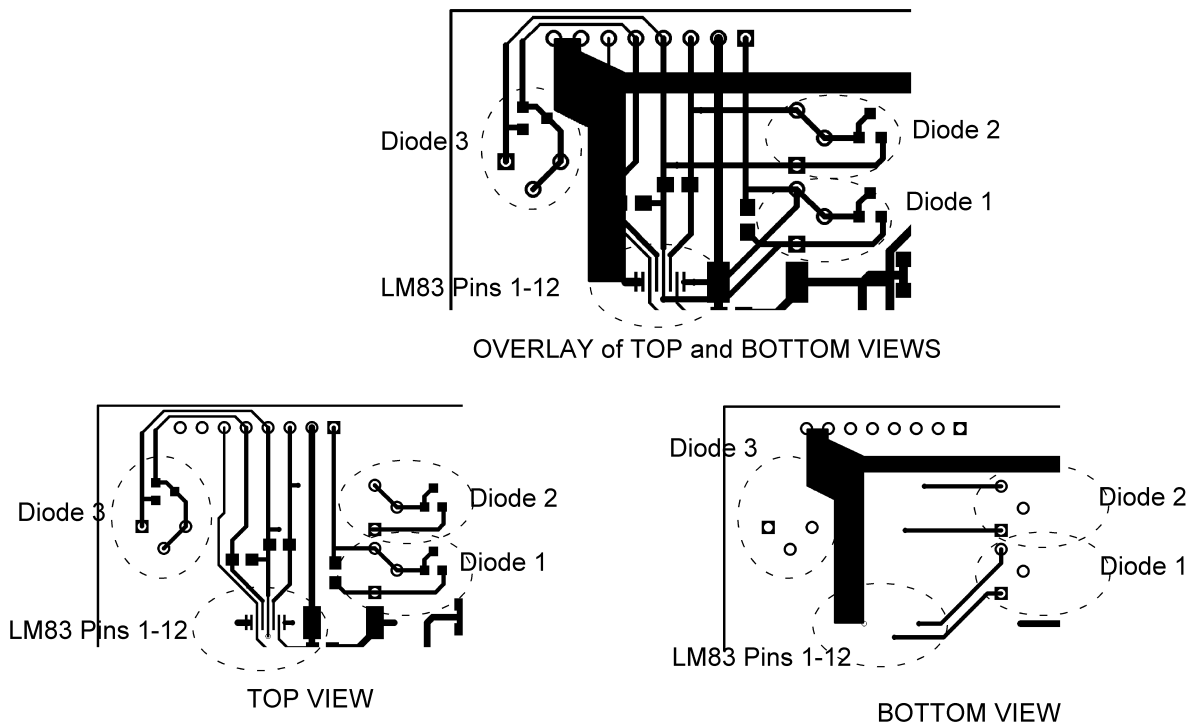


DS101058-17

FIGURE 10. Ideal Diode Trace Layout

Noise coupling into the digital lines greater than 300mVp-p (typical hysteresis), overshoot greater than 500mV above V_{CC} , and undershoot less than 500mV below GND, may prevent successful SMBus communication with the LM83. SMBus no acknowledge is the most common symptom, causing unnecessary traffic on the bus. Although, the SMBus maximum frequency of communication is rather low (100kHz max) care still needs to be taken to ensure proper termination within a system with multiple parts on the bus and long printed circuit board traces. An R/C lowpass filter with a 3db corner frequency of about 40MHz has been included on the LM83's SMBCLK input. Additional resistance can be added in series with the SMBData and SMBCLK lines to further help filter noise and ringing. Minimize noise coupling by keeping digital traces out of switching power supply areas as well as ensuring that digital lines containing high speed data communications cross at right angles to the SMBData and SMBCLK lines.

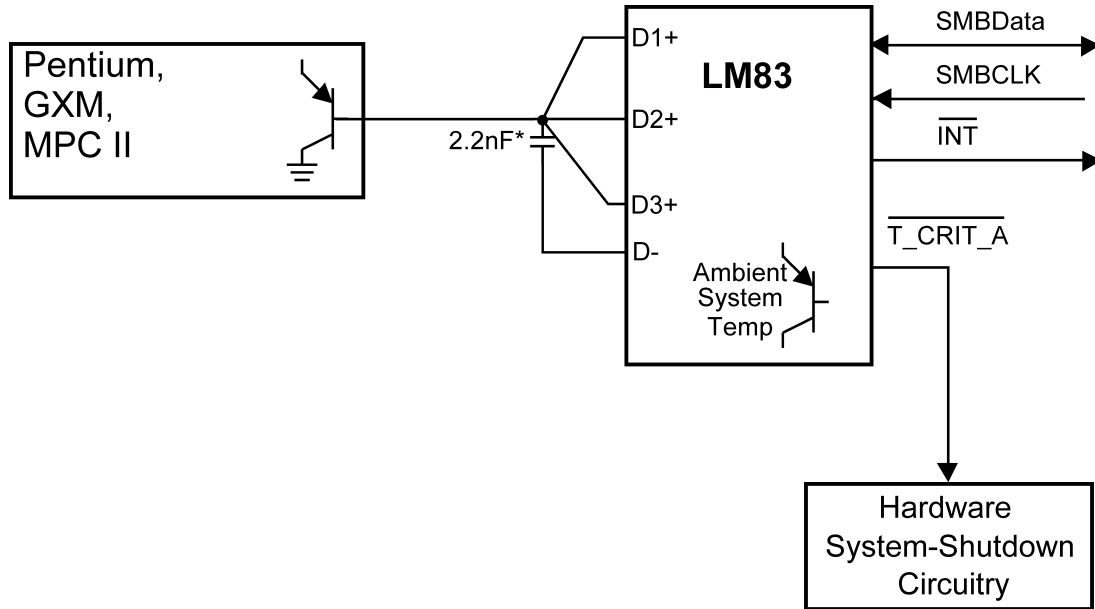
4.0 Typical Applications



DS101058-22

FIGURE 11. LM83 Demo Board Diode Layout

4.0 Typical Applications (Continued)



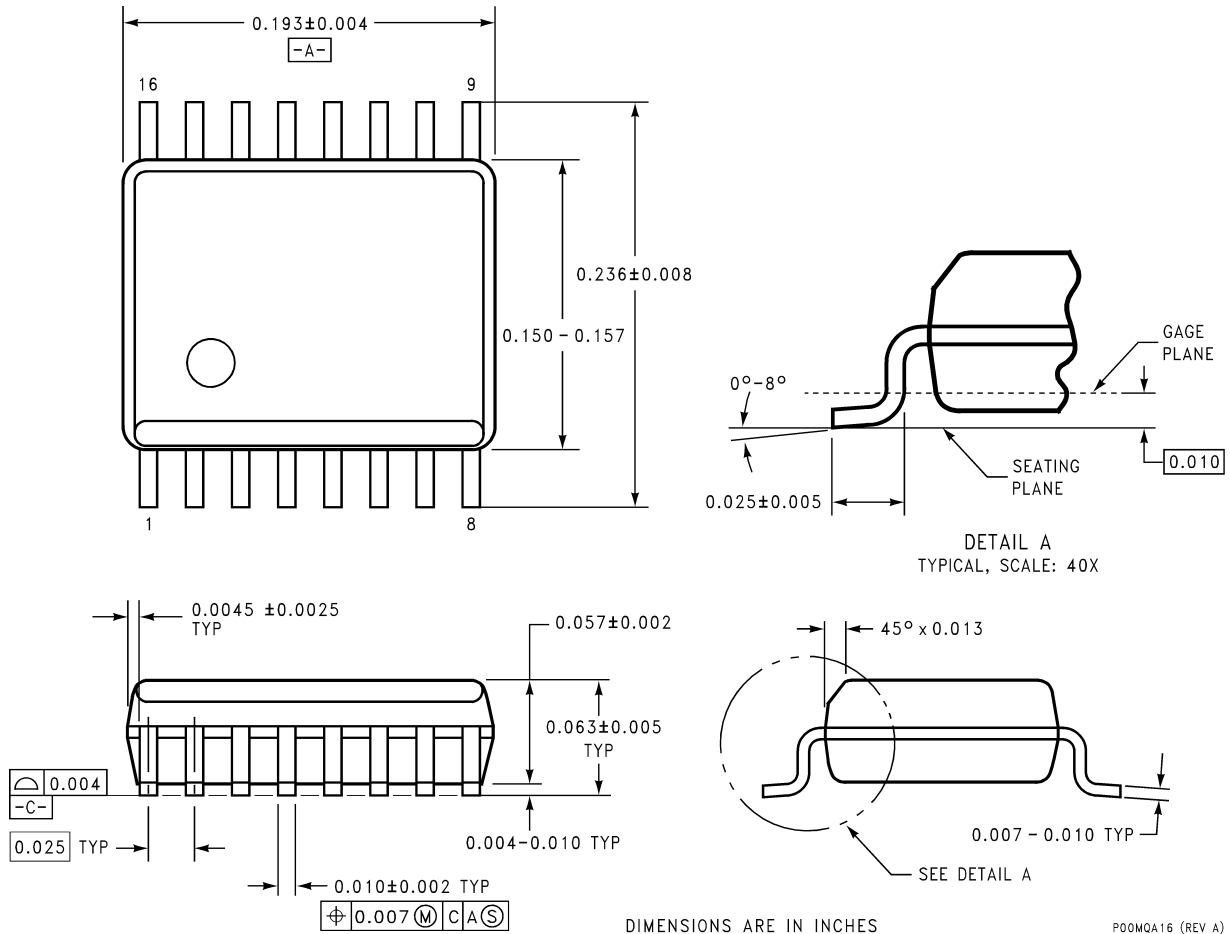
*Note: 2.2nF Capacitor must be placed as close as possible to D+ and D- pins of the LM83.

DS101058-23

Any two or three D+ inputs can be connected in parallel to increase the number of High temperature setpoints for a particular temperature reading. If all three D+ inputs are tied as shown here, D1+, D2+ and D3+ temperature readings will be identical, unless affected by PCB D+ trace resistance differences.

FIGURE 12. Connecting all Three LM83 Diode Inputs in Parallel will Increase the Number of HIGH Setpoints for a Single Temperature Reading to Three.

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead QSOP Package
Order Number LM83CIMQA or LM83CIMQAX
NS Package Number MQA16

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

 **National Semiconductor Corporation**
 Americas
 Tel: 1-800-272-9959
 Fax: 1-800-737-7018
 Email: support@nsc.com
 www.national.com

National Semiconductor Europe
 Fax: +49 (0) 180-530 85 86
 Email: europe.support@nsc.com
 Deutsch Tel: +49 (0) 69 9508 6208
 English Tel: +44 (0) 870 24 0 2171
 Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Response Group
 Tel: 65-2544466
 Fax: 65-2504466
 Email: ap.support@nsc.com

National Semiconductor Japan Ltd.
 Tel: 81-3-5639-7560
 Fax: 81-3-5639-7507

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Mobile Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Transportation and Automotive	www.ti.com/automotive
Video and Imaging	www.ti.com/video

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2011, Texas Instruments Incorporated







Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View LM83CIMQAX/NOPB](#) on WIN SOURCE

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management