THE DATASHEET OF

LM95235DIMM/NOPB

www.win-source.net 0086-755-83957316

Precision Remote Diode Temperature Sensor with SMBus Interface and TruTherm™ Technology

Check for Samples: LM95235, LM95235-Q1

FEATURES

- **Remote and Local Temperature Channels**
- **TruTherm BJT Beta Compensation Technology**
- **LM95235Q is AEC-Q100 Grade 3 Compliant and is Manufactured on an Automotive Grade Flow**
- **Diode Model Selection Bit - MMBT3904 or 65/90-nm Processor Diodes**
- **Two Formats: -128°C to 127.875°C and 0°C to 255.875°C**
- **Digital Filter for Remote Channel**
- **Programmable TCRIT and OS Thresholds**
- **Programmable Shared Hysteresis Register**
- **Diode Fault Detection**
- **Mask, Offset, and Status Registers**
- **SMBus 2.0 Compatible Interface, Supports TIMEOUT**
- **Programmable Conversion Rate for Best Power Consumption**
- **Three-Level Address Pin**
- **Standby Mode One-Shot Conversion Control**
- **Pin-for-Pin Compatible With the LM86 and LM89**
- **8-Pin VSSOP Package**

APPLICATIONS

- **Processor/Computer System Thermal Management (For Example, Laptops, Desktops, Workstations, Servers)**
- **Electronic Test Equipment and Office Electronics**

KEY SPECIFICATIONS

- **Supply Voltage 3.0 to 3.6 V**
- **Supply Current, Conv. Rate = 1 Hz 350 µA (typ)**
- **Remote Diode Temperature Accuracy**
  - **T_A = 25°C to 85°C; T_D = 60°C to 100°C, ±0.75 °C (max)**
  - **T_A = 25°C to 90°C; T_D = 40°C to 125°C, ±1.5 °C (max)**
- **Local Temperature Accuracy**
  - **T_A = 25°C to 100°C, ±2.0 °C (max)**
- **Conversion Rate, Both Channels 16 to 0.4 Hz**

DESCRIPTION

The LM95235 is an 11-bit digital temperature sensor with a 2-wire System Management Bus (SMBus) interface and TruTherm technology that can monitor the temperature of a remote diode as well as its own temperature. The LM95235 can be used to very accurately monitor the temperature of external devices such as microprocessors, graphics processors, or a diode-connected MMBT3904 transistor. For automotive applications the LM95235Q is available that is AEC-Q100 Grade3 compliant and is manufactured on an Automotive Grade Flow. TruTherm BJT (transistor) beta compensation technology allows the LM95235 to precisely monitor thermal diodes found in 90 nm and smaller geometry processes. LM95235 reports temperature in two different formats for +127.875°C/-128°C range and 0°C/255°C range. The LM95235 T_CRIT and OS outputs are asserted when either unmasked channel exceeds its programmed limit and can be used to shutdown the system, to turn on the system fans, or as a microcontroller interrupt function. The current status of the T_CRIT and OS pins can be read back from the status registers via the SMBus interface. All limits have a shared programmable hysteresis register.

The remote temperature channel of the LM95235 has a programmable digital filter. The LM95235 contains a diode model selection bit to select between a typical Intel® processor on a 65 nm or 90 nm process or MMBT3904, as well as an offset register for maximum flexibility and best accuracy.

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DESCRIPTION (CONTINUED)

The LM95235 has a three-level address pin to connect up to 3 devices to the same SMBus master, that is shared with the $\overline{OS}$ output. The LM95235 has a programmable conversion rate register and a standby mode to save power. One conversion can be triggered in standby mode by writing to the one-shot register.

Connection Diagram

Top View

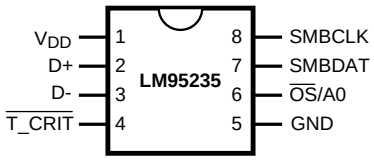

Figure 1. VSSOP-8 Package
See package number DGK0008A

Simplified Block Diagram

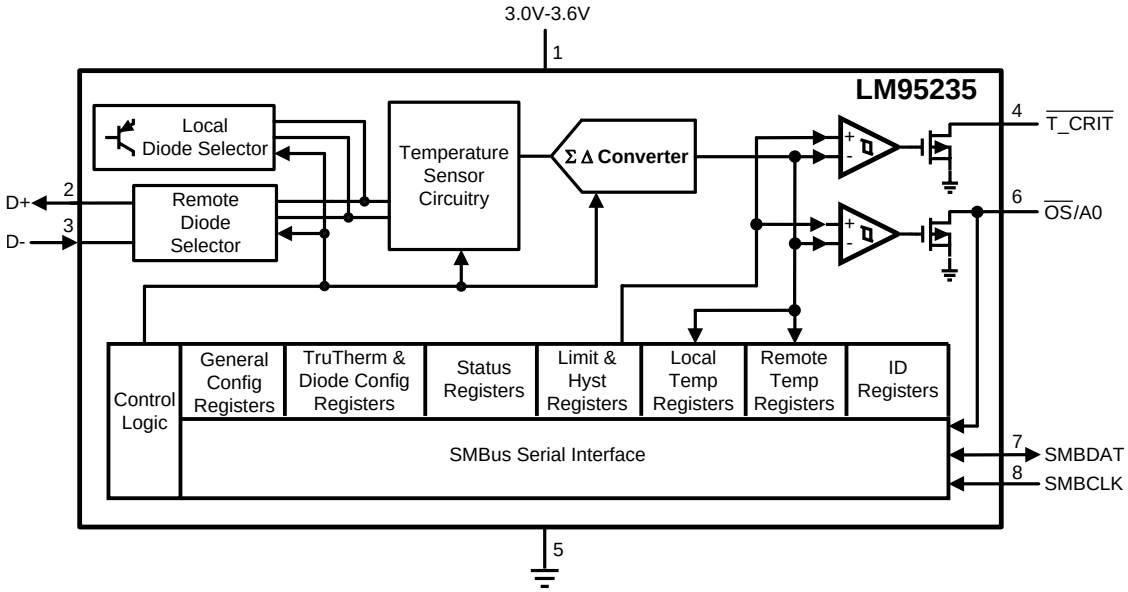

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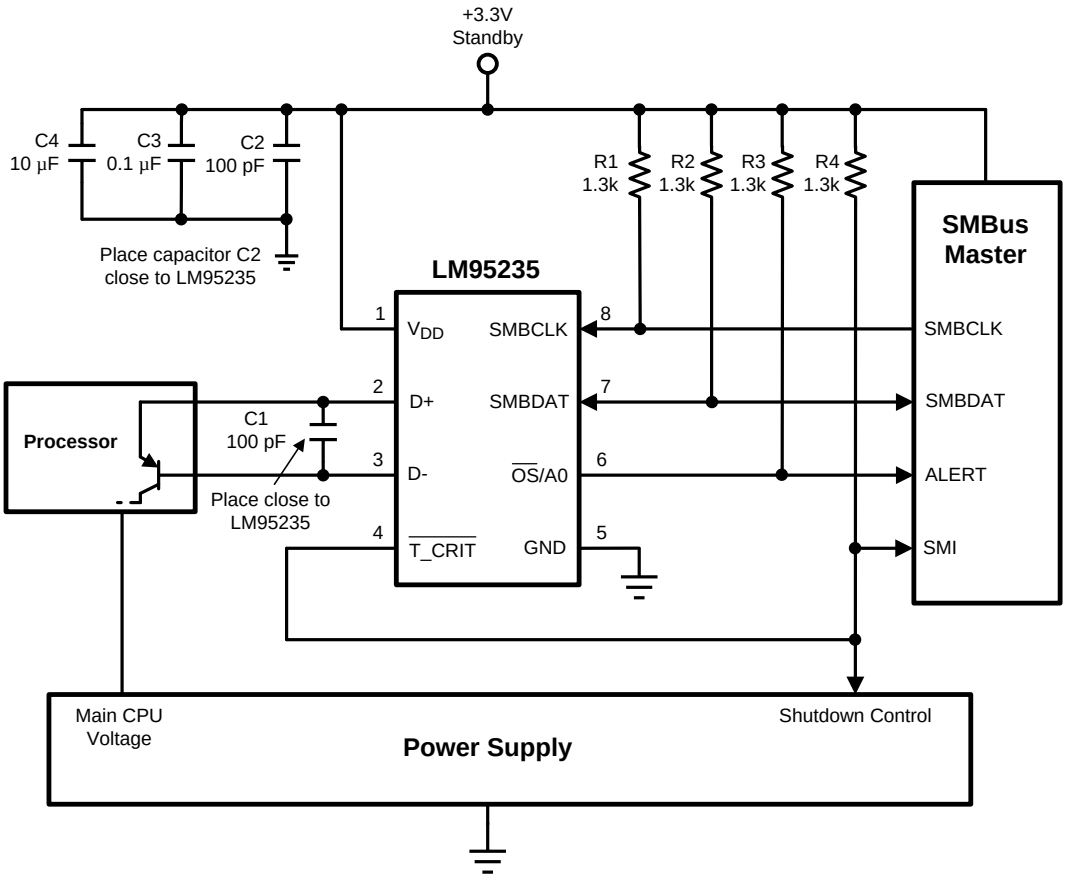
Table 1. Pin Descriptions

Pin Number	Name	Type	Description
1	V_{DD}	Power	Device power supply. Requires bypass capacitor of 10 µF in parallel with 0.1 µF and 100 pF. Place 100 pF closest to device pin.
2	D+	Analog Input/Output	Positive input from the thermal diode.
3	D-	Analog Input/Output	Negative input from the thermal diode.
4	$\overline{T_CRIT}$	Digital Output	Critical temperature output. Open-drain output requires pull-up resistor. Active low.
5	GND	Ground	Device ground.
6	$\overline{OS}$/A0	Digital Input/Output	Over-temperature shutdown comparator output or SMBus slave address input. Defaults as an SMBus slave address input that selects one of three addresses. Can be tied to V_{DD}, GND, or to the middle of a resistor divider connected between V_{DD} and GND. When programmed as an $\overline{OS}$ comparator output it is active low and open drain.
7	SMBDAT	Digital Input/Output	SMBus interface data pin. Open-drain output requires pull-up resistor.
8	SMBCLK	Digital Input	SMBus interface clock pin.

Typical Application



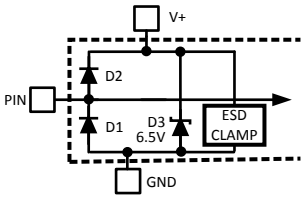
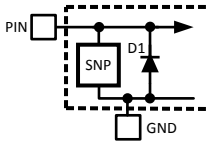
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

Supply Voltage, V_{DD}		-0.3V to 6.0V
Voltage at SMBDAT, SMBCLK, $\overline{T_CRIT}$, $\overline{OS}$/A0 Pins		-0.5V to 6.0V
Voltage at Other Pins		(V_{DD} +0.3V)
Input Current at D- Pin (2)		±1 mA
Input Current at All Other Pins(2)		±5 mA
Output Sink Current, SMBDAT, $\overline{T_Crit}$, $\overline{OS}$ Pins		10 mA
Package Input Current (2)		30 mA
ESD Susceptibility(3)	Human Body Model	2500V
	Machine Model	250V
	Charged Device Model	1000V
Junction Temperature(4)		+125°C
Storage Temperature		-65°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is guaranteed to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.
(2) When the input voltage (V_I) at any pin exceeds the power supplies (V_I < GND or V_I > V_{DD}), the current at that pin should be limited to 5 mA. Parasitic components and or ESD protection circuitry are shown in the figures in Table 2 for the LM95235's pins. Care should be taken not to forward bias the parasitic diodes on pins 2 and 3. Doing so by more than 50 mV may corrupt the temperature measurements. SNP refers to Snap-back device.
(3) Human body model (HBM) is a charged 100 pF capacitor discharged into a 1.5 kΩ resistor. Machine model (MM), is a charged 200 pF capacitor discharged directly into each pin. Charged Device Model (CDM) simulates a pin slowly acquiring charge (such as from a device sliding down the feeder in an automated assembler) then rapidly being discharged.
(4) Thermal resistance junction-to-ambient when attached to a printed circuit board with 1 oz. foil and no airflow is: θ_{JA} for VSSOP-8 package = 210°C/W

Table 2. ESD Protection

Pin No.	Label	Circuit	Pin ESD Protection Structure Circuits
1	V_{DD}	A	 Circuit A
2	D+	A	
3	D-	A	
4	$\overline{T_CRIT}$	B	
5	GND	A	
6	$\overline{OS}$/A0	B	 Circuit B
7	SMBDAT	B	
8	SMBCLK	B	

Operating Ratings (1)

Operating Temperature Range		-40°C to +125°C
Electrical Characteristics Temperature Range, $T_{MIN} \le T_A \le T_{MAX}$	LM95235CIMM	0°C ≤ T_A ≤ +90°C
	LM95235DIMM	-40°C ≤ T_A ≤ +90°C
	LM95235EIMM	-40°C ≤ T_A ≤ +90°C
	LM95235QEIMM	-40°C ≤ T_A ≤ +85°C
Supply Voltage (V_{DD})		+3.0V to +3.6V
Soldering process must comply with Reflow Temperature Profile specifications. Refer to http://www.ti.com/packaging. (2)		

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is guaranteed to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.
(2) Reflow temperature profiles are different for packages containing lead (Pb) than for those that do not.

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Temperature-to-Digital Converter Characteristics

Unless otherwise noted, these specifications apply for V_{DD} = +3.0 Vdc to 3.6 Vdc. **Boldface limits apply for $T_A = T_J = T_{MIN} \leq T_A \leq T_{MAX}$;** all other limits $T_A = T_J$ = +25°C, unless otherwise noted. T_J is the junction temperature of the LM95235. T_A is the ambient temperature of the LM95235. T_D is the junction temperature of the remote thermal diode.

Parameter	Test Conditions		Typical (1)	LM95235 CIMM Limits (2)	LM95235 DIMM Limits (2)	LM95235 EIMM LM95235 QEIMM Limits (2)	Unit
Temperature Accuracy Using Local Diode(3)	T_A = 25°C to +100°C		±1	**±2**	**±2**	**±2**	°C (max)
	T_A = -40°C to +25°C				**±6.0**	**±6.0**	°C (max)
Temperature Accuracy Using Remote Diode(4)	T_A = +25°C to +85°C; T_D = +60°C to +100°C	65nm Intel Processor	±0.5	**±0.75**	**±0.75**	**±0.75**	°C (max)
	T_A = +25°C to T_{MAX}; T_D = +60°C to +100°C	MMBT3904 or 65nm Intel Processor	±0.5	**±1.0**	**±1.0**	**±1.0**	°C (max)
	T_A = +25°C to T_{MAX}; T_D = +40°C to +120°C	MMBT3904 or 65nm Intel Processor	±0.75	**±1.5**	**±1.5**	**±1.5**	°C (max)
	T_A = -40°C to +25°C; T_D = +25°C to +125°C	MMBT3904 or 65nm Intel Processor			**±3.0**		°C (max)
	T_A = -40°C to +25°C; T_D = +25°C to +125°C	MMBT3904				**±3.0**	°C (max)
	T_A = -40°C to +25°C; T_D = -40°C to +25°C	MMBT3904			**±5.0**	**±5.0**	°C (max)
Remote Diode Measurement Resolution	Digital Filter Off		11				Bits
			0.125				°C
	Digital Filter On		13				Bits
			0.03125				°C
Local Diode Measurement Resolution			11				Bits
			0.125				°C
Conversion Time, Fastest Setting (5)	Local and Remote Channels		63	**72**	**72**	**72**	ms (max)
	Local or Remote Channels		33				ms
Quiescent Current	SMBus Inactive, 1 Hz conversion rate(6)		350	**650**	**650**	**650**	µA (max)
	Standby Mode		300				µA
D- Source Voltage			400				mV
External Diode Current Source	High-level		172	**225**	**225**	**225**	µA (max)
	Low-level		10.75				µA
Diode Source Current Ratio			16				
Power-On Reset Voltage				**2.8**	**2.8**	**2.8**	V (max)
				1.6	**1.6**	**1.6**	V (min)
$\overline{T_CRIT}$ Pin Temperature Threshold	Default		+110				°C
$\overline{OS}$ Pin Temperature Threshold	Default		+85				°C

(1) Typical figures are at T_A = 25°C and represent most likely parametric norms at the time of product characterization. The typical specifications are not guaranteed.
(2) Limits are guaranteed to TI's AOQL (Average Outgoing Quality Level).
(3) Local temperature accuracy does not include the effects of self-heating. The rise in temperature due to self-heating is the product of the internal power dissipation of the LM95235 and the thermal resistance. See () for the thermal resistance to be used in the self-heating calculation.
(4) The accuracy of the LM95235 is guaranteed when using a typical thermal diode of an Intel processor on a 65 nm process or an MMBT3904 diode-connected transistor, as selected in the Remote Diode Model Select register. See typical performance curve for performance with Intel processor on a 90nm process.
(5) This specification is provided only to indicate how often temperature data is updated. The LM95235 can be read at any time without regard to conversion state (and will yield last conversion result).
(6) Quiescent current will not increase substantially when the SMBus is active.

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Logic Electrical Characteristics

Digital DC Characteristics

Unless otherwise noted, these specifications apply for V_{DD}= +3.0 Vdc to 3.6 Vdc. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$= +25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	Typical (1)	Limits (2)	Unit (Limit)
SMBDAT, SMBCLK INPUTS					
$V_{IN(1)}$	Logical “1” Input Voltage			**2.1**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage			**0.8**	V (max)
$V_{IN(HYST)}$	SMBDAT and SMBCLK Digital Input Hysteresis		400		mV
$I_{IN(1)}$	Logical “1” Input Current	$V_{IN} = V_{DD}$	-0.005	**-10**	µA (max)
$I_{IN(0)}$	Logical “0” Input Current	V_{IN} = 0 V	0.005	**+10**	µA (max)
C_{IN}	Input Capacitance		5		pF
A0 DIGITAL INPUT					
V_{IH}	Input High Voltage			**0.90 × V_{DD}**	V (min)
V_{IM}	Input Middle Voltage			**0.57 × V_{DD}**	V (max)
				0.43 × V_{DD}	V (min)
V_{IL}	Input Low Voltage			**0.10 × V_{DD}**	V (max)
$I_{IN(1)}$	Logical “1” Input Current	$V_{IN} = V_{DD}$	-0.005	**-10**	µA (max)
$I_{IN(0)}$	Logical “0” Input Current	V_{IN} = 0 V	0.005	**+10**	µA (max)
C_{IN}	Input Capacitance		5		pF
SMBDAT, $\overline{T_CRIT}$, $\overline{OS}$ DIGITAL OUTPUTS					
I_{OH}	High Level Output Leakage Current	$V_{OUT} = V_{DD}$		**10**	µA (max)
$V_{OL(\overline{T_CRIT}, \overline{OS})}$	$\overline{T_CRIT}$, $\overline{OS}$ Low Level Output Voltage	I_{OL} = 6 mA		**0.4**	V (max)
$V_{OL(SMBDAT)}$	SMBDAT Low Level Output Voltage	I_{OL} = 4 mA I_{OL} = 6 mA		**0.4** **0.6**	V (max) V (max)
C_{OUT}	Digital Output Capacitance		5		pF

(1) Typical figures are at T_A = 25°C and represent most likely parametric norms at the time of product characterization. The typical specifications are not guaranteed.
(2) Limits are guaranteed to TI's AOQL (Average Outgoing Quality Level).

SMBus Digital Switching Characteristics

Unless otherwise noted, these specifications apply for V_{DD}= +3.0 Vdc to +3.6 Vdc, C_L (load capacitance) on output lines = 80 pF. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = +25°C, unless otherwise noted.
The switching characteristics of the LM95235 fully meet or exceed the published specifications of the SMBus version 2.0. The following parameters are the timing relationships between SMBCLK and SMBDAT signals related to the LM95235. They adhere to, but are not necessarily, the SMBus specifications.

Parameter		Test Conditions	Typical	Limits	Unit
			(1)	(2)	(Limit)
f_{SMB}	SMBus Clock Frequency			**100** **10**	kHz (max) kHz (min)
t_{LOW}	SMBus Clock Low Time	from $V_{IN(0)}$max to $V_{IN(0)}$max		**4.7** **25**	µs (min) ms (max)
t_{HIGH}	SMBus Clock High Time	from $V_{IN(1)}$min to $V_{IN(1)}$min		**4.0**	µs (min)
$t_{R,SMB}$	SMBus Rise Time	(3)	1		µs (max)
$t_{F,SMB}$	SMBus Fall Time	(4)	0.3		µs (max)

(1) Typical figures are at T_A = 25°C and represent most likely parametric norms at the time of product characterization. The typical specifications are not guaranteed.
(2) Limits are guaranteed to TI's AOQL (Average Outgoing Quality Level).
(3) The output rise time is measured from ($V_{IN(0)}$max - 0.15V) to ($V_{IN(1)}$min + 0.15V).
(4) The output fall time is measured from ($V_{IN(1)}$min + 0.15V) to ($V_{IN(0)}$max - 0.15V).

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SMBus Digital Switching Characteristics (continued)

Unless otherwise noted, these specifications apply for V_{DD}= +3.0 Vdc to +3.6 Vdc, C_L (load capacitance) on output lines = 80 pF. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = +25°C, unless otherwise noted.
The switching characteristics of the LM95235 fully meet or exceed the published specifications of the SMBus version 2.0. The following parameters are the timing relationships between SMBCLK and SMBDAT signals related to the LM95235. They adhere to, but are not necessarily, the SMBus specifications.

Parameter		Test Conditions	Typical	Limits	Unit
			(1)	(2)	(Limit)
t_{OF}	Output Fall Time	C_L = 400 pF, I_O = 3 mA, (4)		**250**	ns (max)
$t_{TIMEOUT}$	SMBDAT and SMBCLK Time Low for Reset of Serial Interface (5)			**25** **35**	ms (min) ms (max)
$t_{SU;DAT}$	Data In Setup Time to SMBCLK High			**250**	ns (min)
$t_{HD;DAT}$	Data Out Stable after SMBCLK Low			**300** **1075**	ns (min) ns (max)
$t_{HD;STA}$	Start Condition SMBDAT Low to SMBCLK Low (Start condition hold before the first clock falling edge)			**100**	ns (min)
$t_{SU;STO}$	Stop Condition SMBCLK High to SMBDAT Low (Stop Condition Setup)			**100**	ns (min)
$t_{SU;STA}$	SMBus Repeated Start-Condition Setup Time, SMBCLK High to SMBDAT Low			**0.6**	µs (min)
t_{BUF}	SMBus Free Time Between Stop and Start Conditions			**1.3**	µs (min)

(5) Holding the SMBDAT and/or SMBCLK lines Low for a time interval greater than $t_{TIMEOUT}$ will reset the LM95235's SMBus state machine, therefore setting SMBDAT and SMBCLK pins to a high impedance state.

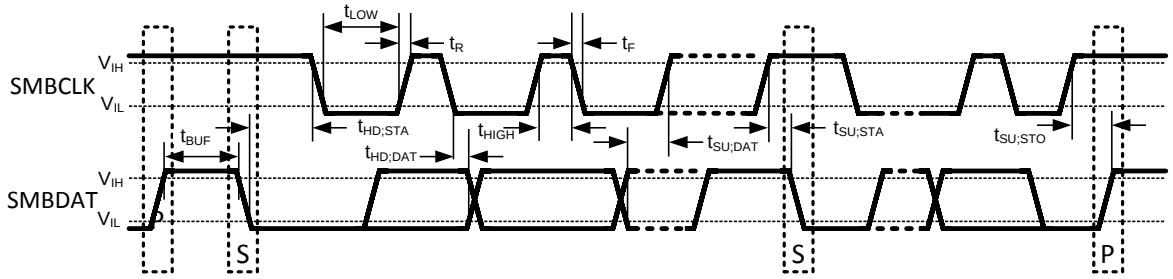

Figure 2. SMBus Communication

Typical Performance Characteristics

Thermal Diode Capacitor or PCB Leakage Current Effect Remote Diode Temperature Reading

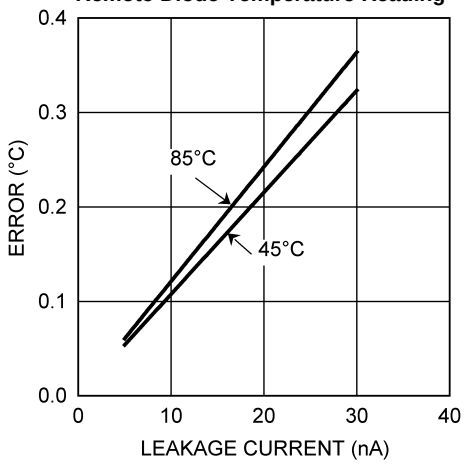

Figure 3.

Remote Temperature Reading Sensitivity to Thermal Diode Filter Capacitance, TruTherm Enabled

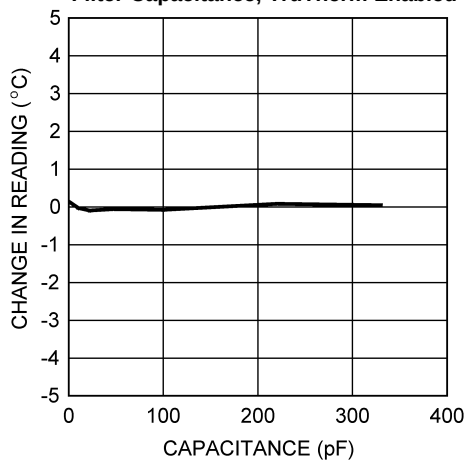

Figure 4.

Conversion Rate Effect on Average Power Supply Current

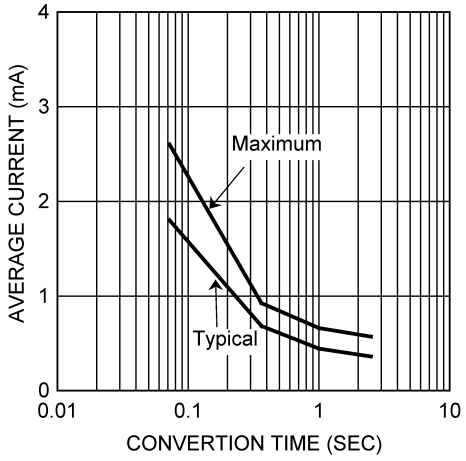

Figure 5.

Intel Processor on 65nm Process or 90nm Process Thermal Diode Performance Comparison

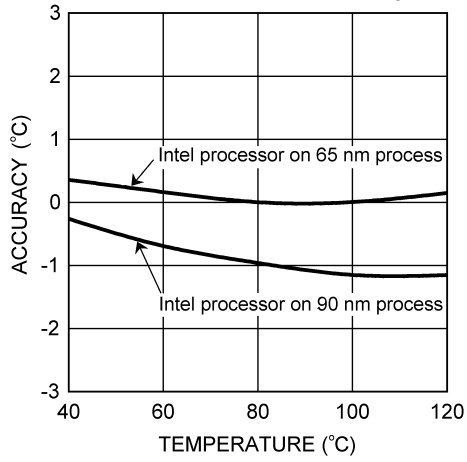

Figure 6. n

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FUNCTIONAL DESCRIPTION

The LM95235 is a temperature sensor that measures Local and Remote temperature zones. The LM95235 uses a ΔV_{be} temperature sensing method. A differential voltage, representing temperature, is digitized using a Sigma-Delta analog to digital converter. TruTherm Technology allows the LM95235 to accurately sense the temperature of a thermal diode found on die fabricated using a sub-micron process. For more information on TruTherm Technology see Applications Hints . The LM95235 is compatible with the serial SMBus version 2.0 two-wire serial interface.

The LM95235 has $\overline{OS}$ and $\overline{TCRIT}$ open-drain digital outputs that indicate the state of the local and remote temperature readings when compared to user-programmable limits. If enabled, the local temperature is compared to the user-programmable Local Shared OS and TCRIT Limit Register (Default Value = 85°C). The comparison result can trigger the $\overline{T_CRIT}$ pin and/or the $\overline{OS}$ pin depending on the settings of the Local TCRIT Mask and OS Mask bits found in Configuration Register 1. The comparison result can also be read back from Status Register 1. If enabled, the remote temperature is compared to the user-programmable Remote TCRIT Limit Register (Default Value = 110°C), and the Remote OS Limit Register (Default Value = 85°C) values. The comparison result can trigger the $\overline{T_CRIT}$ pin and/or the $\overline{OS}$ pin depending on the settings of Configuration Register 1. The following table describes the default temperature settings for each measured temperature that triggers $\overline{T_CRIT}$ and/or $\overline{OS}$ pins:

Output Pin	Remote,°C	Local,°C
$\overline{T_CRIT}$	110	85
$\overline{OS}$	85	85

The following table describes the limit register mapping to the $\overline{T_CRIT}$ and/or $\overline{OS}$ pins:

Output Pin	Remote	Local
$\overline{T_CRIT}$	Remote TCRIT Limit	Local Shared OS/TCRIT Limit
$\overline{OS}$	Remote OS Limit	Local Shared OS/TCRIT Limit

The $\overline{T_CRIT}$ and $\overline{OS}$ outputs are open-drain, active low.

The remote temperature readings support a programmable digital filter. Based on the settings in Configuration Register 2 a digital filter can be turned on to improve the noise performance of the remote temperature as well as to increase the resolution of the temperature reading. If the filter is enabled the filtered readings are used for TCRIT and OS comparisons. The LM95235 may be placed in low power consumption (Standby) mode by setting the STOP/$\overline{RUN}$ bit found in Configuration Register 1. In the Standby mode, the LM95235's SMBus interface remains active while all circuitry not required is turned off. In the Standby mode the host can trigger one round of conversions by writing to the One-Shot Register. The value written into this register is not kept. Local and Remote temperatures will be converted once and the $\overline{T_CRIT}$ and $\overline{OS}$ pins will reflect the comparison results based on this set of conversions results.

All the temperature readings are in 16-bit left-justified word format. The 10-bit plus sign local temperature reading is contained in two 8-bit registers: Local Temp MSB and Local Temp LSB Registers. The remote temperature supports both a 13-bit unsigned and a 12-bit plus sign format. These readings are available in their corresponding registers as described in the LM95235 Register table. The lower 2-bits of the remote temperature reading will contain temperature information only if the digital filter is enabled. If the digital filter is disabled, these two bits will read back 0.

The signed and unsigned remote temperature readings are available simultaneously in separate registers, therefore allowing both negative temperatures and temperatures 128°C and above to be measured.

All Limit Registers support unsigned temperature format with 1°C LSb resolution. The Local Shared TCRIT and OS Limit Register is 7 bits for limits between 0°C and 127°C. The Remote Temperature TCRIT and OS Limit Registers are 8 bits each for limits between 0°C and 255°C.

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CONVERSION SEQUENCE

In the power-up default state the LM95235 takes a maximum of 1 second to convert the Local Temperature, Remote Temperature, and to update all of its registers. Only during the conversion process is the Busy bit (D7) in Status Register 1 (02h) high. These conversions are addressed in a round-robin sequence. The conversion rate may be modified by the Conversion Rate bits found in the Conversion Rate Register (R/W: 04h/0Ah). When the conversion rate is modified a delay is inserted between conversions, the actual maximum conversion time remains at 72 ms. Different conversion rates will cause the LM95235 to draw different amounts of supply current as shown in Figure 7.

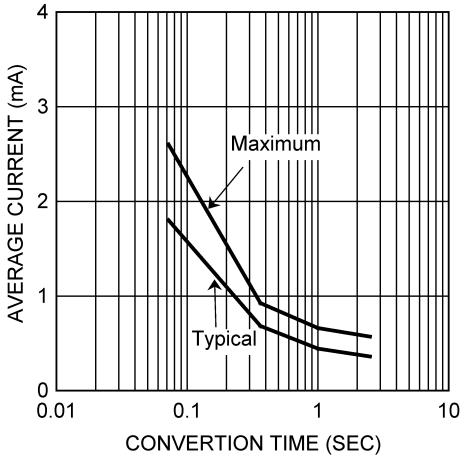

Figure 7. Conversion Rate Effect on Power Supply Current

POWER-ON-DEFAULT STATES

LM95235 always powers up to these known default states. The LM95235 remains in these states until after the first conversion.

1. Command Register set to 00h
2. Conversion Rate register defaults to 02h (1 second).
3. Local Temperature set to 0°C until the end of the first conversion
4. Remote Diode Temperature set to 0°C until the end of the first conversion
5. Remote OS limit default is 55h (85°C).
6. Local Shared and TCRIT limit default is 55h (85°C).
7. Remote TCRIT limit default is 6Eh (110°C).
8. Remote Offset High and Low bytes default to 00h.
9. Configuration Register 1 defaults to 00h. This sets the LM95235 as follows:
   (a) The STOP/$\overline{\text{RUN}}$ defaults to the active/converting mode.
   (b) The Local and Remote TCRIT and OS Masks are reset to 0.
10. Configuration Register 2 defaults to 1Fh. This sets the LM95235 as follows:
   (a) Remote Diode digital filter defaults on.
   (b) The Remote Diode mode defaults to a typical Intel processor on 65/90 nm process.
   (c) Diode Fault Mask bit for TCRIT defaults to 1.
   (d) Diode Fault Mask bit for OS defaults to 0.
   (e) Pin 6 Function defaults to Address Input function (A0).

SMBus INTERFACE

The LM95235 operates as a slave on the SMBus, so the SMBCLK line is an input and the SMBDAT line is bidirectional. The LM95235 never drives the SMBCLK line and it does not support clock stretching. According to SMBus specifications, the LM95235 has a 7-bit slave address. Three SMBus addresses can be selected by connecting pin 6 (A0) to either Low, Mid-Supply or High voltages. Table 3 shows the possible selections.

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Table 3. Address Selection

State of the A0 Pin	SMBus Device Address	
	HEX	Binary
Low	18	001 1000
Mid-Supply	29	010 1001
High	4C	100 1100

The $\overline{OS}$/A0 pin, after power-up, defaults as an address select input pin (A0). After power-up, the $\overline{OS}$/A0 pin can only be programmed as an OS output when it is in the "High" state. Therefore, 4Ch is the only valid slave address that can be used when the $\overline{OS}$/A0 pin is programmed to function as an $\overline{OS}$ output. When the $\overline{OS}$/A0 pin is programmed to function as an A0 input the LM95235 will immediately detect the state of this pin to determine its SMBus slave address. The LM95235 does not latch the state of the A0 pin when it is functioning as an input.

DIGITAL FILTER

In order to suppress erroneous remote temperature readings due to noise, the LM95235 incorporates a digital filter for the Remote Temperature Channel. The filter is accessed in the Configuration Register 2, bits D2 (FE1) and D1(FE0). The filter can be set according to the following table.

FE1	FE0	Filter Setting
0	0	Filter Off
0	1	Reserved
1	0	Reserved
1	1	Filter On

Figure 8 through Figure 10 depict the filter output in response to a step input and an impulse input.

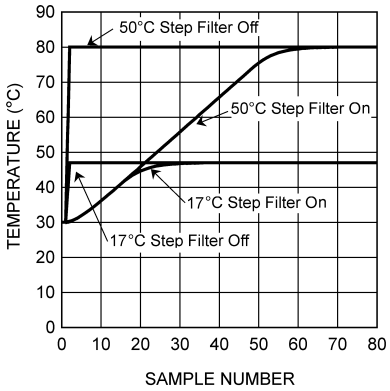


Figure 8. Filter Impulse and Step Response Curve Seventeen and Fifty Degree Step Response

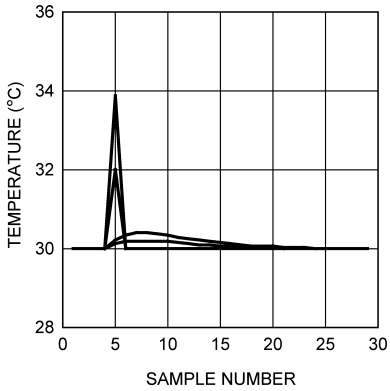


Figure 9. Filter Impulse and Step Response Curve Impulse Response with Input Transients Less Than 4°C

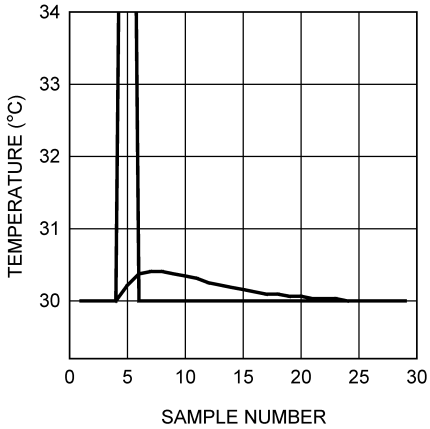
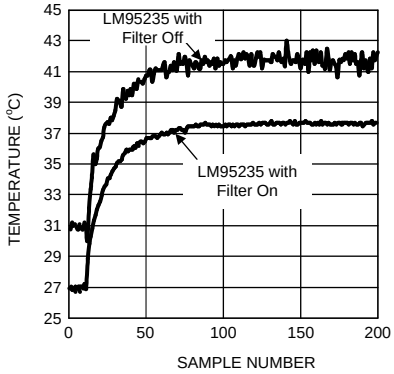


Figure 10. Filter Impulse and Step Response Curve
Impulse Response with Input Transients Greater Than 4°C

Figure 11 shows the filter in use in a typical Intel processor on a 65/90 nm process system. Note that the two curves have been purposely offset for clarity. Inserting the filter does not induce an offset as shown.



A. The filter curves were purposely offset for clarity.

Figure 11. Digital Filter Response in a Typical Intel Processor on a 65 nm or 90 nm Process

TEMPERATURE DATA FORMAT

Temperature data can only be read from the Local and Remote Temperature registers.

Remote temperature data with the digital filter off is represented by an 10-bit plus sign, two's complement word and 11-bit unsigned binary word with an LSb (Least Significant Bit) equal to 0.125°C. The data format is a left justified 16-bit word available in two 8-bit registers. Unused bits report "0".

Remote temperature data with the digital filter on is represented by a 12-bit plus sign, two's complement word and 13-bit unsigned binary word with an LSb (Least Significant Bit) equal to 0.03125°C (1/32°C). The data format is a left justified 16-bit word available in two 8-bit registers. Unused bits report "0".

Table 4. 11-Bit, 2's Complement (10-Bit Plus Sign)

Temperature	Digital Output	
	Binary	Hex
+125°C	0111 1101 0000 0000	7D00h
+25°C	0001 1001 0000 0000	1900h
+1°C	0000 0001 0000 0000	0100h
+0.125°C	0000 0000 0010 0000	0020h
0°C	0000 0000 0000 0000	0000h
-0.125°C	1111 1111 1110 0000	FFE0h

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Table 4. 11-Bit, 2's Complement (10-Bit Plus Sign) (continued)

Temperature	Digital Output	
	Binary	Hex
-1°C	1111 1111 0000 0000	FF00h
-25°C	1110 0111 0000 0000	E700h
-55°C	1100 1001 0000 0000	C900h

Table 5. 11-Bit, Unsigned Binary

Temperature	Digital Output	
	Binary	Hex
+255.875°C	1111 1111 1110 0000	FFE0h
+255°C	1111 1111 0000 0000	FF00h
+201°C	1100 1001 0000 0000	C900h
+125°C	0111 1101 0000 0000	7D00h
+25°C	0001 1001 0000 0000	1900h
+1°C	0000 0001 0000 0000	0100h
+0.125°C	0000 0000 0010 0000	0020h
0°C	0000 0000 0000 0000	0000h

Table 6. 13-Bit, 2's Complement (12-Bit Plus Sign)

Temperature	Digital Output	
	Binary	Hex
+125°C	0111 1101 0000 0000	7D00h
+25°C	0001 1001 0000 0000	1900h
+1°C	0000 0001 0000 0000	0100h
+0.03125°C	0000 0000 0000 1000	0008h
0°C	0000 0000 0000 0000	0000h
-0.03125°C	1111 1111 1111 1000	FFF8h
-1°C	1111 1111 0000 0000	FF00h
-25°C	1110 0111 0000 0000	E700h
-55°C	1100 1001 0000 0000	C900h

Table 7. 13-Bit, Unsigned Binary

Temperature	Digital Output	
	Binary	Hex
+255.875°C	1111 1111 1110 0000	FFE0h
+255°C	1111 1111 0000 0000	FF00h
+201°C	1100 1001 0000 0000	C900h
+125°C	0111 1101 0000 0000	7D00h
+25°C	0001 1001 0000 0000	1900h
+1°C	0000 0001 0000 0000	0100h
+0.03125°C	0000 0000 0000 1000	0008h
0°C	0000 0000 0000 0000	0000h

Local Temperature data is represented by a 10-bit plus sign, two's complement word with an LSb (Least Significant Bit) equal to 0.125°C. The data format is a left justified 16-bit word available in two 8-bit registers. Unused bits will always report "0". Local temperature readings greater than +127.875°C are clamped to +127.875°C, they will not roll-over to negative temperature readings.

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Table 8. 11-Bit, 2's Complement (10-Bit Plus Sign)

Temperature	Digital Output	
	Binary	Hex
+125°C	0111 1101 0000 0000	7D00h
+25°C	0001 1001 0000 0000	1900h
+1°C	0000 0001 0000 0000	0100h
+0.125°C	0000 0000 0010 0000	0020h
0°C	0000 0000 0000 0000	0000h
-0.125°C	1111 1111 1110 0000	FFE0h
-1°C	1111 1111 0000 0000	FF00h
-25°C	1110 0111 0000 0000	E700h
-55°C	1100 1001 0000 0000	C900h

SMBDAT OPEN-DRAIN OUTPUT

The SMBDAT output is an open-drain output and does not have internal pull-ups. A “high” level will not be observed on this pin until pull-up current is provided by some external source, typically a pull-up resistor. Choice of resistor value depends on many system factors but, in general, the pull-up resistor should be as large as possible without effecting the SMBus desired data rate. This will minimize any internal temperature reading errors due to internal heating of the LM95235. The maximum resistance of the pull-up to provide a 2.1V high level, based on LM95235 specification for High Level Output Current with the supply voltage at 3.0V, is 82 kΩ (5%) or 88.7 kΩ (1%).

$\overline{\text{T_CRIT}}$ OUTPUT AND TCRIT LIMIT

The LM95235's $\overline{\text{T_CRIT}}$ pin is an active-low open-drain output that is triggered when the local and/or the remote temperature conversion is above the limits defined by the Remote and/or Local Limit registers. The state of the $\overline{\text{T_CRIT}}$ pin will return to the HIGH state when both the Local and Remote temperatures are below the values programmed into the Limit Registers less the value in the Common Hysteresis Register. Additionally, if the remote temperature exceeds the value in the Remote TCRIT Limit Register the Status Bit for Remote TCRIT (RTCRIT), in Status Register 1, is set to 1. In the same way if the local temperature exceeds the value in the Local Shared OS and TCRIT Limit Register the Status Bit for the Shared Local OS and TCRIT (LOC) bit in Status Register 1 is set to 1.The $\overline{\text{T_CRIT}}$ output and the Status Register flags are updated after every Local and Remote temperature conversion. See Figure 12

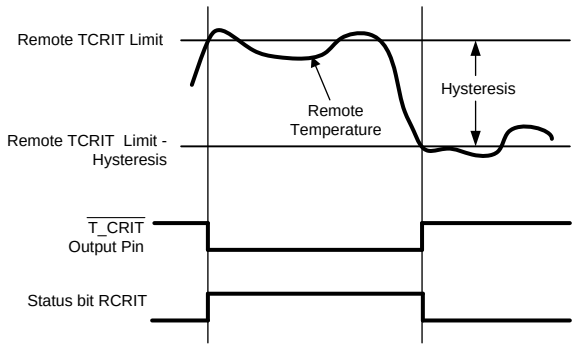

Figure 12. $\overline{\text{T_CRIT}}$ Comparator Temperature Response Diagram

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$\overline{OS}$ OUTPUT AND OS LIMIT

The LM95235's $\overline{OS}$/A0 pin is selected as an $\overline{OS}$ digital output as described in SMBus INTERFACE. As an $\overline{OS}$ pin, it is activated whenever the local and/or remote temperature conversion is above the limits defined by the Limit registers. If the remote temperature exceeds the value in the Remote OS Limit Register the Status Bit for Remote OS (ROS) in Status Register 1 is set to 1. In the same way if the local temperature exceeds the value in the Local Shared OS and TCRIT Limit Register the Status Bit for the Shared Local OS and TCRIT (LOC) bit in Status Register 1 is set to 1. The state of the $\overline{T_CRIT}$ pin output will return to the HIGH state when both the Local and Remote temperatures are below the values programmed into the Limit Registers less the value in the Common Hysteresis Register. The $\overline{OS}$ output and the Status Register flags are updated after every Local and Remote temperature conversion. See Figure 13.

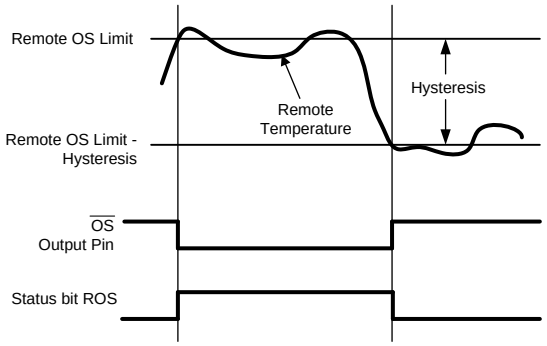

Figure 13. $\overline{OS}$ Temperature Response Diagram

DIODE FAULT DETECTION

The LM95235 is equipped with operational circuitry designed to detect fault conditions concerning the remote diodes. In the event that the D+ pin is detected as shorted to GND, D-, V_{DD} or D+ is floating, the Remote Temperature reading is –128.000°C if signed format is selected and +255.875°C if unsigned format is selected. In addition, the Status Register 1 bit D2 is set.

COMMUNICATING WITH THE LM95235

The data registers in the LM95235 are selected by the Command Register. At power-up the Command Register is set to “00”, the location for the Read Local Temperature Register. The Command Register latches the last location it was set to. Each data register in the LM95235 falls into one of four types of user accessibility:

1. Read only
2. Write only
3. Write/Read same address
4. Write/Read different address

A **Write** to the LM95235 will always include the address byte and the command byte. A write to any register requires one data byte.

Reading the LM95235 can take place either of two ways:

1. If the location latched in the Command Register is correct (most of the time it is expected that the Command Register will point to one of the Read Temperature Registers because that will be the data most frequently read from the LM95235), then the read can simply consist of an address byte, followed by retrieving the data byte.
2. If the Command Register needs to be set, then an address byte, command byte, repeat start, and another address byte will accomplish a read.

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The data byte has the most significant bit first. At the end of a read, the LM95235 can accept either acknowledge or No Acknowledge from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte). When retrieving all 11 bits from a previous remote diode temperature measurement, the master must insure that all 11 bits are from the same temperature conversion. This may be achieved by reading the MSB register first. The LSB will be locked after the MSB is read. The LSB will be unlocked after being read. If the user reads MSBs consecutively, each time the MSB is read, the LSB associated with that temperature will be locked in and override the previous LSB value locked-in.

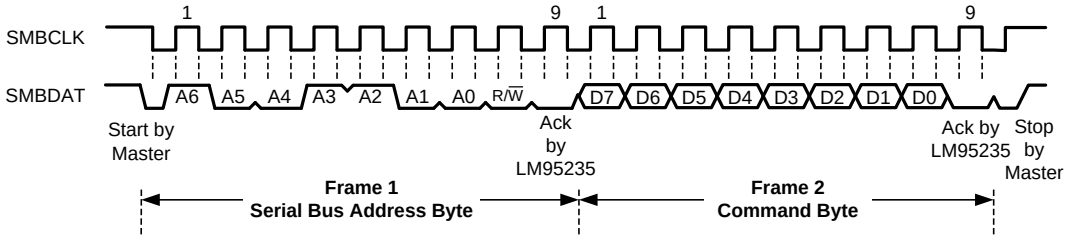

Figure 14. SMBus Timing Diagram for Access of Data (Default Address of 4Ch is shown)
(a) Serial Bus Write to the Internal Command Register

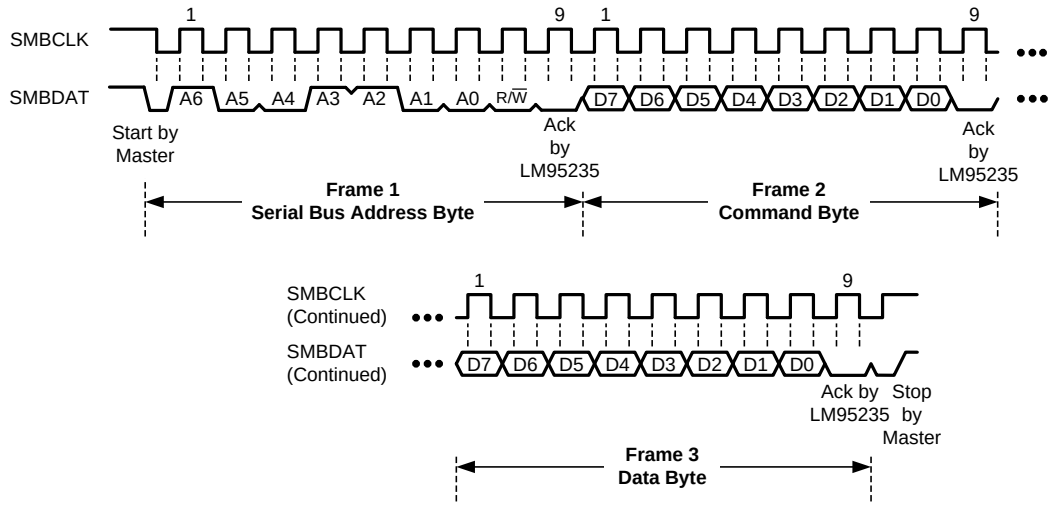

Figure 15. SMBus Timing Diagram for Access of Data (Default Address of 4Ch is shown)
(b) Serial Bus Write to the Internal Command Register Followed by a Data Byte

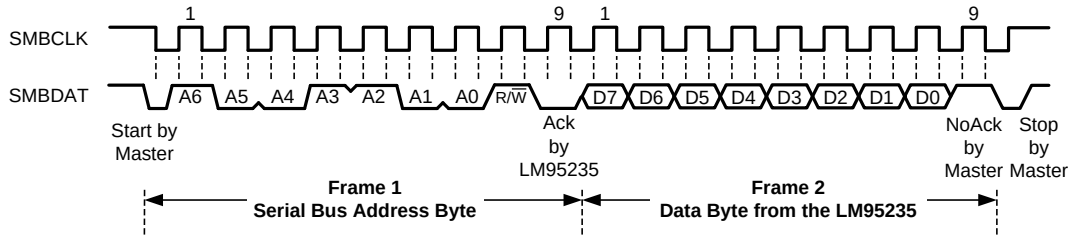

Figure 16. SMBus Timing Diagram for Access of Data (Default Address of 4Ch is shown)
(c) Serial Bus Byte Read from a Register with the Internal Command Register Preset to Desired Value

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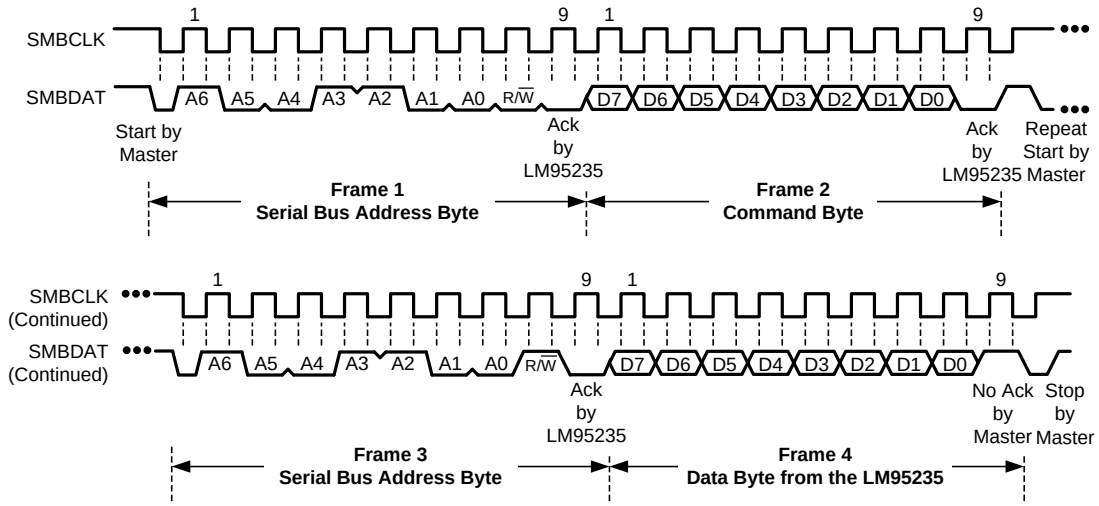

Figure 17. SMBus Timing Diagram for Access of Data (Default Address of 4Ch is shown)
(d) Serial Bus Write Followed by a Repeat Start and Immediate Read

SERIAL INTERFACE RESET

In the event that the SMBus Master is RESET while the LM95235 is transmitting on the SMBDAT line, the LM95235 must be returned to a known state in the communication protocol. This may be done in one of two ways:

1. When SMBDAT is LOW, the LM95235 SMBus state machine resets to the SMBus idle state if either SMBDAT or SMBCLK are held low for more than 35 ms ($t_{TIMEOUT}$). Note that according to SMBus specification 2.0 all devices are to timeout when either the SMBCLK or SMBDAT lines are held low for 25 - 35 ms. Therefore, to insure a timeout of all devices on the bus the SMBCLK or SMBDAT lines must be held low for at least 35 ms.
2. When SMBDAT is HIGH, have the master initiate an SMBus start. The LM95235 will respond properly to an SMBus start condition at any point during the communication. After the start the LM95235 will expect an SMBus Address address byte.

ONE-SHOT CONVERSION

The One-Shot register is used to initiate a single conversion and comparison cycle when the device is in standby mode, after which the device returns to standby. This is not a data register and it is the write operation that causes the one-shot conversion. The data written to this address is irrelevant and is not stored. A zero will always be read from this register.

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LM95235 REGISTERS

Command register selects which registers will be read from or written to. Data for this register should be transmitted during the Command Byte of the SMBus write communication. POR means Power-On Reset.

P0-P7: Command

P7	P6	P5	P4	P3	P2	P1	P0
Command							

Table 9. Register Summary

Register Name	Read Address (Hex)	Write Address (Hex)	No. of bits	POR Default (Hex)	Read/ Write	Description
TEMPERATURE SIGNED VALUE REGISTERS						
Local Temp MSB	0x00	NA	8	-	RO	Supports SMBus byte
Local Temp LSB	0x30	NA	3	-	RO	All unused bits are reported as "0".
Remote Temp MSB – Signed	0x01	NA	8	-	RO	Supports SMBus byte
Remote Temp LSB – Signed	0x10	NA	5/3	-	RO	All unused bits are reported as "0".
TEMPERATURE UNSIGNED VALUE REGISTERS						
Remote Temp MSB – Unsigned	0x31	NA	8	-	RO	Supports SMBus byte reads
Remote Temp LSB – Unsigned	0x32	NA	5/3	-	RO	All unused bits are reported as "0".
DIODE CONFIGURATION REGISTERS						
Configuration Register 2	0xBF	0xBF	5	0x1F	R/W	Filter Enable, Diode Model Select, Diode Fault Mask; Pin 6 $\overline{OS}$/A0 function select
Remote Offset High Byte	0x11	0x11	8	0x00	R/W	2's Complement
Remote Offset Low Byte	0x12	0x12	3	0x00	R/W	2's Complement All unused bits are reported as "0".
GENERAL CONFIGURATION REGISTERS						
Configuration Register 1	0x03/ 0x09	0x09/ 0x03	5	0x00	R/W	STOP/$\overline{RUN}$, Remote TCRIT mask, Remote OS mask, Local TCRIT mask, Local OS mask
Conversion Rate	0x04/0x0A	0x04/0x0A	2	0x02	R/W	Continuous or specific settings
One-Shot	NA	0x0F	-	-	WO	A write to this register activates one conversion if STOP/$\overline{RUN}$ bit = 1.
STATUS REGISTERS						
Status Register 1	0x02	NA	5	-	RO	Busy bit, and status bits
Status Register 2	0x33	NA	2	-	RO	Not Ready bit, Diode detect bit
LIMIT REGISTERS						
Remote OS Limit	0x07/ 0x0D	0x0D/ 0x07	8	0x55	R/W	Unsigned 0 to 255°C Default 85°C
Local Shared OS and T_Crit Limit	0x20	0x20	7	0x55	R/W	Unsigned 0 to 127°C Default 85°C
Remote T_Crit Limit	0x19	0x19	8	0x6E	R/W	Unsigned 0 to 255°C Default 110°C
Common Hysteresis	0x21	0x21	5	0x0A	R/W	up to 31°C
IDENTIFICATION REGISTERS						
Manufacturer ID	0xFE			0x01	RO	Always returns 0x01
Revision ID	0xFF			0xB1	RO	Returns revision number.

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LOCAL and REMOTE MSB and LSB TEMPERATURE REGISTERS

Table 10. Local Temperature MSB

(Read Only Address 00h)

10-bit plus sign format:

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Value	SIGN	64	32	16	8	4	2	1

Temperature Data: LSb = 1°C.

Table 11. Local Temperature LSB

(Read Only Address 30h)

10-bit plus sign format:

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Value	0.5	0.25	0.125	0	0	0	0	0

Temperature Data: LSb = 0.125°C.

Table 12. Signed Remote Temperature MSB

(Read Only Address 01h)

12-bit plus sign format:

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Value	SIGN	64	32	16	8	4	2	1

Temperature Data: LSb = 1°C.

Table 13. Signed Remote Temperature LSB, Filter On

(Read Only Address 10h)

12-bit plus sign binary formats with filter on:

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Value	0.5	0.25	0.125	0.0625	0.03125	0	0	0

Table 14. Signed Remote Temperature LSB, Filter Off

(Read Only Address 10h)

12-bit plus sign binary formats with filter off:

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Value	0.5	0.25	0.125	0	0	0	0	0

Temperature Data: LSb = 0.125°C filter off or 0.03125°C filter on.

Table 15. Unsigned Remote Temperature MSB

(Read Only Address 31h)

13-bit unsigned format:

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Value	128	64	32	16	8	4	2	1

Temperature Data: LSb = 1°C.

Table 16. Unsigned Remote Temperature LSB, Filter On

(Read Only Address 32h)

13-bit unsigned binary formats with filter on:

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Value	0.5	0.25	0.125	0.0625	0.03125	0	0	0

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Table 17. Unsigned Remote Temperature LSB, Filter Off

(Read Only Address 32h)

13-bit unsigned binary formats with filter off:

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Value	0.5	0.25	0.125	0	0	0	0	0

Temperature Data: LSb = 0.125°C filter off or 0.03125°C filter on.

For data synchronization purposes, the MSB register should be read first if the user wants to read both MSB and LSB registers. The LSB will be locked after the MSB is read. The LSB will be unlocked after being read. If the user reads MSBs consecutively, each time the MSB is read, the LSB associated with that temperature will be locked in and override the previous LSB value locked-in.

DIODE CONFIGURATION REGISTERS

Table 18. Configuration Register 2

(Read/write Address BFh)

D7	D6	D5	D4	D3	D2	D1	D0
0	$\overline{OS}$/A0 Function Select	OS Fault Mask	$\overline{T_CRIT}$ Mask	TruTherm Select	RFE1	RFE0	1

Bits	Name	Description
7	Reserved	Reports "0" when read.
6	$\overline{OS}$/A0 Function Select	0: Address (A0) function is enabled 1: Over-temperature Shutdown (OS) is enabled
5	Diode Fault Mask for $\overline{OS}$	0: Off 1: On
4	Diode Fault Mask for $\overline{T_CRIT}$	0: Off 1: On
3	Remote Diode TruTherm Mode Select	0: Selects Diode Model 2, MMBT3904, with TruTherm technology disabled. 1: Selects Diode Model 1, A typical Intel Processor, with 65 nm or 90 nm technology, and TruTherm technology enabled.
2-1	Remote Filter Enable	00: Filter Disable 01: Reserved 10: Reserved 11: Filter Enable
0	Reserved	Reports "1" when read.

Power up default is 1Fh.

Table 19. Remote Offset High Byte (2's Complement)

(R/W Address 11h)

10-bit plus sign format:

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Value	SIGN	64	32	16	8	4	2	1

Power up default is 00h.

Table 20. Remote Offset Low Byte (2's Complement)

10-bit plus sign format:(R/W Address 12h)

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Value	0.50	0.25	0.125	0	0	0	0	0

Power up default is 00h. LSb = 0.125°C.

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GENERAL CONFIGURATION REGISTERS

Table 21. Configuration Register 1

(Read/write Address 03h/09h or 09h/03h):

D7	D6	D5	D4	D3	D2	D1	D0
0	STOP/$\overline{\text{RUN}}$	0	Remote $\overline{\text{T_CRIT}}$ Mask	Remote $\overline{\text{OS}}$ Mask	Local $\overline{\text{T_CRIT}}$ Mask	Local $\overline{\text{OS}}$ Mask	0

Bits	Name	Description
7	Reserved	Reports "0" when read.
6	STOP/$\overline{\text{RUN}}$	0: Active / Converting 1: Standby
5	Reserved	Reports "0" when read.
4	Remote $\overline{\text{T_CRIT}}$ Mask	0: Off 1: On
3	Remote $\overline{\text{OS}}$ Mask	0: Off 1: On
2	Local $\overline{\text{T_CRIT}}$ Mask	0: Off 1: On
1	Local $\overline{\text{OS}}$ Mask	0: Off 1: On
0	Reserved	Reports "0" when read.

Power up default is 00h.

Table 22. Conversion Rate Register

(Read/write Address 04h/0Ah or 0Ah/04h):

2-bit format:

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Value	0	0	0	0	0	0	MSb	LSb

Bits	Name	Description
7:2	Reserved	Reports "0" when read.
1:0	Conversion Rate	00: Continuous (33 ms typical when remote diode is missing or fault or 63 ms typical with remote diode connected) 01: 0.364 seconds 10: 1 second 11: 2.5 seconds

Power up default is 02h (1 second).

Table 23. One Shot Register

(Write Only Address 0Fh):

Writing to this register will start one conversion if the device is in standby mode (i.e. STOP/$\overline{\text{RUN}}$ bit = 1).

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STATUS REGISTERS

Table 24. Status Register 1

(Read Only Address 02h):

D7	D6	D5	D4	D3	D2	D1	D0
Busy	0	0	ROS	0	Diode Fault	RTCRIT	LOC

Bits	Name	Description
7	Busy	When set to "1" the part is converting.
6-5	Reserved	Report "0" when read.
4	ROS	Status Bit for Remote OS
3	Reserved	Reports "0" when read.
2	Diode Fault	Status bit for missing diode (Either D+ is shorted to GND, and/or V_{DD}, and/or D-; or D+ is floating.) Note: The unsigned registers will report 0°C if read; the signed value registers will report -128.000°C.
1	RTCRIT	Status bit for Remote TCRIT.
0	LOC	Status bit for the shared Local OS and TCRIT .

Table 25. Status Register 2

(Read Only Address 33h):

D7	D6	D5	D4	D3	D2	D1	D0
Not Ready	TruTherm 3904 Detect	0	0	0	0	0	0

Bits	Name	Description
7	Not Ready	Waiting for 30 ms power-up sequence to end.
6	TruTherm 3904 Detect	1: MMBT3904 is connected and TruTherm technology is enabled. 0: MMBT3904 is connected and TruTherm technology is disabled.
5-0	Reserved	Reports "0" when read.

LIMIT REGISTERS

Table 26. Unsigned Remote OS Limit - 0°C to 255°C

(Read/Write Address 07h/0Dh or 0Dh/07h):

D7	D6	D5	D4	D3	D2	D1	D0
128	64	32	16	8	4	2	1

Power on Reset default is 55h (85°C).

Table 27. Unsigned Local Shared OS and T_CRIT Limit - 0°C to 127°C

(Read/Write Address 20h):

D7	D6	D5	D4	D3	D2	D1	D0
128	64	32	16	8	4	2	1

Power on Reset default is 55h (85°C).

Table 28. Unsigned Remote T_CRIT Limit - 0°C to 255°C

(Read/Write Address 19h):

D7	D6	D5	D4	D3	D2	D1	D0
128	64	32	16	8	4	2	1

Power on Reset default is 6Eh (110°C).

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Table 29. Common Hysteresis Register

(Read/Write Address 21h):

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	16	8	4	2	1

Power on Reset default is 0Ah (10°C).

IDENTIFICATION REGISTERS

Table 30. Manufacturers ID Register

(Read Only Address FEh): Always returns 01h.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1

Table 31. Revision ID Register

(Read Only Address FFh): Default is B1h. This register will increment by 1 every time there is a revision to the die by Texas Instruments. The initial revision bits for B1h are shown below.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	0	0	0	1

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APPLICATIONS HINTS

The LM95235 can be applied easily in the same way as other integrated-circuit temperature sensors, and its remote diode sensing capability allows it to be used in new ways as well. It can be soldered to a printed circuit board, and because the path of best thermal conductivity is between the die and the pins, its temperature will effectively be that of the printed circuit board lands and traces soldered to the LM95235's pins. This presumes that the ambient air temperature is almost the same as the surface temperature of the printed circuit board; if the air temperature is much higher or lower than the surface temperature, the actual temperature of the LM95235 die will be at an intermediate temperature between the surface and air temperatures. Again, the primary thermal conduction path is through the leads, so the circuit board temperature will contribute to the die temperature much more strongly than will the air temperature.

To measure temperature external to the LM95235's die, use a remote diode. This diode can be located on the die of a target IC, allowing measurement of the IC's temperature, independent of the LM95235's temperature. A discrete diode can also be used to sense the temperature of external objects or ambient air. Remember that a discrete diode's temperature will be affected, and often dominated, by the temperature of its leads. Most silicon diodes do not lend themselves well to this application. It is recommended that an MMBT3904 transistor base-emitter junction be used with the collector tied to the base.

The LM95235's TruTherm technology allows accurate sensing of integrated thermal diodes, such as those found on most processors. With TruTherm technology turned off, the LM95235 can measure a diode-connected transistor such as the MMBT3904 or the thermal diode found in an AMD processor.

The LM95235 has been optimized to measure the remote thermal diode integrated in a typical Intel processor on 65 nm or 90 nm process or an MMBT3904 transistor. Using the Remote Diode Model Select register either pair of remote inputs can be assigned to be either a typical Intel processor on 65 nm or 90 nm process or an MMBT3904.

DIODE NON-IDEALITY

Diode Non-Ideality Factor Effect on Accuracy

When a transistor is connected as a diode, the following relationship holds for variables V_{BE}, T and I_F:

$$I_F = I_S \times \left[e^{\left(\frac{V_{BE}}{\eta \times V_t} \right)} - 1 \right]$$

where

- $V_t = \frac{kT}{q}$
- q = 1.6×10^{-19} Coulombs (the electron charge),
- T = Absolute Temperature in Kelvin
- k = 1.38×10^{-23} joules/K (Boltzmann's constant),
- η is the non-ideality factor of the process the diode is manufactured on,
- I_S = Saturation Current and is process dependent,
- I_f = Forward Current through the base-emitter junction
- V_{BE} = Base-Emitter Voltage drop (1)

In the active region, the -1 term is negligible and may be eliminated, yielding the following equation

$$I_F = I_S \times \left[e^{\left(\frac{V_{BE}}{\eta \times V_t} \right)} \right] \quad (2)$$

In Equation 2, η and I_S are dependant upon the process that was used in the fabrication of the particular diode. By forcing two currents with a very controlled ratio(I_{F2} / I_{F1}) and measuring the resulting voltage difference, it is possible to eliminate the I_S term. Solving for the forward voltage difference yields the relationship:

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$$\Delta V_{BE} = \eta \times \left(\frac{kT}{q}\right) \times \ln\left(\frac{I_{F2}}{I_{F1}}\right) \quad (3)$$

Solving Equation 3 for temperature yields:

$$T = \frac{q \times \Delta V_{BE}}{\eta \times k \times \ln\left(\frac{I_{F2}}{I_{F1}}\right)} \quad (4)$$

Equation 4 holds true when a diode connected transistor such as the MMBT3904 is used. When this "diode" equation is applied to an integrated diode such as a processor transistor with its collector tied to GND as shown in Figure 18 it will yield a wide non-ideality spread. This wide non-ideality spread is not due to true process variation but due to the fact that Equation 4 is an approximation.

TruTherm technology uses the transistor equation, Equation 5, which is a more accurate representation of the topology of the thermal diode found in an FPGA or processor.

$$T = \frac{q \times \Delta V_{BE}}{\eta \times k \times \ln\left(\frac{I_{C2}}{I_{C1}}\right)} \quad (5)$$

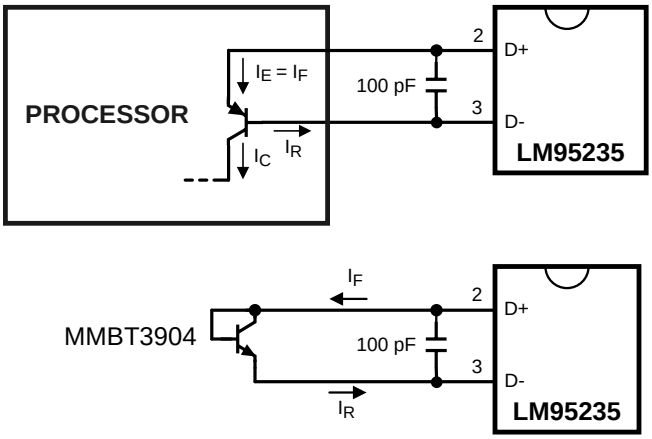

Figure 18. Thermal Diode Current Paths

TruTherm should only be enabled when measuring the temperature of a transistor integrated as shown in the processor of Figure 18, because Equation 5 only applies to this topology.

Calculating Total System Accuracy

The voltage seen by the LM95235 also includes the $I_F R_S$ voltage drop of the series resistance. The non-ideality factor, η, is the only other parameter not accounted for and depends on the diode that is used for measurement. Since ΔV_{BE} is proportional to both η and T, the variations in η cannot be distinguished from variations in temperature. Since the non-ideality factor is not controlled by the temperature sensor, it will directly add to the inaccuracy of the sensor. For the for Intel processor on 65nm process, Intel specifies a +4.06%/-0.897% variation in η from part to part when the processor diode is measured by a circuit that assumes diode equation, Equation 4, as true. As an example, assume a temperature sensor has an accuracy specification of ±1.0°C at a temperature of 80°C (353 Kelvin) and the processor diode has a non-ideality variation of +1.19%/-0.27%. The resulting system accuracy of the processor temperature being sensed will be:

$$T_{ACC} = + 1.0°C + (+4.06\% \text{ of } 353 \text{ K}) = +15.3°C \quad (6)$$

and

$$T_{ACC} = - 1.0°C + (-0.89\% \text{ of } 353 \text{ K}) = -4.1°C \quad (7)$$

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TrueTherm technology uses the transistor equation, Equation 5, resulting in a non-ideality spread that truly reflects the process variation which is very small. The transistor equation non-ideality spread is ±0.39% for the Pentium 4 processor on 90 nm process. The resulting accuracy when using TruTherm technology improves to:

$$T_{ACC} = \pm 0.75°C + (\pm 0.39\% \text{ of } 353 \text{ K}) = \pm 2.16°C \quad (8)$$

The next error term to be discussed is that due to the series resistance of the thermal diode and printed circuit board traces. The thermal diode series resistance is specified on most processor data sheets. For Intel processors in 65 nm process, this is specified at 4.52Ω typical. The LM95235 accommodates the typical series resistance of Intel Processor on 65 nm process. The error that is not accounted for is the spread of the processor's series resistance, that is 2.79Ω to 6.24Ω or ±1.73Ω. The equation to calculate the temperature error due to series resistance (T_{ER}) for the LM95235 is simply:

$$T_{ER} = \left(0.62 \frac{°C}{\Omega}\right) \times R_{PCB} \quad (9)$$

Solving Equation 9 for R_{PCB} equal to ±1.73Ω results in the additional error due to the spread in the series resistance of ±1.07°C. The spread in error cannot be canceled out, as it would require measuring each individual thermal diode device. This is quite difficult and impractical in a large volume production environment.

Equation 9 can also be used to calculate the additional error caused by series resistance on the printed circuit board. Since the variation of the PCB series resistance is minimal, the bulk of the error term is always positive and can simply be cancelled out by subtracting it from the output readings of the LM95235.

Processor Family	Transistor Equation η_T, Non-ideality			Series R,Ω
	Min	Typ	Max	
Intel Processor on 65 nm process	0.997	1.001	1.005	4.52

Processor Family	Diode Equation η_D, Non-ideality			Series R,Ω
	Min	Typ	Max	
Pentium III CPUID 67h	1	1.0065	1.0125	
Pentium III CPUID 68h, PGA370Socket, Celeron	1.0057	1.008	1.0125	
Pentium 4, 423 pin	0.9933	1.0045	1.0368	
Pentium 4, 478 pin	0.9933	1.0045	1.0368	
Pentium 4 on 0.13 micron process, 2 to 3.06 GHz	1.0011	1.0021	1.0030	3.64
Pentium 4 on 90 nm process	1.0083	1.011	1.023	3.33
Intel Processor on 65 nm process	1.000	1.009	1.050	4.52
Pentium M (Centrino)	1.00151	1.00220	1.00289	3.06
MMBT3904		1.003		
AMD Athlon MP model 6	1.002	1.008	1.016	
AMD Athlon 64	1.008	1.008	1.096	
AMD Opteron	1.008	1.008	1.096	
AMD Sempron		1.00261		0.93

Compensating for Different Non-Ideality

In order to compensate for the errors introduced by non-ideality, the temperature sensor is calibrated for a particular processor. Texas Instruments temperature sensors are always calibrated to the typical non-ideality and series resistance of a given processor type. The LM95235 is calibrated for two non-ideality factors and series resistance values thus supporting the MMBT3904 transistor and Intel processors on 65nm process without the requirement for additional trims. For most accurate measurements TruTherm mode should be turned on when measuring the Intel processor on 65nm process to minimize the error introduced by the false non-ideality spread (see Diode Non-Ideality Factor Effect on Accuracy). When a temperature sensor calibrated for a particular processor type is used with a different processor type, additional errors are introduced.

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Temperature errors associated with non-ideality of different processor types may be reduced in a specific temperature range of concern through use of software calibration. Typical Non-ideality specification differences cause a gain variation of the transfer function, therefore the center of the temperature range of interest should be the target temperature for calibration purposes. The following equation can be used to calculate the temperature correction factor (T_{CF}) required to compensate for a target non-ideality differing from that supported by the LM95235.

$$T_{CF} = \left(\frac{\eta_S - \eta_{PROCESSOR}}{\eta_S} \right) x \, (T_{CR} + 273K) \tag{10}$$

where

- η_S = LM95235 non-ideality for accuracy specification
- $\eta_{PROCESSOR}$ = Processor thermal diode typical non-ideality
- T_{CR} = center of the temperature range of interest in °C

The correction factor should be directly added to the temperature reading produced by the LM95235. For example when using the LM95235, with the 3904 mode selected, to measure a AMD Athlon processor, with a typical non-ideality of 1.008, for a temperature range of 60°C to 100°C the correction factor would calculate to:

$$T_{CF} = \left(\frac{1.003 - 1.008}{1.003} \right) \cdot (80 + 273) = -1.75^{o}C \tag{11}$$

Therefore, 1.75°C should be subtracted from the temperature readings of the LM95235 to compensate for the differing typical non-ideality target.

PCB LAYOUT FOR MINIMIZING NOISE

Figure 19. Ideal Diode Trace Layout

In a noisy environment, such as a processor mother board, layout considerations are very critical. Noise induced on traces running between the remote temperature diode sensor and the LM95235 can cause temperature conversion errors. Keep in mind that the signal level the LM95235 is trying to measure is in microvolts. The following guidelines should be followed:

1. V_{DD} should be bypassed with a 0.1 µF capacitor in parallel with 100 pF. The 100 pF capacitor should be placed as close as possible to the power supply pin. A bulk capacitance of approximately 10 µF needs to be in the near vicinity of the LM95235.
2. A 100 pF diode bypass capacitor is recommended to filter high frequency noise but may not be necessary. Make sure the traces to the 100 pF capacitor are matched. Place the filter capacitors close to the LM95235 pins.
3. Ideally, the LM95235 should be placed within 10 cm of the Processor diode pins with the traces being as straight, short and identical as possible. Trace resistance of 1Ω can cause as much as 0.62°C of error. This error can be compensated by using simple software offset compensation.
4. Diode traces should be surrounded by a GND guard ring to either side, above and below if possible. This GND guard should not be between the D+ and D- lines. In the event that noise does couple to the diode lines it would be ideal if it is coupled common mode. That is equally to the D+ and D- lines.
5. Avoid routing diode traces in close proximity to power supply switching or filtering inductors.
6. Avoid running diode traces close to or parallel to high speed digital and bus lines. Diode traces should be kept at least 2 cm apart from the high speed digital traces.

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7. If it is necessary to cross high speed digital traces, the diode traces and the high speed digital traces should cross at a 90 degree angle.
8. The ideal place to connect the LM95235's GND pin is as close as possible to the Processors GND associated with the sense diode.
9. Leakage current between D+ and GND and between D+ and D- should be kept to a minimum. Thirteen nano-amperes of leakage can cause as much as 0.2°C of error in the diode temperature reading. Keeping the printed circuit board as clean as possible will minimize leakage current.

Noise coupling into the digital lines greater than 400 mVp-p (typical hysteresis) and undershoot less than 500 mV below GND, may prevent successful SMBus communication with the LM95235. SMBus no acknowledge is the most common symptom, causing unnecessary traffic on the bus. Although the SMBus maximum frequency of communication is rather low (100 kHz max), care still needs to be taken to ensure proper termination within a system with multiple parts on the bus and long printed circuit board traces. An RC lowpass filter with a 3 dB corner frequency of about 40 MHz is included on the LM95235's SMBCLK input. Additional resistance can be added in series with the SMBDAT and SMBCLK lines to further help filter noise and ringing. Minimize noise coupling by keeping digital traces out of switching power supply areas as well as ensuring that digital lines containing high speed data communications cross at right angles to the SMBDAT and SMBCLK lines.

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REVISION HISTORY

Changes from Revision E (March 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	28

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM95235CIMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 90	T36C	Samples
LM95235CIMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 90	T36C	Samples
LM95235DIMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 90	T36D	Samples
LM95235DIMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 90	T36D	Samples
LM95235EIMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 90	T36E	Samples
LM95235QEIMM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	36QE	
LM95235QEIMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	36QE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LM95235, LM95235-Q1 :

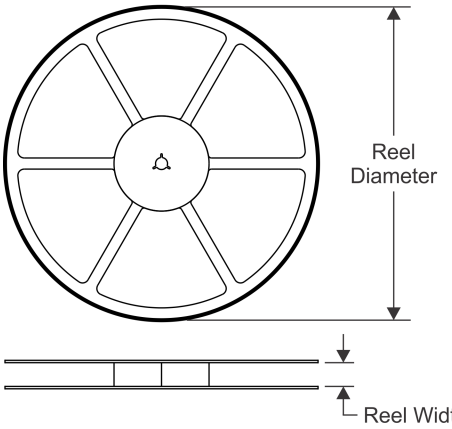
- Catalog: LM95235
- Automotive: LM95235-Q1

NOTE: Qualified Version Definitions:

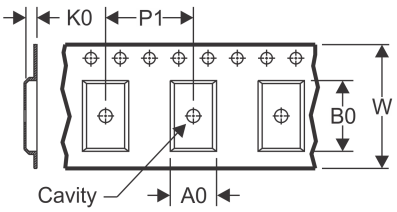
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

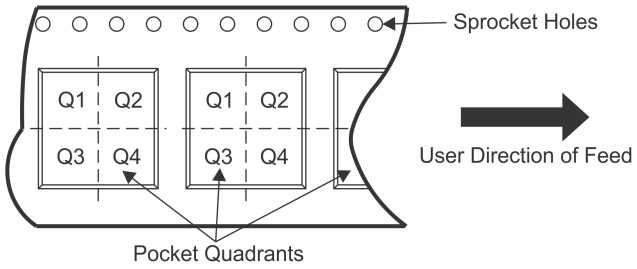


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

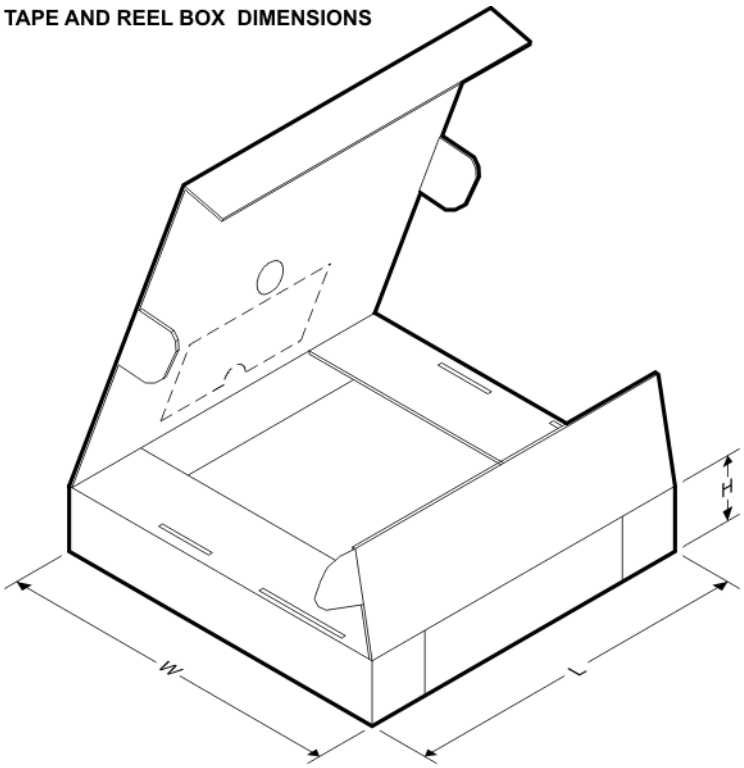
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM95235CIMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM95235CIMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM95235DIMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM95235DIMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM95235EIMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM95235QEIMM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM95235QEIMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

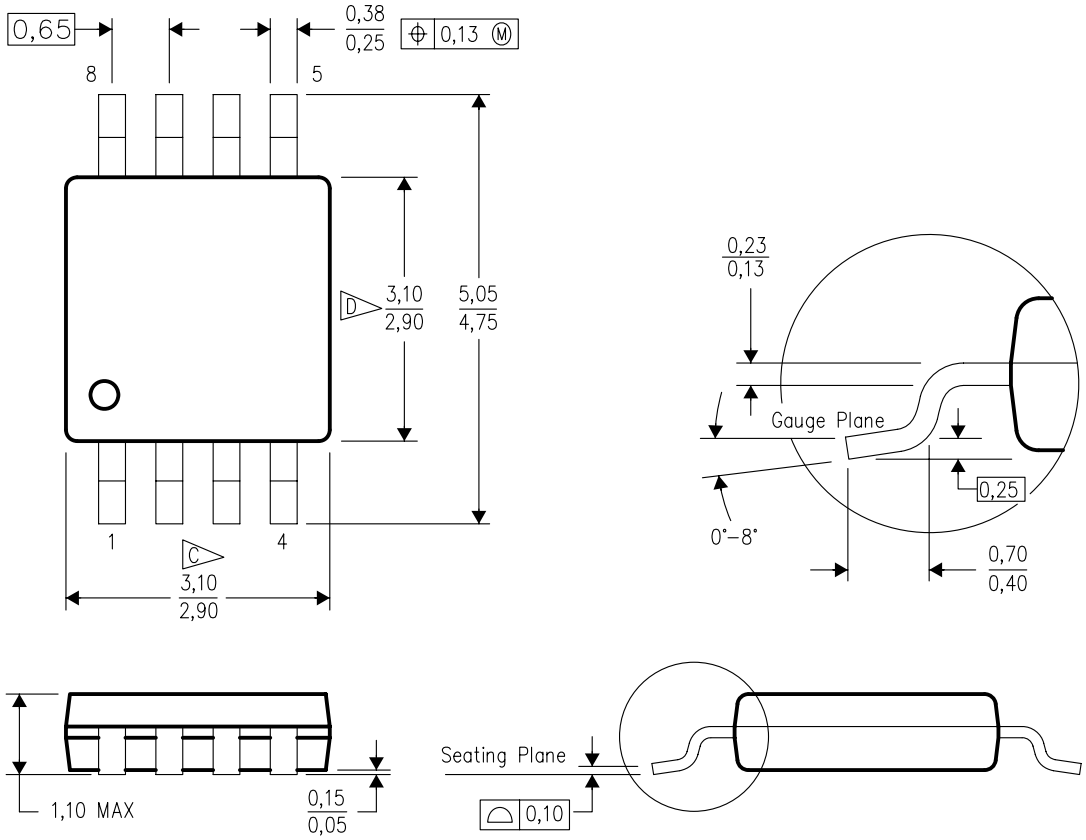
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM95235CIMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM95235CIMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM95235DIMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM95235DIMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM95235EIMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM95235QEIMM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM95235QEIMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0

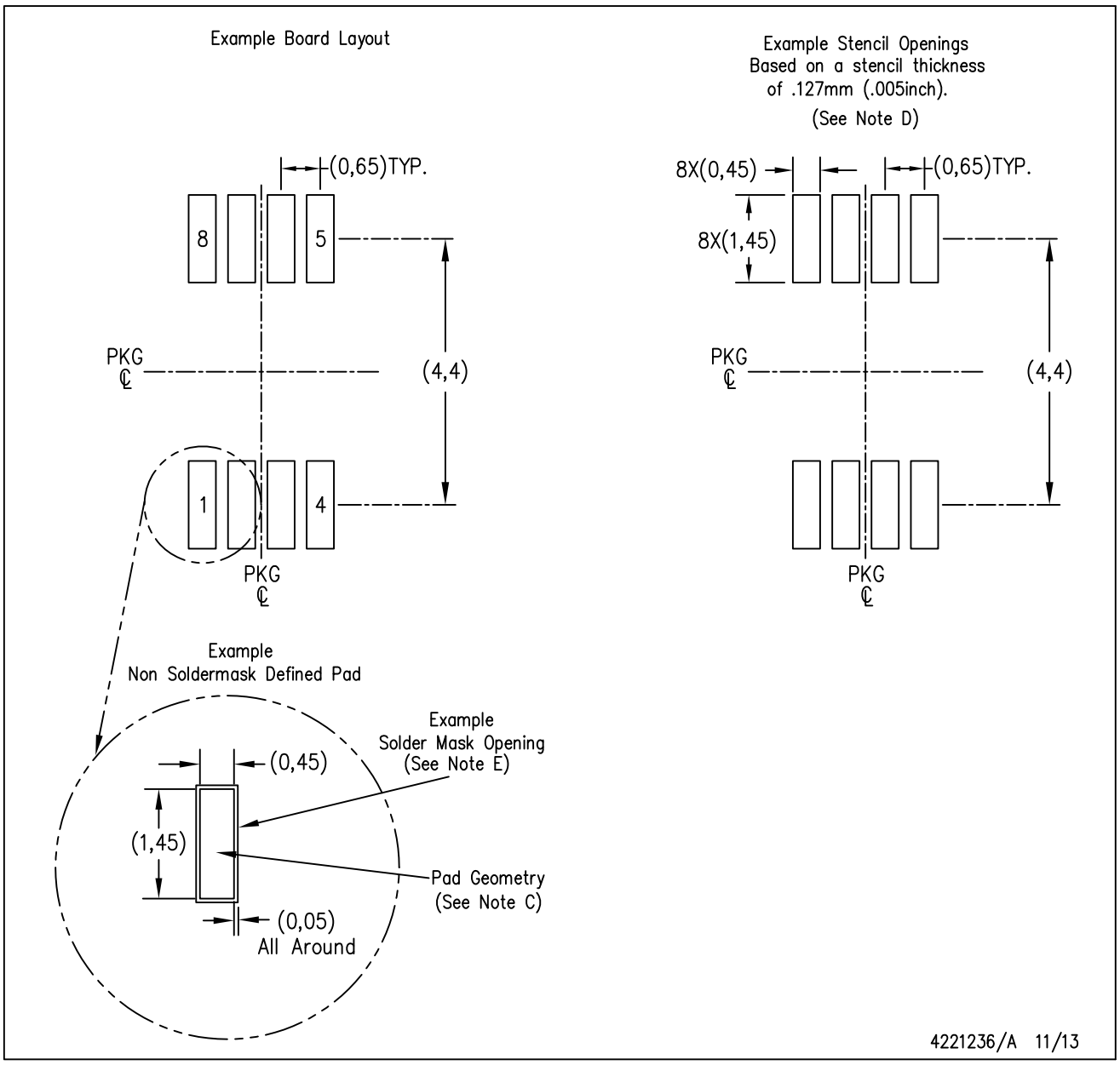
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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