



**THE DATASHEET OF  
LMC6041AIN**



## LMC6041 CMOS Single Micropower Operational Amplifier

Check for Samples: [LMC6041](#)

### FEATURES

- **Low Supply Current:** 14  $\mu\text{A}$  (Typ)
- **Operates from 4.5V to 15.5V Single Supply**
- **Ultra Low Input Current:** 2 fA (Typ)
- **Rail-to-Rail Output Swing**
- **Input Common-Mode Range Includes Ground**

### APPLICATIONS

- **Battery Monitoring and Power Conditioning**
- **Photodiode and Infrared Detector Preamplifier**
- **Silicon Based Transducer Systems**
- **Hand-Held Analytic Instruments**
- **pH Probe Buffer Amplifier**
- **Fire and Smoke Detection Systems**
- **Charge Amplifier for Piezoelectric Transducers**

### DESCRIPTION

Ultra-low power consumption and low input-leakage current are the hallmarks of the LMC6041. Providing input currents of only 2 fA typical, the LMC6041 can operate from a single supply, has output swing extending to each supply rail, and an input voltage range that includes ground.

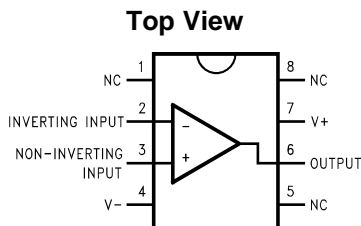
The LMC6041 is ideal for use in systems requiring ultra-low power consumption. In addition, the insensitivity to latch-up, high output drive, and output swing to ground without requiring external pull-down resistors make it ideal for single-supply battery-powered systems.

Other applications for the LMC6041 include bar code reader amplifiers, magnetic and electric field detectors, and hand-held electrometers.

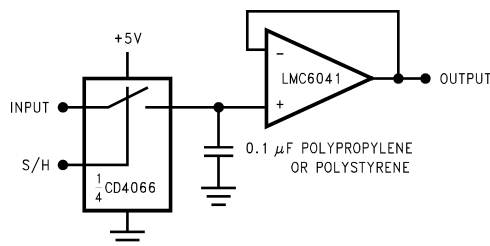
This device is built with TI's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6042 for a dual, and the LMC6044 for a quad amplifier with these features.

### Connection Diagrams



**Figure 1. 8-Pin SOIC or PDIP Package**  
See Package Number D0008A or P0008E



**Figure 2. Low-Leakage Sample and Hold**



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings<sup>(1)(2)</sup>

Differential Input Voltage	±Supply Voltage
Supply Voltage ( $V^+ - V^-$ )	16V
Output Short Circuit to $V^-$	See <sup>(3)</sup>
Output Short Circuit to $V^+$	See <sup>(4)</sup>
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	110°C
ESD Tolerance <sup>(5)</sup>	500V
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Current at Power Supply Pin	35 mA
Voltage at Input/Output Pin	$(V^+) + 0.3V, (V^-) - 0.3V$
Power Dissipation	See <sup>(6)</sup>

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- (3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 110°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
- (4) Do not connect output to  $V^+$  when  $V^+$  is greater than 13V or reliability may be adversely affected.
- (5) Human body model, 1.5 k $\Omega$  in series with 100 pF.
- (6) The maximum power dissipation is a function of  $T_{J(max)}$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(max)} - T_A)/\theta_{JA}$ .

### Operating Ratings

Temperature Range	LMC6041AI, LMC6041I	$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$
Supply Voltage		$4.5\text{V} \leq V^+ \leq 15.5\text{V}$
Power Dissipation		See <sup>(1)</sup>
Thermal Resistance ( $\theta_{JA}$ ) <sup>(2)</sup>	8-Pin PDIP package	101°C/W
	8-Pin SOIC package	165°C/W

- (1) For operating at elevated temperatures the device must be derated based on the thermal resistance  $\theta_{JA}$  with  $P_D = (T_J - T_A)/\theta_{JA}$ .
- (2) All numbers apply for packages soldered directly into a PC board.

## Electrical Characteristics

Unless otherwise specified, all limits ensured for  $T_A = T_J = 25^\circ\text{C}$ . **Boldface** limits apply at the temperature extremes.  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 1.5\text{V}$ ,  $V_O = V^+/2$ , and  $R_L > 1\text{M}$  unless otherwise specified.

Parameter		Test Conditions		Typical <sup>(1)</sup>	LMC6041AI Limit <sup>(2)</sup>	LMC6041I Limit <sup>(2)</sup>	Units (Limit)
$V_{\text{OS}}$	Input Offset Voltage			1	3	6	mV
					<b>3.3</b>	<b>6.3</b>	max
$\text{TCV}_{\text{OS}}$	Input Offset Voltage Average Drift			1.3			$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current			0.002	<b>4</b>	<b>4</b>	pA max
$I_{\text{OS}}$	Input Offset Current			0.001	<b>2</b>	<b>2</b>	pA max
$R_{\text{IN}}$	Input Resistance			>10			Tera $\Omega$
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{\text{CM}} \leq 12.0\text{V}$ $V^+ = 15\text{V}$		75	68	62	dB
					<b>66</b>	<b>60</b>	min
+PSRR	Positive Power Supply Rejection Ratio	$5\text{V} \leq V^+ \leq 15\text{V}$ $V_O = 2.5\text{V}$		75	68	62	dB
					<b>66</b>	<b>60</b>	min
-PSRR	Negative Power Supply Rejection Ratio	$0\text{V} \leq V^- \leq -10\text{V}$ $V_O = 2.5\text{V}$		94	84	74	dB
					<b>83</b>	<b>73</b>	min
CMR	Input Common-Mode Voltage Range	$V^+ = 5\text{V}$ and $15\text{V}$ for CMRR $\geq 50$ dB		-0.4	-0.1	-0.1	V
					<b>0</b>	<b>0</b>	max
		$V^+ - 1.9\text{V}$			$V^+ - 2.3\text{V}$	$V^+ - 2.3\text{V}$	V
					<b><math>V^+ - 2.5\text{V}</math></b>	<b><math>V^+ - 2.4\text{V}</math></b>	min
$A_V$	Large Signal Voltage Gain	$R_L = 100\text{ k}\Omega^{(3)}$	Sourcing	1000	400	300	V/mV
					<b>300</b>	<b>200</b>	min
			Sinking	500	180	90	V/mV
		$R_L = 25\text{ k}\Omega^{(3)}$	Sourcing	1000	200	100	V/mV
					<b>160</b>	<b>80</b>	min
			Sinking	250	100	50	V/mV
			<b>60</b>	<b>40</b>	min		
$V_O$	Output Swing	$V^+ = 5\text{V}$ $R_L = 100\text{ k}\Omega$ to $V^+/2$		4.987	4.970	4.940	V
					<b>4.950</b>	<b>4.910</b>	min
				0.004	0.030	0.060	V
					<b>0.050</b>	<b>0.090</b>	max
		$V^+ = 5\text{V}$ $R_L = 25\text{ k}\Omega$ to $V^+/2$		4.980	4.920	4.870	V
					<b>4.870</b>	<b>4.820</b>	min
				0.010	0.080	0.130	V
					<b>0.130</b>	<b>0.180</b>	max
		$V^+ = 15\text{V}$ $R_L = 100\text{ k}\Omega$ to $V^+/2$		14.970	14.920	14.880	V
					<b>14.880</b>	<b>14.820</b>	min
				0.007	0.030	0.060	V
					<b>0.050</b>	<b>0.090</b>	max
		$V^+ = 15\text{V}$ $R_L = 25\text{ k}\Omega$ to $V^+/2$		14.950	14.900	14.850	V
					<b>14.850</b>	<b>14.800</b>	min
				0.022	0.100	0.150	V
					<b>0.150</b>	<b>0.200</b>	max

(1) Typical Values represent the most likely parametric norm.

(2) All limits are ensured at room temperature (standard type face) or at operating temperature extremes (bold face type).

(3)  $V^+ = 15\text{V}$ ,  $V_{\text{CM}} = 7.5\text{V}$  and  $R_L$  connected to  $7.5\text{V}$ . For Sourcing tests,  $7.5\text{V} \leq V_O \leq 11.5\text{V}$ . For Sinking tests,  $2.5\text{V} \leq V_O \leq 7.5\text{V}$ .

## Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for  $T_A = T_J = 25^\circ\text{C}$ . **Boldface** limits apply at the temperature extremes.  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 1.5\text{V}$ ,  $V_O = V^+/2$ , and  $R_L > 1\text{M}$  unless otherwise specified.

Parameter		Test Conditions	Typical <sup>(1)</sup>	LMC6041AI Limit <sup>(2)</sup>	LMC6041I Limit <sup>(2)</sup>	Units (Limit)
$I_{\text{SC}}$	Output Current $V^+ = 5\text{V}$	Sourcing, $V_O = 0\text{V}$	22	16	13	mA
		Sinking, $V_O = 5\text{V}$	21	<b>10</b>	<b>8</b>	min
$I_{\text{SC}}$	Output Current $V^+ = 15\text{V}$	Sourcing, $V_O = 0\text{V}$	40	15	15	mA
		Sinking, $V_O = 13\text{V}^{(4)}$	39	<b>10</b>	<b>10</b>	min
$I_{\text{S}}$	Supply Current	$V_O = 1.5\text{V}$	14	20	26	$\mu\text{A}$
		$V^+ = 15\text{V}$	18	<b>24</b>	<b>30</b>	max
				<b>31</b>	<b>39</b>	max

(4) Do not connect output to  $V^+$  when  $V^+$  is greater than 13V or reliability may be adversely affected.

## AC Electrical Characteristics

Unless otherwise specified, all limits ensured for  $T_A = T_J = 25^\circ\text{C}$ . **Boldface** limits apply at the temperature extremes.  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 1.5\text{V}$ ,  $V_O = V^+/2$ , and  $R_L > 1\text{M}$  unless otherwise specified.

Parameter		Test Conditions	Typ <sup>(1)</sup>	LMC6041AI Limit <sup>(2)</sup>	LMC6041I Limit <sup>(2)</sup>	Units (Limit)
SR	Slew Rate	See <sup>(3)</sup>	0.02	0.015	0.010	V/ $\mu\text{s}$
				<b>0.010</b>	<b>0.007</b>	min
GBW	Gain-Bandwidth Product		75			kHz
$\phi_m$	Phase Margin		60			Deg
$e_n$	Input-Referred Voltage Noise	$F = 1\text{ kHz}$	83			nV/ $\sqrt{\text{Hz}}$
$i_n$	Input-Referred Current Noise	$F = 1\text{ kHz}$	0.0002			pA/ $\sqrt{\text{Hz}}$
THD	Total Harmonic Distortion	$F = 1\text{ kHz}$ , $A_V = -5$ $R_L = 100\text{ k}\Omega$ , $V_O = 2\text{ V}_{\text{pp}}$ $\pm 5\text{V}$ Supply	0.01			%

(1) Typical Values represent the most likely parametric norm.

(2) All limits are ensured at room temperature (standard type face) or at operating temperature extremes (bold face type).

(3)  $V^+ = 15\text{V}$ . Connected as Voltage Follower with 10V step input. Number specified in the slower of the positive and negative slew rates.

### Typical Performance Characteristics

$V_S = \pm 7.5V$ ,  $T_A = 25^\circ C$  unless otherwise specified

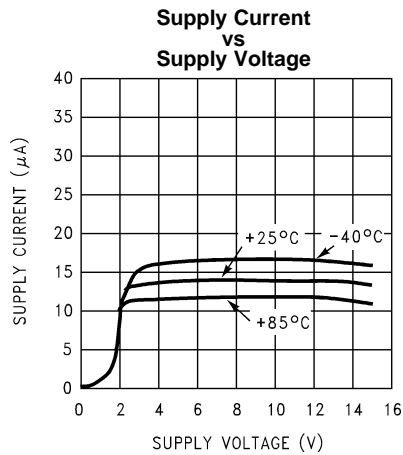


Figure 3.

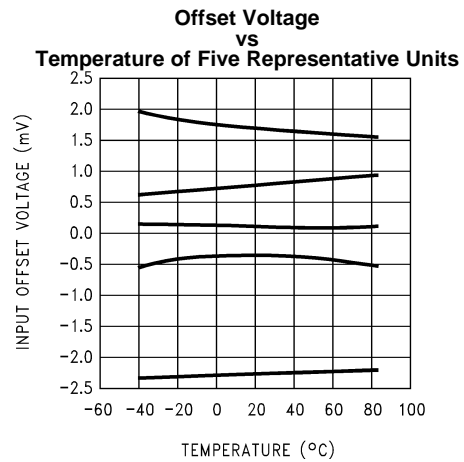


Figure 4.

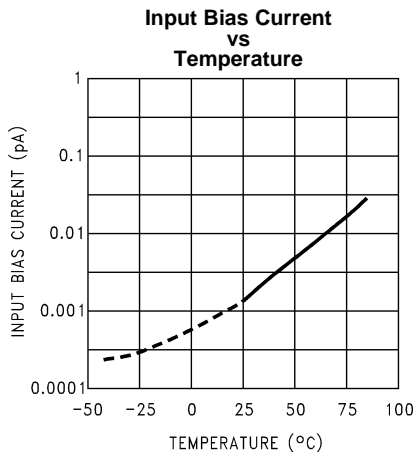


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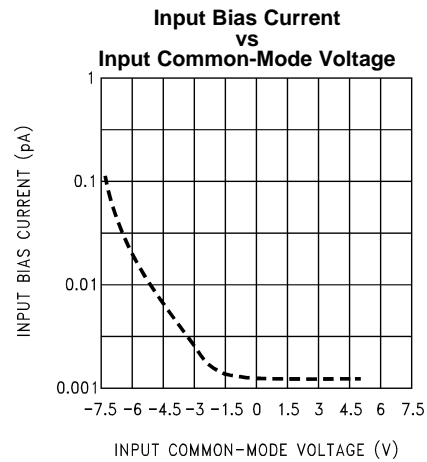


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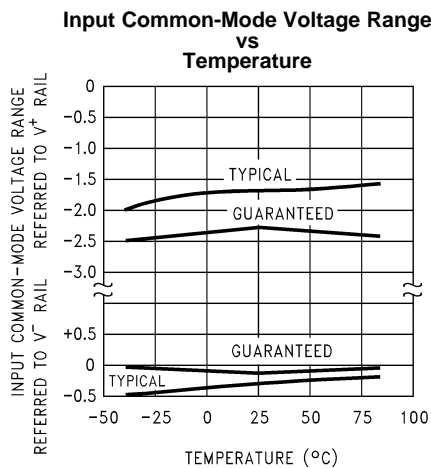


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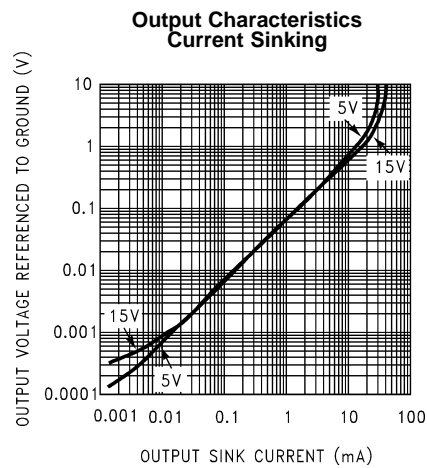


Figure 8.

**Typical Performance Characteristics (continued)**

$V_S = \pm 7.5V$ ,  $T_A = 25^\circ C$  unless otherwise specified

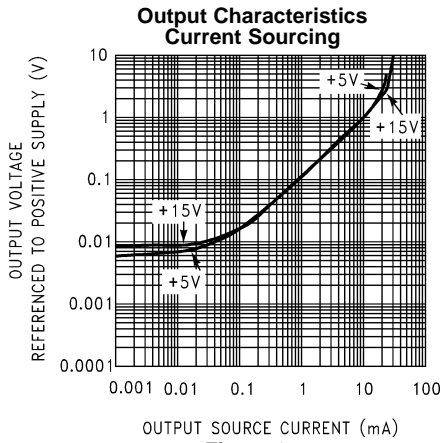


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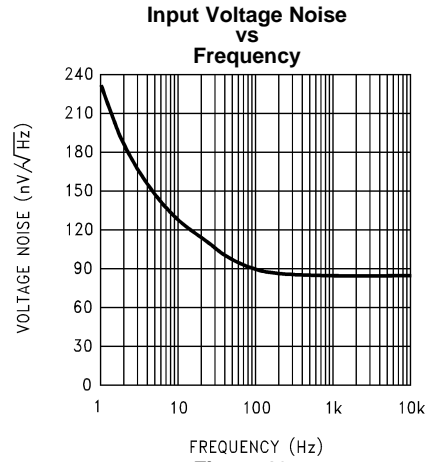


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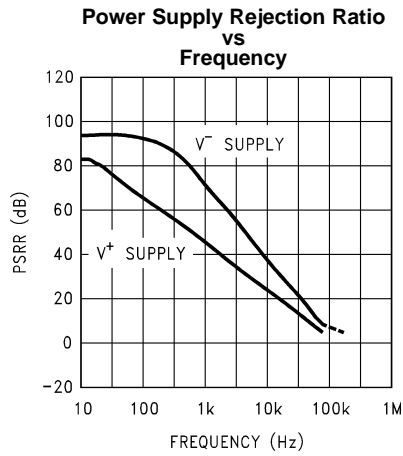


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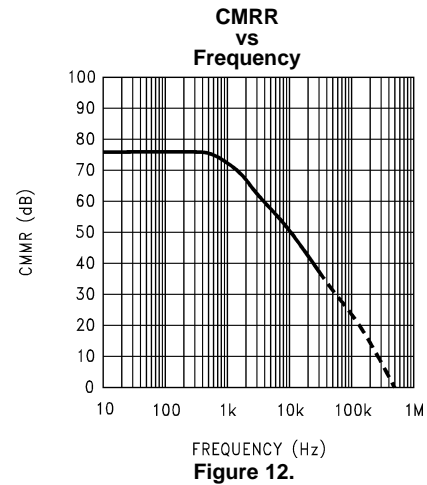


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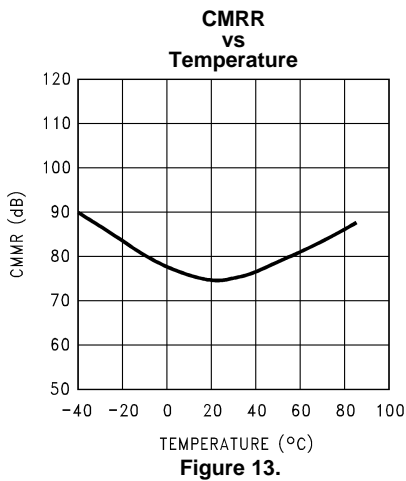


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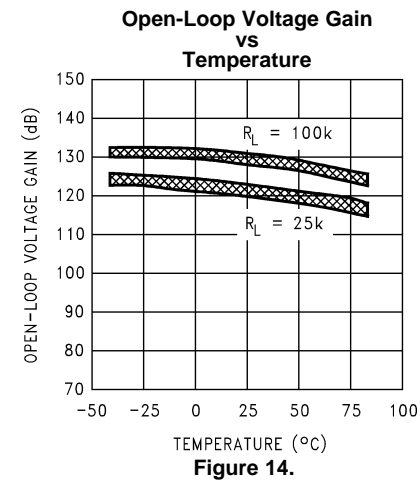


Figure 14.

Typical Performance Characteristics (continued)

$V_S = \pm 7.5V$ ,  $T_A = 25^\circ C$  unless otherwise specified

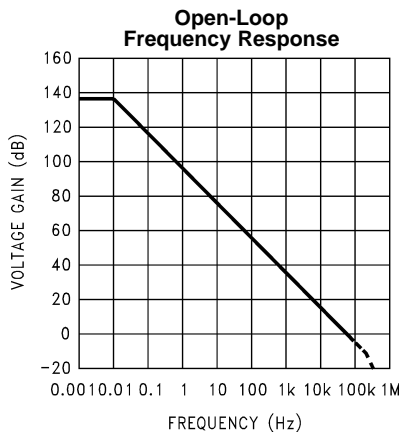


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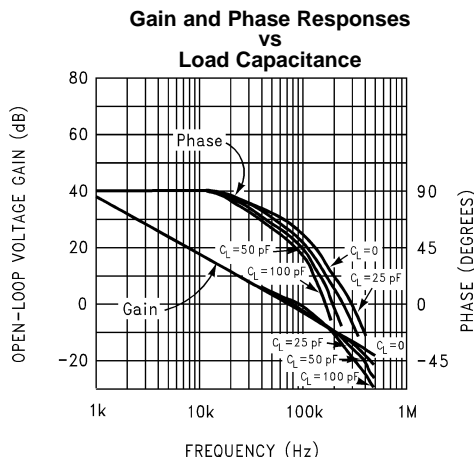


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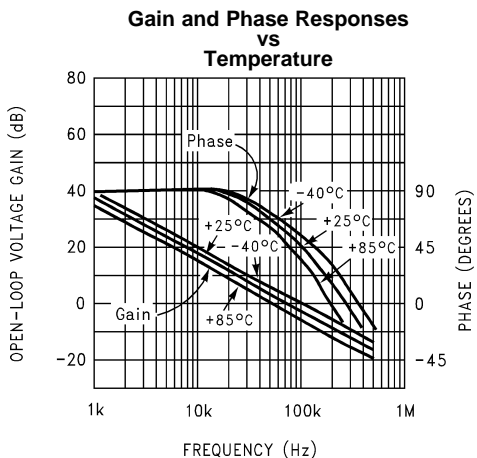


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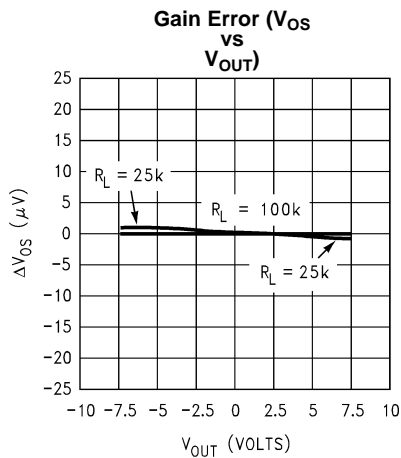


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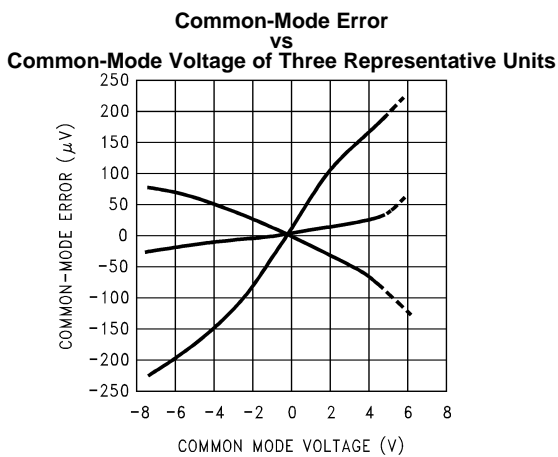


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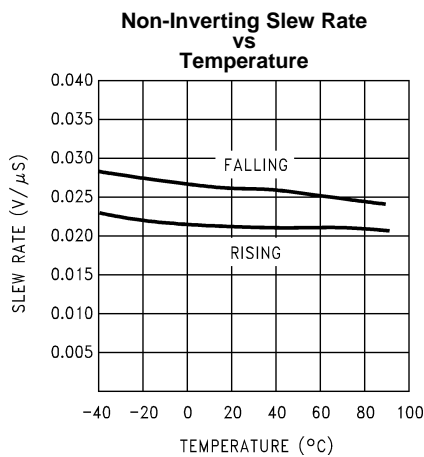


Figure 20.

**Typical Performance Characteristics (continued)**

$V_S = \pm 7.5V$ ,  $T_A = 25^\circ C$  unless otherwise specified

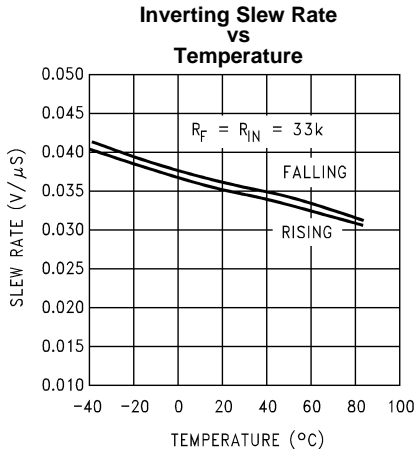


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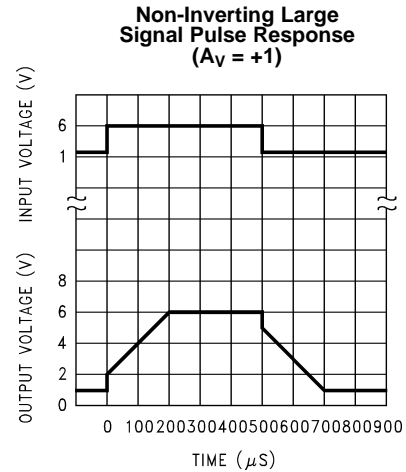


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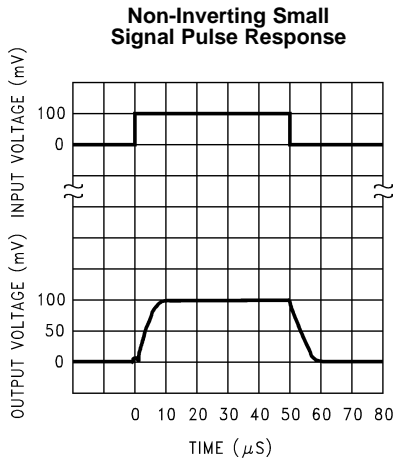


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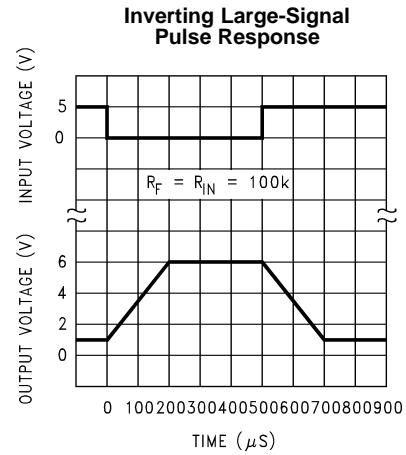


Figure 24.

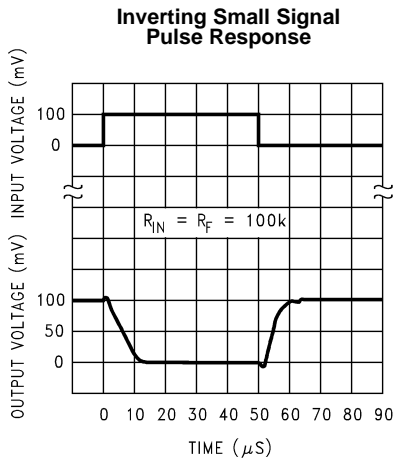


Figure 25.

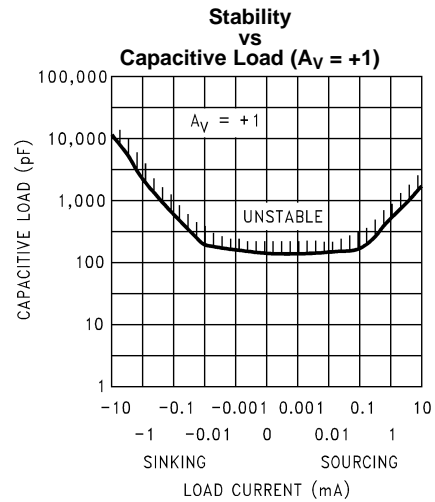
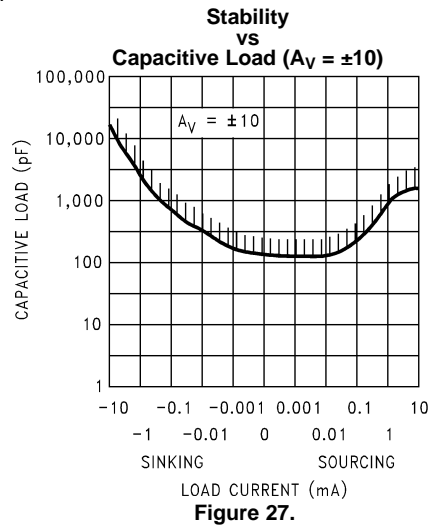


Figure 26.

**Typical Performance Characteristics (continued)**

$V_S = \pm 7.5V$ ,  $T_A = 25^\circ C$  unless otherwise specified



## APPLICATIONS HINTS

### AMPLIFIER TOPOLOGY

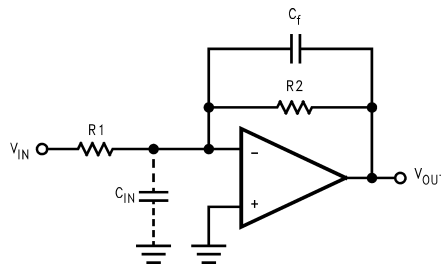
The LMC6041 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6041 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

### COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance with amplifiers with ultra-low input current, like the LMC6041.

Although the LMC6041 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuits board parasitics, reduce phase margins.

When high input impedance are demanded, guarding of the LMC6041 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See [Printed-Circuit-Board Layout for High Impedance Work](#).)



**Figure 28. Cancelling the Effect of Input Capacitance**

The effect of input capacitance can be compensated for by adding a capacitor. Adding a capacitor,  $C_f$ , around the feedback resistor (as in [Figure 28](#)) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \quad (1)$$

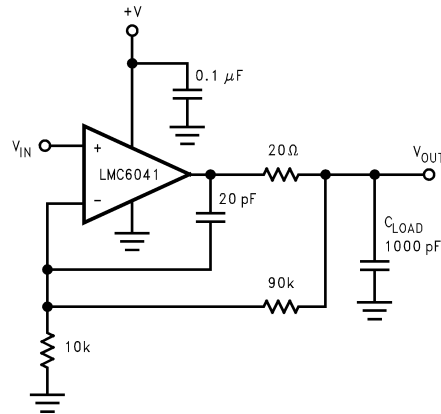
or

$$R_1 C_{IN} \leq R_2 C_f \quad (2)$$

Since it is often difficult to know the exact value of  $C_{IN}$ ,  $C_f$  can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.

### CAPACITIVE LOAD TOLERANCE

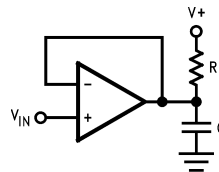
Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in [Figure 29](#).



**Figure 29. LMC6041 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads**

In the circuit of [Figure 29](#), R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to  $V^+$  ([Figure 30](#)). Typically a pull up resistor conducting 10  $\mu$ A or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see [Electrical Characteristics](#)).

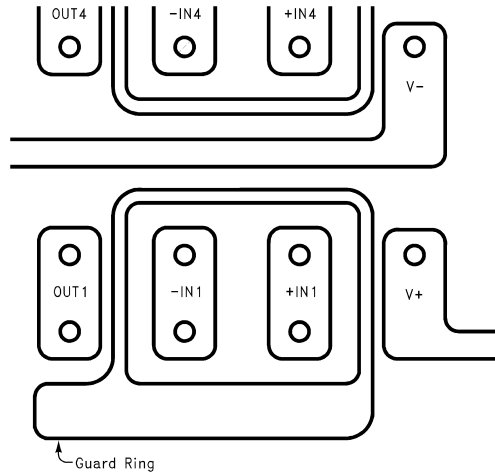


**Figure 30. Compensating for Large Capacitive Loads with a Pull Up Resistor**

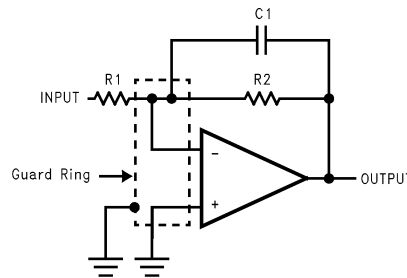
## PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6041, typically less than 2fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

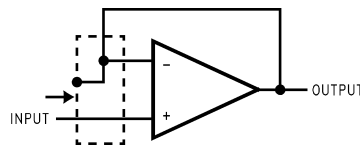
To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6041's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in [Figure 31](#). To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of  $10^{12}\Omega$ , which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6041's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of  $10^{11}\Omega$  would cause only 0.05 pA of leakage current. See [Figure 34](#) for typical connections of guard rings for standard op-amp configurations.



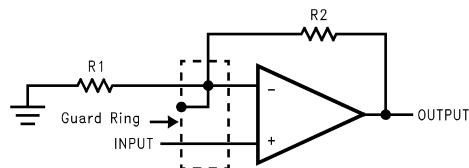
**Figure 31. Example of Guard Ring in P.C. Board Layout**



**Figure 32. Inverting Amplifier**



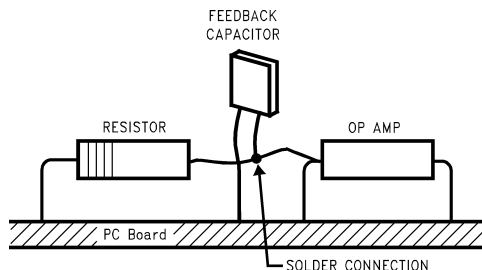
**Figure 33. Follower**



Non-Inverting Amplifier

**Figure 34. Typical Connections of Guard Rings**

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See [Figure 35](#).



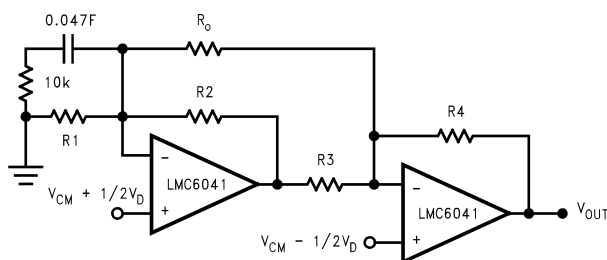
(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

**Figure 35. Air Wiring**

### Typical Single-Supply Applications

$$(V^+ = 5.0 V_{DC})$$

The extremely high input impedance, and low power consumption, of the LMC6041 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these type of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.



**Figure 36. Two Op-Amp Instrumentation Amplifier**

The circuit in [Figure 36](#) is recommended for applications where the common-mode input range is relatively low and the differential gain will be in the range of 10 to 1000. This two op-amp instrumentation amplifier features an independent adjustment of the gain and common-mode rejection trim, and a total quiescent supply current of less than 28  $\mu$ A. To maintain ultra-high input impedance, it is advisable to use ground rings and consider PC board layout an important part of the overall system design (see [Printed-Circuit-Board Layout for High Impedance Work](#)). Referring to [Figure 36](#), the input voltages are represented as a common-mode input  $V_{CM}$  plus a differential input  $V_D$ .

Rejection of the common-mode component of the input is accomplished by making the ratio of  $R1/R2$  equal to  $R3/R4$ . So that where,

$$\frac{R3}{R4} = \frac{R2}{R1}$$

$$V_{OUT} = \frac{R4}{R3} \left( 1 + \frac{R3}{R4} + \frac{R2 + R3}{R_O} \right) V_D \quad (3)$$

A suggested design guideline is to minimize the difference of value between  $R1$  through  $R4$ . This will often result in improved resistor tempco, amplifier gain, and CMRR over temperature. If  $R_N = R1 = R2 = R3 = R4$  then the gain equation can be simplified:

$$V_{OUT} = 2 \left( 1 + \frac{R_N}{R_O} \right) V_D \quad (4)$$

Due to the “zero-in, zero-out” performance of the LMC6041, and output swing rail-rail, the dynamic range is only limited to the input common-mode range of 0V to  $V_S - 2.3V$ , worst case at room temperature. This feature of the LMC6041 makes it an ideal choice for low-power instrumentation systems.

A complete instrumentation amplifier designed for a gain of 100 is shown in Figure 37. Provisions have been made for low sensitivity trimming of CMRR and gain.

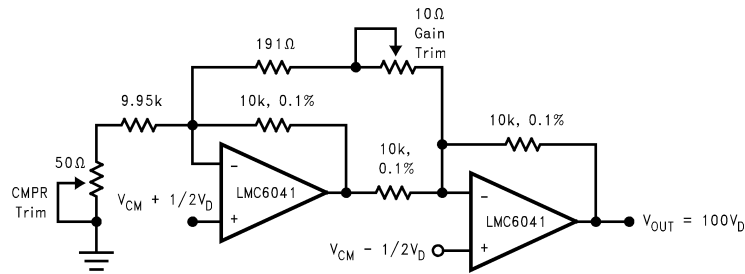


Figure 37. Low-Power Two-Op-Amp Instrumentation Amplifier

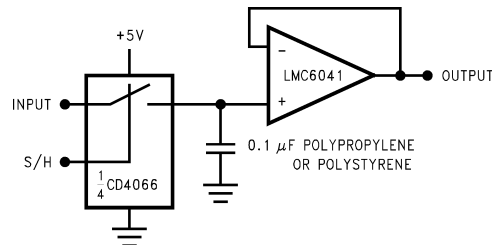


Figure 38. Low-Leakage Sample and Hold

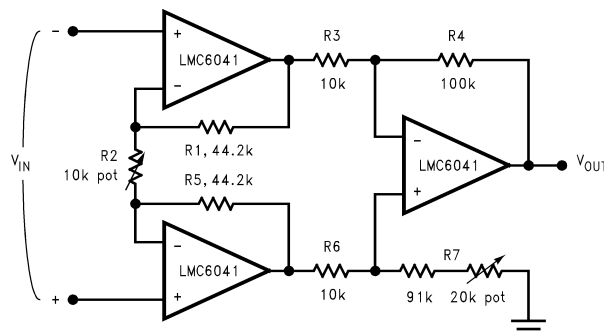


Figure 39. Instrumentation Amplifier

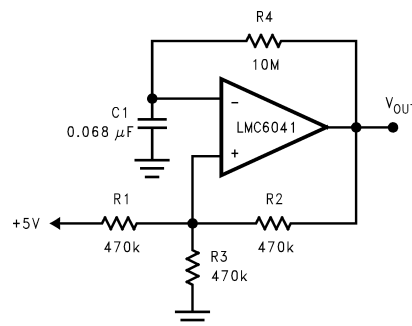


Figure 40. 1 Hz Square-Wave Oscillator

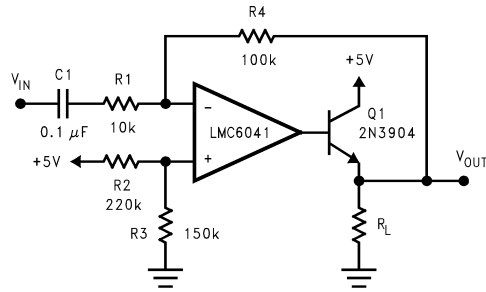


Figure 41. AC Coupled Power Amplifier

### REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format .....	<a href="#">15</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC6041AIM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMC60 41AIM	
LMC6041AIM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC60 41AIM	<a href="#">Samples</a>
LMC6041AIMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC60 41AIM	<a href="#">Samples</a>
LMC6041IM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC60 41IM	<a href="#">Samples</a>
LMC6041IMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC60 41IM	<a href="#">Samples</a>
LMC6041IN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 85	LMC60 41IN	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6041AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6041IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6041AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6041IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

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