# THE DATASHEET OF

# LMC7111BIN

# LMC7111 Tiny CMOS Operational Amplifier with Rail-to-Rail Input and Output

**Check for Samples: LMC7111**

## FEATURES

- **Tiny 5-Pin SOT-23 Package Saves Space**
- **Very Wide Common Mode Input Range**
- **Specified at 2.7V, 5V, and 10V**
- **Typical Supply Current 25 µA at 5V**
- **50 kHz Gain-Bandwidth at 5V**
- **Similar to Popular LMC6462**
- **Output to Within 20 mV of Supply Rail at 100k Load**
- **Good Capacitive Load Drive**

## APPLICATIONS

- **Mobile Communications**
- **Portable Computing**
- **Current Sensing for Battery Chargers**
- **Voltage Reference Buffering**
- **Sensor Interface**
- **Stable Bias for GaAs RF Amps**

## DESCRIPTION

The LMC7111 is a micropower CMOS operational amplifier available in the space saving SOT-23 package. This makes the LMC7111 ideal for space and weight critical designs. The wide common-mode input range makes it easy to design battery monitoring circuits which sense signals above the $V^+$ supply. The main benefits of the Tiny package are most apparent in small portable electronic devices, such as mobile phones, pagers, and portable computers. The tiny amplifiers can be placed on a board where they are needed, simplifying board layout.

## Connection Diagram

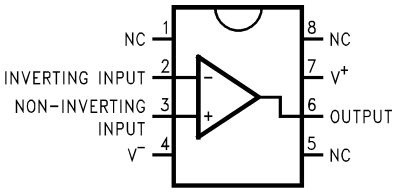



**Figure 1. 8-Pin PDIP**
**Top View**

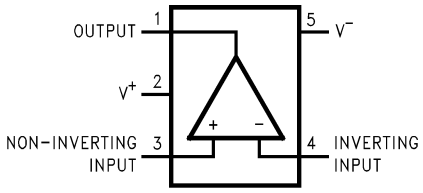



**Figure 2. 5-Pin SOT-23**
**Top View**

**Figure 3. Actual Size**

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings (1)(2)

| | | |
|---|---|---|
| ESD Tolerance (3) | SOT-23 Package | 2000V |
| | PDIP Package | 1500V |
| Differential Input Voltage | | ±Supply Voltage |
| Voltage at Input/Output Pin | | $(V^+)$ + 0.3V, $(V^-)$ − 0.3V |
| Supply Voltage $(V^+ - V^-)$ | | 11V |
| Current at Input Pin | | ±5 mA |
| Current at Output Pin (4) | | ±30 mA |
| Current at Power Supply Pin | | 30 mA |
| Lead Temp. (Soldering, 10 sec.) | | 260°C |
| Storage Temperature Range | | −65°C to +150°C |
| Junction Temperature (5) | | 150°C |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Human Body Model is 1.5 kΩ in series with 100 pF.
(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $\theta_{JA}$ and $T_A$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

## Operating Ratings (1)

| | | |
|---|---|---|
| Supply Voltage | | $2.5V \le V^+ \le 11V$ |
| Junction Temperature Range | LMC7111AI, LMC7111BI | $-40°C \le T_J \le +85°C$ |
| Thermal Resistance ($\theta_{JA}$) | 8-Pin PDIP | 115°C/W |
| | 5-Pin SOT-23 | 325°C/W |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not specified. For ensured specifications and the test conditions, see the Electrical Characteristics.

## 2.7V DC Electrical Characteristics

Unless otherwise specified, all limits specified for $T_J$ = 25°C, $V^+$ = 2.7V, $V^-$ = 0V, $V_{CM} = V_O = V^+/2$ and $R_L$ > 1 MΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (1) | LMC7111AI Limit (2) | LMC7111BI Limit (2) | Units |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | $V^+$ = 2.7V | 0.9 | 3 | 7 | mV |
| | | | | **5** | **9** | max |
| $TCV_{OS}$ | Input Offset Voltage Average Drift | | 2.0 | | | µV/°C |
| $I_B$ | Input Bias Current | See (3) | 0.1 | 1<br>**20** | 1<br>**20** | pA<br>max |
| $I_{OS}$ | Input Offset Current | See (3) | 0.01 | 0.5<br>**10** | 0.5<br>**10** | pA<br>max |
| $R_{IN}$ | Input Resistance | | >10 | | | Tera Ω |
| +PSRR | Positive Power Supply Rejection Ratio | $2.7V \le V^+ \le 5.0V$, $V^- = 0V$, $V_O = 2.5V$ | 60 | 55<br>**50** | 55<br>**50** | dB<br>min |
| −PSRR | Negative Power Supply Rejection Ratio | $-2.7V \le V^- \le -5.0V$, $V^- = 0V$, $V_O = 2.5V$ | 60 | 55<br>**50** | 55<br>**50** | dB<br>min |

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) Bias Current specified by design and processing.

## 2.7V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits specified for $T_J$ = 25°C, $V^+$ = 2.7V, $V^-$ = 0V, $V_{CM} = V_O = V^+/2$ and $R_L$ > 1 MΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (1) | LMC7111AI Limit(2) | LMC7111BI Limit(2) | Units |
|---|---|---|---|---|---|---|
| $V_{CM}$ | Input Common-Mode Voltage Range | $V^+$ = 2.7V<br>For CMRR ≥ 50 dB | −0.10 | 0.0<br>**0.40** | 0.0<br>**0.40** | V<br>min |
| | | | 2.8 | 2.7<br>**2.25** | 2.7<br>**2.25** | V<br>max |
| $C_{IN}$ | Common-Mode Input Capacitance | | 3 | | | pF |
| $V_O$ | Output Swing | $V^+$ = 2.7V<br>$R_L$ = 100 kΩ | 2.69 | 2.68<br>**2.4** | 2.68<br>**2.4** | V<br>min |
| | | | 0.01 | 0.02<br>**0.08** | 0.02<br>**0.08** | V<br>max |
| | | $V^+$ = 2.7V<br>$R_L$ = 10 kΩ | 2.65 | 2.6<br>**2.4** | 2.6<br>**2.4** | V<br>min |
| | | | 0.03 | 0.1<br>**0.3** | 0.1<br>**0.3** | V<br>max |
| $I_{SC}$ | Output Short Circuit Current | Sourcing, $V_O$ = 0V | 7 | 1<br>**0.7** | 1<br>**0.7** | mA<br>min |
| | | Sinking, $V_O$ = 2.7V | 7 | 1<br>**0.7** | 1<br>**0.7** | mA<br>min |
| $A_{VOL}$ | Voltage Gain | Sourcing | 400 | | | V/mv<br>min |
| | | Sinking | 150 | | | V/mv<br>min |
| $I_S$ | Supply Current | $V^+$ = +2.7V,<br>$V_O = V^+/2$ | 20 | 45<br>**60** | 50<br>**65** | µA<br>max |

## 2.7V AC Electrical Characteristics

Unless otherwise specified, all limits specified for $T_J$ = 25°C, $V^+$ = 2.7V, $V^-$ = 0V, $V_{CM} = V_O = V^+/2$ and $R_L$ > 1 MΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (1) | LMC7111AI Limit (2) | LMC7111BI Limit(2) | Units |
|---|---|---|---|---|---|---|
| SR | Slew Rate | See (3) | 0.015 | | | V/µs |
| GBW | Gain-Bandwidth Product | | 40 | | | kHz |

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) Connected as Voltage Follower with 1.0V step input. Number specified is the slower of the positive and negative slew rates. Input referred, $V^+$ = 2.7V and $R_L$ = 100 kΩ connected to 1.35V. Amp excited with 1 kHz to produce $V_O$ = 1 $V_{PP}$.

## 3V DC Electrical Characteristics

Unless otherwise specified, all limits specified for $T_J$ = 25°C, $V^+$ = 3V, $V^-$ = 0V, $V_{CM} = V_O = V^+/2$ and $R_L$ > 1 MΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (1) | LMC7111AI Limit(2) | LMC7111BI Limit(2) | Units |
|---|---|---|---|---|---|---|
| $V_{CM}$ | Input Common-Mode Voltage Range | $V^+$ = 3V<br>For CMRR ≥ 50 dB | −0.25 | 0.0 | 0.0 | V<br>min |
| | | | 3.2 | 3.0<br>**2.8** | 3.0<br>**2.8** | V<br>max |

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.

## 3.3V DC Electrical Characteristics

Unless otherwise specified, all limits specified for $T_J$ = 25°C, $V^+$ = 3.3V, $V^-$ = 0V, $V_{CM} = V_O = V^+/2$ and $R_L$ > 1 MΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (1) | LMC7111AI Limit (2) | LMC7111BI Limit (2) | Units |
|---|---|---|---|---|---|---|
| $V_{CM}$ | Input Common-Mode Voltage Range | $V^+$ = 3.3V For CMRR ≥ 50 dB | −0.25 | −0.1 **0.00** | −0.1 **0.00** | V min |
| | | | 3.5 | 3.4 **3.2** | 3.4 **3.2** | V max |

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.

## 5V DC Electrical Characteristics

Unless otherwise specified, all limits specified for $T_J$ = 25°C, $V^+$ = 5V, $V^-$ = 0V, $V_{CM} = V_O = V^+/2$ and $R_L$ > 1 MΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (1) | LMC7111AI Limit(2) | LMC7111BI Limit(2) | Units |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | $V^+$ = 5V | 0.9 | | | mV max |
| $TCV_{OS}$ | Input Offset Voltage Average Drift | | 2.0 | | | µV/°C |
| $I_B$ | Input Bias Current | See (3) | 0.1 | 1 **20** | 1 **20** | pA max |
| $I_{OS}$ | Input Offset Current | See (3) | 0.01 | 0.5 **10** | 0.5 **10** | pA max |
| $R_{IN}$ | Input Resistance | | >10 | | | Tera Ω |
| CMRR | Common Mode Rejection Ratio | 0V ≤ $V_{CM}$ ≤ 5V | 85 | 70 | 60 | dB min |
| +PSRR | Positive Power Supply Rejection Ratio | 5V ≤ $V^+$ ≤10V, $V^-$ = 0V, $V_O$ = 2.5V | 85 | 70 | 60 | dB min |
| −PSRR | Negative Power Supply Rejection Ratio | −5V ≤ $V^-$ ≤−10V, $V^-$ = 0V, $V_O$ = −2.5V | 85 | 70 | 60 | dB min |
| $V_{CM}$ | Input Common-Mode Voltage Range | $V^+$ = 5V For CMRR ≥ 50 dB | −0.3 | −0.20 **0.00** | −0.20 **0.00** | V min |
| | | | 5.25 | 5.20 **5.00** | 5.20 **5.00** | V max |
| $C_{IN}$ | Common-Mode Input Capacitance | | 3 | | | pF |
| $V_O$ | Output Swing | $V^+$ = 5V $R_L$ = 100 kΩ | 4.99 | 4.98 | 4.98 | Vmin |
| | | | 0.01 | 0.02 | 0.02 | Vmax |
| | | $V^+$ = 5V $R_L$ = 10 kΩ | 4.98 | 4.9 | 4.9 | Vmin |
| | | | 0.02 | 0.1 | 0.1 | Vmin |
| $I_{SC}$ | Output Short Circuit Current | Sourcing, $V_O$ = 0V | 7 | 5 **3.5** | 5 **3.5** | mA min |
| | | Sinking, $V_O$ = 3V | 7 | 5 **3.5** | 5 **3.5** | mA min |
| $A_{VOL}$ | Voltage Gain | Sourcing | 500 | | | V/mv min |
| | | Sinking | 200 | | | V/mv min |
| $I_S$ | Supply Current | $V^+$ = +5V, $V_O = V^+/2$ | 25 | | | µA max |

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) Bias Current specified by design and processing.

## 5V AC Electrical Characteristics

Unless otherwise specified, all limits specified for $T_J$ = 25°C, $V^+$ = 5V, $V^-$ = 0V, $V_{CM}$ = $V_O$ = $V^+$/2 and $R_L$ > 1 MΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (1) | LMC7111AI Limit(2) | LMC7111BI Limit(2) | Units |
|---|---|---|---|---|---|---|
| SR | Slew Rate | Positive Going Slew Rate(3) | 0.027 | 0.015 | 0.010 | V/µs |
| GBW | Gain-Bandwidth Product | | 50 | | | kHz |

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) Connected as Voltage Follower with 1.0V step input. Number specified is the slower of the positive slew rate. The negative slew rate is faster. Input referred, $V^+$ = 5V and $R_L$ = 100 kΩ connected to 1.5V. Amp excited with 1 kHz to produce $V_O$ = 1 $V_{PP}$.

## 10V DC Electrical Characteristics

Unless otherwise specified, all limits specified for $T_J$ = 25°C, $V^+$ = 10V, $V^-$ = 0V, $V_{CM}$ = $V_O$ = $V^+$/2 and $R_L$ > 1 MΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (1) | LMC7111AI Limit (2) | LMC7111BI Limit(2) | Units |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | $V^+$ = 10V | 0.9 | 3<br>**5** | 7<br>**9** | mV<br>max |
| $TCV_{OS}$ | Input Offset Voltage Average Drift | | 2.0 | | | µV/°C |
| $I_B$ | Input Bias Current | | 0.1 | 1<br>**20** | 1<br>**20** | pA<br>max |
| $I_{OS}$ | Input Offset Current | | 0.01 | 0.5<br>**10** | 0.5<br>**10** | pA<br>max |
| $R_{IN}$ | Input Resistance | | >10 | | | Tera Ω |
| +PSRR | Positive Power Supply Rejection Ratio | 5V ≤ $V^+$ ≤10V, $V^-$ = 0V, $V_O$ = 2.5V | 80 | | | dB<br>min |
| −PSRR | Negative Power Supply Rejection Ratio | −5V ≤ $V^-$ ≤−10V, $V^-$ = 0V, $V_O$ = 2.5V | 80 | | | dB<br>min |
| $V_{CM}$ | Input Common-Mode Voltage Range | $V^+$ = 10V<br>For CMRR ≥ 50 dB | −0.2 | −0.15<br>**0.00** | −0.15<br>**0.00** | V<br>min |
| | | | 10.2 | 10.15<br>**10.00** | 10.15<br>**10.00** | V<br>max |
| $C_{IN}$ | Common-Mode Input Capacitance | | 3 | | | pF |
| $I_{SC}$ | Output Short Circuit Current (3) | Sourcing, $V_O$ = 0V | 30 | 20<br>**7** | 20<br>**7** | mA<br>min |
| | | Sinking, $V_O$ = 10V | 30 | 20<br>**7** | 20<br>**7** | mA<br>min |
| $A_{VOL}$ | Voltage Gain 100 kΩ Load | Sourcing | 500 | | | V/mv<br>min |
| | | Sinking | 200 | | | V/mv<br>min |
| $I_S$ | Supply Current | $V^+$ = +10V, $V_O$ = $V^+$/2 | 25 | 50<br>**65** | 60<br>**75** | µA<br>max |
| $V_O$ | Output Swing | $V^+$ = 10V<br>$R_L$ = 100 kΩ | 9.99 | 9.98 | 9.98 | Vmin |
| | | | 0.01 | 0.02 | 0.02 | Vmax |
| | | $V^+$ = 10V<br>$R_L$ = 10 kΩ | 9.98 | 9.9 | 9.9 | Vmin |
| | | | 0.02 | 0.1 | 0.1 | Vmin |

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) Bias Current specified by design and processing.

## 10V AC Electrical Characteristics

Unless otherwise specified, all limits specified for $T_J$ = 25°C, $V^+$ = 10V, $V^-$ = 0V, $V_{CM} = V_O = V^+/2$ and $R_L$ > 1 MΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (1) | LMC7111AI Limit (2) | LMC7111BI Limit (2) | Units |
|---|---|---|---|---|---|---|
| SR | Slew Rate | See (3) | 0.03 | | | V/µs |
| GBW | Gain-Bandwidth Product | | 50 | | | kHz |
| $\varphi_m$ | Phase Margin | | 50 | | | deg |
| $G_m$ | Gain Margin | | 15 | | | dB |
| | Input-Referred Voltage Noise | f = 1 kHz $V_{CM}$ = 1V | 110 | | | nV/ $\sqrt{Hz}$ |
| | Input-Referred Current Noise | f = 1 kHz | 0.03 | | | pA/$\sqrt{Hz}$ |

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) Connected as Voltage Follower with 1.0V step input. Number specified is the slower of the positive and negative slew rates. Input referred, $V^+$ = 10V and $R_L$ = 100 kΩ connected to 5V. Amp excited with 1 kHz to produce $V_O = 2\ V_{PP}$.

## Typical Performance Characteristics

$T_A$ = 25°C unless specified, Single Supply

**Supply Current vs. Supply Voltage**

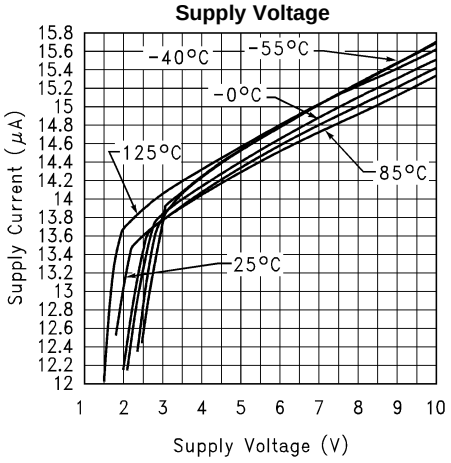



**Figure 4.**

**Voltage Noise vs. Frequency**

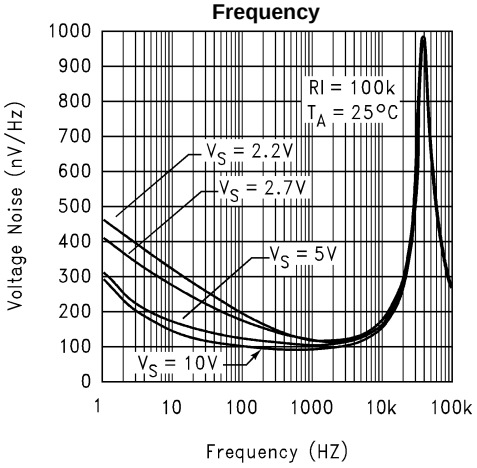



**Figure 5.**

## 2.7V Performance

**Offset Voltage vs. Common Mode Voltage @ 2.7V**

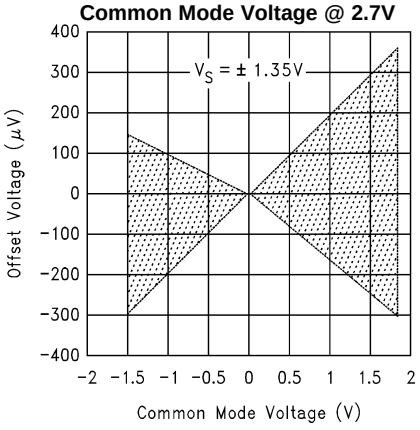



**Figure 6.**

**Sinking Output vs. Output Voltage**

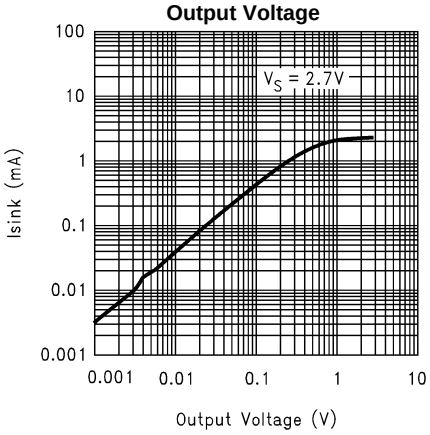



**Figure 7.**

**Sourcing Output vs. Output Voltage**

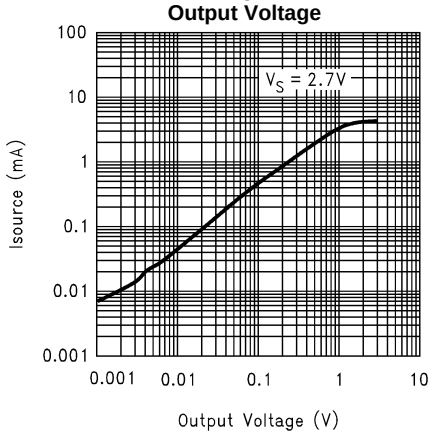



**Figure 8.**

**Gain and Phase vs. Capacitive Load @ 2.7V**

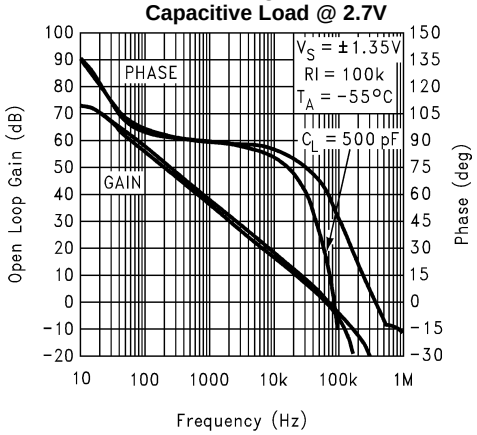



**Figure 9.**

## 2.7V Performance (continued)

**Gain and Phase vs. Capacitive Load @ 2.7V**

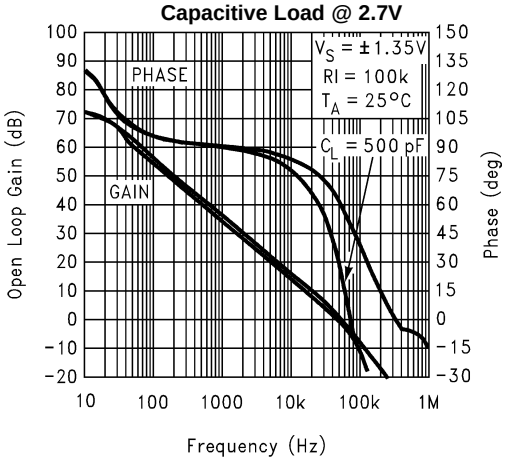



**Figure 10.**

**Gain and Phase vs. Capacitive Load @ 2.7V**

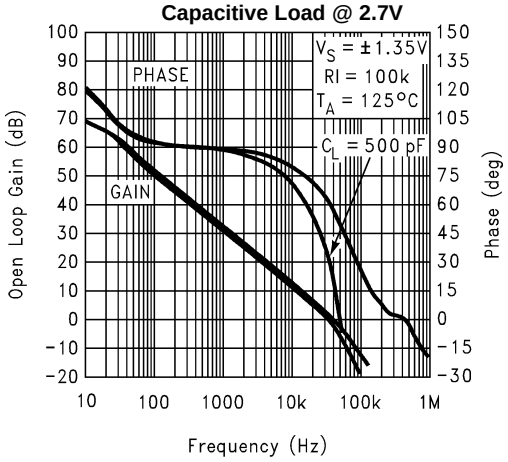



**Figure 11.**

## 3V Performance

**Voltage Noise vs. Common Mode Voltage @ 3V**

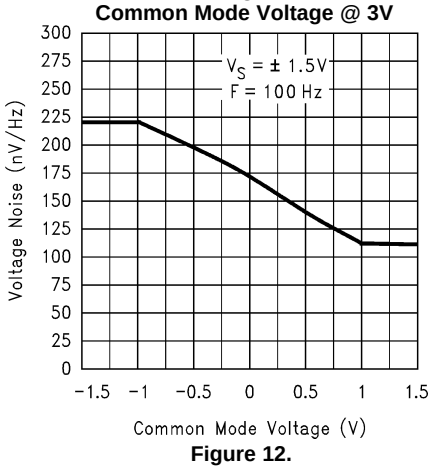



**Figure 12.**

**Output Voltage vs. Input Voltage @ 3V**

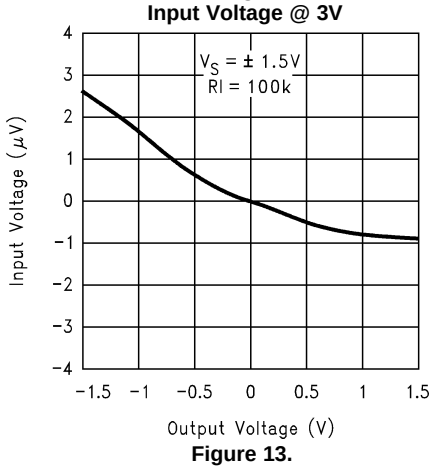



**Figure 13.**

**Offset Voltage vs. Common Mode Voltage @ 3V**

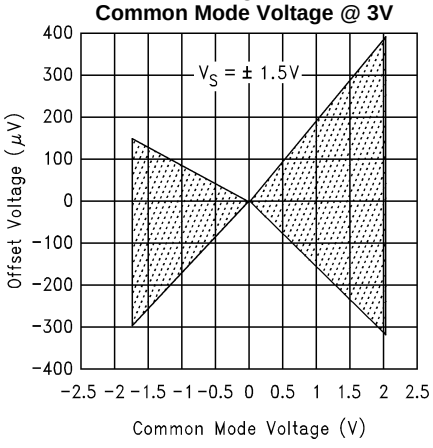



**Figure 14.**

**Sourcing Output vs. Output Voltage**

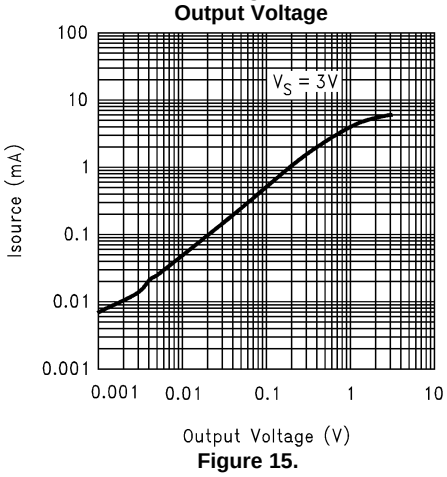



**Figure 15.**

## 3V Performance (continued)

**Sinking Output vs. Output Voltage**

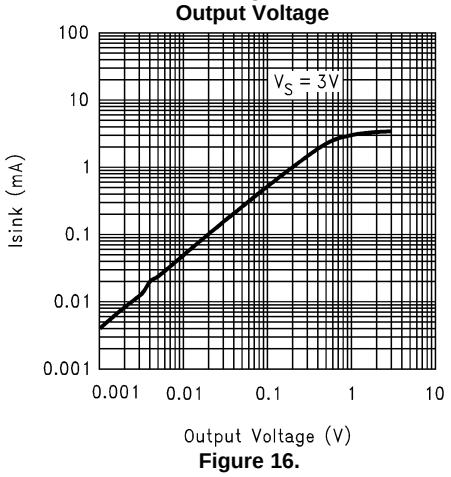



**Figure 16.**

**Gain and Phase vs. Capacitive Load @ 3V**

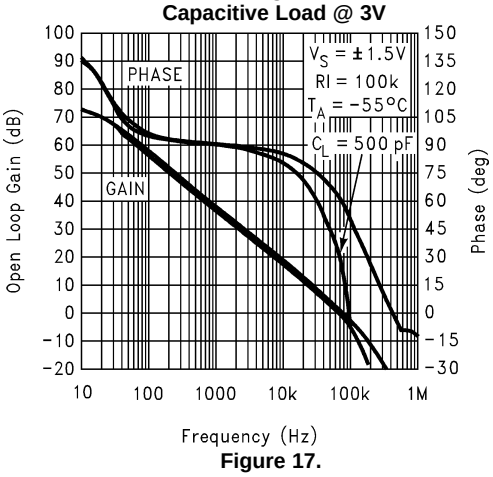



**Figure 17.**

**Gain and Phase vs. Capacitive Load @ 3V**

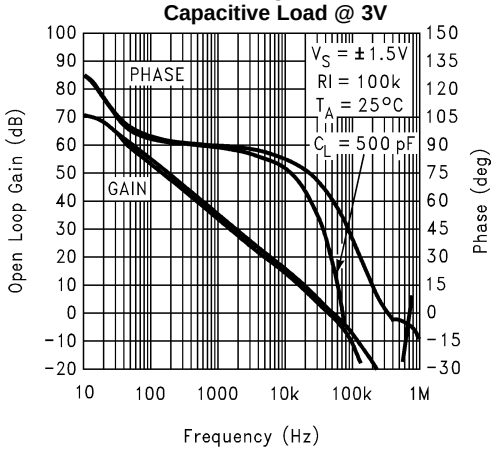



**Figure 18.**

**Gain and Phase vs. Capacitive Load @ 3V**

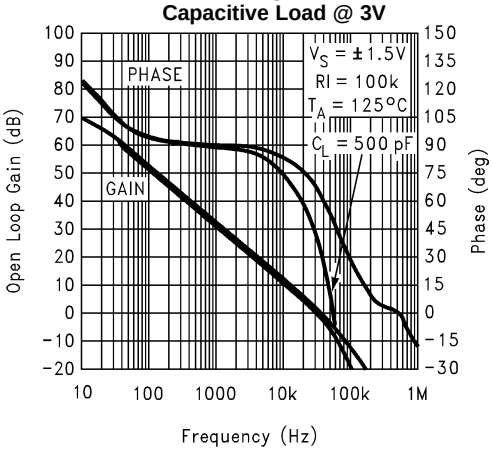



**Figure 19.**

## 5V Performance

**Voltage Noise vs. Common Mode Voltage @ 5V**

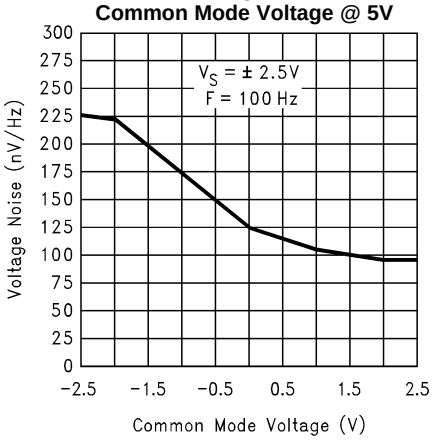



**Figure 20.**

**Output Voltage vs. Input Voltage @ 5V**

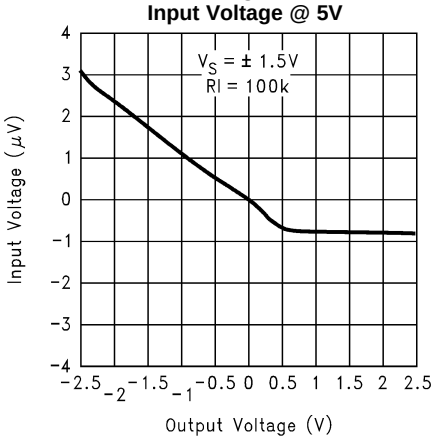



**Figure 21.**

## 5V Performance (continued)

**Offset Voltage vs. Common Mode Voltage @ 5V**

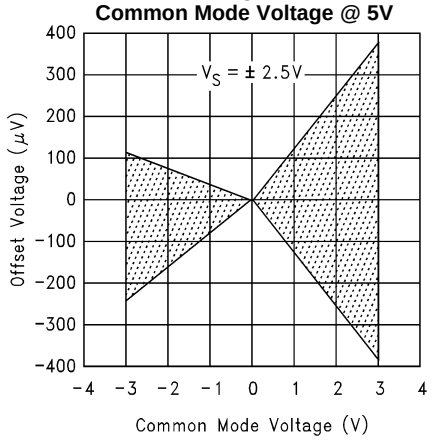



**Figure 22.**

**Sourcing Output vs. Output Voltage**

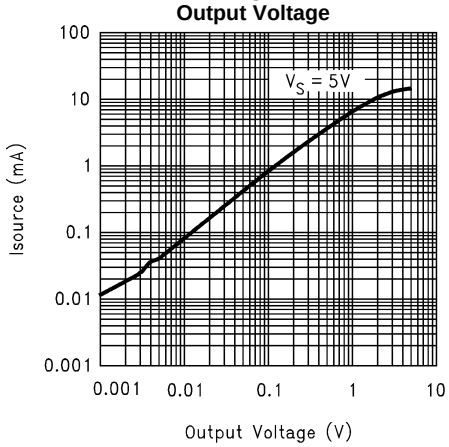



**Figure 23.**

**Sinking Output vs. Output Voltage**

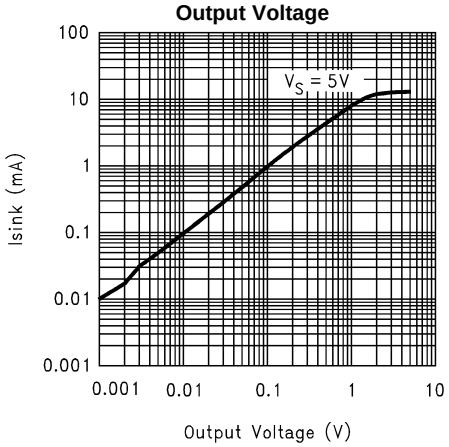



**Figure 24.**

**Gain and Phase vs. Capacitive Load @ 5V**

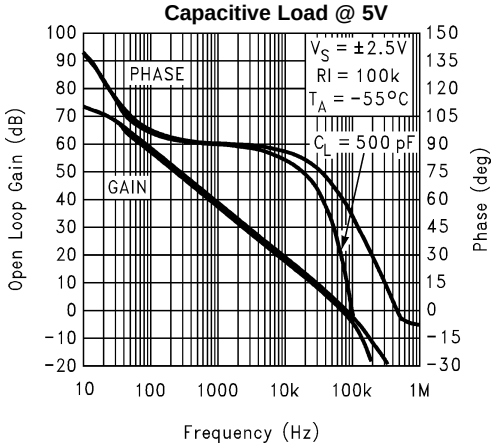



**Figure 25.**

**Gain and Phase vs. Capacitive Load @ 5V**

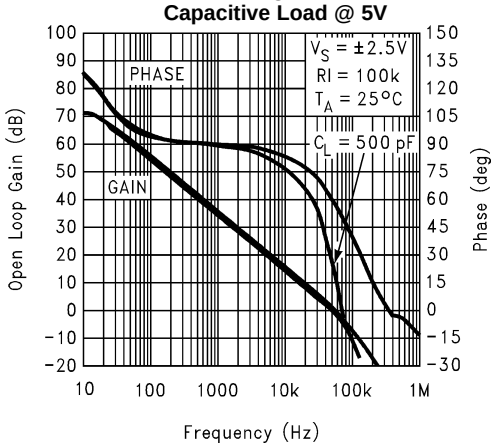



**Figure 26.**

**Gain and Phase vs. Capacitive Load @ 5V**

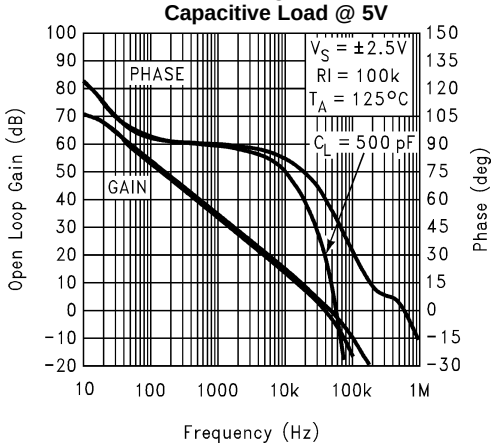



**Figure 27.**

## 5V Performance (continued)

**Non-Inverting Small Signal Pulse Response at 5V**

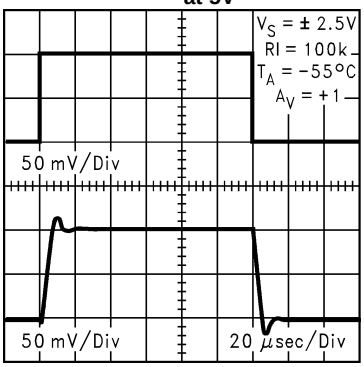



**Figure 28.**

**Non-Inverting Small Signal Pulse Response at 5V**

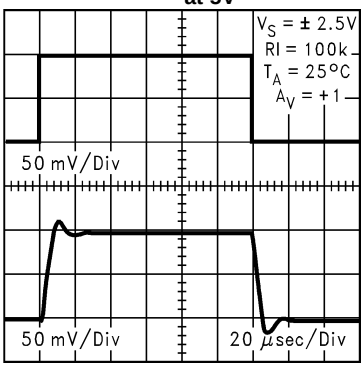



**Figure 29.**

**Non-Inverting Small Signal Pulse Response at 5V**

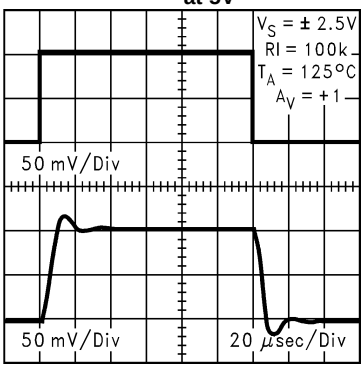



**Figure 30.**

**Non-Inverting Large Signal Pulse Response at 5V**

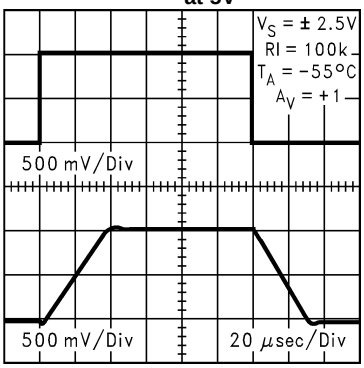



**Figure 31.**

**Non-Inverting Large Signal Pulse Response at 5V**

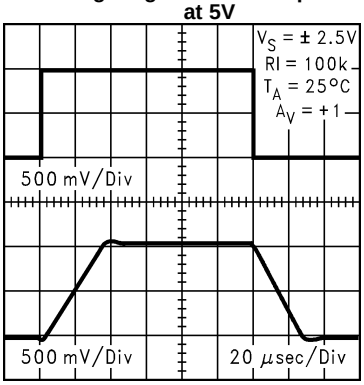



**Figure 32.**

**Non-Inverting Large Signal Pulse Response at 5V**

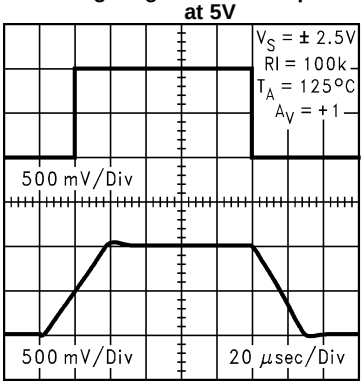



**Figure 33.**

## 5V Performance (continued)

**Inverting Small Signal Pulse Response at 5V**

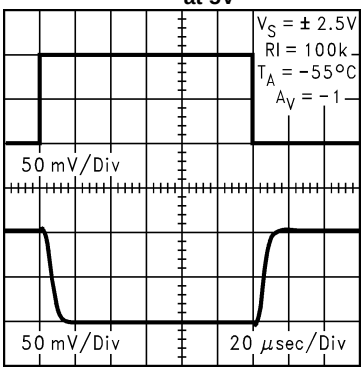



**Figure 34.**

**Inverting Small Signal Pulse Response at 5V**

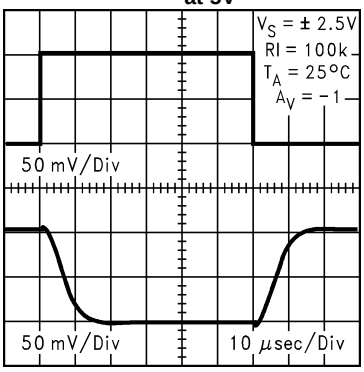



**Figure 35.**

**Inverting Small Signal Pulse Response at 5V**

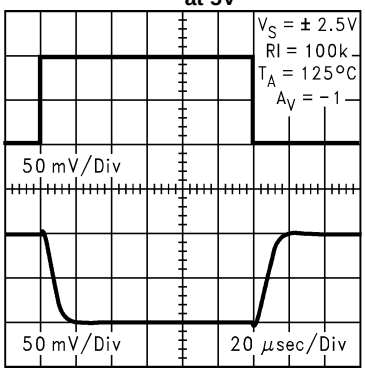



**Figure 36.**

**Inverting Large Signal Pulse Response at 5V**

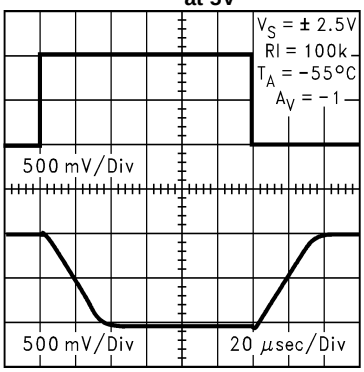



**Figure 37.**

**Inverting Large Signal Pulse Response at 5V**

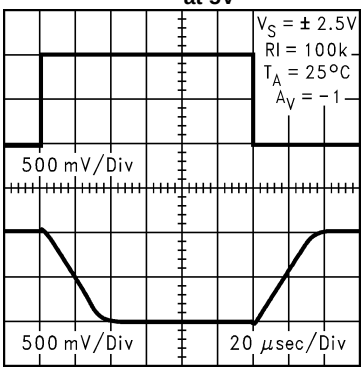



**Figure 38.**

**Inverting Large Signal Pulse Response at 5V**

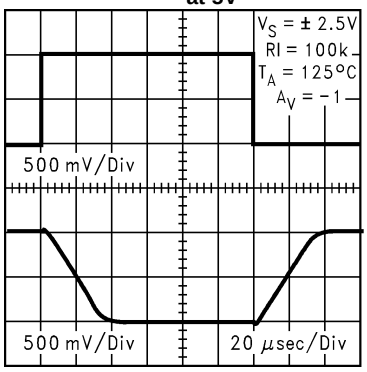



**Figure 39.**

## 10V Performance

**Voltage Noise vs. Common Mode Voltage @ 10V**

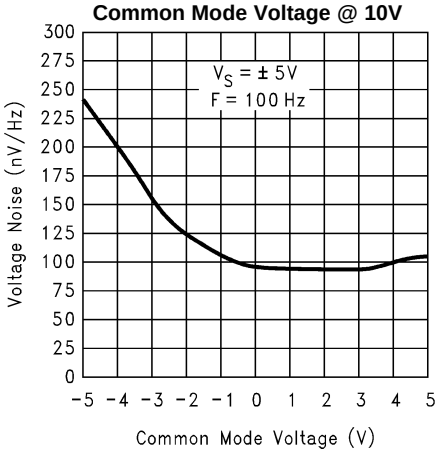



**Figure 40.**

**Output Voltage vs. Input Voltage @ 10V**

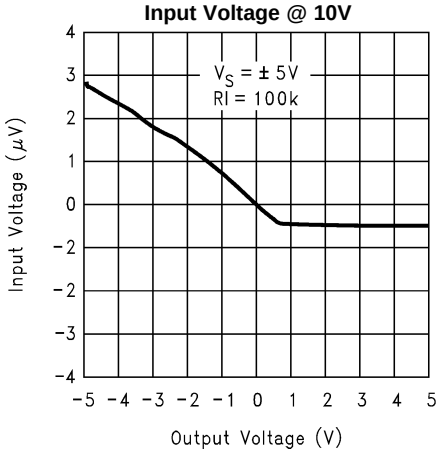



**Figure 41.**

**Offset Voltage vs. Common Mode Voltage @ 10V**

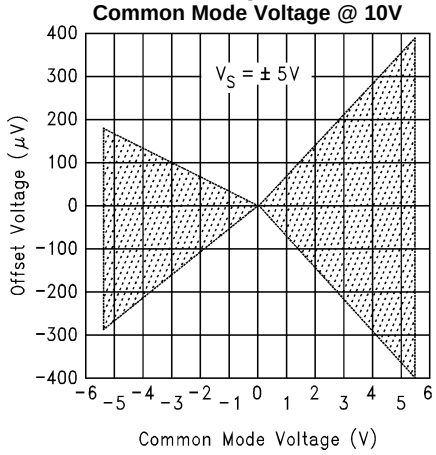



**Figure 42.**

**Sourcing Output vs. Output Voltage**

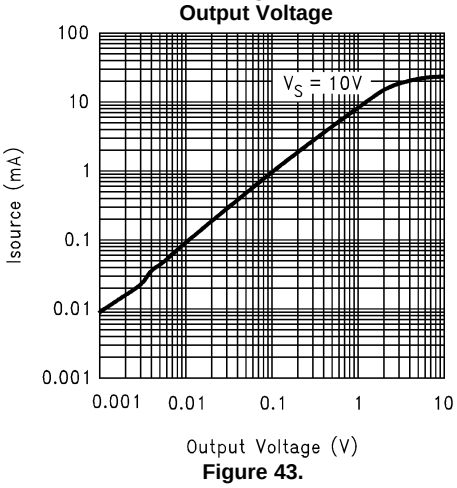



**Figure 43.**

**Sinking Output vs. Output Voltage**

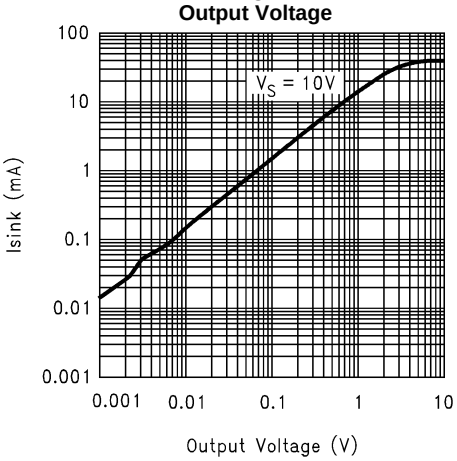



**Figure 44.**

**Gain and Phase vs. Capacitive Load @ 10V**

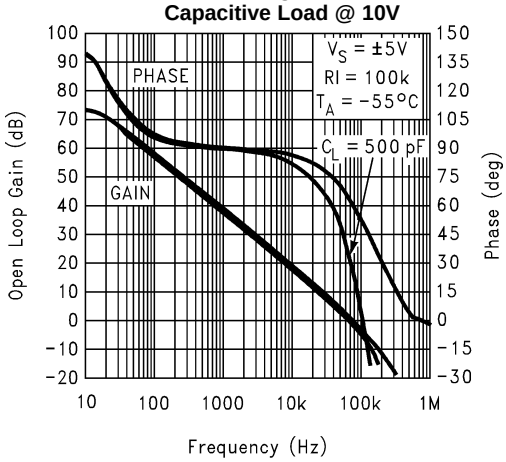



**Figure 45.**

## 10V Performance (continued)

**Gain and Phase vs. Capacitive Load @ 10V**

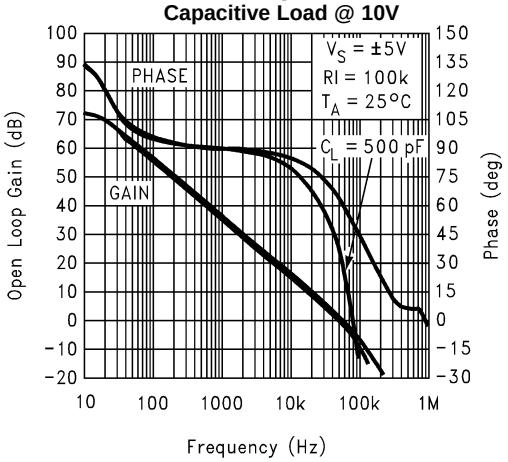



**Figure 46.**

**Gain and Phase vs. Capacitive Load @ 10V**

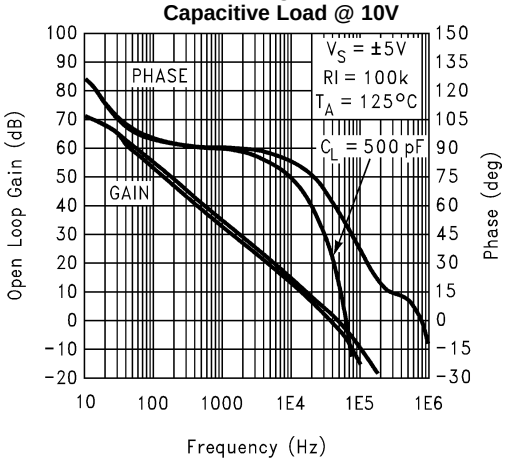



**Figure 47.**

**Non-Inverting Small Signal Pulse Response at 10V**

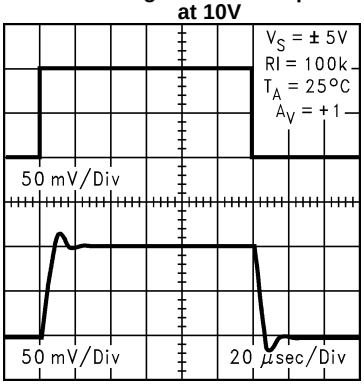



**Figure 48.**

**Non-Inverting Large Signal Pulse Response at 10V**

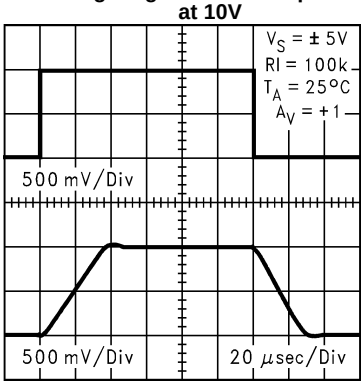



**Figure 49.**

**Inverting Small Signal Pulse Response at 10V**

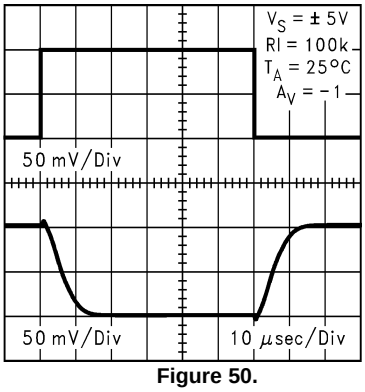



**Figure 50.**

**Inverting Large Signal Pulse Response at 10V**

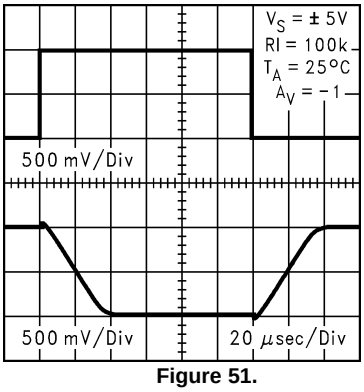



**Figure 51.**

# APPLICATION INFORMATION

## BENEFITS OF THE LMC7111 TINY AMP

### Size

The small footprint of the SOT-23 packaged Tiny amp, (0.120 x 0.118 inches, 3.05 x 3.00 mm) saves space on printed circuit boards, and enable the design of smaller electronic products. Because they are easier to carry, many customers prefer smaller and lighter products.

### Height

The height (0.056 inches, 1.43 mm) of the Tiny amp makes it possible to use it in PCMCIA type III cards.

### Signal Integrity

Signals can pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, the Tiny amp can be placed closer to the signal source, reducing noise pickup and increasing signal integrity. The Tiny amp can also be placed next to the signal destination, such as a buffer for the reference of an analog to digital converter.

### Simplified Board Layout

The Tiny amp can simplify board layout in several ways. First, by placing an amp where amps are needed, instead of routing signals to a dual or quad device, long pc traces may be avoided.

By using multiple Tiny amps instead of duals or quads, complex signal routing and possibly crosstalk can be reduced.

### DIPs available for prototyping

LMC7111 amplifiers packaged in conventional 8-pin dip packages can be used for prototyping and evaluation without the need to use surface mounting in early project stages.

### Low Supply Current

The typical 25 µA supply current of the LMC7111 extends battery life in portable applications, and may allow the reduction of the size of batteries in some applications.

### Wide Voltage Range

The LMC7111 is characterized at 2.7V, 3V, 3.3V, 5V and 10V. Performance data is provided at these popular voltages. This wide voltage range makes the LMC7111 a good choice for devices where the voltage may vary over the life of the batteries.

## INPUT COMMON MODE VOLTAGE RANGE

The LMC7111 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage.

The absolute maximum input voltage is 300 mV beyond either rail at room temperature. Voltages greatly exceeding this maximum rating can cause excessive current to flow in or out of the input pins, adversely affecting reliability.

Applications that exceed this rating must externally limit the maximum input current to ±5 mA with an input resistor as shown in Figure 52.

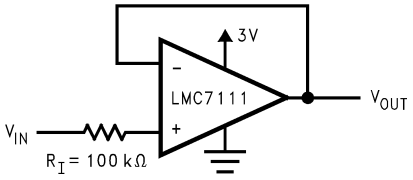



**Figure 52. $R_I$ Input Current Protection for Voltages Exceeding the Supply Voltage**

## CAPACITIVE LOAD TOLERANCE

The LMC7111 can typically directly drive a 300 pF load with $V_S$ = 10V at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in Figure 53. This simple technique is useful for isolating the capacitive input of multiplexers and A/D converters.

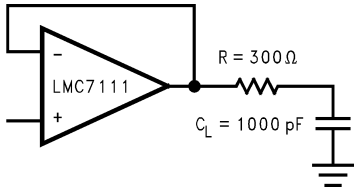



**Figure 53. Resistive Isolation of a 330 pF Capacitive Load**

## COMPENSATING FOR INPUT CAPACITANCE WHEN USING LARGE VALUE FEEDBACK RESISTORS

When using very large value feedback resistors, (usually > 500 kΩ) the large feed back resistance can react with the input capacitance due to transducers, photodiodes, and circuit board parasitics to reduce phase margins.

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in Figure 54), $C_f$ is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \quad (1)$$

or

$$R_1 C_{IN} \leq R_2 C_f \quad (2)$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a breadboard, so the actual optimum value for $C_F$ may be different. The values of $C_F$ should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

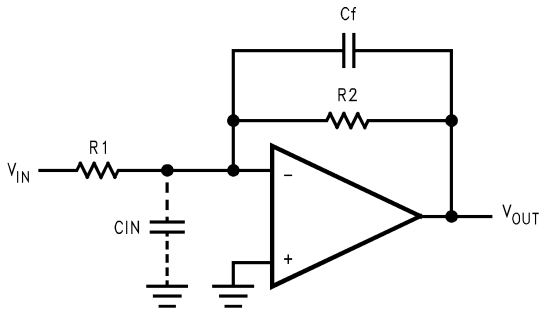



**Figure 54. Cancelling the Effect of Input Capacitance**

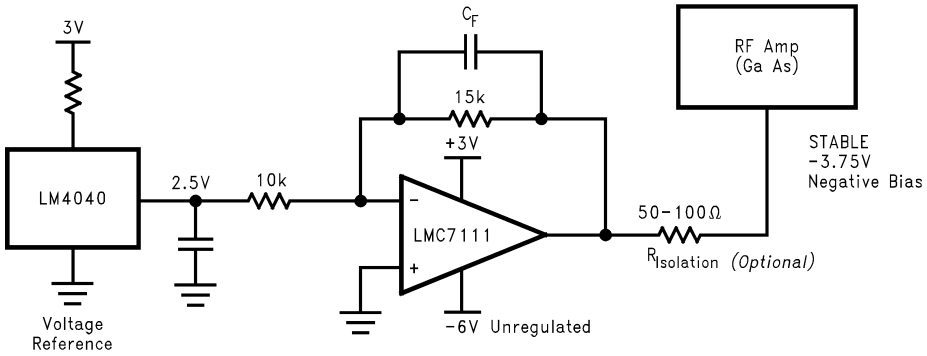
## OUTPUT SWING

The output of the LMC7111 will go to within 100 mV of either power supply rail for a 10 kΩ load and to 20 mV of the rail for a 100 kΩ load. This makes the LMC7111 useful for driving transistors which are connected to the same power supply. By going very close to the supply, the LMC7111 can turn the transistors all the way on or all the way off.

## BIASING GaAs RF AMPLIFIERS

The capacitive load capability, low current draw, and small size of the SOT-23 LMC7111 make it a good choice for providing a stable negative bias to other integrated circuits.

The very small size of the LMC7111 and the LM4040 reference take up very little board space.




$C_F$ and $R_{isolation}$ prevent oscillations when driving capacitive loads.

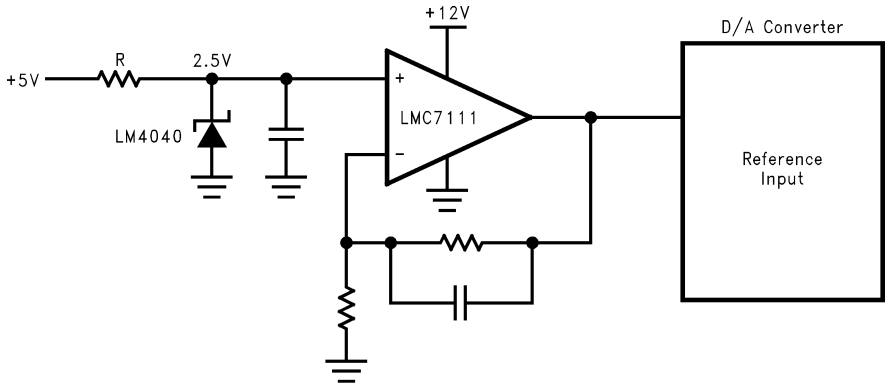
**Figure 55. Stable Negative Bias**

## REFERENCE BUFFER FOR A-TO-D CONVERTERS

The LMC7111 can be used as a voltage reference buffer for analog-to-digital converters. This works best for A-to-D converters whose reference input is a static load, such as dual slope integrating A-to-Ds. Converters whose reference input is a dynamic load (the reference current changes with time) may need a faster device, such as the LMC7101 or the LMC7131.

The small size of the LMC7111 allows it to be placed close to the reference input. The low supply current (25 µA typical) saves power.

For A-to-D reference inputs which require higher accuracy and lower offset voltage, please see the LMC6462 datasheet. The LMC6462 has performance similar to the LMC7111. The LMC6462 is available in two grades with reduced input voltage offset.




## DUAL AND QUAD DEVICES WITH SIMILAR PERFORMANCE

The LMC6462 and LMC6464 are dual and quad devices with performance similar to the LMC7111. They are available in both conventional through-hole and surface mount packaging. Please see the LMC6462/4 datasheet for details.

## SPICE MACROMODEL

A SPICE macromodel is available for the LMC7111. This model includes simulation of:

- Input common-mode voltage range
- Frequency and transient response

- Quiescent and dynamic supply current
- Output swing dependence on loading conditions and many more characteristics as listed on the macro model disk. Visit the LMC7111 product page on http://www.ti.com for the spice model.

## ADDITIONAL SOT-23 TINY DEVICES

Additional parts are available in the space saving SOT-23 Tiny package, including amplifiers, voltage references, and voltage regulators. These devices include—

**LMC7101** 1 MHz gain-bandwidth rail-to-rail input and output amplifier—high input impedance and high gain, 700 µA typical current 2.7V, 3V, 5V and 15V specifications.

**LM7131** Tiny Video amp with 70 MHz gain bandwidth. Specified at 3V, 5V and ± 5V supplies.

**LMC7211** Comparator in a tiny package with rail-to-rail input and push-pull output. Typical supply current of 7 µA. Typical propagation delay of 7 µs. Specified at 2.7V, 5V and 15V supplies.

**LMC7221** Comparator with an open drain output for use in mixed voltage systems. Similar to the LMC7211, except the output can be used with a pull-up resistor to a voltage different than the supply voltage.

**LP2980** Micropower SOT 50 mA Ultra Low-Dropout Regulator.

**LM4040** Precision micropower shunt voltage reference. Fixed voltages of 2.5000V, 4.096V, 5.000V, 8.192V and 10.000V.

**LM4041** Precision micropower shunt voltage reference 1.225V and adjustable.

Visit http://www.ti.com for more information.

## REVISION HISTORY

| Changes from Revision D (March 2013) to Revision E | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 18 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LMC7111BIM5 | NRND | SOT-23 | DBV | 5 | 1000 | TBD | Call TI | Call TI | -40 to 85 | A01B | |
| LMC7111BIM5/NOPB | ACTIVE | SOT-23 | DBV | 5 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | A01B | Samples |
| LMC7111BIM5X | NRND | SOT-23 | DBV | 5 | 3000 | TBD | Call TI | Call TI | -40 to 85 | A01B | |
| LMC7111BIM5X/NOPB | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | A01B | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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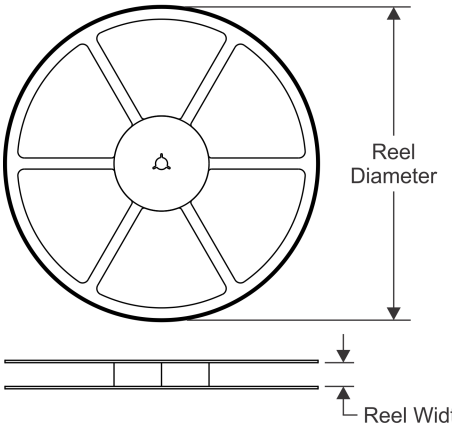
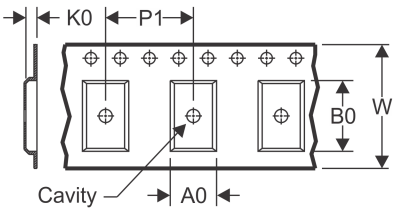
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

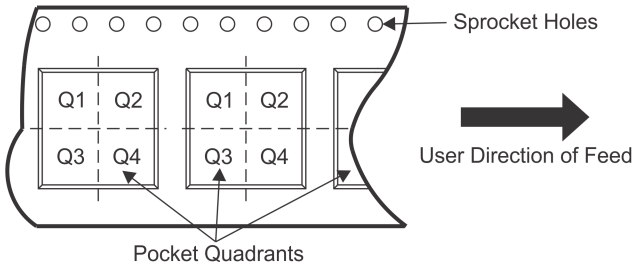



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

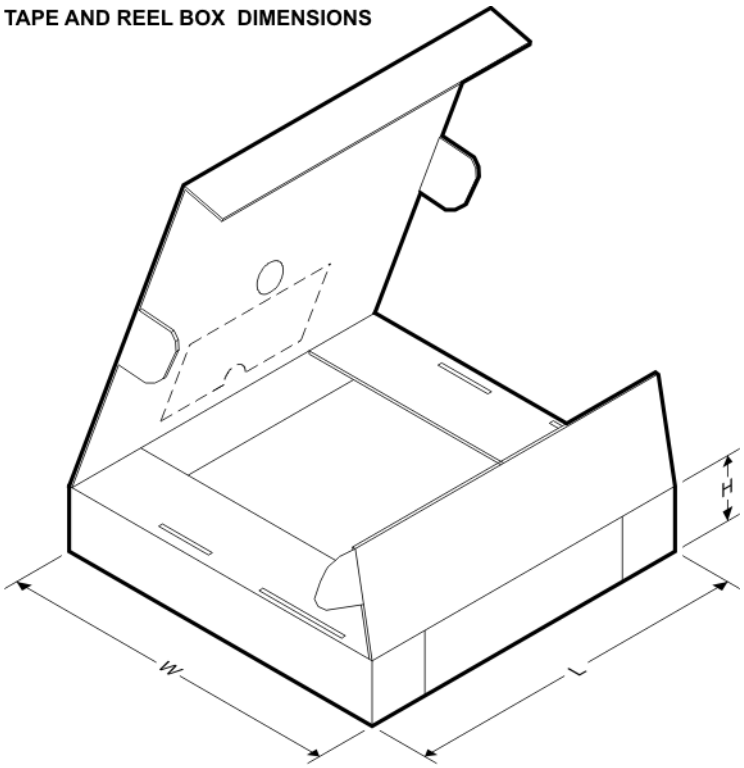
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LMC7111BIM5 | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LMC7111BIM5/NOPB | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LMC7111BIM5X | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LMC7111BIM5X/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

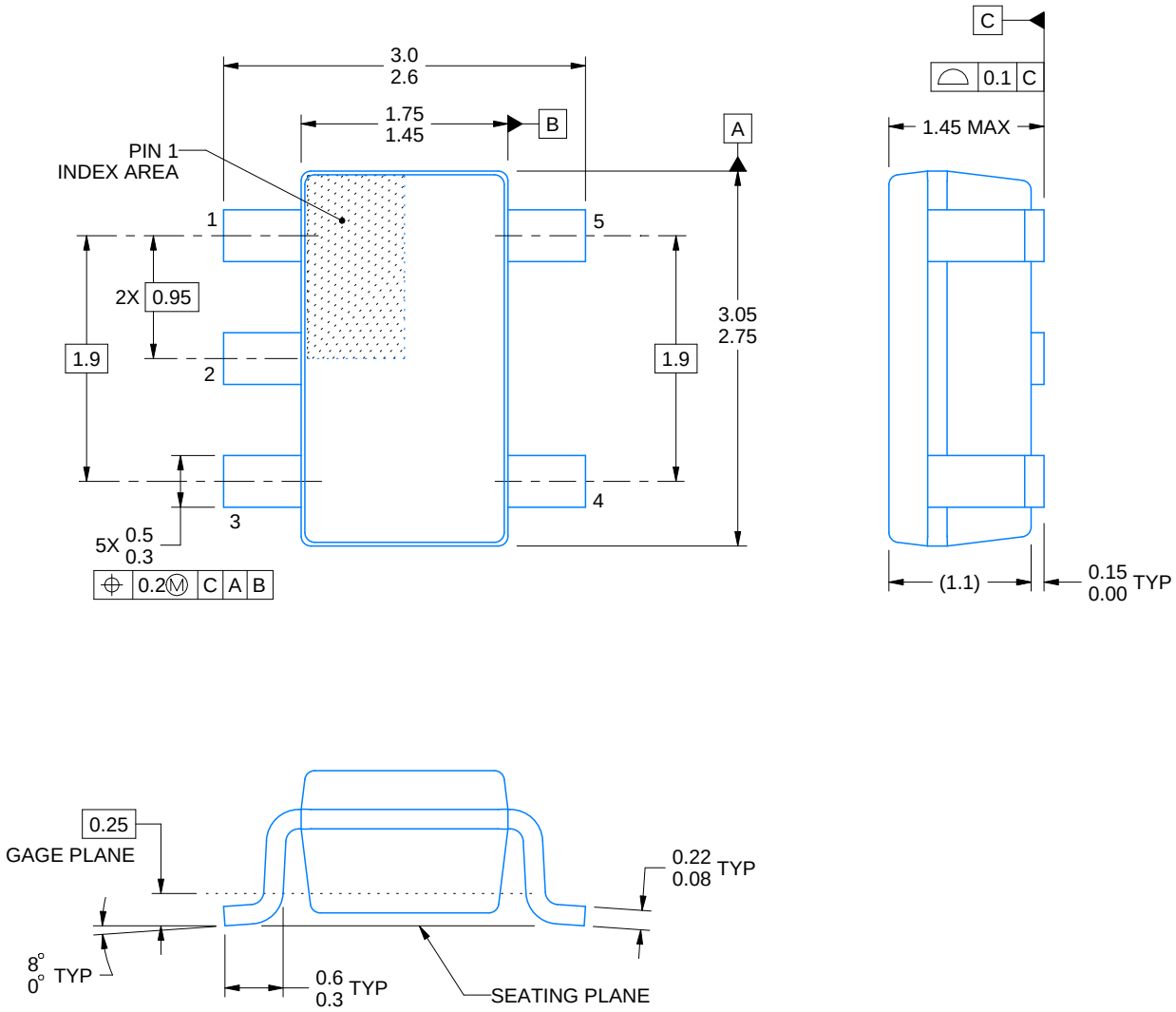
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LMC7111BIM5 | SOT-23 | DBV | 5 | 1000 | 210.0 | 185.0 | 35.0 |
| LMC7111BIM5/NOPB | SOT-23 | DBV | 5 | 1000 | 210.0 | 185.0 | 35.0 |
| LMC7111BIM5X | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| LMC7111BIM5X/NOPB | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

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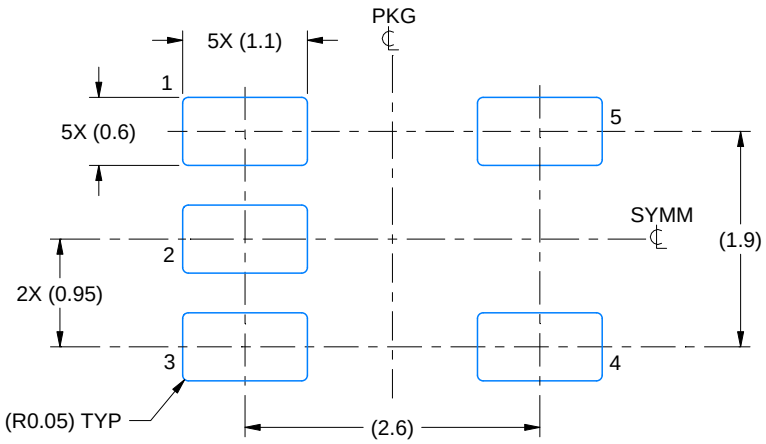
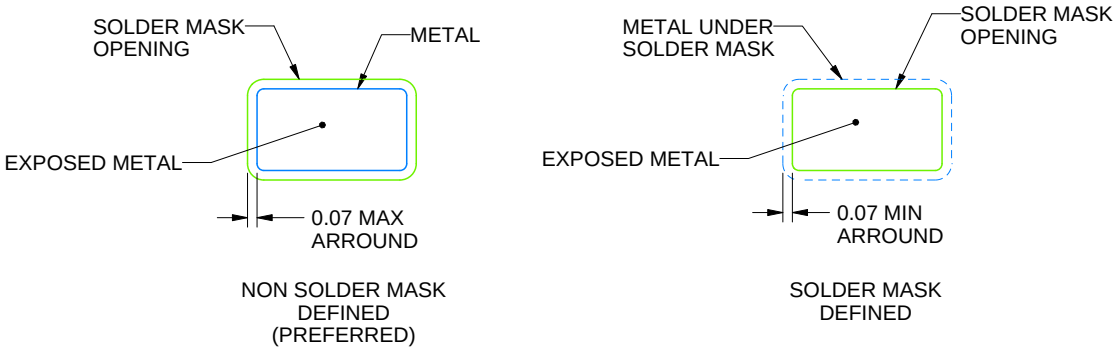
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X




SOLDER MASK DETAILS

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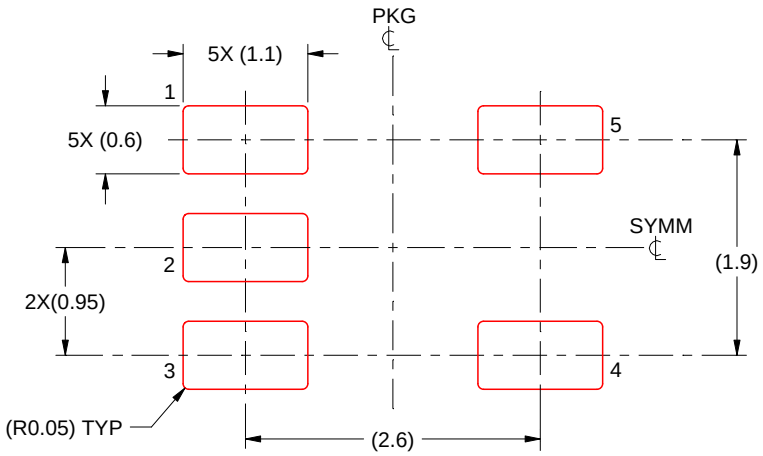
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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