



# THE DATASHEET OF LMH6654MFX/NOPB



## LMH6654, LMH6655 Single and Dual Low Power, 250 MHz, Low Noise Amplifiers

### 1 Features

- ( $V_S = \pm 5\text{ V}$ ,  $T_J = 25\text{ }^\circ\text{C}$ , Typical Values Unless Specified)
- Voltage Feedback Architecture
- Unity Gain Bandwidth 250 MHz
- Supply Voltage Range  $\pm 2.5\text{V}$  to  $\pm 6\text{V}$
- Slew Rate 200 V/ $\mu\text{sec}$
- Supply Current 4.5 mA/channel
- Input Common Mode Voltage  $-5.15\text{V}$  to  $+3.7\text{V}$
- Output Voltage Swing ( $R_L = 100\ \Omega$ )  $-3.6\text{V}$  to  $3.4\text{V}$
- Input Voltage Noise  $4.5\text{ nV}/\sqrt{\text{Hz}}$
- Input Current Noise  $1.7\text{ pA}/\sqrt{\text{Hz}}$
- Settling Time to 0.01% 25 ns

### 2 Applications

- ADC Drivers
- Consumer Video
- Active Filters
- Pulse Delay Circuits
- xDSL Receiver
- Pre-amps

### 3 Description

The LMH6654 and LMH6655 single and dual high speed voltage feedback amplifiers are designed to have unity-gain stable operation with a bandwidth of 250 MHz. They operate from  $\pm 2.5\text{ V}$  to  $\pm 6\text{ V}$  and each channel consumes only 4.5 mA. The amplifiers feature very low voltage noise and wide output swing to maximize signal-to-noise ratio, and possess a true single supply capability with input common mode voltage range extending 150 mV below negative rail and within 1.3 V of the positive rail. The high speed and low power combination of the LMH6654 and LMH6655 make these products an ideal choice for many portable, high speed applications where power is at a premium.

The LMH6654 and LMH6655 are built on TI's Advance VIP10™ (Vertically Integrated PNP) complementary bipolar process.

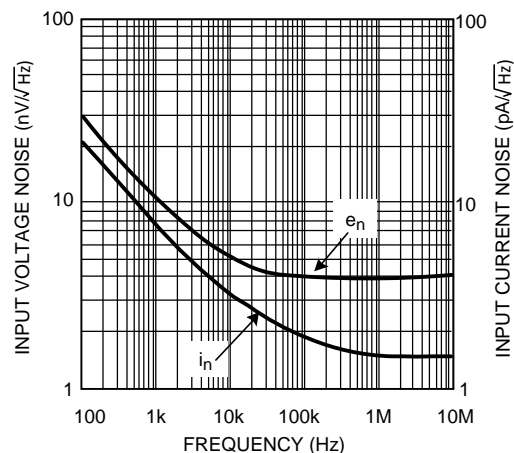
The LMH6654 is packaged in 5-Pin SOT-23 and 8-Pin SOIC. The LMH6655 is packaged in 8-Pin VSSOP (DGK) and 8-Pin SOIC.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH6654	SOIC (8)	4.90 mm x 3.91 mm
LMH6654	SOT-23 (5)	2.90 mm x 1.60 mm
LMH6655	SOIC (8)	4.90 mm x 3.91 mm
LMH6655	VSSOP (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Figure 1. Input Voltage and Current Noise vs. Frequency ( $V_S = \pm 5\text{V}$ )**



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## 4 Revision History

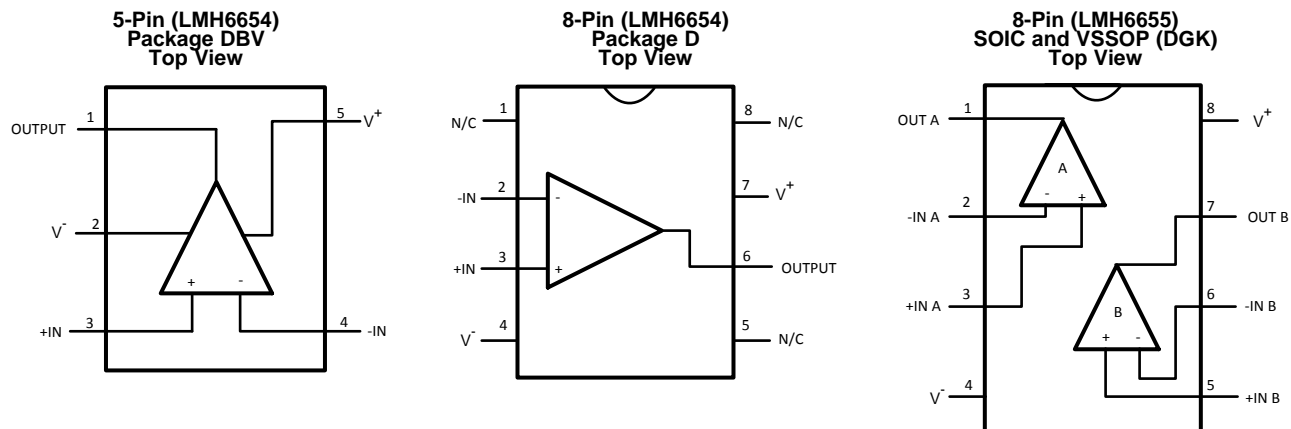
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision D (March 2013) to Revision E</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>Changed data sheet structure and organization. Added, updated, or renamed the following sections: Device Information Table, Application and Implementation; Power Supply Recommendations; Device and Documentation Support; Mechanical, Packaging, and Ordering Information. Deleted Switching Characteristics due to redundancy. ....</li> </ul>	<b>1</b>
<ul style="list-style-type: none"> <li>Changed from Junction Temperature Range to "Operating Temperature Range" .....</li> </ul>	<b>4</b>
<ul style="list-style-type: none"> <li>Deleted <math>T_J = 25^\circ\text{C}</math>.....</li> </ul>	<b>5</b>
<ul style="list-style-type: none"> <li>Deleted <math>T_J = 25^\circ\text{C}</math> .....</li> </ul>	<b>7</b>

<b>Changes from Revision C (March 2013) to Revision D</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>Changed layout of National Data Sheet to TI format .....</li> </ul>	<b>19</b>

## 5 Pin Configuration and Functions



**Pin Functions**

NAME	PIN			I/O	DESCRIPTION
	LMH6654		LMH6655		
	DBV	D	DGK		
-IN	4	2		I	Inverting Input
+IN	3	3		I	Non-inverting Input
-IN A			2	I	ChA Inverting Input
+IN A			3	I	ChA Non-inverting Input
-IN B			6	I	ChB Inverting Input
+IN B			5	I	ChB Non-inverting Input
N/C		1, 5, 8		—	No Connection
OUT A			1	O	ChA Output
OUT B			7	O	ChB Output
OUTPUT	1	6		O	Output
V <sup>-</sup>	2	4	4	I	Negative Supply
V <sup>+</sup>	5	7	8	I	Positive Supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
V <sub>IN</sub> Differential		±1.2	V
Output Short Circuit Duration	See <sup>(2)</sup>		
Supply Voltage (V <sup>+</sup> - V <sup>-</sup> )		13.2	V
Voltage at Input pins		V <sup>+</sup> +0.5 V <sup>-</sup> -0.5	V
Junction Temperature <sup>(3)</sup>		150	°C
Soldering Information	Infrared or Convection (20 sec.)	235	°C
	Wave Soldering (10 sec.)	260	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.
- (3) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, R<sub>θJA</sub> and T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(MAX)</sub> - T<sub>A</sub>)/R<sub>θJA</sub>. All numbers apply for packages soldered directly onto a PC board.

### 6.2 Handling Ratings

	MIN	MAX	UNIT
T <sub>stg</sub> Storage temperature range	-65	150	°C
V <sub>(ESD)</sub> Electrostatic discharge <sup>(1)</sup>	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(2)</sup>		2000
	Machine model (MM) <sup>(3)</sup>		200

- (1) Human body model, 1.5 kΩ in series with 100 pF. Machine model: 0Ω in series with 100 pF.
- (2) JEDEC document JEP155 states that 2000-V HBM allows safe manufacturing with a standard ESD control process.
- (3) JEDEC document JEP157 states that 200-V MM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply Voltage (V <sup>+</sup> - V <sup>-</sup> )	±2.5		±6.0	V
Operating Temperature Range	-40		85	°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Table.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SOIC (D)	VSSOP (DGK)	SOT-23 (D)	UNIT
	8 PINS	8 PINS	5 PINS	
R <sub>θJA</sub> Junction-to-ambient thermal resistance	172	235	265	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 ±5V Electrical Characteristics

Unless otherwise specified, all limits ensured for  $V^+ = +5V$ ,  $V^- = -5V$ ,  $V_{CM} = 0V$ ,  $A_V = +1$ ,  $R_F = 25\Omega$  for gain = +1,  $R_F = 402\Omega$  for gain  $\geq +2$ , and  $R_L = 100\Omega$ . **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
<b>DYNAMIC PERFORMANCE</b>						
$f_{CL}$	Close Loop Bandwidth	$A_V = +1$		250		MHz
		$A_V = +2$		130		
		$A_V = +5$		52		
		$A_V = +10$		26		
GBWP	Gain Bandwidth Product	$A_V \geq +5$		260		MHz
	Bandwidth for 0.1 dB Flatness	$A_V = +1$		18		MHz
$\phi_m$	Phase Margin			50		deg
SR	Slew Rate <sup>(3)</sup>	$A_V = +1$ , $V_{IN} = 2 V_{PP}$		200		V/ $\mu$ s
$t_s$	Settling Time 0.01%	$A_V = +1$ , 2V Step		25		ns
				15		ns
$t_r$	Rise Time	$A_V = +1$ , 0.2V Step		1.4		ns
$t_f$	Fall Time	$A_V = +1$ , 0.2V Step		1.2		ns
<b>DISTORTION and NOISE RESPONSE</b>						
$e_n$	Input Referred Voltage Noise	$f \geq 0.1$ MHz		4.5		$nV/\sqrt{Hz}$
$i_n$	Input-Referred Current Noise	$f \geq 0.1$ MHz		1.7		$pA/\sqrt{Hz}$
	Second Harmonic Distortion	$A_V = +1$ , $f = 5$ MHz		-80		dBc
	Third Harmonic Distortion	$V_O = 2 V_{PP}$ , $R_L = 100\Omega$		-85		
$X_t$	Crosstalk (for LMH6655 only)	Input Referred, 5 MHz, Channel-to-Channel		-80		dB
DG	Differential Gain	$A_V = +2$ , NTSC, $R_L = 150\Omega$		0.01%		
DP	Differential Phase	$A_V = +2$ , NTSC, $R_L = 150\Omega$		0.025		deg
<b>INPUT CHARACTERISTICS</b>						
$V_{OS}$	Input Offset Voltage	$V_{CM} = 0V$	-3 -4	$\pm 1$	3 4	mV
TC $V_{OS}$	Input Offset Average Drift	$V_{CM} = 0V$ <sup>(4)</sup>		6		$\mu V/^\circ C$
$I_B$	Input Bias Current	$V_{CM} = 0V$		5	12 18	$\mu A$
$I_{OS}$	Input Offset Current	$V_{CM} = 0V$	-1 -2	0.3	1 2	$\mu A$
$R_{IN}$	Input Resistance	Common Mode		4		M $\Omega$
		Differential Mode		20		k $\Omega$
$C_{IN}$	Input Capacitance	Common Mode		1.8		pF
		Differential Mode		1		
CMRR	Common Mode Rejection Ratio	Input Referred, $V_{CM} = 0V$ to $-5V$	70 68	90		dB
CMVR	Input Common- Mode Voltage Range	CMRR $\geq 50$ dB		-5.15	-5.0	V
				3.5	3.7	
<b>TRANSFER CHARACTERISTICS</b>						
$A_{VOL}$	Large Signal Voltage Gain	$V_O = 4 V_{PP}$ , $R_L = 100\Omega$	60 58	67		dB

(1) All limits are specified by testing or statistical analysis.

(2) Typical Values represent the most likely parametric norm.

(3) Slew rate is the slower of the rising and falling slew rates. Slew rate is rate of change from 10% to 90% of output voltage step.

(4) Offset voltage average drift is determined by dividing the change in  $V_{OS}$  at temperature extremes into the total temperature change.

**±5V Electrical Characteristics (continued)**

Unless otherwise specified, all limits ensured for  $V^+ = +5V$ ,  $V^- = -5V$ ,  $V_{CM} = 0V$ ,  $A_V = +1$ ,  $R_F = 25\Omega$  for gain = +1,  $R_F = 402\Omega$  for gain  $\geq +2$ , and  $R_L = 100\Omega$ . **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
<b>OUTPUT CHARACTERISTICS</b>						
$V_O$	Output Swing High	No Load	3.4 <b>3.2</b>	3.6		V
	Output Swing Low	No Load		-3.9	-3.7 <b>-3.5</b>	
	Output Swing High	$R_L = 100\Omega$	3.2 <b>3.0</b>	3.4		
	Output Swing Low	$R_L = 100\Omega$		-3.6	-3.4 <b>-3.2</b>	
$I_{SC}$	Short Circuit Current <sup>(5)</sup>	Sourcing, $V_O = 0V$ $\Delta V_{IN} = 200\text{ mV}$	145 <b>130</b>	280		mA
		Sinking, $V_O = 0V$ $\Delta V_{IN} = 200\text{ mV}$	100 <b>80</b>	185		
$I_{OUT}$	Output Current	Sourcing, $V_O = +3V$		80		mA
		Sinking, $V_O = -3V$		120		
$R_O$	Output Resistance	$A_V = +1$ , $f < 100\text{ kHz}$		0.08		$\Omega$
<b>POWER SUPPLY</b>						
PSRR	Power Supply Rejection Ratio	Input Referred, $V_S = \pm 5V$ to $\pm 6V$	60	76		dB
$I_S$	Supply Current (per channel)			4.5	6 7	mA

(5) Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.

## 6.6 5V Electrical Characteristics

Unless otherwise specified, all limits ensured for  $V^+ = +5V$ ,  $V^- = -0V$ ,  $V_{CM} = 2.5V$ ,  $A_V = +1$ ,  $R_F = 25\ \Omega$  for gain = +1,  $R_F = 402\ \Omega$  for gain  $\geq +2$ , and  $R_L = 100\ \Omega$  to  $V^+/2$ . **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
<b>DYNAMIC PERFORMANCE</b>						
$f_{CL}$	Close Loop Bandwidth	$A_V = +1$		230		MHz
		$A_V = +2$		120		
		$A_V = +5$		50		
		$A_V = +10$		25		
GBWP	Gain Bandwidth Product	$A_V \geq +5$		250		MHz
	Bandwidth for 0.1 dB Flatness	$A_V = +1$		17		MHz
$\phi_m$	Phase Margin			48		deg
SR	Slew Rate <sup>(3)</sup>	$A_V = +1$ , $V_{IN} = 2\ V_{PP}$		190		V/ $\mu$ s
$t_s$	Settling Time 0.01%	$A_V = +1$ , 2V Step		30		ns
				20		ns
$t_r$	Rise Time	$A_V = +1$ , 0.2V Step		1.5		ns
$t_f$	Fall Time	$A_V = +1$ , 0.2V Step		1.35		ns
<b>DISTORTION and NOISE RESPONSE</b>						
$e_n$	Input Referred Voltage Noise	$f \geq 0.1\ \text{MHz}$		4.5		$nV/\sqrt{\text{Hz}}$
$i_n$	Input Referred Current Noise	$f \geq 0.1\ \text{MHz}$		1.7		$pA/\sqrt{\text{Hz}}$
	Second Harmonic Distortion	$A_V = +1$ , $f = 5\ \text{MHz}$		-65		dBc
	Third Harmonic Distortion	$V_O = 2\ V_{PP}$ , $R_L = 100\ \Omega$		-70		
$X_t$	Crosstalk (for LMH6655 only)	Input Referred, 5 MHz		-78		dB
<b>INPUT CHARACTERISTICS</b>						
$V_{OS}$	Input Offset Voltage	$V_{CM} = 2.5V$	-5 <b>-6.5</b>	$\pm 2$	5 <b>6.5</b>	mV
TC $V_{OS}$	Input Offset Average Drift	$V_{CM} = 2.5V$ <sup>(4)</sup>		6		$\mu V/^\circ C$
$I_B$	Input Bias Current	$V_{CM} = 2.5V$		6	12 <b>18</b>	$\mu A$
$I_{OS}$	Input Offset Current	$V_{CM} = 2.5V$	-2 <b>-3</b>	0.5	2 <b>3</b>	$\mu A$
$R_{IN}$	Input Resistance	Common Mode		4		M $\Omega$
		Differential Mode		20		k $\Omega$
$C_{IN}$	Input Capacitance	Common Mode		1.8		pF
		Differential Mode		1		
CMRR	Common Mode Rejection Ratio	Input Referred, $V_{CM} = 0V$ to $-2.5V$	70 <b>68</b>	90		dB
CMVR	Input Common Mode Voltage Range	CMRR $\geq 50\ \text{dB}$		-0.15	0	V
				3.5	3.7	
<b>TRANSFER CHARACTERISTICS</b>						
$A_{VOL}$	Large Signal Voltage Gain	$V_O = 1.6\ V_{PP}$ , $R_L = 100\ \Omega$	58 <b>55</b>	64		dB

(1) All limits are specified by testing or statistical analysis.

(2) Typical Values represent the most likely parametric norm.

(3) Slew rate is the slower of the rising and falling slew rates. Slew rate is rate of change from 10% to 90% of output voltage step.

(4) Offset voltage average drift is determined by dividing the change in  $V_{OS}$  at temperature extremes into the total temperature change.

**5V Electrical Characteristics (continued)**

Unless otherwise specified, all limits ensured for  $V^+ = +5V$ ,  $V^- = -0V$ ,  $V_{CM} = 2.5V$ ,  $A_V = +1$ ,  $R_F = 25\ \Omega$  for gain = +1,  $R_F = 402\ \Omega$  for gain  $\geq +2$ , and  $R_L = 100\ \Omega$  to  $V^+/2$ . **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
<b>OUTPUT CHARACTERISTICS</b>						
$V_O$	Output Swing High	No Load	3.6 <b>3.4</b>	3.75		V
	Output Swing Low	No Load		0.9	1.1 <b>1.3</b>	
	Output Swing High	$R_L = 100\ \Omega$	3.5 <b>3.35</b>	3.70		
	Output Swing Low	$R_L = 100\ \Omega$		1	1.3 <b>1.45</b>	
$I_{SC}$	Short Circuit Current <sup>(5)</sup>	Sourcing, $V_O = 2.5V$ $\Delta V_{IN} = 200\ mV$	90 <b>80</b>	170		mA
		Sinking, $V_O = 2.5V$ $\Delta V_{IN} = 200\ mV$	70 <b>60</b>	140		
$I_{OUT}$	Output Current	Sourcing, $V_O = +3.5V$		30		mA
		Sinking, $V_O = 1.5V$		60		
$R_O$	Output Resistance	$A_V = +1$ , $f < 100\ kHz$		.08		$\Omega$
<b>POWER SUPPLY</b>						
PSRR	Power Supply Rejection Ratio	Input Referred, $V_S = \pm 2.5V$ to $\pm 3V$	60	75		dB
$I_S$	Supply Current (per channel)			4.5	6 7	mA

(5) Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.

### 6.7 Typical Characteristics

25°C,  $V^+ = \pm 5\text{ V}$ ,  $V^- = -5$ ,  $R_F = 25\ \Omega$  for gain = +1,  $R_F = 402\ \Omega$  for gain  $\geq +2$  and  $R_L = 100\ \Omega$ , unless otherwise specified.

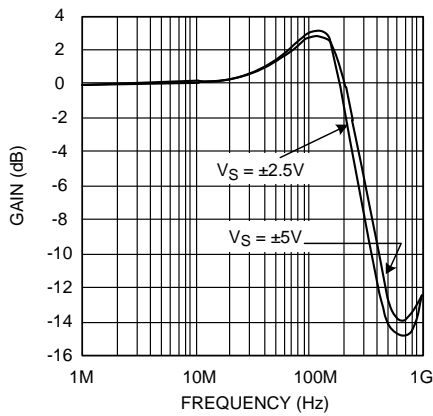


Figure 2. Closed Loop Bandwidth (G = +1)

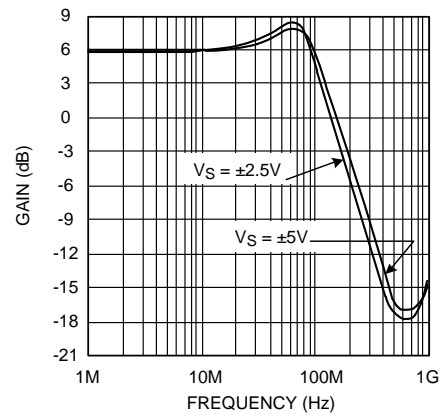


Figure 3. Closed Loop Bandwidth (G = +2)

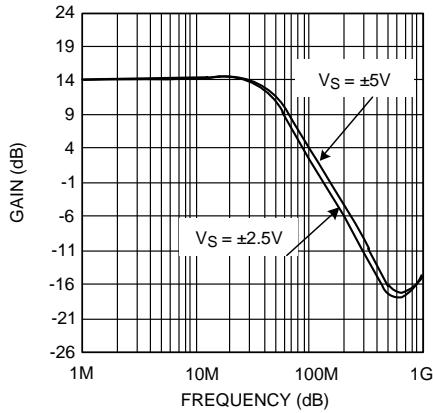


Figure 4. Closed Loop Bandwidth (G = +5)

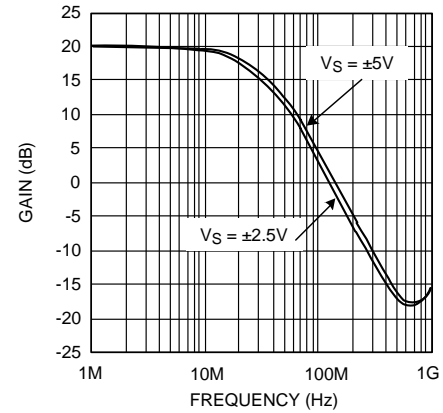


Figure 5. Closed Loop Bandwidth (G = +10)

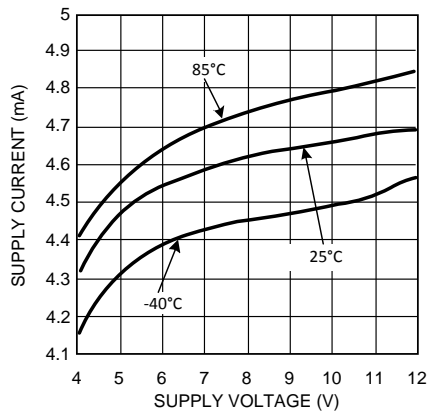


Figure 6. Supply Current per Channel vs. Supply Voltage

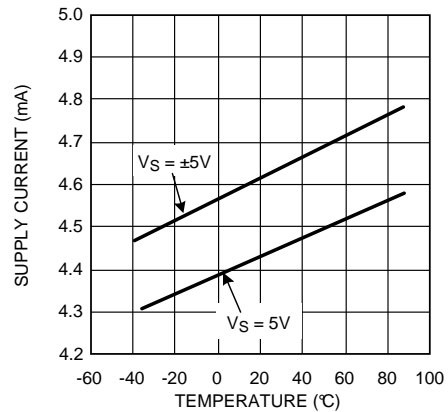
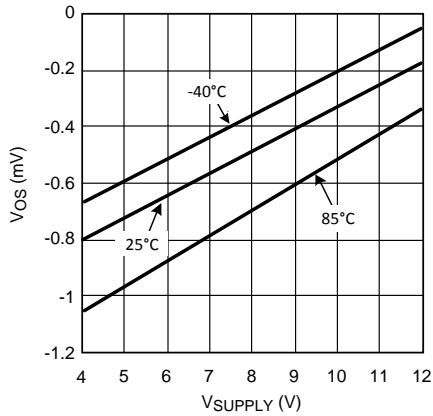


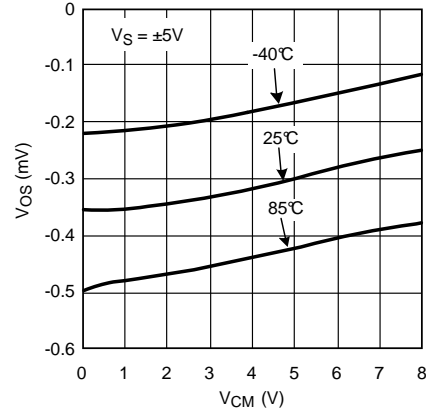
Figure 7. Supply Current per Channel vs. Temperature

**Typical Characteristics (continued)**

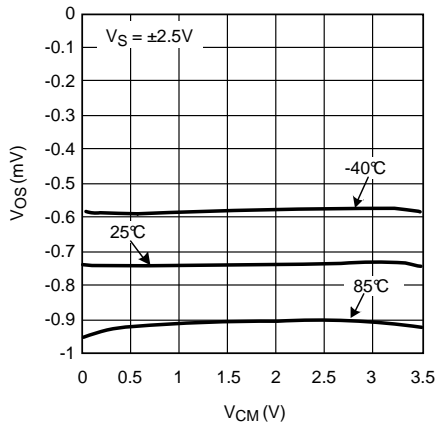
25°C,  $V^+ = \pm 5\text{ V}$ ,  $V^- = -5$ ,  $R_F = 25\ \Omega$  for gain = +1,  $R_F = 402\ \Omega$  for gain  $\geq +2$  and  $R_L = 100\ \Omega$ , unless otherwise specified.



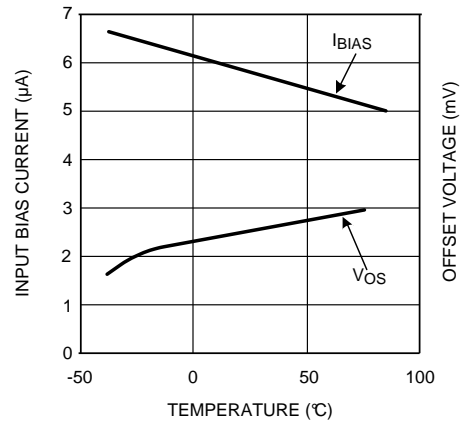
**Figure 8. Offset Voltage vs. Supply Voltage ( $V_{CM} = 0\text{V}$ )**



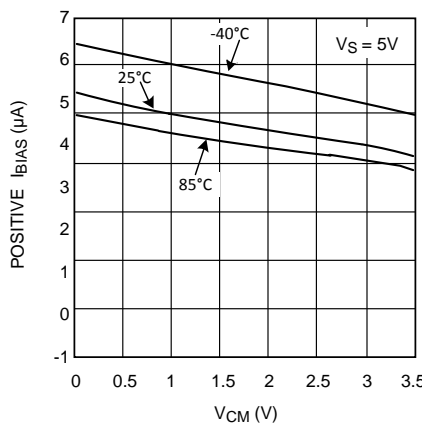
**Figure 9. Offset Voltage vs. Common Mode**



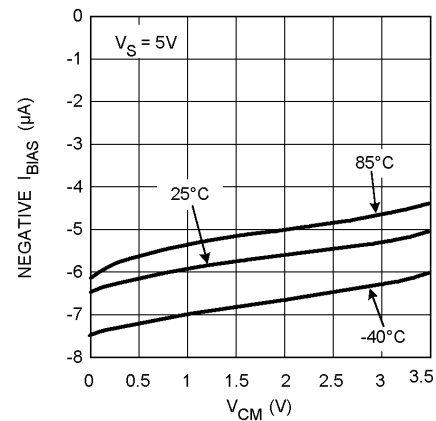
**Figure 10. Offset Voltage vs. Common Mode**



**Figure 11. Bias Current and Offset Voltage vs. Temperature**



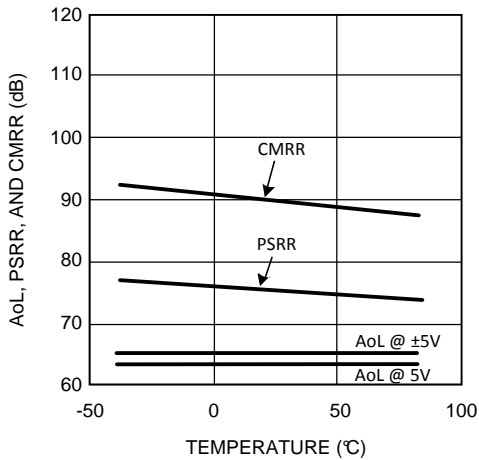
**Figure 12. Bias Current vs. Common Mode Voltage**



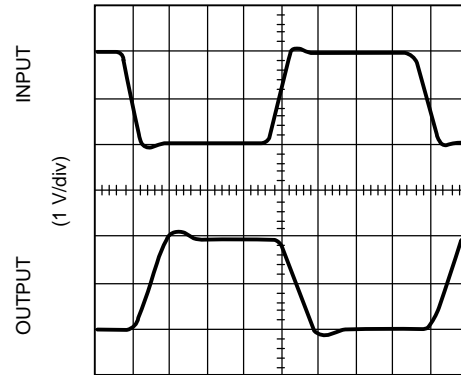
**Figure 13. Bias Current vs. Common Mode Voltage**

**Typical Characteristics (continued)**

25°C,  $V^+ = \pm 5\text{ V}$ ,  $V^- = -5$ ,  $R_F = 25\ \Omega$  for gain = +1,  $R_F = 402\ \Omega$  for gain  $\geq +2$  and  $R_L = 100\ \Omega$ , unless otherwise specified.

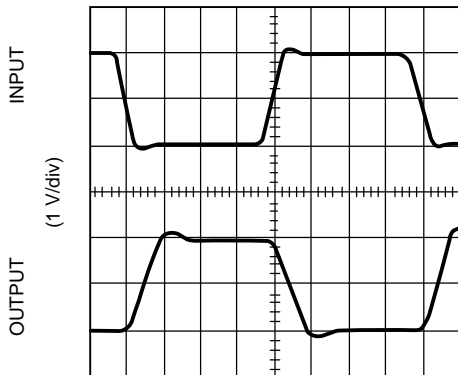


**Figure 14.  $A_{OL}$ , PSRR and CMRR vs. Temperature**



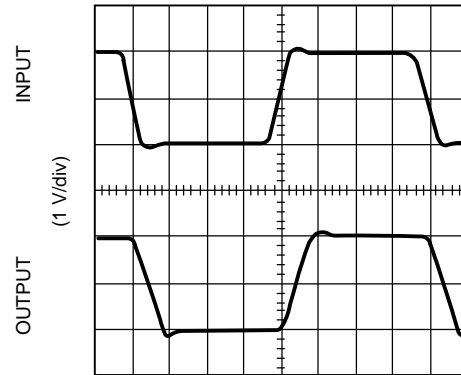
TIME (12.5 ns/div)

**Figure 15. Inverting Large Signal Pulse Response ( $V_S = 5\text{V}$ )**



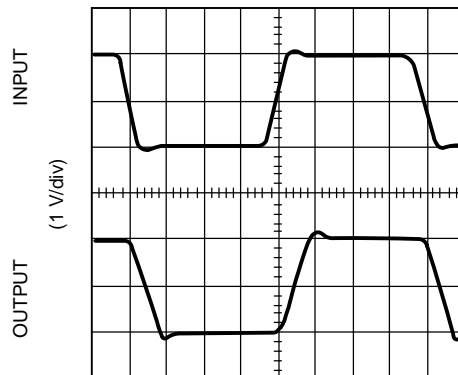
TIME (12.5 ns/div)

**Figure 16. Inverting Large Signal Pulse Response ( $V_S = \pm 5\text{V}$ )**



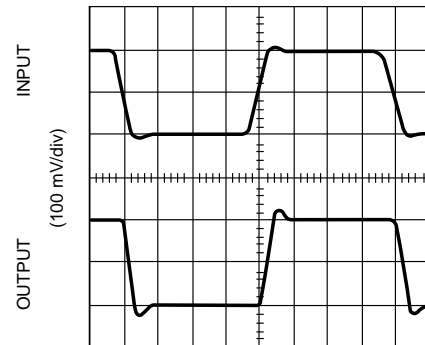
TIME (12.5 ns/div)

**Figure 17. Non-Inverting Large Signal Pulse Response ( $V_S = 5\text{V}$ )**



TIME (12.5 ns/div)

**Figure 18. Non-Inverting Large Signal Pulse Response ( $V_S = \pm 5\text{V}$ )**



TIME (12.5 ns/div)

**Figure 19. Non-Inverting Small Signal Pulse Response ( $V_S = 5\text{V}$ )**

### Typical Characteristics (continued)

25°C,  $V^+ = \pm 5\text{ V}$ ,  $V^- = -5$ ,  $R_F = 25\ \Omega$  for gain = +1,  $R_F = 402\ \Omega$  for gain  $\geq +2$  and  $R_L = 100\ \Omega$ , unless otherwise specified.

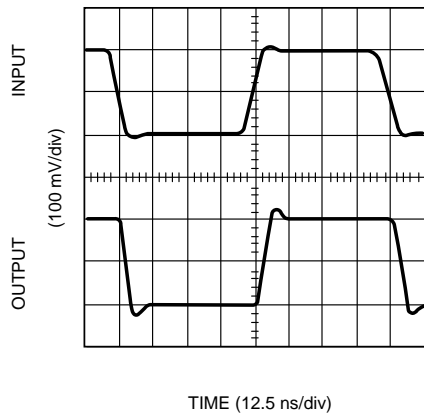


Figure 20. Non-Inverting Small Signal Pulse Response ( $V_S = \pm 5\text{V}$ )

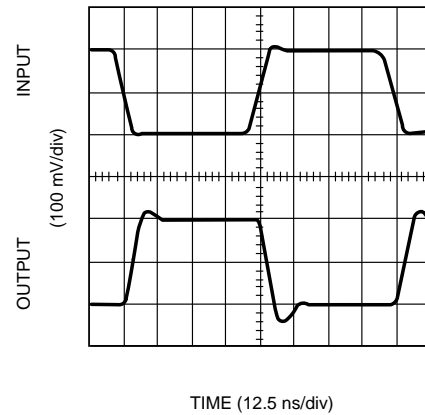


Figure 21. Inverting Small Signal Pulse Response ( $V_S = 5\text{V}$ )

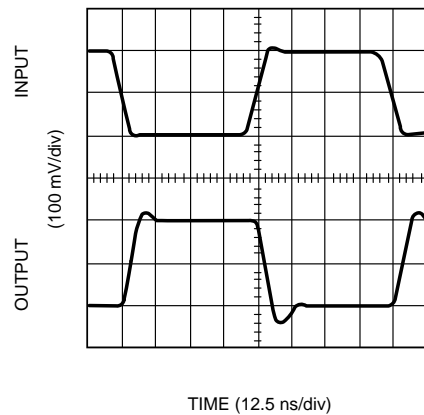


Figure 22. Inverting Small Signal Pulse Response ( $V_S = \pm 5\text{V}$ )

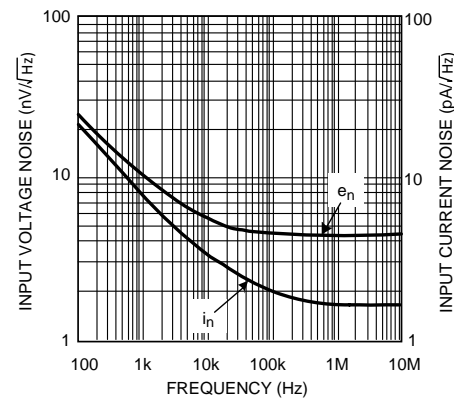


Figure 23. Input Voltage and Current Noise vs. Frequency ( $V_S = 5\text{V}$ )

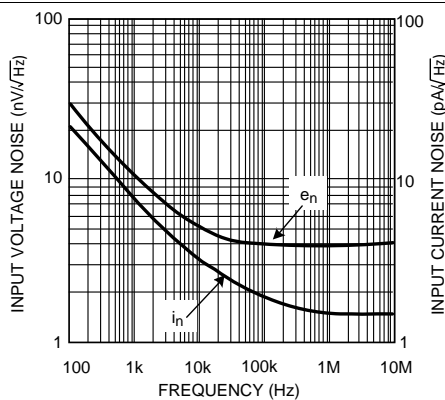


Figure 24. Input Voltage and Current Noise vs. Frequency ( $V_S = \pm 5\text{V}$ )

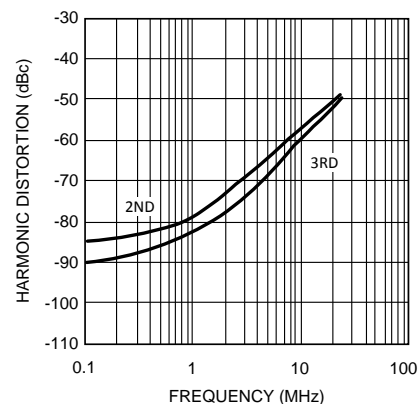
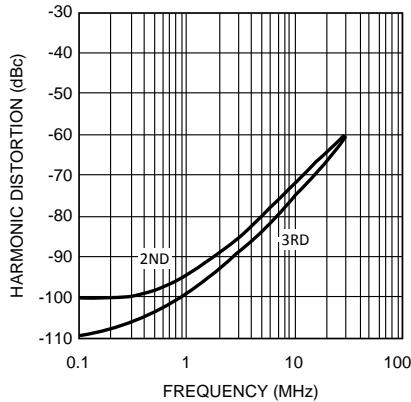


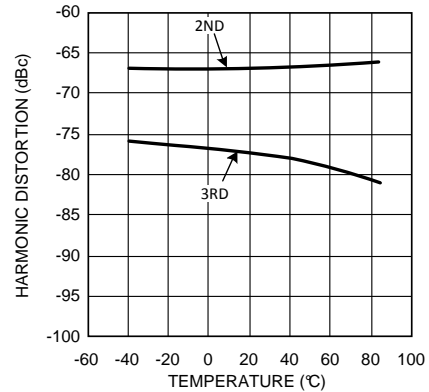
Figure 25. Harmonic Distortion vs. Frequency  
 $G = +1$ ,  $V_O = 2\text{ V}_{PP}$ ,  $V_S = 5\text{V}$

Typical Characteristics (continued)

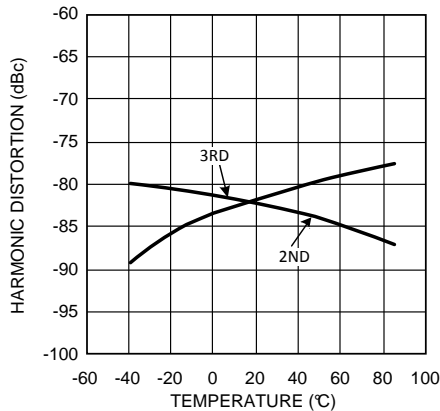
25°C,  $V^+ = \pm 5\text{ V}$ ,  $V^- = -5$ ,  $R_F = 25\ \Omega$  for gain = +1,  $R_F = 402\ \Omega$  for gain  $\geq +2$  and  $R_L = 100\ \Omega$ , unless otherwise specified.



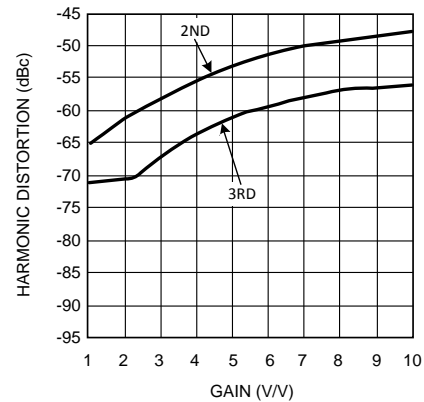
**Figure 26. Harmonic Distortion vs. Frequency**  
 $G = +1$ ,  $V_O = 2\text{ V}_{PP}$ ,  $V_S = \pm 5\text{ V}$



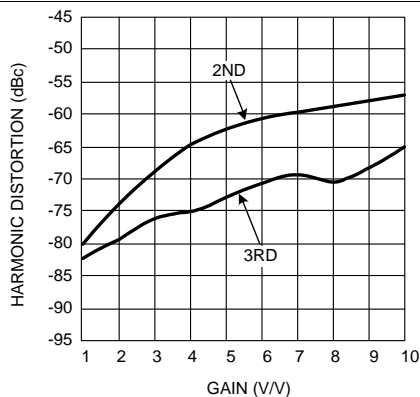
**Figure 27. Harmonic Distortion vs. Temperature**  
 $V_S = 5\text{ V}$ ,  $f = 5\text{ MHz}$ ,  $V_O = 2\text{ V}_{PP}$



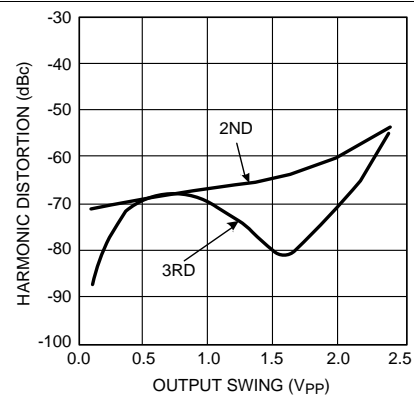
**Figure 28. Harmonic Distortion vs. Temperature**  
 $V_S = \pm 5\text{ V}$ ,  $f = 5\text{ MHz}$ ,  $V_O = 2\text{ V}_{PP}$



**Figure 29. Harmonic Distortion vs. Gain**  
 $V_S = 5\text{ V}$ ,  $f = 5\text{ MHz}$ ,  $V_O = 2\text{ V}_{PP}$



**Figure 30. Harmonic Distortion vs. Gain**  
 $V_S = \pm 5\text{ V}$ ,  $f = 5\text{ MHz}$ ,  $V_O = 2\text{ V}_{PP}$



**Figure 31. Harmonic Distortion vs. Output Swing**  
 $(G = +2, V_S = 5\text{ V}, f = 5\text{ MHz})$

Typical Characteristics (continued)

25°C,  $V^+ = \pm 5\text{ V}$ ,  $V^- = -5$ ,  $R_F = 25\ \Omega$  for gain = +1,  $R_F = 402\ \Omega$  for gain  $\geq +2$  and  $R_L = 100\ \Omega$ , unless otherwise specified.

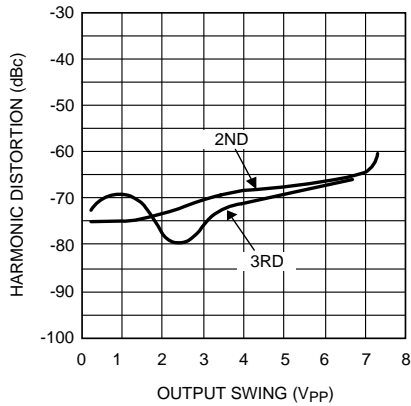


Figure 32. Harmonic Distortion vs. Output Swing ( $G = +2$ ,  $V_S = \pm 5\text{V}$ ,  $f = 5\text{ MHz}$ )

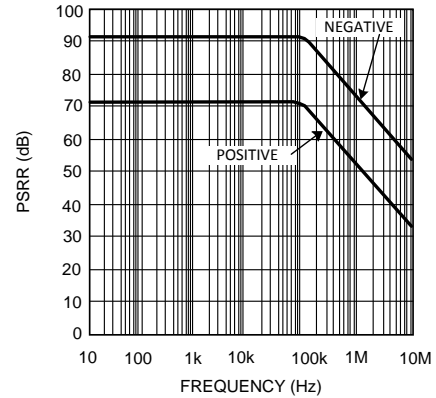


Figure 33. PSRR vs. Frequency

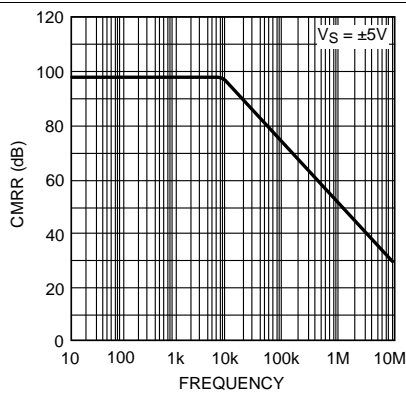


Figure 34. CMRR vs. Frequency

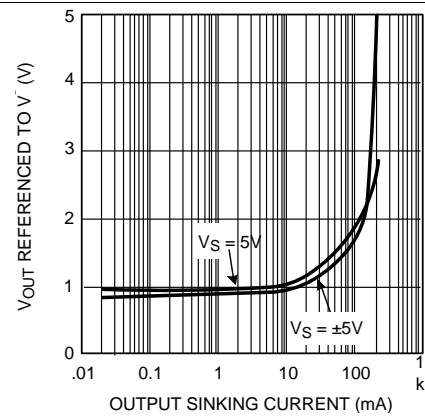


Figure 35. Output Sinking Current

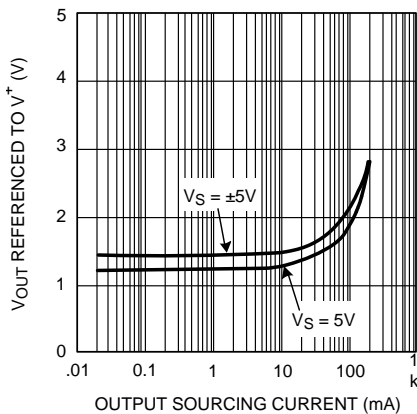


Figure 36. Output Sourcing Current

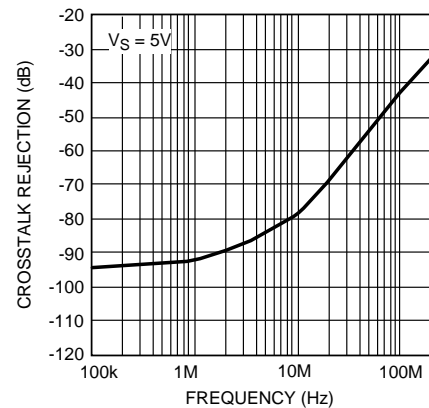
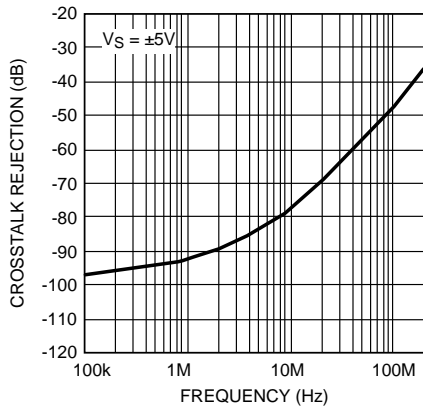


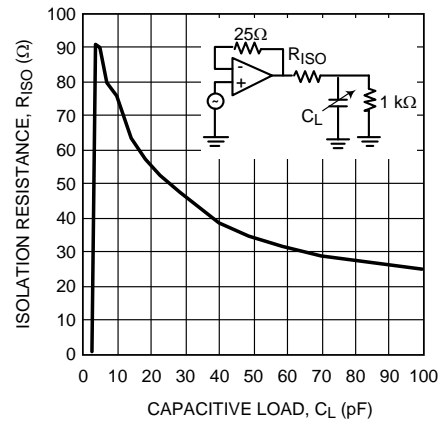
Figure 37. CrossTalk vs. Frequency (LMH6655 only)

**Typical Characteristics (continued)**

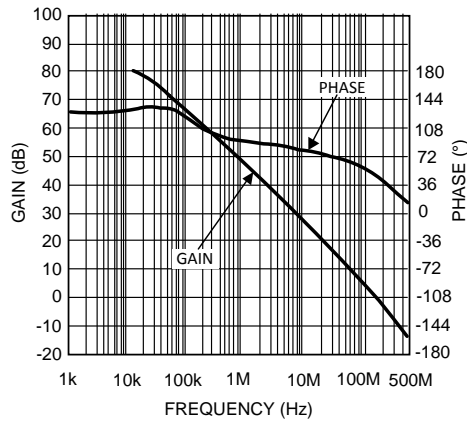
25°C,  $V^+ = \pm 5\text{ V}$ ,  $V^- = -5$ ,  $R_F = 25\ \Omega$  for gain = +1,  $R_F = 402\ \Omega$  for gain  $\geq +2$  and  $R_L = 100\ \Omega$ , unless otherwise specified.



**Figure 38. CrossTalk vs. Frequency (LMH6655 only)**



**Figure 39. Isolation Resistance vs. Capacitive Load**



**Figure 40. Open Loop Gain and Phase vs. Frequency**

## 7 Application and Implementation

### 7.1 Application Information

The LMH6654 single and LMH6655 dual high speed, voltage feedback amplifiers are manufactured on TI's new VIP10™ (Vertically Integrated PNP) complementary bipolar process. These amplifiers can operate from  $\pm 2.5$  V to  $\pm 6$  V power supply. They offer low supply current, wide bandwidth, very low voltage noise and large output swing. Many of the typical performance plots found in the datasheet can be reproduced if 50  $\Omega$  coax and 50  $\Omega$   $R_{IN}/R_{OUT}$  resistors are used.

### 7.2 Typical Application

#### 7.2.1 Design Requirements

##### 7.2.1.1 Components Selection and Feedback Resistor

It is important in high-speed applications to keep all component leads short since wires are inductive at high frequency. For discrete components, choose carbon composition axially leaded resistors and micro type capacitors. Surface mount components are preferred over discrete components for minimum inductive effect. Never use wire wound type resistors in high frequency applications.

Large values of feedback resistors can couple with parasitic capacitance and cause undesired effects such as ringing or oscillation in high-speed amplifiers. Keep resistors as low as possible consistent with output loading consideration. For a gain of 2 and higher, 402  $\Omega$  feedback resistor used for the typical performance plots gives optimal performance. For unity gain follower, a 25  $\Omega$  feedback resistor is recommended rather than a direct short. This effectively reduces the Q of what would otherwise be a parasitic inductance (the feedback wire) into the parasitic capacitance at the inverting input.

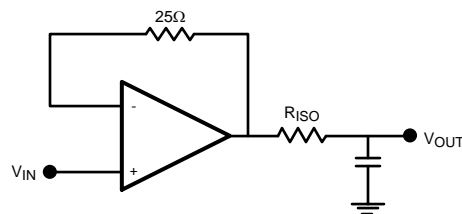
#### 7.2.2 Detailed Design Procedure

##### 7.2.2.1 Driving Capacitive Loads

Capacitive loads decrease the phase margin of all op amps. The output impedance of a feedback amplifier becomes inductive at high frequencies, creating a resonant circuit when the load is capacitive. This can lead to overshoot, ringing and oscillation. To eliminate oscillation or reduce ringing, an isolation resistor can be placed as shown in [Figure 41](#) below. At frequencies above

$$F = \frac{1}{2 \pi R_{ISO} C_{LOAD}} \quad (1)$$

the load impedance of the Amplifier approaches  $R_{ISO}$ . The desired performance depends on the value of the isolation resistor. The isolation resistance vs. capacitance load graph in the typical performance characteristics provides the means for selection of the value of  $R_S$  that provides  $\leq 3$  dB peaking in closed loop  $A_V = 1$  response. In general, the bigger the isolation resistor, the more damped the pulse response becomes. For initial evaluation, a 50 $\Omega$  isolation resistor is recommended.



**Figure 41. Isolation Resistor Placement**

## Typical Application (continued)

### 7.2.2.2 Bias Current Cancellation

In order to cancel the bias current errors of the non-inverting configuration, the parallel combination of the gain setting  $R_g$  and feedback  $R_f$  resistors should equal the equivalent source resistance  $R_{seq}$  as defined in Figure 42. Combining this constraint with the non-inverting gain equation, allows both  $R_f$  and  $R_g$  to be determined explicitly from the following equations:

$$R_f = A_V R_{seq} \text{ and } R_g = R_f / (A_V - 1) \quad (2)$$

For inverting configuration, bias current cancellation is accomplished by placing a resistor  $R_b$  on the non-inverting input equal in value to the resistance seen by the inverting input ( $R_f // (R_g + R_s)$ ). The additional noise contribution of  $R_b$  can be minimized through the use of a shunt capacitor.

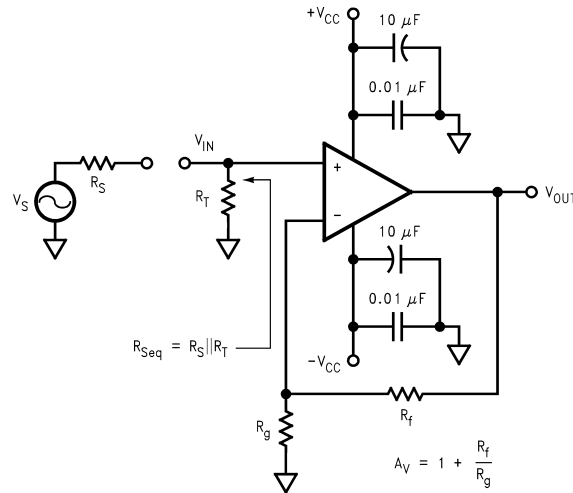


Figure 42. Non-Inverting Amplifier Configuration

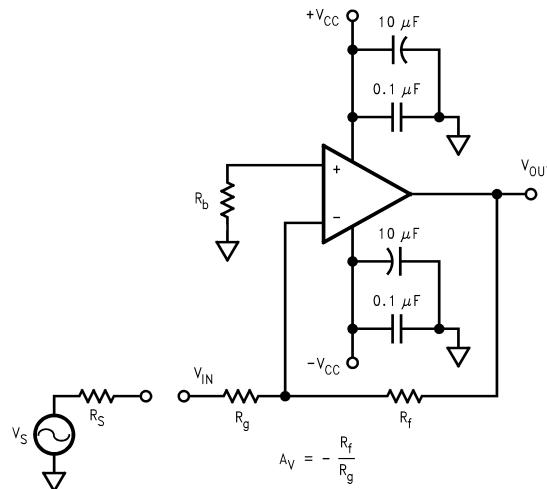
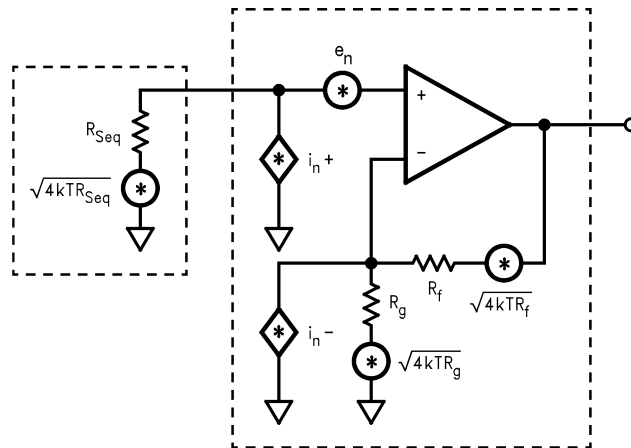


Figure 43. Inverting Amplifier Configuration

**Typical Application (continued)**

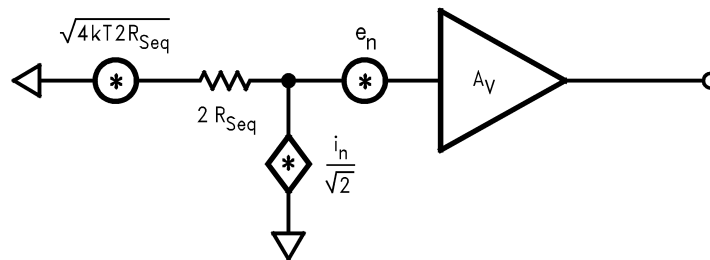
**7.2.2.3 Total Input Noise vs. Source Resistance**

The noise model for the non-inverting amplifier configuration showing all noise sources is described in Figure 44. In addition to the intrinsic input voltage noise ( $e_n$ ) and current noise ( $i_n = i_{n+} = i_{n-}$ ) sources, there also exists thermal voltage noise  $e_r = \sqrt{4kTR}$  associated with each of the external resistors. Equation 3 provides the general form for total equivalent input voltage noise density ( $e_{ni}$ ). Equation 4 is a simplification of Equation 3 that assumes  $R_f \parallel R_g = R_{seq}$  for bias current cancellation. Figure 45 illustrates the equivalent noise model using this assumption. The total equivalent output voltage noise ( $e_{no}$ ) is  $e_{ni} \cdot A_V$ .



**Figure 44. Non-Inverting Amplifier Noise Model**

$$e_{ni} = \sqrt{e_n^2 + (i_{n+} \cdot R_{Seq})^2 + 4kTR_{Seq} + (i_{n-} \cdot (R_f \parallel R_g))^2 + 4kT(R_f \parallel R_g)} \tag{3}$$



**Figure 45. Noise Model with  $R_f \parallel R_g = R_{seq}$**

$$e_{ni} = \sqrt{e_n^2 + 2 (i_n \cdot R_{Seq})^2 + 4kT (2R_{Seq})} \tag{4}$$

If bias current cancellation is not a requirement, then  $R_f \parallel R_g$  does not need to equal  $R_{seq}$ . In this case, according to Equation 3,  $R_f$  and  $R_g$  should be as low as possible in order to minimize noise. Results similar to Equation 3 are obtained for the inverting configuration on if  $R_{seq}$  is replaced by  $R_b \parallel R_g$  is replaced by  $R_g + R_s$ . With these substitutions, Equation 3 will yield an  $e_{ni}$  referred to the non-inverting input. Referring  $e_{ni}$  to the inverting input is easily accomplished by multiplying  $e_{ni}$  by the ratio of non-inverting to inverting gains.

## Typical Application (continued)

### 7.2.2.3.1 Noise Figure

Noise Figure (NF) is a measure of the noise degradation caused by an amplifier.

$$NF = 10 \text{LOG} \left[ \frac{S_i/N_i}{S_o/N_o} \right] = 10 \text{LOG} \left[ \frac{e_{ni}^2}{e_t^2} \right] \quad (5)$$

The noise figure formula is shown in [Equation 5](#). The addition of a terminating resistor  $R_T$ , reduces the external thermal noise but increases the resulting NF.

The NF is increased because the  $R_T$  reduces the input signal amplitude thus reducing the input SNR.

$$\left[ \frac{e_n^2 + i_n^2 (R_{Seq} + (R_f \parallel R_g))^2 + 4KTR_{Seq} + 4kt (R_f \parallel R_g)}{4kTR_{Seq}} \right] \quad (6)$$

The noise figure is related to the equivalent source resistance ( $R_{Seq}$ ) and the parallel combination of  $R_f$  and  $R_g$ . To minimize noise figure, the following steps are recommended:

1. Minimize  $R_f \parallel R_g$
2. Choose the Optimum  $R_s$  ( $R_{OPT}$ )

$R_{OPT}$  is the point at which the NF curve reaches a minimum and is approximated by:

$$R_{OPT} \approx (e_n/i_n)$$

## 8 Power Supply Recommendations

### 8.1 Power Dissipation

The package power dissipation should be taken into account when operating at high ambient temperature and/or high power dissipative conditions. In determining maximum operable temperature of the device, make sure the total power dissipation of the device is considered; this power dissipated in the device with a load connected to the output as well as the nominal dissipation of the op amp.

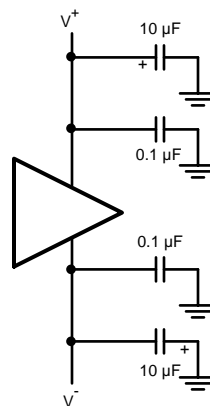
## 9 Layout

### 9.1 Layout Guidelines

With all high frequency devices, board layouts with stray capacitance have a strong influence on the AC performance. The LMH6654/LMH6655 are not exception and the inverting input and output pins are particularly sensitive to the coupling of parasitic capacitance to AC ground. Parasitic capacitances on the inverting input and output nodes to ground could cause frequency response peaking and possible circuit oscillation. Therefore, the power supply, ground traces and ground plan should be placed away from the inverting input and output pins. Also, it is very important to keep the parasitic capacitance across the feedback to an absolute minimum.

The PCB should have a ground plane covering all unused portion of the component side of the board to provide a low impedance path. All trace lengths should be minimized to reduce series inductance.

Supply bypassing is required for the amplifiers performance. The bypass capacitors provide a low impedance return current path at the supply pins. They also provide high frequency filtering on the power supply traces. It is recommended that a ceramic decoupling capacitor 0.1  $\mu\text{F}$  chip should be placed with one end connected to the ground plane and the other side as close as possible to the power pins. An additional 10  $\mu\text{F}$  tantalum electrolytic capacitor should be connected in parallel, to supply current for fast large signal changes at the output.



**Figure 46. Supply Bypass Capacitors**

#### 9.1.1 Evaluation Boards

TI provides the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization.

DEVICE	PACKAGE	EVALUATION BOARD PN
LMH6654MF	5-Pin SOT-23	LMH730216
LMH6654MA	8-Pin SOIC	LMH730227
LMH6655MA	8-Pin SOIC	LMH730036
LMH6655MM	8-Pin VSSOP (DGK)	LMH730123

Components Needed to Evaluate the LMH6654 on the LMH730227 Evaluation Board:

- $R_f$ ,  $R_g$  use the datasheet to select values.
- $R_{IN}$ ,  $R_{OUT}$  typically 50  $\Omega$  (Refer to the Basic Operation section of the evaluation board datasheet for details)
- $R_f$  is an optional resistor for inverting again configurations (select  $R_f$  to yield desired input impedance =  $R_g || R_f$ )
- $C_1$ ,  $C_2$  use 0.1  $\mu\text{F}$  ceramic capacitors
- $C_3$ ,  $C_4$  use 10  $\mu\text{F}$  tantalum capacitors

Components not used:

1.  $C_5$ ,  $C_6$ ,  $C_7$ ,  $C_8$
2. R1 thru R8

The evaluation boards are designed to accommodate dual supplies. The board can be modified to provide single operation. For best performance;

- 1) Do not connect the unused supply.
- 2) Ground the unused supply pin.

## 10 Device and Documentation Support

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

##### 10.1.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMH6654	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LMH6655	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 10.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 10.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6654MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH6654MA	<a href="#">Samples</a>
LMH6654MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH6654MA	<a href="#">Samples</a>
LMH6654MF	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	A66A	
LMH6654MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A66A	<a href="#">Samples</a>
LMH6654MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A66A	<a href="#">Samples</a>
LMH6655MA	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMH6655MA	
LMH6655MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH6655MA	<a href="#">Samples</a>
LMH6655MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH6655MA	<a href="#">Samples</a>
LMH6655MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A67A	<a href="#">Samples</a>
LMH6655MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A67A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6654MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6654MF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6654MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6654MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6655MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6655MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6655MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6654MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6654MF	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMH6654MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMH6654MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMH6655MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6655MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMH6655MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DBV0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/D 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

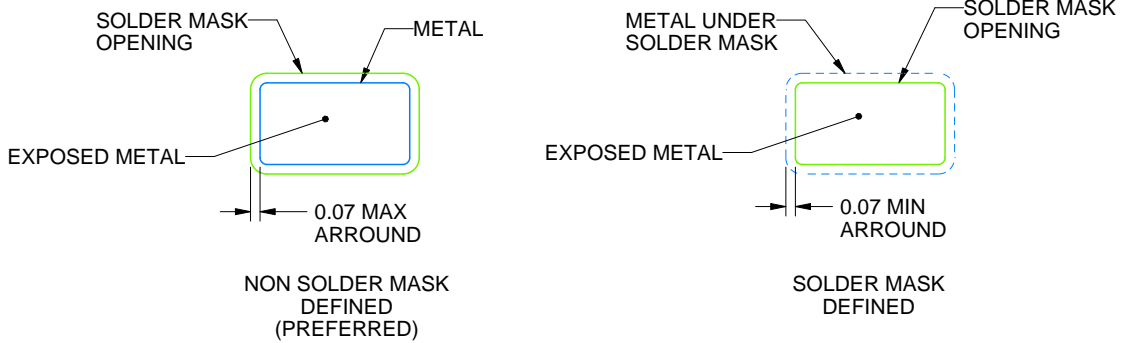
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

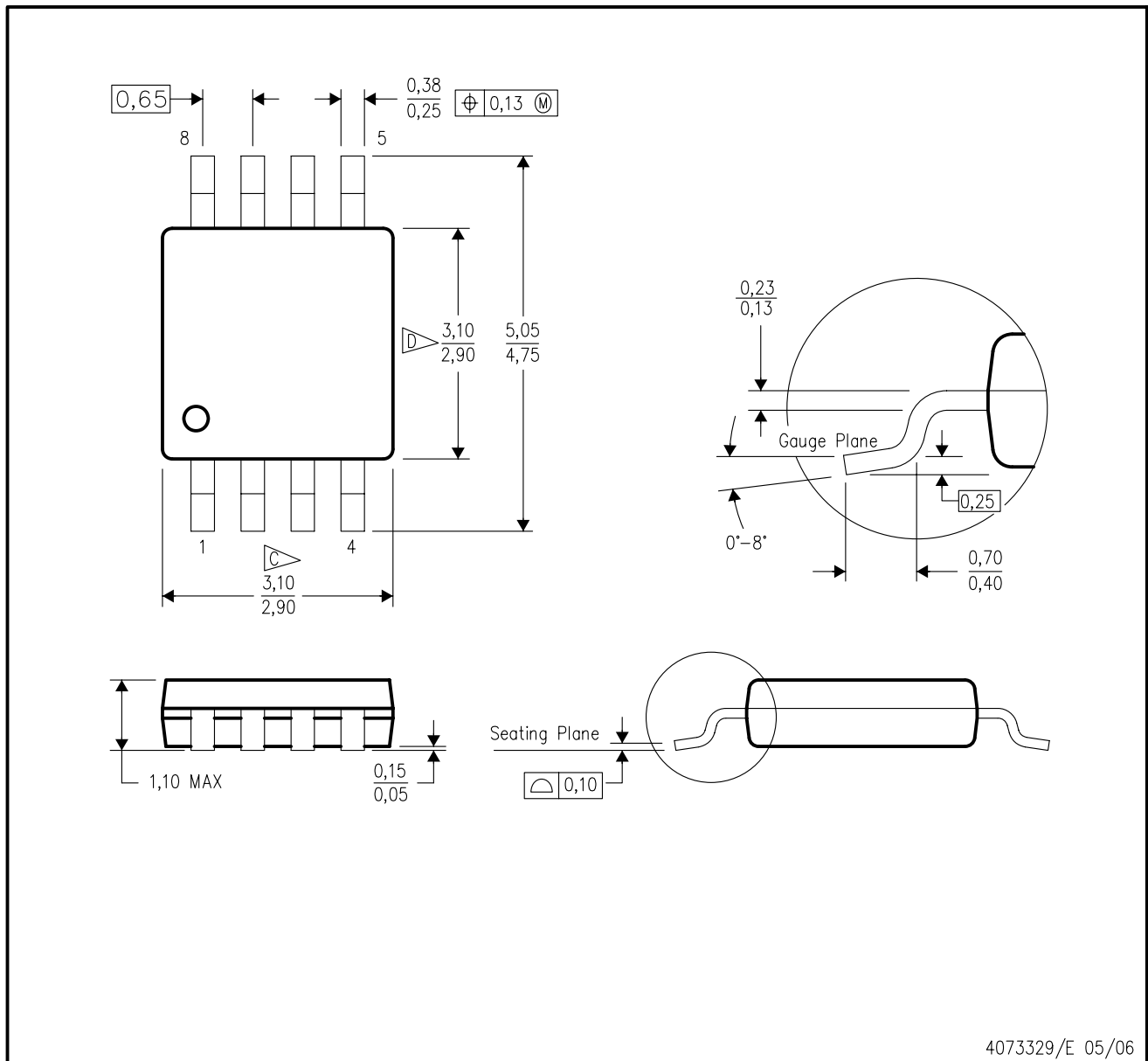
4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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