THE DATASHEET OF

LNK363PG

LNK362-364

LinkSwitch®-XT Family

Energy Efficient, Low Power Off-Line Switcher IC

Product Highlights

Optimized for Lowest System Cost

- Proprietary IC trimming and transformer construction techniques enable *Clampless*™ designs with LNK362 for lower system cost, component count and higher efficiency
- Fully integrated auto-restart for short circuit and open loop protection
- Self-biased supply – saves transformer auxiliary winding and associated bias supply components
- Frequency jittering greatly reduces EMI
- Meets HV creepage requirements between DRAIN and all other pins both on the PCB and at the package
- Lowest component count switcher solution

Features Superior to Linear/RCC

- Accurate hysteretic thermal shutdown protection – automatic recovery improves field reliability
- Universal input range allows worldwide operation
- Simple ON/OFF control, no loop compensation needed
- Eliminates bias winding – simpler, lower cost transformer
- Very low component count – higher reliability and single side printed circuit board
- Auto-restart reduces delivered power by 95% during short circuit and open loop fault conditions
- High bandwidth provides fast turn-on with no overshoot and excellent transient load response

EcoSmart® – Extremely Energy-Efficient

- Easily meets all global energy efficiency regulations with no added components
- No-load consumption <300 mW without bias winding at 265 VAC input (<50 mW with bias winding)
- ON/OFF control provides constant efficiency to very light loads – ideal for mandatory CEC regulations

Applications

- Chargers/adapters for cell/cordless phones, PDAs, digital cameras, MP3/portable audio players, and shavers
- Supplies for appliances, industrial systems, and metering

Description

LinkSwitch-XT incorporates a 700 V power MOSFET, oscillator, simple ON/OFF control scheme, a high-voltage switched current source, frequency jittering, cycle-by-cycle current limit and thermal shutdown circuitry onto a monolithic IC. The startup and operating power are derived directly from the DRAIN pin, eliminating the need for a bias winding and associated circuitry.

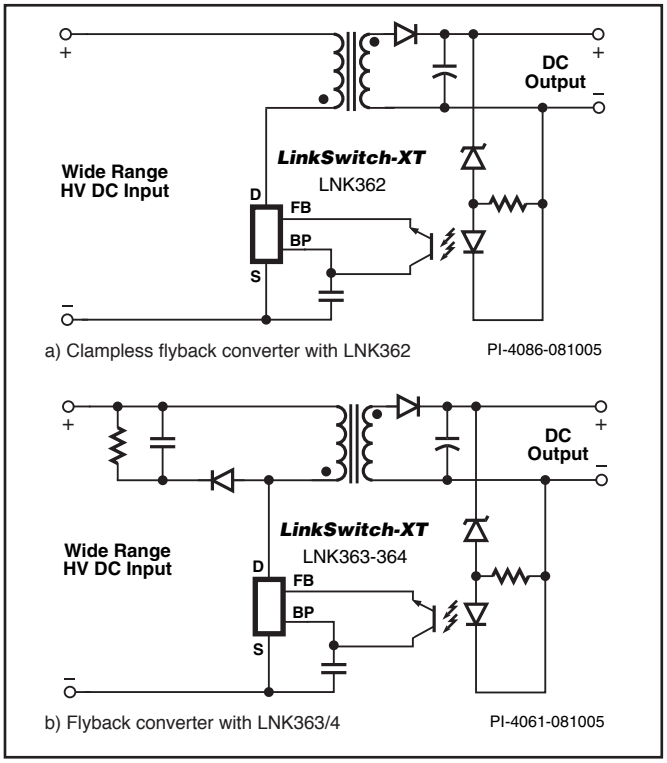


Figure 1. Typical Application with LinkSwitch-XT.

OUTPUT POWER TABLE(4)				
PRODUCT(3)	230 VAC ±15%		85-265 VAC	
	Adapter(1)	Open Frame(2)	Adapter(1)	Open Frame(2)
LNK362P/G/D	2.8 W	2.8 W	2.6 W	2.6 W
LNK363P/G/D	5 W	7.5 W	3.7 W	4.7 W
LNK364P/G/D	5.5 W	9 W	4 W	6 W

Table 1. Output Power Table.

Notes:
1. Minimum continuous power in a typical non-ventilated enclosed adapter measured at 50 °C ambient.
2. Minimum practical continuous power in an open frame design with adequate heat sinking, measured at 50 °C ambient.
3. Packages: P: DIP-8B, G: SMD-8B, D: SO-8C. Please see Part Ordering Information.
4. See Key Application Considerations section for complete description of assumptions.

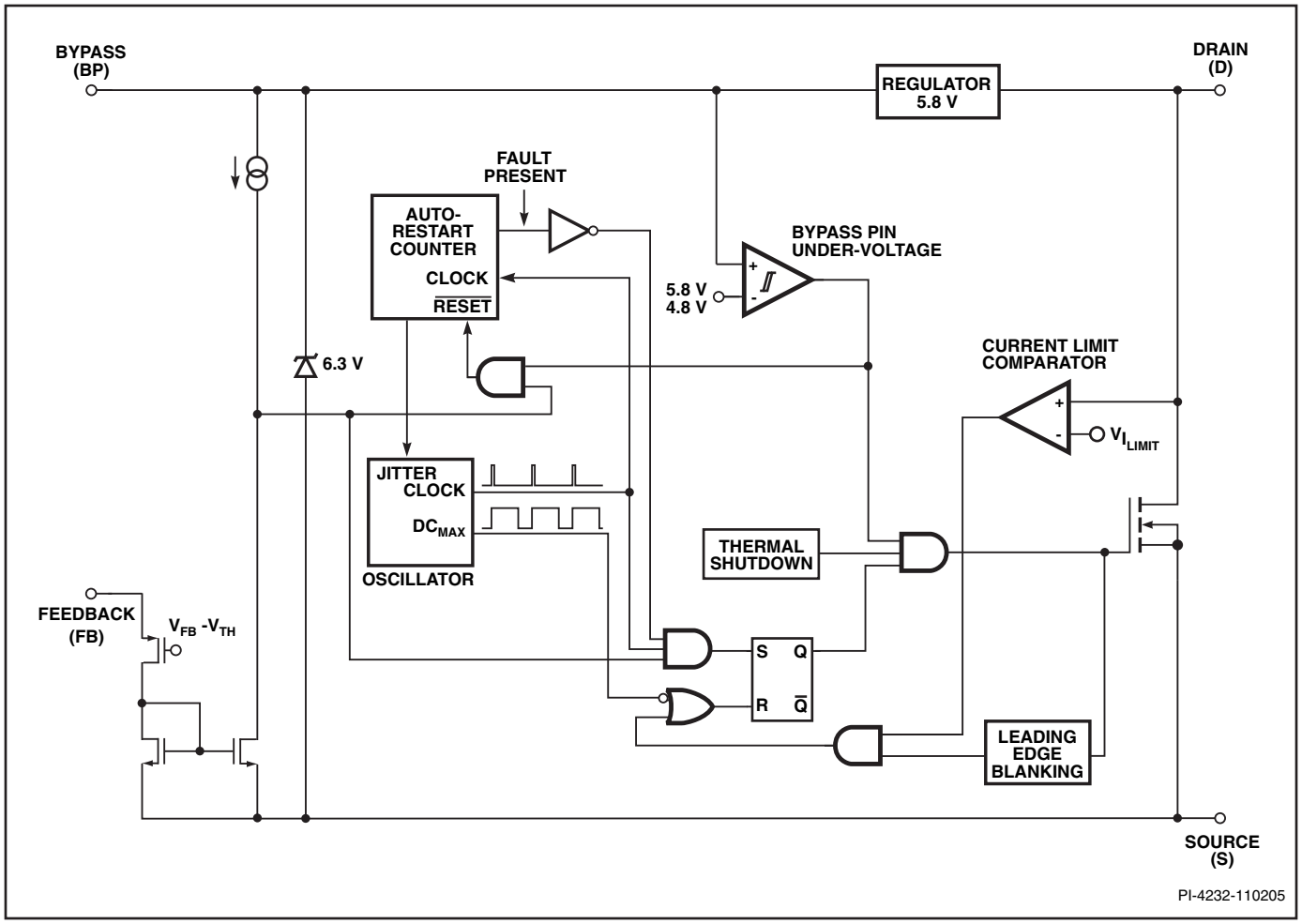


Figure 2. Functional Block Diagram.

Pin Functional Description

DRAIN (D) Pin:
Power MOSFET drain connection. Provides internal operating current for both startup and steady-state operation.

BYPASS (BP) Pin:
Connection point for a 0.1 µF external bypass capacitor for the internally generated 5.8 V supply. If an external bias winding is used, the current into the BP pin must not exceed 1 mA.

FEEDBACK (FB) Pin:
During normal operation, switching of the power MOSFET is controlled by this pin. MOSFET switching is disabled when a current greater than 49 µA is delivered into this pin.

SOURCE (S) Pin:
This pin is the power MOSFET source connection. It is also the ground reference for the BYPASS and FEEDBACK pins.

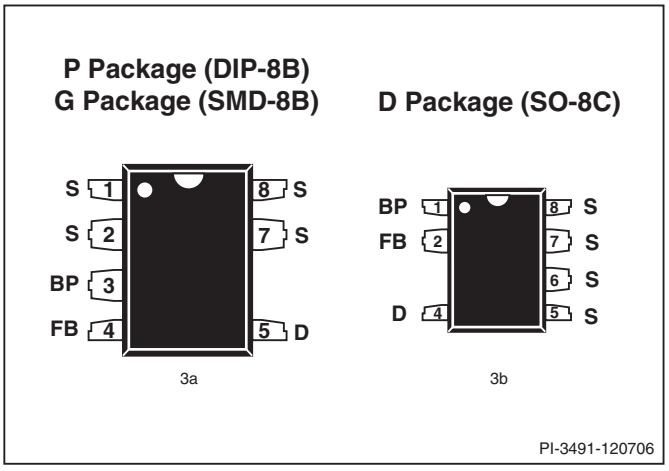


Figure 3. Pin Configuration.

LinkSwitch-XT Functional Description

LinkSwitch-XT combines a high-voltage power MOSFET switch with a power supply controller in one device. Unlike conventional PWM (pulse width modulator) controllers, a simple ON/OFF control regulates the output voltage. The controller consists of an oscillator, feedback (sense and logic) circuit, 5.8 V regulator, BYPASS pin undervoltage circuit, over-temperature protection, frequency jittering, current limit circuit, and leading edge blanking integrated with a 700 V power MOSFET. The *LinkSwitch-XT* incorporates additional circuitry for auto-restart.

Oscillator

The typical oscillator frequency is internally set to an average of 132 kHz. Two signals are generated from the oscillator: the maximum duty cycle signal (DC_{MAX}) and the clock signal that indicates the beginning of each cycle.

The oscillator incorporates circuitry that introduces a small amount of frequency jitter, typically 9 kHz peak-to-peak, to minimize EMI emission. The modulation rate of the frequency jitter is set to 1.5 kHz to optimize EMI reduction for both average and quasi-peak emissions. The frequency jitter should be measured with the oscilloscope triggered at the falling edge of the DRAIN waveform. The waveform in Figure 4 illustrates the frequency jitter.

Feedback Input Circuit

The feedback input circuit at the FB pin consists of a low impedance source follower output set at 1.65 V for LNK362 and 1.63 V for LNK363/364. When the current delivered into this pin exceeds 49 µA, a low logic level (disable) is generated at the output of the feedback circuit. This output is sampled at the beginning of each cycle on the rising edge of the clock signal. If high, the power MOSFET is turned on for that cycle (enabled), otherwise the power MOSFET remains off (disabled). Since the sampling is done only at the beginning of each cycle, subsequent changes in the FB pin voltage or current during the remainder of the cycle are ignored.

5.8 V Regulator and 6.3 V Shunt Voltage Clamp

The 5.8 V regulator charges the bypass capacitor connected to the BYPASS pin to 5.8 V by drawing a current from the voltage on the DRAIN, whenever the MOSFET is off. The BYPASS pin is the internal supply voltage node. When the MOSFET is on, the *LinkSwitch-XT* runs off of the energy stored in the bypass capacitor. Extremely low power consumption of the internal circuitry allows the device to operate continuously from the current drawn from the DRAIN pin. A bypass capacitor value of 0.1 µF is sufficient for both high frequency decoupling and energy storage.

In addition, there is a 6.3 V shunt regulator clamping the BYPASS pin at 6.3 V when current is provided to the BYPASS pin through an external resistor. This facilitates powering of the device externally through a bias winding to decrease the no-load consumption to less than 50 mW.

BYPASS Pin Undervoltage

The BYPASS pin undervoltage circuitry disables the power MOSFET when the BYPASS pin voltage drops below 4.8 V. Once the BYPASS pin voltage drops below 4.8 V, it must rise back to 5.8 V to enable (turn-on) the power MOSFET.

Over-Temperature Protection

The thermal shutdown circuitry senses the die temperature. The threshold is set at 142 °C typical with a 75 °C hysteresis. When the die temperature rises above this threshold (142 °C) the power MOSFET is disabled and remains disabled until the die temperature falls by 75 °C, at which point it is re-enabled.

Current Limit

The current limit circuit senses the current in the power MOSFET. When this current exceeds the internal threshold (I_{LIMIT}), the power MOSFET is turned off for the remainder of that cycle. The leading edge blanking circuit inhibits the current limit comparator for a short time (t_{LEB}) after the power MOSFET is turned on. This leading edge blanking time has been set so that current spikes caused by capacitance and rectifier reverse recovery time will not cause premature termination of the switching pulse.

Auto-Restart

In the event of a fault condition such as output overload, output short circuit, or an open loop condition, *LinkSwitch-XT* enters into auto-restart operation. An internal counter clocked by the oscillator gets reset every time the FB pin is pulled high. If the FB pin is not pulled high for approximately 40 ms, the power MOSFET switching is disabled for 800 ms. The auto-restart alternately enables and disables the switching of the power MOSFET until the fault condition is removed.

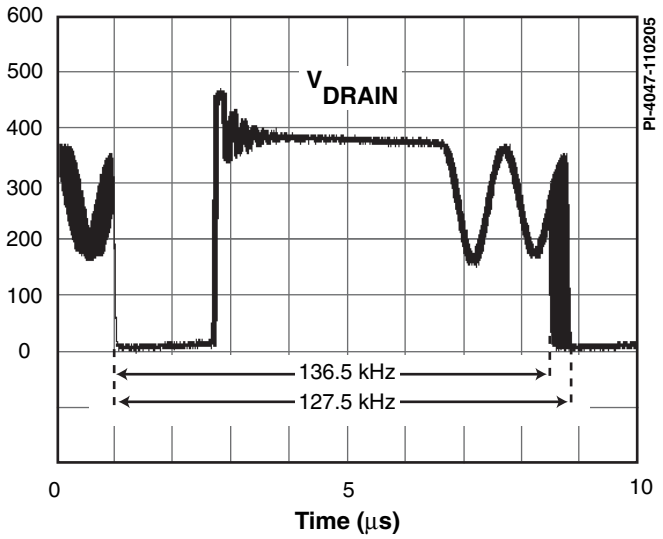


Figure 4. Frequency Jitter.

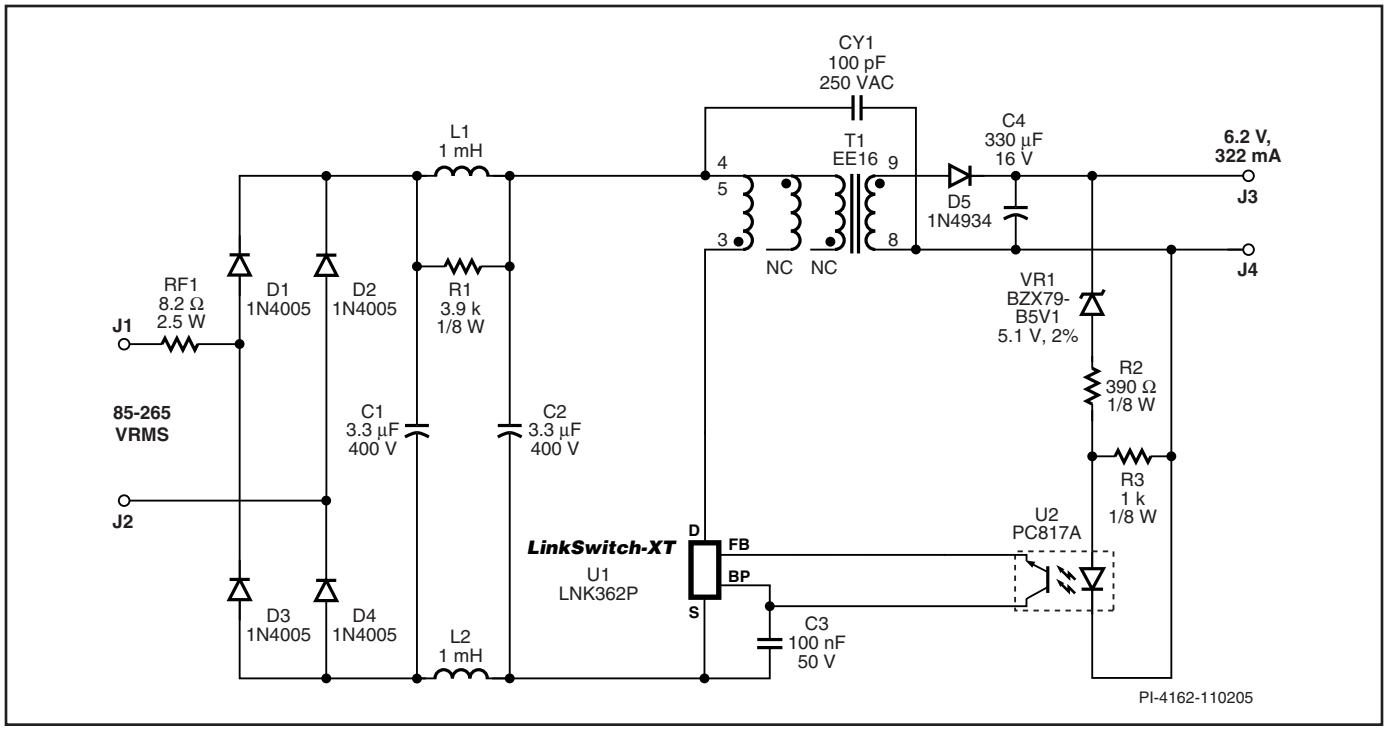


Figure 5. 2 W Universal Input CV Adapter Using LNK362.

Applications Example

A 2 W CV Adapter

The schematic shown in Figure 5 is a typical implementation of a universal input, 6.2 V ±7%, 322 mA adapter using LNK362. This circuit makes use of the *Clampless* technique to eliminate the primary clamp components and reduce the cost and complexity of the circuit.

The *EcoSmart* features built into the *LinkSwitch-XT* family allow this design to easily meet all current and proposed energy efficiency standards, including the mandatory California Energy Commission (CEC) requirement for average operating efficiency.

The AC input is rectified by D1 to D4 and filtered by the bulk storage capacitors C1 and C2. Resistor RF1 is a flameproof, fusible, wire wound type and functions as a fuse, inrush current limiter and, together with the π filter formed by C1, C2, L1 and L2, differential mode noise attenuator. Resistor R1 damps ringing caused by L1 and L2.

This simple input stage, together with the frequency jittering of *LinkSwitch-XT*, a low value Y1 capacitor and PI's *E-Shield*™ windings within T1, allow the design to meet both conducted and radiated EMI limits with >10 dBµV margin. The low value of CY1 is important to meet the requirement for a very low touch current (the line frequency current that flows through CY1) often specified for adapters, in this case <10 µA.

The rectified and filtered input voltage is applied to the primary winding of T1. The other side of the primary is driven by the integrated MOSFET in U1. No primary clamp is required as the low value and tight tolerance of the LNK362 internal current limit allows the transformer primary winding capacitance to provide adequate clamping of the leakage inductance drain voltage spike.

The secondary of the flyback transformer T1 is rectified by D5, a low cost, fast recovery diode, and filtered by C4, a low ESR capacitor. The combined voltage drop across VR1, R2 and the LED of U2 determines the output voltage. When the output voltage exceeds this level, current will flow through the LED of U2. As the LED current increases, the current fed into the FEEDBACK pin of U1 increases until the turnoff threshold current (~49 µA) is reached, disabling further switching cycles of U1. At full load, almost all switching cycles will be enabled, and at very light loads, almost all the switching cycles will be disabled, giving a low effective frequency and providing high light load efficiency and low no-load consumption.

Resistor R3 provides 1 mA through VR1 to bias the Zener closer to its test current. Resistor R2 allows the output voltage to be adjusted to compensate for designs where the value of the Zener may not be ideal, as they are only available in discrete voltage ratings. For higher output accuracy, the Zener may be replaced with a reference IC such as the TL431.

The *LinkSwitch-XT* is completely self-powered from the DRAIN pin, requiring only a small ceramic capacitor C3 connected to the BYPASS pin. No auxiliary winding on the transformer is required.

Key Application Considerations

LinkSwitch-XT Design Considerations

Output Power Table

The data sheet maximum output power table (Table 1) represents the maximum practical continuous output power level that can be obtained under the following assumed conditions:

1. The minimum DC input voltage is 90 V or higher for 85 VAC input, or 240 V or higher for 230 VAC input or 115 VAC with a voltage doubler. The value of the input capacitance should be large enough to meet these criteria for AC input designs.
2. Secondary output of 6 V with a fast PN rectifier diode.
3. Assumed efficiency of 70%.
4. Voltage only output (no secondary-side constant current circuit).
5. Discontinuous mode operation (K_p >1).
6. A primary clamp (RCD or Zener) is used.
7. The part is board mounted with SOURCE pins soldered to a sufficient area of copper to keep the SOURCE pin temperature at or below 100 °C.
8. Ambient temperature of 50 °C for open frame designs and an internal enclosure temperature of 60 °C for adapter designs.

Below a value of 1, K_P is the ratio of ripple to peak primary current. Above a value of 1, K_P is the ratio of primary MOSFET OFF time to the secondary diode conduction time. Due to the flux density requirements described below, typically a *LinkSwitch-XT* design will be discontinuous, which also has the benefits of allowing lower cost fast (instead of ultra-fast) output diodes and reducing EMI.

***Clampless* Designs**

Clampless designs rely solely on the drain node capacitance to limit the leakage inductance induced peak drain-to-source voltage. Therefore, the maximum AC input line voltage, the value of V_{OR}, the leakage inductance energy, a function of leakage inductance and peak primary current, and the primary winding capacitance determine the peak drain voltage. With no significant dissipative element present, as is the case with an external clamp, the longer duration of the leakage inductance ringing can increase EMI.

The following requirements are recommended for a universal input or 230 VAC only *Clampless* design:

1. A *Clampless* design should only be used for $P_O \leq 2.5$ W, using the LNK362† and a V_{OR}** ≤ 90 V.
2. For designs where $P_O \leq 2$ W, a two-layer primary should be used to ensure adequate primary intra-winding capacitance in the range of 25 pF to 50 pF.
3. For designs where $2 < P_O \leq 2.5$ W, a bias winding should be added to the transformer using a standard recovery rectifier diode to act as a clamp. This bias winding may also be used to externally power the device by connecting a resistor from the bias-winding capacitor to the BYPASS pin. This inhibits the internal high-voltage current source, reducing device dissipation and no-load consumption.
4. For designs where $P_O > 2.5$ W *Clampless* designs are not practical and an external RCD or Zener clamp should be used.
5. Ensure that worst-case high line, peak drain voltage is below the BV_{DSS} specification of the internal MOSFET and ideally ≤ 650 V to allow margin for design variation.

†For 110 VAC only input designs it may be possible to extend the power range of *Clampless* designs to include the LNK363. However, the increased leakage ringing may degrade EMI performance.

**V_{OR} is the secondary output plus output diode forward voltage drop that is reflected to the primary via the turns ratio of the transformer during the diode conduction time. The V_{OR} adds to the DC bus voltage and the leakage spike to determine the peak drain voltage.

Audible Noise

The cycle skipping mode of operation used in *LinkSwitch-XT* can generate audio frequency components in the transformer. To limit this audible noise generation, the transformer should be designed such that the peak core flux density is below 1500 Gauss (150 mT). Following this guideline and using the standard transformer production technique of dip varnishing practically eliminates audible noise. Vacuum impregnation of the transformer should not be used due to the high primary capacitance and increased losses that result. Higher flux densities are possible, however careful evaluation of the audible noise performance should be made using production transformer samples before approving the design.

Ceramic capacitors that use dielectrics, such as Z5U, when used in clamp circuits may also generate audio noise. If this is the case, try replacing them with a capacitor having a different dielectric or construction, for example a film type.

LinkSwitch-XT Layout Considerations

See Figure 6 for a recommended circuit board layout for *LinkSwitch-XT* (P & G package).

Single Point Grounding

Use a single point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pins.

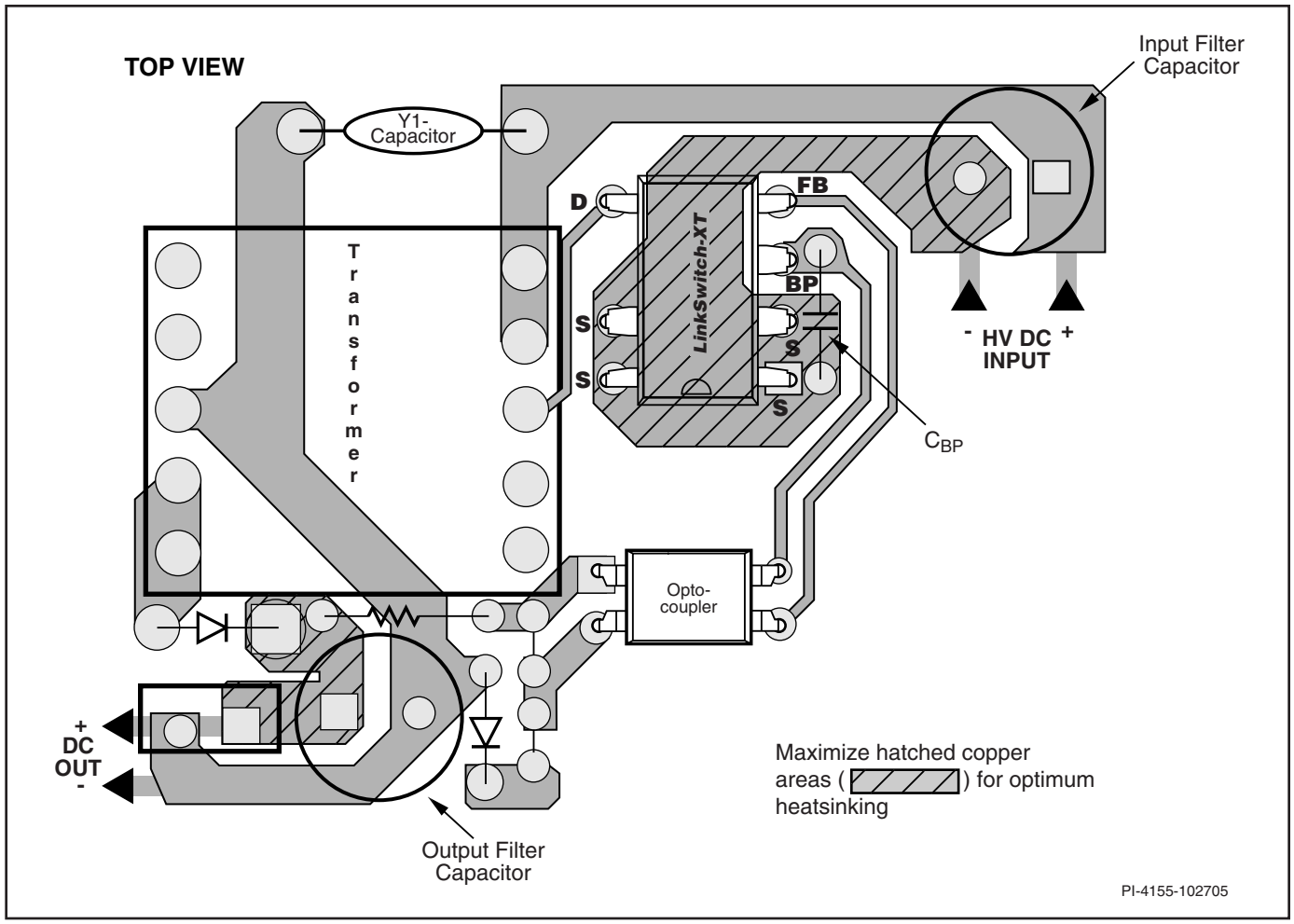


Figure 6. Recommended Printed Circuit Layout for LinkSwitch-XT using P Package in a Flyback Converter Configuration.

Bypass Capacitor C_{BP}
The BYPASS pin capacitor should be located as near as possible to the BYPASS and SOURCE pins.

Primary Loop Area
The area of the primary loop that connects the input filter capacitor, transformer primary and *LinkSwitch-XT* together should be kept as small as possible.

Primary Clamp Circuit
A clamp is used to limit peak voltage on the DRAIN pin at turn-off. This can be achieved by using an RCD clamp or a Zener (~200 V) and diode clamp across the primary winding. In all cases, to minimize EMI, care should be taken to minimize the circuit path from the clamp components to the transformer and *LinkSwitch-XT*.

Thermal Considerations
The copper area underneath the *LinkSwitch-XT* acts not only as a single point ground, but also as a heatsink. As this area is connected to the quiet source node, it should be maximized for good heat sinking of *LinkSwitch-XT*. The same applies to the cathode of the output diode.

Y-Capacitor
The placement of the Y-type cap should be directly from the primary input filter capacitor positive terminal to the common/return terminal of the transformer secondary. Such a placement will route high magnitude common-mode surge currents away from the *LinkSwitch-XT* device. Note that if an input pi (C, L, C) EMI filter is used, then the inductor in the filter should be placed between the negative terminals of the input filter capacitors.

Optocoupler
Place the optocoupler physically close to the *LinkSwitch-XT* to minimize the primary-side trace lengths. Keep the high current, high-voltage drain and clamp traces away from the optocoupler to prevent noise pick up.

Output Diode
For best performance, the area of the loop connecting the secondary winding, the output diode and the output filter

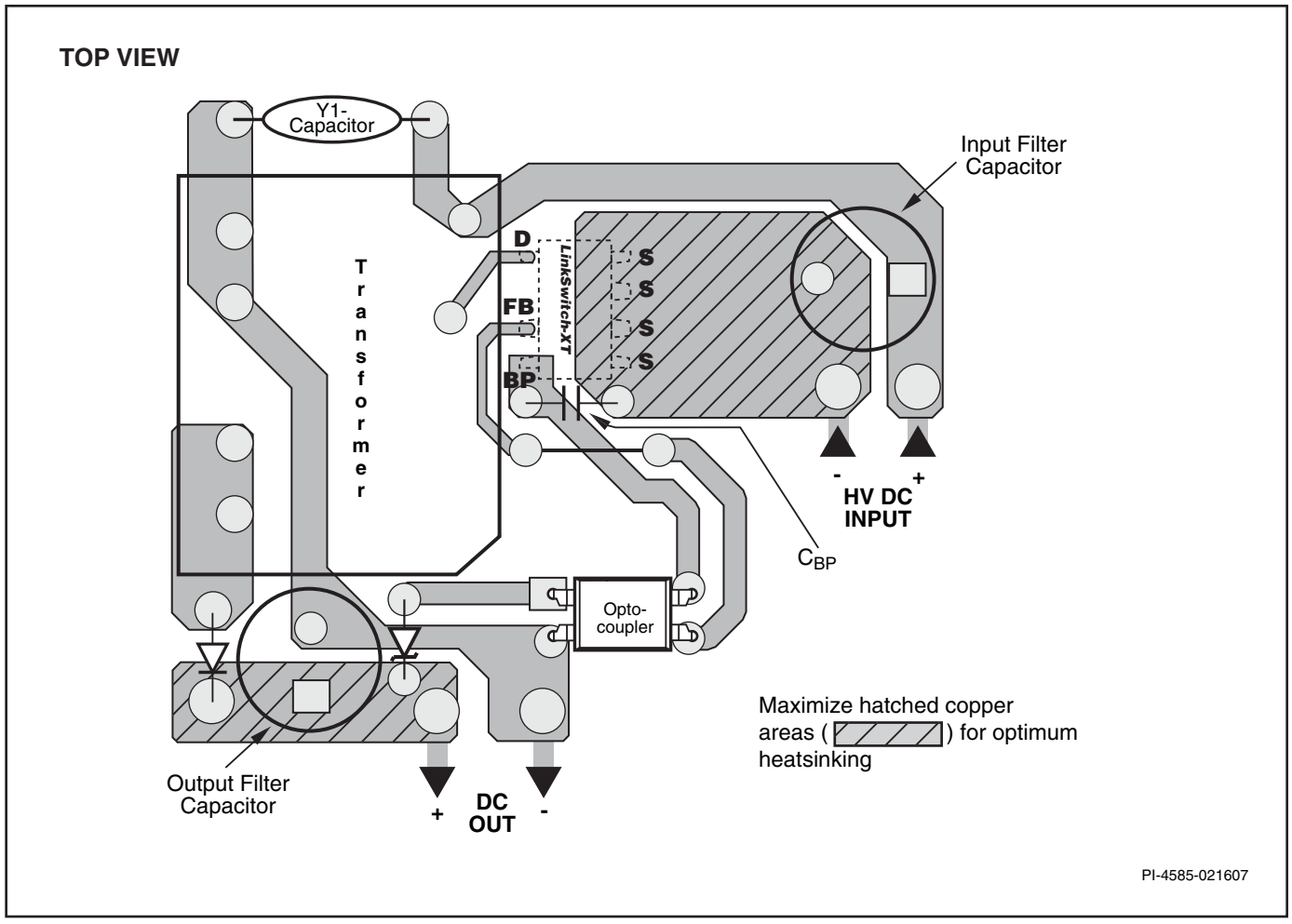


Figure 7. Recommended Printed Circuit Layout for LinkSwitch-XT using D Package in a Flyback Converter Configuration.

capacitor should be minimized. In addition, sufficient copper area should be provided at the anode and cathode terminals of the diode for heat sinking. A larger area is preferred at the quiet cathode terminal. A large anode area can increase high frequency radiated EMI.

Quick Design Checklist

As with any power supply design, all *LinkSwitch-XT* designs should be verified on the bench to make sure that component specifications are not exceeded under worst-case conditions. The following minimum set of tests is strongly recommended:

1. Maximum drain voltage – Verify that V_{DS} does not exceed 650 V at the highest input voltage and peak (overload) output power. The 50 V margin to the 700 V BV_{DSS} specification gives margin for design variation, especially in *Clampless* designs.
2. Maximum drain current – At maximum ambient temperature, maximum input voltage and peak output (overload) power, verify drain current waveforms for any signs of transformer saturation and excessive leading-edge current spikes at startup. Repeat under steady state conditions and verify that the leading-edge current spike event is below $I_{LIMIT(MIN)}$ at the end of the $t_{LEB(MIN)}$. Under all conditions, the maximum drain current should be below the specified absolute maximum ratings.
3. Thermal Check – At specified maximum output power, minimum input voltage and maximum ambient temperature, verify that the temperature specifications are not exceeded for *LinkSwitch-XT*, transformer, output diode and output capacitors. Enough thermal margin should be allowed for part-to-part variation of the $R_{DS(ON)}$ of *LinkSwitch-XT* as specified in the data sheet. Under low line, maximum power, a maximum *LinkSwitch-XT* SOURCE pin temperature of 105 °C is recommended to allow for these variations.

Design Tools

Up-to-date information on design tools can be found at the Power Integrations web site: www.powerint.com.

ABSOLUTE MAXIMUM RATINGS(1,5)

DRAIN Voltage .....-0.3 V to 700 V
Peak DRAIN Current: LNK362.....200 mA (375 mA)(2)
LNK363/364.....400 mA (750 mA)(2)
FEEDBACK Voltage .....-0.3 V to 9 V
FEEDBACK Current .....100 mA
BYPASS Voltage.....-0.3 V to 9 V
Storage Temperature .....-65 °C to 150 °C
Operating Junction Temperature(3) .....-40 °C to 150 °C
Lead Temperature(4) ..... 260 °C

Notes:
1. All voltages referenced to SOURCE, T_A = 25 °C.
2. The higher peak DRAIN current is allowed while the DRAIN voltage is simultaneously less than 400 V.
3. Normally limited by internal circuitry.
4. 1/16 in. from case for 5 seconds.
5. Maximum ratings specified may be applied, one at a time, without causing permanent damage to the product. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect product reliability.

THERMAL IMPEDANCE

Thermal Impedance: P or G Package:
(θ_{JA}) ..... 70 °C/W(3); 60 °C/W(4)
(θ_{JC})(1) ..... 11 °C/W
D Package:
(θ_{JA}) .... 100 °C/W(3); 80 °C/W(4)
(θ_{JC})(2) ..... 30 °C/W

Notes:
1. Measured on pin 2 (SOURCE) close to plastic interface.
2. Measured on pin 8 (SOURCE) close to plastic interface.
3. Soldered to 0.36 sq. in. (232 mm^2), 2 oz. (610 g/m^2) copper clad.
4. Soldered to 1 sq. in. (645 mm^2), 2 oz. (610 g/m^2) copper clad.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 8 (Unless Otherwise Specified)		Min	Typ	Max	Units
CONTROL FUNCTIONS							
Output Frequency	f_{OSC}	T_J = 25 °C	Average	124	132	140	kHz
			Peak-Peak Jitter		9		
Maximum Duty Cycle	DC_{MAX}	S2 Open		60			%
FEEDBACK Pin Turnoff Threshold Current	I_{FB}	T_J = 25 °C		30	49	68	µA
FEEDBACK Pin Voltage at Turnoff Threshold	V_{FB}	T_J = 0 °C to 125 °C	LNK362	1.55	1.65	1.75	V
			LNK363-364	1.53	1.63	1.73	
DRAIN Supply Current	I_{S1}	V_{FB} ≥2 V (MOSFET Not Switching) See Note A			200	250	µA
	I_{S2}	FEEDBACK Open (MOSFET Switching)			250	300	µA
BYPASS Pin Charge Current	I_{CH1}	V_{BP} = 0 V, T_J = 25 °C See Note C		-5.5	-3.5	-1.8	mA
	I_{CH2}	V_{BP} = 4 V, T_J = 25 °C See Note C		-3.8	-2.3	-1.0	
BYPASS Pin Voltage	V_{BP}			5.55	5.8	6.10	V
BYPASS Pin Voltage Hysteresis	V_{BPH}			0.8	1.0	1.2	V

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 8 (Unless Otherwise Specified)		Min	Typ	Max	Units
CONTROL FUNCTIONS (cont)							
BYPASS Pin Supply Current	I_{BPSC}	See Note D		68			µA
CIRCUIT PROTECTION							
Current Limit	I_{LIMIT} (See Note E)	di/dt = 30 mA/µs T_J = 25 °C	LNK362	130	140	150	mA
		di/dt = 42 mA/µs T_J = 25 °C	LNK363	195	210	225	
		di/dt = 50 mA/µs T_J = 25 °C	LNK364	233	250	268	
Power Coefficient	I^2f	di/dt = 30 mA/µs T_J = 25 °C	LNK362	2199	2587		A^2Hz
		di/dt = 42 mA/µs T_J = 25 °C	LNK363	4948	5821		
		di/dt = 50 mA/µs T_J = 25 °C	LNK364	7425	8250		
Leading Edge Blanking Time	t_{LEB}	T_J = 25 °C See Note F	LNK362	300	375		ns
			LNK363/364	170	250		
Current Limit Delay	t_{ILD}	T_J = 25 °C See Note F			125		ns
Thermal Shutdown Temperature	T_{SD}			135	142	150	°C
Thermal Shutdown Hysteresis	T_{SHD}	See Note G			75		°C
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	LNK362 I_D = 14 mA	T_J = 25 °C		48	55	Ω
			T_J = 100 °C		76	88	
		LNK363 I_D = 21 mA	T_J = 25 °C		29	33	
			T_J = 100 °C		46	54	
		LNK364 I_D = 25 mA	T_J = 25 °C		24	28	
			T_J = 100 °C		38	45	
OFF-State Drain Leakage Current	I_{DSS}	V_{BP} = 6.2 V, V_{FB} ≥2 V, V_{DS} = 560 V, T_J = 125 °C				50	µA

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 8 (Unless Otherwise Specified)		Min	Typ	Max	Units
OUTPUT (cont)							
Breakdown Voltage	BV_{DSS}	V_{BP} = 6.2 V, V_{FB} ≥ 2 V, See Note H, T_J = 25 °C		700			V
DRAIN Supply Voltage				50			V
Output Enable Delay	t_{EN}	See Figure 10				10	µs
Output Disable Setup Time	t_{DST}				0.5		µs
Auto-Restart ON-Time	t_{AR}	T_J = 25 °C See Note I	LNK362		40		ms
			LNK363-364		45		
Auto-Restart Duty Cycle	DC_{AR}				5		%

NOTES:

A. Total current consumption is the sum of I_{S1} and I_{DSS} when FEEDBACK pin voltage is ≥2 V (MOSFET not switching) and the sum of I_{S2} and I_{DSS} when FEEDBACK pin is shorted to SOURCE (MOSFET switching).

B Since the output MOSFET is switching, it is difficult to isolate the switching current from the supply current at the DRAIN. An alternative is to measure the BYPASS pin current at 6 V.

C. See Typical Performance Characteristics section Figure 15 for BYPASS pin startup charging waveform.

D. This current is only intended to supply an optional optocoupler connected between the BYPASS and FEEDBACK pins and not any other external circuitry.

E. For current limit at other di/dt values, refer to Figure 14.

F. This parameter is guaranteed by design.

G. This parameter is derived from characterization.

H. Breakdown voltage may be checked against minimum BV_{DSS} specification by ramping the DRAIN pin voltage up to but not exceeding minimum BV_{DSS}.

I. Auto-restart on time has the same temperature characteristics as the oscillator (inversely proportional to frequency).

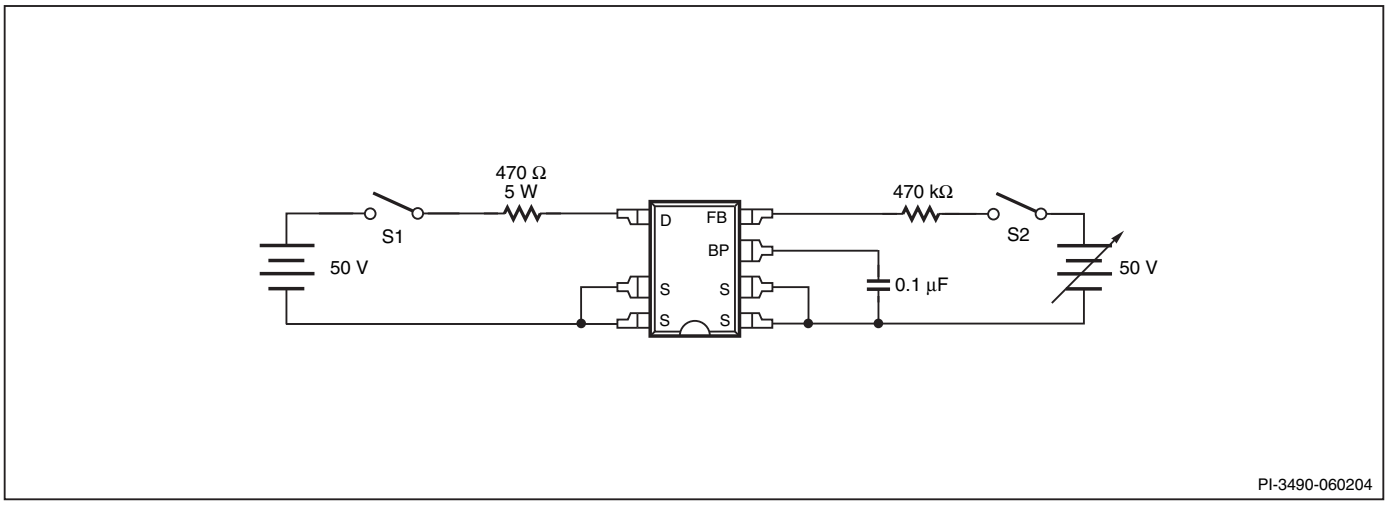


Figure 8. LinkSwitch-XT General Test Circuit.

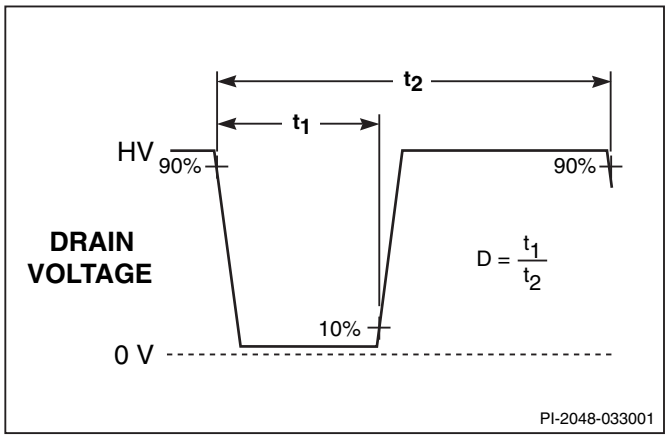


Figure 9. LinkSwitch-XT Duty Cycle Measurement.

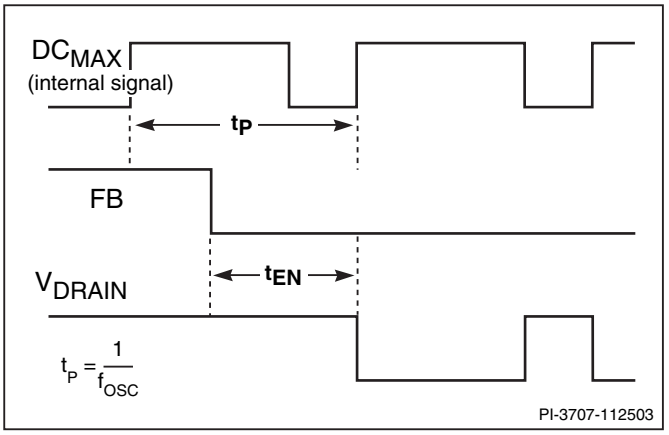


Figure 10. LinkSwitch-XT Output Enable Timing.

Typical Performance Characteristics

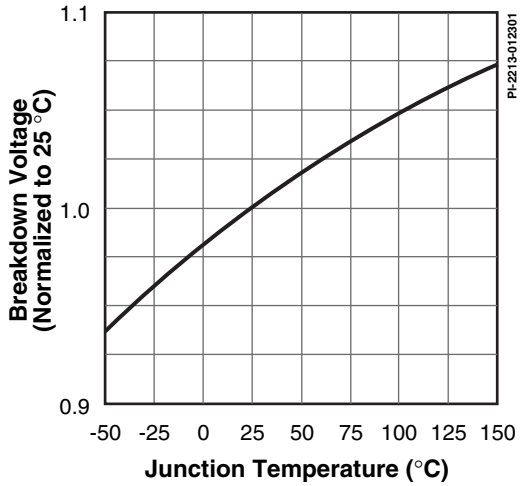


Figure 11. Breakdown vs. Temperature.

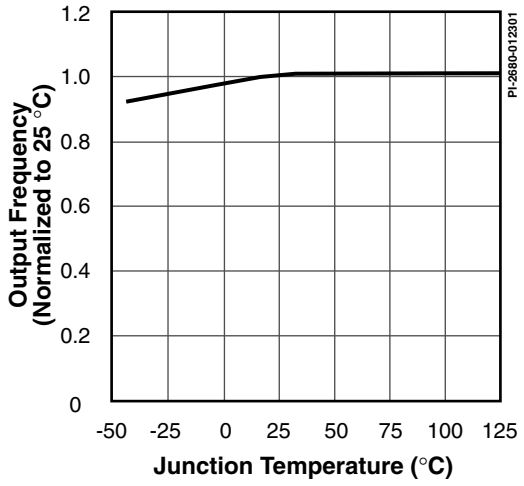


Figure 12. Frequency vs. Temperature.

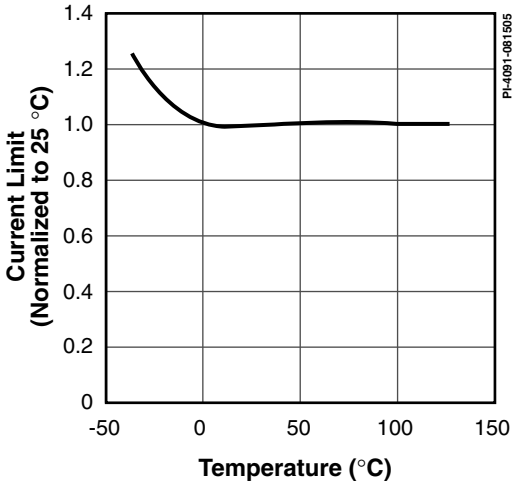


Figure 13. Current Limit vs. Temperature.

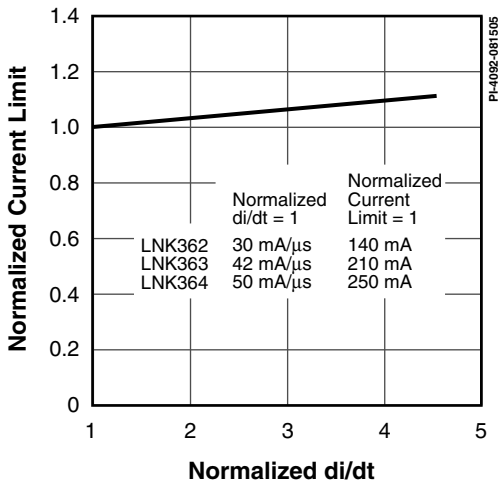


Figure 14. Current Limit vs. di/dt.

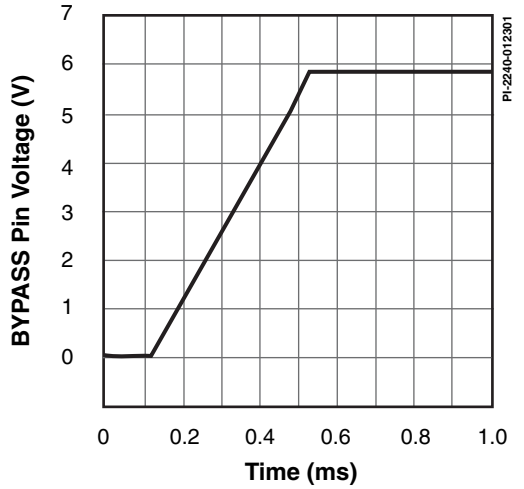


Figure 15. BYPASS Pin Startup Waveform.

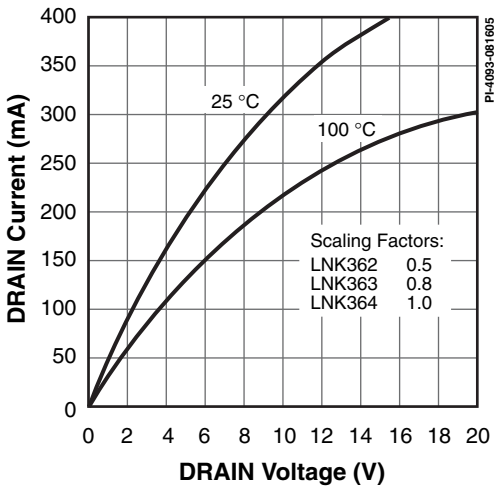


Figure 16. Output Characteristics.

Typical Performance Characteristics (cont.)

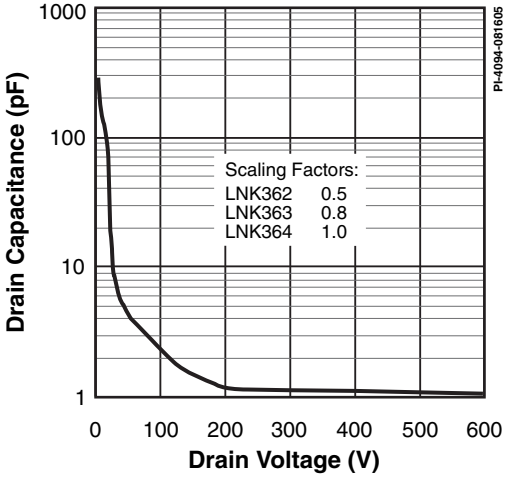


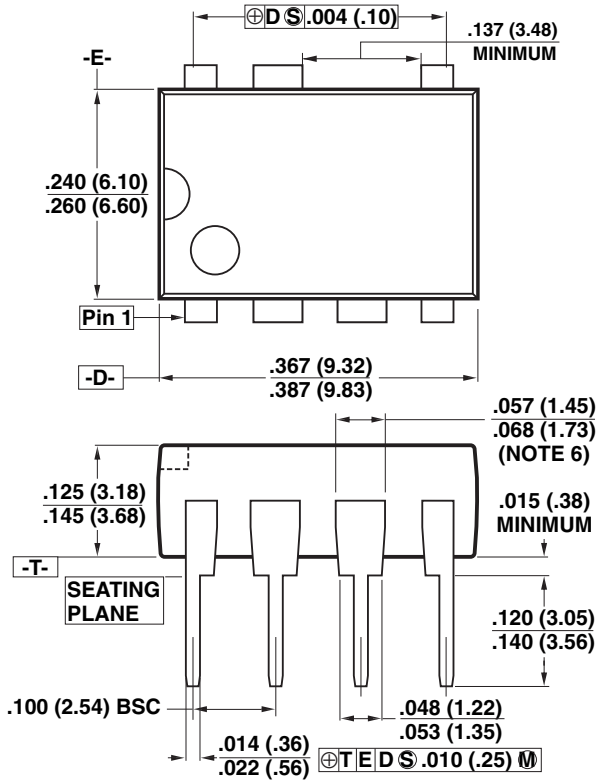
Figure 17. C_{OSS} vs. Drain Voltage.

PART ORDERING INFORMATION

LNK 364 G N - TL

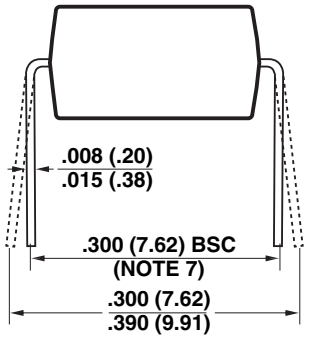
***LinkSwitch* Product Family**	
XT Series Number	
Package Identifier	
G	Plastic Surface Mount DIP
P	Plastic DIP
D	Plastic SO-8
Lead Finish	
N	Pure Matte Tin (RoHS Compliant)
G	RoHS Compliant and Halogen Free (P and D package only)
Tape & Reel and Other Options	
Blank	Standard Configurations
TL	Tape & Reel, 1 k pcs minimum for G Package. 2.5 k pcs for D Package. Not available for P Package.

DIP-8B



Notes:

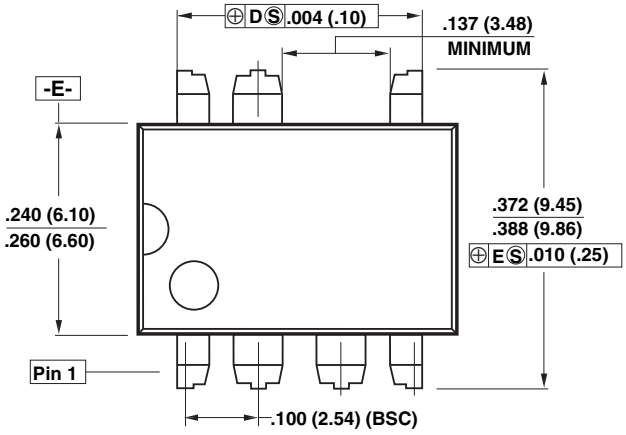
1. Package dimensions conform to JEDEC specification MS-001-AB (Issue B 7/85) for standard dual-in-line (DIP) package with .300 inch row spacing.
2. Controlling dimensions are inches. Millimeter sizes are shown in parentheses.
3. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
4. Pin locations start with Pin 1, and continue counter-clockwise to Pin 8 when viewed from the top. The notch and/or dimple are aids in locating Pin 1. Pin 6 is omitted.
5. Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).
6. Lead width measured at package body.
7. Lead spacing measured with the leads constrained to be perpendicular to plane T.

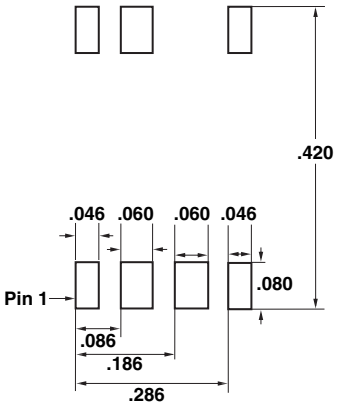


P08B

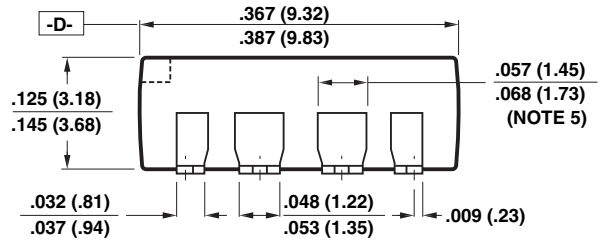
PI-2551-121504

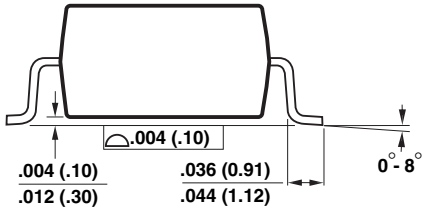
SMD-8B





Solder Pad Dimensions





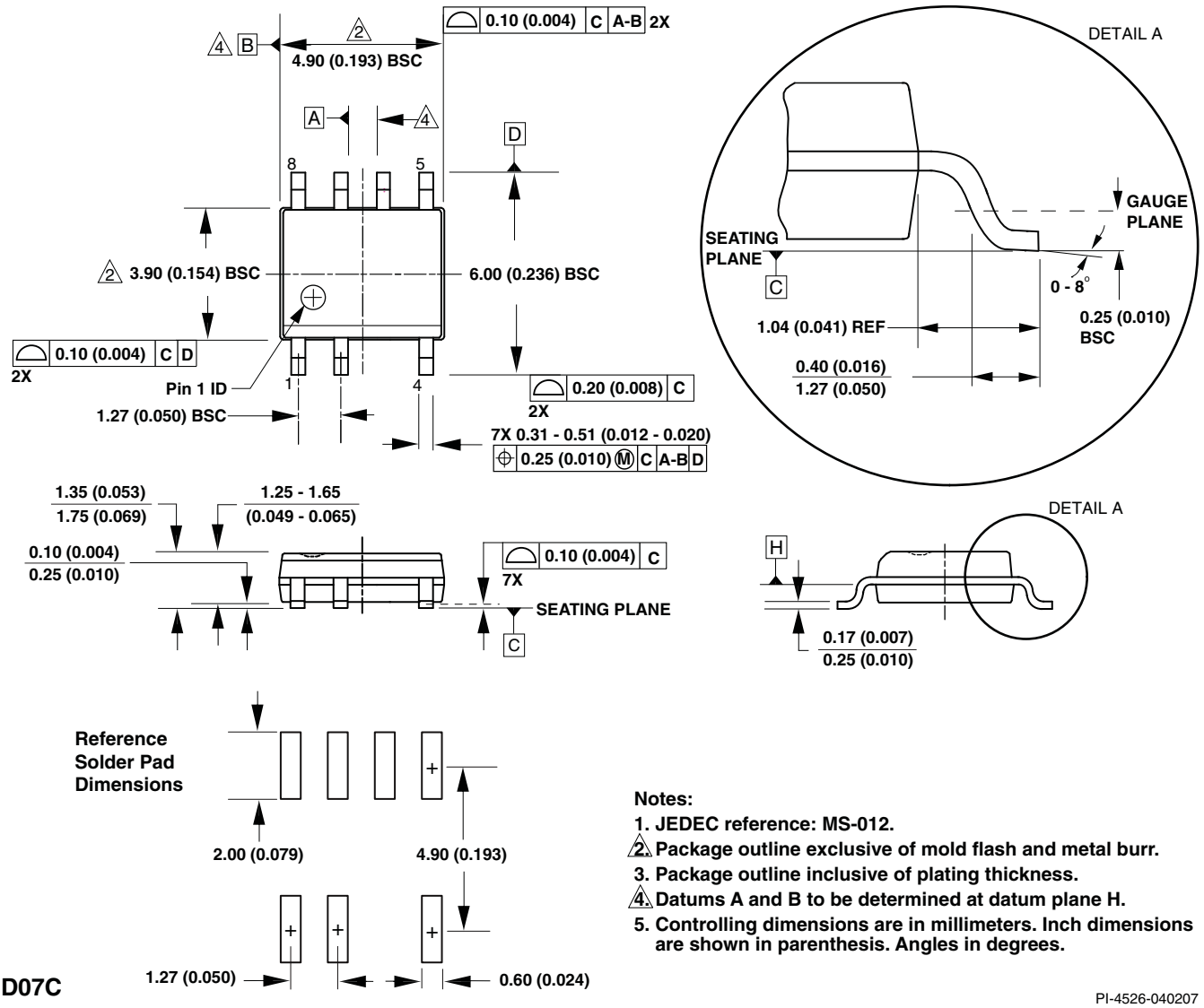
Notes:

1. Controlling dimensions are inches. Millimeter sizes are shown in parentheses.
2. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
3. Pin locations start with Pin 1, and continue counter-clockwise to Pin 8 when viewed from the top. Pin 6 is omitted.
4. Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).
5. Lead width measured at package body.
6. D and E are referenced datums on the package body.

G08B

PI-2546-121504

SO-8C



Notes:

1. JEDEC reference: MS-012.
2. Package outline exclusive of mold flash and metal burr.
3. Package outline inclusive of plating thickness.
4. Datums A and B to be determined at datum plane H.
5. Controlling dimensions are in millimeters. Inch dimensions are shown in parenthesis. Angles in degrees.

D07C

PI-4526-040207

Revision	Notes	Date
B	1) Released Final Data Sheet.	11/05
C	1) Corrected Application Example section.	12/05
D	1) Added SO-8C package.	2/07
E	1) Updated Part Ordering Information section with Halogen Free	11/08

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