THE DATASHEET OF

LP2952IMX/NOPB

www.win-source.net 0086-755-83957316

LP295x Adjustable Micropower Low-Dropout Voltage Regulators

1 Features

- 2.3-V to 30-V Input Voltage Range
- Output Voltage Adjusts from 1.23 V to 29 V
- 250-mA Output Current
- Extremely Low Quiescent Current
- Low Dropout Voltage
- Extremely Tight Line and Load Regulation
- Very Low Temperature Coefficient
- Current and Thermal Limiting
- Reverse Battery-Input Protection
- 50-mA (Typical) Automatic Output Discharge
- LP2953 Versions Only
  - Auxiliary Comparator Included With CMOS- and TTL-Compatible Output Levels. Can Be Used for Fault Detection, Low-Input Line Detection, and so on.

2 Applications

- High-Efficiency Linear Regulator
- Regulator With Undervoltage Shutdown
- Low-Dropout Battery-Powered Regulator
- Snap-ON/Snap-OFF Regulator

3 Description

The LP2952 and LP2953 are micropower voltage regulators with very low quiescent current (130 µA typical at 1-mA load) and very low dropout voltage (typically 60 mV at light load and 470 mV at 250-mA load current). They are ideally suited for battery-powered systems. Furthermore, the quiescent current increases only slightly at dropout, which prolongs battery life.

The LP2952 and LP2953 retain all the desirable characteristics of the LP2951, but offer increased output current, additional features, and an improved shutdown function.

The automatic output discharge pulls the output down quickly when the shutdown is activated.

The error flag goes low if the output voltage drops out of regulation.

Reverse battery-input protection is provided.

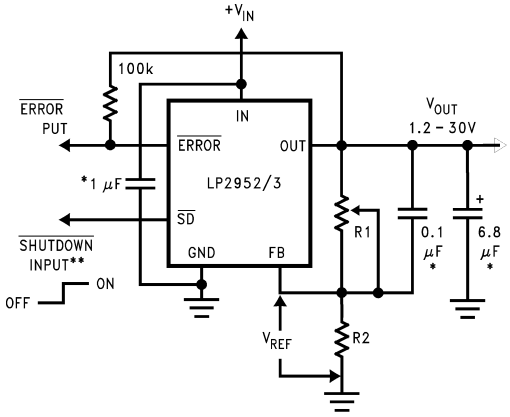
The internal voltage reference is made available for external use, providing a low temperature coefficient (20 ppm/°C) reference with very good line (0.03%) and load (0.04%) regulation.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP2952x	SOIC (16)	9.90 mm × 3.91 mm
LP2953x	SOIC (16)	9.90 mm × 3.91 mm
	PDIP (16)	21.755 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 5
6.5 Electrical Characteristics: 3.3-V Versions ... 5
6.6 Electrical Characteristics: 5-V Versions ... 5
6.7 Electrical Characteristics: All Voltage Options ... 6
6.8 Typical Characteristics ... 9
7 Detailed Description ... 14
7.1 Overview ... 14
7.2 Functional Block Diagrams ... 14
7.3 Feature Description ... 15
7.4 Device Functional Mode ... 16
8 Application and Implementation ... 17
8.1 Application Information ... 17
8.2 Typical Applications ... 21
9 Power Supply Recommendations ... 30
10 Layout ... 31
10.1 Layout Guidelines ... 31
10.2 Layout Example ... 31
10.3 Power Dissipation: Heatsink Requirements (Industrial Temperature Range Devices) ... 32
11 Device and Documentation Support ... 34
11.1 Related Links ... 34
11.2 Trademarks ... 34
11.3 Electrostatic Discharge Caution ... 34
11.4 Glossary ... 34
12 Mechanical, Packaging, and Orderable Information ... 34

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (December 2014) to Revision F — **Page**

- Deleted "Assured" ... 1
- Changed "Output Pulldown Crowbar" to "Automatic Output Discharge" ... 1
- Changed "internal crowbar" to "automatic output discharge" ... 1
- Added word "input" after "battery" in Features and Description ... 1
- Changed pin names for IN and OUT to match TI nomenclature; fix typos ... 1
- Changed max junc. temp from 125°C to 150°C ... 4
- Changed wording of footnote 12 ... 8
- Added second bullet for "LP2953 versions only" ... 14
- Added Automatic Output Dischange subsection ... 16
- Deleted sentence "To achieve the smallest form factor, the TO-92 package is selected." ... 22
- Changed "With an efficiency of 83.3% and a 250-mA maximum load, the internal power dissipation is 250 mW, which corresponds to a 19.2°C junction temperature rise for the SOIC package." to "With a $V_{IN} – V_{OUT}$ differential of 1 V and a maximum load current of 250 mA the internal junction temperature (T_J) of the SOIC package will rise 19.2° above the ambient temperature." ... 22
- Deleted "Thermal Resistance for Various Copper Heatsinking Patterns" table ... 33

Changes from Revision D (September 2013) to Revision E — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section; updated *Thermal Information* values; deleted obsolete LP2953AM references ... 1

Changes from Revision C (March 2005) to Revision D — **Page**

- Changed layout of National Data Sheet to TI format ... 30

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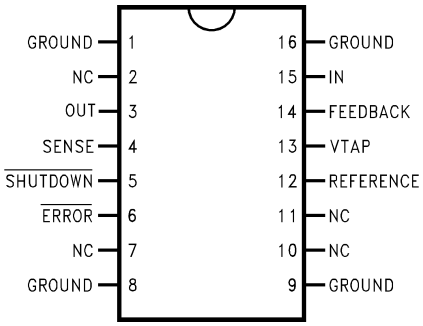
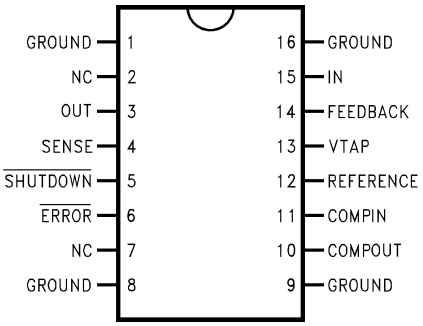
5 Pin Configuration and Functions

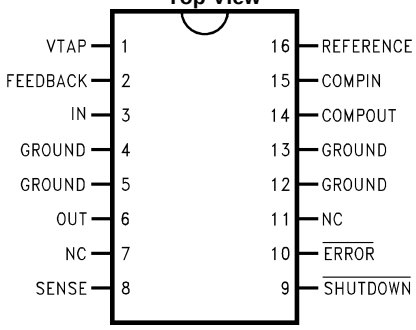
16 Pins
LP2952 SOIC (D) Package
Top View



16 Pins
LP2953 SOIC (D) Package
Top View



16 Pins
LP2953 PDIP (NBG) Package
Top View



Pin Functions LP2952-N

PIN		I/O	DESCRIPTION
NAME	SOIC(D)		
$\overline{\text{ERROR}}$	6	O	Error signal output
FEEDBACK	14	I	Error amplifier noninverting input
GROUND	1, 8, 9, 16	-	Ground
IN	15	I	Regulator power input
NC	2, 7, 10, 11	-	NC
OUT	3	O	Regulated output voltage
REFERENCE	12	O	Internal reference voltage output
SENSE	4	I	Feedback voltage sense input
$\overline{\text{SHUTDOWN}}$	5	I	Shutdown input
VTAP	13	I	Internal resistor divider input

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Pin Functions LP2953

PIN			I/O	DESCRIPTION
NAME	SOIC(D)	PDIP(NBG)		
COMPIN	10	15	I	Auxiliary comparator input
COMPOUT	11	14	O	Auxiliary comparator output
$\overline{\text{ERROR}}$	6	10	O	Error signal output
FEEDBACK	14	2	I	Error amplifier noninverting input
GROUND	1, 8, 9, 16	4, 5, 12, 13	-	Ground
IN	15	3	I	Regulator power input
NC	2, 7	7, 11	-	NC
OUT	3	6	O	Regulated output voltage
REFERENCE	12	16	O	Internal reference voltage output
SENSE	4	8	I	Feedback voltage sense input
$\overline{\text{SHUTDOWN}}$	5	9	I	Shutdown input
VTAP	13	1	I	Internal resistor divider input

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power dissipation(2)	Internally Limited		
Input supply voltage	−20	30	V
FEEDBACK input voltage(3)	−0.3	5	V
Comparator input voltage(4)	−0.3	30	V
$\overline{\text{SHUTDOWN}}$ input voltage(4)	−0.3	30	V
Comparator output voltage(4)	−0.3	30	V
Maximum junction temperature		150	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using the equation for $P_{(MAX)}$: $P_{(MAX)} = (T_{J(MAX)} – T_A) / R_{\theta JA}$.
Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. See *Power Supply Recommendations* for additional information on heatsinking and thermal resistance.
(3) When used in dual-supply systems where the regulator load is returned to a negative supply, the output voltage must be diode-clamped to ground.
(4) May exceed the input supply voltage.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating junction temperature	−40	125	°C
Input supply voltage	2.3	30	V

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6.4 Thermal Information

THERMAL METRIC[1]		LP2952, LP2953	LP2953	UNIT
		SOIC (D)	PDIP (NBG)	
		16 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	76.9	42.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.4	28.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	34.6	22.2	
ψ_{JT}	Junction-to-top characterization parameter	7.3	12.0	
ψ_{JB}	Junction-to-board characterization parameter	34.3	22.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: 3.3-V Versions

Limits are assured by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods. Unless otherwise specified: MIN (minimum) and MAX (maximum) specifications in apply over the full Operating Temperature Range and TYP (typical) values apply at T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1 V, I_{OUT} = 1 mA, C_{OUT} = 2.2 µF for 5-V parts and 4.7 µF for 3.3-V parts. FEEDBACK pin is tied to VTAP pin, OUT pin is tied to SENSE pin.

PARAMETER		TEST CONDITIONS	LP2952AI-3.3, LP2953AI-3.3			LP2952I-3.3, LP2953I-3.3			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OUT}	Output voltage	T_J = 25°C	3.284	3.3	3.317	3.267	3.3	3.333	V
			3.260	3.3	3.340	3.234	3.3	3.366	
		1 mA ≤ I_{OUT} ≤ 250 mA	3.254	3.3	3.346	3.221	3.3	3.379	

6.6 Electrical Characteristics: 5-V Versions

Limits are assured by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods. Unless otherwise specified, MIN (minimum) and MAX (maximum) specifications in apply over the full Operating Temperature Range and TYP (typical) values apply at T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1 V, I_{OUT} = 1 mA, C_{OUT} = 2.2 µF for 5-V parts and 4.7 µF for 3.3-V parts. FEEDBACK pin is tied to VTAP pin, OUT pin is tied to SENSE pin.

PARAMETER		TEST CONDITIONS	LP2952AI, LP2953AI			LP2952I, LP2953I			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OUT}	Output voltage	T_J = 25°C	4.975	5	5.025	4.95	5	5.05	V
			4.94	5	5.06	4.9	5	5.1	
		1 mA ≤ I_{OUT} ≤ 250 mA	4.93	5	5.07	4.88	5	5.12	

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6.7 Electrical Characteristics: All Voltage Options

Limits are assured by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods. Unless otherwise specified, MIN (minimum) and MAX (maximum) specifications in apply over the full Operating Temperature Range and TYP (typical) values apply at T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1 V, I_{OUT} = 1 mA, C_{OUT} = 2.2 µF for 5-V parts and 4.7 µF for 3.3-V parts. FEEDBACK pin is tied to VTAP pin, OUT pin is tied to SENSE pin.

PARAMETER		TEST CONDITIONS	LP2952AI, LP2953AI, LP2952AI-3.3, LP2953AI-3.3(1)			LP2952I, LP2953I, LP2952I-3.3, LP2953I-3.3			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
REGULATOR									
$\frac{\Delta V_{OUT}}{\Delta T}$	Output voltage temperature coefficient	See(2)		20	100		20	150	ppm/°C
$\frac{\Delta V_{OUT}}{\Delta V}$	Output voltage line regulation	T_J = 25°C V_{IN} = $V_{OUT(NOM)}$ + 1 V to 30 V		0.03%	0.1%		0.03%	0.2%	
		V_{IN} = $V_{OUT(NOM)}$ + 1 V to 30 V		0.03%	0.2%		0.03%	0.4%	
$\frac{\Delta V_{OUT}}{\Delta V}$	Output voltage load regulation(3)	T_J = 25°C I_{OUT} = 1 mA to 250 mA		0.04%	0.16%		0.04%	0.20%	
		I_{OUT} = 0.1 mA to 1 mA		0.04%	0.20%		0.04%	0.30%	
$V_{IN} - V_{OUT}$	Dropout voltage(4)	T_J = 25°C, I_{OUT} = 1 mA		60	100		60	100	mV
		I_{OUT} = 1 mA		60	150		60	150	
		I_{OUT} = 50 mA		240	300		240	300	
		I_{OUT} = 50 mA		240	420		240	420	
		T_J = 25°C, I_{OUT} = 100 mA		310	400		310	400	
		I_{OUT} = 100 mA		310	520		310	520	
		T_J = 25°C, I_{OUT} = 250 mA		470	600		470	600	
		I_{OUT} = 250 mA		470	800		470	800	
I_{GND}	Ground pin current(5)	T_J = 25°C, I_{OUT} = 1 mA		130	170		130	170	µA
		I_{OUT} = 1 mA		130	200		130	200	
		T_J = 25°C, I_{OUT} = 50 mA		1.1	2		1.1	2	mA
		I_{OUT} = 50 mA		1.1	2.5		1.1	2.5	
		T_J = 25°C, I_{OUT} = 100 mA		4.5	6		4.5	6	
		I_{OUT} = 100 mA		4.5	8		4.5	8	
		T_J = 25°C, I_{OUT} = 250 mA		21	28		21	28	
		I_{OUT} = 250 mA		21	33		21	33	
I_{GND}	Ground pin current at dropout	V_{IN} = $V_{OUT(NOM)}$ − 0.5 V		165	210		165	210	µA
		I_{OUT} = 100 µA –40°C ≤ T_J ≤ 125°C		165	240		165	240	
I_{GND}	Ground pin current at shutdown(5)	T_J = 25°C, $V_{SHUTDOWN}$ ≤ 1.1 V		105	140		105	140	µA
I_{LIMIT}	Current limit	T_J = 25°C, V_{OUT} = 0		380	500		380	500	mA
		V_{OUT} = 0		380	530		380	530	
$\frac{\Delta V_{OUT}}{\Delta P_D}$	Thermal regulation	T_J = 25°C; see(6)		0.05	0.2		0.05	0.2	%/W

(1) Drive $\overline{SHUTDOWN}$ pin with TTL or CMOS low level to shut off regulator, high level to turn on regulator.
(2) Output or reference voltage temperature coefficient is defined as the worst-case voltage change divided by the total temperature range.
(3) Load regulation is measured at constant junction temperature using low duty-cycle pulse testing. Two separate tests are performed, one for the range of I_{OUT} = 100 µA to 1 mA and one for the range of I_{OUT} =1 mA to 250 mA. Changes in output voltage due to heating effects are covered by the thermal regulation specification.
(4) Dropout voltage is defined as the input-to-output differential at which the output voltage drops 100 mV below the value measured with a 1-V differential. At very low values of programmed output voltage, the input voltage minimum of 2 V (2.3 V over temperature) must be observed.
(5) Ground pin current is the regulator quiescent current. The total current drawn from the source is the sum of the ground pin current, output load current, and current through the external resistive divider (if used).
(6) Thermal regulation is the change in output voltage at a time t after a change in power dissipation, excluding load or line regulation effects. Specifications are for a 200-mA load pulse at V_{IN} = $V_{OUT(NOM)}$ + 15 V (3-W pulse) for t = 10 ms.

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Electrical Characteristics: All Voltage Options (continued)

Limits are assured by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods. Unless otherwise specified, MIN (minimum) and MAX (maximum) specifications in apply over the full Operating Temperature Range and TYP (typical) values apply at T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1 V, I_{OUT} = 1 mA, C_{OUT} = 2.2 µF for 5-V parts and 4.7 µF for 3.3-V parts. FEEDBACK pin is tied to VTAP pin, OUT pin is tied to SENSE pin.

PARAMETER		TEST CONDITIONS	LP2952AI, LP2953AI, LP2952AI-3.3, LP2953AI-3.3(1)			LP2952I, LP2953I, LP2952I-3.3, LP2953I-3.3			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
e_n	Output noise voltage (10 Hz to 100 kHz) I_{OUT} = 100 mA	C_{OUT} = 4.7 µF		400			400		µV RMS
		C_{OUT} = 33 µF		260			260		
		C_{OUT} = 33 µF(7)		80			80		
V_{REF}	Reference voltage	T_J = 25°C, see(8)	1.215	1.23	1.245	1.205	1.23	1.255	V
		see(8),	1.205		1.255	1.19		1.27	
$\frac{\Delta V_{REF}}{V_{REF}}$	Reference voltage line regulation	V_{IN} = 2.5 V to V_{OUT} + 1 V		0.03%	0.1%		0.03%	0.2%	
		V_{IN} = $V_{OUT(NOM)}$+ 1 V to 30 V(9)		0.03%	0.2%		0.03%	0.4%	
$\frac{\Delta V_{REF}}{V_{REF}}$	Reference voltage load regulation	T_J = 25°C, I_{REF} = 0 to 200 µA		0.25%	0.4%		0.25%	0.8%	
		I_{REF} = 0 to 200 µA		0.25%	0.6%		0.25%	1.0%	
$\frac{\Delta V_{REF}}{\Delta T}$	Reference voltage temperature coefficient	See(2), –40°C ≤ T_J ≤ 125°C		20			20		ppm/°C
$I_{B(FB)}$	Feedback pin bias current	T_J = 25°C		20	40		20	40	nA
				20	60		20	60	
$I_{O(SINK)}$	Output off pulldown current	T_J = 25°C; see (10)	30			30			mA
		See (10)	20			20			
DROPOUT DETECTION COMPARATOR									
I_{OH}	Output high leakage	T_J = 25°C, V_{OH} = 30 V		0.01	1		0.01	1	µA
		V_{OH} = 30 V		0.01	2		0.01	2	
V_{OL}	Output low voltage	T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ − 0.5 V $I_{OUT(COMP)}$ = 400 µA		150	250		150	250	mV
		V_{IN} = $V_{OUT(NOM)}$ − 0.5 V $I_{OUT(COMP)}$ = 400 µA		150	400		150	400	
$V_{THR(MAX)}$	Upper threshold voltage	T_J = 25°C, see(11)	−80	−60	−35	−80	−60	−35	mV
		See(11)	−95	−60	−25	−95	−60	−25	
$V_{THR(MIN)}$	Lower threshold voltage	T_J = 25°C, see(11)	−110	−85	−55	−110	−85	−55	mV
		See(11)	−160	−85	−40	−160	−85	−40	
HYST	Hysteresis	See(11)		15			15		mV

(7) Connect a 0.1-µF capacitor from the OUT pin to the FEEDBACK pin.
(8) V_{REF} ≤ V_{OUT} ≤ (V_{IN} − 1 V), 2.3 V ≤ V_{IN} ≤ 30 V, 100 µA ≤ I_{OUT} ≤ 250 mA.
(9) Two separate tests are performed, one covering 2.5 V ≤ V_{IN} ≤ $V_{OUT(NOM)}$) + 1 V and the other test for $V_{OUT(NOM)}$ + 1 V ≤ V_{IN} ≤ 30 V.
(10) $V_{SHUTDOWN}$ ≤ 1.1 V, V_{OUT} = $V_{OUT(NOM)}$
(11) Comparator thresholds are expressed in terms of a voltage differential at the FEEDBACK pin below the nominal reference voltage measured at V_{IN} = $V_{OUT(NOM)}$ + 1 V. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain, which is V_{OUT} / V_{REF} = (R1 + R2) / R2 (see Figure 31).

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Electrical Characteristics: All Voltage Options (continued)

Limits are assured by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods. Unless otherwise specified, MIN (minimum) and MAX (maximum) specifications in apply over the full Operating Temperature Range and TYP (typical) values apply at T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1 V, I_{OUT} = 1 mA, C_{OUT} = 2.2 µF for 5-V parts and 4.7 µF for 3.3-V parts. FEEDBACK pin is tied to VTAP pin, OUT pin is tied to SENSE pin.

PARAMETER		TEST CONDITIONS	LP2952AI, LP2953AI, LP2952AI-3.3, LP2953AI-3.3(1)			LP2952I, LP2953I, LP2952I-3.3, LP2953I-3.3			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$\overline{\text{SHUTDOWN}}$ INPUT(12)									
V_{OS}	Input offset voltage	T_J = 25°C (Referred to V_{REF})	−7.5	±3	7.5	−7.5	±3	7.5	mV
			−10		10	−10		10	
HYST	Hysteresis			6			6		mV
I_B	Input bias current	T_J = 25°C $V_{IN}(\overline{SD})$ = 0 V to 5 V	−30	10	30	−30	10	−30	nA
		$V_{IN}(\overline{SD})$ = 0 V to 5 V	−50		50	−50		50	
AUXILIARY COMPARATOR (LP2953 Only)									
V_{OS}	Input offset voltage	T_J = 25°C (Referred to V_{REF})	−7.5	±3	7.5	−7.5	±3	7.5	mV
		(Referred to V_{REF})	−10	±3	10	−10	±3	10	
HYST	Hysteresis			6			6		mV
I_B	Input bias current	T_J = 25°C, $V_{IN(COMP)}$ = 0 V to 5 V	−30	10	30	−30	10	30	nA
		$V_{IN(COMP)}$ = 0 V to 5 V	−50	10	50	−50	10	50	
I_{OH}	Output high leakage	T_J = 25°C, V_{OH} = 30 V		0.01	1		0.01	1	µA
		$V_{IN(COMP)}$ = 1.3 V		0.01	2		0.01	2	
V_{OL}	Output low voltage	T_J = 25°C, $V_{IN(COMP)}$ = 1.1 V		150	250		150	250	mV
		$I_{OUT(COMP)}$ = 400 µA		150	400		150	400	

(12) Drive $\overline{\text{SHUTDOWN}}$ pin with TTL or CMOS-low level to shut regulator OFF, high level to turn regulator ON.

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6.8 Typical Characteristics

Unless otherwise specified: V_{IN} = 6 V, I_{OUT} = 1 mA, C_{OUT} = 2.2 µF, V_{SD} = 3 V, T_A = 25°C, V_{OUT} = 5 V.

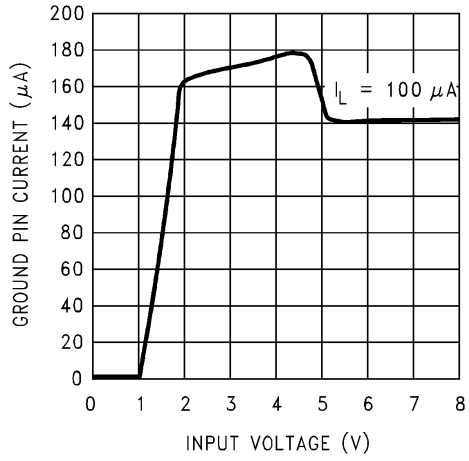

Figure 1. Quiescent Current

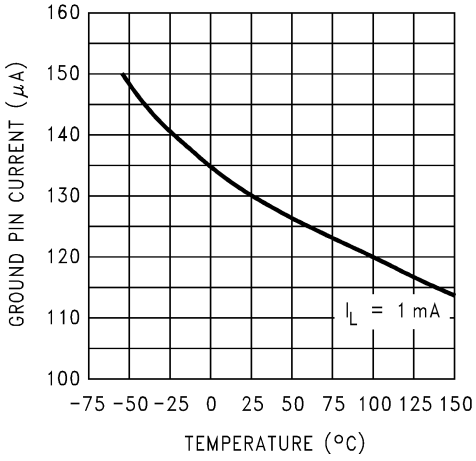

Figure 2. Quiescent Current

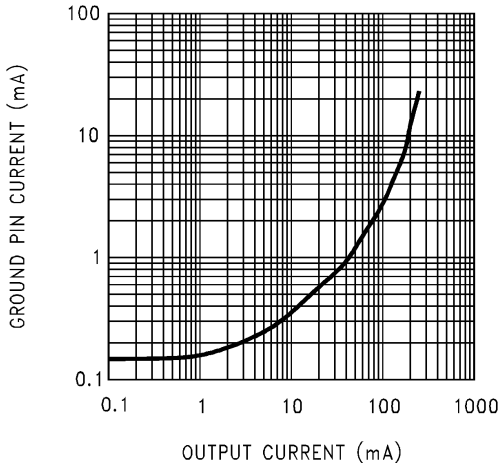

Figure 3. Ground Pin Current vs Load

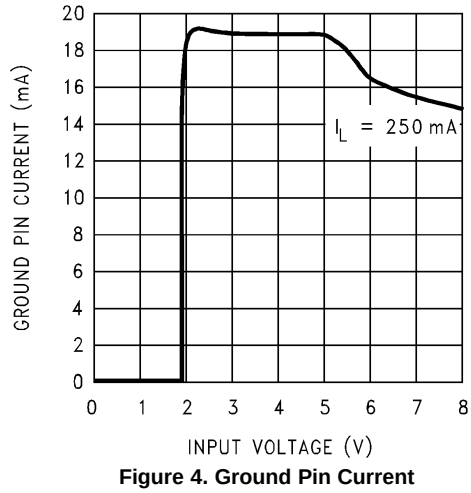

Figure 4. Ground Pin Current

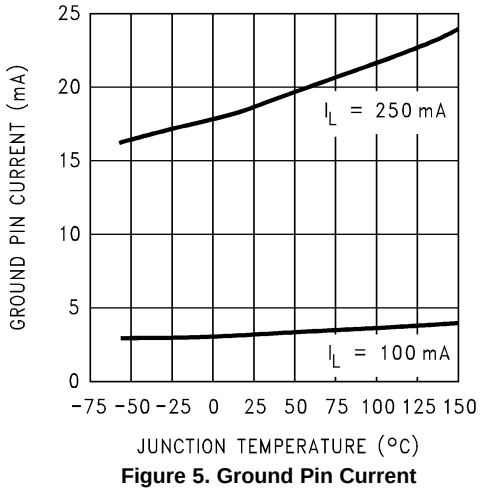

Figure 5. Ground Pin Current

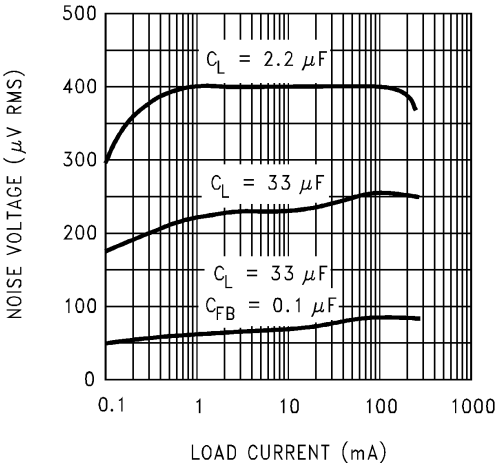

Figure 6. Output Noise Voltage

Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 6 V, I_{OUT} = 1 mA, C_{OUT} = 2.2 µF, V_{SD} = 3 V, T_A = 25°C, V_{OUT} = 5 V.

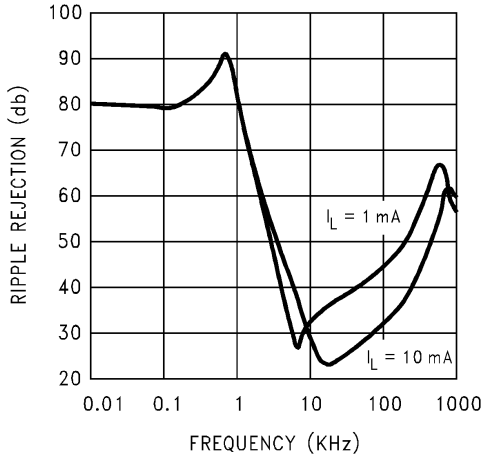

Figure 7. Ripple Rejection

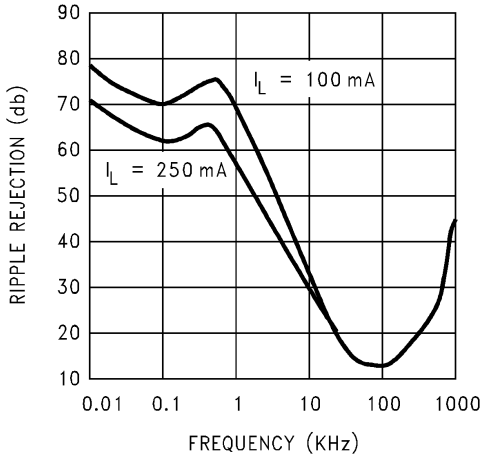

Figure 8. Ripple Rejection

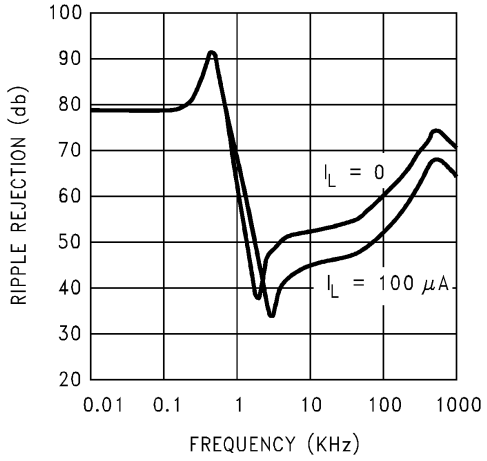

Figure 9. Ripple Rejection

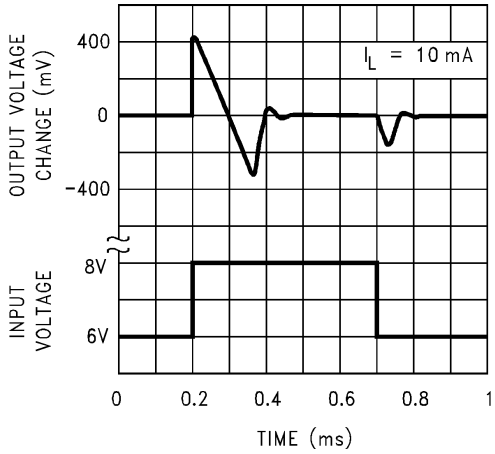

Figure 10. Line Transient Response

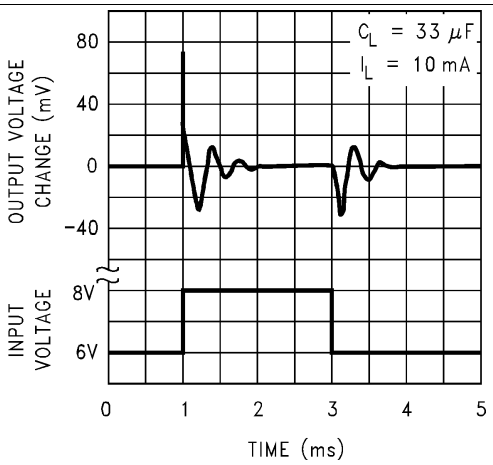

Figure 11. Line Transient Response

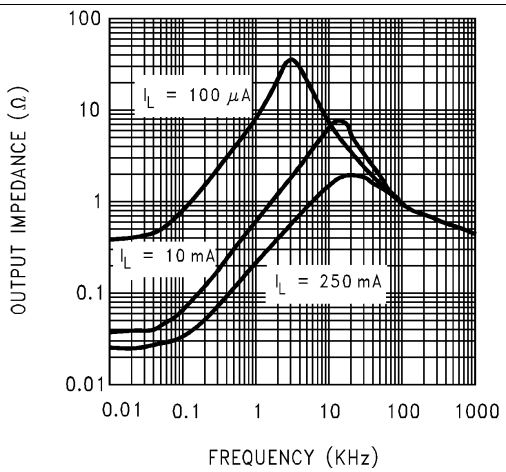

Figure 12. Output Impedance

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Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 6 V, I_{OUT} = 1 mA, C_{OUT} = 2.2 µF, V_{SD} = 3 V, T_A = 25°C, V_{OUT} = 5 V.

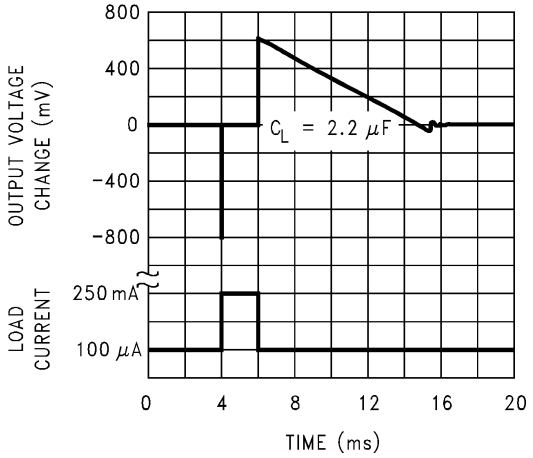

Figure 13. Load Transient Response

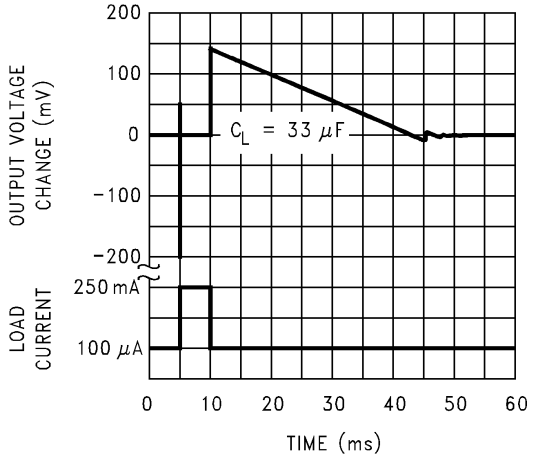

Figure 14. Load Transient Response

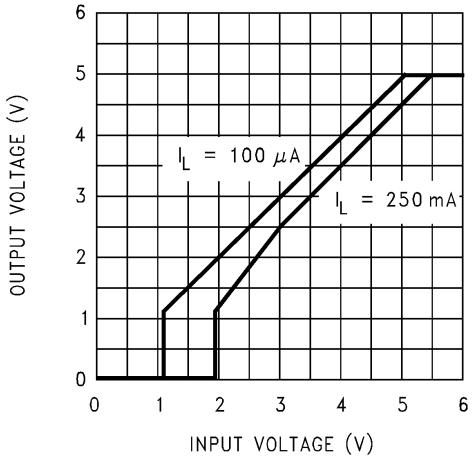

Figure 15. Dropout Characteristics

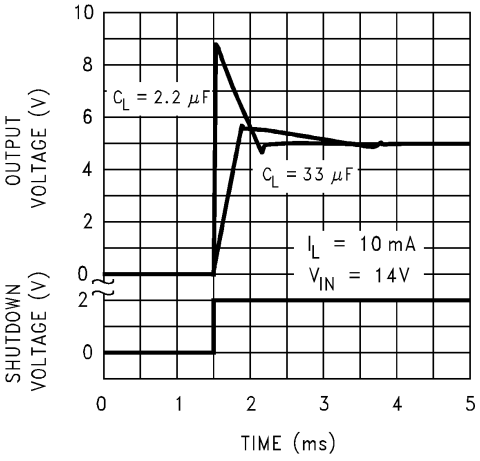

Figure 16. Enable Transient

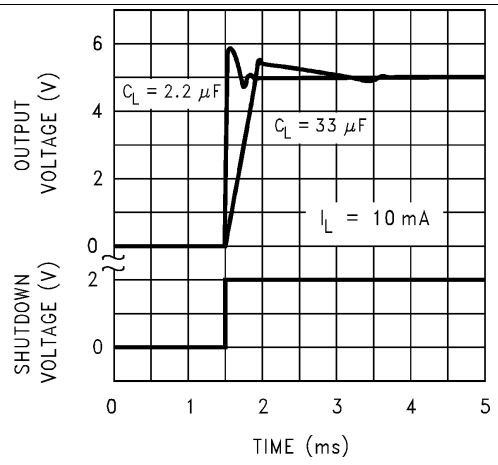

Figure 17. Enable Transient

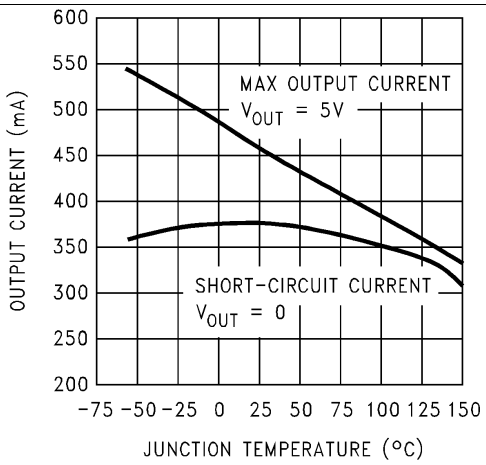

Figure 18. Short-Circuit Output Current and Maximum Output Current

Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 6 V, I_{OUT} = 1 mA, C_{OUT} = 2.2 µF, V_{SD} = 3 V, T_A = 25°C, V_{OUT} = 5 V.

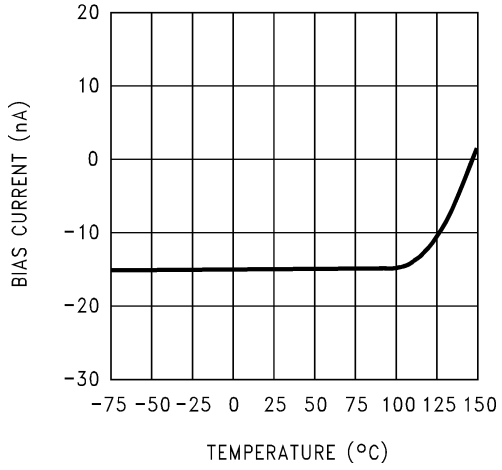

Figure 19. Feedback Bias Current

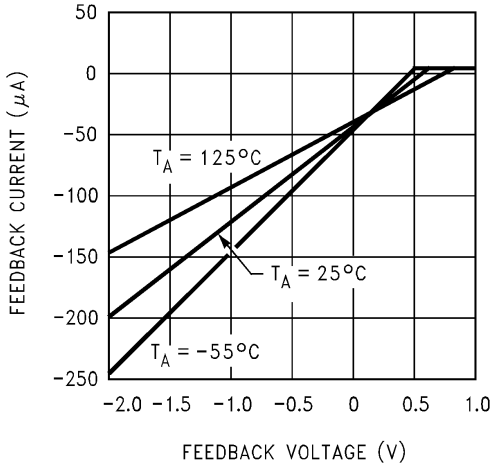

Figure 20. FEEDBACK Pin Current

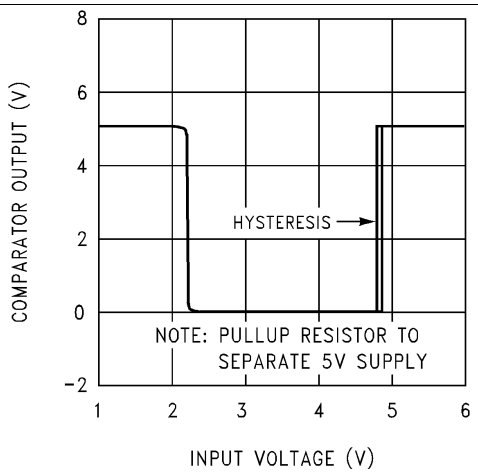

Figure 21. Error Output

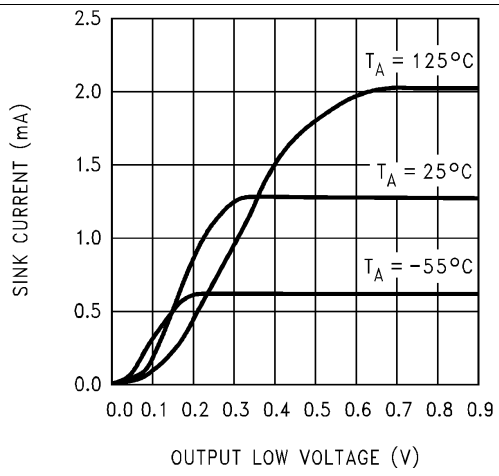

Figure 22. Comparator Sink Current

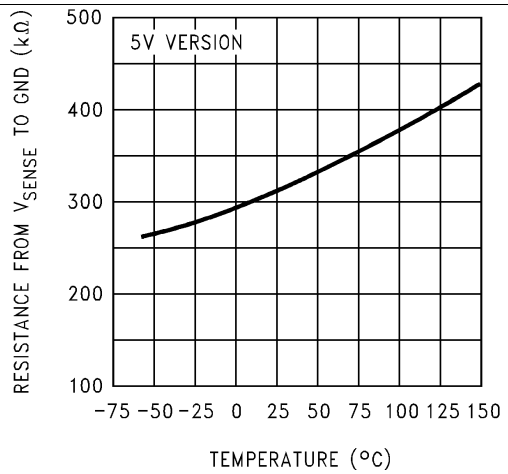

Figure 23. Divider Resistance

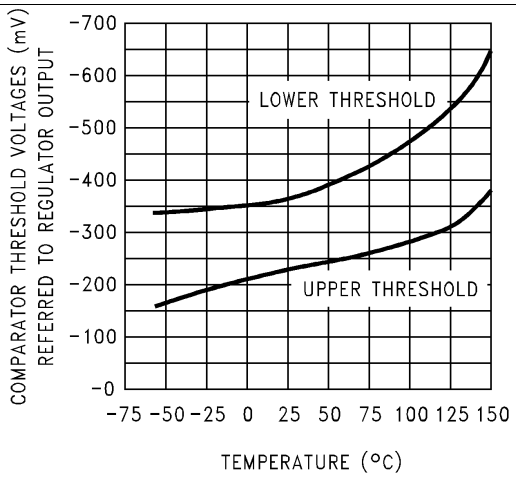

Figure 24. Dropout Detection Comparator Threshold Voltages

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Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 6 V, I_{OUT} = 1 mA, C_{OUT} = 2.2 µF, V_{SD} = 3 V, T_A = 25°C, V_{OUT} = 5 V.

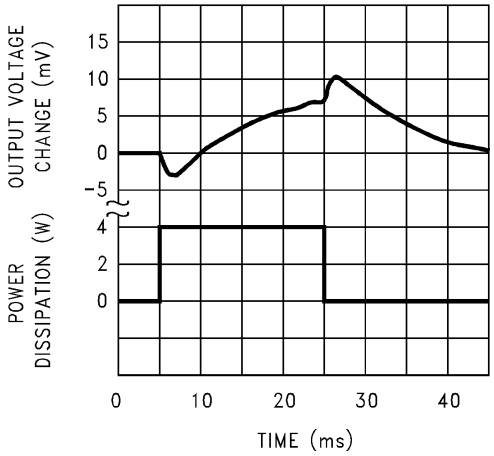

Figure 25. Thermal Regulation

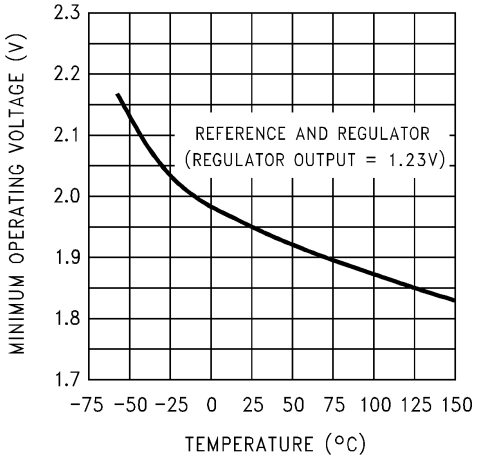

Figure 26. Minimum Operating Voltage

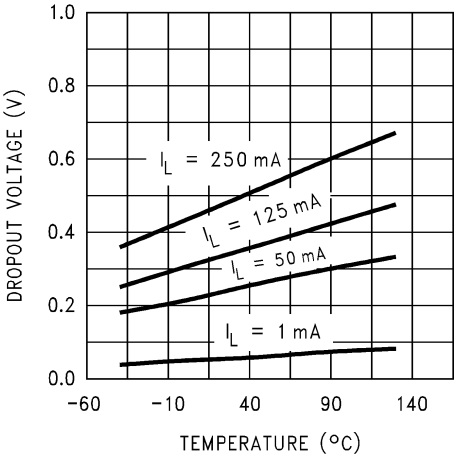

Figure 27. Dropout Voltage

7 Detailed Description

7.1 Overview

The LP2952 and LP2953 are very high accuracy micropower voltage regulators with low quiescent current (130 µA, typical) and low dropout voltage (typically 60 mV at light loads and 490 mV at 250 mA). They are ideally suited for use in battery-powered systems.

The LP2952 and LP2953 block diagram contains several features, including:

- Very high accuracy 1.23-V reference.
- Internal protection circuitry, such as thermal foldback current limit, thermal shutdown protection, and reverse battery-input protection.
- Fixed 5-V and 3.3-V versions.
- Error flag output which may be used for a power-on reset.
- Shutdown input, allowing turn off the regulator when the $\overline{\text{SHUTDOWN}}$ pin is pulled low.

LP2953 versions only:

- An auxiliary comparator is designed for customer special purpose when shutdown is activated, this is a CMOS- or TTL-compatible output level.
- Automatic output discharge when the $\overline{\text{SHUTDOWN}}$ pin is pulled low.

7.2 Functional Block Diagrams

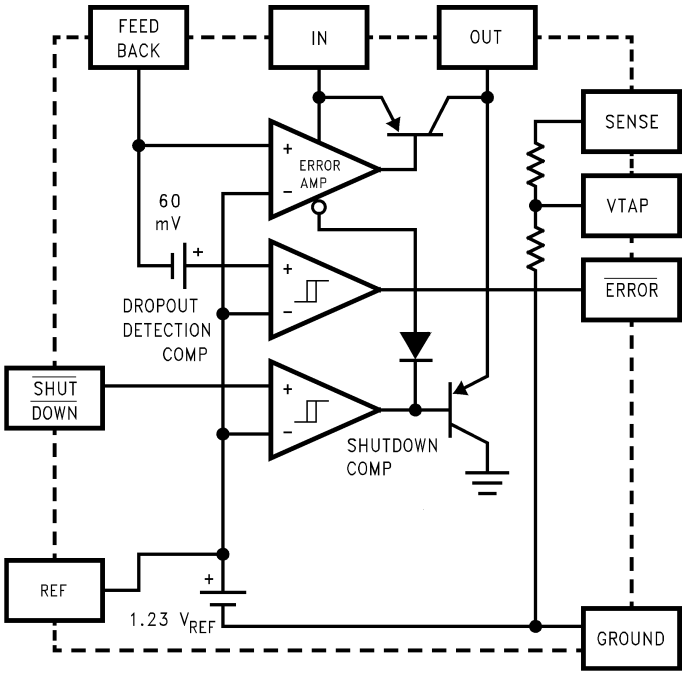

Figure 28. LP2952 Block Diagram

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Functional Block Diagrams (continued)

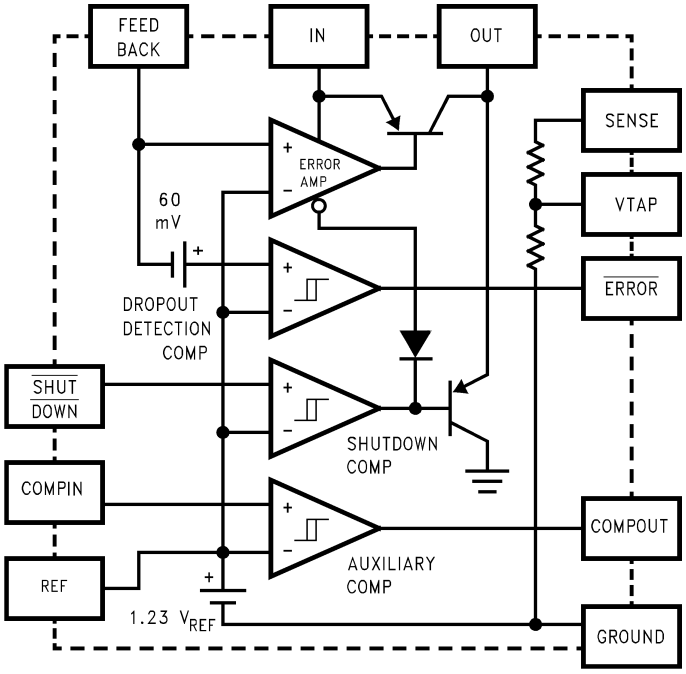

Figure 29. LP2953 Block Diagram

7.3 Feature Description

7.3.1 Fixed Voltage Options and Programmable Voltage Version

The LP2952 and LP2953 provide 2 fixed output options: 3.3 V and 5 V. To meet different requirements for the application, they can also be used as programmable voltage regulators with external resistor networks; see *Application Information* for more details.

7.3.2 High-Accuracy Output Voltage

With special and careful design to minimize all contributions to the output voltage error, the LP2952 and LP2953 distinguished themselves as very high output voltage accuracy micropower LDO. This includes a tight initial tolerance (0.5% typical), extremely good load and line regulation, and a very low output voltage temperature coefficient, making the part an ideal a low-power voltage reference.

7.3.3 Error Detection Comparator Output

The LP2952 and LP2953 will generate a logic low output when the output falls out of regulation by more than approximately 5%. See *Application Information* for more details.

7.3.4 Auxiliary Comparator

An auxiliary comparator is designed for customer special purpose when shutdown is activated. This block is still active and can be used to generate fault detection, low input line detection signal for system controllers. The comparator output level is CMOS- or TTL-compatible. See *Application Information* for more details.

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Feature Description (continued)

7.3.5 Short-Circuit Protection (Current Limit)

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate in a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases. Note also that if a current limit occurs and the resulting output voltage is low, excessive power may be dissipated across the LDO resulting in a thermal shutdown of the output. A thermal foldback feature limits the short-circuit current to protect the regulator from damage under all load conditions. If the OUT pin is forced below 0 V before $\overline{\text{SHUTDOWN}}$ goes high and the load current required exceeds the thermal foldback current limit, the device may not start up correctly.

7.3.6 Thermal Protection

The device contains a thermal shutdown protection circuit to turn off the output current when excessive heat is dissipated in the LDO. The thermal time-constant of the semiconductor die is fairly short, and thus the output cycles on and off at a high rate when thermal shutdown is reached until the power dissipation is reduced. The internal protection circuitry of the device is designed to protect against thermal overload conditions. The circuitry is not intended to replace a proper heatsink. Continuously running the device into thermal shutdown degrades its reliability.

7.3.7 Automatic Output Discharge

Both LP2952 and LP2953 employ an internal 50-mA (typical) pulldown to discharge the output when the $\overline{\text{SHUTDOWN}}$ pin is low and the output is disabled.

7.4 Device Functional Mode

7.4.1 Shutdown Mode

When pulling the $\overline{\text{SHUTDOWN}}$ pin to low level, the LP2952 and LP2953 will enter shutdown mode, and a very low quiescent current is consumed. This function is designed for applications which needs a shutdown mode to effectively enhance battery life cycle. When the $\overline{\text{SHUTDOWN}}$ pin is low the automatic output discharge circuity will be active. See *Application Information* for more details.

7.4.2 Operation with 30 V ≥ V_{IN} > $V_{OUT(TARGET)}$ + 1 V

The device operate if the input voltage is equal to, or exceeds, $V_{OUT(TARGET)}$ + 1 V, and $\overline{\text{SHUTDOWN}}$ is pulled to high level. At input voltages below the minimum V_{IN} requirement, the devices do not operate correctly and output voltage may not reach target value.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

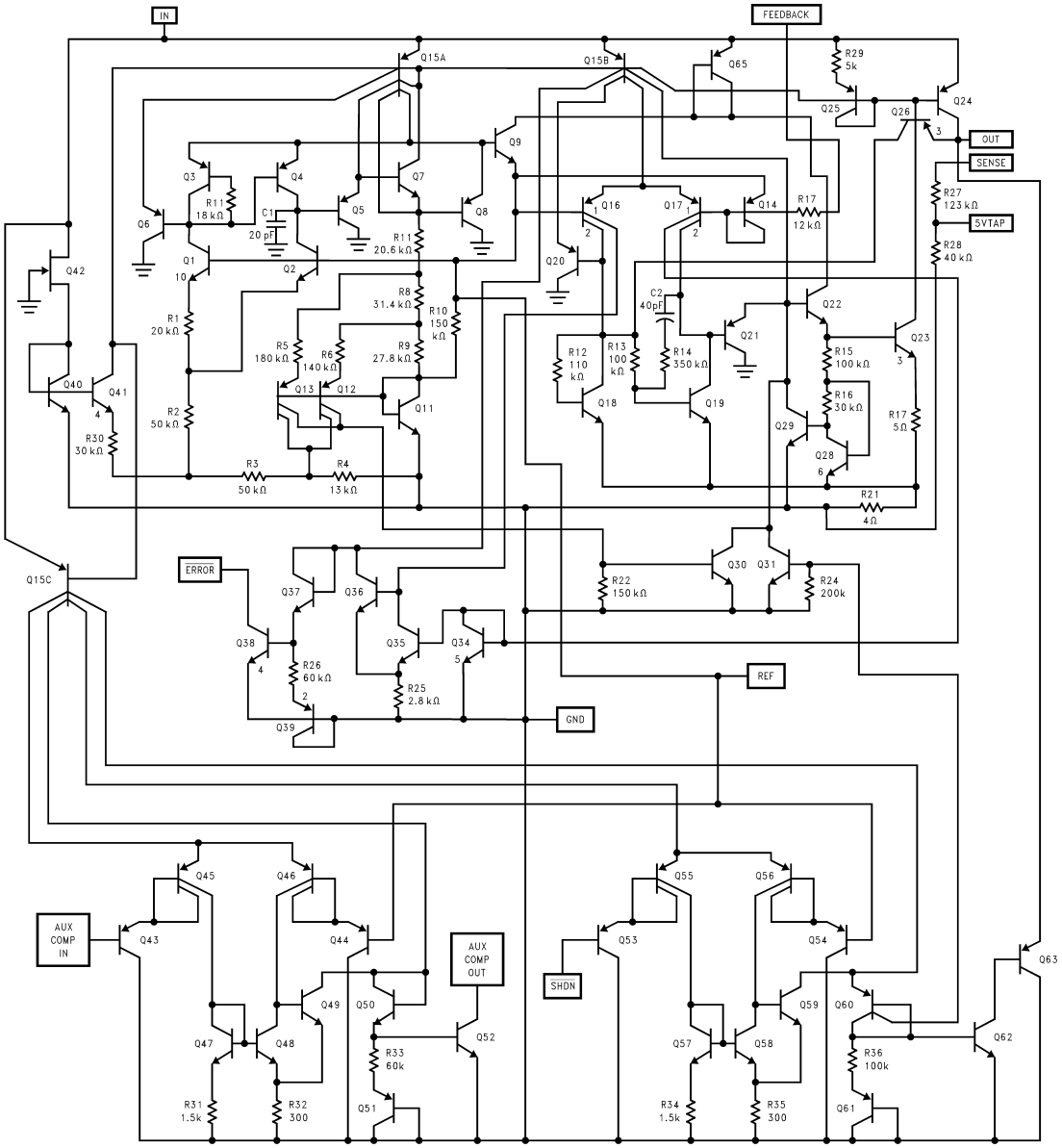

Figure 30. Schematic Diagram

Application Information (continued)

8.1.1 External Capacitors

A 2.2-µF (or greater) capacitor is required between the OUT pin and ground to assure stability when the output is set to 5 V. Without this capacitor, the device will oscillate. Most types of tantalum or aluminum electrolytic capacitors will work here. Film types will work, but are more expensive. Many aluminum electrolytic capacitors contain electrolytes which freeze at −30°C, which requires the use of solid tantalum capacitors below −25°C. The important parameters of the capacitor are an equivalent series resistance (ESR) of about 5 Ω or less and a resonant frequency above 500 kHz (the ESR may increase by a factor of 20 or 30 as the temperature is reduced from 25°C to −30°C). The value of this capacitor may be increased without limit.

At lower values of output current, less output capacitance is required for stability. The capacitor can be reduced to 0.68 µF for currents below 10 mA or 0.22 µF for currents below 1 mA.

Programming the output for voltages below 5 V runs the error amplifier at lower gains requiring more output capacitance for stability. At 3.3-V output, a minimum of 4.7 µF is required. For the worst-case condition of 1.23-V output and 250 mA of load current, a 6.8-µF (or larger) capacitor should be used.

A 1-µF capacitor should be placed from the IN pin to ground if there is more than 10 inches of wire between the IN pin and the ac filter capacitor or if a battery input is used.

Stray capacitance to the FEEDBACK pin can cause instability. This problem is most likely to appear when using high-value external resistors to set the output voltage. Adding a 100-pF capacitor between the OUT and FEEDBACK pins and increasing the output capacitance to 6.8 µF (or greater) will cure the problem.

8.1.2 Minimum Load

When setting the output voltage using an external resistive divider, a minimum current of 1 µA is recommended through the resistors to provide a minimum load.

It should be noted that a minimum load current is specified in several of the *Electrical Characteristics: All Voltage Options* test conditions, so this value must be used to obtain correlation on these tested limits.

8.1.3 Programming the Output Voltage

The regulator may be pin-strapped for 5-V operation using its internal resistive divider by tying the OUTPUT and SENSE pins together and also tying the FEEDBACK and VTAP pins together.

Alternatively, it may be programmed for any voltage between the 1.23-V reference and the 30-V maximum rating using an external pair of resistors (see Figure 31). The complete equation for the output voltage is:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) + (I_{FB} \times R1) \quad (1)$$

where

- V_{REF} is the 1.23-V reference and I_{FB} is the FEEDBACK pin bias current (−20 nA, typical).

The minimum recommended load current of 1 µA sets an upper limit of 1.2 MΩ on the value of R2 in cases where the regulator must work with no load (see *Minimum Load*). I_{FB} will produce a typical 2% error in V_{OUT} which can be eliminated at room temperature by trimming R1. For better accuracy, choosing R2 = 100 kΩ will reduce this error to 0.17% while increasing the resistor program current to 12 µA. Because the typical quiescent current is 120 µA, this added current is negligible.

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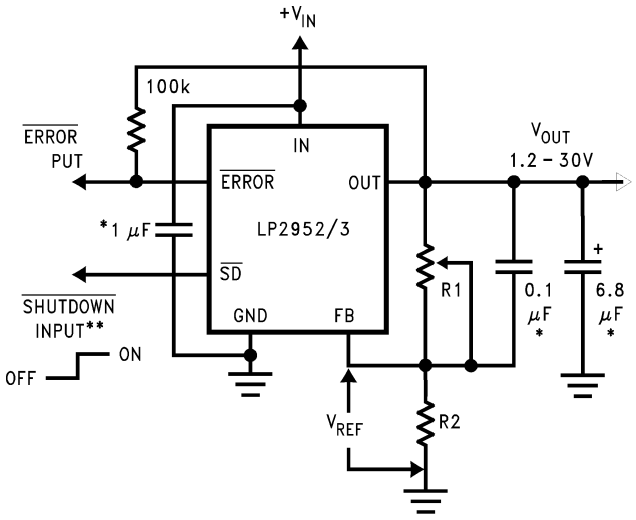
Application Information (continued)



* See *Power Supply Recommendations*
** Drive with TTL-low to shutdown

Figure 31. Adjustable Regulator

8.1.4 Dropout Voltage

The dropout voltage of the regulator is defined as the minimum input-to-output voltage differential required for the output voltage to stay within 100 mV of the output voltage measured with a 1-V differential. The dropout voltage is independent of the programmed output voltage.

8.1.5 Dropout Detection Comparator

This comparator produces a logic low whenever the output falls out of regulation by more than about 5%. This value results from the comparator built-in offset of 60 mV divided by the 1.23-V reference (see *Functional Block Diagrams*). The 5% low trip level remains constant regardless of the programmed output voltage. An out-of-regulation condition can result from low input voltage, current limiting, or thermal limiting.

Figure 32 gives a timing diagram showing the relationship between the output voltage, the $\overline{\text{ERROR}}$ output, and input voltage as the input voltage is ramped up and down to a regulator programmed for 5-V output. The $\overline{\text{ERROR}}$ signal becomes low at about 1.3-V input. It goes high at about 5-V input, where the output equals 4.75 V. Because the dropout voltage is load dependent, the input voltage trip points will vary with load current. The output voltage trip point does not vary.

The comparator has an open-collector output which requires an external pullup resistor. This resistor may be connected to the regulator output or some other supply voltage. Using the regulator output prevents an invalid high on the comparator output that occurs if it is pulled up to an external voltage while the regulator input voltage is reduced below 1.3 V. In selecting a value for the pullup resistor, note that while the output can sink 400 μA, this current adds to battery drain. Suggested values range from 100 kΩ to 1 MΩ. This resistor is not required if the output is unused.

When $V_{IN} \leq 1.3$ V, the $\overline{\text{ERROR}}$ pin becomes a high impedance, allowing the error flag voltage to rise to its pullup voltage. Using V_{OUT} as the pullup voltage (rather than an external 5-V source) will keep the error flag voltage below 1.2 V (typical) in this condition. The user may wish to divide down the error flag voltage using equal-value resistors (10 kΩ is suggested) to ensure a low-level logic signal during any fault condition, while still allowing a valid logic high level during normal operation.

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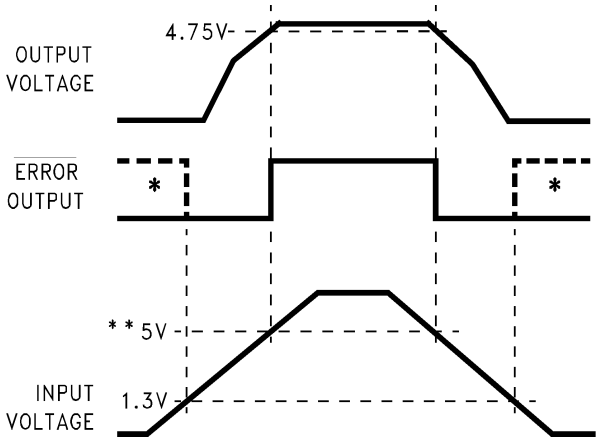
Application Information (continued)



* In shutdown mode, $\overline{\text{ERROR}}$ will go high if it has been pulled up to an external supply. To avoid this invalid response, pull up to regulator output.
** Exact value depends on dropout voltage. (See *Power Supply Recommendations*)

Figure 32. $\overline{\text{ERROR}}$ Output Timing

8.1.6 Output Isolation

The regulator output can be left connected to an active voltage source (such as a battery) with the regulator input power shut off, as long as the regulator ground pin is connected to ground. If the ground pin is left floating, damage to the regulator can occur if the output is pulled up by an external voltage source. If the regulator input power (V_{IN}) is applied, and the $\overline{\text{SHUTDOWN}}$ pin is low, the automatic output discharge circuit will be active, and any voltage source applied to the output will be discharged to ground.

8.1.7 Reducing Output Noise

In reference applications it may be advantageous to reduce the ac noise present on the output. One method is to reduce regulator bandwidth by increasing output capacitance. This is relatively inefficient, because large increases in capacitance are required to get significant improvement.

Noise can be reduced more effectively by a bypass capacitor placed across R1 (see Figure 31). The formula for selecting the capacitor to be used is:

$$C_B = \frac{1}{2\pi\ R1 \times 20\ Hz} \tag{2}$$

This gives a value of about 0.1 µF. When this is used, the output capacitor must be 6.8 µF (or greater) to maintain stability. The 0.1-µF capacitor reduces the high-frequency gain of the circuit to unity, lowering the output noise from 260 µV to 80 µV using a 10-Hz to 100-kHz bandwidth. Also, noise is no longer proportional to the output voltage, so improvements are more pronounced at high output voltages.

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Application Information (continued)

8.1.8 Auxiliary Comparator (LP2953 Only)

The LP2953 contains an auxiliary comparator whose inverting input is connected to the 1.23-V reference. The auxiliary comparator has an open-collector output whose electrical characteristics are similar to the dropout detection comparator. The noninverting input and output are brought out for external connections.

8.1.9 $\overline{\text{SHUTDOWN}}$ Input

A logic-level signal will shut off the regulator output when a low (< 1.2 V) is applied to the $\overline{\text{SHUTDOWN}}$ input.

To prevent possible mis-operation, the $\overline{\text{SHUTDOWN}}$ input must be actively terminated. If the input is driven from open-collector logic, a pullup resistor (20 kΩ to 100 kΩ is recommended) should be connected from the $\overline{\text{SHUTDOWN}}$ input to the regulator input.

If the $\overline{\text{SHUTDOWN}}$ input is driven from a source that actively pulls high and low (like an op-amp), the pullup resistor is not required, but may be used.

If the shutdown function is not to be used, the cost of the pullup resistor can be saved by simply tying the $\overline{\text{SHUTDOWN}}$ input directly to the regulator input.

NOTE

Because the *Absolute Maximum Ratings* state that the $\overline{\text{SHUTDOWN}}$ input can not go more than 0.3 V below ground, the reverse battery-input protection feature which protects the regulator input is sacrificed if the $\overline{\text{SHUTDOWN}}$ input is tied directly to the regulator input.

If reverse-battery input protection is required in an application, the pullup resistor between the $\overline{\text{SHUTDOWN}}$ input and the regulator input must be used.

8.2 Typical Applications

8.2.1 Basic 5-V Regulator

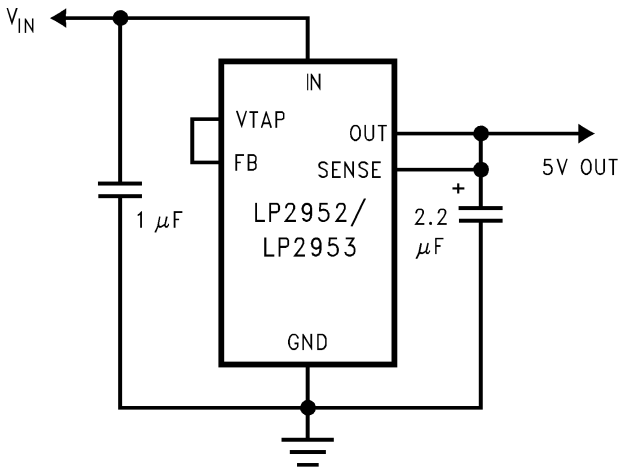

Figure 33. Basic 5-V Regulator

Typical Applications (continued)

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	DESIGN REQUIREMENT
Input voltage	6 V, ±10%, provided by the DC-DC converter switching at 1 MHz
Output voltage	5 V, ±1%
Output current	250 mA (maximum), 1 mA (minimum)
RMS noise, 10 Hz to 100 kHz	1 mV typical
PSRR at 1 kHz	50 dB typical

8.2.1.2 Detailed Design Procedure

At 150-mA loading, the dropout of the LP2952 and LP2953 has 600-mV maximum dropout over temperature — thus, a 1500-mV headroom is sufficient for operation over both input and output voltage accuracy. The efficiency of the LP2952 and LP2953 in this configuration is V_{OUT} / V_{IN} = 83.3%. Input and output capacitors are selected in accordance with the *External Capacitors* section. Ceramic capacitances of 1 µF for the input and one 2.2-µF capacitor for the output are selected. With an efficiency of 83.3% and a 250-mA maximum load, the internal power dissipation is 250 mW, which corresponds to a 19.2°C junction temperature rise for the SOIC package. With a V_{IN} – V_{OUT} differential of 1 V and a maximum load current of 250 mA the internal junction temperature (T_J) of the SOIC package will rise 19.2°C above the ambient temperature. With an 85°C maximum ambient temperature, the junction temperature is at 104.2°C. To minimize noise, a bypass capacitor of 100 pF is selected between OUT and FEEDBACK pins.

8.2.1.3 Application Curves

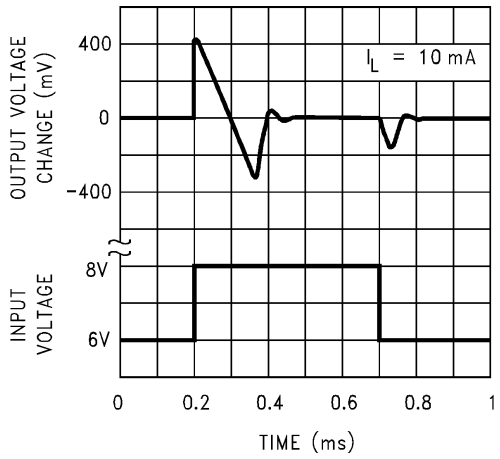

Figure 34. Line Transient Response

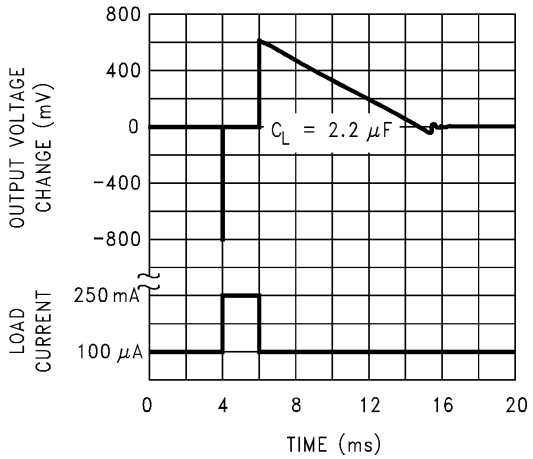

Figure 35. Load Transient Response

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8.2.2 5-V Current Limiter with Load Fault Indicator

Figure 36 is the example circuit for 5-V current limiter with load fault indicator, it has the following features:

- Output voltage equals $+V_{IN}$ minimum dropout voltage, which varies with output current. Current limits at a maximum of 380 mA (typical).
- Select R1 so that the comparator input voltage is 1.23 V at the output voltage which corresponds to the desired fault current value.

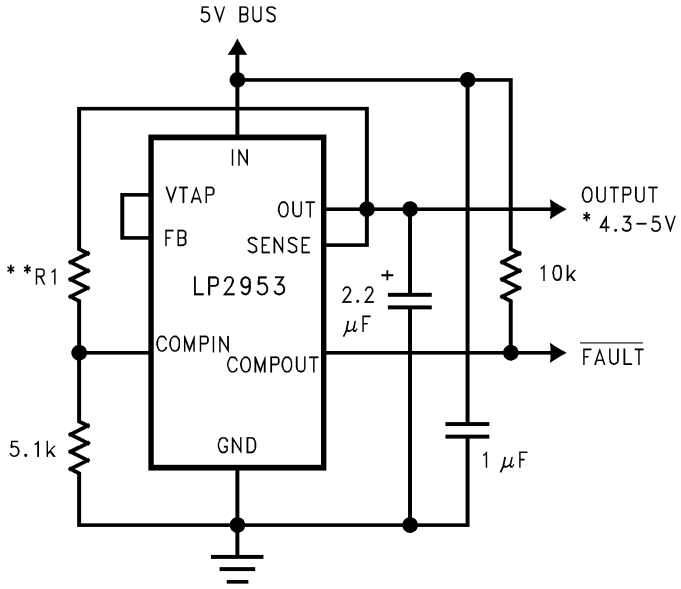

Figure 36. 5-V Current Limiter With Load Fault Indicator

8.2.3 Low Temperature Coefficient Current Sink

The LP2952 or LP2953 can be used as a low drift current source as Figure 37 shows. By connecting V_{OUT} to FEEDBACK, V_{OUT} will be regulated at 1.235 V, and current consumption at R is I_{OUT} = 1.23/R.

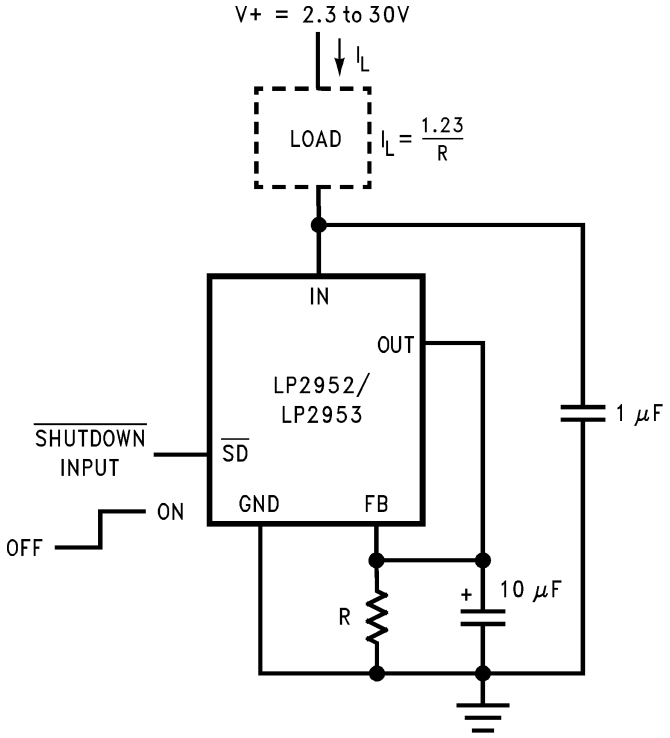

Figure 37. Low Temperature Coefficient Current Sink

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8.2.4 5-V Regulator With Error Flags for Low Battery and Out of Regulation

Figure 38 is the example circuit for 5-V regulator with error flags for low battery and out of regulation, it has the following features:

- Connect to logic or microprocessor control inputs.
- LOW BATT flag warns the user that the battery has discharged down to about 5.8 V, giving the user time to recharge the battery or power down some hardware with high power requirements. The output is still in regulation at this time.
- OUT OF REGULATION flag indicates when the battery is almost completely discharged, and can be used to initiate a power-down sequence.

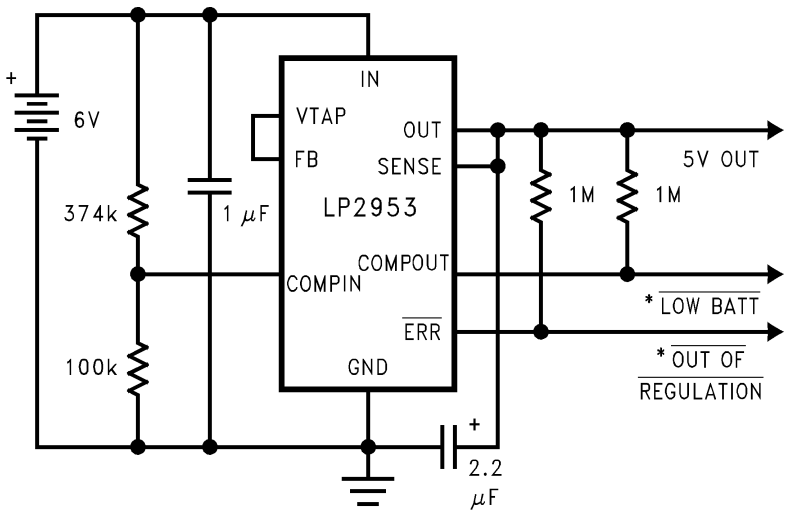

Figure 38. 5-V Regulator With Error Flags for Low Battery and Out of Regulation

8.2.5 5-V Battery Powered Supply With Backup and Low Battery Flag

Figure 39 is the example circuit for 5-V battery powered supply with backup and low battery flag, it has the following features:

- The circuit switches to the NI-CAD backup battery when the main battery voltage drops below about 5.6 V and returns to the main battery when its voltage is recharged to about 6 V.
- The 5-V MAIN output powers circuitry which requires no backup, and the 5-V MEMORY output powers critical circuitry which cannot be allowed to lose power.
- The $\overline{\text{BATTERY LOW}}$ flag goes low whenever the circuit switches to the NI-CAD backup battery.

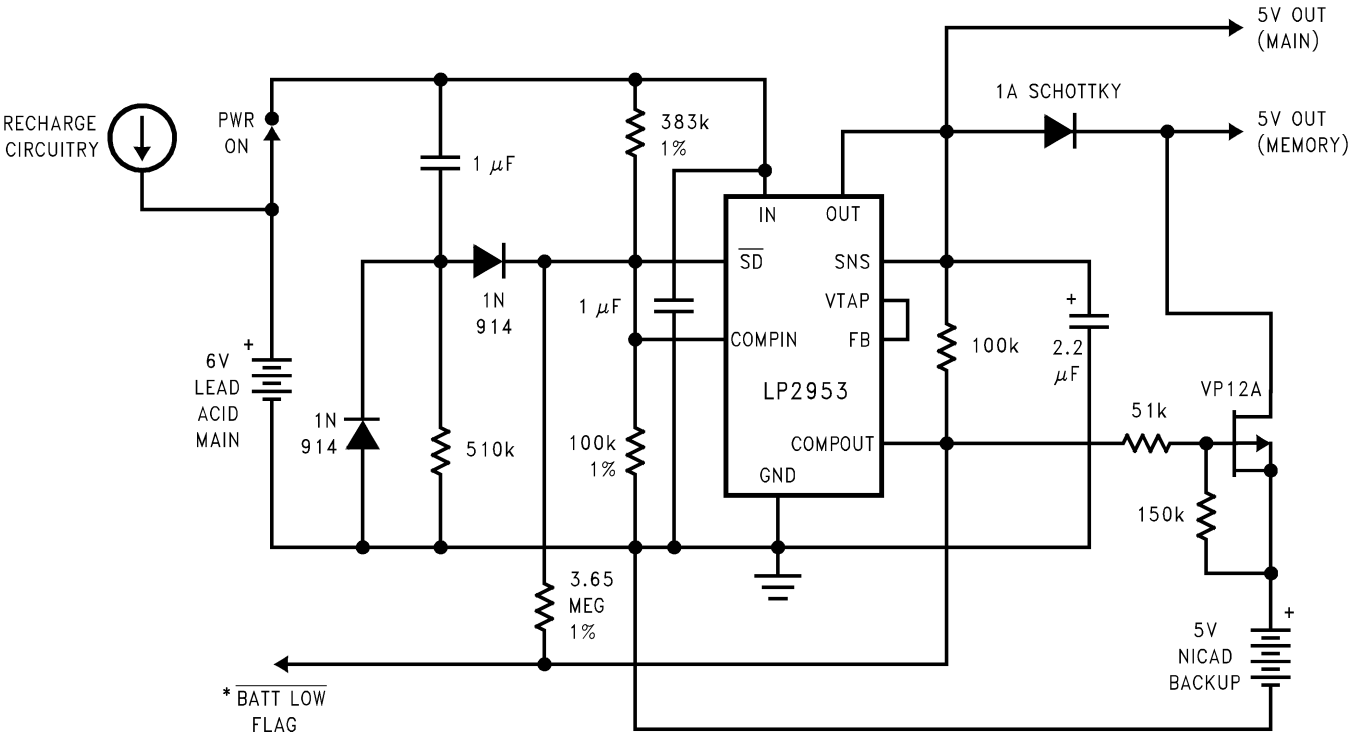

Figure 39. 5-V Battery Powered Supply With Backup and Low Battery Flag

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8.2.6 5-V Regulator With Timed Power-On Reset

Figure 40 is the circuit designed to generate a adjustable power on reset signal. Adjusting R_T and C_T values causes a certain delay time as Figure 41 shows.

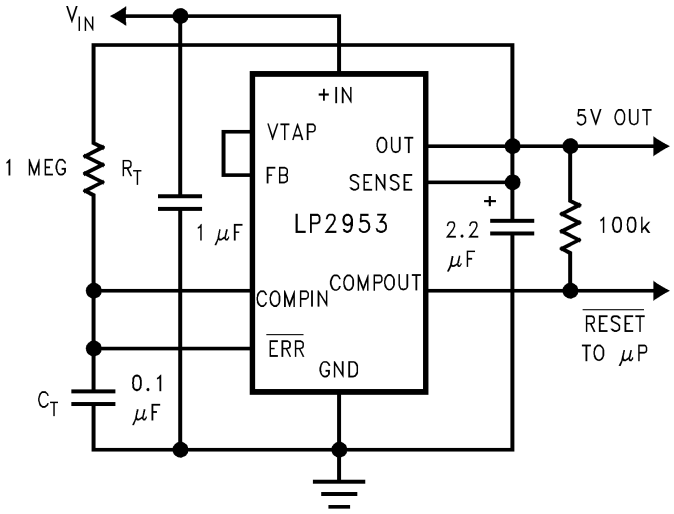
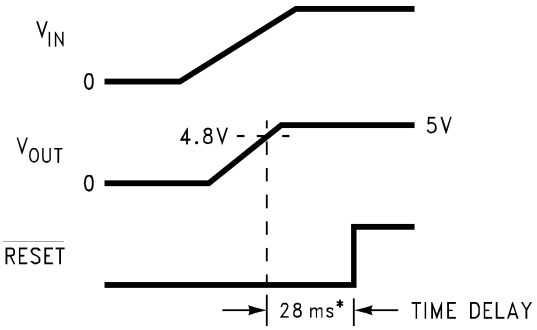


Figure 40. 5-V Regulator With Timed Power-On Reset



* R_T = 1 MΩ, C_T = 0.1 μF

Figure 41. Timing Diagram for Timed Power-On Reset

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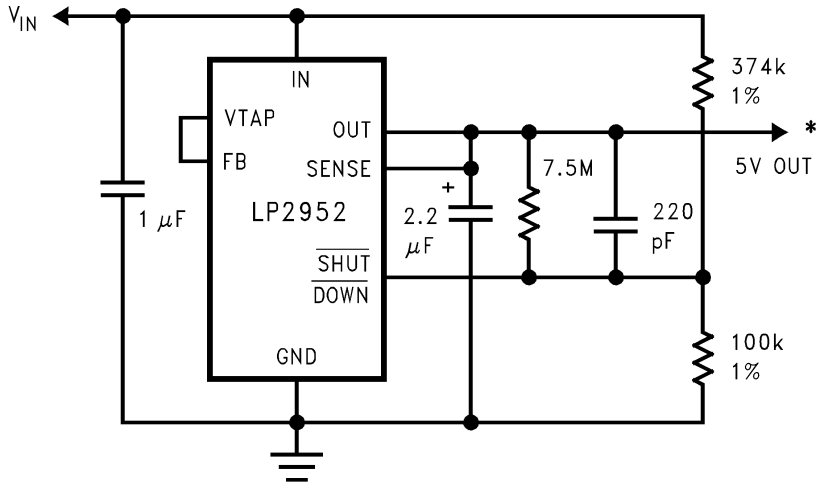
8.2.7 5-V Regulator With Snap-ON and Snap-OFF Features and Hysteresis

Figure 42 is the circuit designed to generate 5-V regulator with snap-ON and snap-OFF features and hysteresis. The output turns on at V_{IN} = 5.87 V and turns off at V_{IN} = 5.64 V.



* Turns on at V_{IN} = 5.87 V
Turns off at V_{IN} = 5.64 V
(for component values shown)

Figure 42. 5-V Regulator With Snap-ON and Snap-OFF Features and Hysteresis

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8.2.8 5-V Regulator With Error Flags for Low Battery and Out of Regulation With Snap-ON or Snap-OFF Output

Figure 43 is the circuit as 5-V regulator with error flags for low battery and out of regulation with Snap-ON/Snap-OFF output. It has the following features:

- Connect to logic or microprocessor control inputs.
- LOW BATT flag warns the user that the battery has discharged down to about 5.8 V, giving the user time to recharge the battery or shutdown hardware with high power requirements. The output is still in regulation at this time.
- OUT OF REGULATION flag goes low if the output goes below about 4.7 V, which could occur from a load fault.
- OUTPUT has Snap-ON or Snap-OFF feature. Regulator snaps ON at about 5.7-V input, and OFF at about 5.6 V.

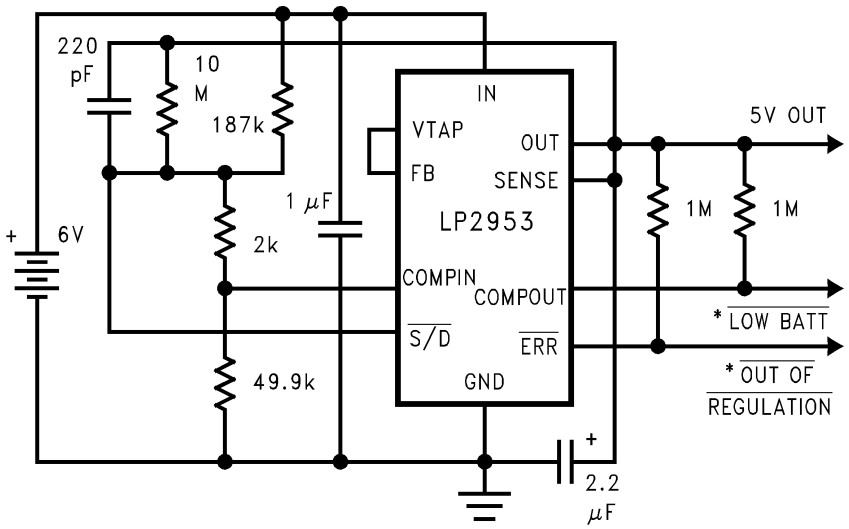


Figure 43. 5-V Regulator With Error Flags for Low Battery and Out of Regulation With Snap-ON or Snap-OFF Output

8.2.9 5-V Regulator With Timed Power-On Reset, Snap-ON and Snap-OFF Features, and Hysteresis

Figure 44 is the circuit designed for 5-V regulator with timed power-on reset, Snap-ON and Snap-OFF features, and hysteresis. Its timing diagram shows as Figure 45.

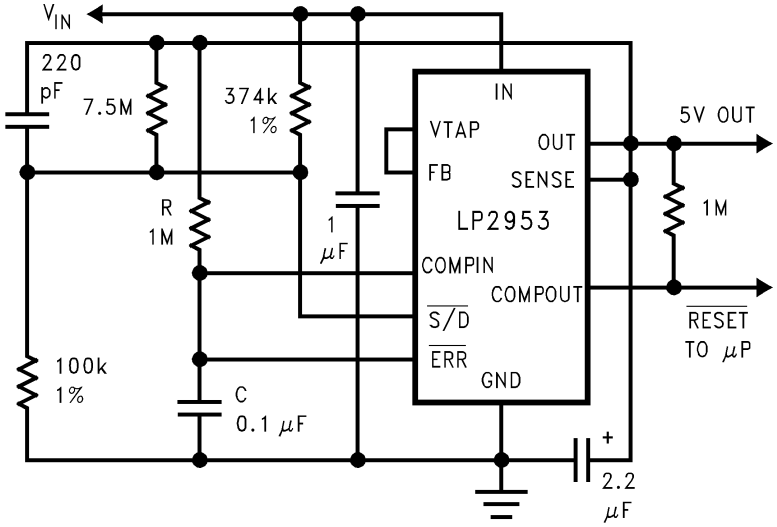
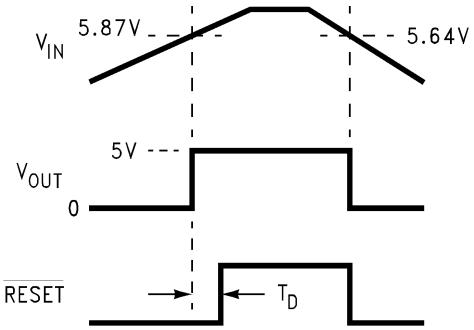


Figure 44. 5-V Regulator With Timed Power-On Reset, Snap-ON or Snap-OFF Feature, and Hysteresis



t_d = (0.28), RC = 28 ms for components shown.

Figure 45. Timing Diagram

9 Power Supply Recommendations

The LP2952 and LP2953 is designed to operate from an input voltage supply range between 2.3 V and 30 V. The input voltage range provides adequate headroom in order for the device to have a regulated output, normally V_{IN} should be 1 V higher than output voltage to provide a sufficient headroom. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

Maximum V_{IN} should never be higher than 30 V. Input voltage beyond 30 V may trigger EOS and cause permanent damage to the device.

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10 Layout

10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitors, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device. In most applications, this ground plane is necessary to meet thermal requirements.

10.2 Layout Example

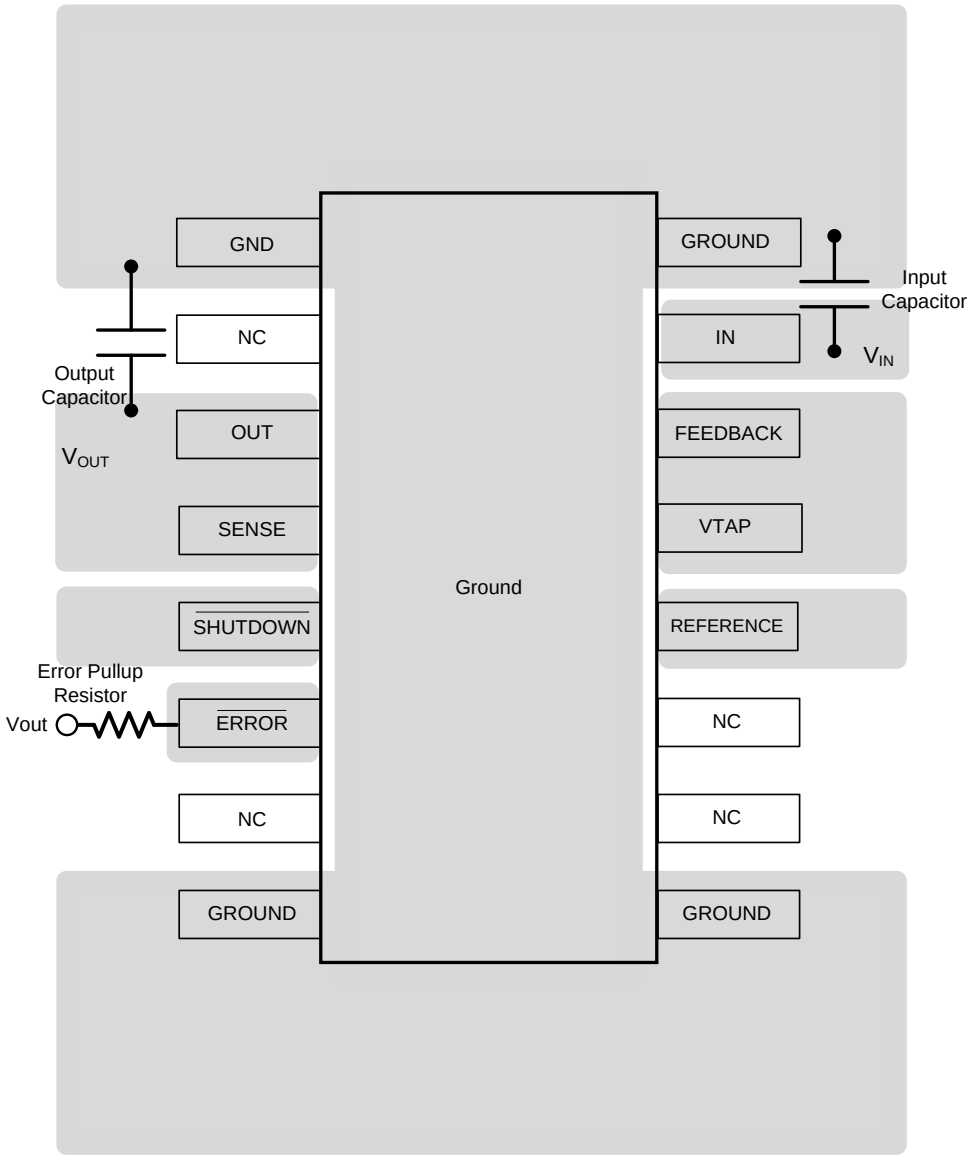

Figure 46. Layout Schematic

10.3 Power Dissipation: Heatsink Requirements (Industrial Temperature Range Devices)

The maximum allowable power dissipation for the LP2952 or LP2953 is limited by the maximum operating junction temperature (125°C) and the external factors that determine how quickly heat flows away from the part: the ambient temperature and the junction-to-ambient thermal resistance ($R_{\theta JA}$) for the specific application.

The industrial temperature range (−40°C ≤ T_J ≤ 125°C) parts are manufactured in PDIP and surface-mount packages which contain a copper lead frame that allows heat to be effectively conducted away from the die, through the ground pins of the IC, and into the copper of the PC board. Details on heatsinking using PC board copper are covered later.

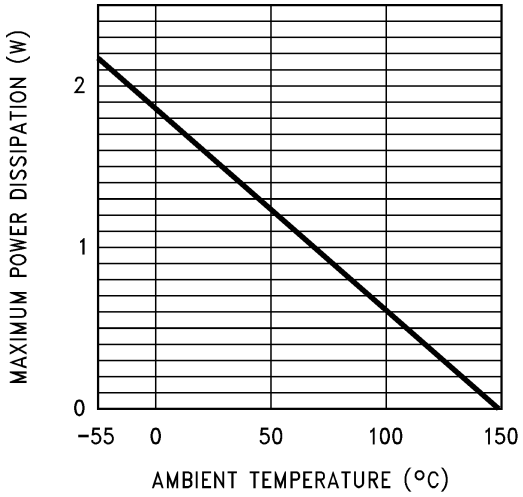

Figure 47. Power Dissipation vs Ambient Temperature for $R_{\theta JA}$ = 95°C/W

To determine if a heatsink is required, the maximum power dissipated by the regulator, $P_{(MAX)}$, must be calculated. It is important to remember that if the regulator is powered from a transformer connected to the AC line, the maximum specified AC input voltage must be used (because this produces the maximum DC input voltage to the regulator). Figure 48 shows the voltages and currents which are present in the circuit. The formula for calculating the power dissipated in the regulator is also shown in Figure 48:

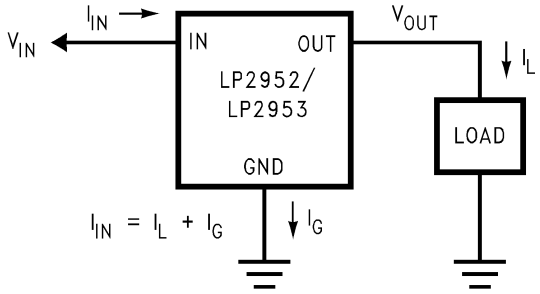

Figure 48. $P_{TOTAL} = (V_{IN} - V_{OUT}) I_{OUT} + (V_{IN}) I_G$ Current/Voltage Diagram

The next parameter which must be calculated is the maximum allowable temperature rise, $T_{R(MAX)}$. This is calculated by using the formula:

$$T_{R(MAX)} = T_{J(MAX)} - T_{A(MAX)} = R_{\theta JA} \times P_{(MAX)} \quad (3)$$

where:

- $T_{J(MAX)}$ is the maximum allowable junction temperature
- $T_{A(MAX)}$ is the maximum ambient temperature

Using the calculated values for $T_{R(MAX)}$ and $P_{(MAX)}$, the required value for junction-to-ambient thermal resistance, $R_{\theta JA}$, can now be found.

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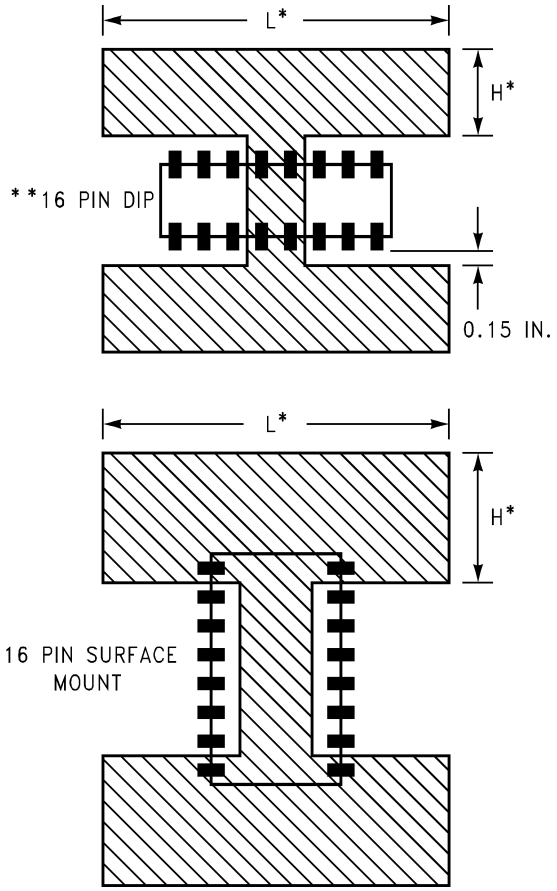
Power Dissipation: Heatsink Requirements (Industrial Temperature Range Devices) (continued)

The heatsink is made using the PC board copper. The heat is conducted from the die, through the lead frame (inside the part), and out the pins which are soldered to the PC board. The pins used for heat conduction are given in Table 2.

Table 2. Heat Conducting Pins

PART	PACKAGE	PINS
LP2953IN, LP2953AIN	16-pin PDIP	4, 5, 12, 13
LP2953IN-3.3, LP2953AIN-3.3		
LP2952IM, LP2952AIM	16-pin surface mount (SOIC)	1, 8, 9, 16
LP2952IM-3.3, LP2952AIM-3.3		
LP2953IM, LP2953AIM		
LP2953IM-3.3, LP2953AIM-3.3		

Figure 49 shows copper patterns which may be used to dissipate heat from the LP2952 and LP2953.



* For best results, use L = 2H.
** 14-Pin PDIP is similar, see Table 2 for pins designated for heatsinking.

Figure 49. Copper Heatsink Patterns

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11 Device and Documentation Support

11.1 Related Links

Table 3 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LP2952-N	Click here	Click here	Click here	Click here	Click here
LP2952A	Click here	Click here	Click here	Click here	Click here
LP2953	Click here	Click here	Click here	Click here	Click here
LP2953A	Click here	Click here	Click here	Click here	Click here

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2952AIM	NRND	SOIC	D	16	48	TBD	Call TI	Call TI	-40 to 125	LP2952AIM	
LP2952AIM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LP2952AIM	Samples
LP2952AIMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LP2952AIM	Samples
LP2952IM	NRND	SOIC	D	16	48	TBD	Call TI	Call TI	-40 to 125	LP2952IM	
LP2952IM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LP2952IM	Samples
LP2952IMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LP2952IM	Samples
LP2953AIM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LP2953AIM	Samples
LP2953AIMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LP2953AIM	Samples
LP2953IM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LP2953IM	Samples
LP2953IMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LP2953IM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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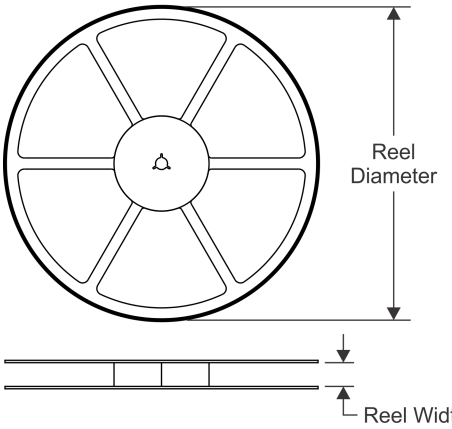
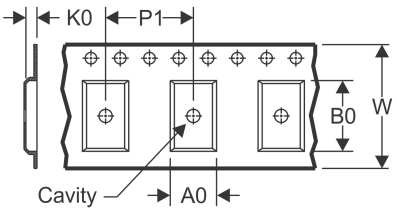
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

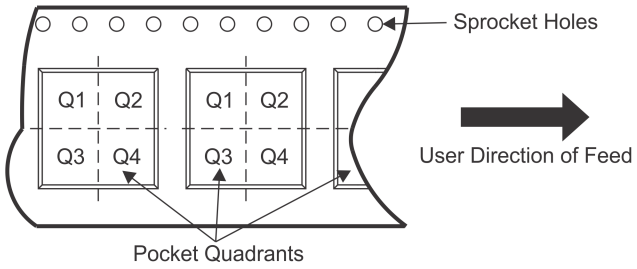


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

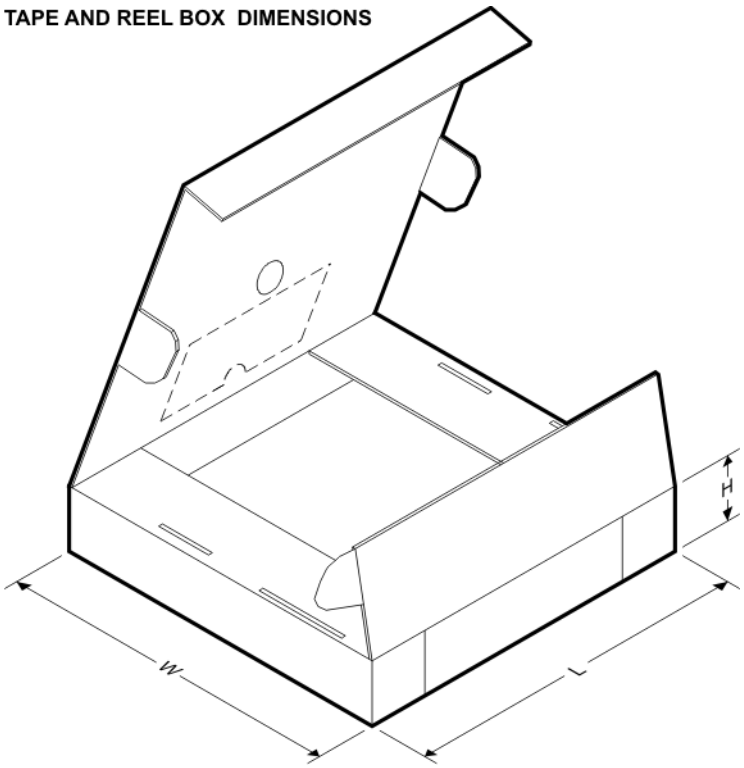
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2952AIMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
LP2952IMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
LP2953AIMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
LP2953IMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

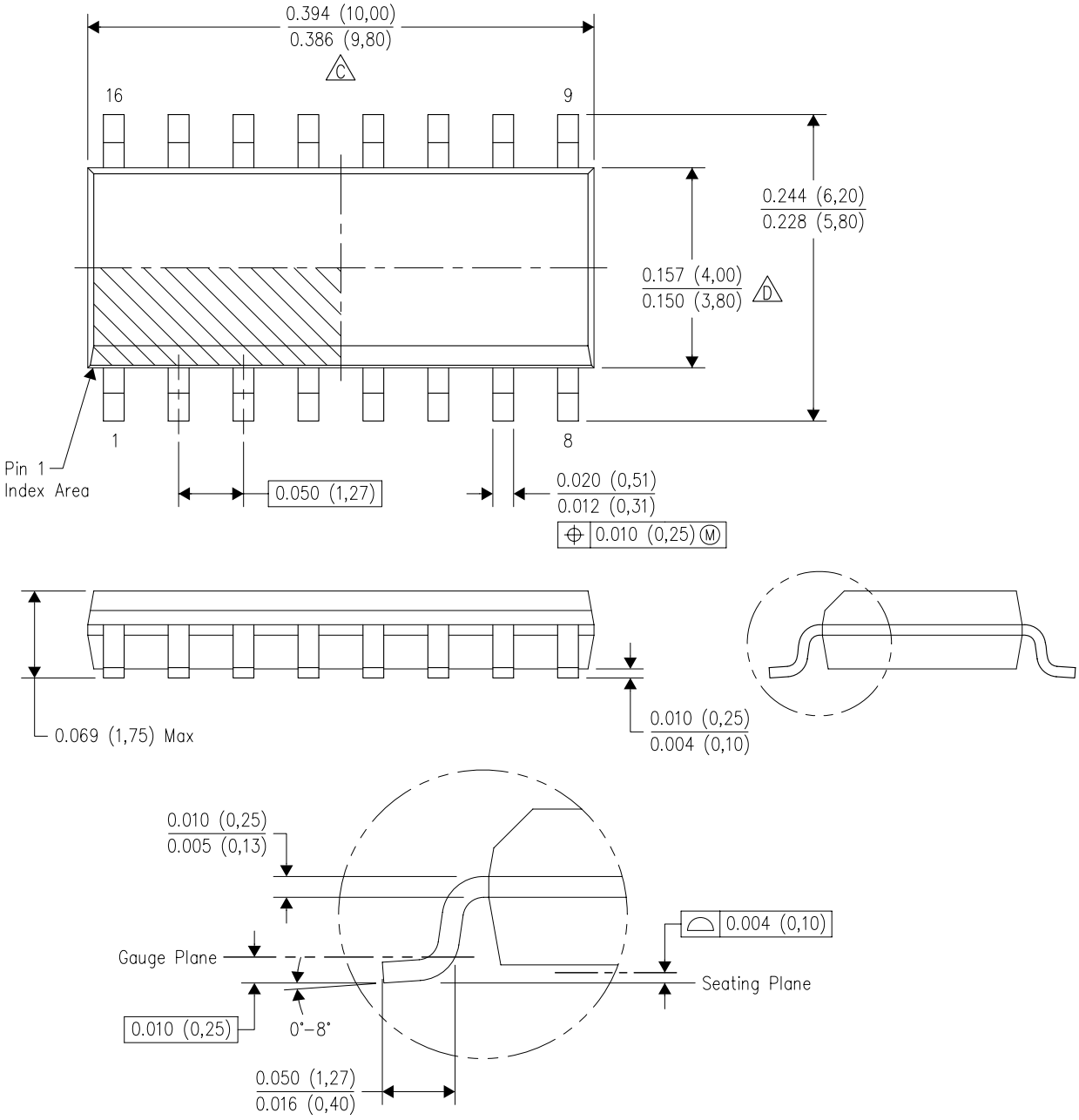
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2952AIMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0
LP2952IMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0
LP2953AIMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0
LP2953IMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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