



**THE DATASHEET OF
LP2985AIM5X-3.3/NOPB**



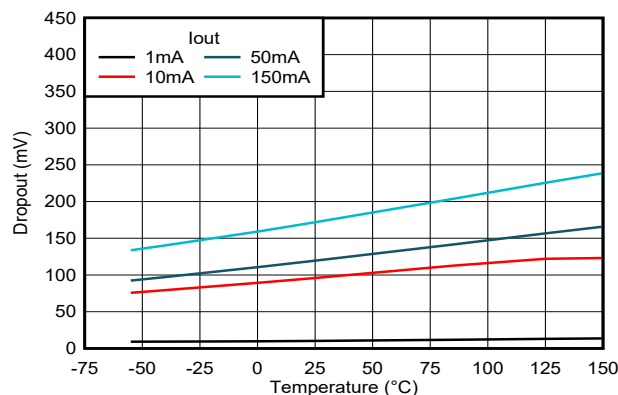
LP2985-N 150-mA, Low-Noise, Low-Power, Ultra-Low-Dropout Regulator in a SOT-23 Package

1 Features

- V_{IN} range: 2.5 V to 16 V
- V_{OUT} range (new chip):
 - 1.2 V to 5.0 V (fixed, 100-mV steps)
- V_{OUT} range (legacy chip): 2.5 V to 6.1 V
- V_{OUT} accuracy:
 - $\pm 1\%$ for A-grade legacy chip
 - $\pm 1.5\%$ for standard-grade legacy chip
 - $\pm 0.5\%$ for new chip only
- Output accuracy over load, and temperature:
 - $\pm 1\%$ for new chip
- Output current: Up to 150 mA
- Low I_Q (new chip): 71 μA at $I_{LOAD} = 0$ mA
- Low I_Q (new chip): 750 μA at $I_{LOAD} = 150$ mA
- Shutdown current:
 - 0.05 μA (typ) for legacy chip
 - 1.12 μA (typ) for new chip
- Low noise: 30 μV_{RMS} with 10-nF bypass capacitor
- Output current limiting and thermal protection
- Stable with 2.2- μF ceramic capacitors
- High PSRR: 70 dB at 1 kHz, 40 dB at 1 MHz
- Operating junction temperature: -40°C to $+125^\circ\text{C}$
- Package: 5-pin SOT-23 (DBV) ultra-low dropout voltage

2 Applications

- Washers and dryers
- Land mobile radios
- Active antenna system mMIMO
- Cordless power tools
- Motor drives and control boards



Dropout Voltage vs Temperature for New Chip

3 Description

The LP2985-N is a fixed-output, wide-input, low-noise, low-dropout voltage regulator supporting an input voltage range from 2.5 V to 16 V and up to 150 mA of load current. The LP2985-N supports an output range of 1.2 V to 5.0 V (new chip) and 2.5 V to 6.1 V (legacy chip).

Additionally, the LP2985-N (new chip) has a 1% output accuracy across load and temperature that can meet the needs of low-voltage microcontrollers (MCUs) and processors.

Low output noise of 30 μV_{RMS} (with 10-nF bypass capacitors) and wide bandwidth PSRR performance of greater than 70 dB at 1 kHz and 40 dB at 1 MHz help attenuate the switching frequency of an upstream DC/DC converter and minimize post regulator filtering.

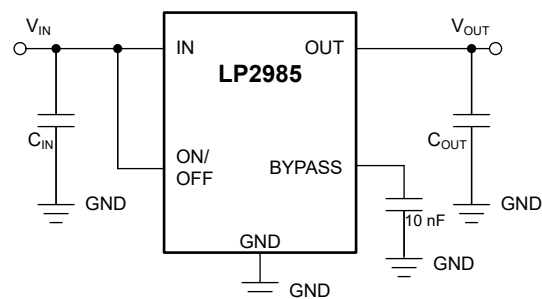
The internal soft-start time and current-limit protection reduce inrush current during start up, thus minimizing input capacitance. Standard protection features, such as overcurrent and overtemperature protection, are included.

The LP2985-N is available in a 5-pin, 2.9-mm \times 1.6-mm SOT-23 (DBV) package.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
LP2985-N	DBV (SOT-23, 5)	2.9 mm \times 2.8 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length \times width) is a nominal value and includes pins, where applicable.



Typical Application Circuit



Table of Contents

1 Features	1	7.4 Device Functional Modes.....	18
2 Applications	1	8 Application and Implementation	19
3 Description	1	8.1 Application Information.....	19
4 Revision History	2	8.2 Typical Application.....	22
5 Pin Configuration and Functions	3	8.3 Power Supply Recommendations.....	27
6 Specifications	4	8.4 Layout.....	27
6.1 Absolute Maximum Ratings.....	4	9 Device and Documentation Support	29
6.2 ESD Ratings.....	4	9.1 Documentation Support.....	29
6.3 Recommended Operating Conditions.....	4	9.2 Device Nomenclature.....	29
6.4 Thermal Information.....	5	9.3 Receiving Notification of Documentation Updates.....	29
6.5 Electrical Characteristics.....	5	9.4 Support Resources.....	29
6.6 Typical Characteristics.....	9	9.5 Trademarks.....	29
7 Detailed Description	15	9.6 Electrostatic Discharge Caution.....	29
7.1 Overview.....	15	9.7 Glossary.....	29
7.2 Functional Block Diagrams.....	15	10 Mechanical, Packaging, and Orderable Information	29
7.3 Feature Description.....	16		

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision Z (May 2023) to Revision AA (July 2023)	Page
• Widening IGND spec limits to accommodate complete VOUT range.....	5

Changes from Revision Y (December 2016) to Revision Z (May 2023)	Page
• Added M3-suffix devices to document.....	1
• Changed entire document to align with new format and updated detailed description of the features, functions, and applications of the LDO.....	1
• Added links to <i>Applications</i> section.....	1
• Added M3-suffix (new chip) curves to <i>Typical Characteristics</i> section.....	9
• Added <i>Block Diagram for New Chip</i> to <i>Functional Block Diagrams</i> section.....	15
• Added M3-suffix (new chip) curves to <i>Application Curves</i> section.....	23

5 Pin Configuration and Functions

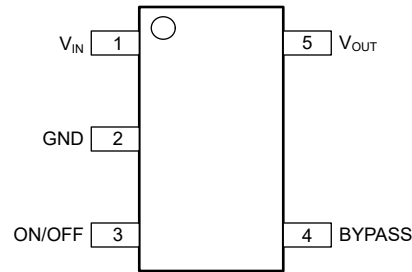


Figure 5-1. DBV Package, 5-Pin SOT-23 (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
BYPASS	4	I/O	BYPASS pin to achieve low noise performance. Connecting an external capacitor between the BYPASS pin and ground reduces reference voltage noise. See the Recommended Operating Conditions section for more information.
GND	2	—	Ground
ON/OFF	3	I	Enable pin for the LDO. Driving the ON/OFF pin high enables the device. Driving this pin low disables the device. High and low thresholds are listed in the Electrical Characteristics table. Tie this pin to V_{IN} if unused.
V_{IN}	1	I	Input supply pin. Use a capacitor with a value of 1 μF or larger from this pin to ground. See the Input and Output Capacitor Requirements section for more information.
V_{OUT}	5	O	Output of the regulator. Use a capacitor with a value of 2.2 μF or larger from this pin to ground. ⁽¹⁾ See the Input and Output Capacitor Requirements section for more information.

- (1) The nominal output capacitance must be greater than 2.2 μF . Throughout this document, the nominal derating on these capacitors is 50%. Make sure that the effective capacitance at the pin is greater than 1 μF .

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT
V _{IN}	Continuous input voltage range (for legacy chip)	-0.3	16	V
	Continuous input voltage range (for new chip)	-0.3	18	
V _{OUT}	Output voltage range (for legacy chip)	-0.3	9	
	Output voltage range (for new chip)	-0.3	V _{IN} + 0.3 or 9 (whichever is smaller)	
V _{BYPASS}	BYPASS pin voltage range (for new chip)	-0.3	3	
V _{ON/OFF}	ON/OFF pin voltage range (for legacy chip)	-0.3	16	
	ON/OFF pin voltage range (for new chip)	-0.3	18	
Current	Maximum output	Internally limited		
Temperature	Operating junction, T _J	-55	150	°C
	Storage, T _{stg}	-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages with respect to GND.

6.2 ESD Ratings

			VALUE (Legacy Chip)	VALUE (New Chip)	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	±1000	

- (1) JEDEC document JEP155 states that 2-kV HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V _{IN}	Supply input voltage (for legacy chip)	2.2		16	V
	Supply input voltage (for new chip)	2.5		16	
V _{OUT}	Output voltage (for legacy chip)	1.2		10.0	
	Output voltage (for new chip)	1.2		5.0	
V _{BYPASS}	Bypass voltage		1.2		
V _{ON/OFF}	Enable voltage (for legacy chip)	0		V _{IN}	
	Enable voltage (for new chip)	0		16	
I _{OUT}	Output current	0		150	
C _{IN} ^{(2) (1)}	Input capacitor		1		μF
C _{OUT}	Output capacitor (for legacy chip)	2.2	4.7		μF
	Output capacitance (for new chip) ⁽¹⁾	1	2.2	200	
T _J	Operating junction temperature	-40		125	°C

- (1) All capacitor values are assumed to derate to 50% of the nominal capacitor value. Maintain an effective output capacitance of 1 μF minimum for stability.
- (2) Minimum input capacitor of 2.2 μF is required if the source impedance is more than 0.5 Ω.

6.4 Thermal Information

THERMAL METRIC (2) (1)		Legacy Chip	New Chip	UNIT
		DBV (SOT23-5)	DBV (SOT23-5)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	205.4	178.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.8	77.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.7	47.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.3	15.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	46.3	46.9	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.
- (2) Thermal performance results are based on the JEDEC standard of 2s2p PCB configuration. These thermal metric parameters can be further improved by 35-55% based on thermally optimized PCB layout designs. See the analysis of the [Impact of board layout on LDO thermal performance](#) application report.

6.5 Electrical Characteristics

specified at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 1.0\text{ V}$ or $V_{IN} = 2.5\text{ V}$ (whichever is greater), $I_{OUT} = 1\text{ mA}$, $V_{ON/OFF} = 2\text{ V}$, $C_{IN} = 1.0\text{ }\mu\text{F}$, and $C_{OUT} = 2.2\text{ }\mu\text{F}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ΔV_{OUT}	Output voltage tolerance	$I_L = 1\text{ mA}$	Legacy chip (standard grade)	-1.5		1.5	%
			Legacy chip (A grade)	-1.0		1.0	
			New chip	-0.5		0.5	
		$1\text{ mA} \leq I_L \leq 50\text{ mA}$	Legacy chip (standard grade)	-2.5		2.5	
			Legacy chip (A grade)	-1.5		1.5	
			New chip	-0.5		0.5	
		$1\text{ mA} \leq I_L \leq 150\text{ mA}$	Legacy chip (standard grade)	-3.0		3.0	
			Legacy chip (A grade)	-2.5		2.5	
			New chip	-0.5		0.5	
		$1\text{ mA} \leq I_L \leq 50\text{ mA}$, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	Legacy chip (standard grade)	-3.5		3.5	
			Legacy chip (A grade)	-2.5		2.5	
			New chip	-1		1	
$1\text{ mA} \leq I_L \leq 150\text{ mA}$, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	Legacy chip (standard grade)	-4.0		4.0			
	Legacy chip (A grade)	-3.5		3.5			
	New chip	-1		1			
$\Delta V_{OUT(\Delta V_{IN})}$	Line regulation	$V_{O(NOM)} + 1\text{ V} \leq V_{IN} \leq 16\text{ V}$	Legacy chip	0.007	0.014	%V	
			New chip	0.002	0.014		
		$V_{O(NOM)} + 1\text{ V} \leq V_{IN} \leq 16\text{ V}$, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	Legacy chip	0.007	0.032		
			New chip	0.002	0.032		

6.5 Electrical Characteristics (continued)

specified at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 1.0\text{ V}$ or $V_{IN} = 2.5\text{ V}$ (whichever is greater), $I_{OUT} = 1\text{ mA}$, $V_{ON/OFF} = 2\text{ V}$, $C_{IN} = 1.0\text{ }\mu\text{F}$, and $C_{OUT} = 2.2\text{ }\mu\text{F}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT		
$V_{IN} - V_{OUT}$	Dropout voltage ⁽¹⁾	$I_{OUT} = 0\text{ mA}$	Legacy chip		1	3	mV		
			New chip		1	2.75			
		$I_{OUT} = 0\text{ mA}, -40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	Legacy chip					5	
			New chip						3
		$I_{OUT} = 1\text{ mA}$	Legacy chip					7	10
			New chip					11.5	14
		$I_{OUT} = 1\text{ mA}, -40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	Legacy chip						15
			New chip						17
		$I_{OUT} = 10\text{ mA}$	Legacy chip					40	60
			New chip					98	115
		$I_{OUT} = 10\text{ mA}, -40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	Legacy chip						90
			New chip						148
		$I_{OUT} = 50\text{ mA}$	Legacy chip					120	150
			New chip					120	145
		$I_{OUT} = 50\text{ mA}, -40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	Legacy chip						225
			New chip						184
		$I_{OUT} = 150\text{ mA}$	Legacy chip					280	350
			New chip					180	198
		$I_{OUT} = 150\text{ mA}, -40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	Legacy chip						575
			New chip						254

6.5 Electrical Characteristics (continued)

specified at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 1.0\text{ V}$ or $V_{IN} = 2.5\text{ V}$ (whichever is greater), $I_{OUT} = 1\text{ mA}$, $V_{ON/OFF} = 2\text{ V}$, $C_{IN} = 1.0\text{ }\mu\text{F}$, and $C_{OUT} = 2.2\text{ }\mu\text{F}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{GND}	GND pin current	$I_{OUT} = 0\text{ mA}$	Legacy chip	65	95	μA	
			New chip	69	95		
		$I_{OUT} = 0\text{ mA}, -40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	Legacy chip	125			
			New chip	123			
		$I_{OUT} = 1\text{ mA}$	Legacy chip	75	110		
			New chip	78	110		
		$I_{OUT} = 1\text{ mA}, -40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	Legacy chip	170			
			New chip	140			
		$I_{OUT} = 10\text{ mA}$	Legacy chip	120	220		
			New chip	175	210		
		$I_{OUT} = 10\text{ mA}, -40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	Legacy chip	400			
			New chip	250			
		$I_{OUT} = 50\text{ mA}$	Legacy chip	350	600		
			New chip	380	440		
		$I_{OUT} = 50\text{ mA}, -40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	Legacy chip	900			
			New chip	650			
		$I_{OUT} = 150\text{ mA}$	Legacy chip	850	1200		
			New chip	765	890		
		$I_{OUT} = 150\text{ mA}, -40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	Legacy chip	2000			
			New chip	1060			
$V_{ON/OFF} < 0.3\text{ V}, V_{IN} = 16\text{ V}$	Legacy chip	0.01	0.08				
	New chip	1.25	1.75				
$V_{ON/OFF} < 0.15\text{ V}, V_{IN} = 16\text{ V}, -40^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$	Legacy chip	0	1				
	New chip	1.12	2.25				
$V_{ON/OFF} < 0.15\text{ V}, V_{IN} = 16\text{ V}, -40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	Legacy chip	0.01	2				
	New chip	1.12	2.75				
V_{UVLO+}	Rising bias supply UVLO	V_{IN} rising, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$		2.2	2.4	V	
V_{UVLO-}	Falling bias supply UVLO	V_{IN} falling, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	New chip	1.9		V	
$V_{UVLO(HYST)}$	UVLO hysteresis	$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$		0.130		V	
$V_{ON/OFF}$	ON/OFF input voltage	Low = Output OFF	Legacy chip	0.55	V		
			New chip	0.72			
		Low = Output OFF, $V_{OUT} + 1 \leq V_{IN} \leq 16\text{ V}, -40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	Legacy chip	0.15			
			New chip	0.15			
		High = Output ON	Legacy chip	1.4			
			New chip	0.85			
		High = Output ON, $V_{OUT} + 1 \leq V_{IN} \leq 16\text{ V}, -40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	Legacy chip	1.6			
			New chip	1.6			

6.5 Electrical Characteristics (continued)

specified at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 1.0\text{ V}$ or $V_{IN} = 2.5\text{ V}$ (whichever is greater), $I_{OUT} = 1\text{ mA}$, $V_{ON/OFF} = 2\text{ V}$, $C_{IN} = 1.0\text{ }\mu\text{F}$, and $C_{OUT} = 2.2\text{ }\mu\text{F}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$I_{ON/OFF}$	ON/OFF input current	$V_{ON/OFF} = 0\text{ V}$	Legacy chip	0.01		μA	
			New chip	0.42			
		$V_{ON/OFF} = 0\text{ V}$, $V_{OUT} + 1 \leq V_{IN} \leq 16\text{ V}$, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	Legacy chip		-1		
			New chip		-0.9		
		$V_{ON/OFF} = 5\text{ V}$	Legacy chip		5		
			New chip		0.011		
$V_{ON/OFF} = 5\text{ V}$, $V_{OUT} + 1 \leq V_{IN} \leq 16\text{ V}$, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	Legacy chip			15			
	New chip			2.20			
$I_{O(PK)}$	Peak output current	$V_{OUT} \geq V_{O(NOM)} - 5\%$ (steady state)	Legacy chip	300	350	mA	
			New chip	300	350		
$I_{O(SC)}$	Short output current	$R_L = 0\text{ }\Omega$ (steady state)	Legacy chip		400	mA	
			New chip		375		
$\Delta V_O/\Delta V_{IN}$	Ripple rejection	$f = 1\text{ kHz}$, $C_{BYPASS} = 10\text{ nF}$, $C_{OUT} = 10\text{ }\mu\text{F}$	Legacy chip		45	dB	
			New chip		78		
V_n	Output noise voltage	Bandwidth = 300 Hz to 50 kHz, $C_{BYPASS} = 10\text{ nF}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 150\text{ mA}$	Legacy chip		30	μVRMS	
			New chip		30		
T_{sd+}	Thermal shutdown threshold	Shutdown, temperature increasing	New chip		170	$^\circ\text{C}$	
T_{sd-}		Reset, temperature decreasing			150		

- (1) Dropout voltage (V_{DO}) is defined as the input-to-output differential at which the output voltage drops 100 mV below the value measured with a 1 V differential. V_{DO} is measured with $V_{IN} = V_{OUT(nom)} - 100\text{ mV}$ for fixed output devices.

6.6 Typical Characteristics

at operating temperature $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 1.0\text{ V}$ or 2.5 V (whichever is greater), $I_{OUT} = 1\text{ mA}$, ON/OFF pin tied to V_{IN} , $C_{IN} = 1.0\ \mu\text{F}$, and $C_{OUT} = 4.7\ \mu\text{F}$ (unless otherwise noted)

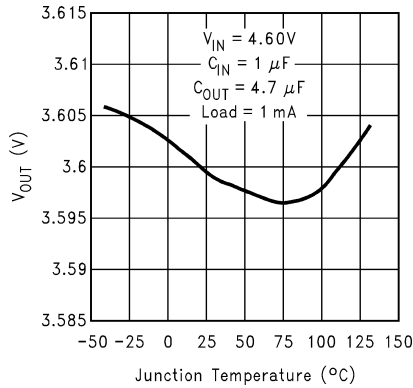


Figure 6-1. V_{OUT} vs Temperature for Legacy Chip

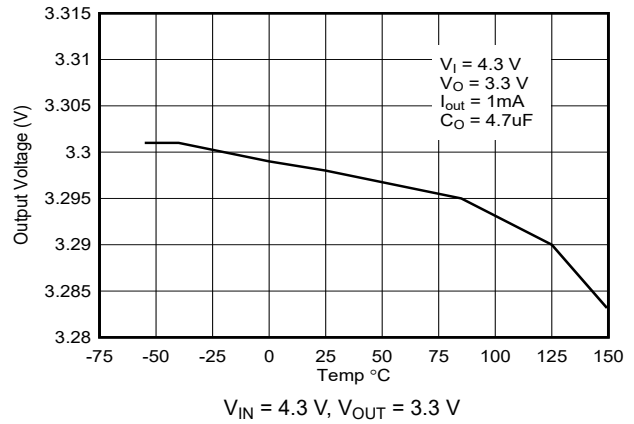


Figure 6-2. V_{OUT} vs Temperature for New Chip

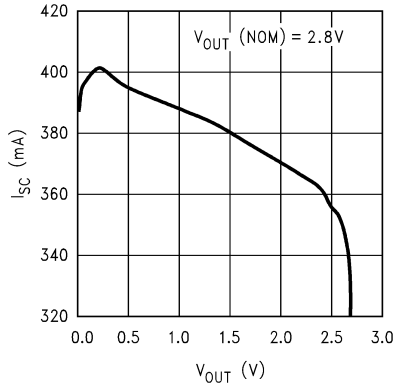


Figure 6-3. Short-Circuit Current vs Output Voltage for Legacy Chip

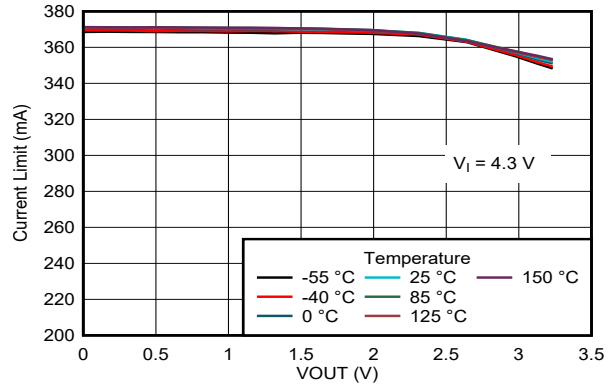


Figure 6-4. Short-Circuit Current vs Output Voltage for New Chip

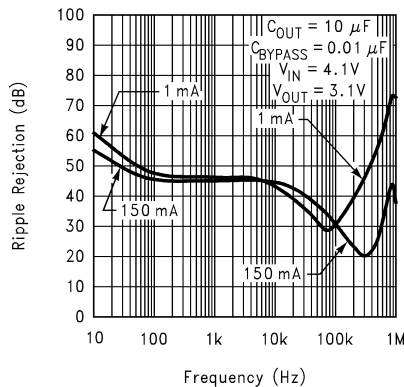


Figure 6-5. Ripple Rejection vs Frequency for Legacy Chip

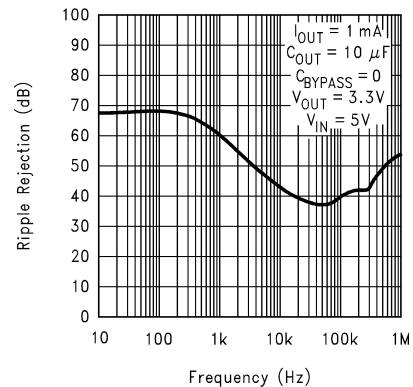


Figure 6-6. Ripple Rejection vs Frequency for Legacy Chip

6.6 Typical Characteristics (continued)

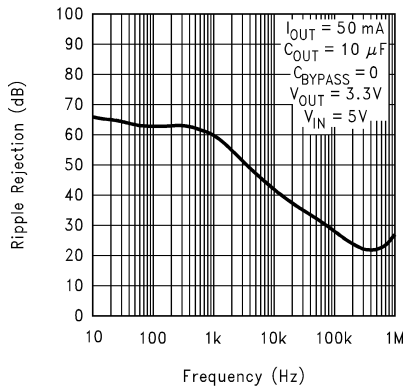


Figure 6-7. Ripple Rejection vs Frequency for Legacy Chip

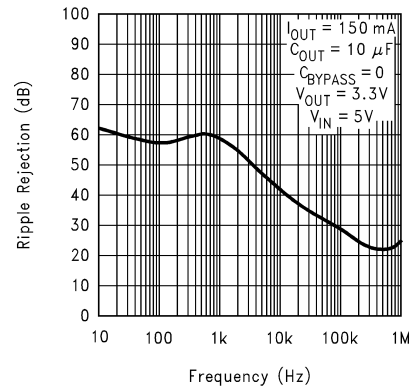


Figure 6-8. Ripple Rejection vs Frequency for Legacy Chip

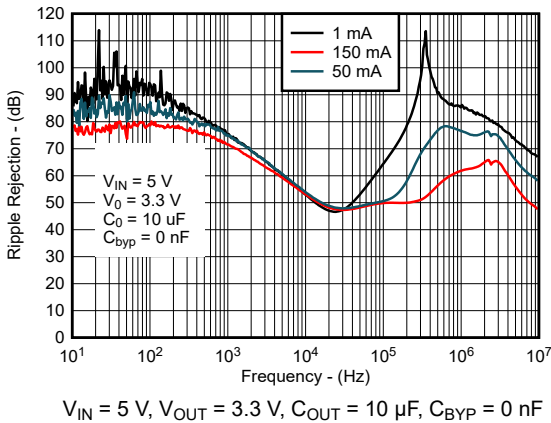


Figure 6-9. Ripple Rejection vs Frequency for New Chip

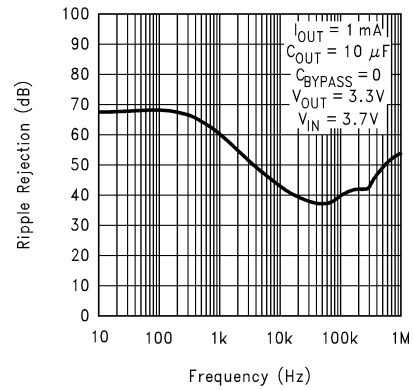


Figure 6-10. Ripple Rejection vs Frequency for Legacy Chip

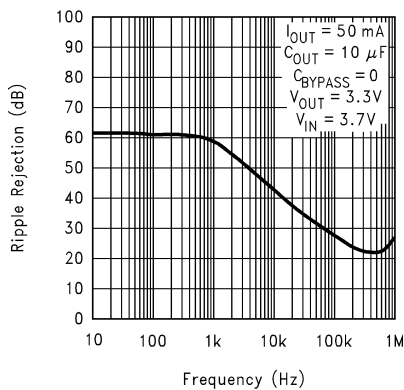


Figure 6-11. Ripple Rejection vs Frequency for Legacy Chip

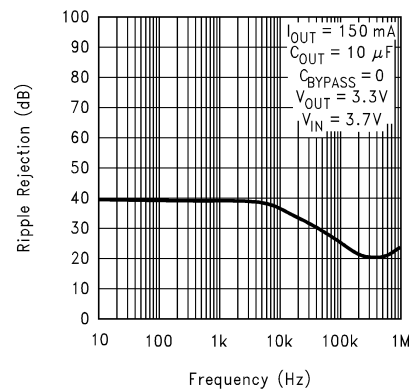


Figure 6-12. Ripple Rejection vs Frequency for Legacy Chip

6.6 Typical Characteristics (continued)

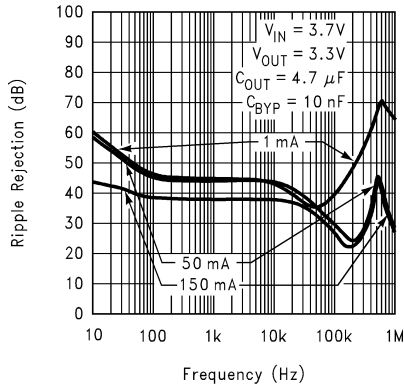


Figure 6-13. Ripple Rejection vs Frequency for Legacy Chip

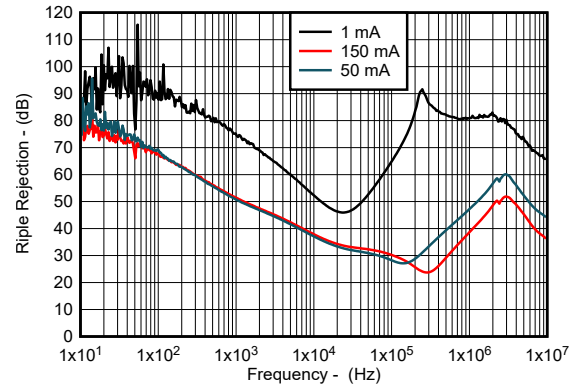


Figure 6-14. Ripple Rejection vs Frequency for New Chip

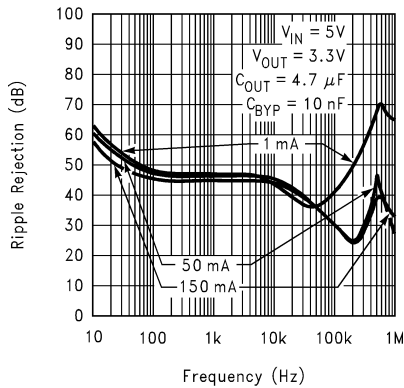


Figure 6-15. Ripple Rejection vs Frequency for Legacy Chip

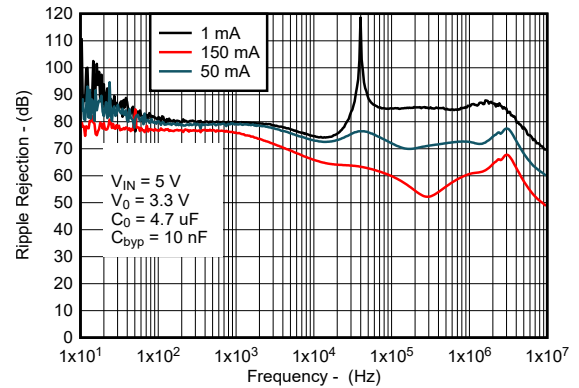


Figure 6-16. Ripple Rejection vs Frequency for New Chip

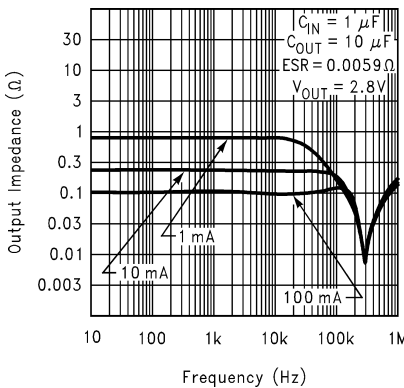


Figure 6-17. Output Impedance vs Frequency for Legacy Chip

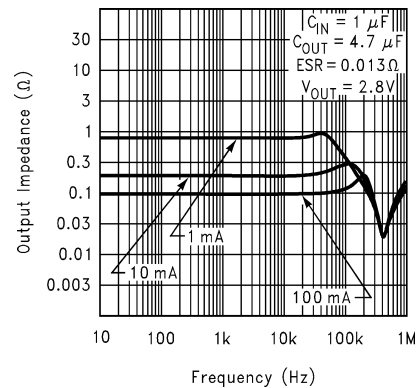


Figure 6-18. Output Impedance vs Frequency for Legacy Chip

6.6 Typical Characteristics (continued)

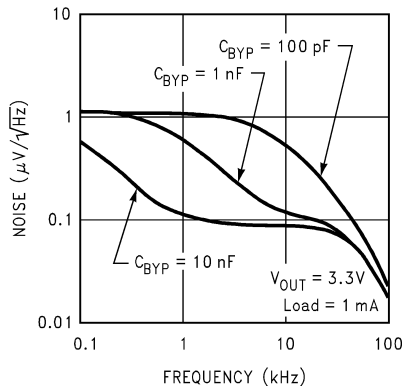


Figure 6-19. Output Noise Density for Legacy Chip

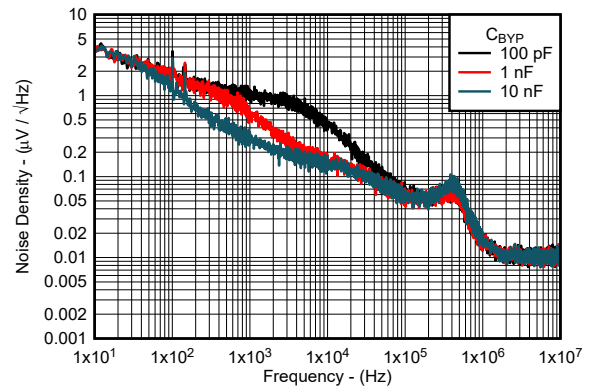


Figure 6-20. Output Noise Density vs Frequency for New Chip

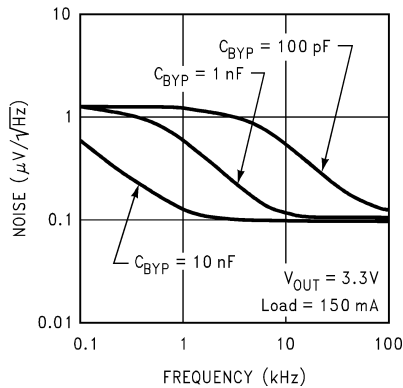


Figure 6-21. Output Noise Density for Legacy Chip

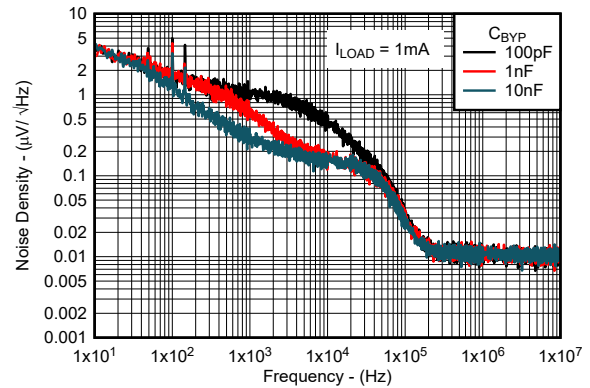


Figure 6-22. Output Noise Density vs Frequency for New Chip

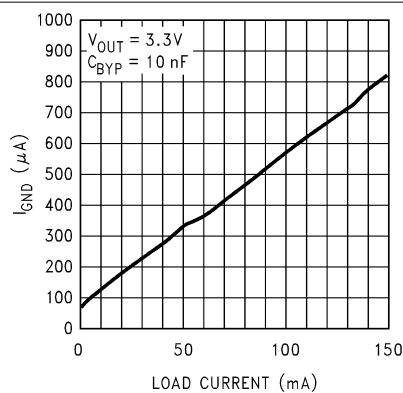


Figure 6-23. Ground Pin vs Load Current for Legacy Chip

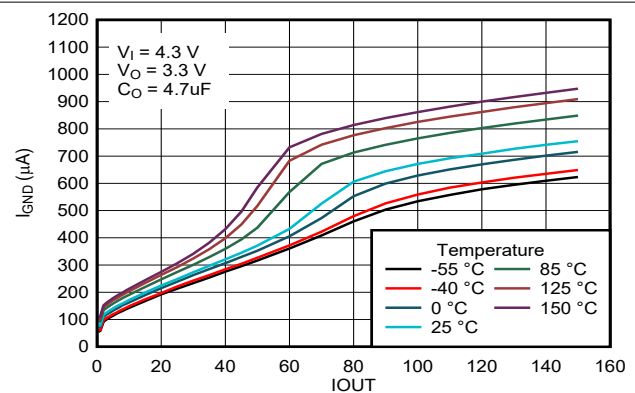


Figure 6-24. Ground Pin Current vs Load Current for New Chip

6.6 Typical Characteristics (continued)

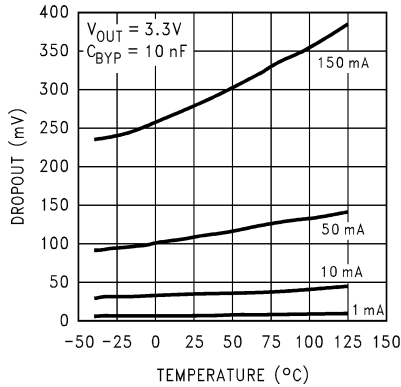


Figure 6-25. Dropout Voltage vs Temperature for Legacy Chip

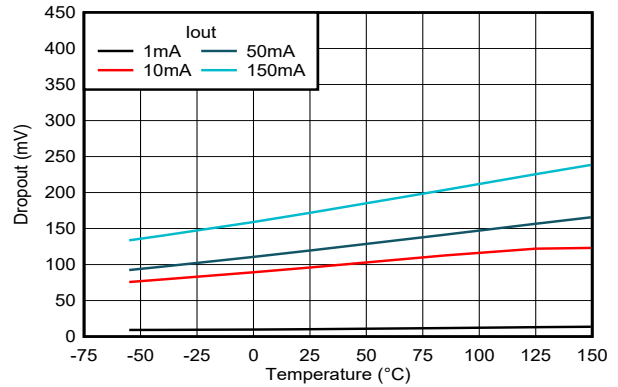


Figure 6-26. Dropout Voltage vs Temperature for New Chip

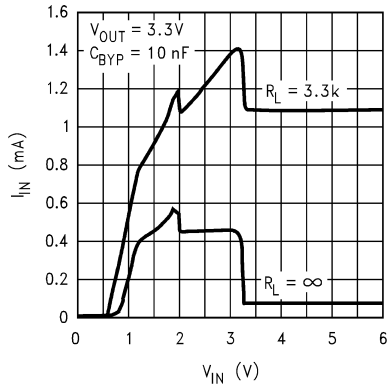


Figure 6-27. Input Current vs V_{IN} for Legacy Chip

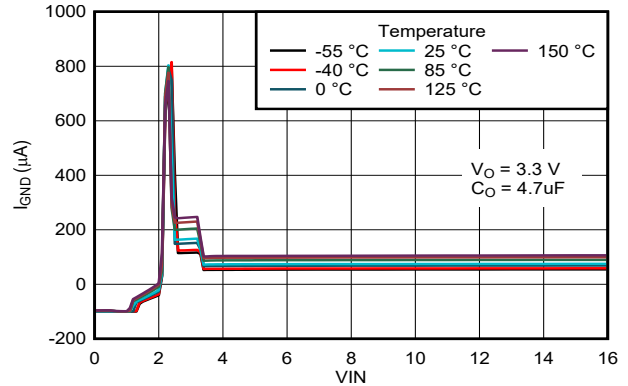


Figure 6-28. Input Current vs V_{IN} for New Chip

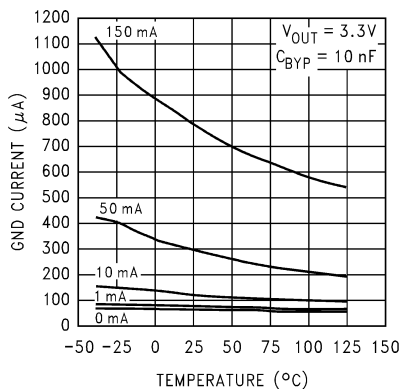


Figure 6-29. GND Pin Current vs Temperature for Legacy Chip

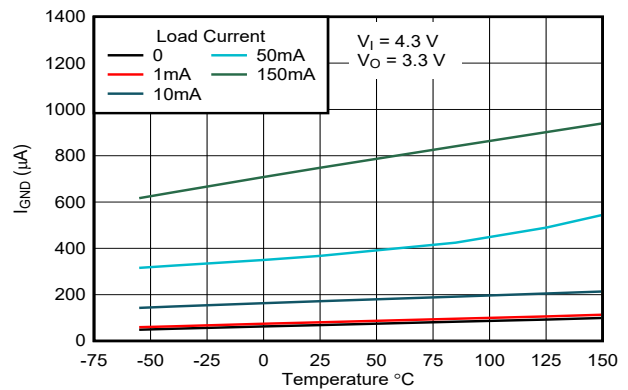


Figure 6-30. GND Pin Current vs Temperature for New Chip

6.6 Typical Characteristics (continued)

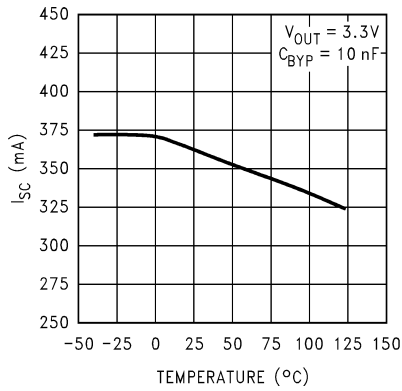


Figure 6-31. Instantaneous Short-Circuit Current for Legacy Chip

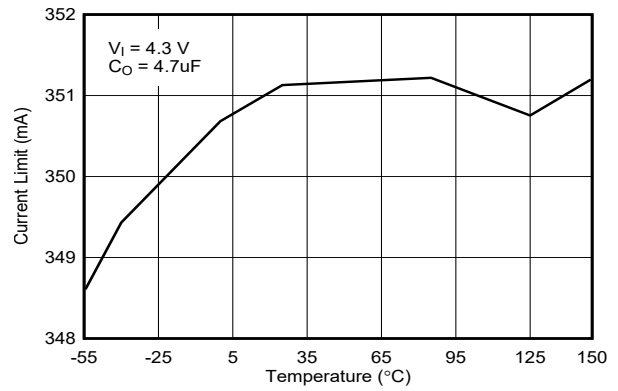


Figure 6-32. Short-Circuit Current vs Temperature for New Chip

7 Detailed Description

7.1 Overview

The LP2985-N is a fixed-output, low-noise, high PSRR, low-dropout regulator that offers exceptional, cost-effective performance for both portable and nonportable applications. The LP2985-N has an output tolerance of 1% across line, load, and temperature variation (for the new chip) and is capable of delivering 150 mA of continuous load current.

This device features integrated overcurrent protection, thermal shutdown, output enable, and internal output pulldown and has a built-in soft-start mechanism for controlled inrush current. This device delivers excellent line and load transient performance. The operating ambient temperature range of the device is from -40°C to $+125^{\circ}\text{C}$.

7.2 Functional Block Diagrams

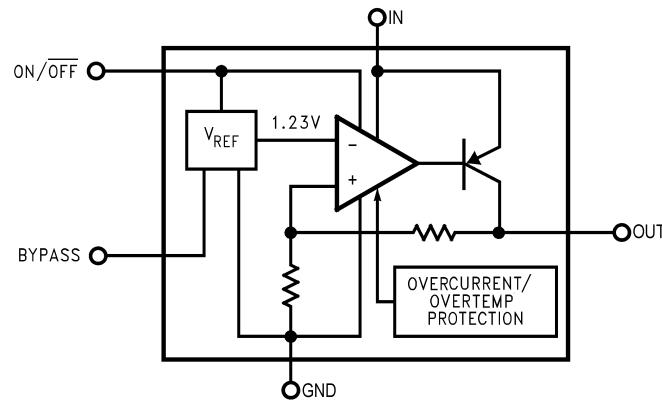


Figure 7-1. Block Diagram for Legacy Chip

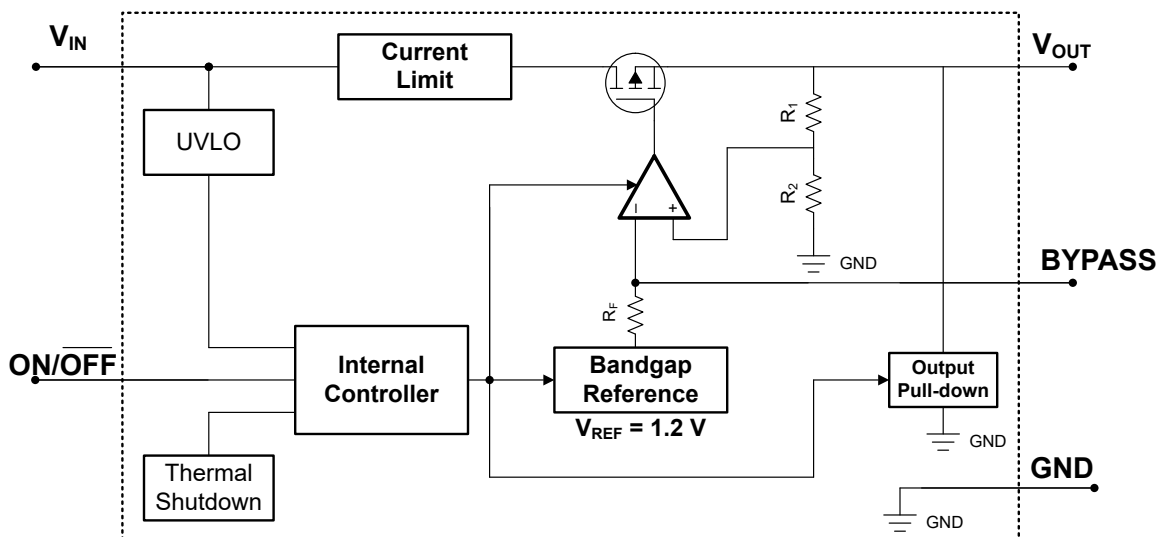


Figure 7-2. Block Diagram for New Chip

7.3 Feature Description

7.3.1 Output Enable

The ON/ $\overline{\text{OFF}}$ pin for the device is an active-high pin. The output voltage is enabled when the voltage of the ON/ $\overline{\text{OFF}}$ pin is greater than the high-level input voltage of the ON/ $\overline{\text{OFF}}$ pin and disabled with the ON/ $\overline{\text{OFF}}$ pin voltage is less than the low-level input voltage of the ON/ $\overline{\text{OFF}}$ pin. If independent control of the output voltage is not needed, connect the ON/ $\overline{\text{OFF}}$ pin to the input of the device.

The device has an internal pulldown circuit that activates when the device is disabled by pulling the ON/ $\overline{\text{OFF}}$ pin voltage lower than the low-level input voltage of the ON/ $\overline{\text{OFF}}$ pin to actively discharge the output voltage.

7.3.2 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{\text{IN}} - V_{\text{OUT}}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the [Recommended Operating Conditions](#) table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{\text{DS(ON)}}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{\text{DS(ON)}}$ of the device.

$$R_{\text{DS(ON)}} = \frac{V_{\text{DO}}}{I_{\text{RATED}}} \quad (1)$$

7.3.3 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the [Electrical Characteristics](#) table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power $[(V_{\text{IN}} - V_{\text{OUT}}) \times I_{\text{CL}}]$. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the [Know Your Limits application note](#).

Figure 7-3 shows a diagram of the current limit.

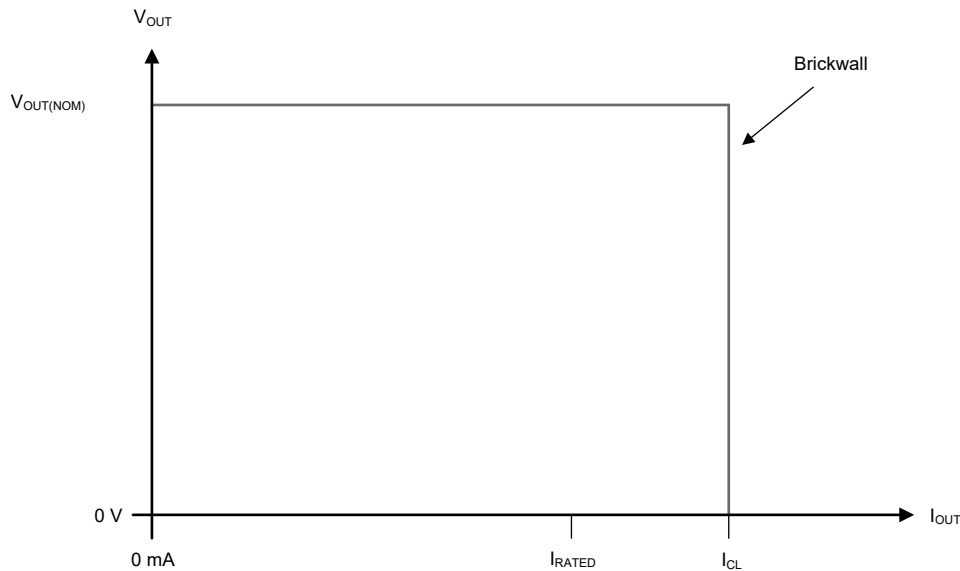


Figure 7-3. Current Limit

7.3.4 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the [Electrical Characteristics](#) table.

7.3.5 Output Pulldown

The new chip has an output pulldown circuit. The output pulldown activates in the following conditions:

- When the device is disabled ($V_{ON/OFF} < V_{ON/OFF(LOW)}$)
- If $1.0\text{ V} < V_{IN} < V_{UVLO}$

Do not rely on the output pulldown circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can flow from the output to the input. This reverse current flow can cause damage to the device. See the [Reverse Current](#) section for more details.

7.3.6 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device can cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start up can be high from large $V_{IN} - V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start up completes.

For reliable operation, limit the junction temperature to the maximum listed in the [Recommended Operating Conditions](#) table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

7.4 Device Functional Modes

7.4.1 Device Functional Mode Comparison

Table 7-1 shows the conditions that lead to the different modes of operation. See the [Electrical Characteristics](#) table for parameter values.

Table 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	$V_{ON/OFF}$	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{ON/OFF} > V_{ON/OFF(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{ON/OFF} > V_{ON/OFF(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{ON/OFF} < V_{ON/OFF(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The ON/OFF voltage has previously exceeded the ON/OFF rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

7.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the ON/OFF pin to less than the maximum ON/OFF pin low-level input voltage (see the [Electrical Characteristics](#) table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LP2985-N is a linear voltage regulator operating from 2.5 V to 16 V on the input and regulates voltages between 1.2 V to 5 V (for the new chip) with 1% accuracy across line, load and temperature (for the new chip) and 150-mA maximum output current. The LP2985-N low output noise of 30 μV_{RMS} (with 10-nF bypass capacitors) and wide bandwidth PSRR performance of greater than 70 dB at 1 kHz and 40 dB at 1 MHz help attenuate the switching frequency of an upstream DC/DC converter and minimize post regulator filtering.

8.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors listed in the [Recommended Operating Conditions](#) table account for an effective capacitance of approximately 50% of the nominal value.

8.1.2 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5 Ω . A higher value capacitor can be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor within the range specified in the [Recommended Operating Conditions](#) table for stability.

8.1.3 Noise Bypass Capacitor (C_{BYPASS})

The LP2985-N allows for low-noise performance with the use of a bypass capacitor that is connected to the internal band-gap reference with the BYPASS pin. This high-impedance band-gap circuitry is biased in the microampere range and, thus, cannot be loaded significantly, otherwise, the output (and, correspondingly, the output of the regulator) changes. Thus, for best output accuracy, dc leakage current through C_{BYPASS} must be minimized as much as possible and must never exceed 100 nA. The C_{BYPASS} capacitor also impacts the start-up behavior of the regulator. Inrush current and start-up time increase with larger bypass capacitor values.

Use a 10-nF capacitor for C_{BYPASS} . Ceramic and film capacitors are good choices for this purpose.

8.1.4 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3 \text{ V}$.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

Figure 8-1 shows one approach for protecting the device.

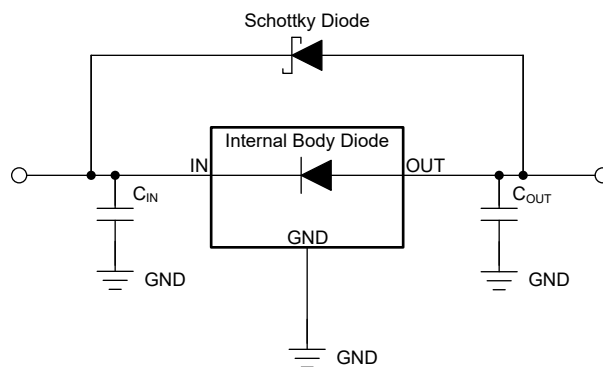


Figure 8-1. Example Circuit for Reverse Current Protection Using a Schottky Diode

8.1.5 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

Note

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (3)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the [Thermal Information](#) table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

8.1.6 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The [Thermal Information](#) table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (4)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

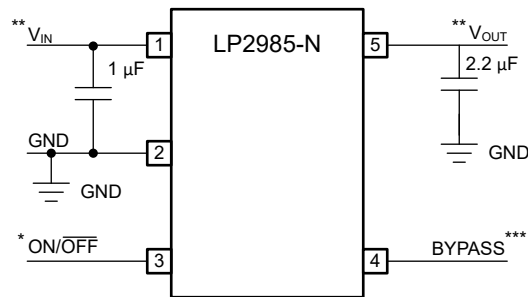
$$T_J = T_B + \psi_{JB} \times P_D \quad (5)$$

where:

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the [Semiconductor and IC Package Thermal Metrics application note](#).

8.2 Typical Application



*The ON/OFF input must be actively terminated. Tie to V_{IN} if this function is not used. **Minimum capacitance is shown to ensure stability (can be increased without limit). Ceramic capacitor required for output (see the [Input and Output Capacitor Requirements](#) section). ***Reduces output noise (can be omitted if application is not noise critical). Use ceramic or film type with very low leakage current (see the [Noise Bypass Capacitor \(\$C_{BYPASS}\$ \)](#) section).

Figure 8-2. Typical Application Schematic

8.2.1 Design Requirements

Table 8-1 lists the typical design parameters.

Table 8-1. Design Parameters for the New Chip

DESIGN PARAMETERS	VALUE
Input voltage	4.3 V, $\pm 10\%$ provided by the DC/DC converter switching at 1 MHz
Output voltage	3.3 V, $\pm 1\%$
Output current	0 mA–150 mA (maximum)
RMS noise, 300 Hz to 50 kHz	$< 30 \mu V_{RMS}$
PSRR at 100 kHz	> 40 dB

8.2.2 Detailed Design Procedure

8.2.2.1 Capacitor Characteristics

The LP2985-N was designed to work with ceramic capacitors on the output to take advantage of the benefits these capacitors offer. For capacitance values in the 2.2- μF to 4.7- μF range, ceramics are the least expensive and also have the lowest ESR values (which makes these components the most efficient at eliminating high-frequency noise). The ESR of a typical 2.2- μF ceramic capacitor is in the range of 10 m Ω to 20 m Ω , which easily meets the ESR limits required for stability by the LP2985-N.

One disadvantage of ceramic capacitors is that the capacitance can vary with temperature. Most large-value ceramic capacitors ($\geq 2.2 \mu F$) are manufactured with the Z5U or Y5V temperature characteristic, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

This capacitance drop can cause problems if a 2.2- μF capacitor is used on the output because that capacitor can drop to approximately 1 μF at high ambient temperatures (which can cause the LM2985 to oscillate). If Z5U or Y5V capacitors are used on the output, a minimum capacitance value of 2.2 μF must be observed.

A better choice for temperature coefficient in ceramic capacitors is X7R, which holds the capacitance within $\pm 15\%$. Unfortunately, the larger values of capacitance are not offered by all manufacturers in the X7R dielectric.

Tantalum capacitors are less desirable than ceramics for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1- μF to 4.7- μF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. Which means that although a tantalum capacitor can possibly have an ESR value within the stable range, the capacitor must be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value.

The ESR of a typical tantalum increases by approximately 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed.

8.2.2.2 ON/OFF Input Operation

The LP2985-N is shut off by driving the ON/OFF input low, and turned on by pulling the ON/OFF input high. If this feature is not used, the ON/OFF input must be tied to V_{IN} to keep the regulator output on at all times.

To provide proper operation, the signal source used to drive the ON/OFF input must be able to swing above and below the specified turn-on/turn-off voltage thresholds listed in the *Electrical Characteristics* section under $V_{ON/OFF}$. For the legacy chip, to prevent misoperation, the turn-on (and turn-off) voltage signals applied to the ON/OFF input must have a slew rate that is ≥ 40 mV/ μ s. But for the new chip, there is no restriction on the slew rate of the voltage signals applied to the ON/OFF pin.

8.2.3 Application Curves

at operating temperature $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 1.0$ V or 2.5 V (whichever is greater), $I_{OUT} = 1$ mA, ON/OFF pin tied to V_{IN} , $C_{IN} = 1.0$ μ F, and $C_{OUT} = 4.7$ μ F (unless otherwise noted)

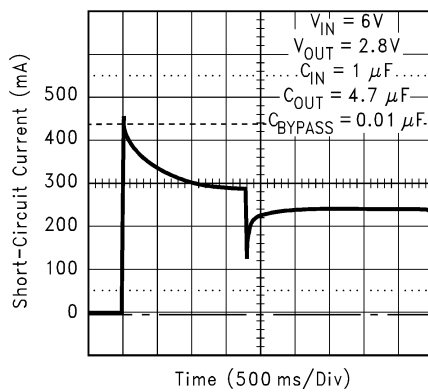


Figure 8-3. Short-Circuit Current for Legacy Chip at $V_{IN} = 6$ V

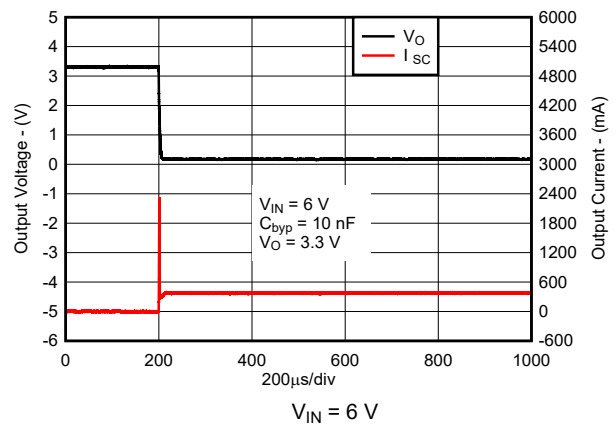


Figure 8-4. Short-Circuit Current for New Chip at $V_{IN} = 6$ V

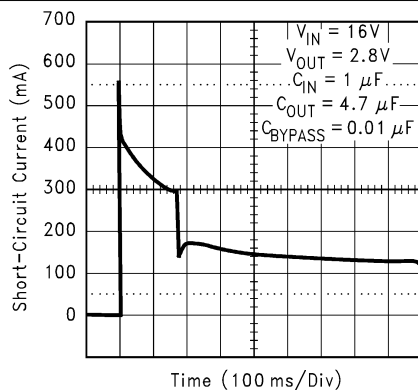


Figure 8-5. Short-Circuit Current for Legacy Chip at $V_{IN} = 16$ V

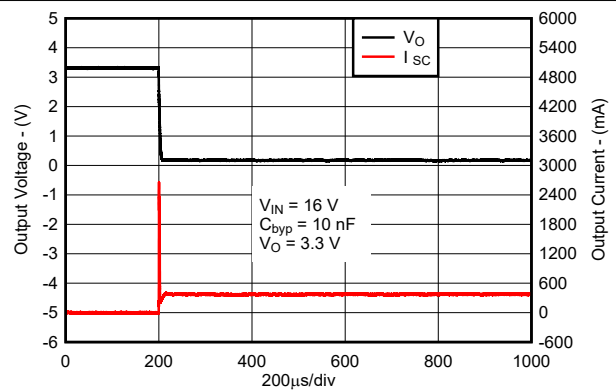


Figure 8-6. Short-Circuit Current for New Chip at $V_{IN} = 16$ V

8.2.3 Application Curves (continued)

at operating temperature $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 1.0\text{ V}$ or 2.5 V (whichever is greater), $I_{OUT} = 1\text{ mA}$, ON/OFF pin tied to V_{IN} , $C_{IN} = 1.0\text{ }\mu\text{F}$, and $C_{OUT} = 4.7\text{ }\mu\text{F}$ (unless otherwise noted)

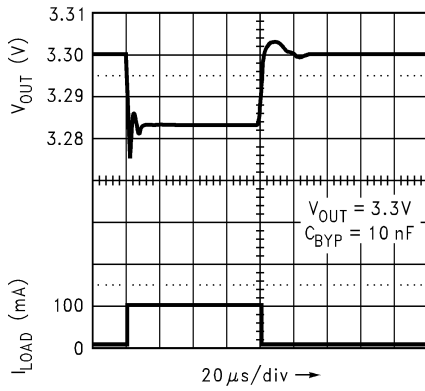


Figure 8-7. Load Transient Response for Legacy Chip

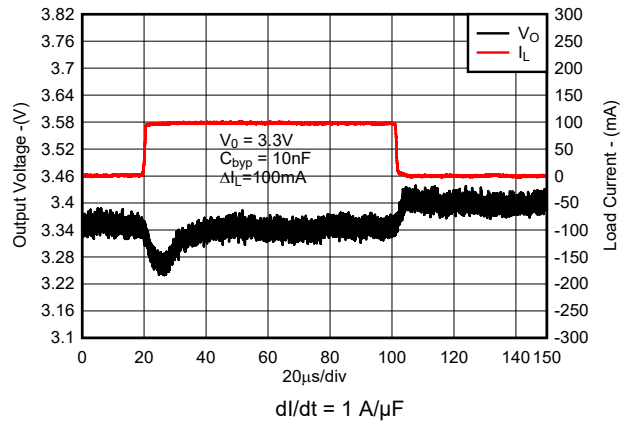


Figure 8-8. Load Transient Response for New Chip

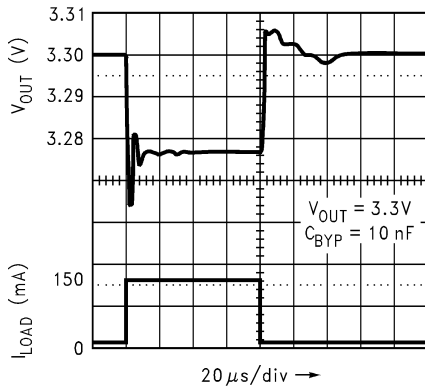


Figure 8-9. Load Transient Response for Legacy Chip

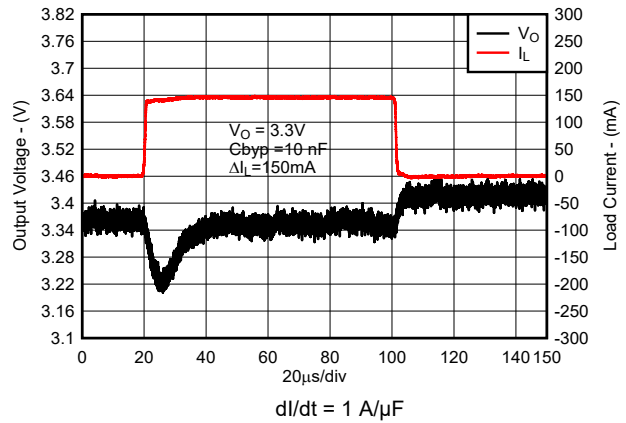


Figure 8-10. Load Transient for New Chip

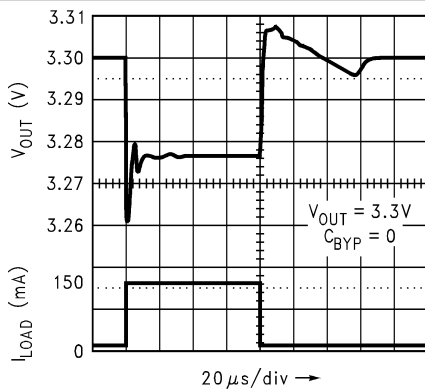


Figure 8-11. Load Transient Response for Legacy Chip

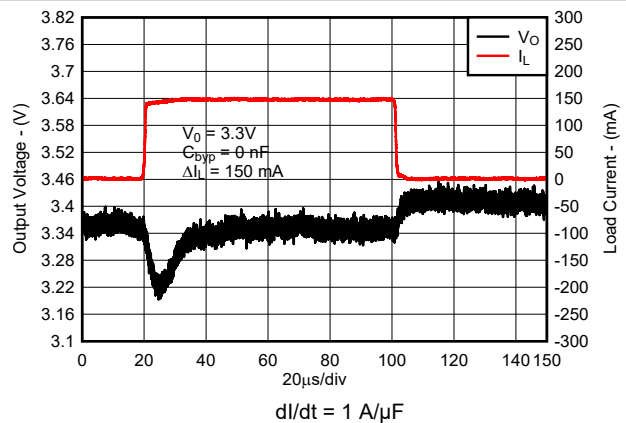


Figure 8-12. Load Transient Response for New Chip

8.2.3 Application Curves (continued)

at operating temperature $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 1.0\text{ V}$ or 2.5 V (whichever is greater), $I_{OUT} = 1\text{ mA}$, ON/OFF pin tied to V_{IN} , $C_{IN} = 1.0\text{ }\mu\text{F}$, and $C_{OUT} = 4.7\text{ }\mu\text{F}$ (unless otherwise noted)

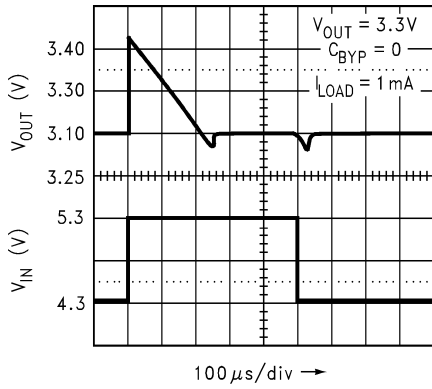


Figure 8-13. Line Transient Response for Legacy Chip

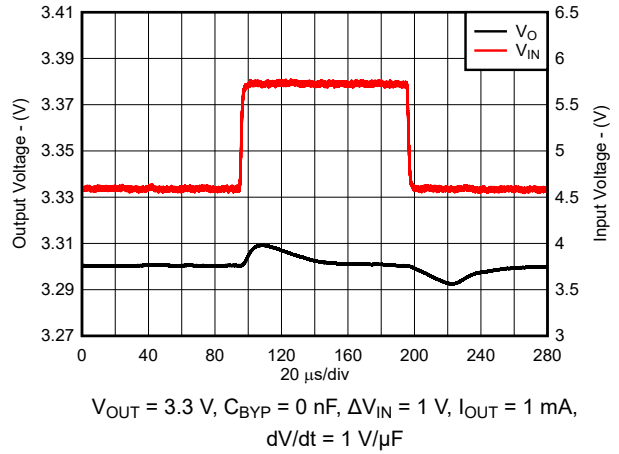


Figure 8-14. Line Transient Response for New Chip

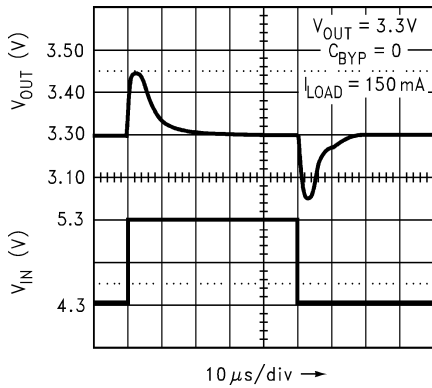


Figure 8-15. Line Transient Response for Legacy Chip

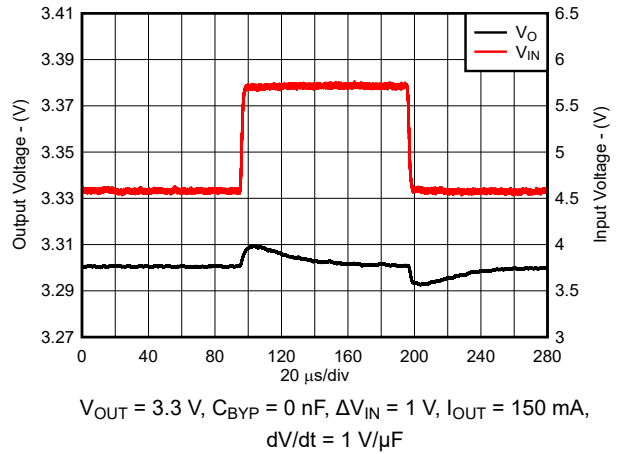


Figure 8-16. Line Transient Response for New Chip

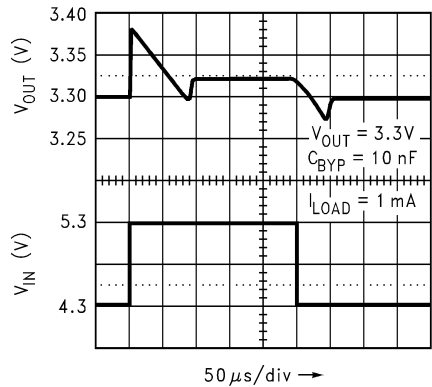


Figure 8-17. Line Transient Response for Legacy Chip

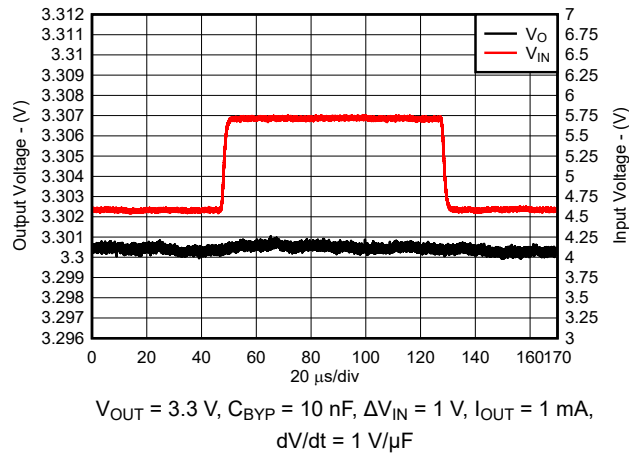


Figure 8-18. Line Transient Response for New Chip

8.2.3 Application Curves (continued)

at operating temperature $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 1.0\text{ V}$ or 2.5 V (whichever is greater), $I_{OUT} = 1\text{ mA}$, ON/OFF pin tied to V_{IN} , $C_{IN} = 1.0\text{ }\mu\text{F}$, and $C_{OUT} = 4.7\text{ }\mu\text{F}$ (unless otherwise noted)

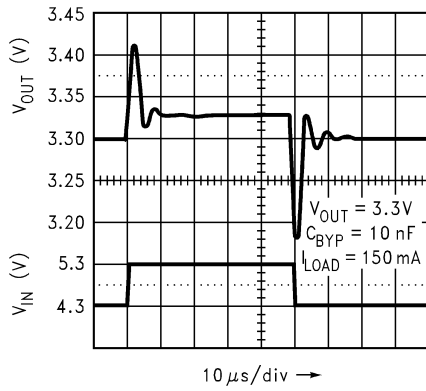


Figure 8-19. Line Transient Response for Legacy Chip

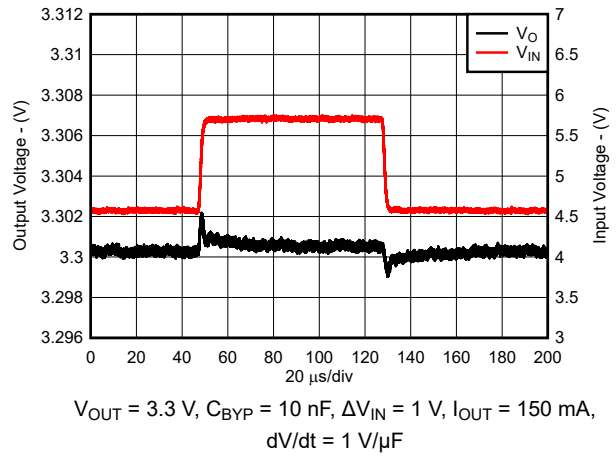


Figure 8-20. Line Transient Response for New Chip

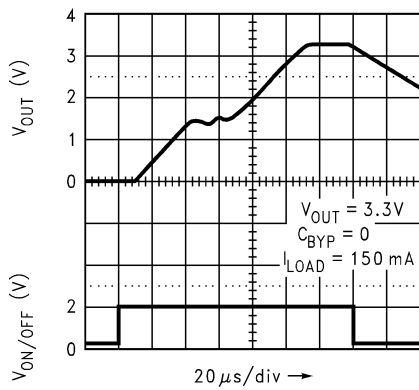


Figure 8-21. Turn-On Time for Legacy Chip

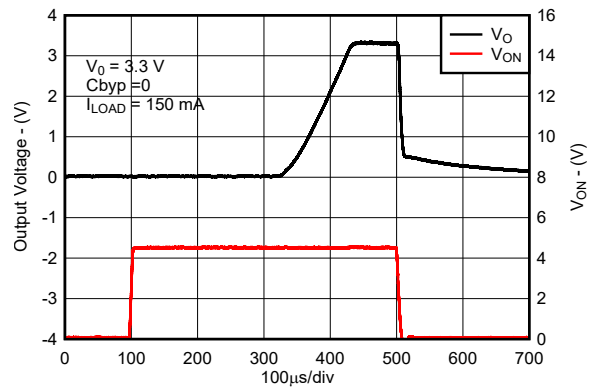


Figure 8-22. Turn-On Time for New Chip

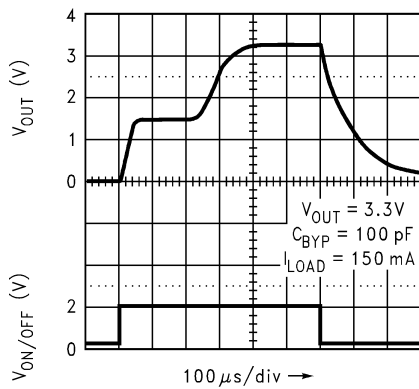


Figure 8-23. Turn-On Time for Legacy Chip

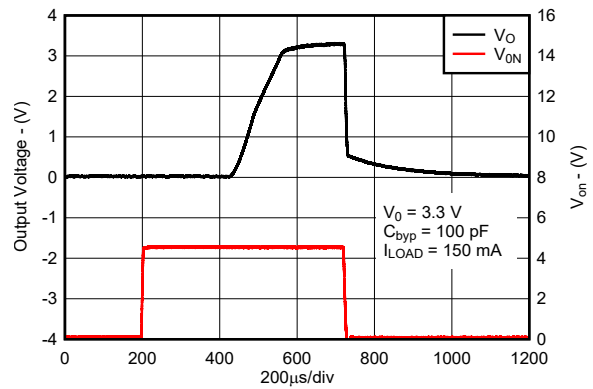


Figure 8-24. Turn-On Time for New Chip

8.2.3 Application Curves (continued)

at operating temperature $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 1.0\text{ V}$ or 2.5 V (whichever is greater), $I_{OUT} = 1\text{ mA}$, ON/OFF pin tied to V_{IN} , $C_{IN} = 1.0\text{ }\mu\text{F}$, and $C_{OUT} = 4.7\text{ }\mu\text{F}$ (unless otherwise noted)

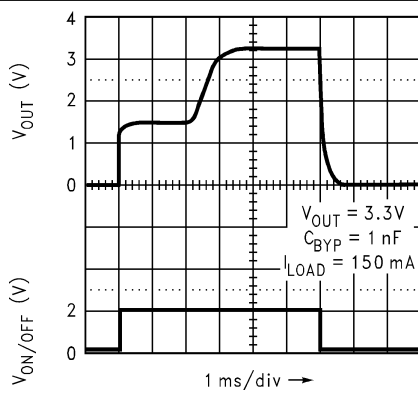


Figure 8-25. Turn-On Time for Legacy Chip

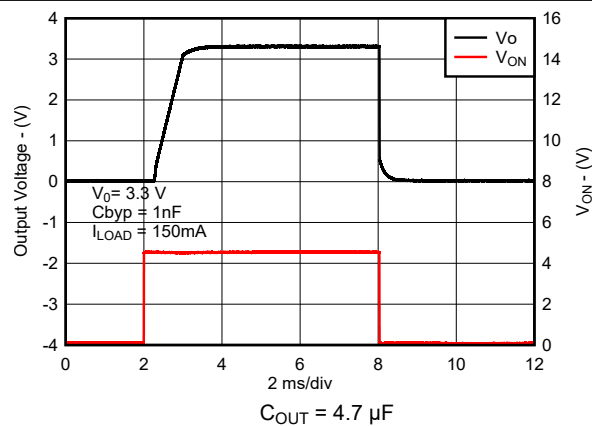


Figure 8-26. Turn-On Time for New Chip

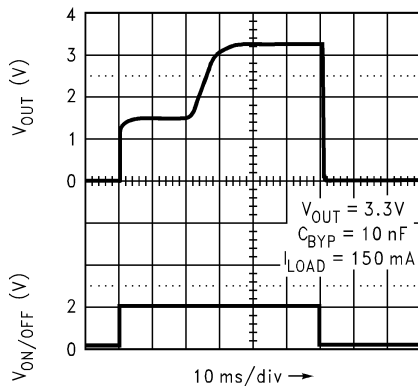


Figure 8-27. Turn-On Time for Legacy Chip

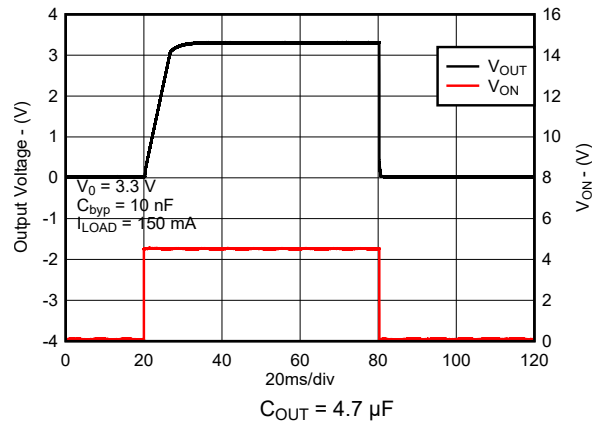


Figure 8-28. Turn-On Time for New Chip

8.3 Power Supply Recommendations

A power supply can be used at the input voltage within the ranges given in the [Recommended Operating Conditions](#) table. Use bypass capacitors as described in the [Layout Guidelines](#) section.

8.4 Layout

8.4.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close as possible to each other, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

A ground reference plane is also recommended and is either embedded in the PCB or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device. In most applications, this ground plane is necessary to meet thermal requirements.

8.4.2 Layout Example

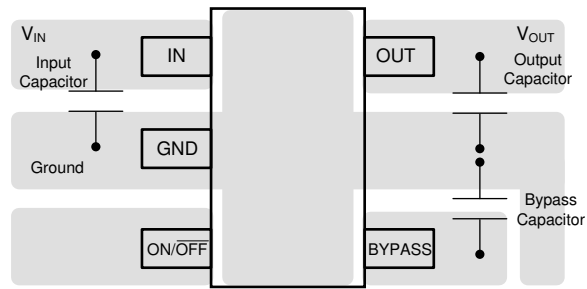


Figure 8-29. LP2985 SOT-23 Package Typical Layout

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

- Texas Instruments, [Semiconductor and IC Package Thermal Metrics application note](#)
- Texas Instruments, [Using New Thermal Metrics application note](#)
- Texas Instruments, [Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs application note](#)

9.2 Device Nomenclature

Table 9-1. Available Options⁽¹⁾

PRODUCT	V _{OUT}
LP2985cxxxz-y.y/NOPB Legacy chip	xxx is the package designator. z is the package quantity. X is for large quantity reel and non-X is for small quantity reel. y.y is the nominal output voltage (for example, 3.3 = 3.3 V; 5.0 = 5.0 V). c is the accuracy specification, A for higher accuracy and non-A for standard grade.
LP2985Axxxz-y.y/M3 New chip	xxx is the package designator. z is the package quantity. X is for large quantity reel and non-X is for small quantity reel. y.y is the nominal output voltage (for example, 3.3 = 3.3 V; 5.0 = 5.0 V). M3 is a suffix designator for newer chip redesigns, fabricated on the latest TI process technology.

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.5 Trademarks

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All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2985AIM5-2.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LAUA	Samples
LP2985AIM5-2.7/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LALA	Samples
LP2985AIM5-2.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L0KA	Samples
LP2985AIM5-2.9/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LAXA	Samples
LP2985AIM5-3.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	L0OA	Samples
LP2985AIM5-3.1/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L0PA	Samples
LP2985AIM5-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L0RA	Samples
LP2985AIM5-3.6/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	L0SA	Samples
LP2985AIM5-3.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	L0YA	Samples
LP2985AIM5-4.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L0TA	Samples
LP2985AIM5-4.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LA7A	Samples
LP2985AIM5-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L0UA	Samples
LP2985AIM5-5.7/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM		LKTA	Samples
LP2985AIM5-6.1/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LF6A	Samples
LP2985AIM5X-2.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LAUA	Samples
LP2985AIM5X-2.6/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LCEA	Samples
LP2985AIM5X-2.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	L0KA	Samples
LP2985AIM5X-2.9/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LAXA	Samples
LP2985AIM5X-3.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	L0OA	Samples
LP2985AIM5X-3.1/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L0PA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2985AIM5X-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L0RA	Samples
LP2985AIM5X-3.6/M3	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L0SA	Samples
LP2985AIM5X-3.6/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	L0SA	Samples
LP2985AIM5X-3.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L0YA	Samples
LP2985AIM5X-4.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	L0TA	Samples
LP2985AIM5X-4.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LA7A	Samples
LP2985AIM5X-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L0UA	Samples
LP2985AIM5X-6.1/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LF6A	Samples
LP2985IM5-2.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LAUB	Samples
LP2985IM5-2.7/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM		LALB	Samples
LP2985IM5-2.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	L0KB	Samples
LP2985IM5-2.9/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LAXB	Samples
LP2985IM5-3.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	L0OB	Samples
LP2985IM5-3.1/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L0PB	Samples
LP2985IM5-3.2/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L0QB	Samples
LP2985IM5-3.3/NOM3	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L0RB	Samples
LP2985IM5-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	L0RB	Samples
LP2985IM5-3.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LAIB	Samples
LP2985IM5-3.6/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(L0SB, L0YB)	Samples
LP2985IM5-3.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	L0YB	Samples
LP2985IM5-4.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	L0TB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2985IM5-4.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM		LA7B	Samples
LP2985IM5-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	L0UB	Samples
LP2985IM5-5.7/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM		LKTB	Samples
LP2985IM5-6.1/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM		LF6B	Samples
LP2985IM5X-2.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LAUB	Samples
LP2985IM5X-2.7/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM		LALB	Samples
LP2985IM5X-2.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	L0KB	Samples
LP2985IM5X-3.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	L0OB	Samples
LP2985IM5X-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	L0RB	Samples
LP2985IM5X-3.6/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L0SB	Samples
LP2985IM5X-4.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	L0TB	Samples
LP2985IM5X-4.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM		LA7B	Samples
LP2985IM5X-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	L0UB	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



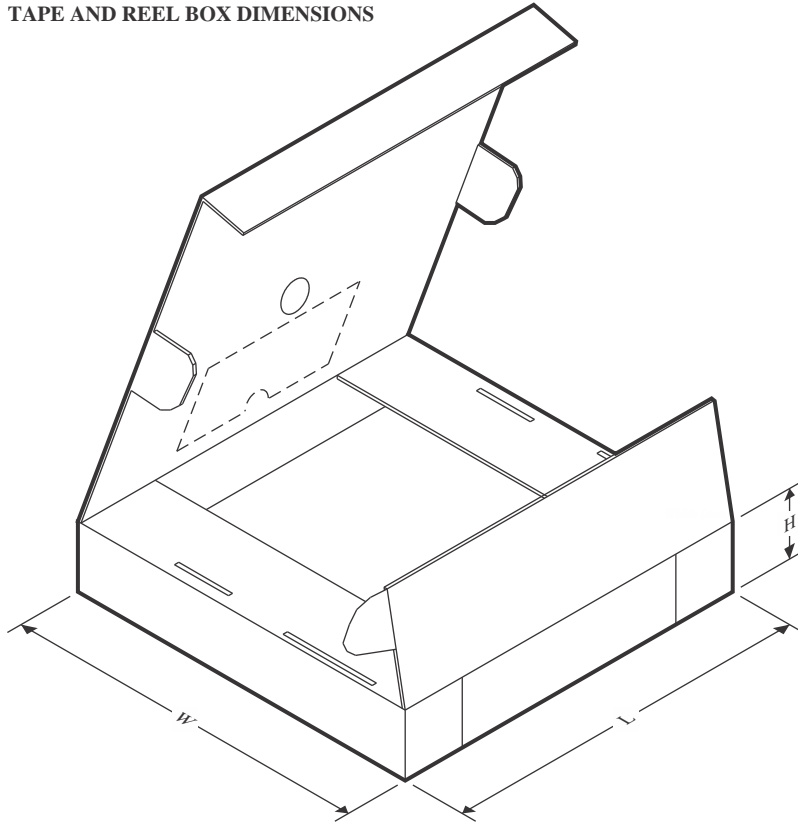
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2985AIM5-2.5/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-2.7/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-2.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-2.9/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-3.0/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-3.1/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-3.6/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-3.8/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-4.0/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-4.5/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-5.0/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-5.7/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-6.1/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-2.5/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-2.6/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-2.8/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2985AIM5X-2.9/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-3.1/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-3.6/M3	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-3.6/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-3.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-4.0/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-4.5/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-6.1/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-2.5/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-2.7/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-2.8/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-2.9/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.0/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.1/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.2/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.3/NOM3	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.5/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.6/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.8/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-4.0/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-4.5/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-5.7/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-6.1/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-2.7/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-2.8/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-3.0/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-3.3/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-3.6/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-4.5/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-5.0/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2985AIM5-2.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5-2.7/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2985AIM5-2.8/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2985AIM5-2.9/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2985AIM5-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5-3.1/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2985AIM5-3.6/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5-3.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5-4.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5-4.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5-5.7/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2985AIM5-6.1/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2985AIM5X-2.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-2.6/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985AIM5X-2.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-2.9/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985AIM5X-3.1/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2985AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-3.6/M3	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-3.6/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-3.8/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985AIM5X-4.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-4.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-6.1/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985IM5-2.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5-2.7/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2985IM5-2.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5-2.9/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2985IM5-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5-3.1/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2985IM5-3.2/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2985IM5-3.3/NOM3	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5-3.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5-3.6/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5-3.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5-4.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5-4.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5-5.7/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2985IM5-6.1/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2985IM5X-2.7/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985IM5X-2.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5X-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5X-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5X-3.6/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985IM5X-4.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5X-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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