THE DATASHEET OF

LP2985AITPX-2.8

LP2985-N Micropower 150-mA Low-Noise Ultra-Low-Dropout Regulator in a SOT-23 Package Designed for Use With Very Low ESR Output Capacitors

1 Features

- Input Voltage Range: 2.5 V to 16 V
- Ultra Low-Dropout Voltage
- Ensured 150 mA Output Current
- Requires Minimum External Components
- Stable With Low-ESR Output Capacitor
- < 1 µA Quiescent Current When Shut Down
- Low Ground Pin Current at All Loads
- Output Voltage Accuracy 1% (A Grade)
- High Peak Current Capability
- Low Z_{OUT}: 0.3 Ω Typical (10 Hz to 1 MHz)
- Overtemperature and Overcurrent Protection
- −40°C to 125°C Junction Temperature Range
- Custom Voltages Available

2 Applications

- Cellular Phones
- Palmtop and Laptop Computers
- Personal Digital Assistants (PDA)
- Camcorders, Personal Stereos, Cameras

3 Description

The LP2985-N low noise linear (LDO) regulator delivers up to 150-mA output current and only requires 300-mV dropout voltage of input to output. Using an optimized vertically integrated PNP (VIP) process, the LP2985-N delivers unequaled performance for all battery-powered designs. The LP2985-N device provides 1% tolerance precision output voltage with only 75-µA quiescent current at 1-mA load and 850 µA at 150-mA load. By adding a 10-nF bypass capacitor, the output noise can be reduced to 30 μV_{RMS} in a 30-kHz bandwidth.

The LP2985-N is designed to work with a ceramic output capacitor with equivalent series resistance (ESR) as low as 5 mΩ. The device is available with fixed output voltage from 2.5 V to 6.1 V. Contact Texas Instrument Sales for specific voltage option needs.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP2985-N	SOT-23 (5)	2.90 mm x 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

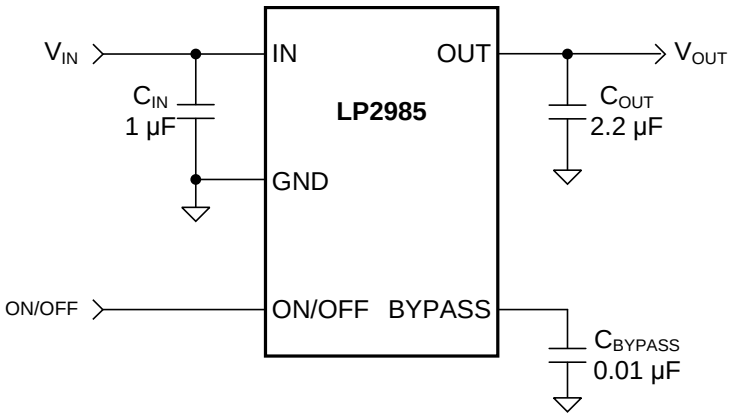


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision X (May 2015) to Revision Y — **Page**

- Added top nav icon for TI Designs ... 1
- Deleted "Smallest Possible Size (SOT-23 Package)" from *Features* ... 1
- Deleted all information re: DSBGA package - it is no longer available ... 1
- Deleted DSBGA pin function info from *Pin Functions* ... 3
- Deleted infor re: DSBGA package; changed "...value of $R_{\theta JA}$ for the SOT-23 package is 175.7°C/W ..." to "...value of $R_{\theta JA}$ for the SOT-23 package is 169.0°C/W..." in footnote 3 to *Abs Max* table - see update thermal info for SOT-23 in *Thermal Information* ... 4
- Changed "All pins except 3 and 4 (SOT-23)" to "Pins 3 and 4 ." ... 4
- Changed thermal values for SOT-23 package; added Note 2 to *Thermal Information* table ... 5
- Deleted footnote 1 to *Electrical Characteristics* ... 5
- Changed content in last 2 paragraphs of *Reverse Input-Output Voltage* ... 17
- Added *Power Dissipation* and *Estimating Junction Temperature* subsections ... 18

Changes from Revision W (September 2014) to Revision X — **Page**

- Changed pin names in text and app circuit drawing "VOUT" and "VIN" to "OUT" and "IN"; replace *Handling Ratings* with *ESD Ratings*; update *Thermal Values* ... 1
- Changed footnote 1 to *Ab Max* table per new format ... 4
- Changed location of storage temperature range from *Handling Ratings* to *Ab Max* table ... 4
- Added required *Application Information* section ... 14

Changes from Revision V (April 2013) to Revision W — **Page**

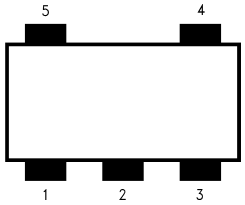
- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* ... 1

Changes from Revision U (April 2013) to Revision V **Page**

- Changed layout of National Semiconductor data sheet 22

5 Pin Configuration and Functions

DBV Package
5 Pin SOT-23
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
BYPASS	4	I/O	Bypass capacitor for low noise operation
GND	2	—	Common ground (device substrate)
IN	1	I	Input voltage
ON/OFF	3	I	Logic high enable input
OUT	5	O	Regulated output voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Operating junction temperature	–40	125	°C
Power dissipation(3)	Internally Limited		
Input supply voltage (survival)	–0.3	16	V
Input supply voltage (operating)	2.5	16	V
Shutdown input voltage (survival)	–0.3	16	V
Output voltage (survival)(4)	–0.3	9	V
I_{OUT} (survival)	Short Circuit Protected		
Input-output voltage (survival)(5)	–0.3	16	V
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_{J_MAX}, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using:

$$P_{MAX} = \frac{T_{J\_MAX} - T_A}{R_{\theta JA}}$$

Where the value of $R_{\theta JA}$ for the SOT-23 package is 169.0°C/W in a typical PC board mounting.
Exceeding the maximum allowable dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.
(4) For 12-V option, output voltage survival: –0.3 to +16 V. If used in a dual-supply system where the regulator load is returned to a negative supply, the LP2985-N output must be diode-clamped to ground.
(5) The output PNP structure contains a diode between the IN to OUT pins that is normally reverse-biased. Reversing the polarity from IN to OUT will turn on this diode.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Pins 3 and 4	±1000	V
			Pins 1, 2, and 5	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Supply input voltage	3.1(1)	16	V
$V_{ON/OFF}$	ON/OFF input voltage	0	V_{IN}	V
I_{OUT}	Output current		150	mA
T_J	Operating junction temperature	–40	125	°C

(1) Recommended minimum V_{IN} is the greater of 3.1 V or $V_{OUT(MAX)}$ + rated dropout voltage (maximum) for operating load current.

6.4 Thermal Information

THERMAL METRIC[1]		LP2985-N DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance, High K[2]	169.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	121.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.0	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Thermal resistance value $R_{\theta JA}$ is based on the EIA/JEDEC High-K printed circuit board defined by JESD51-7 High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.

6.5 Electrical Characteristics

Unless otherwise specified: $V_{IN} = V_{O(NOM)} + 1$ V, $I_L = 1$ mA, $C_{IN} = 1$ µF, $C_{OUT} = 4.7$ µF, $V_{ON/OFF} = 2$ V, $T_J = 25°C$.

PARAMETER		TEST CONDITIONS	TYP	LP2985AI-X.X[1]		LP2985I-X.X[1]		UNIT
				MIN	MAX	MIN	MAX	
ΔV_O	Output voltage tolerance	I_L = 1 mA		−1	1	–1.5	1.5	$\%V_{NOM}$
		1 mA ≤ I_L ≤ 50 mA		−1.5	1.5	–2.5	2.5	
		1 mA ≤ I_L ≤ 50 mA, –40°C ≤ T_J ≤ 125°C		−2.5	2.5	–3.5	3.5	
		1 mA ≤ I_L ≤ 150 mA		−2.5	2.5	–3	3	
		1 mA ≤ I_L ≤ 150 mA, –40°C ≤ T_J ≤ 125°C		−3.5	3.5	–4	4	
$\Delta V_O/\Delta V_{IN}$	Output voltage	V_O(NOM)+1 V ≤ V_{IN} ≤ 16 V	0.007		0.014		0.014	%/V
	Line regulation	V_O(NOM)+1 V ≤ V_{IN} ≤ 16 V, –40°C ≤ T_J ≤ 125°C			0.032		0.032	
$V_{IN}–V_O$	Dropout voltage[2]	I_L = 0 mA	1		3		3	mV
		I_L = 0 mA, –40°C ≤ T_J ≤ 125°C			5		5	
		I_L = 1 mA	7		10		10	
		I_L = 1 mA, –40°C ≤ T_J ≤ 125°C			15		15	
		I_L = 10 mA	40		60		60	
		I_L = 10 mA, –40°C ≤ T_J ≤ 125°C			90		90	
		I_L = 50 mA	120		150		150	
		I_L = 50 mA, –40°C ≤ T_J ≤ 125°C			225		225	
		I_L = 150 mA	280		350		350	
		I_L = 150 mA, –40°C ≤ T_J ≤ 125°C			575		575	

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL).
(2) Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below the value measured with a 1-V differential.

Electrical Characteristics (continued)

Unless otherwise specified: $V_{IN} = V_{O(NOM)} + 1$ V, $I_L = 1$ mA, $C_{IN} = 1$ µF, $C_{OUT} = 4.7$ µF, $V_{ON/OFF} = 2$ V, $T_J = 25°C$.

PARAMETER		TEST CONDITIONS	TYP	LP2985AI-X.X(1)		LP2985I-X.X(1)		UNIT
				MIN	MAX	MIN	MAX	
I_{GND}	Ground pin current	$I_L = 0$ mA	65		95		95	µA
		$I_L = 0$ mA, –40°C ≤ T_J ≤ 125°C			125		125	
		$I_L = 1$ mA	75		110		110	
		$I_L = 1$ mA, –40°C ≤ T_J ≤ 125°C			170		170	
		$I_L = 10$ mA	120		220		220	
		$I_L = 10$ mA, –40°C ≤ T_J ≤ 125°C			400		400	
		$I_L = 50$ mA	350		600		600	
		$I_L = 50$ mA, –40°C ≤ T_J ≤ 125°C			1000		1000	
		$I_L = 150$ mA	850		1500		1500	
		$I_L = 150$ mA, –40°C ≤ T_J ≤ 125°C			2500		2500	
		$V_{ON/OFF} < 0.3$ V	0.01		0.8		0.8	
		$V_{ON/OFF} < 0.15$ V, –40°C ≤ T_J ≤ 125°C	0.05		2		2	
$V_{ON/OFF}$	ON/OFF input voltage(3)	High = O/P ON	1.4					V
		High = O/P ON, –40°C ≤ T_J ≤ 125°C		1.6		1.6		
		Low = O/P OFF	0.55					
		Low = O/P OFF, –40°C ≤ T_J ≤ 125°C			0.15		0.15	
$I_{ON/OFF}$	ON/OFF input current	$V_{ON/OFF} = 0$ V	0.01					µA
		$V_{ON/OFF} = 0$ V, –40°C ≤ T_J ≤ 125°C			−2		−2	
		$V_{ON/OFF} = 5$ V	5					
		$V_{ON/OFF} = 5$ V, –40°C ≤ T_J ≤ 125°C			15		15	
e_n	Output noise voltage (RMS)	BW = 300 Hz to 50 kHz,						µV
		$C_{OUT} = 10$ µF	30					
		$C_{BYPASS} = 10$ nF						
$\Delta V_O/\Delta V_{IN}$	Ripple rejection	f = 1 kHz, $C_{BYPASS} = 10$ nF	45					dB
		$C_{OUT} = 10$ µF						
$I_O(SC)$	Short circuit current	$R_L = 0$ Ω (steady state)(4)	400					mA
$I_O(PK)$	Peak output current	$V_{OUT} \geq V_{O(NOM)}$ –5%	350					mA

(3) The ON/OFF input must be properly driven to prevent possible misoperation. For details, refer to *ON/OFF Input Operation*.
(4) The LP2985-N has foldback current limiting which allows a high peak current when $V_{OUT} > 0.5$ V, and then reduces the maximum output current as V_{OUT} is forced to ground (see *Typical Characteristics* curves).

6.6 Typical Characteristics

Unless otherwise specified: C_{IN} = 1 µF, C_{OUT} = 4.7 µF, V_{IN} = $V_{OUT(NOM)}$ + 1, T_A = 25°C, ON/$\overline{OFF}$ pin is tied to V_{IN}.

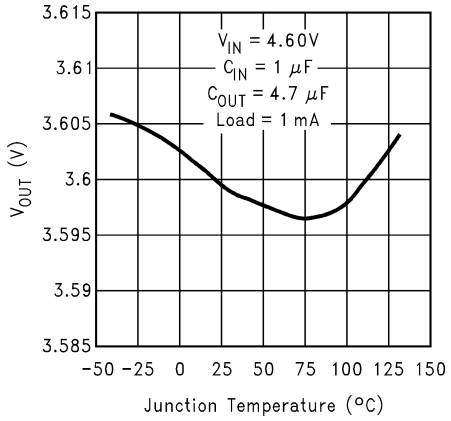


Figure 1. V_{OUT} vs Temperature

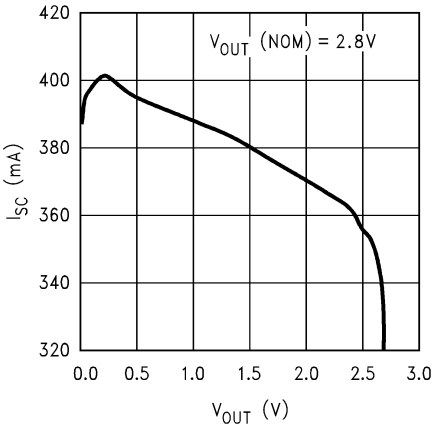


Figure 2. Short Circuit Current vs Output Voltage

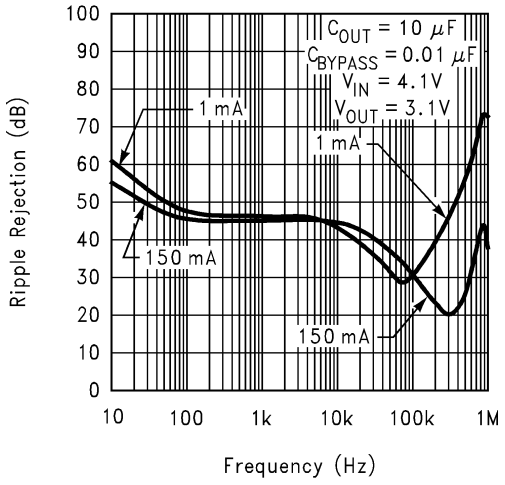


Figure 3. Ripple Rejection

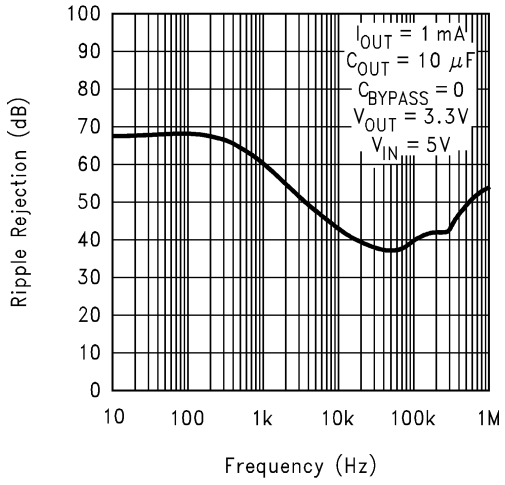


Figure 4. Ripple Rejection

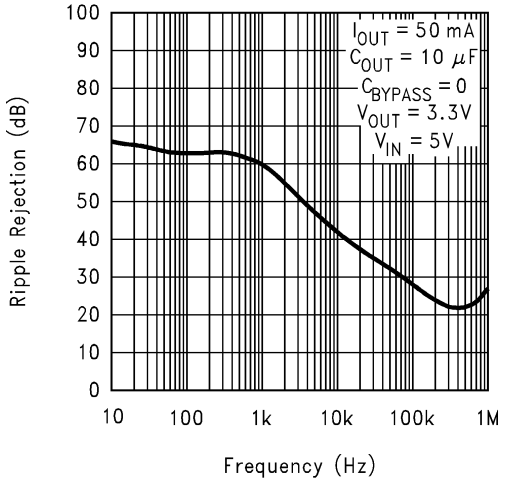


Figure 5. Ripple Rejection

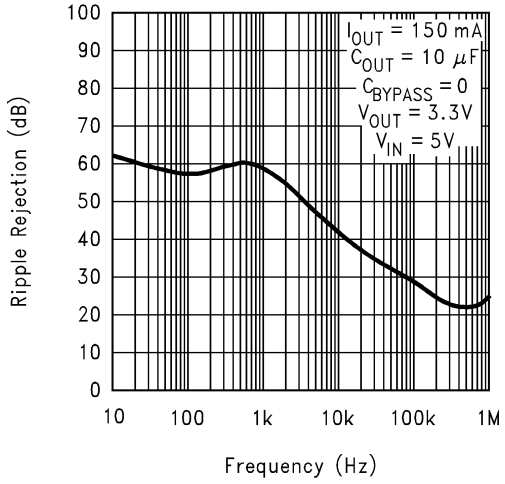


Figure 6. Ripple Rejection

Typical Characteristics (continued)

Unless otherwise specified: C_{IN} = 1 µF, C_{OUT} = 4.7 µF, V_{IN} = $V_{OUT(NOM)}$ + 1, T_A = 25°C, ON/$\overline{OFF}$ pin is tied to V_{IN}.

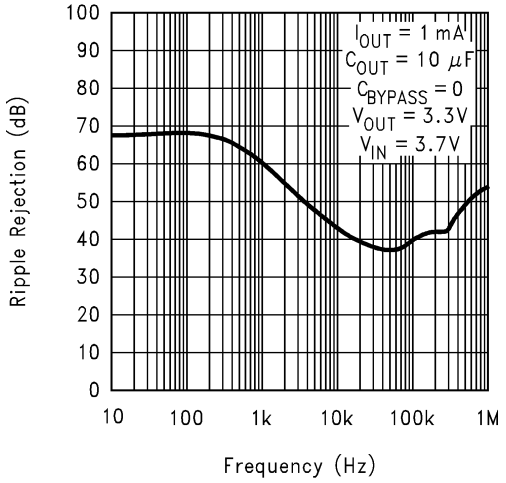


Figure 7. Ripple Rejection

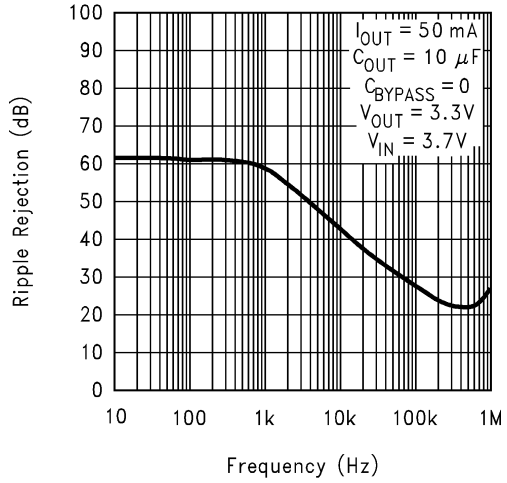


Figure 8. Ripple Rejection

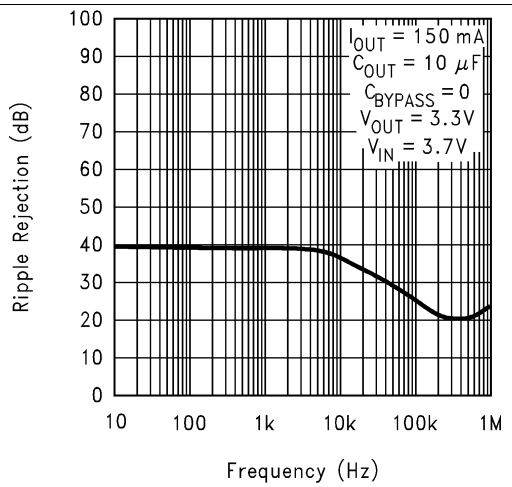


Figure 9. Ripple Rejection

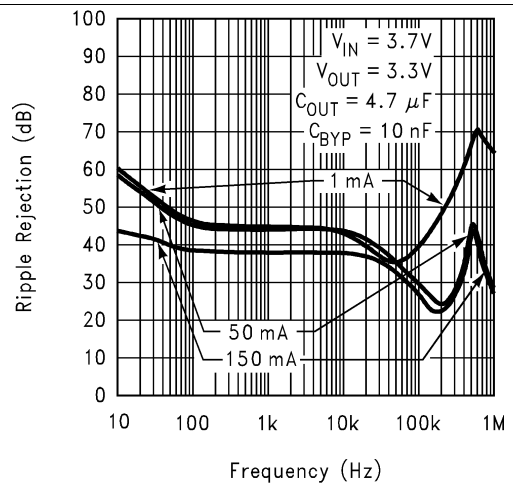


Figure 10. Ripple Rejection

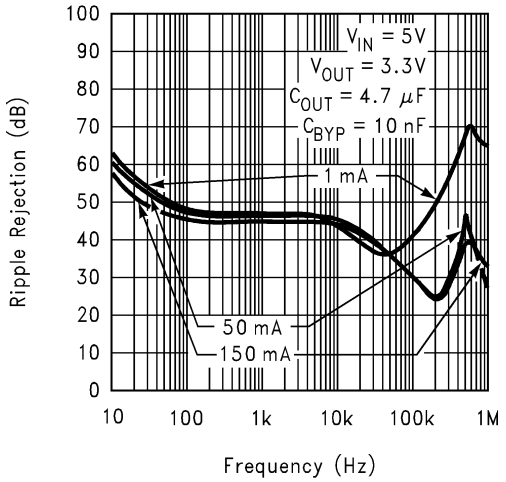


Figure 11. Ripple Rejection

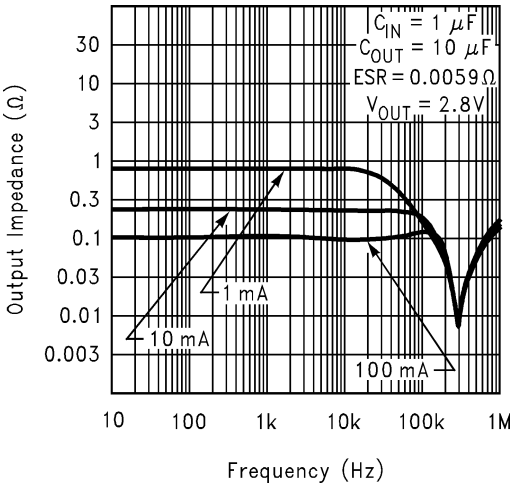


Figure 12. Output Impedance vs Frequency

Typical Characteristics (continued)

Unless otherwise specified: C_{IN} = 1 µF, C_{OUT} = 4.7 µF, V_{IN} = $V_{OUT(NOM)}$ + 1, T_A = 25°C, ON/$\overline{OFF}$ pin is tied to V_{IN}.

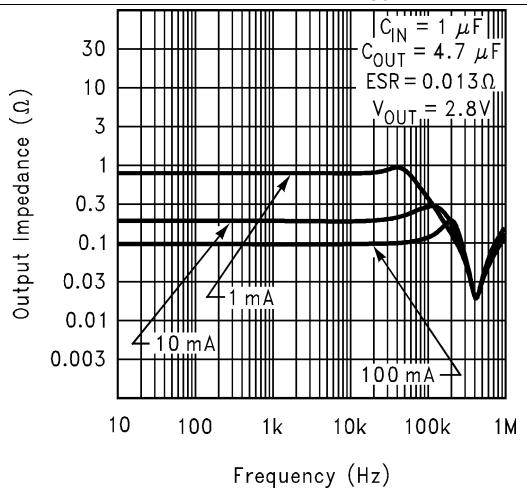


Figure 13. Output Impedance vs Frequency

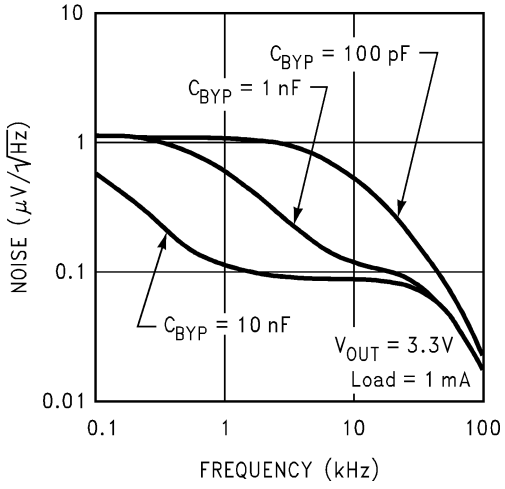


Figure 14. Output Noise Density

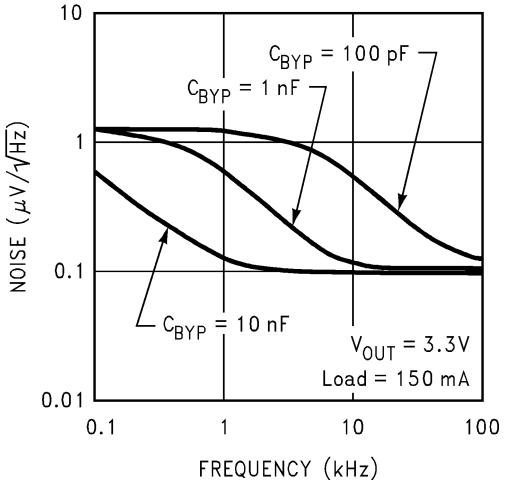


Figure 15. Output Noise Density

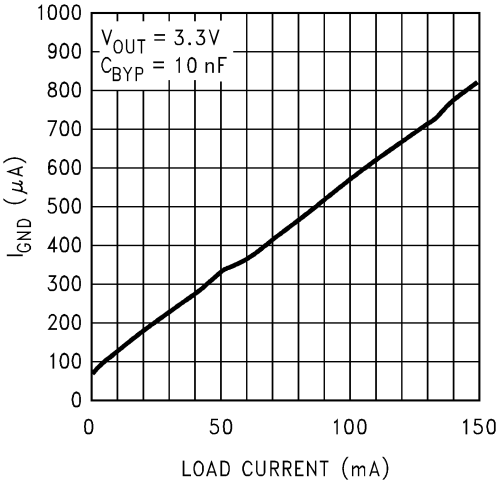


Figure 16. Ground Pin vs Load Current

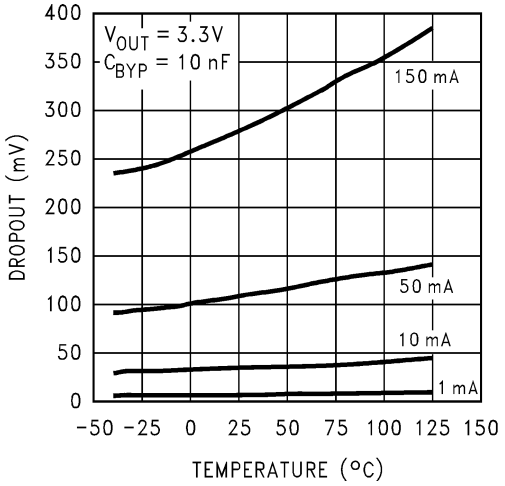


Figure 17. Dropout Voltage vs Temperature

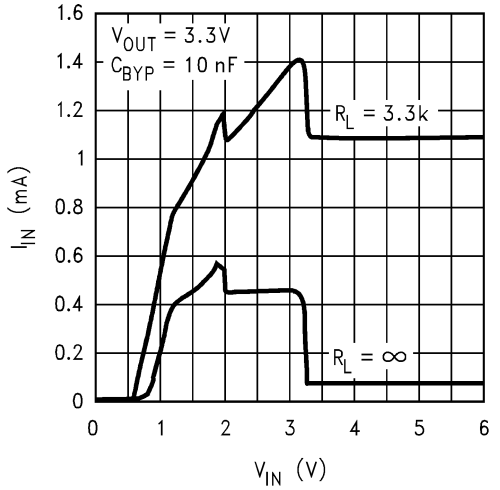


Figure 18. Input Current vs Pin

Typical Characteristics (continued)

Unless otherwise specified: C_{IN} = 1 µF, C_{OUT} = 4.7 µF, V_{IN} = $V_{OUT(NOM)}$ + 1, T_A = 25°C, ON/$\overline{OFF}$ pin is tied to V_{IN}.

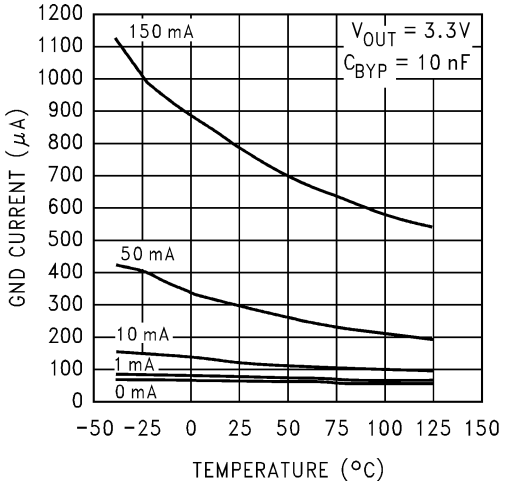


Figure 19. GND Pin Current vs Temperature

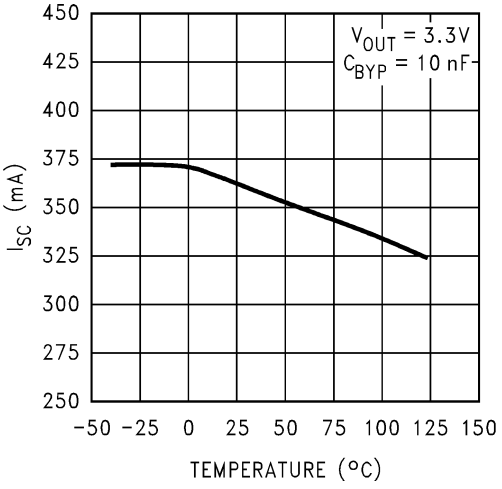


Figure 20. Instantaneous Short Circuit Current

7 Detailed Description

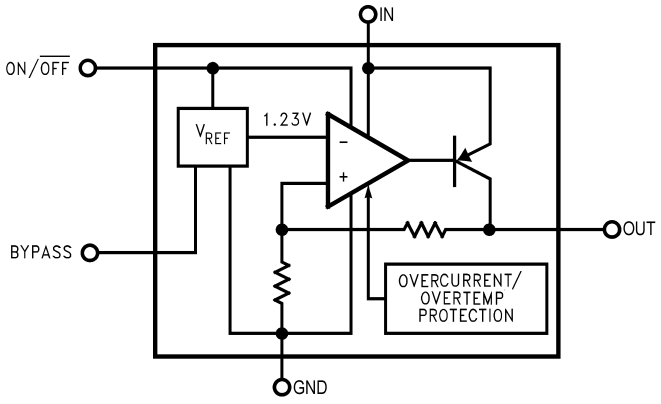
7.1 Overview

The LP2985-N family of fixed-output, ultra-low-dropout and low-noise regulators offers exceptional, cost-effective performance for battery-powered applications. Available in output voltages from 2.5 V to 5 V, the family has an output tolerance of 1% for the A version (1.5% for the non-A version) and is capable of delivering 150-mA continuous load current. Standard regulator features, such as overcurrent and overtemperature protection, are also included.

Using an optimized vertically integrated PNP (VIP) process, the LP2985-N contains several features to facilitate battery powered designs:

- Multiple voltage options
- Low dropout voltage, typical dropout of 300 mV at 150-mA load current and 7 mV at 1-mA load.
- Low quiescent current and low ground current, typically 850-µA at 150 mA load, and 75-µA at 1-mA load.
- A shutdown feature is available, allowing the regulator to consume only 0.01-µA typically when the ON/$\overline{\text{OFF}}$ pin is pulled low.
- Overtemperature protection and overcurrent protection circuitry is designed to safeguard the device during unexpected conditions
- Enhanced stability: The LP2985-N is stable with output capacitor ESR as low as 5 mΩ, which allows the use of ceramic capacitors on the output.
- Low noise: A BYPASS pin allows for low-noise operation, with a typical output noise of 30 μV_{RMS}, with the use of a 10-nF bypass capacitor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Multiple Voltage Options

In order to meet different application's requirement, the LP2985-N family provide multiple fixed output options from 2.5 V to 6.1 V. Consult factory for custom voltages.

7.3.2 Output Voltage Accuracy

Output voltage accuracy specifies minimum and maximum output voltage error, relative to the expected nominal output voltage stated as a percent. This accuracy error includes the errors introduced by the internal reference and the load and line regulation across the full range of rated load and line operating conditions over temperature, unless otherwise specified by the *Electrical Characteristics*. Output voltage accuracy also accounts for all variations between manufacturing lots.

Feature Description (continued)

7.3.3 Ultra-Low-Dropout Voltage

Generally speaking, the dropout voltage often refers to the voltage difference between the input and output voltage ($V_{DO} = V_{IN} – V_{OUT}$), where the main current pass-FET is fully on in the ohmic region of operation and is characterized by the classic $R_{DS(ON)}$ of the FET. V_{DO} indirectly specifies a minimum input voltage above the nominal programmed output voltage at which the output voltage is expected to remain within its accuracy boundary. If the input falls below this V_{DO} limit ($V_{IN} < V_{OUT} + V_{DO}$), then the output voltage decreases in order to follow the input voltage.

7.3.4 Low Ground Current

LP2985-N uses a vertical PNP process which allows for quiescent currents that are considerably lower than those associated with traditional lateral PNP regulators, typically 850 μA at 150-mA load and 75 μA at 1-mA load.

7.3.5 Sleep Mode

When pull ON/OFF pin to low level, LP2985-N enters sleep mode, and less than 2-μA quiescent current is consumed. This function is designed for the application which needs a sleep mode to effectively enhance battery life cycle.

7.3.6 Internal Protection Circuitry

7.3.6.1 Short Circuit Protection (Current Limit)

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate in a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases. Note also that if a current limit occurs and the resulting output voltage is low, excessive power may be dissipated across the LDO, resulting in a thermal shutdown of the output.

A foldback feature limits the short-circuit current to protect the regulator from damage under all load conditions. If V_{OUT} is forced below 0 V before EN goes high and the load current required exceeds the foldback current limit, the device may not start up correctly.

7.3.6.2 Thermal Protection

The LP2985-N contains a thermal shutdown protection circuit to turn off the output current when excessive heat is dissipated in the LDO. The thermal time-constant of the semiconductor die is fairly short, and thus the output cycles on and off at a high rate when thermal shutdown is reached until the power dissipation is reduced.

The internal protection circuitry of the LP2985-N is designed to protect against thermal overload conditions. The circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown degrades its reliability.

7.3.7 Enhanced Stability

The LP2985-N is designed specifically to work with ceramic output capacitors, utilizing circuitry which allows the regulator to be stable across the entire range of output current with an output capacitor whose ESR is as low as 5 mΩ. For output capacitor requirement, please refer to *Output Capacitor*.

7.3.8 Low Noise

The LP2985-N includes a low-noise reference ensuring minimal noise during operation because the internal reference is normally the dominant term in noise analysis. Further noise reduction can be achieved by adding an external bypass bapacitor between the BYPASS pin and the GND pin.

7.4 Device Functional Modes

7.4.1 Operation with $V_{OUT(TARGET)}$ + 0.6 V ≥ V_{IN} > 16 V

The device operate if the input voltage is equal to, or exceeds $V_{OUT(TARGET)}$ + 0.6 V. At input voltages below the minimum V_{IN} requirement, the devices do not operate correctly and output voltage may not reach target value.

7.4.2 Operation With ON/$\overline{OFF}$ Control

If the voltage on the ON/$\overline{OFF}$ pin is less than 0.15 V, the device is disabled, and in this state shutdown current does not exceed 2 μA. Raising ON/$\overline{OFF}$ above 1.6 V initiates the start-up sequence of the device.

8 Application and Implementation

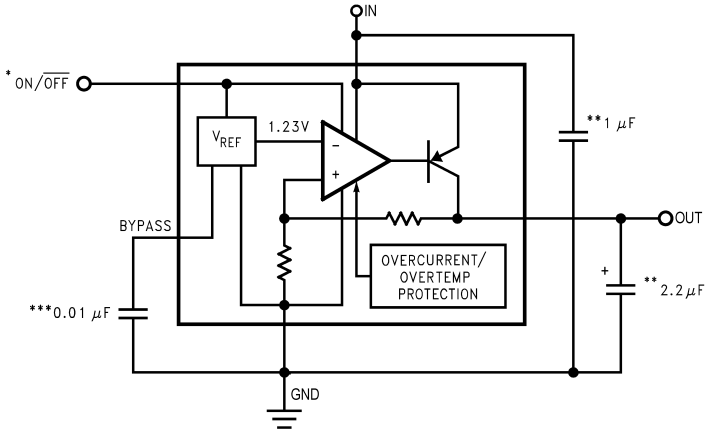
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP2985-N is a linear voltage regulator operating from 2.5 V to 16 V on the input and regulates voltages between 2.5 V to 6.1 V with 1% accuracy and 150-mA maximum output current. Efficiency is defined by the ratio of output voltage to input voltage because the LP2985-N is a linear voltage regulator. To achieve high efficiency, the dropout voltage (V_{IN} – V_{OUT}) must be as small as possible, thus requiring a very-low-dropout LDO. Successfully implementing an LDO in an application depends on the application requirements. If the requirements are simply input voltage and output voltage, compliance specifications (such as internal power dissipation or stability) must be verified to ensure a solid design. If timing, start-up, noise, power supply rejection ratio (PSRR), or any other transient specification is required, then the design becomes more challenging.

8.2 Typical Application



*ON/$\overline{OFF}$ input must be actively terminated. Tie to V_{IN} if this function is not to be used.
**Minimum capacitance is shown to ensure stability (may be increased without limit). Ceramic capacitor required for output (see *Output Capacitor*).
***Reduces output noise (may be omitted if application is not noise critical). Use ceramic or film type with very low leakage current (see *Noise Bypass Capacitor*).

Figure 21. Typical Application Schematic

8.2.1 Design Requirements

For typical design parameters, see Table 1.

Table 1. Design Parameters

DESIGN PARAMETERS	VALUE
Input voltage	4.3 V, ±10% provided by the DC-DC converter switching at 1 MHz
Output voltage	3.3 V, ±5%
Output current	150 mA (maximum), 1 mA (minimum)
RMS noise, 300 Hz to 50 kHz	< 50 μV_{RMS}
PSRR at 1 kHz	> 40 dB

8.2.2 Detailed Design Procedure

At 150-mA loading, the dropout of the LP2985-N has 575-mV maximum dropout over temperature, thus an 1000-mV headroom is sufficient for operation over both input and output voltage accuracy. The efficiency of the LP2985-N in this configuration is V_{OUT} / V_{IN} = 76.7%. To achieve the smallest form factor, the SOT-23 package is selected.

Input and output capacitors are selected in accordance with the *Capacitor Characteristics* section. Ceramic capacitances of 1 µF for the input and one 2.2-µF capacitor for the output are selected. With an efficiency of 76.7% and a 150-mA maximum load, the internal power dissipation is 150 mW, which corresponds to a 26°C junction temperature rise for the SOT-23 package. With an 85°C maximum ambient temperature, the junction temperature is at 111°C. To minimize noise, a bypass capacitance (C_{BYPASS}) of 0.01 µF is selected.

8.2.2.1 External Capacitors

Like any low-dropout regulator, the LP2985-N requires external capacitors for regulator stability. These capacitors must be correctly selected for good performance.

8.2.2.1.1 Input Capacitor

An input capacitor whose capacitance is ≥ 1 µF is required between the LP2985-N input and ground (the amount of capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

NOTE

Tantalum capacitors can suffer catastrophic failure due to surge current when connected to a low-impedance source of power (like a battery or very large capacitor). If a Tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will be ≥ 1 µF over the entire operating temperature range.

8.2.2.1.2 Output Capacitor

The LP2985-N is designed specifically to work with ceramic output capacitors, utilizing circuitry which allows the regulator to be stable across the entire range of output current with an output capacitor whose ESR is as low as 5 mΩ. It may also be possible to use tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost (see *Capacitor Characteristics*).

The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR value which is within the stable range. Curves are provided which show the stable ESR range as a function of load current (see Figure 22).

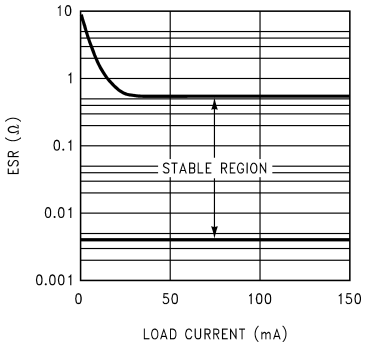


Figure 22. ESR Graph

NOTE

The output capacitor must maintain its ESR within the stable region over the full operating temperature range of the application to assure stability.

The LP2985-N requires a minimum of 2.2 µF on the output (output capacitor size can be increased without limit).

It is important to remember that capacitor tolerance and variation with temperature must be taken into consideration when selecting an output capacitor so that the minimum required amount of output capacitance is provided over the full operating temperature range. Ceramic capacitors can exhibit large changes in capacitance with temperature (see *Capacitor Characteristics*). The output capacitor must be located not more than 1 cm from the output pin and returned to a clean analog ground.

8.2.2.1.3 Noise Bypass Capacitor

Connecting a 10-nF capacitor to the BYPASS pin significantly reduces noise on the regulator output. The capacitor is connected directly to a high-impedance circuit in the bandgap reference.

Because this circuit has only a few microamperes flowing in it, any significant loading on this node will cause a change in the regulated output voltage. For this reason, DC leakage current through the noise bypass capacitor must never exceed 100 nA and must be kept as low as possible for best output voltage accuracy.

The types of capacitors best suited for the noise bypass capacitor are ceramic and film. High-quality ceramic capacitors with either NPO or COG dielectric typically have very low leakage. 10-nF polypropolene and polycarbonate film capacitors are available in small surface-mount packages and typically have extremely low leakage current.

8.2.2.2 Capacitor Characteristics

The LP2985-N was designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the 2.2-µF to 4.7-µF range, ceramics are the least expensive and also have the lowest ESR values (which makes them best for eliminating high-frequency noise). The ESR of a typical 2.2-µF ceramic capacitor is in the range of 10 mΩ to 20 mΩ, which easily meets the ESR limits required for stability by the LP2985-N.

One disadvantage of ceramic capacitors is that their capacitance can vary with temperature. Most large value ceramic capacitors (≥ 2.2 µF) are manufactured with the Z5U or Y5V temperature characteristic, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

This could cause problems if a 2.2-µF capacitor were used on the output because it will drop down to approximately 1 µF at high ambient temperatures (which could cause the LM2985 to oscillate). If Z5U or Y5V capacitors are used on the output, a minimum capacitance value of 4.7 µF must be observed.

A better choice for temperature coefficient in ceramic capacitors is X7R, which holds the capacitance within ±15%. Unfortunately, the larger values of capacitance are not offered by all manufacturers in the X7R dielectric.

Tantalum capacitors are less desirable than ceramics for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1 µF to 4.7 µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a Tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value.

Note that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

8.2.2.3 ON/$\overline{\text{OFF}}$ Input Operation

The LP2985-N is shut off by driving the ON/$\overline{\text{OFF}}$ input low, and turned on by pulling it high. If this feature is not to be used, the ON/$\overline{\text{OFF}}$ input must be tied to V_{IN} to keep the regulator output on at all times.

To assure proper operation, the signal source used to drive the ON/$\overline{\text{OFF}}$ input must be able to swing above and below the specified turn-on/turn-off voltage thresholds listed in the *Electrical Characteristics* section under $V_{ON/OFF}$. To prevent mis-operation, the turn-on (and turn-off) voltage signals applied to the ON/OFF input must have a slew rate which is ≥ 40 mV/µs.

CAUTION

The regulator output voltage cannot be ensured if a slow-moving AC (or DC) signal is applied that is in the range between the specified turn-on and turn-off voltages listed under the electrical specification $V_{ON/OFF}$ (see *Electrical Characteristics*).

8.2.2.4 Reverse Input-Output Voltage

The PNP power transistor used as the pass element in the LP2985-N has an inherent diode connected between the regulator output and input. During normal operation (where the input voltage is higher than the output) this diode is reverse-biased).

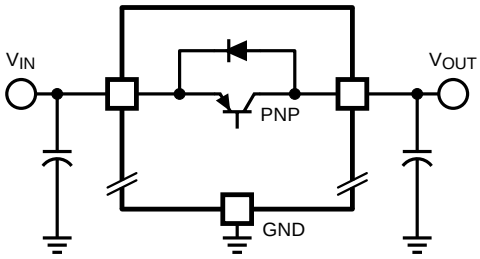


Figure 23. Reverse Current Path

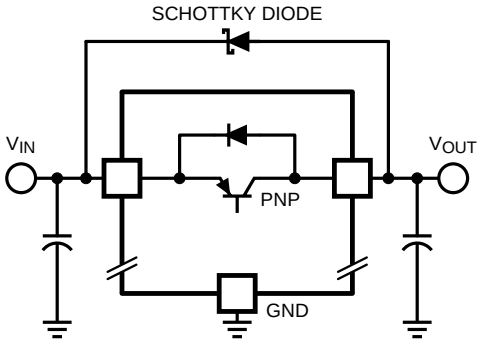


Figure 24. Reverse Current Protection

However, if the output voltage is higher than the input voltage, this diode turns ON, and current flows into the regulator OUT pin. In such cases, a parasitic SCR can latch, allowing a high current to flow into the IN pin and out the ground (GND) pin, which can damage the device.

In any application where the voltage at the OUT pin may possibly be higher than the voltage at the IN pin, an external Schottky diode must be connected from V_{IN} to V_{OUT} (cathode on V_{IN}, anode on V_{OUT}), to limit the reverse voltage across the LP2985-N to 0.3 V (see *Absolute Maximum Ratings*).

8.2.2.5 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane connected to the tab or pad is critical to ensuring reliable operation. Device power dissipation depends on input voltage, output voltage, and load conditions and can be calculated with Equation 1.

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT(MAX)} \quad (1)$$

Power dissipation can be minimized, and greater efficiency can be achieved, by using the lowest available voltage drop option that would still be greater than the dropout voltage (V_{DO}). However, keep in mind that higher voltage drops result in better dynamic (that is, PSRR and transient) performance.

On the SOT-23 (DBV) package, the primary conduction path for heat is through the device leads to the PCB, predominately device lead 2 (GND). TI recommends that the trace from lead 2 be extended under the package body and connected to an internal ground plane with thermal vias.

The maximum allowable junction temperature ($T_{J(MAX)}$) determines maximum power dissipation allowed ($P_{D(MAX)}$) for the device package.

Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A), according to Equation 2 or Equation 3:

$$T_{J(MAX)} = T_{A(MAX)} + (R_{\theta JA} \times P_{D(MAX)}) \quad (2)$$

$$P_{D(MAX)} = (T_{J(MAX)} - T_{A(MAX)}) / R_{\theta JA} \quad (3)$$

Unfortunately, this $R_{\theta JA}$ is highly dependent on the heat-spreading capability of the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in *Thermal Information* is determined by the specific EIA/JEDEC JESD51-7 standard for PCB and copper-spreading area, and is to be used only as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper area acting as a heat sink.

8.2.2.6 Estimating Junction Temperature

The EIA/JEDEC standard recommends the use of psi (Ψ) thermal characteristics to estimate the junction temperatures of surface mount devices on a typical PCB board application. These characteristics are not true thermal resistance values, but rather package specific thermal characteristics that offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of copper-spreading area. The key thermal characteristics (Ψ_{JT} and Ψ_{JB}) are given in *Thermal Information* and are used in accordance with Equation 4 or Equation 5.

$$T_{J(MAX)} = T_{TOP} + (\Psi_{JT} \times P_{D(MAX)})$$

where

- $P_{D(MAX)}$ is explained in Equation 1.
- T_{TOP} is the temperature measured at the center-top of the device package. (4)

$$T_{J(MAX)} = T_{BOARD} + (\Psi_{JB} \times P_{D(MAX)})$$

where

- $P_{D(MAX)}$ is explained in Equation 1.
- T_{BOARD} is the PCB surface temperature measured 1-mm from the device package and centered on the package edge. (5)

For more information about the thermal characteristics Ψ_{JT} and Ψ_{JB}, see *Semiconductor and IC Package Thermal Metrics*, available for download at www.ti.com.

For more information about measuring T_{TOP} and T_{BOARD}, see *Using New Thermal Metrics*; and for more information about the EIA/JEDEC JESD51 PCB used for validating $R_{\theta JA}$, see *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs*. These application notes are available at www.ti.com.com.

8.2.3 Application Curves

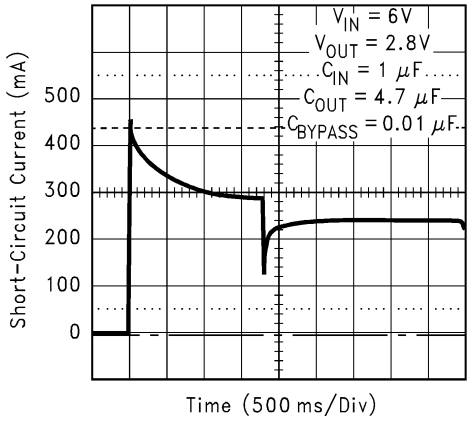


Figure 25. Short-Circuit Current

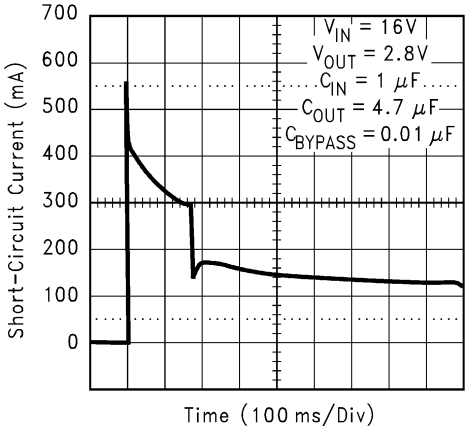


Figure 26. Short-Circuit Current

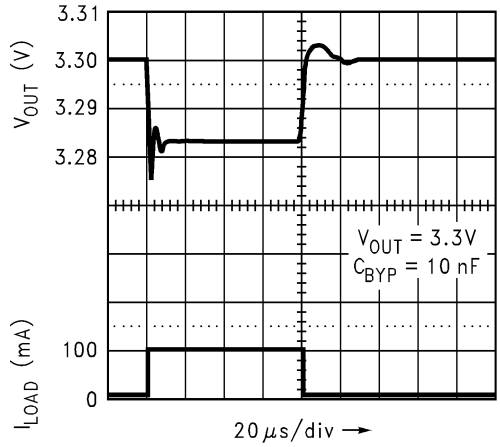


Figure 27. Load Transient Response

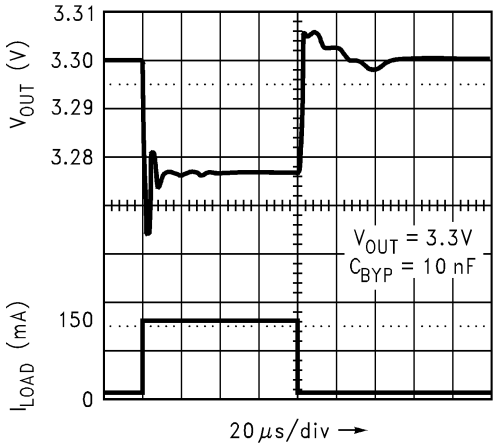


Figure 28. Load Transient Response

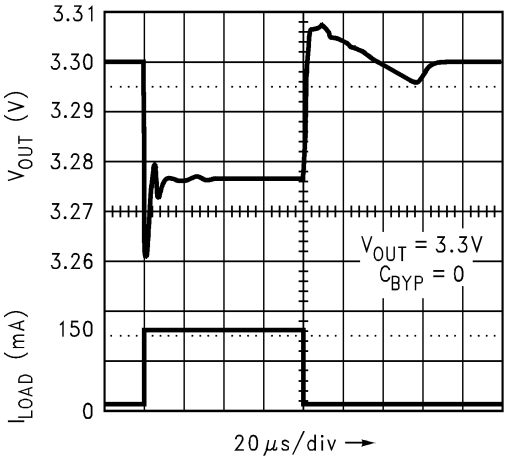


Figure 29. Load Transient Response

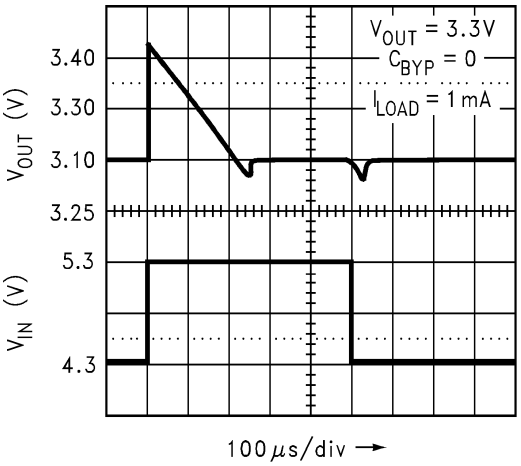


Figure 30. Line Transient Response

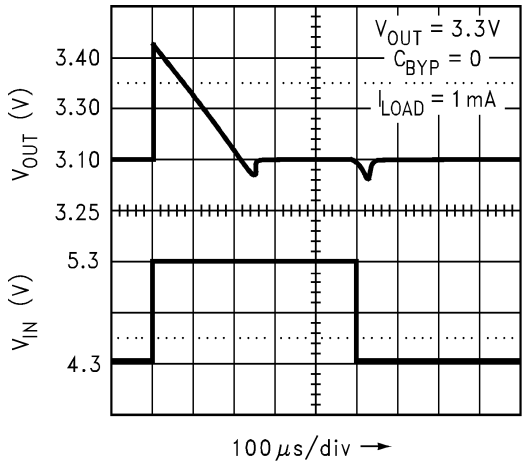


Figure 31. Line Transient Response

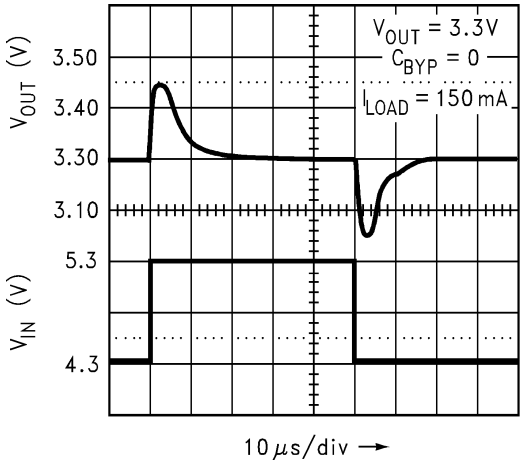


Figure 32. Line Transient Response

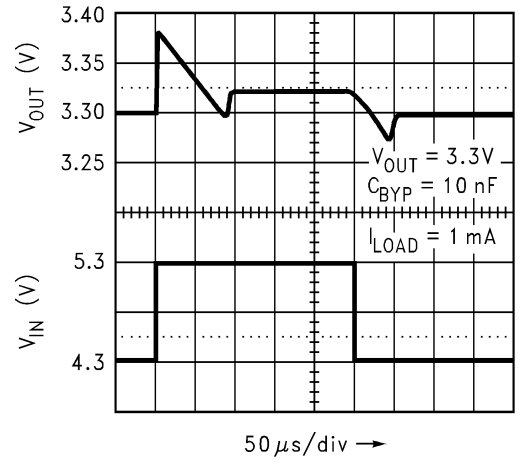


Figure 33. Line Transient Response

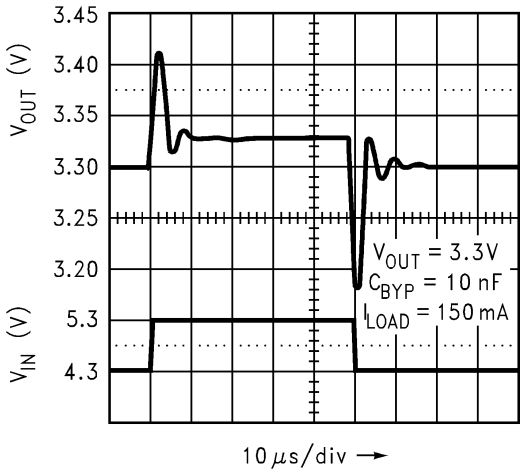


Figure 34. Line Transient Response

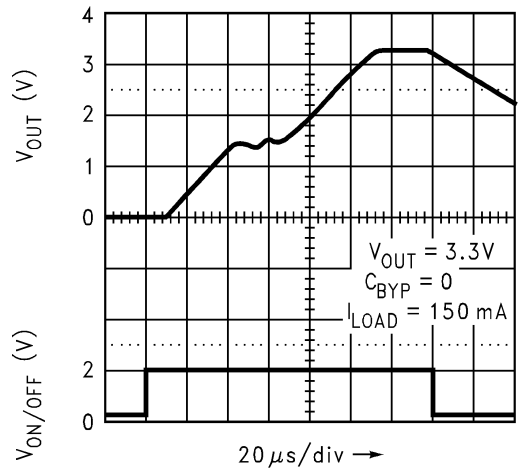


Figure 35. Turn-On Time

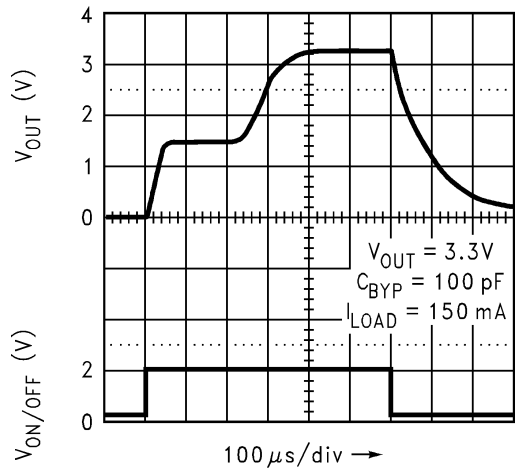


Figure 36. Turnon Time

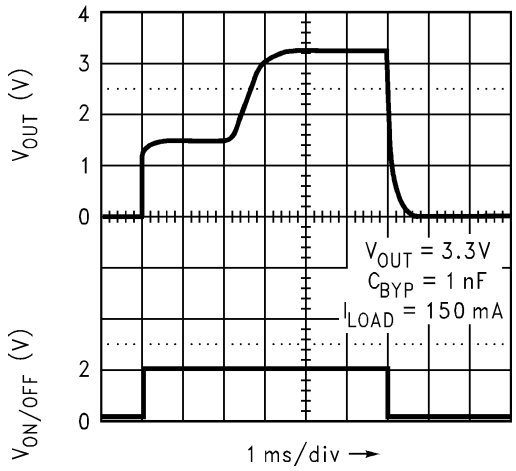


Figure 37. Turnon Time

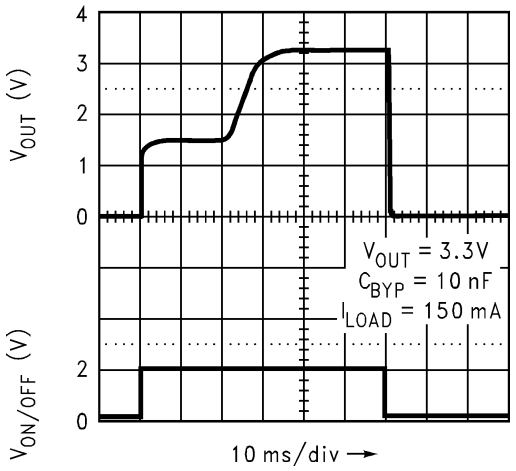


Figure 38. Turnon Time

9 Power Supply Recommendations

The LP2985-N is designed to operate from an input voltage supply range between V_{IN} of 2.5 V and 16 V. (Recommended minimum V_{IN} is the greater of 3.1 V or $V_{OUT(max)}$ + rated dropout voltage (max) for operating load current.) The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help to improve the output noise performance.

10 Layout

10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close as possible to each other, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device. In most applications, this ground plane is necessary to meet thermal requirements.

10.2 Layout Example

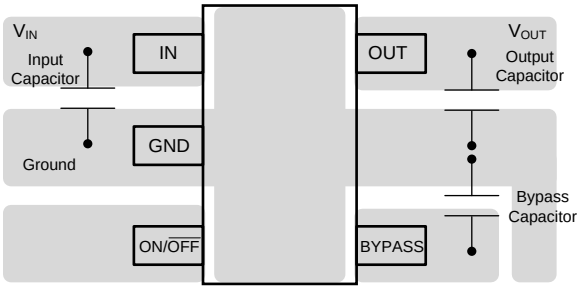


Figure 39. LP2985 SOT-23 Package Typical Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

- *Semiconductor and IC Package Thermal Metrics*
- *Using New Thermal Metrics*
- *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2985AIM5-2.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LAUA	Samples
LP2985AIM5-2.7/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LALA	Samples
LP2985AIM5-2.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0KA	Samples
LP2985AIM5-2.9/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LAXA	Samples
LP2985AIM5-3.0	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	L0OA	
LP2985AIM5-3.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0OA	Samples
LP2985AIM5-3.1/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0PA	Samples
LP2985AIM5-3.3	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	L0RA	
LP2985AIM5-3.3/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0RA	Samples
LP2985AIM5-3.6/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0SA	Samples
LP2985AIM5-3.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0YA	Samples
LP2985AIM5-4.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0TA	Samples
LP2985AIM5-4.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LA7A	Samples
LP2985AIM5-5.0	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	L0UA	
LP2985AIM5-5.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0UA	Samples
LP2985AIM5-5.7/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LKTA	Samples
LP2985AIM5-6.1/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LF6A	Samples
LP2985AIM5X-2.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LAUA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2985AIM5X-2.6/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LCEA	Samples
LP2985AIM5X-2.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0KA	Samples
LP2985AIM5X-2.9/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LAXA	Samples
LP2985AIM5X-3.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0OA	Samples
LP2985AIM5X-3.1/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0PA	Samples
LP2985AIM5X-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0RA	Samples
LP2985AIM5X-3.6/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0SA	Samples
LP2985AIM5X-3.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0YA	Samples
LP2985AIM5X-4.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0TA	Samples
LP2985AIM5X-4.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LA7A	Samples
LP2985AIM5X-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0UA	Samples
LP2985AIM5X-6.1/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LF6A	Samples
LP2985IM5-2.5	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	LAUB	
LP2985IM5-2.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LAUB	Samples
LP2985IM5-2.7/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LALB	Samples
LP2985IM5-2.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0KB	Samples
LP2985IM5-2.9/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LAXB	Samples
LP2985IM5-3.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0OB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2985IM5-3.1/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0PB	Samples
LP2985IM5-3.2/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0QB	Samples
LP2985IM5-3.3	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	L0RB	
LP2985IM5-3.3/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0RB	Samples
LP2985IM5-3.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LAIB	Samples
LP2985IM5-3.6/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0SB	Samples
LP2985IM5-3.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0YB	Samples
LP2985IM5-4.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0TB	Samples
LP2985IM5-4.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LA7B	Samples
LP2985IM5-5.0	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	L0UB	
LP2985IM5-5.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0UB	Samples
LP2985IM5-5.7/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LKTB	Samples
LP2985IM5-6.1/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LF6B	Samples
LP2985IM5X-2.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LAUB	Samples
LP2985IM5X-2.7/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LALB	Samples
LP2985IM5X-2.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0KB	Samples
LP2985IM5X-3.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0OB	Samples
LP2985IM5X-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0RB	Samples
LP2985IM5X-3.6/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0SB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2985IM5X-4.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0TB	Samples
LP2985IM5X-4.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LA7B	Samples
LP2985IM5X-5.0	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125	L0UB	
LP2985IM5X-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0UB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

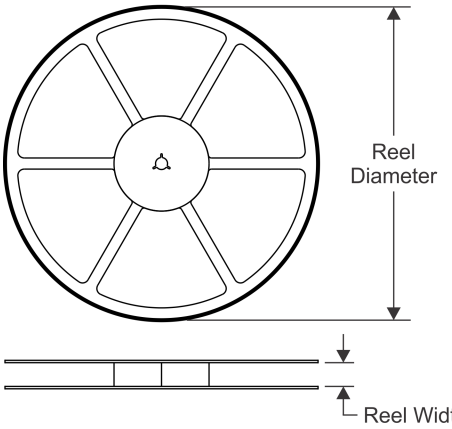
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

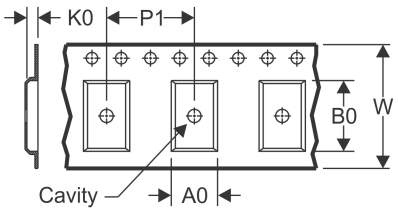
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

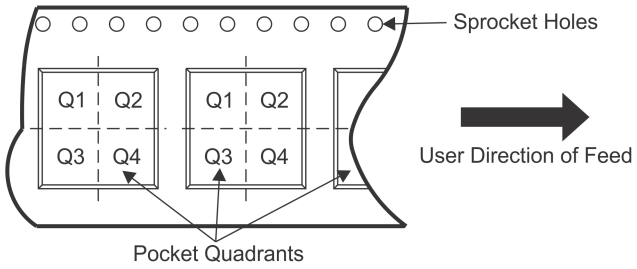


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

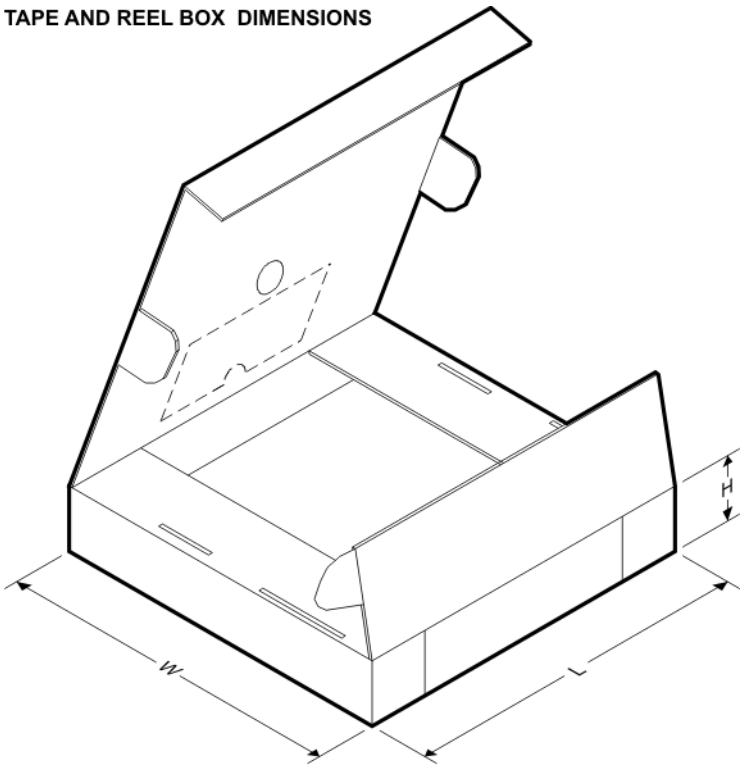


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2985AIM5-2.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-2.7/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-2.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-2.9/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-3.0	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-3.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-3.1/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-3.3	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-3.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-3.6/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-3.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-4.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-4.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-5.0	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-5.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-5.7/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-6.1/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2985AIM5X-2.6/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-2.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-2.9/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-3.1/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-3.6/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-3.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-4.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-4.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-6.1/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-2.5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-2.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-2.7/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-2.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-2.9/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.1/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.2/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.3	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.6/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-4.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-4.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-5.0	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-5.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-5.7/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-6.1/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-2.7/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-2.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-3.6/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-4.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-4.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-5.0	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2985AIM5-2.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-2.7/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-2.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-2.9/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-3.0	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-3.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-3.1/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-3.3	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-3.3/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-3.6/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-3.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-4.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-4.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-5.0	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-5.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-5.7/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-6.1/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5X-2.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-2.6/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-2.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

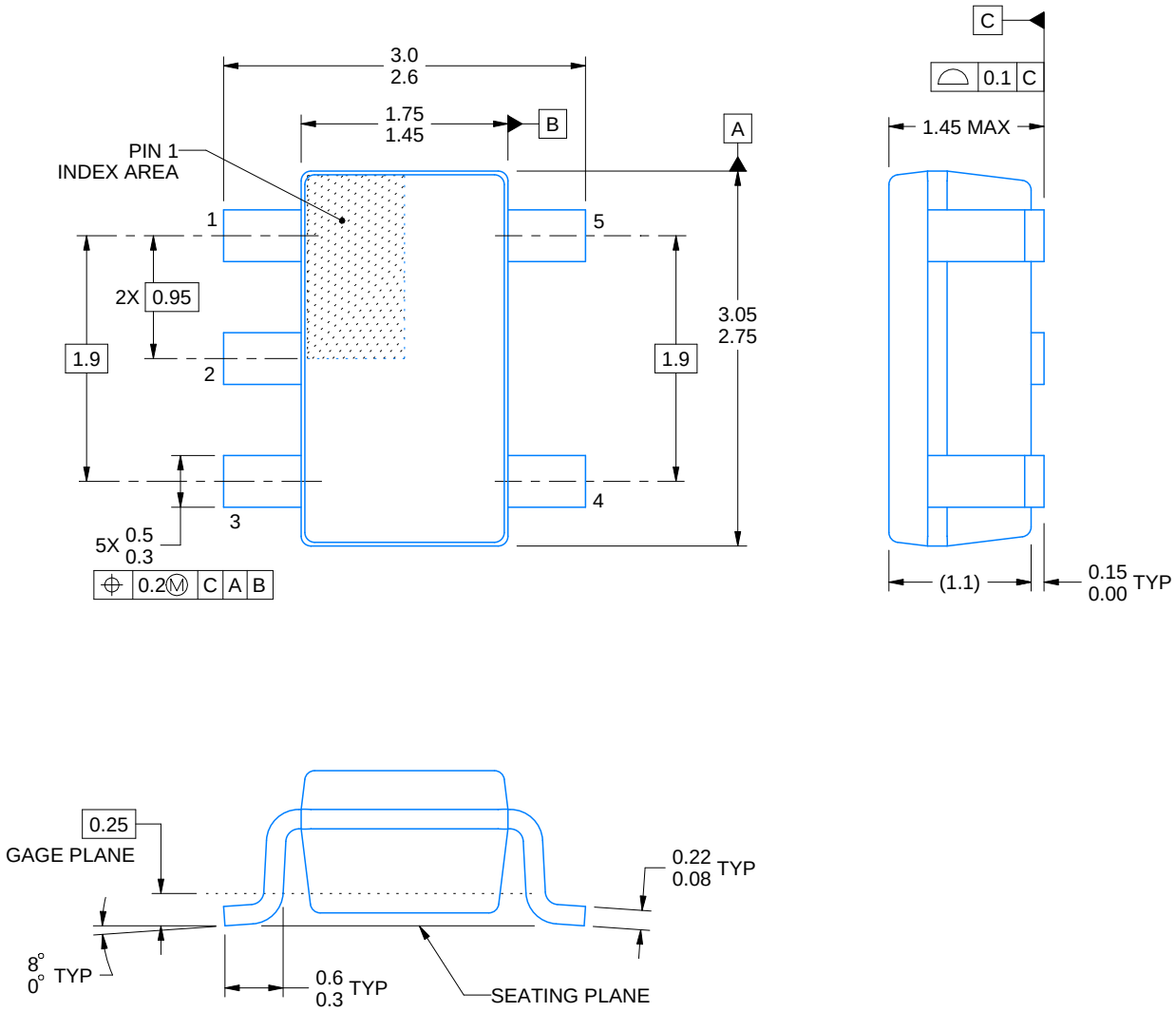
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2985AIM5X-2.9/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-3.1/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-3.6/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-3.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-4.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-4.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-6.1/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5-2.5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-2.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-2.7/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-2.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-2.9/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-3.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-3.1/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-3.2/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-3.3	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-3.3/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-3.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-3.6/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-3.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-4.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-4.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-5.0	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-5.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-5.7/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-6.1/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5X-2.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5X-2.7/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5X-2.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5X-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5X-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5X-3.6/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5X-4.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5X-4.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5X-5.0	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5X-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

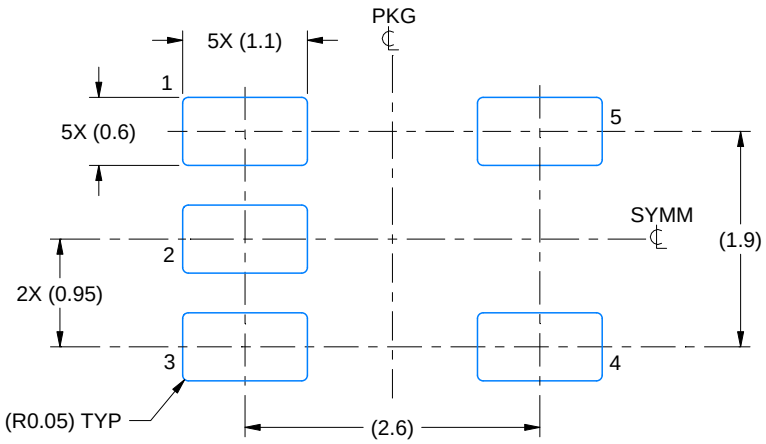
SMALL OUTLINE TRANSISTOR



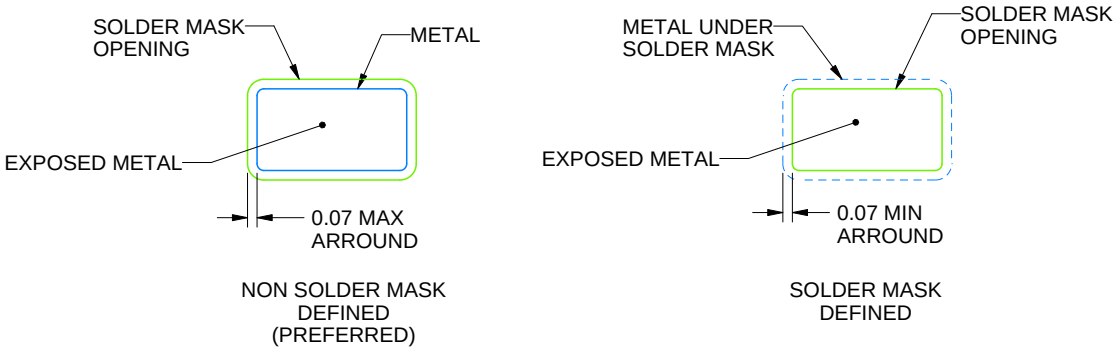
4214839/D 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

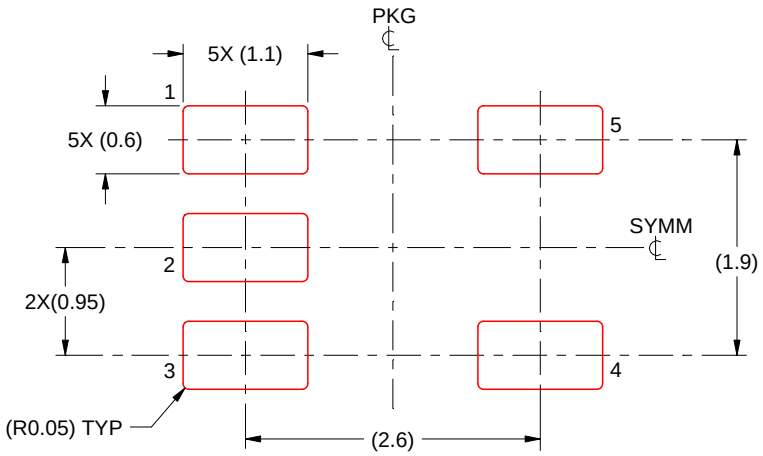


SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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