



THE DATASHEET OF LP3986TLX-3333

LP3986 Dual Micropower 150 mA Ultra Low-Dropout CMOS Voltage Regulators in DSBGA Package

Check for Samples: [LP3986](#)

FEATURES

- Miniature 8-I/O DSBGA Package
- Stable With 1 μ F Ceramic and High Quality Tantalum Output Capacitors
- Fast Turn-on
- Two Independent Regulators
- Logic Controlled Enable
- Over Current and Thermal Protection

APPLICATIONS

- CDMA Cellular Handsets
- GSM Cellular Handsets
- Portable Information Appliances
- Portable Battery Applications

DESCRIPTION

The LP3986 is a 150 mA dual low dropout regulator designed for portable and wireless applications with demanding performance and board space requirements.

The LP3986 is stable with a small 1 μ F $\pm$ 30% ceramic output capacitor requiring smallest possible board space.

The LP3986's performance is optimized for battery powered systems to deliver ultra low noise, extremely low dropout voltage and low quiescent current independent of load current. Regulator ground current increases very slightly in dropout, further prolonging the battery life. Optional external bypass capacitor reduces the output noise further without slowing down the load transient response. Fast start-up time is achieved by utilizing a speed-up circuit that actively pre-charges the bypass capacitor. Power supply rejection is better than 60 dB at low frequencies and 55 dB at 10 kHz. High power supply rejection is maintained at low input voltage levels common to battery operated circuits.

The LP3986 is available in a DSBGA package. Performance is specified for a -40°C to $+125^{\circ}\text{C}$ temperature range. For single LDO applications, please refer to the LP3985 datasheet.

Table 1. Key Specifications

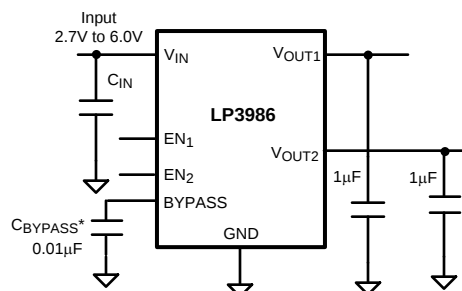
	VALUE	UNIT
Guaranteed output current per regulator	150	mA
Typical quiescent current when both regulators in shutdown mode	1	nA
Typical dropout voltage at 150 mA output current	60	mV
Typical ground current	115	μ A
Typical output noise	40	μ V
Fast turn-on circuit	200	μ s
Junction temperature	-40 to $+125$	$^{\circ}\text{C}$



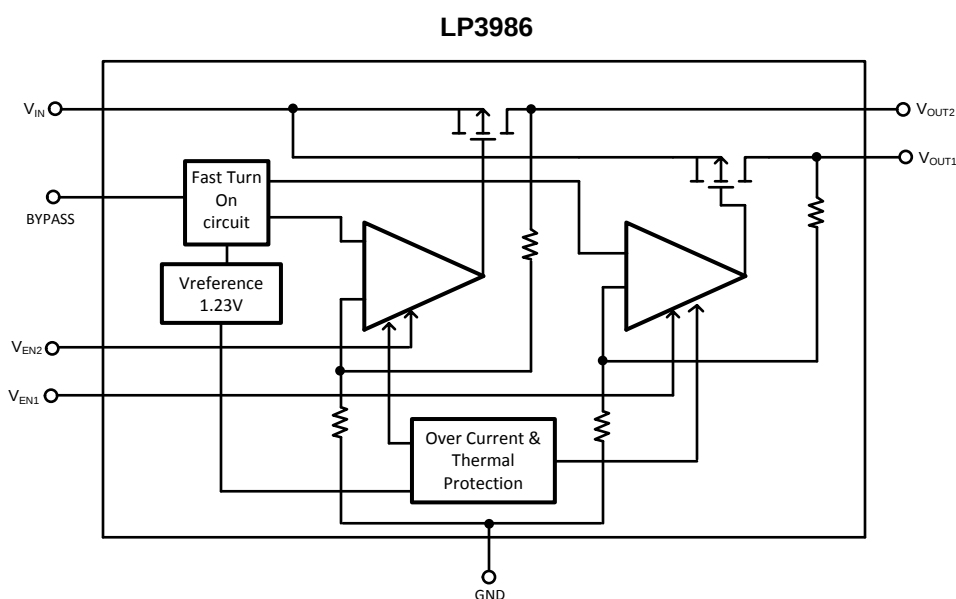
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

Typical Application Circuit



Block Diagram



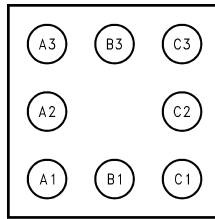
Pin Functions

PIN DESCRIPTIONS

Name	DSBGA ⁽¹⁾	Function
V _{OUT2}	A1	Output Voltage of the second LDO
EN ₂	B1	Enable input for the second LDO
BYPASS	C1	Bypass capacitor for the bandgap
GND	C2	Common ground
GND	C3	Common ground
EN ₁	B3	Enable input for the first LDO
V _{OUT1}	A3	Output Voltage of the first LDO
V _{IN}	A2	Common input for both LDOs

- (1) The pin numbering scheme for the DSBGA package was revised in April 2002 to conform to JEDEC standard. Only the pin numbers were revised. No changes to the physical location of the inputs/outputs were made. For reference purposes, the obsolete numbering scheme had V_{OUT2} as pin 1, EN₂ as pin 2, BYPASS as pin 3, GND as pins 4 and 5, EN₁ as pin 6, V_{OUT1} as pin 7, and V_{IN} as pin 8.

Connection Diagram



8 Bump DSBGA Package – Top View
See Package Number YZR0008



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾ ⁽²⁾ ⁽³⁾

V_{IN}, V_{EN}	–0.3 to 6.5V
V_{OUT}	–0.3 to $(V_{IN}+0.3V) \leq 6.5V$
Junction Temperature	150°C
Storage Temperature	–65°C to +150°C
Pad Temp. ⁽⁴⁾	235°C
Maximum Power Dissipation ⁽⁵⁾	364mW
ESD Rating ⁽⁶⁾	
Human Body Model	2kV
Machine Model	200V

- (1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see [Electrical Characteristics](#).
- (2) All voltages are with respect to the potential at the GND pin.
- (3) **If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.**
- (4) Additional information on pad temperature can be found in TI's AN-1112 application report (SNVA009).
- (5) The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using the formula: $P_D = (T_J - T_A)/\theta_{JA}$. Where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. The 364mW rating appearing under Absolute Maximum Ratings results from substituting the Absolute Maximum junction temperature, 150°C, for T_J , 70°C for T_A , and 220°C/W for θ_{JA} . More power can be dissipated safely at ambient temperatures below 70°C. Less power can be dissipated safely at ambient temperatures above 70°C. The Absolute Maximum power dissipation can be increased by 4.5mW for each degree below 70°C, and it must be derated by 4.5mW for each degree above 70°C.
- (6) The human body model is 100pF discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

Operating Ratings ^{(1) (2)}

V_{IN}	2.7 to 6V
V_{EN}	0 to $(V_{IN} + 0.3V) \leq 6V$
Junction Temperature	-40°C to +125°C
Thermal Resistance	
θ_{JA}	220°C/W
Maximum Power Dissipation ⁽³⁾	250mW

- (1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see [Electrical Characteristics](#).
- (2) All voltages are with respect to the potential at the GND pin.
- (3) Like the Absolute Maximum power dissipation, the maximum power dissipation for operation depends on the ambient temperature. The 250mW rating appearing under Operating Ratings results from substituting the maximum junction temperature for operation, 125°C, for T_J , 70°C for T_A , and 220°C/W for θ_{JA} into (1) above. More power can be dissipated at ambient temperatures below 70°C. Less power can be dissipated at ambient temperatures above 70°C. The maximum power dissipation for operation can be increased by 4.5mW for each degree below 70°C, and it must be derated by 4.5mW for each degree above 70°C.

Electrical Characteristics

Unless otherwise specified: $V_{IN} = V_{OUT(nom)} + 0.5V$, $C_{IN} = 1\mu F$, $I_{OUT} = 1mA$, $C_{OUT} = 1\mu F$, $C_{BYPASS} = 0.01\mu F$. Typical values and limits appearing in standard typeface are for $T_J = 25^\circ C$. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, -40°C to +125°C. ^{(1) (2)}

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
ΔV_{OUT}	Output Voltage Tolerance	$I_{OUT} = 1mA$		-2.5 -3.0	2.5 3.0	% of $V_{OUT(nom)}$
	Line Regulation Error ⁽³⁾	$V_{IN} = (V_{OUT(nom)} + 0.5V)$ to 6.0V, $I_{OUT} = 1mA$	0.006		0.092 0.128	%/V
	Load Regulation Error ⁽⁴⁾	$I_{OUT} = 1mA$ to 150 mA	0.003		0.006 0.01	%/mA
	Output AC Line Regulation	$V_{IN} = V_{OUT(nom)} + 1V$, $I_{OUT} = 150mA$ (Figure 1)	1.5			mV _{P-P}
PSRR	Power Supply Rejection Ratio	$V_{IN} = 3.1V$, $f = 1kHz$, $I_{OUT} = 50mA$ (Figure 2)	60			dB
		$V_{IN} = 3.1V$, $f = 10kHz$, $I_{OUT} = 50mA$ (Figure 2)	50			
I_Q	Quiescent Current	Both Regulators ON $V_{EN} = 1.4V$, $I_{OUT} = 0mA$	115		200	μA
		Both Regulators ON $V_{EN} = 1.4V$, $I_{OUT} = 0$ to 150 mA	220		320	
		One Regulator ON $V_{EN} = 1.4V$, $I_{OUT} = 0mA$	75		130	
		One Regulator ON $V_{EN} = 1.4V$, $I_{OUT} = 0$ to 150 mA	130		200	
		$V_{EN} = 0.4V$, Both Regulators OFF (shutdown)	0.001		2 4	
	Dropout Voltage ⁽⁵⁾	$I_{OUT} = 1mA$ $I_{OUT} = 150mA$	0.4 60		2 100	mV
I_{SC}	Short Circuit Current Limit	Output Grounded	600			mA

- (1) All limits are guaranteed. All electrical characteristics having room temperature limits are tested during production with $T_J = 25^\circ C$ or correlated using Statistical Quality Control (SQC) methods. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
- (2) The target output voltage, which is labeled $V_{OUT(nom)}$, is the desired voltage option.
- (3) The output voltage changes slightly with line voltage. An increase in the line voltage results in a slight increase in the output voltage and vice versa.
- (4) The output voltage changes slightly with load current. An increase in the load current results in a slight decrease in the output voltage and vice versa. Tested limit applies to V_{out} 's of 2.5V and greater.
- (5) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100mV below its nominal value.

Electrical Characteristics (continued)

Unless otherwise specified: $V_{IN} = V_{OUT(nom)} + 0.5V$, $C_{IN} = 1\mu F$, $I_{OUT} = 1mA$, $C_{OUT} = 1\mu F$, $C_{BYPASS} = 0.01\mu F$. Typical values and limits appearing in standard typeface are for $T_J = 25^\circ C$. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, $-40^\circ C$ to $+125^\circ C$. ⁽¹⁾ ⁽²⁾

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
$I_{OUT(PK)}$	Peak Output Current ⁽⁶⁾	$V_{OUT} \geq V_{OUT(nom)} - 5\%$	500	300		mA
T_{ON}	Turn-On Time ⁽⁷⁾	$C_{BYPASS} = 0.01\mu F$	200			μs
e_n	Output Noise Voltage	$BW = 10\text{ Hz to }100\text{ kHz}$, $C_{OUT} = 1\mu F$	40			μV_{rms}
$pn(1/f)$	Output Noise Density	$f = 120\text{ Hz}$, $C_{OUT} = 1\mu F$	1			$\mu V/\sqrt{Hz}$
I_{EN}	Maximum Input Current at EN	$V_{EN} = 0.4$ and $V_{IN} = 6V$	± 10			nA
V_{IL}	Maximum Low Level Input Voltage at EN	$V_{IN} = 2.7$ to $6V$			0.4	V
V_{IH}	Minimum High Level Input Voltage at EN	$V_{IN} = 2.7$ to $6V$		1.4		V
Xtalk	Crosstalk Rejection	$\Delta I_{Load1} = 150\text{ mA at }1\text{KHz rate}$ $\Delta I_{Load2} = 1\text{ mA}$ $\Delta V_{OUT2}/\Delta V_{OUT1}$	-60			dB
		$\Delta I_{Load2} = 150\text{ mA at }1\text{KHz rate}$ $\Delta I_{Load1} = 1\text{ mA}$ $\Delta V_{OUT2}/\Delta V_{OUT1}$	-60			
C_{IN}	Input capacitance ⁽⁸⁾	All $V_{OUT} > 2.5V$,		1		μF
		If $V_{OUT} = 1.8V$, $V_{IN_MIN} \geq 2.9V$		4.7		μF
C_{OUT}	Capacitance ⁽⁸⁾	All $V_{OUT} > 2.5V$,		1	22	μF
		If $V_{OUT} = 1.8V$, $V_{IN_MIN} \geq 2.9V$		2.2	22	μF
	ESR	See ⁽⁹⁾		5	500	m Ω

(6) I_{PEAK} guaranteed for V_{out} 's of 2.5V and greater.

(7) Turn-on time is that between the enable input just exceeding V_{IH} and the output voltage just reaching 95% of its nominal value.

(8) Range of capacitor values for which the device will remain stable. This electrical specification is guaranteed by design.

(9) Range of capacitor ESR values for which the device will remain stable. This electrical specification is guaranteed by design.

TEST SIGNALS

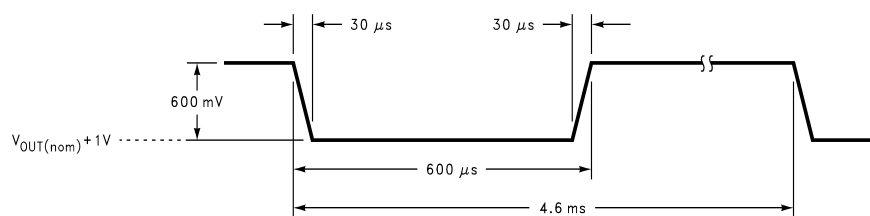


Figure 1. Line Regulation Input Test Signal

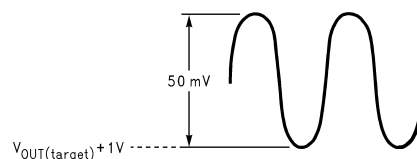


Figure 2. PSRR Input Test Signal

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, $C_{IN} = C_{OUT} = 1\mu\text{F}$ Ceramic, $C_{BP} = 0.01\mu\text{F}$, $V_{IN} = V_{OUT} + 0.5$, $T_A = 25^\circ\text{C}$, both enable pins are tied to V_{IN}

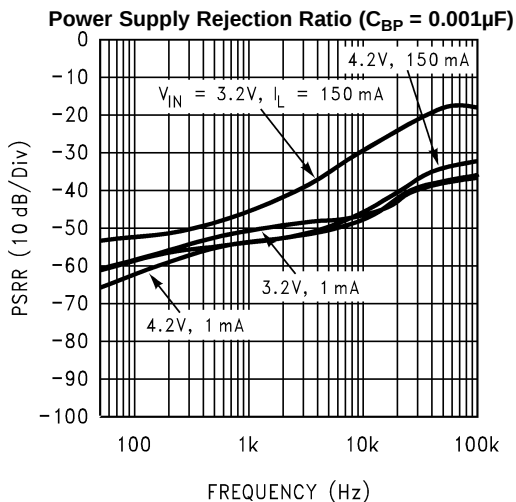


Figure 3.

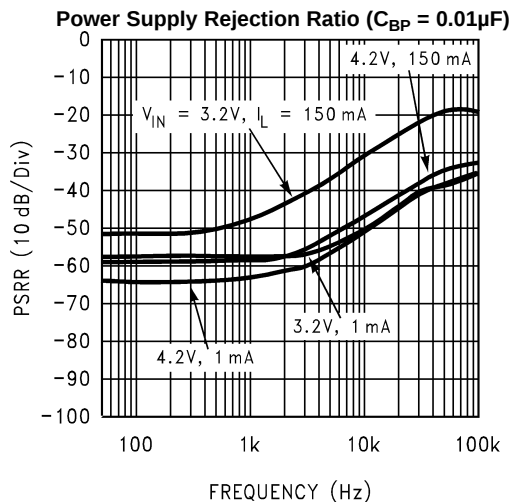


Figure 4.

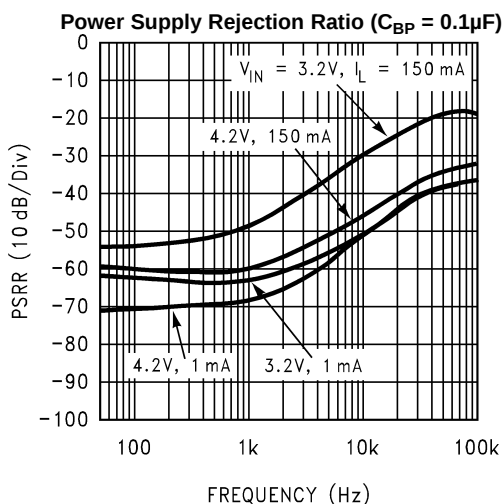


Figure 5.

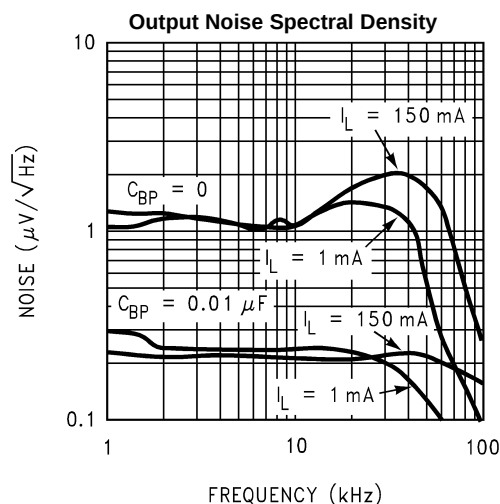


Figure 6.

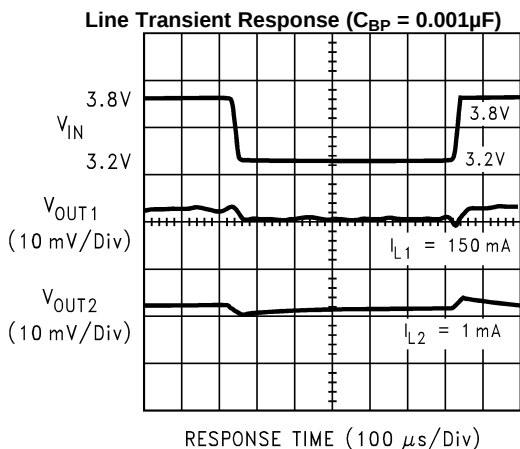


Figure 7.

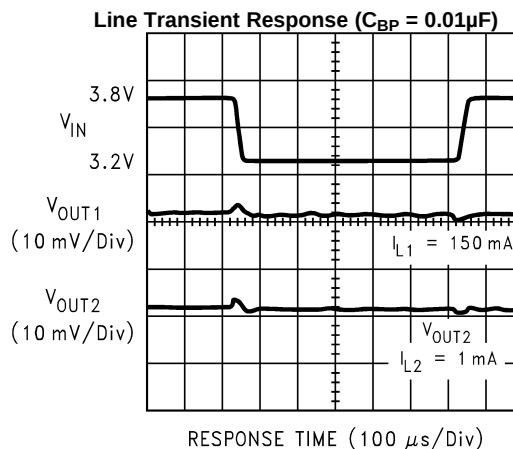


Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 1\mu\text{F}$ Ceramic, $C_{BP} = 0.01\mu\text{F}$, $V_{IN} = V_{OUT} + 0.5$, $T_A = 25^\circ\text{C}$, both enable pins are tied to V_{IN}

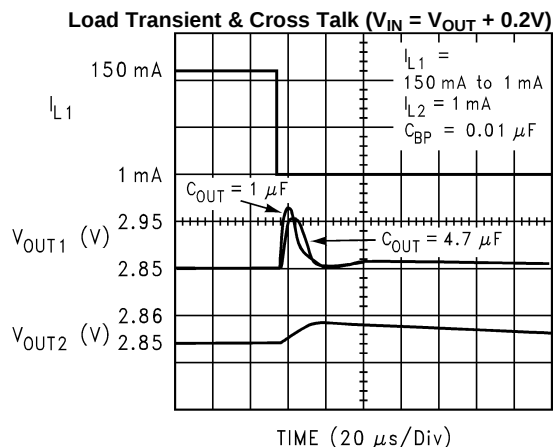


Figure 9.

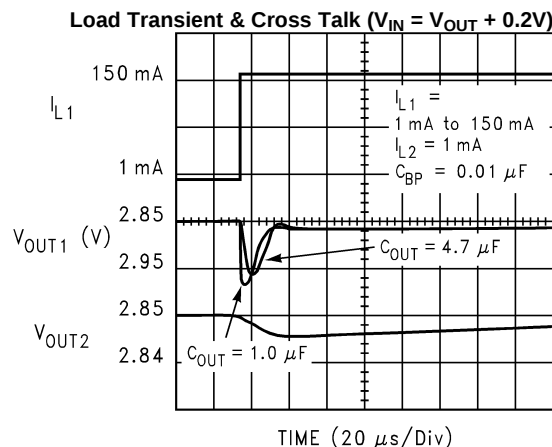


Figure 10.

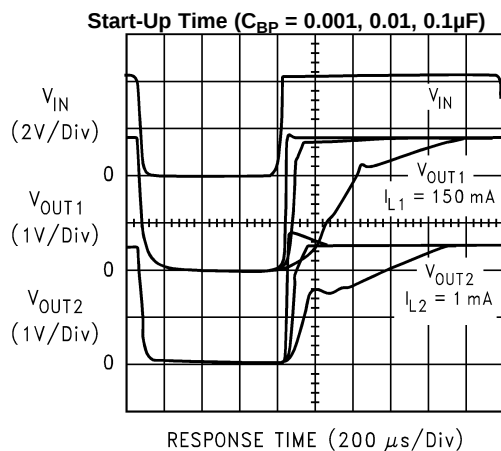


Figure 11.

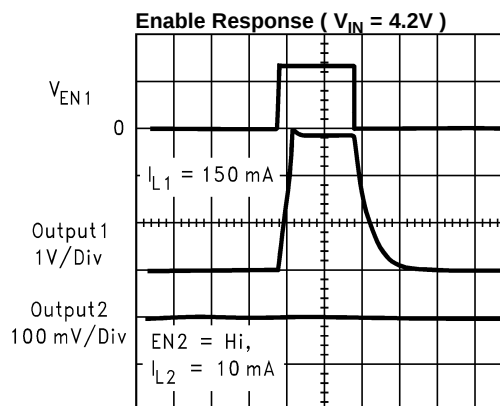
Time (50 $\mu\text{s}/\text{Div}$)

Figure 12.

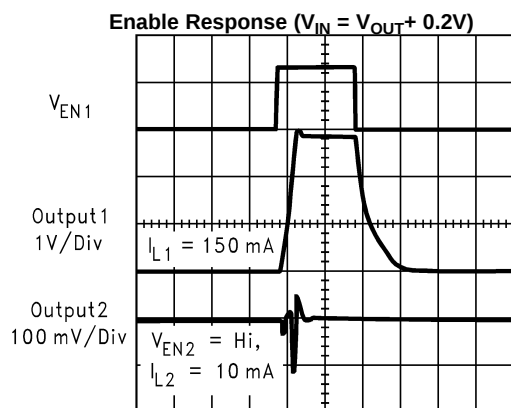
Time (50 $\mu\text{s}/\text{Div}$)

Figure 13.

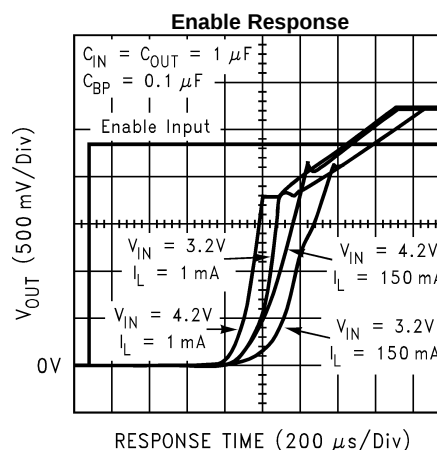


Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 1\mu\text{F}$ Ceramic, $C_{BP} = 0.01\mu\text{F}$, $V_{IN} = V_{OUT} + 0.5$, $T_A = 25^\circ\text{C}$, both enable pins are tied to V_{IN}

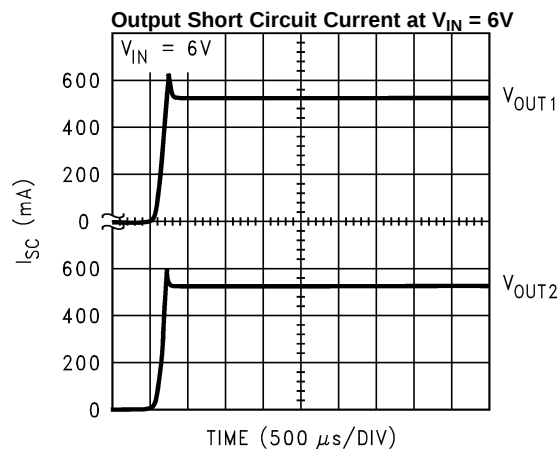


Figure 15.

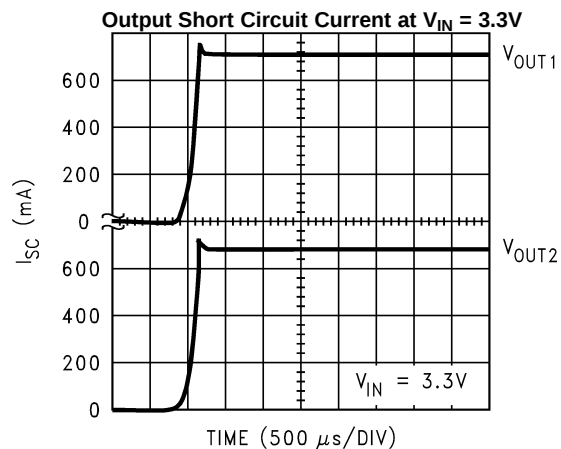


Figure 16.

APPLICATION HINTS

EXTERNAL CAPACITORS

Like any low-dropout regulator, the LP3986 requires external capacitors for regulator stability. The LP3986 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

An input capacitance of $\approx 1\mu\text{F}$ is required between the LP3986 input pin and ground (the amount of the capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will be $\approx 1\mu\text{F}$ over the entire operating temperature range.

OUTPUT CAPACITOR

The LP3986 is designed specifically to work with very small ceramic output capacitors, any ceramic capacitor (temperature characteristics X7R, X5R, Z5U or Y5V) in 1 to 22 μF range with 5m Ω to 500m Ω ESR range is suitable in the LP3986 application circuit.

It may also be possible to use tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost (see next section Capacitor Characteristics).

The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR (Equivalent Series Resistance) value which is within a stable range.

NO-LOAD STABILITY

The LP3986 will remain stable and in regulation with no-load (other than the internal voltage divider). This is specially important in CMOS RAM keep-alive applications.

CAPACITOR CHARACTERISTICS

The LP3986 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the range of 1 μF to 4.7 μF range, ceramic capacitors are the smallest, least expensive and have the lowest ESR values (which makes them best for eliminating high frequency noise). The ESR of a typical 1 μF ceramic capacitor is in the range of 20 m Ω to 40 m Ω , which easily meets the ESR requirement for stability by the LP3986.

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of -55°C to +125°C, will only vary the capacitance to within $\pm 15\%$. Most large value ceramic capacitors ($\approx 2.2\mu\text{F}$) are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature goes from 25°C to 85°C. Therefore, X7R is recommended over Z5U and Y5 in applications where the ambient temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1 μF to 4.7 μF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed.

NOISE BYPASS CAPACITOR

Connecting a 0.01 μ F capacitor between the C_{BYPASS} pin and ground significantly reduces noise on the regulator output. This cap is connected directly to a high impedance node in the band gap reference circuit. Any significant loading on this node will cause a change on the regulated output voltage. For this reason, DC leakage current through this pin must be kept as low as possible for best output voltage accuracy. The use of this 0.01 μ F bypass capacitor is strongly recommended to prevent overshoot on the output during start up.

The types of capacitors best suited for the noise bypass capacitor are ceramic and film. High-quality ceramic capacitors with either NPO or COG dielectric typically have very low leakage. Polypropylene and polycarbonate film capacitors are available in small surface-mount packages and typically have extremely low leakage current.

Unlike many other LDOs, addition of a noise reduction capacitor does not effect the transient response of the device.

ON/OFF INPUT OPERATION

The LP3986 is turned off by pulling the V_{EN} pin low, and turned on by pulling it high. If this feature is not used, the V_{EN} pin should be tied to V_{IN} to keep the regulator output on at all times. To assure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

FAST ON-TIME

The LP3986 outputs are turned on after V_{ref} voltage reaches its final value (1.23V nominal). To speed up this process, the noise reduction capacitor at the bypass pin is charged with an internal 70 μ A current source. The current source is turned off when the bandgap voltage reaches approximately 95% of its final value. The turn on time is determined by the time constant of the bypass capacitor. The smaller the capacitor value, the shorter the turn on time, but less noise gets reduced. As a result, turn on time and noise reduction need to be taken into design consideration when choosing the value of the bypass capacitor.

DSBGA MOUNTING

The DSBGA package requires specific mounting techniques which are detailed in TI's AN-1112 application report (SNVA009), in particular the section *Surface Mount Assembly Considerations*.

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

DSBGA LIGHT SENSITIVITY

Exposing the DSBGA device to direct sunlight will cause misoperation of the device. Light sources such as halogen lamps can effect electrical performance if brought near to the device.

The wavelengths which have most detrimental effect are reds and infra-reds, which means that the fluorescent lighting used inside most buildings has very little effect on performance. A DSBGA test board was brought to within 1cm of a fluorescent desk lamp and the effect on the regulated output voltage was negligible, showing a deviation of less than 0.1% from nominal.

REVISION HISTORY

Changes from Revision T (February 2013) to Revision U

Page

- Changed layout of National Data Sheet to TI format [11](#)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3986TL-2518/NOPB	ACTIVE	DSBGA	YZR	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		D 30	Samples
LP3986TL-2525/NOPB	ACTIVE	DSBGA	YZR	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		D 27	Samples
LP3986TL-2626/NOPB	ACTIVE	DSBGA	YZR	8		TBD	Call TI	Call TI		D 28	Samples
LP3986TL-2818/NOPB	ACTIVE	DSBGA	YZR	8		TBD	Call TI	Call TI		D 25	Samples
LP3986TL-2828/NOPB	ACTIVE	DSBGA	YZR	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D 10	Samples
LP3986TL-285285/NOPB	ACTIVE	DSBGA	YZR	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D 11	Samples
LP3986TL-2929/NOPB	ACTIVE	DSBGA	YZR	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		D 15	Samples
LP3986TL-3028/NOPB	ACTIVE	DSBGA	YZR	8		TBD	Call TI	Call TI		D 26	Samples
LP3986TL-3030/NOPB	ACTIVE	DSBGA	YZR	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D 12	Samples
LP3986TL-3131/NOPB	ACTIVE	DSBGA	YZR	8		TBD	Call TI	Call TI	-40 to 125	D 13	Samples
LP3986TL-3333/NOPB	ACTIVE	DSBGA	YZR	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		D 17	Samples
LP3986TLX-2518/NOPB	ACTIVE	DSBGA	YZR	8		TBD	Call TI	Call TI		D 30	Samples
LP3986TLX-2525/NOPB	ACTIVE	DSBGA	YZR	8		TBD	Call TI	Call TI		D 27	Samples
LP3986TLX-2626/NOPB	ACTIVE	DSBGA	YZR	8		TBD	Call TI	Call TI		D 28	Samples
LP3986TLX-2818/NOPB	ACTIVE	DSBGA	YZR	8		TBD	Call TI	Call TI		D 25	Samples
LP3986TLX-2828/NOPB	ACTIVE	DSBGA	YZR	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D 10	Samples
LP3986TLX-2929/NOPB	ACTIVE	DSBGA	YZR	8		TBD	Call TI	Call TI		D 15	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3986TLX-3028/NOPB	ACTIVE	DSBGA	YZR	8		TBD	Call TI	Call TI		D 26	Samples
LP3986TLX-3030/NOPB	ACTIVE	DSBGA	YZR	8		TBD	Call TI	Call TI	-40 to 125	D 12	Samples
LP3986TLX-3333/NOPB	ACTIVE	DSBGA	YZR	8		TBD	Call TI	Call TI		D 17	Samples
LP3986TLX285285/NOPB	ACTIVE	DSBGA	YZR	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		D 11	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3986TL-2518/NOPB	DSBGA	YZR	8	250	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1
LP3986TL-2525/NOPB	DSBGA	YZR	8	250	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1
LP3986TL-2828/NOPB	DSBGA	YZR	8	250	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1
LP3986TL-285285/NOPB	DSBGA	YZR	8	250	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1
LP3986TL-2929/NOPB	DSBGA	YZR	8	250	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1
LP3986TL-3030/NOPB	DSBGA	YZR	8	250	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1
LP3986TL-3333/NOPB	DSBGA	YZR	8	250	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1
LP3986TLX-2828/NOPB	DSBGA	YZR	8	3000	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1
LP3986TLX285285/NOPB	DSBGA	YZR	8	3000	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1

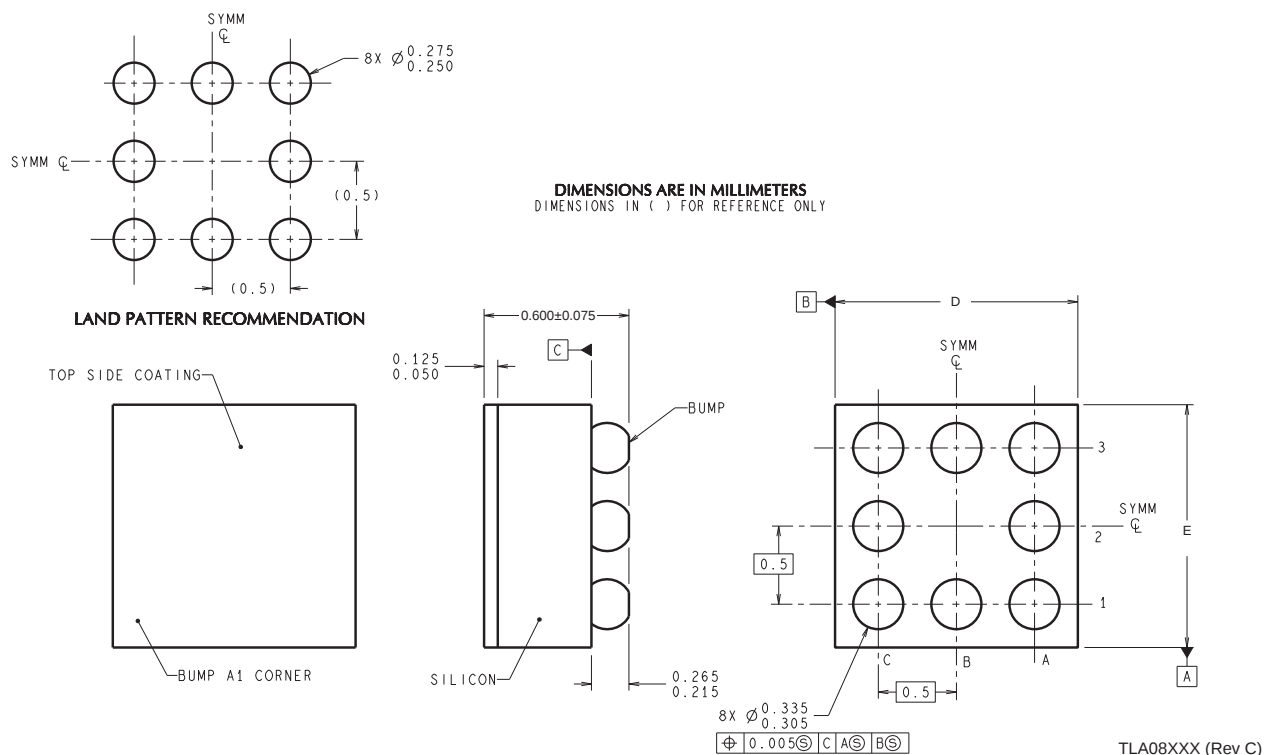
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3986TL-2518/NOPB	DSBGA	YZR	8	250	210.0	185.0	35.0
LP3986TL-2525/NOPB	DSBGA	YZR	8	250	210.0	185.0	35.0
LP3986TL-2828/NOPB	DSBGA	YZR	8	250	210.0	185.0	35.0
LP3986TL-285285/NOPB	DSBGA	YZR	8	250	210.0	185.0	35.0
LP3986TL-2929/NOPB	DSBGA	YZR	8	250	210.0	185.0	35.0
LP3986TL-3030/NOPB	DSBGA	YZR	8	250	210.0	185.0	35.0
LP3986TL-3333/NOPB	DSBGA	YZR	8	250	210.0	185.0	35.0
LP3986TLX-2828/NOPB	DSBGA	YZR	8	3000	210.0	185.0	35.0
LP3986TLX285285/NOPB	DSBGA	YZR	8	3000	210.0	185.0	35.0

YZR0008



D: Max = 1.591 mm, Min = 1.53 mm

E: Max = 1.591 mm, Min = 1.53 mm

4215045/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View LP3986TLX-3333](#) on WIN SOURCE

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management