THE DATASHEET OF

LP3990MF-1.2

LP3990 150-mA Linear Voltage Regulator for Digital Applications

1 Features

- 1% Voltage Accuracy at Room Temperature
- Stable with Ceramic Capacitor
- Logic Controlled Enable
- No Noise Bypass Capacitor Required
- Thermal-Overload and Short-Circuit Protection
- Input Voltage Range, 2 V to 6 V
- Output Voltage Range, 0.8 V to 3.3 V
- Output Current, 150 mA
- Output Stable - Capacitors, 1 µF
- Virtually Zero I_Q (Disabled), < 10 nA
- Very Low I_Q (Enabled), 43 µA
- Low Output Noise, 150 μV_{RMS}
- PSRR, 55 dB at 1 kHz
- Fast Start-Up, 105 µs

2 Applications

- Cellular Handsets
- Hand-Held Information Appliances

3 Description

The LP3990 regulator is designed to meet the requirements of portable, battery-powered systems providing an accurate output voltage, low-noise, and low-quiescent current. The LP3990 will provide a 0.8-V output from the low input voltage of 2 V at up to a 150-mA load current. When switched into shutdown mode via a logic signal at the enable pin (EN), the power consumption is reduced to virtually zero.

The LP3990 is designed to be stable with space-saving ceramic capacitors with values as low as 1 µF.

Performance is specified for a –40°C to 125°C junction temperature range.

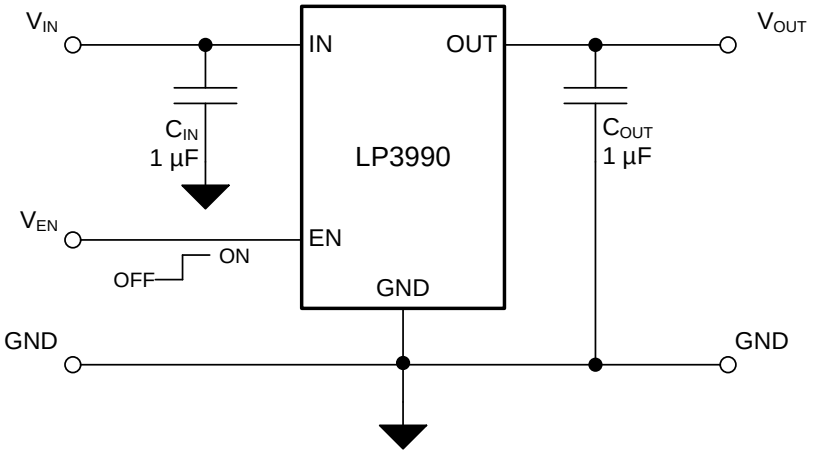
For output voltages other than 0.8 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V, 2.5 V, 2.8 V, or 3.3 V, please contact the Texas Instruments sales office.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP3990	DSBGA (4)	1.324 mm x 1.045 mm (MAX)
	WSON (6)	2.90 mm x 1.60 mm
	SOT-23 (5)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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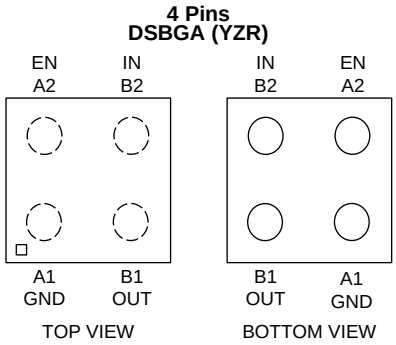
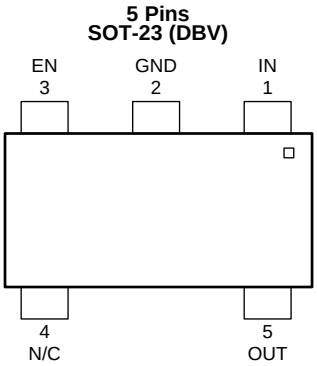
4 Revision History

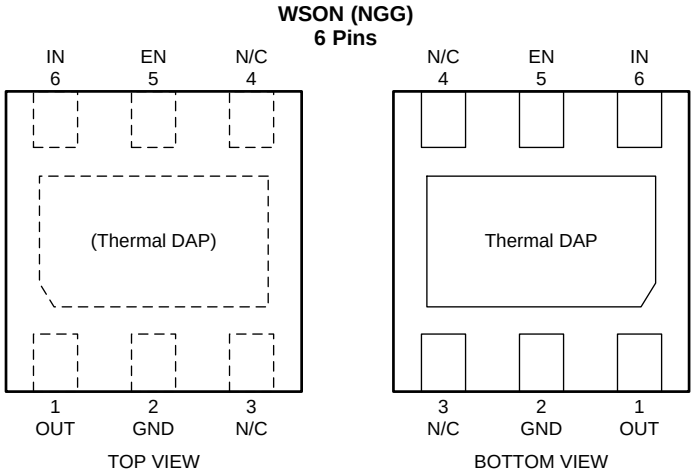
Changes from Revision I (May 2013) to Revision J **Page**

- Added *Device Information* and *Handling Rating* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections; moved some curves to *Application Curves* section ... 1

5 Pin Configuration and Functions







Pin Functions

PIN				I/O	DESCRIPTION
NAME	DSBGA YZR	SOT-23 DBV	WSON NGG		
GND	A1	2	2	—	Common Ground.
EN	A2	3	5	I	Enable Input; Enables the Regulator when ≥ 0.95 V. Disables the Regulator when ≤ 0.4 V. Enable Input has 1-MΩ (typical) pull-down resistor to GND.
OUT	B1	5	1	O	Voltage output. A 1-µF Low ESR Capacitor should be connected to this Pin. Connect this output to the load circuit.
IN	B2	1	6	I	Voltage supply Input. A 1-µF capacitor should be connected at this input.
N/C	N/A	4	3	I	No internal connection.
N/C		N/A	4	I	No internal connection.
N/C			Pad	—	Thermal pad. Connect to Pin 2.

6 Specifications

6.1 Absolute Maximum Ratings (1)(2)(3)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input voltage	–0.3	6.5	V
Output voltage	–0.3	Note (4)	
ENABLE input voltage	–0.3	6.5	
Continuous power dissipation internally limited	Note (5)		

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) All voltages are with respect to the potential at the GND pin.
(4) The lower of V_{IN} + 0.3 V or 6.5 V.
(5) Internal thermal shutdown circuitry protects the device from permanent damage.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	–2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	250	1500	
		Machine model	–200	200	

(1) JEDEC document JEP155 states that 2000-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Input voltage, V_{IN}	2		6	V
Enable input voltage, V_{EN}	0.0		V_{IN}	
Junction temperature, T_J (1)	–40		125	°C

(1) $T_{J(max)} = (T_{A(max)} + (R_{\theta JA} \times P_{D(max)}))$

6.4 Thermal Information

THERMAL METRIC (1)		LP3990			UNIT
		YZR (DSBGA)	DBV (SOT-23)	NGG (WSON)	
		4 PINS	5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	188.9	165.2	53.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.0	69.9	51.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	105.3	27.3	28.2	
ψ_{JT}	Junction-to-top characterization parameter	0.7	1.8	0.6	
ψ_{JB}	Junction-to-board characterization parameter	105.2	26.8	28.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	8.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics[1][2]

Unless otherwise noted, V_{EN} = 950 mV, V_{IN} = V_{OUT} + 1 V or V_{IN} = 2 V, whichever is higher. C_{IN} = 1 µF, I_{OUT} = 1 mA, C_{OUT} = 0.47 µF.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	Note [3], T_J = 25°C		2		6	V
ΔV_{OUT}	Output voltage tolerance	I_{LOAD} = 1 mA T_J = 25°C	DSBGA	–1		1%	
			WQFN	–1.5%		1.5%	
			SOT-23	–1.5%		1.5%	
		Over full line and load regulation	DSBGA	–2.5%		2.5%	
			WQFN	–3%		3%	
			SOT-23	–4%		4%	
	Line regulation error	V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to 6 V		0.1	0.02	0.1	%/V
	Load regulation error	I_{OUT} = 1 mA to 150 mA	V_{OUT} = 0.8 V to 1.95 V DSBGA	–0.005	0.002	0.005	%/mA
			V_{OUT} = 0.8 V to 1.95 V WQFN, SOT-23	–0.008	0.003	0.008	
			V_{OUT} = 2 V to 3.3 V DSBGA	–0.002	0.0005	0.002	
			V_{OUT} = 2 V to 3.3 V WQFN, SOT-23	–0.005	0.002	0.005	
V_{DO}	Dropout voltage	I_{OUT} = 150 mA[4] [5]			120	200	mV
I_{LOAD}	Load current	Note [5][6], T_J = 25°C		0			µA
I_Q	Quiescent current	V_{EN} = 950 mV, I_{OUT} = 0 mA			43	80	µA
		V_{EN} = 950 mV, I_{OUT} = 150 mA			65	120	
		V_{EN} = 0.4 V (output disabled), T_J = 25°C			0.002	0.2	
I_{SC}	Short circuit current limit	Note [7]			550	1000	mA
I_{OUT}	Maximum output current			150			
PSRR	Power Supply Rejection Ratio	f = 1 kHz, I_{OUT} = 1 mA to 150 mA			55		dB
		f = 10 kHz, I_{OUT} = 150 mA			35		
e_η	Output noise voltage[5]	BW = 10 Hz to 100 kHz	V_{OUT} = 0.8 V		60		μV_{RMS}
			V_{OUT} = 1.5 V		125		
			V_{OUT} = 3.3 V		180		
$T_{SHUTDOWN}$	Thermal shutdown junction temperature	Junction temperature (T_J) rising until the output is disabled			155		°C
		Hysteresis			15		

(1) All voltages are with respect to the device GND terminal, unless otherwise stated.
(2) Minimum and Maximum limits are ensured through test, design, or statistical correlation over the operating junction temperature range (T_J) of –40°C to 125°C, unless otherwise stated. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.
(3) $V_{IN(MIN)}$ = $V_{OUT(NOM)}$ + 0.5 V, or 2 V, whichever is higher.
(4) Dropout voltage is voltage difference between input and output at which the output voltage drops to 100 mV below its nominal value. This parameter applies only for output voltages above 2 V.
(5) This electrical specification is verified by design.
(6) The device maintains the regulated output voltage without the load.
(7) Short-circuit current is measured with V_{OUT} pulled to 0 V and V_{IN} worst case = 6 V.

Electrical Characteristics(1)(2) (continued)

Unless otherwise noted, V_{EN} = 950 mV, V_{IN} = V_{OUT} + 1 V or V_{IN} = 2 V, whichever is higher. C_{IN} = 1 µF, I_{OUT} = 1 mA, C_{OUT} = 0.47 µF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE CONTROL CHARACTERISTICS						
I_{EN}(8)	Maximum input current at EN pin	V_{EN} = 0 V (Output is disabled) T_J = 25°C		0.001	0.1	µA
		V_{EN} = 6 V	2.5	6	10	
V_{IL}	Low input threshold	V_{IN} = 2 V to 6 V V_{EN} falling from ≥ V_{IH} until the output is disabled			0.4	V
V_{IH}	High input threshold	V_{IN} = 2 V to 6 V V_{EN} rising from ≤ V_{IL} until the output is enabled	0.95			

(8) ENABLE Pin has 1-MΩ (typical) resistor connected to GND.

6.6 Output Capacitor, Recommended Specifications(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{OUT}	Output capacitance	Capacitance(2)	0.7(3)	1	500	µF
		ESR	5			mΩ

(1) Unless otherwise specified, values and limits apply for T_J = 25°C.
(2) The full operating conditions for the application should be considered when selecting a suitable capacitor to ensure that the minimum value of capacitance is always met. Recommended capacitor type is X7R. However, dependent on application, X5R, Y5V, and Z5U can also be used. (See *Detailed Design Procedure*.)
(3) Limit applies over the full operating junction temperature range (T_J) of −40°C to 125°C.

6.7 Timing Requirements

				MIN	NOM(1)	MAX(2)	UNIT
T_{ON}	Turnon time (3)	From V_{EN} ↑ V_{IH} to V_{OUT} 95% level ($V_{IN(MIN)}$ to 6 V)	V_{OUT} = 0.8 V		80	150	µs
			V_{OUT} = 1.5 V		105	200	
			V_{OUT} = 3.3 V		175	250	
Transient response	Line transient response (ΔV_{OUT})	T_{rise} = T_{fall} = 30 µs(3), ΔV_{IN} = 600 mV			8	16	mV (pk-pk)
	Load transient response (ΔV_{OUT})	T_{rise} = T_{fall} = 1 µs(3), I_{OUT} = 1 mA to 150 mA, C_{OUT} = 1 µF			55	100	mV

(1) Nom values apply for T_J = 25°C.
(2) Maximum limits apply over the full operating junction temperature (T_J) range of −40°C to 125°C.
(3) This electrical specification is verified by design.

6.8 Typical Performance Characteristics

Unless otherwise specified, C_{IN} = 1 µF ceramic, C_{OUT} = 0.47 µF ceramic, V_{IN} = $V_{OUT(NOM)}$ + 1 V, T_A = 25°C, $V_{OUT(NOM)}$ = 1.5 V; V_{EN} = V_{IN}.

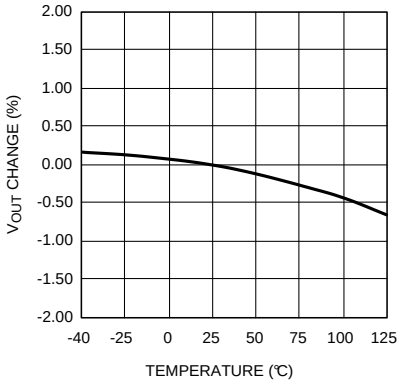


Figure 1. Output Voltage Change vs Temperature

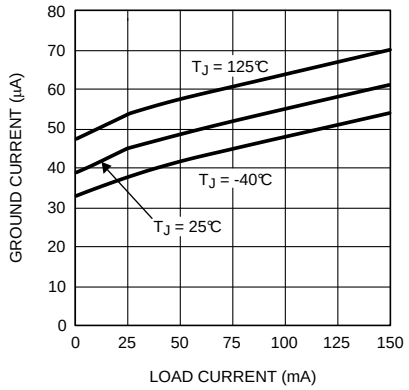
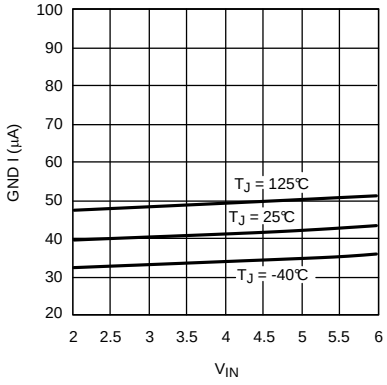
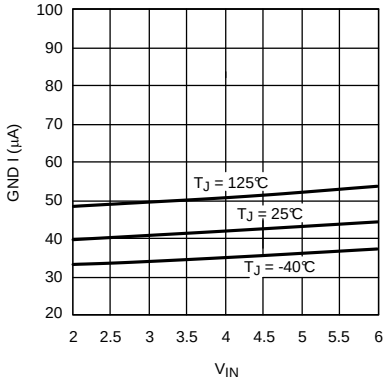


Figure 2. Ground Current vs Load Current



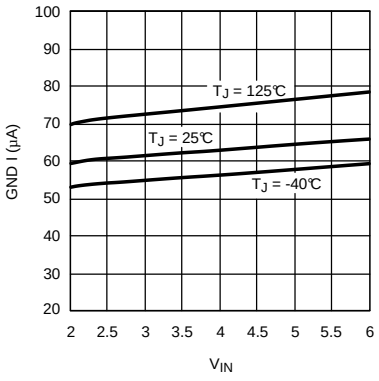
I_{LOAD} = 0 mA

Figure 3. Ground Current vs V_{IN}



I_{LOAD} = 1 mA

Figure 4. Ground Current vs V_{IN}



I_{LOAD} = 150 mA

Figure 5. Ground Current vs V_{IN}

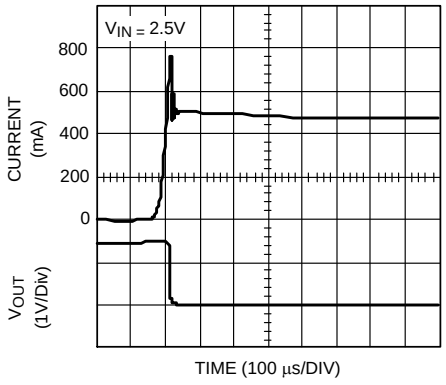


Figure 6. Short Circuit Current

Typical Performance Characteristics (continued)

Unless otherwise specified, C_{IN} = 1 µF ceramic, C_{OUT} = 0.47 µF ceramic, V_{IN} = $V_{OUT(NOM)}$ + 1 V, T_A = 25°C, $V_{OUT(NOM)}$ = 1.5 V; V_{EN} = V_{IN}.

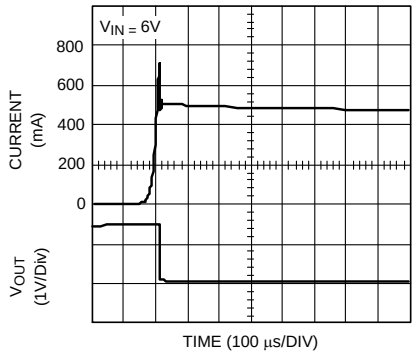


Figure 7. Short Circuit Current

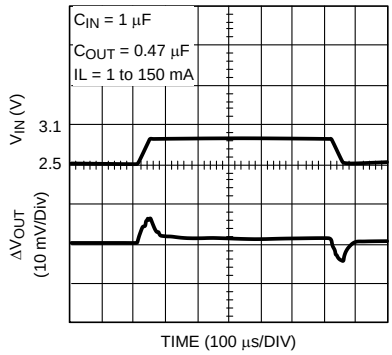


Figure 8. Line Transient

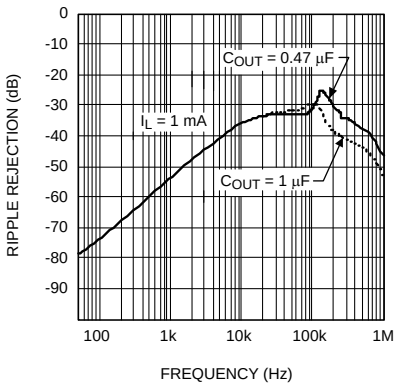


Figure 9. Power Supply Rejection Ratio

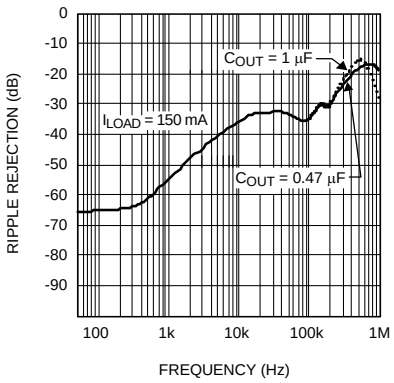


Figure 10. Power Supply Rejection Ratio

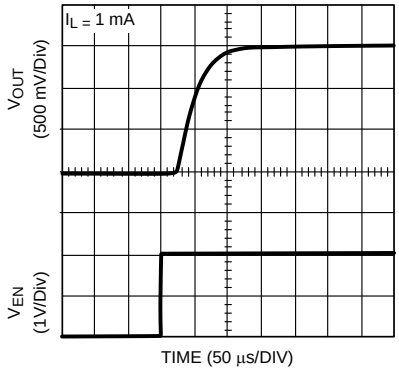


Figure 11. Enable Start-Up Time

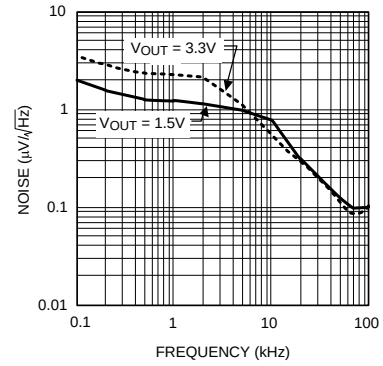


Figure 12. Noise Density

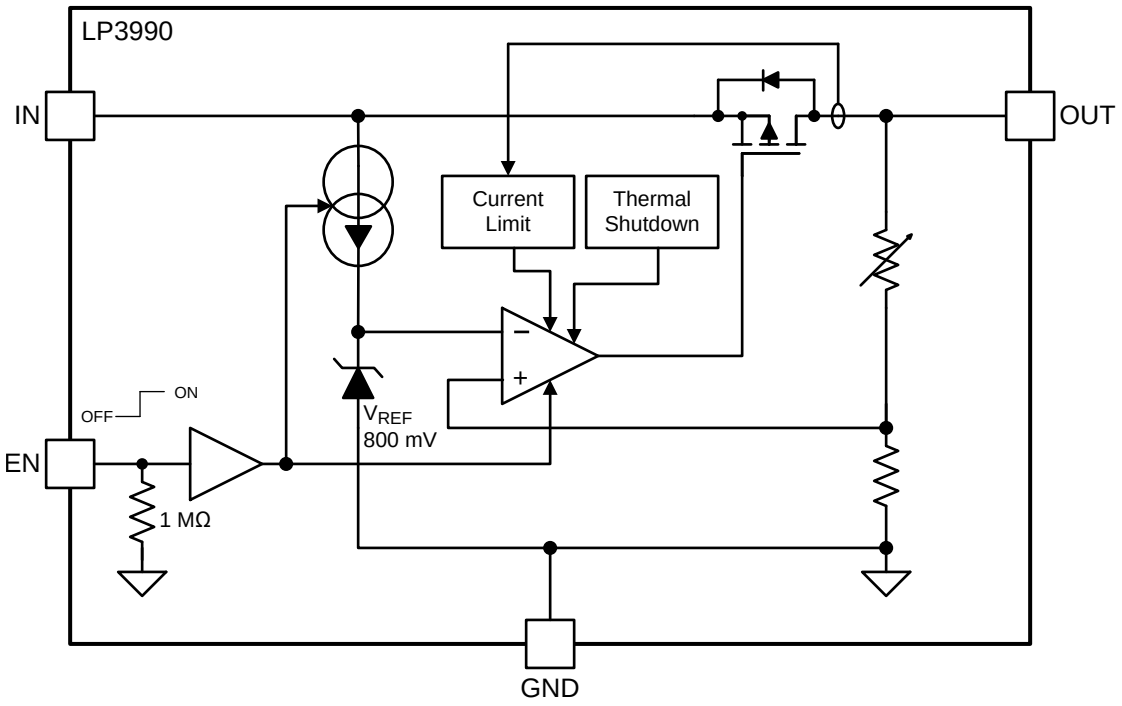
7 Detailed Description

7.1 Overview

Designed meet the requirements of portable, battery-powered digital systems providing an accurate output voltage with fast start-up. When disabled via a low logic signal at the enable pin (EN), the power consumption is reduced to virtually zero

The LP3990 is designed to perform with a single 1-µF input capacitor and a single 1-µF ceramic output capacitor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable (EN)

The LP3990 Enable (EN) pin is internally held low by a 1-MΩ resistor to GND. The EN pin voltage must be higher than the V_{IH} threshold to ensure that the device is fully enabled under all operating conditions. The EN pin voltage must be lower than the V_{IL} threshold to ensure that the device is fully disabled. If the EN pin is left open the LP3990 output will be disabled.

7.3.2 Thermal Overload Protection (T_{SD})

Thermal Shutdown disables the output when the junction temperature rises to approximately 155°C which allows the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The Thermal Shutdown circuitry of the LP3990 has been designed to protect against temporary thermal overload conditions. The Thermal Shutdown circuitry was not intended to replace proper heat-sinking. Continuously running the LP3990 device into thermal shutdown may degrade device reliability.

7.4 Device Functional Modes

7.4.1 Enable (EN)

The LP3990 EN pin is internally held low by a 1-MΩ resistor to GND. The EN pin voltage must be higher than the V_{IH} threshold to ensure that the device is fully enabled under all operating conditions.

7.4.2 Minimum Operating Input Voltage (V_{IN})

The LP3990 does not include any dedicated UVLO circuitry. The LP3990 internal circuitry is not fully functional until V_{IN} is at least 2 V. The output voltage is not regulated until $V_{IN} \geq (V_{OUT} + V_{DO})$, or 2 V, whichever is higher.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP3990 is a linear voltage regulator for digital applications designed to be stable with space-saving ceramic capacitors as small as 1 µF.

8.2 Typical Application

Figure 13 shows the typical application circuit for the LP3990. The input and output capacitances may need to be increased above the 1 µF shown for some applications.

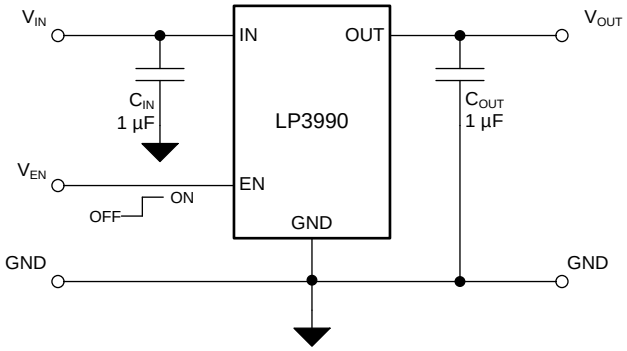


Figure 13. LP3990 Typical Application

8.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2 V to 6 V
Output voltage	1.8 V
Output current	100 mA
Output capacitor range	1 µF
Input/output capacitor ESR range	5 mΩ to 500 mΩ

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Available input voltage range
- Output voltage needed
- Output current needed
- Input and output capacitors

8.2.2.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum allowable power dissipation for the device in a given package can be calculated using Equation 1:

$$P_{D\text{-}MAX} = ((T_{J\text{-}MAX} - T_A) / R_{\theta JA}) \quad (1)$$

The actual power being dissipated in the device can be represented by Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

These two equations establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation (P_D) and/or excellent package thermal resistance ($R_{\theta JA}$) is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) may be increased.

In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) may have to be derated. $T_{A\text{-}MAX}$ is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum allowable power dissipation in the device package in the application ($P_{D\text{-}MAX}$), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by Equation 3:

$$T_{A\text{-}MAX} = (T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})) \quad (3)$$

Alternately, if $T_{A\text{-}MAX}$ can not be derated, the P_D value must be reduced. This can be accomplished by reducing V_{IN} in the 'V_{IN}–V_{OUT}' term as long as the minimum V_{IN} is met, or by reducing the I_{OUT} term, or by some combination of the two.

8.2.2.2 External Capacitors

In common with most regulators, the LP3990 requires external capacitors for regulator stability. The LP3990 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

8.2.2.3 Input Capacitor

An input capacitor is required for stability. It is recommended that a 1-µF capacitor be connected between the LP3990 IN pin and GND pin (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the IN pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: To ensure stable operation it is essential that good PCB design practices are employed to minimize ground impedance and keep input inductance low. If these conditions cannot be met, or if long leads are used to connect the battery or other power source to the LP3990, then it is recommended that the input capacitor is increased. Also, tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain approximately 1 µF over the entire operating temperature range.

8.2.2.4 Output Capacitor

The LP3990 is designed specifically to work with very small ceramic output capacitors. A 1-µF ceramic capacitor (temperature types Z5U, Y5V or X7R/X5R) with ESR between 5 mΩ to 500 mΩ, is suitable in the LP3990 application circuit.

For this device the output capacitor should be connected between the OUT pin and GND pin.

It is also possible to use tantalum or film capacitors at the device output, but these are not as attractive for reasons of size and cost (see *Capacitor Characteristics*).

The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the range 5 mΩ to 500 mΩ for stability.

8.2.2.5 No-Load Stability

The LP3990 will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

8.2.2.6 Capacitor Characteristics

The LP3990 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 0.47 µF to 4.7 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1-µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LP3990.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly, depending on the operating conditions and capacitor type.

In particular, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application. The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size, with smaller sizes giving poorer performance figures in general. As an example, Figure 14 shows a typical graph comparing different capacitor case sizes in a Capacitance vs. DC Bias plot. As shown in the graph, increasing the DC Bias condition can result in the capacitance value falling below the minimum value given in the recommended capacitor specifications table (0.7 µF in this case). Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (for example, 0402) may not be suitable in the actual application.

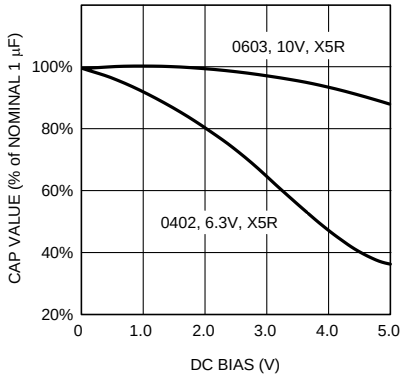


Figure 14. Graph Showing A Typical Variation In Capacitance vs DC Bias

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of –55°C to 125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of –55°C to 85°C. Many large value ceramic capacitors, larger than 1 µF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore, X7R and X5R types are recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47-µF to 4.7-µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed.

8.2.2.7 Enable Control

The LP3990 features an active high Enable pin, EN, which turns the device on when pulled high. When not enabled the regulator output is off and the device typically consumes 2 nA.

If the application does not require the Enable switching feature, the EN pin should be tied to V_{IN} to keep the regulator output permanently on.

To ensure proper operation, the signal source used to drive the EN input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the *Electrical Characteristics* section under V_{IL} and V_{IH}.

An internal 1-MΩ pull-down resistor ties the EN input to ground, ensuring that the device remains off if the EN pin is left open circuit.

8.2.3 Application Curves

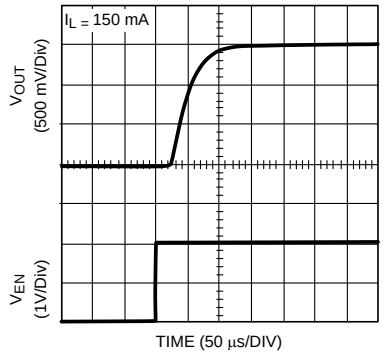


Figure 15. Enable Start-Up Time

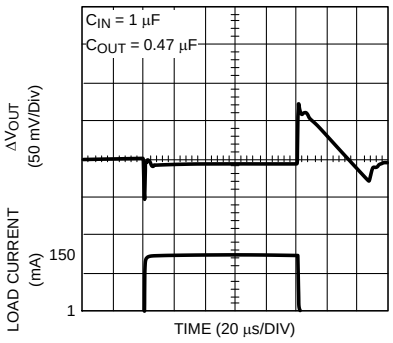


Figure 16. Load Transient

9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 2 V to 6 V. The input supply should be well regulated and free of spurious noise. To ensure that the LP3990 output voltage is well regulated, the input supply should be at least V_{OUT} + 0.5 V, or 2 V, whichever is higher. A minimum capacitor value of 1-µF is required to be within 1 cm of the IN pin.

10 Layout

10.1 Layout Guidelines

The dynamic performance of the LP3990 is dependant on the layout of the PCB. PCB layout practices that are adequate for typical LDO's may degrade the load regulation, PSRR, noise, or transient performance of the LP3990.

Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LP3990, and as close as is practical to the package. The ground connections for C_{IN} and C_{OUT} should be back to the LP3990 ground pin using as wide, and as short, of a copper trace as is practical.

Connections using long trace lengths, narrow trace widths, and/or connections through vias should be avoided. These will add parasitic inductances and resistance that results in inferior performance especially during transient conditions.

A Ground Plane, either on the opposite side of a two-layer PCB, or embedded in a multi-layer PCB, is strongly recommended. This Ground Plane serves two purposes : 1) Provide a circuit reference plane to assure accuracy, and 2) provides a thermal plane to remove heat from the LP3990 WSON package through thermal vias under the package DAP.

10.2 Layout Examples

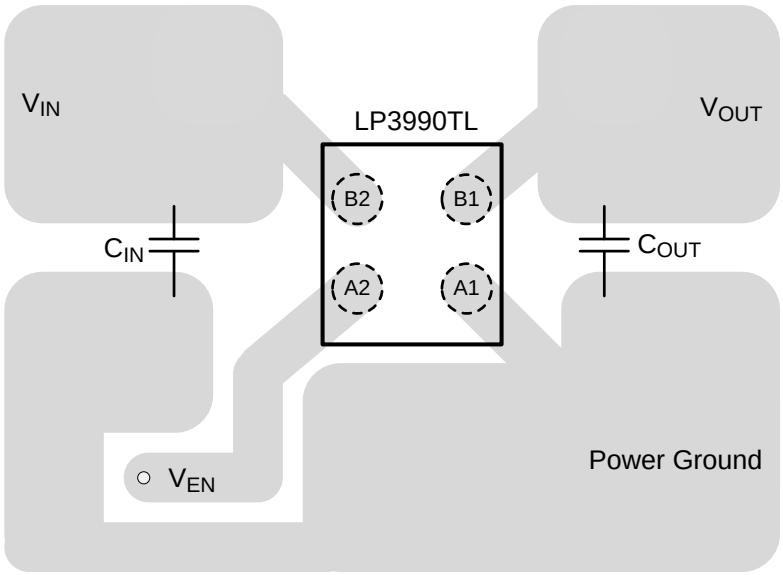


Figure 17. LP3990 DSBGA Layout

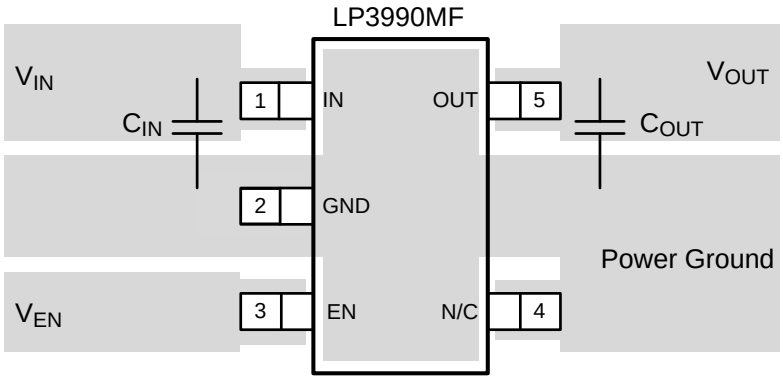


Figure 18. LP3990 SOT-23 Layout

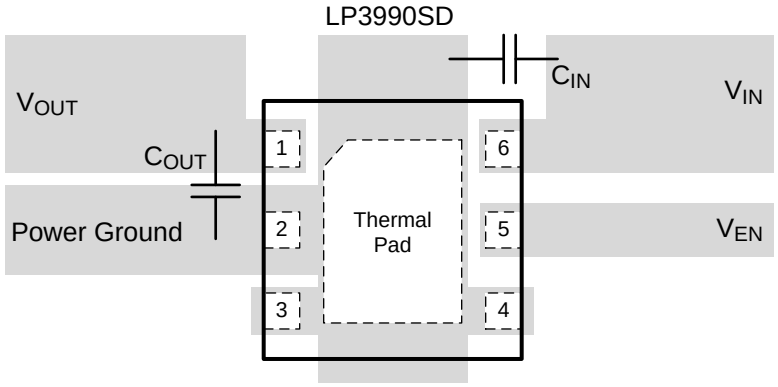


Figure 19. LP3990 WSON Layout

10.3 DSBGA Mounting

The DSBGA package requires specific mounting techniques, which are detailed in TI Application Note *DSBGA Wafer Level Chip Scale Package*SNVA009.

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

10.4 DSBGA Light Sensitivity

Exposing the DSBGA device to direct light may affect the operation of the device. Light sources, such as halogen lamps, can affect electrical performance, if placed in close proximity to the device.

Light with wavelengths in the infra-red portion of the spectrum is the most detrimental, and so, fluorescent lighting used inside most buildings, has little or no effect on performance.

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3990MF-1.2/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SCDB	Samples
LP3990MF-1.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SCFB	Samples
LP3990MF-2.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SCJB	Samples
LP3990MF-2.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SCKB	Samples
LP3990MF-3.3/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SCLB	Samples
LP3990MFX-1.2/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SCDB	Samples
LP3990MFX-1.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SCFB	Samples
LP3990MFX-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SCLB	Samples
LP3990SD-1.2/NOPB	ACTIVE	WSON	NGG	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L086B	Samples
LP3990SD-1.5/NOPB	ACTIVE	WSON	NGG	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L087B	Samples
LP3990SD-1.8/NOPB	ACTIVE	WSON	NGG	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L088B	Samples
LP3990TL-0.8/NOPB	ACTIVE	DSBGA	YZR	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3990TL-1.2/NOPB	ACTIVE	DSBGA	YZR	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3990TL-1.35/NOPB	ACTIVE	DSBGA	YZR	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3990TL-1.5/NOPB	ACTIVE	DSBGA	YZR	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3990TL-1.8/NOPB	ACTIVE	DSBGA	YZR	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3990TL-2.5/NOPB	ACTIVE	DSBGA	YZR	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3990TL-2.8/NOPB	ACTIVE	DSBGA	YZR	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3990TLX-0.8/NOPB	ACTIVE	DSBGA	YZR	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3990TLX-1.2/NOPB	ACTIVE	DSBGA	YZR	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3990TLX-1.5/NOPB	ACTIVE	DSBGA	YZR	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3990TLX-1.8/NOPB	ACTIVE	DSBGA	YZR	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3990TLX-2.5/NOPB	ACTIVE	DSBGA	YZR	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3990TLX-2.8/NOPB	ACTIVE	DSBGA	YZR	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LP3990 :

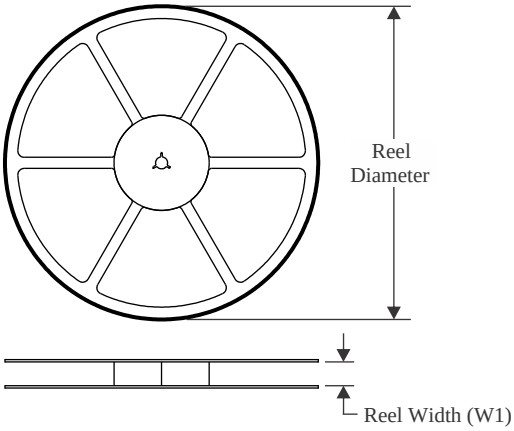
- Automotive: LP3990-Q1

NOTE: Qualified Version Definitions:

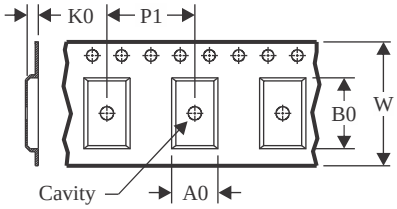
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

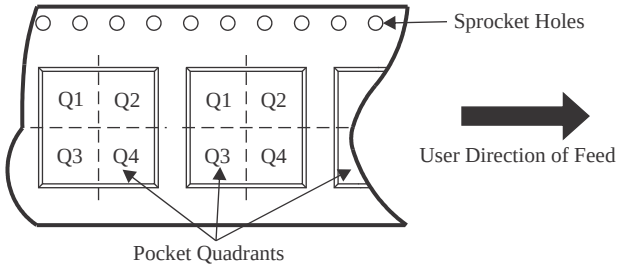


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

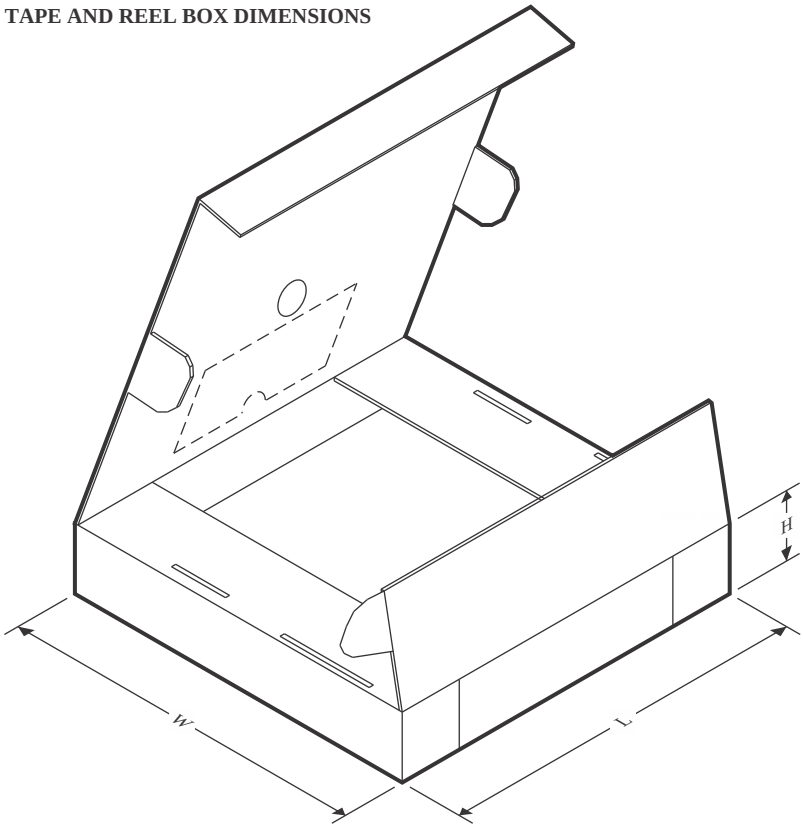


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3990MF-1.2/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MF-1.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MF-2.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MF-2.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MF-3.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MFX-1.2/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MFX-1.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MFX-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990SD-1.2/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP3990SD-1.5/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP3990SD-1.8/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP3990TL-0.8/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TL-1.2/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TL-1.35/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TL-1.5/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TL-1.8/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3990TL-2.5/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TL-2.8/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TLX-0.8/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TLX-1.2/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TLX-1.5/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TLX-1.8/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TLX-2.5/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TLX-2.8/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3990MF-1.2/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP3990MF-1.8/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP3990MF-2.5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP3990MF-2.8/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP3990MF-3.3/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP3990MFX-1.2/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP3990MFX-1.8/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP3990MFX-3.3/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP3990SD-1.2/NOPB	WSON	NGG	6	1000	208.0	191.0	35.0
LP3990SD-1.5/NOPB	WSON	NGG	6	1000	208.0	191.0	35.0
LP3990SD-1.8/NOPB	WSON	NGG	6	1000	208.0	191.0	35.0
LP3990TL-0.8/NOPB	DSBGA	YZR	4	250	208.0	191.0	35.0
LP3990TL-1.2/NOPB	DSBGA	YZR	4	250	208.0	191.0	35.0
LP3990TL-1.35/NOPB	DSBGA	YZR	4	250	208.0	191.0	35.0
LP3990TL-1.5/NOPB	DSBGA	YZR	4	250	208.0	191.0	35.0
LP3990TL-1.8/NOPB	DSBGA	YZR	4	250	208.0	191.0	35.0
LP3990TL-2.5/NOPB	DSBGA	YZR	4	250	208.0	191.0	35.0
LP3990TL-2.8/NOPB	DSBGA	YZR	4	250	208.0	191.0	35.0

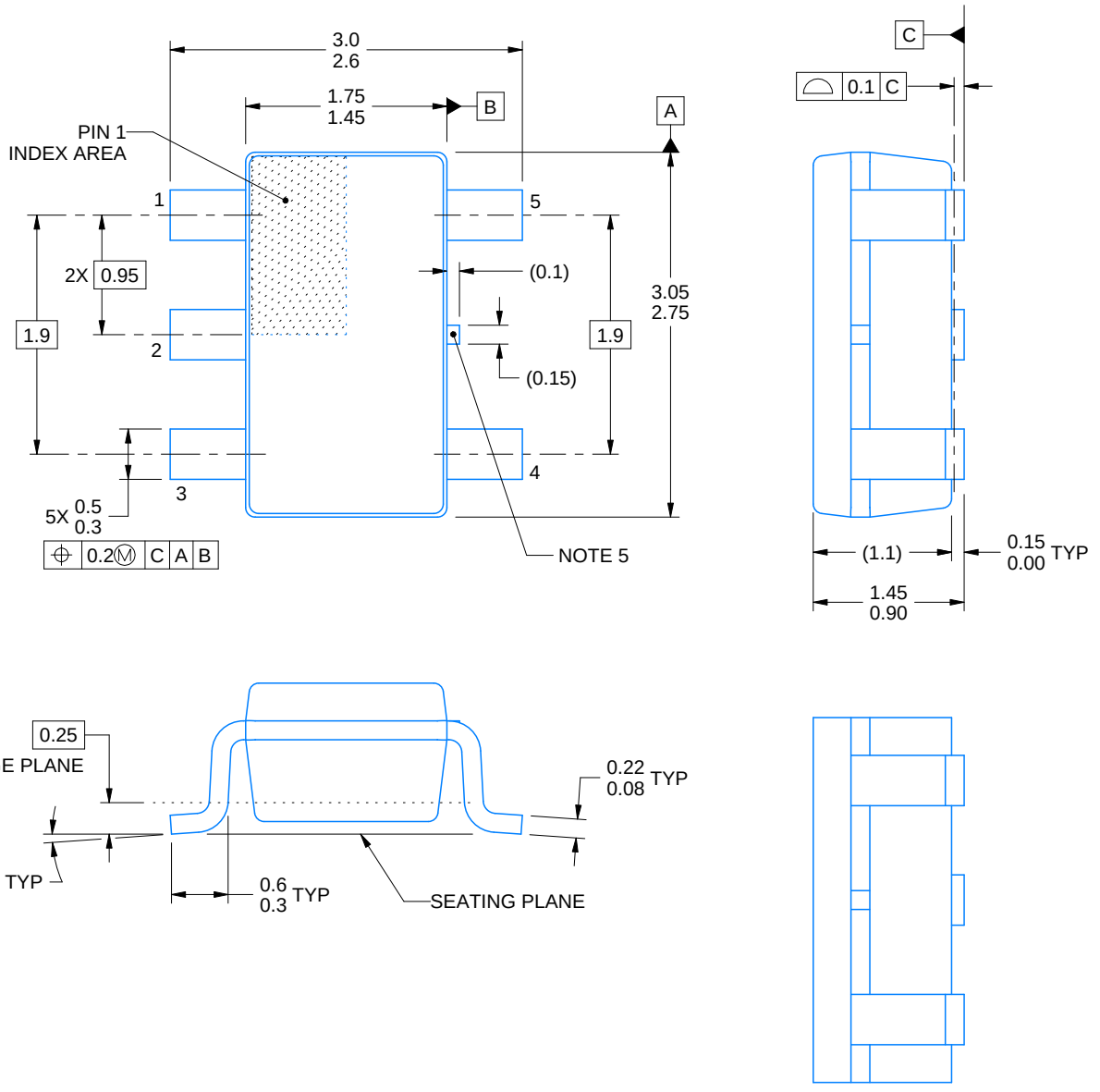
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3990TLX-0.8/NOPB	DSBGA	YZR	4	3000	208.0	191.0	35.0
LP3990TLX-1.2/NOPB	DSBGA	YZR	4	3000	208.0	191.0	35.0
LP3990TLX-1.5/NOPB	DSBGA	YZR	4	3000	208.0	191.0	35.0
LP3990TLX-1.8/NOPB	DSBGA	YZR	4	3000	208.0	191.0	35.0
LP3990TLX-2.5/NOPB	DSBGA	YZR	4	3000	208.0	191.0	35.0
LP3990TLX-2.8/NOPB	DSBGA	YZR	4	3000	208.0	191.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

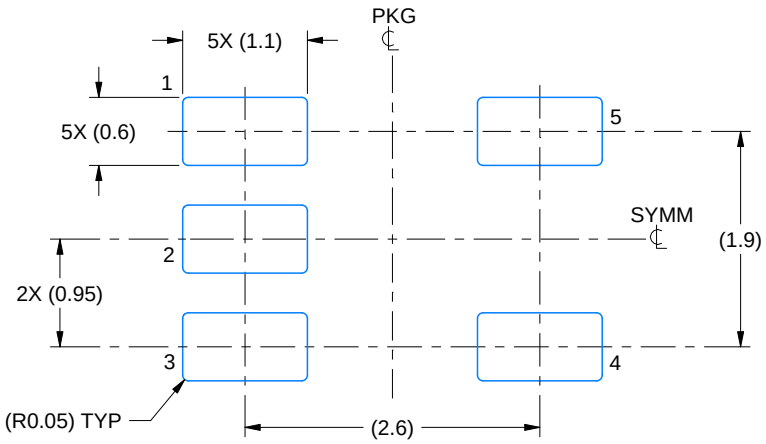


ALTERNATIVE PACKAGE SINGULATION VIEW

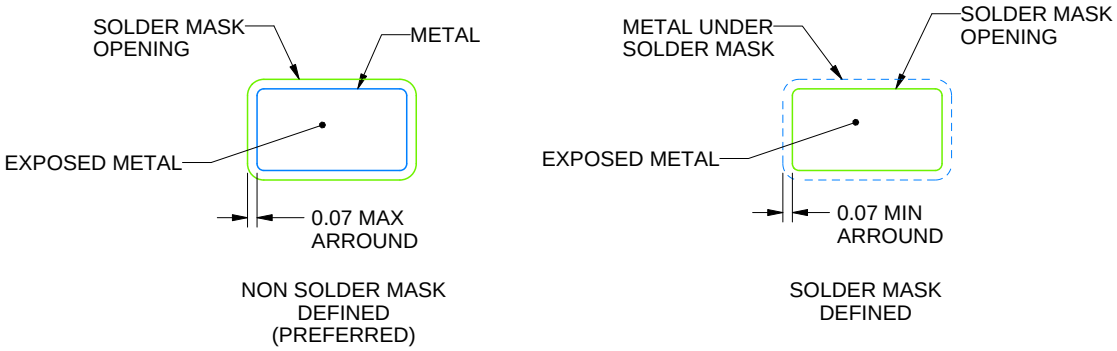
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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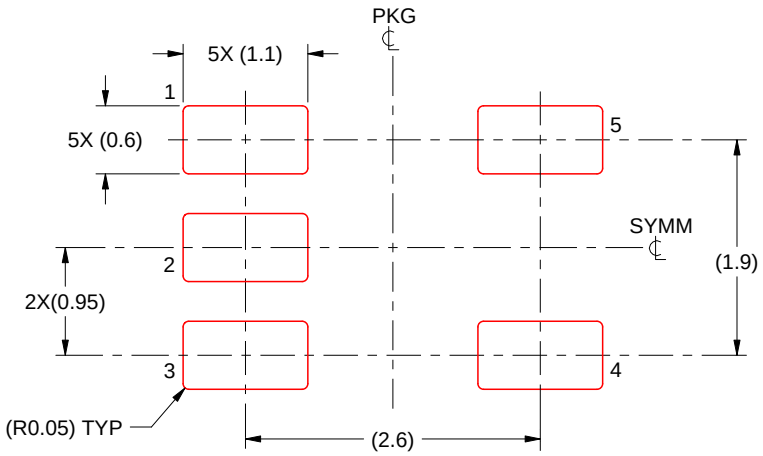
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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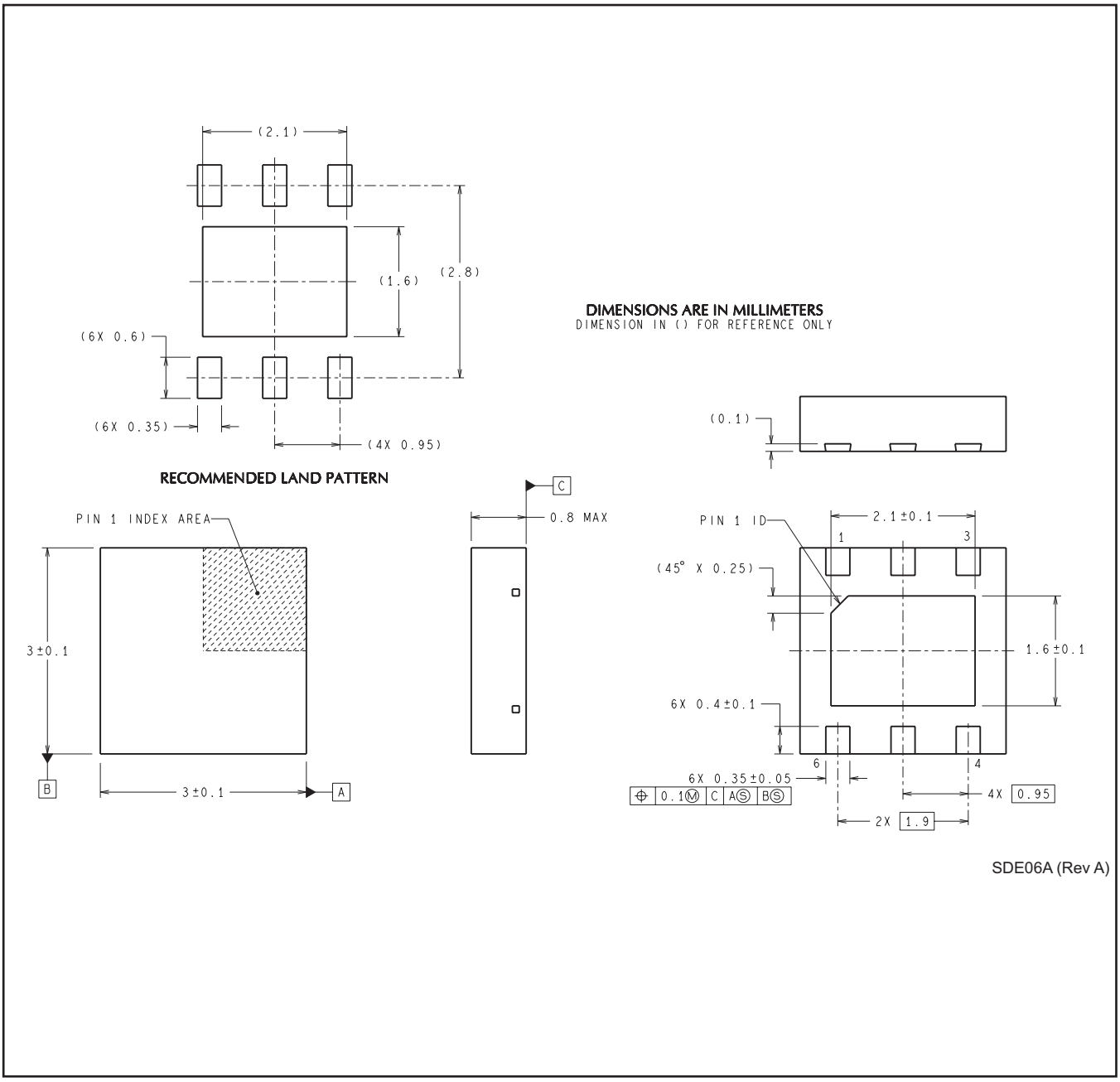
NOTES: (continued)

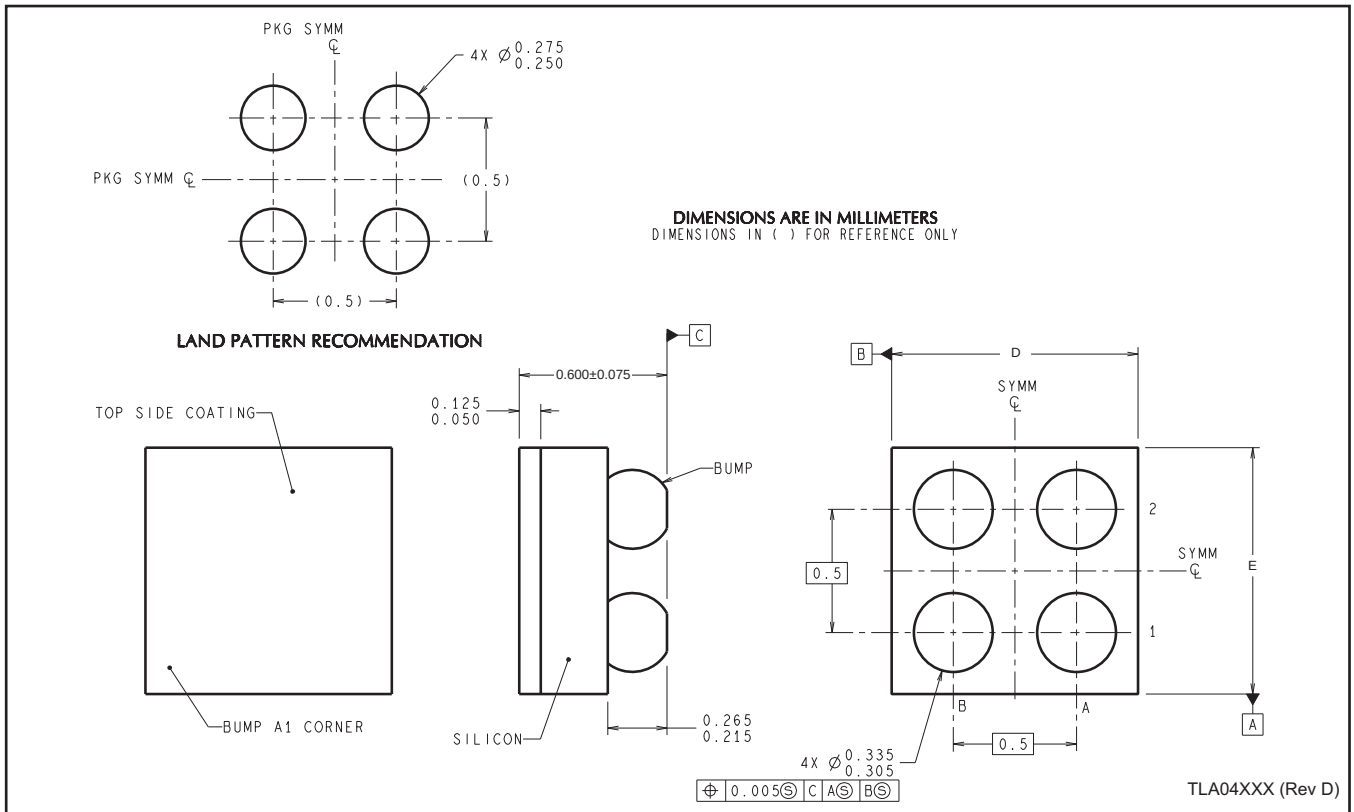
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

NGG0006A



SDE06A (Rev A)

YZR0004



D: Max = 1.324 mm, Min =1.263 mm

E: Max = 1.045 mm, Min =0.984 mm

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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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