



# THE DATASHEET OF LP8725TLE-B/NOPB

## LP8725 Power Management Unit for Application or Multimedia Processors and Subsystems

Check for Samples: [LP8725](#)

### FEATURES

- Two High-Efficiency Step-Down DC-DC Converters,  $I_{OUT} = 600\text{ mA}$ , With a 4-MHz Switching Frequency Using Small 1- $\mu\text{H}$  Inductors, With Options up to 800 mA
- Three Digital LDOs for up to 300-mA Load Current Each
- Two Low-Noise Analog 300-mA LDOs
- Two Low-Input Low-Output Regulators,  $I_{OUT} = 300\text{ mA}$
- I<sup>2</sup>C-Compatible Interface for Control of Internal Registers
- Adjustable Startup Sequence Through Serial Interface or Configuration
- Thermal Shutdown Protection

### APPLICATIONS

- Multimedia Processors
- Portable Handheld Products

### KEY SPECIFICATIONS

- 190 mV typ. Dropout Voltage on digital LDOs @ 300 mA
- 2% typ. Output Voltage Accuracy on digital and analog LDOs
- 10  $\mu\text{Vrms}$  Output Noise on analog LDOs
- $\pm 2\%$  typ. Output Voltage Bucks up to 93% efficiency
- 30-bump DSBGA package (0.5 mm pitch)

### DESCRIPTION

This device is a multi-function programmable Power Management Unit (PMU), optimized for sub block power solutions. This device integrates two highly efficient 600-mA step-down DC-DC converters configurable up to 800-mA load with Dynamic Voltage Scaling (DVS) via the serial interface, two low-noise analog LDOs, three digital LDOs for up to 300 mA load current each, two Low-Input Low-Output (LILO) regulators, and an I<sup>2</sup>C-compatible serial interface to allow a host controller access to the internal control registers. The device also features programmable power-on sequencing. LDO regulators provide high PSRR and low noise ideally suited for supplying power to both analog and digital loads.

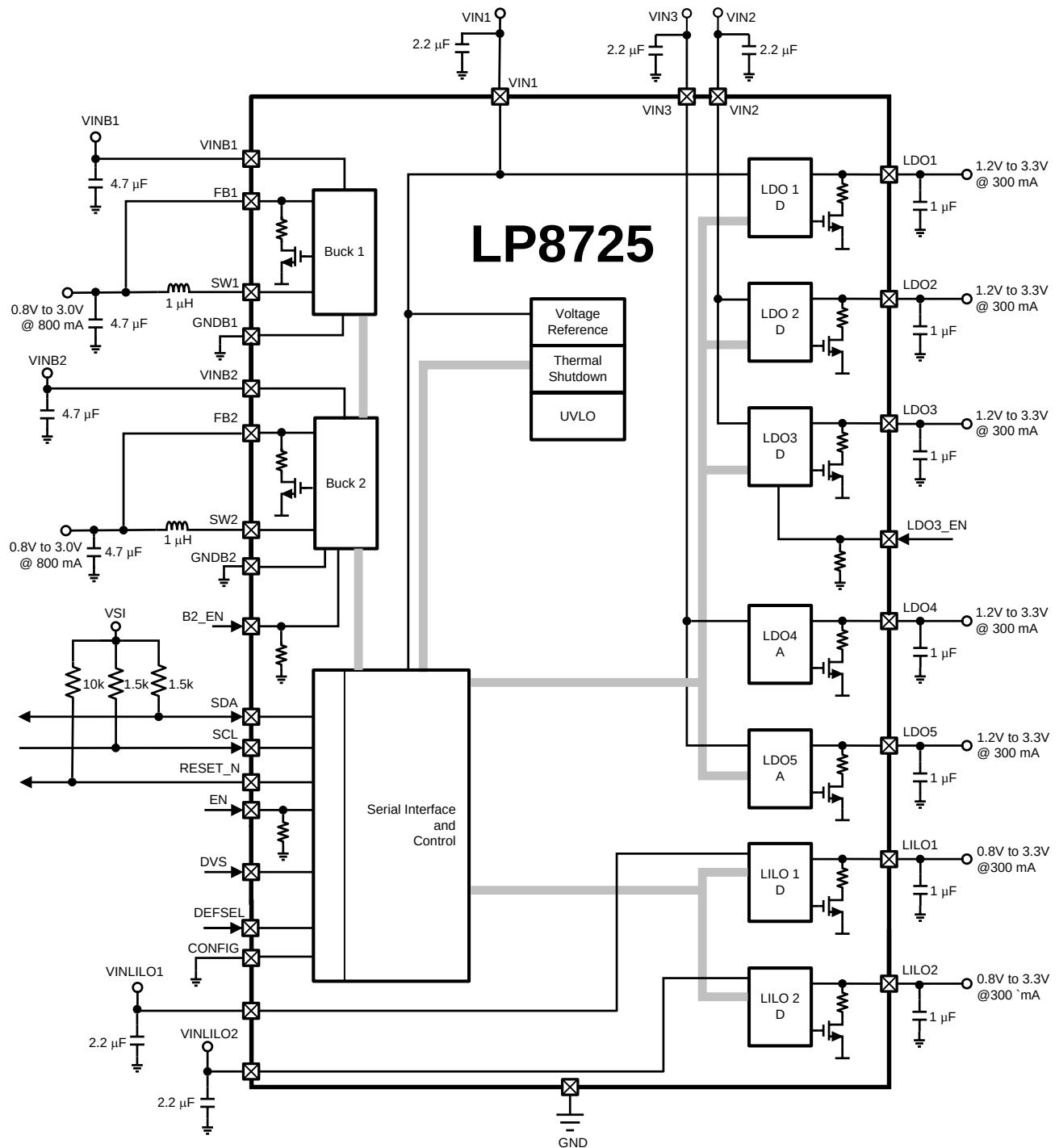
The device can be configured either as a Sub\_PMU for modules (for example, camera or multimedia modules) or as a stand-alone PMU that powers the processor itself.



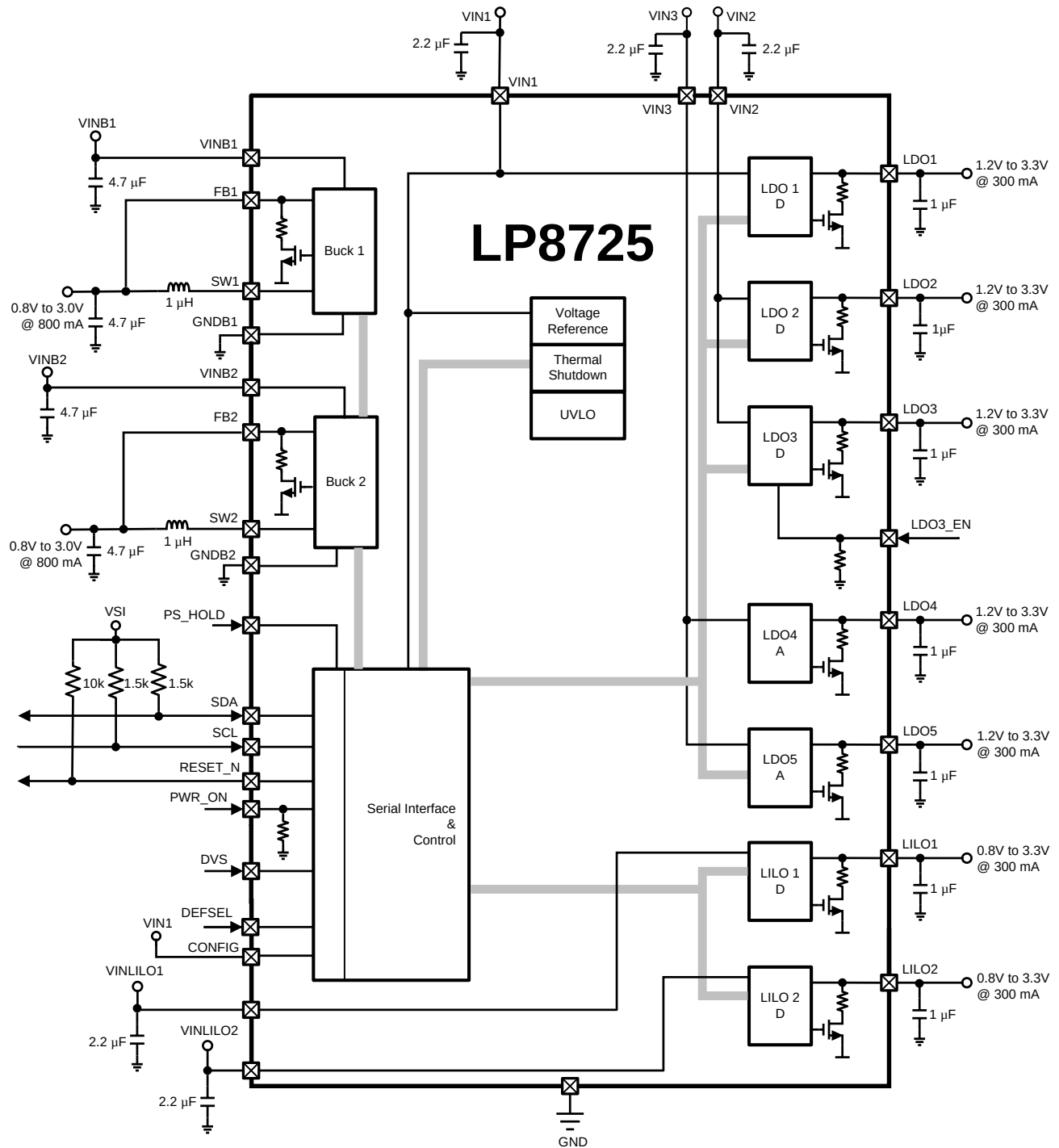
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

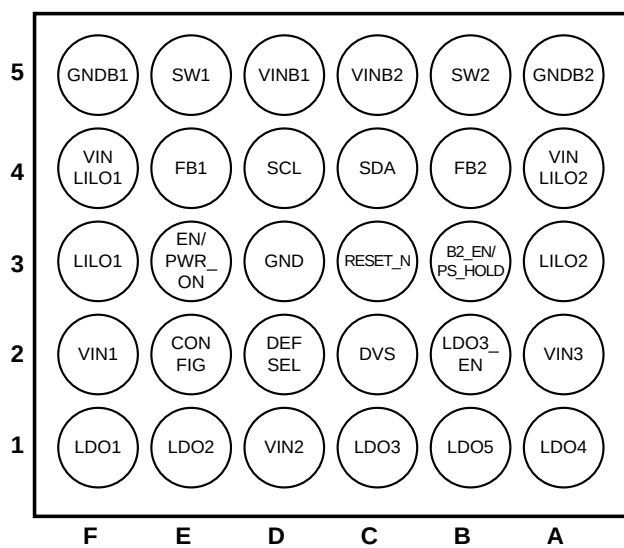
## TYPICAL APPLICATION (SUB-PMU)



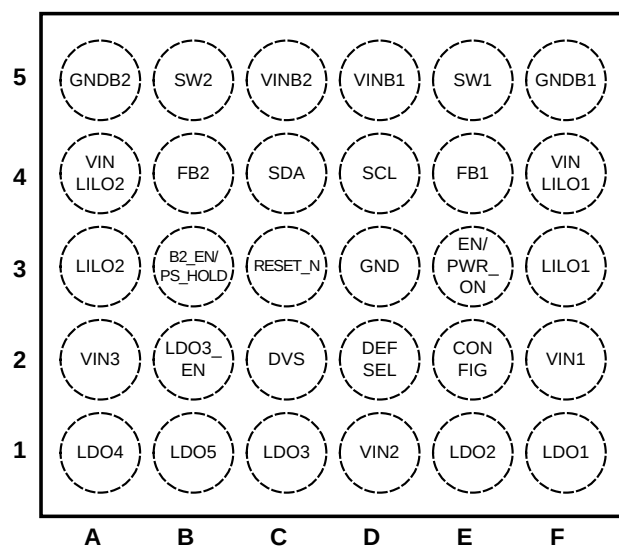
## TYPICAL APPLICATION (PMU)



## CONNECTION DIAGRAMS



Bottom View



Top View

### PIN DESCRIPTIONS

| Name          | Pin No. | Description                                                                                                                                                                                                                                                                                            |
|---------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| B2_EN/PS_HOLD | B3      | CONFIG=0: B2_EN is the enable for BUCK2 output if this pin is high and if BUCK2_EN register bit is set to 0. (B2_EN and the register bit are logical OR.) Internal 500 kΩ pull-down resistor in this configuration only.<br>CONFIG=1: PS_HOLD is a power supply hold input from an external processor. |
| CONFIG        | E2      | Connect to GND for SUB_PMU or connect to VIN1 for PMU.                                                                                                                                                                                                                                                 |
| DEFSEL        | D2      | Control input that sets default voltages and start-up sequence. Must be hard wired to VIN1 or GND for specific application.<br>When DEFSEL=VIN1 then setup 1 is used for default voltages and startup sequences.<br>When DEFSEL=GND then setup 2 is used for default voltages and startup sequences.   |
| DVS           | C2      | Dynamic Voltage Scaling (operational when REG 0x00<2> is '0').<br>DVS=1 then BUCK voltage set BUCK1_V1 is in use.<br>DVS=0 then BUCK voltage set BUCK1_V2 is in use.<br>This pin must be driven to its logic high or low whenever the BUCK1 or BUCK2 outputs are enabled.                              |
| EN/PWR_ON     | E3      | CONFIG=0: EN=1 turns on outputs or standby mode if EN=0.<br>CONFIG=1: PWR_ON=1 starts power up sequence after 30 ms of de-bounce time. Internal 500K pull-down resistor.                                                                                                                               |
| FB1           | E4      | BUCK1 Feedback. Active pull-down when BUCK1 turns off.                                                                                                                                                                                                                                                 |
| FB2           | B4      | BUCK2 Feedback. Active pull-down when BUCK2 turns off.                                                                                                                                                                                                                                                 |
| GND           | D3      | IC Ground                                                                                                                                                                                                                                                                                              |
| GNDB1         | F5      | BUCK1 Ground.                                                                                                                                                                                                                                                                                          |
| GNDB2         | A5      | BUCK2 Ground.                                                                                                                                                                                                                                                                                          |
| LDO1          | F1      | LDO1 output.                                                                                                                                                                                                                                                                                           |
| LDO2          | E1      | LDO2 output.                                                                                                                                                                                                                                                                                           |
| LDO3          | C1      | LDO3 output.                                                                                                                                                                                                                                                                                           |
| LDO3_EN       | B2      | Enable for LDO3 output if this pin is high and if LDO3_EN register bit is set to 0. (LDO3_EN and the register bit are logical OR.) Internal 500 kΩ pull-down resistor.                                                                                                                                 |
| LDO4          | A1      | LDO4 output.                                                                                                                                                                                                                                                                                           |
| LDO5          | B1      | LDO5 output                                                                                                                                                                                                                                                                                            |
| LIL01         | F3      | LIL01 output.                                                                                                                                                                                                                                                                                          |
| LIL02         | A3      | LIL02 output.                                                                                                                                                                                                                                                                                          |
| RESET_N       | C3      | CONFIG=0: Goes high typ. 30 ms after EN=1 and goes low when EN=0.<br>CONFIG=1: Goes high typ. 60 ms after PWR_ON=1 and goes low 30 ms after PS_HOLD=0.<br>External pull-up resistor is needed, typical 10 kΩ.                                                                                          |
| SCL           | D4      | Serial Interface Clock Input. External pull-up resistor is needed, typical 1.5 kΩ.                                                                                                                                                                                                                     |
| SDA           | C4      | Serial Interface Data Input/Output. Open Drain output, external pull-up resistor is needed, typical 1.5 kΩ.                                                                                                                                                                                            |
| SW1           | E5      | BUCK1 Switch node of DC-DC converter BUCK1.                                                                                                                                                                                                                                                            |
| SW2           | B5      | BUCK2 Switch node of DC-DC converter BUCK2.                                                                                                                                                                                                                                                            |
| VIN1          | F2      | Input for LDO1.                                                                                                                                                                                                                                                                                        |
| VINB1         | D5      | Input for BUCK1.                                                                                                                                                                                                                                                                                       |
| VIN2          | D1      | Input for LDO2 and LDO3.                                                                                                                                                                                                                                                                               |
| VINB2         | C5      | Input for BUCK2.                                                                                                                                                                                                                                                                                       |
| VIN3          | A2      | Input for LDO4 and LDO5.                                                                                                                                                                                                                                                                               |
| VINLIL01      | F4      | Input for LIL01.                                                                                                                                                                                                                                                                                       |
| VINLIL02      | A4      | Input for LIL02.                                                                                                                                                                                                                                                                                       |



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## DEVICE DESCRIPTION

### Operation Modes

**POWER-ON-RESET:** In SUB\_PMU configuration - After VIN1 goes above UVLO high threshold, then all internal registers of LP8725 are reset to the default values from the DEFSEL setting, after which LP8725 goes to STANDBY mode. In PMU configuration - When PWR\_ON goes high while VIN1 is above the UVLO high threshold, all internal registers of LP8725 are reset to the default values from the DEFSEL setting. This process duration max is typically 500  $\mu$ s.

**STANDBY:** In STANDBY mode only serial interface is working and all other PMU functions are disabled – PMU is in low-power condition. In STANDBY mode LP8725 can be (re)configured via Serial Interface. The LP8725 only enters STANDBY mode automatically in SUB\_PMU configuration.

**STARTUP:** STARTUP sequence is defined by registers contents. STARTUP sequence starts:

- 1) If rising edge on EN-pin in SUB\_PMU configuration.
- 2) After cooling down from thermal shutdown event if EN=1 in SUB\_PMU configuration.
- 3) If PWR\_ON is still high after 30 ms (typical de-bounce time) in PMU configuration. It is not recommended to write to LP8725 registers during STARTUP. If doing so then current STARTUP sequence may become undefined.

In SUB\_PMU configuration RESET\_N is de-asserted 30 ms (typical) after EN=1. In PMU configuration RESET\_N is de-asserted a further 30 ms (typical) after PWR\_ON de-bounce time has ended.

It is not recommended to write to LP8725 registers during startup. If doing so then current STARTUP sequence may become undefined.

**IDLE:** The LP8725 will enter into IDLE mode (normal operating mode) after end of startup sequence. In IDLE mode all LDOs and BUCK can be enabled/disabled via Serial Interface. Also in IDLE mode the LP8725 can be (re)configured via Serial Interface.

**SHUTDOWN:** SHUTDOWN sequence follows the reverse order of the startup sequence defined by registers contents:

- 1) If falling edge on EN-pin in SUB\_PMU configuration.
- 2) If PS\_HOLD and PWR\_ON both go low for typically 30 ms in PMU configuration. Device immediately shuts down if the temperature exceeds thermal shutdown threshold TSD +160°C.

RESET\_N is asserted when the device starts to shut down.

It is not recommended to write to LP8725 registers during SHUT DOWN. If doing so then current SHUTDOWN sequence may become undefined.

In SUB\_PMU configuration the device shuts down to STANDBY mode.

In PMU configuration the device shuts down completely (so registers will be reset on next PWR\_ON high).

**SLEEP:** The load current for each of the LDO outputs should be no greater than 5mA when the device is put into SLEEP mode. In Sleep mode Ground current is minimized. SLEEP mode is controlled by the serial interface, Register 0x00 bit 1.

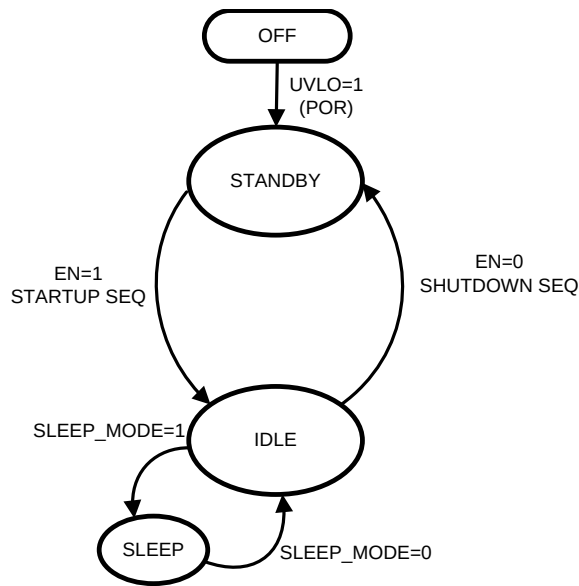
SLEEP Mode is controlled by the Serial Interface.

**Table 1. Application Configuration<sup>(1)(2)</sup>**

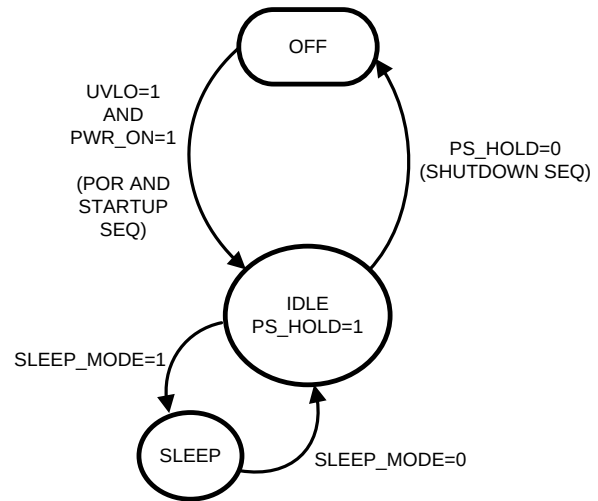
| CONFIG | Application | Pin B3 Function | Pin E3 Function | Slave Address, DEFSEL = 1 | Slave Address, DEFSEL = 0 |
|--------|-------------|-----------------|-----------------|---------------------------|---------------------------|
| GND    | SUB_PMU     | B2_EN           | EN              | 7h'78                     | 7h'7A                     |
| VIN1   | PMU         | PS_HOLD         | PWR_ON          | 7h'79                     | 7h'7B                     |

(1) The LP8725 and LP8725-A are both configured as either SUB\_PMU or PMU by the wiring of the CONFIG pin on the application of power to the device.

(2) These are dependent on whether DEFSEL is connected to VIN1 or GND when PWR\_ON/EN=1.



**Figure 1. SUB-PMU Mode, CONFIG = 0**



**Figure 2. PMU Mode, CONFIG = 1**

## Additional Functions

**DVS:** Dynamic Voltage Scaling allows using 2 set voltages for BUCKs. This is controlled via Serial Interface. BUCK1 can also be controlled by the external DVS pin.

**FAULT DETECTION** If BUCK1/BUCK2 and LDO1 are not masked then if one of the outputs is pulled down - e.g., short circuit, then RESET\_N is asserted (low)..

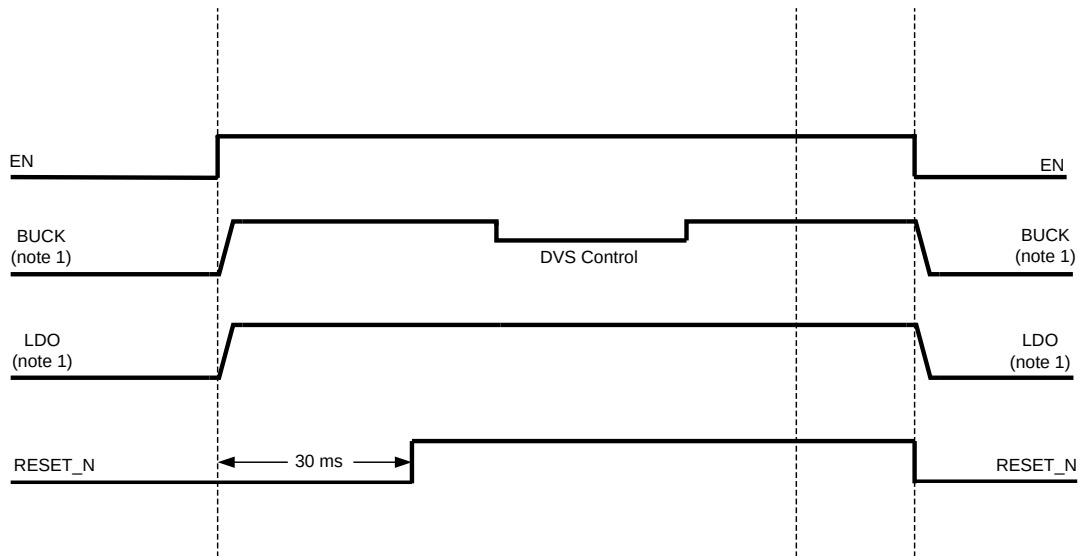
**Table 2. Default Start-Up Enable Sequence<sup>(1)</sup>**

| Part No. | DEFSEL         | Start-Up Sequence                                                                                         | Shut Down Sequence                     |
|----------|----------------|-----------------------------------------------------------------------------------------------------------|----------------------------------------|
| LP8725   | VIN1 (setup 1) | BUCK1 <b>then</b> BUCK2 and LILO2 <b>then</b> LDO1, LDO2, LDO4 and LDO5 <b>then</b> LDO3 and LILO1        | In reverse order of start-up sequence. |
| LP8725   | GND (setup 2)  | BUCK1 and LILO2 <b>then</b> BUCK2, LDO1, LDO2, LDO5 and LILO1 <b>then</b> LDO3 and LDO4.                  | In reverse order of start-up sequence. |
| LP8725-A | VIN1 (setup 1) | LDO1, LDO2, LDO5 and LILO1 <b>then</b> LDO4 and LILO2                                                     | In reverse order of start-up sequence. |
| LP8725-A | GND (setup 2)  | BUCK1 and BUCK2 <b>then</b> LDO2 and LDO3 <b>then</b> LDO1, LDO4 and LDO5 <b>then</b> LILO1 and LILO2     | In reverse order of start-up sequence. |
| LP8725-B | VIN1 or GND    | BUCK1 <b>then</b> BUCK2 <b>then</b> LDO1 <b>then</b> LILO2                                                | In reverse order of start-up sequence. |
| LP8725-C | VIN1 or GND    | BUCK1 <b>then</b> BUCK2 and LDO5 <b>then</b> LDO1 and LDO2 and LILO 1and LILO 2 <b>then</b> LDO3 and LDO4 | In reverse order of start-up sequence. |
| LP8725-D | VIN1 or GND    | BUCK1 <b>then</b> BUCK2, LDO3, LILO1 and LILO2                                                            | In reverse order of start-up sequence. |

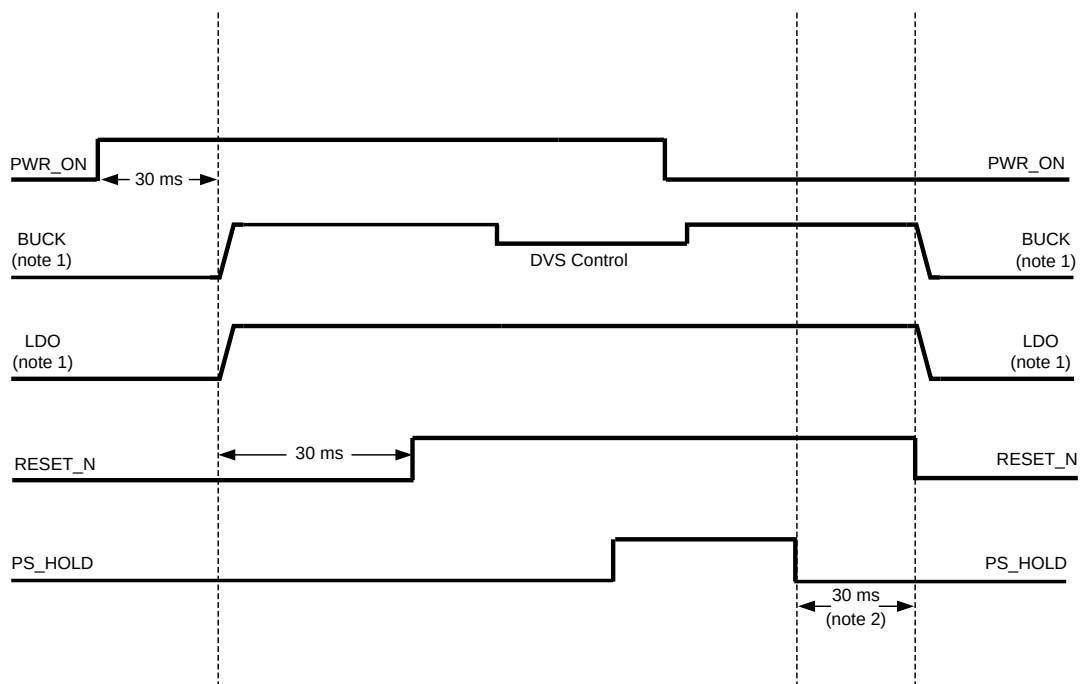
(1) These are dependent on whether DEFSEL is connected to VIN1 or GND when PWR\_ON/EN=1.



## Power On and Power Off Sequences



**Figure 3. Simplified startup Sequence if CONFIG=GND (SUB\_PMU)**



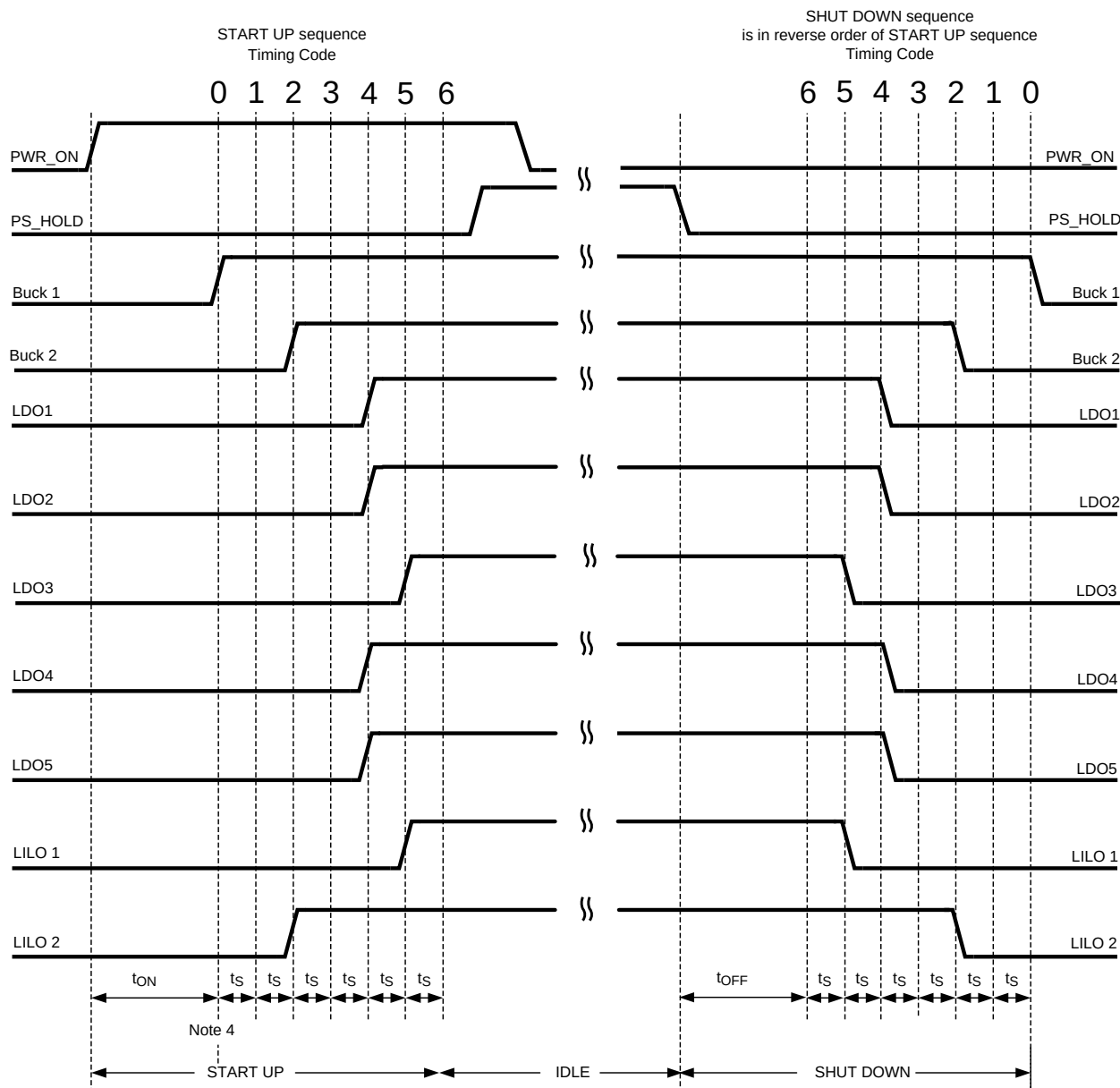
All timing is typical.

**Note 1** See detailed on/off sequence diagrams for the different DEFSEL options.

**Note 2** PS\_HOLD needs to be held low for >30 ms before RESET\_N is asserted low. PMU should then start shutdown sequence opposite of startup sequence.

**Figure 4. Simplified Startup Sequence if CONFIG=VIN1 (PMU)**

**Figure 5. LP8725 Startup and Shutdown Sequence if CONFIG=VIN1** Note 1, Note 2



All timing is typical.

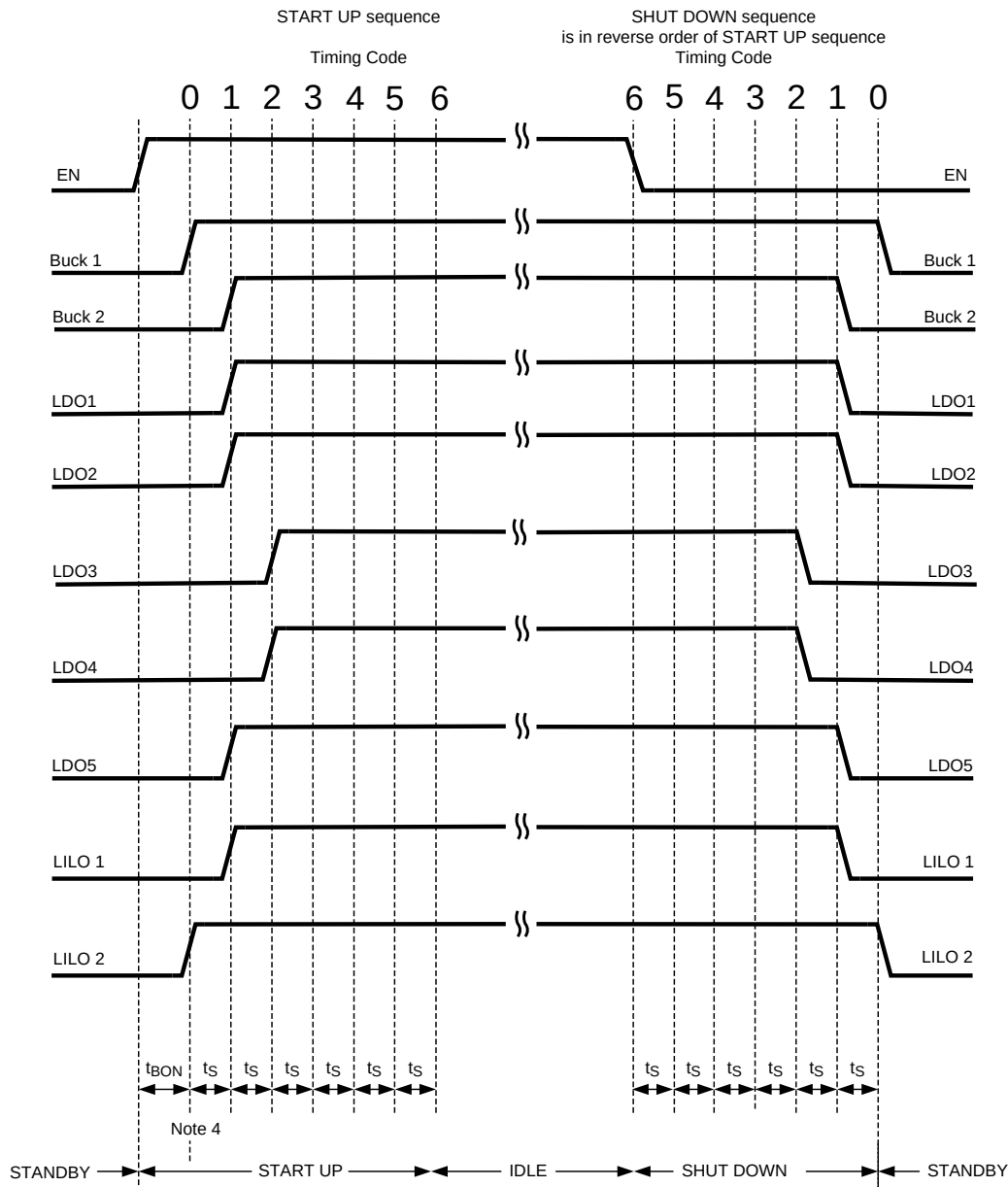
t<sub>ON/OFF</sub> 30 ms typ. de-bounce times

t<sub>s</sub> Programmable time steps. (Typically 64  $\mu$ s/step.) Time step accuracy is defined by OSC frequency accuracy.

**Note 1** STARTUP and SHUTDOWN sequences are defined by registers. Sequences given here are valid if there the registers are not rewritten via Serial Interface.

**Note 2** The timing showed here define time points when LDOs and BUCK are enabled/disabled. Enabling /disabling process duration depends on voltages and loading conditions. Buck startup duration is typically 170  $\mu$ s. LDO startup duration is typically 35  $\mu$ s. For details please see LDOs and BUCK Electrical Specifications.

**Note 4** At this time point registers are reset to POR default values.

**Figure 6. LP8725 Startup and Shutdown Sequence if CONFIG=GND, DEFSEL=GND** Note 1, Note 2


All timing is typical.

$t_{BON}$  75  $\mu$ s - Reference and bias turn ON.

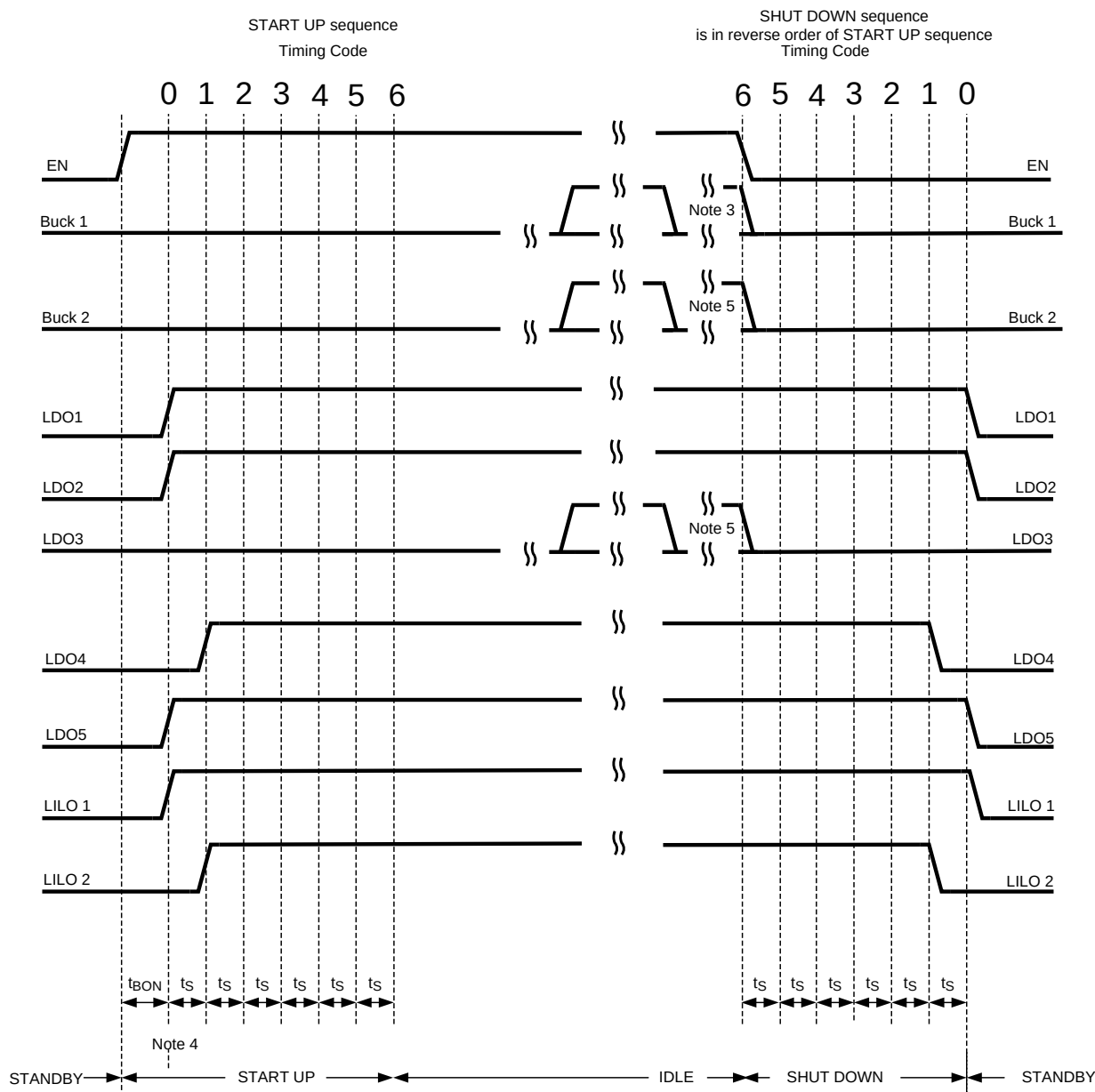
$t_s$  Programmable time steps. (**Typically 64  $\mu$ s/step.**) Time step accuracy is defined by OSC frequency accuracy.

**Note 1** STARTUP and SHUTDOWN sequences are defined by registers. Sequences given here are valid if there the registers are not rewritten via Serial Interface.

**Note 2** The timing showed here define time points when LDOs and BUCK are enabled/disabled. Enabling /disabling process duration depends on voltages and loading conditions. Buck startup duration is typically 170  $\mu$ s. LDO startup duration is typically 35  $\mu$ s. For details please see LDOs and BUCK Electrical Specifications.

**Note 4** At this time point registers are reset to POR default values.

Figure 7. LP8725-A Startup and Shutdown Sequence if CONFIG=GND, DEFSEL=VIN1 <sup>Note 1, Note 2</sup>



All timing is typical.

**t<sub>BON</sub>** 75 μs - Reference and bias turn ON.

**t<sub>s</sub>** Programmable time steps. (**Typically 64 μs/step.**) Time step accuracy is defined by OSC frequency accuracy.

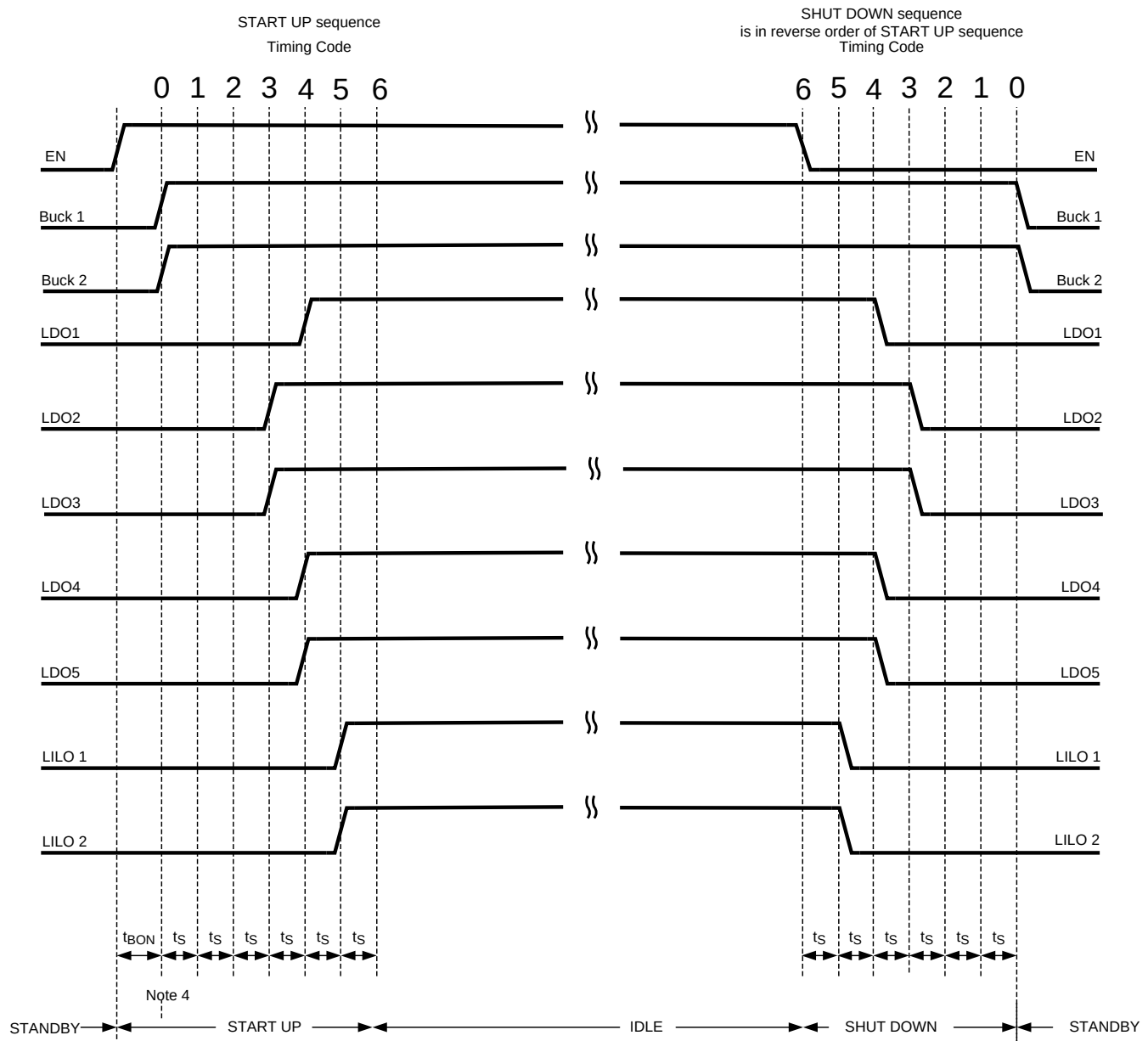
**Note 1** STARTUP and SHUTDOWN sequences are defined by registers. Sequences given here are valid if there the registers are not rewritten via Serial Interface.

**Note 2** The timing showed here define time points when LDOs and BUCK are enabled/disabled. Enabling /disabling process duration depends on voltages and loading conditions. Buck startup duration is typically 170 μs. LDO startup duration is typically 35 μs. For details please see LDOs and BUCK Electrical Specifications.

**Note 3** BUCK1 is disabled. If it is enabled via Serial Interface and the startup sequence is not changed, then it will be disabled, with no delay, from falling edge of EN-pin.

**Note 4** At this time point registers are reset to POR default values.

**Note 5** BUCK2 and LDO3 are enabled by B2\_EN and LDO3\_EN respectively (or via serial interface). If these inputs are high when EN goes high then these outputs turn on after t<sub>s</sub>= 6.

**Figure 8. LP8725-A Startup and Shutdown Sequence if CONFIG=GND, DEFSEL=GND** Note 1, Note 2


All timing is typical.

$t_{BON}$  75  $\mu$ s - Reference and bias turn ON.

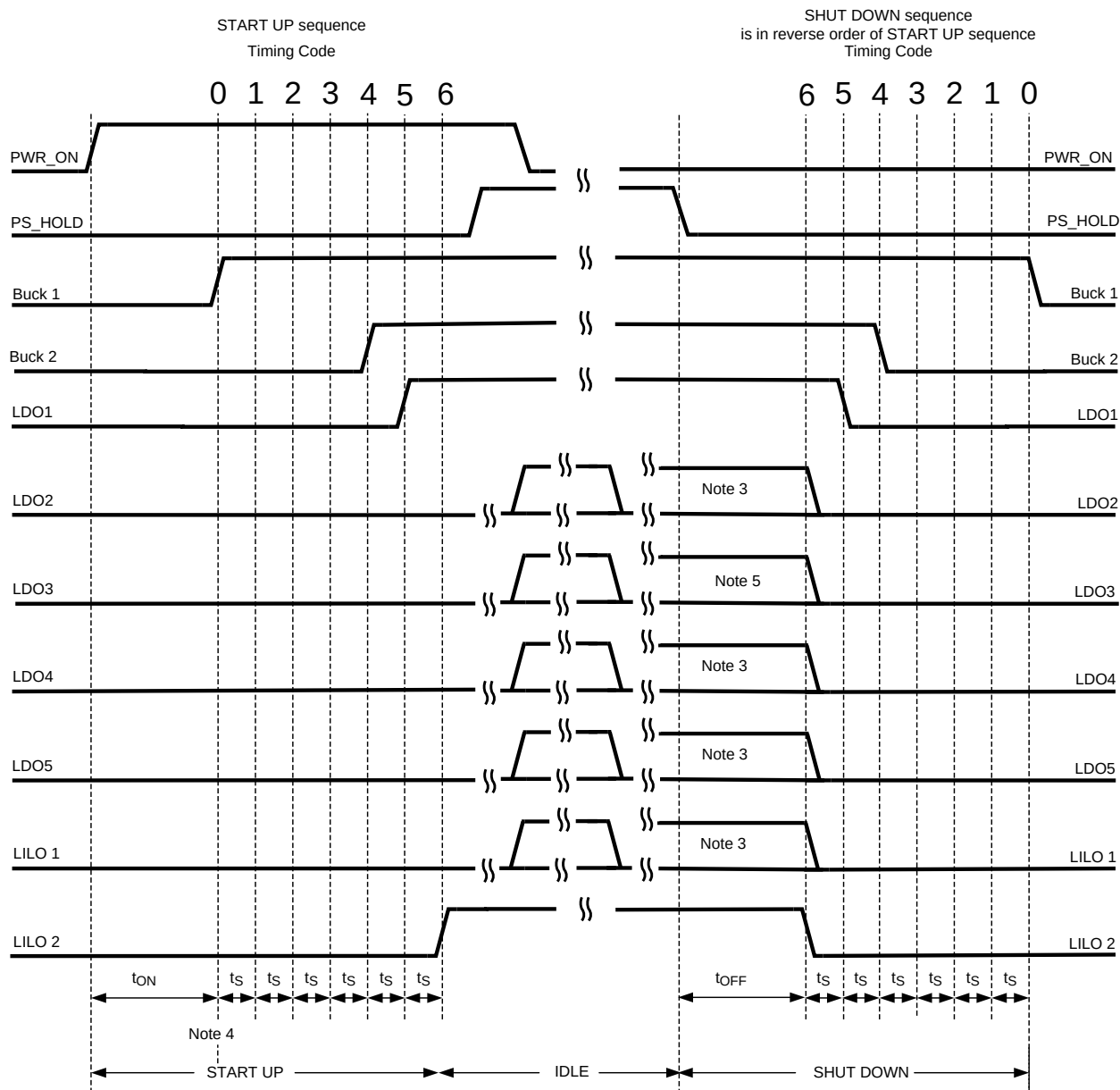
$t_s$  Programmable time steps. (**Typically 64  $\mu$ s/step.**) Time step accuracy is defined by OSC frequency accuracy.

**Note 1** STARTUP and SHUTDOWN sequences are defined by registers. Sequences given here are valid if there the registers are not rewritten via Serial Interface.

**Note 2** The timing showed here define time points when LDOs and BUCK are enabled/disabled. Enabling /disabling process duration depends on voltages and loading conditions. Buck startup duration is typically 170  $\mu$ s. LDO startup duration is typically 35  $\mu$ s. For details please see LDOs and BUCK Electrical Specifications.

**Note 4** At this time point registers are reset to POR default values.

**Figure 9. LP8725-B Startup and Shutdown Sequence if CONFIG=VIN1, DEFSEL=VIN1 or DEFSEL=GND** Note 1, Note 2



All timing is typical.

$t_{ON/OFF}$  30 ms typ. de-bounce times.

$t_s$  Programmable time steps. (Typically 64  $\mu$ s/step.) Time step accuracy is defined by OSC frequency accuracy.

**Note 1** STARTUP and SHUTDOWN sequences are defined by registers. Sequences given here are valid if there the registers are not rewritten via Serial Interface.

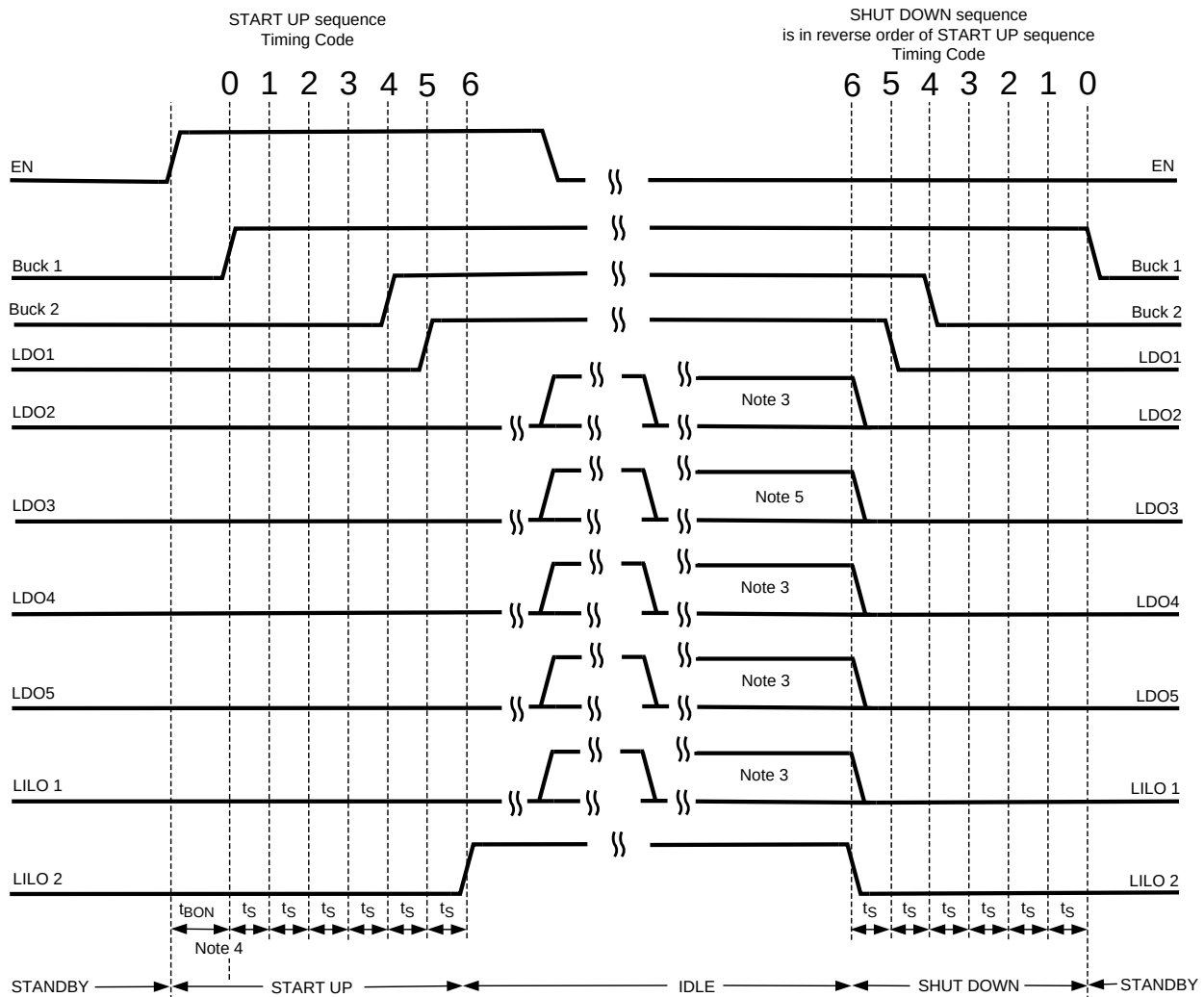
**Note 2** The timing showed here define time points when LDOs and BUCK are enabled/disabled. Enabling /disabling process duration depends on voltages and loading conditions. Buck startup duration is typically 170  $\mu$ s. LDO startup duration is typically 35  $\mu$ s. For details please see LDOs and BUCK Electrical Specifications.

**Note 3** LDO2, 4, 5 and LILO1 are disabled. If they are enabled via Serial Interface and the startup sequence is not changed, then they will be disabled, with no delay, from falling edge of EN-pin.

**Note 4** At this time point registers are reset to POR default values.

**Note 5** LDO3 is enabled by LDO3\_EN (or via serial interface). If this input is high when PWR\_ON goes high then this output turns on after  $t_s = 6$ .

**Figure 10. LP8725-B Startup and Shutdown Sequence if CONFIG=GND, DEFSEL=VIN1 or DEFSEL=GND** Note 1, Note 2



All timing is typical.

$t_{BON}$  75  $\mu$ s - Reference and bias turn ON.

$t_s$  Programmable time steps. (Typically 64  $\mu$ s/step.) Time step accuracy is defined by OSC frequency accuracy.

**Note 1** STARTUP and SHUT DOWN sequences are defined by registers. Sequences given here are valid if there the registers are not rewritten via Serial Interface.

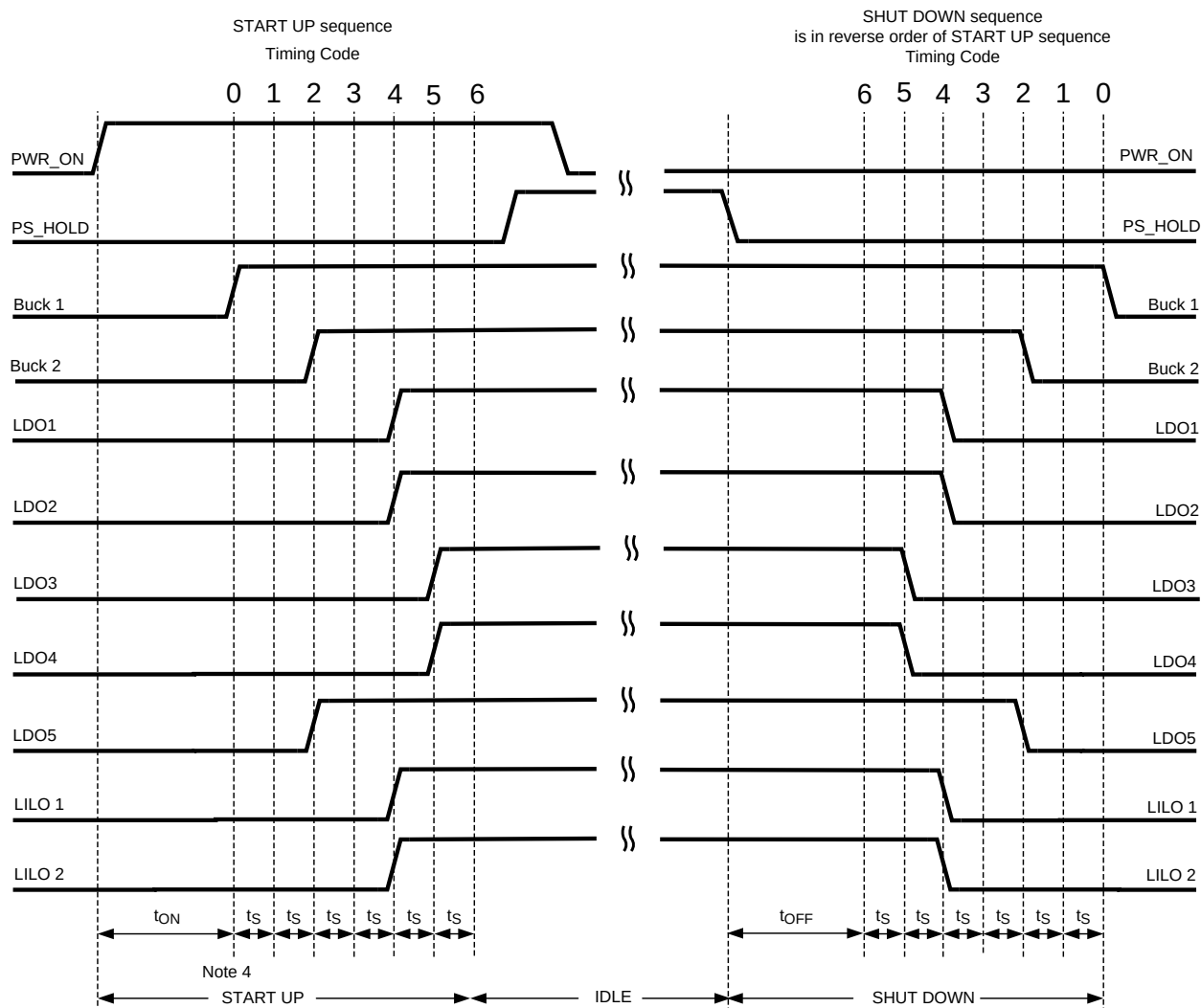
**Note 2** The timing showed here define time points when LDOs and BUCK are enabled/disabled. Enabling /disabling process duration depends on voltages and loading conditions. Buck startup duration is typically 170  $\mu$ s. LDO startup duration is typically 35  $\mu$ s. For details please see LDOs and BUCK Electrical Specifications.

**Note 3** LDO2, 4, 5 and LILO1 are disabled. If they are enabled via Serial Interface and the startup sequence is not changed, then they will be disabled, with no delay, from falling edge of EN-pin.

**Note 4** At this time point registers are reset to POR default values.

**Note 5** LDO3 is enabled by LDO3\_EN (or via serial interface). If this input is high when PWR\_ON goes high then this output turns on after  $t_s = 6$ .

**Figure 11. LP8725-C Startup and Shutdown Sequence if CONFIG=VIN1, DEFSEL=VIN1 or DEFSEL=GND** Note 1, Note 2



All timing is typical.

$t_{ON/OFF}$  30 ms typ. de-bounce times.

$t_s$  Programmable time steps. (Typically 64  $\mu s$ /step.) Time step accuracy is defined by OSC frequency accuracy.

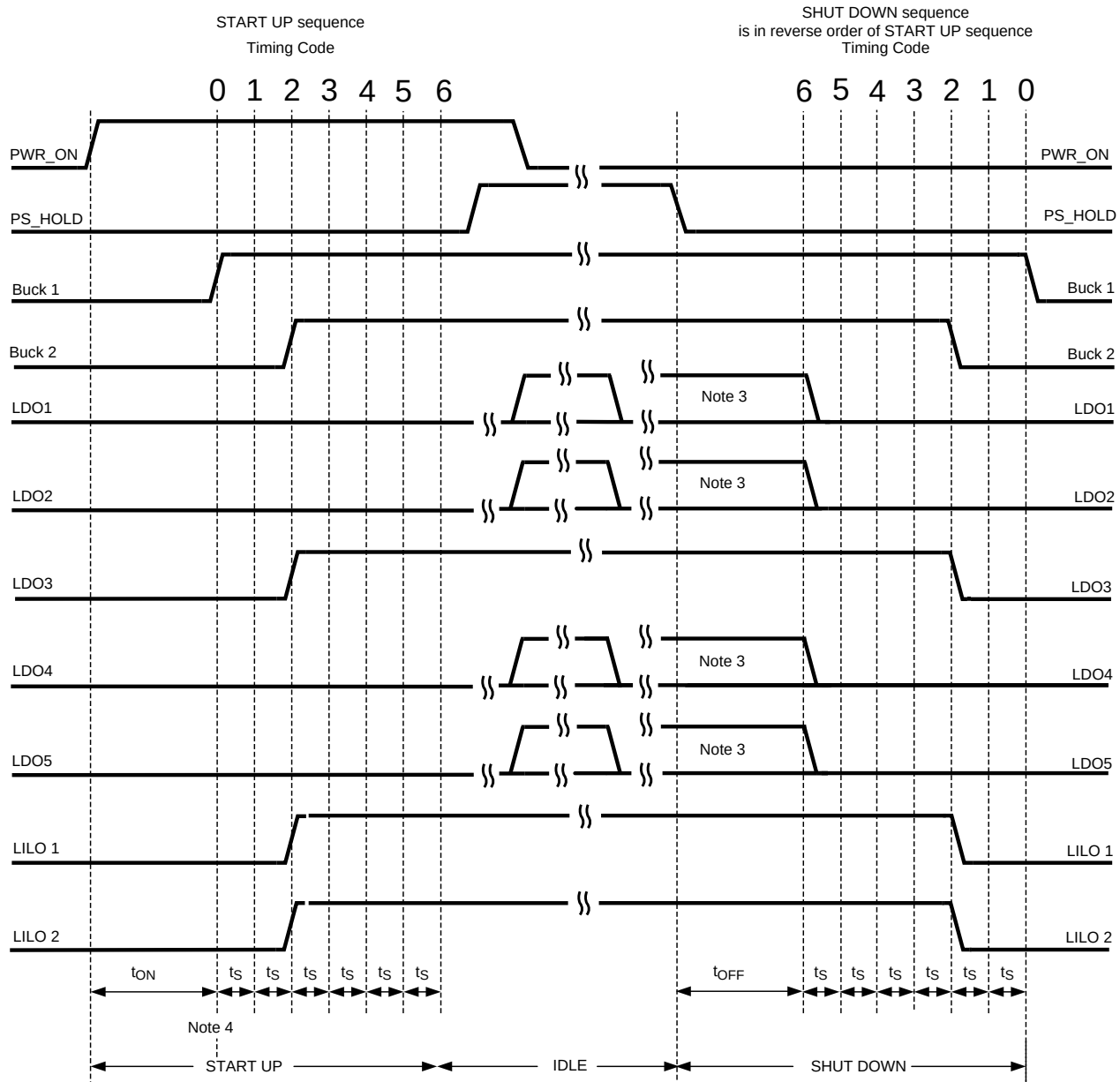
**Note 1** STARTUP and SHUTDOWN sequences are defined by registers. Sequences given here are valid if there the registers are not rewritten via Serial Interface.

**Note 2** The timing showed here define time points when LDOs and BUCK are enabled/disabled. Enabling /disabling process duration depends on voltages and loading conditions. Buck startup duration is typically 170  $\mu s$ . LDO startup duration is typically 35  $\mu s$ . For details please see LDOs and BUCK Electrical Specifications.

**Note 4** At this time point registers are reset to POR default values.



**Figure 12. LP8725-D Startup and Shutdown Sequence if CONFIG=VIN1, DEFSEL=VIN1 or DEFSEL=GND** Note 1, Note 2



All timing is typical.

$t_{ON/OFF}$  30 ms typ. de-bounce times.

$t_s$  Programmable time steps. (Typically 64  $\mu$ s/step.) Time step accuracy is defined by OSC frequency accuracy.

**Note 1** STARTUP and SHUTDOWN sequences are defined by registers. Sequences given here are valid if there the registers are not rewritten via Serial Interface.

**Note 2** The timing showed here define time points when LDOs and BUCK are enabled/disabled. Enabling /disabling process duration depends on voltages and loading conditions. Buck startup duration is typically 170  $\mu$ s. LDO startup duration is typically 35  $\mu$ s. For details please see LDOs and BUCK Electrical Specifications.

**Note 3** LDO1, 2, 4, 5 are disabled. If they are enabled via Serial Interface and the startup sequence is not changed, then they will be disabled, with no delay, from falling edge of EN-pin.

**Note 4** At this time point registers are reset to POR default values.

**Note 5** LDO3 is enabled by LDO3\_EN (or via serial interface). If this input is high when PWR\_ON goes high then this output turns on after  $t_s$  = 6.

**Table 3. Default Output Voltages<sup>(1)(2)</sup>**

| Output | Max Current (mA) | Voltage Range (V) | Default output Voltage [V] and default ON/OFF (PWR_ON/EN=1) |               |
|--------|------------------|-------------------|-------------------------------------------------------------|---------------|
|        |                  |                   | DEFSEL = VIN1                                               | DEFSEL = GND  |
| BUCK1  | 800              | 0.8 to 3.0        | 1.0*/1.2** ON                                               | 1.2*/1.0** ON |
| BUCK2  | 600              | 0.8 to 3.0        | 1.8*/1.8** ON                                               | 1.8*/1.8** ON |
| LDO1   | 300              | 1.2 to 3.3        | 2.8 ON                                                      | 2.6 ON        |
| LDO2   | 300              | 1.2 to 3.3        | 1.8 ON                                                      | 2.8 ON        |
| LDO3   | 300              | 1.2 to 3.3        | 3.3 ON                                                      | 2.8 ON        |
| LDO4   | 300              | 1.2 to 3.3        | 3.3 ON                                                      | 2.8 ON        |
| LDO5   | 300              | 1.2 to 3.3        | 2.8 ON                                                      | 2.8 ON        |
| LIL01  | 300              | 0.8 to 3.3        | 1.2 ON                                                      | 3.3 ON        |
| LIL02  | 300              | 0.8 to 3.3        | 1.2 ON                                                      | 1.2 ON        |

(1) These are dependent on whether DEFSEL is connected to VIN1 or GND when PWR\_ON/EN=1.

(2) BUCK1 voltages are set to \*BUCK1\_V1 and \*\*BUCK1\_V2 as selected by DVS1\_V and the DVS pin.  
BUCK2 voltages are set to \*BUCK2\_V1 and \*\*BUCK2\_V2 as selected by DVS2\_V.

**Table 4. LP8725-A Alternative Part's Default Output Voltages<sup>(1)(2)</sup>**

| Output | Max Current (mA) | Voltage Range (V) | Default output Voltage [V] and default ON/OFF (PWR_ON/EN=1) |               |
|--------|------------------|-------------------|-------------------------------------------------------------|---------------|
|        |                  |                   | DEFSEL = VIN1                                               | DEFSEL = GND  |
| BUCK1  | 800              | 0.8 to 3.0        | 1.1*/1.0** OFF                                              | 1.3*/1.2** ON |
| BUCK2  | 600              | 0.8 to 3.0        | 1.1*/1.0** OFF***                                           | 1.3*/1.2** ON |
| LDO1   | 300              | 1.2 to 3.3        | 2.6 ON                                                      | 2.8 ON        |
| LDO2   | 300              | 1.2 to 3.3        | 3.0 ON                                                      | 2.8 ON        |
| LDO3   | 300              | 1.2 to 3.3        | 3.3 OFF****                                                 | 2.8 ON        |
| LDO4   | 300              | 1.2 to 3.3        | 3.0 ON                                                      | 2.8 ON        |
| LDO5   | 300              | 1.2 to 3.3        | 2.8 ON                                                      | 2.8 ON        |
| LIL01  | 300              | 0.8 to 3.3        | 1.8 ON                                                      | 1.8 ON        |
| LIL02  | 300              | 0.8 to 3.3        | 1.0 ON                                                      | 1.8 ON        |

(1) These are dependent on whether DEFSEL is connected to VIN1 or GND when PWR\_ON/EN=1.

(2) BUCK1 voltages are set to \*BUCK1\_V1 and \*\*BUCK1\_V2 as selected by DVS1\_V and the DVS pin.  
BUCK2 voltages are set to \*BUCK2\_V1 and \*\*BUCK2\_V2 as selected by DVS2\_V.

\*\*\* Only if pin B2\_EN=0 if in SUB\_PMU configuration

\*\*\*\* Only if pin LDO3\_EN=0

**Table 5. LP8725-B Alternative Part's Default Output Voltages<sup>(1)(2)</sup>**

| Output | Max Current (mA) | Voltage Range (V) | Default output Voltage [V] and default ON/OFF (PWR_ON/EN=1) |               |
|--------|------------------|-------------------|-------------------------------------------------------------|---------------|
|        |                  |                   | DEFSEL = VIN1                                               | DEFSEL = GND  |
| BUCK1  | 800              | 0.8 to 3.0        | 1.2*/1.2** ON                                               | 1.2*/1.2** ON |
| BUCK2  | 600              | 0.8 to 3.0        | 1.8*/1.8** ON                                               | 1.8*/1.8** ON |
| LDO1   | 300              | 1.2 to 3.3        | 2.6 ON                                                      | 1.8 ON        |
| LDO2   | 300              | 1.2 to 3.3        | 2.8 OFF                                                     | 2.8 OFF       |
| LDO3   | 300              | 1.2 to 3.3        | 2.8 OFF***                                                  | 2.8 OFF***    |
| LDO4   | 300              | 1.2 to 3.3        | 1.2 OFF                                                     | 1.2 OFF       |
| LDO5   | 300              | 1.2 to 3.3        | 1.2 OFF                                                     | 1.2 OFF       |
| LILO1  | 300              | 0.8 to 3.3        | 2.5 OFF                                                     | 2.5 OFF       |
| LILO2  | 300              | 0.8 to 3.3        | 3.3 ON                                                      | 3.3 ON        |

(1) These are dependent on whether DEFSEL is connected to VIN1 or GND when PWR\_ON/EN=1.

(2) BUCK1 voltages are set to \*BUCK1\_V1 and \*\*BUCK1\_V2 as selected by DVS1\_V and the DVS pin.  
BUCK2 voltages are set to \*BUCK2\_V1 and \*\*BUCK2\_V2 as selected by DVS2\_V.

\*\*\* Only if pin LDO3\_EN=0

**Table 6. LP8725-C Alternative Part's Default Output Voltages<sup>(1)</sup>**

| Output | Max Current (mA) | Voltage Range (V) | Default output Voltage [V] and default ON/OFF (PWR_ON/EN=1) |              |
|--------|------------------|-------------------|-------------------------------------------------------------|--------------|
|        |                  |                   | DEFSEL = VIN1                                               | DEFSEL = GND |
| BUCK1  | 800              | 0.8 to 3.0        | 1.2 ON                                                      | 1.2 ON       |
| BUCK2  | 600              | 0.8 to 3.0        | 1.8 ON                                                      | 1.8 ON       |
| LDO1   | 300              | 1.2 to 3.3        | 2.6 ON                                                      | 2.6 ON       |
| LDO2   | 300              | 1.2 to 3.3        | 2.8 ON                                                      | 2.8 ON       |
| LDO3   | 300              | 1.2 to 3.3        | 2.8 ON                                                      | 2.8 ON       |
| LDO4   | 300              | 1.2 to 3.3        | 2.5 ON                                                      | 2.5 ON       |
| LDO5   | 300              | 1.2 to 3.3        | 3.3 ON                                                      | 3.3 ON       |
| LILO1  | 300              | 0.8 to 3.3        | 1.2 ON                                                      | 1.2 ON       |
| LILO2  | 300              | 0.8 to 3.3        | 1.2 ON                                                      | 1.2 ON       |

(1) These are dependent on whether DEFSEL is connected to VIN1 or GND when PWR\_ON/EN=1.

**Table 7. LP8725-D Alternative Part's Default Output Voltages<sup>(1)(2)</sup>**

| Output | Max Current (mA) | Voltage Range (V) | Default output Voltage [V] and default ON/OFF (PWR_ON/EN=1) |               |
|--------|------------------|-------------------|-------------------------------------------------------------|---------------|
|        |                  |                   | DEFSEL = VIN1                                               | DEFSEL = GND  |
| BUCK1  | 800              | 0.8 to 3.0        | 1.3*/1.3** ON                                               | 1.3*/1.3** ON |
| BUCK2  | 800              | 0.8 to 3.0        | 1.8*/1.8** ON                                               | 1.8*/1.8** ON |
| LDO1   | 300              | 1.2 to 3.3        | 2.8 OFF                                                     | 2.8 OFF       |
| LDO2   | 300              | 1.2 to 3.3        | 1.8 OFF                                                     | 1.8 OFF       |
| LDO3   | 300              | 1.2 to 3.3        | 1.8 ON                                                      | 1.8 ON        |
| LDO4   | 300              | 1.2 to 3.3        | 3.0 OFF                                                     | 3.0 OFF       |
| LDO5   | 300              | 1.2 to 3.3        | 1.8 OFF                                                     | 1.2 OFF       |
| LIL01  | 300              | 0.8 to 3.3        | 3.0 ON                                                      | 3.0 ON        |
| LIL02  | 300              | 0.8 to 3.3        | 3.0 ON                                                      | 3.0 ON        |

(1) These are dependent on whether DEFSEL is connected to VIN1 or GND when PWR\_ON/EN=1.

(2) BUCK1 voltages are set to \*BUCK1\_V1 and \*\*BUCK1\_V2 as selected by DVS1\_V and the DVS pin.  
BUCK2 voltages are set to \*BUCK2\_V1 and \*\*BUCK2\_V2 as selected by DVS2\_V.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS<sup>(1) (2)</sup>

|                                                                  |                                   |      |
|------------------------------------------------------------------|-----------------------------------|------|
| $V_{IN1}$                                                        | -0.3V to +6V                      |      |
| $V_{IN2}, V_{IN3}, V_{INLILO1}, V_{INLILO2}, V_{INB1}, V_{INB2}$ | -0.3V to $V_{IN1}+0.3V$ and <6.0V |      |
| Logic and control pins: Voltage to GND                           | -0.3V to $V_{IN1}+0.3V$ and <6.0V |      |
| Continuous Power Dissipation <sup>(3)</sup>                      | Internally Limited                |      |
| Junction Temperature ( $T_{J-MAX}$ )                             | 150°C                             |      |
| Storage Temperature Range                                        | -65 to 150°C                      |      |
| ESD Rating <sup>(4)</sup>                                        | Human Body Model                  | 2kV  |
|                                                                  | Machine Model                     | 200V |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the potential at the GND pin.
- (3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at  $T_J = 150^\circ\text{C}$  (typ.) and disengages at  $T_J = 130^\circ\text{C}$ .
- (4) The human-body model is 100 pF discharged through 1.5 k $\Omega$ . The machine model is a 200 pF capacitor discharged directly into each pin, MIL-STD-883 3015.7.

## OPERATING RATINGS<sup>(1) (2)</sup>

|                                                        |                   |
|--------------------------------------------------------|-------------------|
| $V_{IN1}$                                              | 2.6 to 4.5V       |
| $V_{IN2}, V_{IN3}, V_{INB1}, V_{INB2}$                 | 2.6V to $V_{IN1}$ |
| $V_{INLILO1}, V_{INLILO2}$                             | 1.8V to $V_{IN1}$ |
| All input-only pins                                    | 0V to $V_{IN1}$   |
| Junction Temperature ( $T_J$ )                         | -40 to 125°C      |
| Ambient Temperature ( $T_A$ ) <sup>(3)</sup>           | -40 to 85°C       |
| Maximum Power Dissipation ( $T_A = 70^\circ\text{C}$ ) | 1.3 W             |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the potential at the GND pin.
- (3) In applications where high power dissipation and/or poor package resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature ( $T_{A-MAX}$ ) is dependent on the maximum operating junction temperature ( $T_{J-MAX}$ ). The maximum power dissipation of the device in the application ( $P_{D-MAX}$ ) and the junction to ambient thermal resistance of the package ( $\theta_{JA}$ ) in the application, as given by the following equation:  $T_{A-MAX} = T_{J-MAX} (\theta_{JA} \times P_{D-MAX})$ . Due to the pulsed nature of testing the part, the temp in the Electrical Characteristic table is specified as  $T_A = T_J$ .

## THERMAL PROPERTIES

|                                                                                                                            |        |
|----------------------------------------------------------------------------------------------------------------------------|--------|
| Junction-to-Ambient Thermal Resistance ( $\theta_{JA}$ ) <sup>(1)</sup> , $\theta_{JA}$ 4-Layer JEDEC Board <sup>(2)</sup> | 41°C/W |
|----------------------------------------------------------------------------------------------------------------------------|--------|

- (1) In applications where high power dissipation and/or poor package resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature ( $T_{A-MAX}$ ) is dependent on the maximum operating junction temperature ( $T_{J-MAX}$ ). The maximum power dissipation of the device in the application ( $P_{D-MAX}$ ) and the junction to ambient thermal resistance of the package ( $\theta_{JA}$ ) in the application, as given by the following equation:  $T_{A-MAX} = T_{J-MAX} (\theta_{JA} \times P_{D-MAX})$ . Due to the pulsed nature of testing the part, the temp in the Electrical Characteristic table is specified as  $T_A = T_J$ .
- (2) Junction-to-ambient thermal resistance is highly application and board layout dependent. In applications where high power dissipation exists, special care must be given to thermal dissipation issues in board design.

## CURRENT CONSUMPTION

Unless otherwise noted,  $V_{IN1}=V_{IN2}=V_{IN3}=V_{INB1}=V_{INB2}=V_{INLILO1}=V_{INLILO2}=3.6V$ ;  $C_{LDOX}=1\mu F$ ;  $C_{BUCKOUT}=C_{BUCKIN}=4.7\mu F$ ;  $C_{VIN1-3}=C_{VINLILO1}=C_{VINLILO2}=2.2\mu F$ . Typical values and limits appearing in normal type apply for  $T_J=25^\circ C$ . Limits appearing in **boldface** type apply over the entire junction temperature range for operation,  $T_J = -40$  to  $+125^\circ C$ . <sup>(1)</sup>

| Symbol           | Parameter                        | Conditions                             | Min | Typ | Max        | Unit    |
|------------------|----------------------------------|----------------------------------------|-----|-----|------------|---------|
| $I_{Q(Standby)}$ | Standby Current                  | All outputs disabled EN = 0            |     | 3.3 | <b>8</b>   | $\mu A$ |
| $I_{Q(SLEEP)}$   | Current in SLEEP Mode at no load | Outputs disabled via control registers |     | 50  | <b>80</b>  |         |
|                  |                                  | Only Buck1 and LDO1 enabled            |     | 95  |            |         |
|                  |                                  | All outputs enabled                    |     | 205 | <b>280</b> |         |
| $I_{Q(IDLE)}$    | Current at no load               | Outputs disabled via control registers |     | 145 | <b>210</b> |         |
|                  |                                  | Only Buck1 and LDO1 enabled            |     | 205 |            |         |
|                  |                                  | All outputs enabled                    |     | 420 | <b>600</b> |         |

(1) Min and Max limits are specified by design, test or statistical analysis. Typical numbers are not verified, but do represent the most likely norm.

## THERMAL SHUTDOWN

The Thermal Shutdown (TSD) function monitors the chip temperature ( $T_J$ ) to protect the chip from temperature damage caused, e.g., by excessive power dissipation. <sup>(1)</sup>

| Symbol | Parameter      | Conditions | Min | Typ | Max | Unit       |
|--------|----------------|------------|-----|-----|-----|------------|
|        | TSD            |            |     | 160 |     | $^\circ C$ |
|        | TSD Hysteresis |            |     | 20  |     | $^\circ C$ |

(1) Min and Max limits are specified by design, test or statistical analysis. Typical numbers are not verified, but do represent the most likely norm.

## UNDER-VOLTAGE LOCK OUT

This device has Under-Voltage Lock Out (UVLO) that checks VIN1-pin voltage before starting Power On sequence. UVLO is also checked during Power On sequence. If the VDD voltage is less than UVLO threshold the PMU will not Power On. After the PMU successfully passed Power On sequence UVLO is not monitored. <sup>(1)</sup>

| Symbol     | Parameter                          | Conditions | Min          | Typ | Max          | Unit |
|------------|------------------------------------|------------|--------------|-----|--------------|------|
| $V_{UVLO}$ | UVLO Threshold<br>$V_{IN1}$ rising | CONFIG = 0 |              | 2.3 |              | V    |
|            |                                    | CONFIG = 1 | <b>2.825</b> | 3.0 | <b>3.185</b> |      |
|            | Hysteresis                         | CONFIG = 0 |              | 400 |              | mV   |
|            |                                    | CONFIG = 1 |              | 800 |              |      |

(1) Min and Max limits are specified by design, test or statistical analysis. Typical numbers are not verified, but do represent the most likely norm.

## LOGIC AND CONTROL

Unless otherwise noted,  $V_{IN1}=V_{IN2}=V_{IN3}=V_{INB1}=V_{INB2}=V_{INLILO1}=V_{INLILO2}=3.6V$ ;  $C_{LDOX}=1\mu F$ ;  $C_{BUCKOUT}=C_{BUCKIN}=4.7\mu F$ ;  $C_{VIN1-3}=C_{VINLILO1}=C_{VINLILO2}=2.2\mu F$ . Typical values and limits appearing in normal type apply for  $T_J=25^\circ C$ . Limits appearing in **boldface** type apply over the entire junction temperature range for operation,  $T_J = -40$  to  $+125^\circ C$ . <sup>(1)</sup>

| Symbol                          | Parameter               | Conditions                                                                                  | Min        | Typ | Max        | Unit    |
|---------------------------------|-------------------------|---------------------------------------------------------------------------------------------|------------|-----|------------|---------|
| <b>Logic and Control Inputs</b> |                         |                                                                                             |            |     |            |         |
| $V_{IL}$                        | Input Low Level         | EN, SCL, SDA, DVS, PS_HOLD, PWR_ON, BUCK2_EN, LDO3_EN                                       |            |     | <b>0.4</b> | V       |
| $V_{IH}$                        | Input High Level        | EN, SCL, SDA, DVS, PS_HOLD, PWR_ON, BUCK2_EN, LDO3_EN                                       | <b>1.2</b> |     |            | V       |
| $I_{IL}$                        | Input Low Level Current | EN, SCL, SDA, DVS, PS_HOLD, PWR_ON, DVS, DEFSEL, CONFIG, BUCK2_EN, LDO3_EN<br>$V_{IL} = 0V$ |            | 0   | <b>2</b>   | $\mu A$ |

(1) Min and Max limits are specified by design, test or statistical analysis. Typical numbers are not verified, but do represent the most likely norm.

## LOGIC AND CONTROL (continued)

Unless otherwise noted,  $V_{IN1}=V_{IN2}=V_{IN3}=V_{INB1}=V_{INB2}=V_{INLILO1}=V_{INLILO2}=3.6V$ ;  $C_{LODX}=1\mu F$ ;  $C_{BUCKOUT}=C_{BUCKIN}=4.7\mu F$ ,  $C_{VIN1-3}=C_{VINLILO1}C_{VINLILO2}=2.2\mu F$ . Typical values and limits appearing in normal type apply for  $T_J=25^\circ C$ . Limits appearing in **boldface** type apply over the entire junction temperature range for operation,  $T_J = -40$  to  $+125^\circ C$ .<sup>(1)</sup>

| Symbol                           | Parameter                | Conditions                                                 | Min | Typ  | Max | Unit       |
|----------------------------------|--------------------------|------------------------------------------------------------|-----|------|-----|------------|
| $I_{IH}$                         | Input High Level Current | PS_HOLD, DEFSEL, CONFIG, DVS<br>$V_{IH} = V_{IN1}$         |     | 0    | 2   |            |
| $R_{PD}$                         | Pull Down Resistance     | From EN, PWR_ON, B2_EN, and LDO3_EN                        |     | 500  |     | k $\Omega$ |
| <b>Logic and Control Outputs</b> |                          |                                                            |     |      |     |            |
| $V_{OL}$                         | Output Low Level         | SDA, RESET_N<br>$I_{OUT} = 2mA$                            |     | 0.14 | 0.3 | V          |
| $I_{OH}$                         | Output High Level        | SDA, RESET_N have Open drain outputs<br>$V_{OH} = V_{IN1}$ |     | 0    | 2   | $\mu A$    |

## BUCK CONVERTERS

Unless otherwise noted,  $V_{IN1}=V_{IN2}=V_{IN3}=V_{INB1}=V_{INB2}=V_{INLILO1}=V_{INLILO2}=3.6V$ ;  $C_{LODX}=1\mu F$ ;  $C_{BUCKOUT}=C_{BUCKIN}=4.7\mu F$ ,  $C_{VIN1-3}=C_{VINLILO1}C_{VINLILO2}=2.2\mu F$ . Typical values and limits appearing in normal type apply for  $T_J=25^\circ C$ . Limits appearing in **boldface** type apply over the entire junction temperature range for operation,  $T_J = -40$  to  $+125^\circ C$ .<sup>(1) (2)</sup>

| Symbol          | Parameter                   | Conditions                                                                                                                               | Min | Typ  | Max  | Unit       |
|-----------------|-----------------------------|------------------------------------------------------------------------------------------------------------------------------------------|-----|------|------|------------|
| $V_{FB}$        | BUCK1 Feedback Voltage      | $V_{OUT} = 1.8V$                                                                                                                         | -2  |      | +2   | %          |
|                 | BUCK2 Feedback Voltage      |                                                                                                                                          | -3  |      | +3   |            |
| $R_{DS(on)(P)}$ | Pin-Pin resistance for PFET | $I_{OUT} = 200\text{ mA}$                                                                                                                |     | 265  |      | m $\Omega$ |
| $R_{DS(on)(N)}$ | Pin-Pin resistance for NFET | $I_{OUT} = -200\text{ mA}$                                                                                                               |     | 150  |      | m $\Omega$ |
| $I_{LIM}$       | Switch Peak Current Limit   | Open-loop, programmable:<br>250 mA max $I_{OUT}$ typ<br>450 mA max $I_{OUT}$ typ<br>600 mA max $I_{OUT}$ typ<br>800 mA max $I_{OUT}$ typ |     | 460  |      | mA         |
|                 |                             |                                                                                                                                          |     | 780  |      |            |
|                 |                             |                                                                                                                                          | 750 | 1050 | 1500 |            |
|                 |                             |                                                                                                                                          |     | 1370 |      |            |
| $t_{STUP}$      | Startup Time                | $I_{OUT} = 0mA$ to 100 mA                                                                                                                |     | 170  |      | $\mu s$    |
| $f_{SW}$        | Switching Frequency         |                                                                                                                                          | 3.6 | 4.1  | 4.4  | MHz        |

- (1) Min and Max limits are specified by design, test or statistical analysis. Typical numbers are not verified, but do represent the most likely norm.
- (2) The parameters in the electrical characteristic table are tested under open loop conditions at  $V_{IN} = 3.6V$  unless otherwise specified. For performance over the input voltage range and closed loop condition, refer to the datasheet curves.

## DIGITAL LDOs (1, 2, 3)

Unless otherwise noted,  $V_{IN1}=V_{IN2}=V_{IN3}=V_{INB1}=V_{INB2}=V_{INLILO1}=V_{INLILO2}=3.6V$ ;  $C_{LODX}=1\mu F$ ;  $C_{BUCKOUT}=C_{BUCKIN}=4.7\mu F$ ,  $C_{VIN1-3}=C_{VINLILO1}C_{VINLILO2}=2.2\mu F$ . Typical values and limits appearing in normal type apply for  $T_J=25^\circ C$ . Limits appearing in **boldface** type apply over the entire junction temperature range for operation,  $T_J = -40$  to  $+125^\circ C$ .<sup>(1)</sup>

| Symbol           | Parameter                          | Conditions                                                                | Min  | Typ | Max  | Unit |
|------------------|------------------------------------|---------------------------------------------------------------------------|------|-----|------|------|
| $V_{OUT}$        | LDO1 Output Voltage Accuracy       | $I_{OUT} = 1mA$ , $V_{OUT} = 2.8V$                                        | -1.5 |     | +1.5 | %    |
|                  |                                    |                                                                           | -2   |     | +2   |      |
|                  | LDOs 2 & 3 Output Voltage Accuracy |                                                                           | -2   |     | +2   |      |
|                  |                                    |                                                                           | -2.5 |     | +2.5 |      |
| $\Delta V_{OUT}$ | Line Regulation                    | $V_{OUT} + 0.5V \leq V_{IN2} \leq 4.5V$<br>$I_{OUT} = 1mA$ <sup>(2)</sup> |      | 2   |      | mV   |
|                  | Load Regulation                    | $1 < I_{OUT} < 300\text{ mA}$                                             |      | 2   |      |      |

- (1) Min and Max limits are specified by design, test or statistical analysis. Typical numbers are not verified, but do represent the most likely norm.
- (2) The minimum input voltage equals  $V_{OUT}(\text{nom}) + 0.5V$  or  $2.5V$ , which ever is greater.

## DIGITAL LDOs (1, 2, 3) (continued)

Unless otherwise noted,  $V_{IN1}=V_{IN2}=V_{IN3}=V_{INB1}=V_{INB2}=V_{INLILO1}=V_{INLILO2}=3.6V$ ;  $C_{LODX}=1\mu F$ ;  $C_{BUCKOUT}=C_{BUCKIN}=4.7\mu F$ ,  $C_{VIN1-3}=C_{VINLILO1}C_{VINLILO2}=2.2\mu F$ . Typical values and limits appearing in normal type apply for  $T_J=25^\circ C$ . Limits appearing in **boldface** type apply over the entire junction temperature range for operation,  $T_J = -40$  to  $+125^\circ C$ . <sup>(1)</sup>

| Symbol      | Parameter                                 | Conditions                                                             | Min        | Typ | Max        | Unit          |
|-------------|-------------------------------------------|------------------------------------------------------------------------|------------|-----|------------|---------------|
| $V_{DO}$    | Dropout Voltage                           | $I_{OUT} = 300\text{ mA}$<br>Nominal $V_{OUT} = 2.8V$ <sup>(3)</sup>   |            | 190 | <b>270</b> | mV            |
| $I_{OUT}$   | Output Current                            |                                                                        | <b>0</b>   |     | <b>300</b> | mA            |
| $I_{SLEEP}$ | Max Output Current in Sleep Mode          |                                                                        |            |     | <b>1</b>   | mA            |
| $I_{SC}$    | Output Current Limit                      | $V_{OUT} = 0V$                                                         |            | 650 |            | mA            |
| $e_N$       | Output Voltage Noise                      | $10\text{ Hz} \leq f \leq 100\text{ KHz}$<br>$I_{OUT} = 300\text{ mA}$ |            | 35  |            | $\mu V_{RMS}$ |
| PSRR        | Power Supply Rejection Ratio              | $f \leq 10\text{ KHz}$ , $I_{OUT} = 20\text{ mA}$                      |            | 65  |            | dB            |
| $t_{STUP}$  | Startup Time                              | $I_{OUT} = 0\text{ mA}$ to $300\text{ mA}$ in Idle mode.               |            | 20  |            | $\mu s$       |
| $V_{OS}$    | Start-up Overshoot                        | $I_{OUT} = 300\text{ mA}$ <sup>(4)</sup>                               |            |     | <b>30</b>  | mV            |
| $C_{OUT}$   | External Output Capacitance for Stability | <sup>(4)</sup>                                                         | <b>0.5</b> | 1   | <b>20</b>  | $\mu F$       |

(3) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.

(4) This specification is guaranteed by design.

## LOW-NOISE ANALOG LDOs (4, 5)

Unless otherwise noted,  $V_{IN1}=V_{IN2}=V_{IN3}=V_{INB1}=V_{INB2}=V_{INLILO1}=V_{INLILO2}=3.6V$ ;  $C_{LODX}=1\mu F$ ;  $C_{BUCKOUT}=C_{BUCKIN}=4.7\mu F$ ,  $C_{VIN1-3}=C_{VINLILO1}C_{VINLILO2}=2.2\mu F$ . Typical values and limits appearing in normal type apply for  $T_J=25^\circ C$ . Limits appearing in **boldface** type apply over the entire junction temperature range for operation,  $T_J = -40$  to  $+125^\circ C$ . <sup>(1)</sup>

| Symbol           | Parameter                                 | Conditions                                                                        | Min         | Typ | Max         | Unit          |
|------------------|-------------------------------------------|-----------------------------------------------------------------------------------|-------------|-----|-------------|---------------|
| $V_{OUT}$        | Output Voltage Accuracy                   | $I_{OUT} = 1\text{ mA}$ , $V_{OUT} = 2.8V$                                        | -2          |     | +2          | %             |
|                  |                                           |                                                                                   | <b>-2.5</b> |     | <b>+2.5</b> |               |
| $\Delta V_{OUT}$ | Line Regulation                           | $V_{OUT} + 0.5V \leq V_{IN3} \leq 4.5V$<br>$I_{OUT} = 1\text{ mA}$ <sup>(2)</sup> |             | 1   |             | mV            |
|                  | Load Regulation                           | $1 < I_{OUT} < 300\text{ mA}$                                                     |             | 1   |             |               |
| $V_{DO}$         | Dropout Voltage                           | $I_{OUT} = 300\text{ mA}$<br>Nominal $V_{OUT} = 2.8V$ <sup>(3)</sup>              |             | 220 | <b>310</b>  | mV            |
| $I_{OUT}$        | Output Current                            |                                                                                   | <b>0</b>    |     | <b>300</b>  | mA            |
| $I_{SLEEP}$      | Max Output Current in Sleep Mode          |                                                                                   |             |     | <b>1</b>    | mA            |
| $I_{SC}$         | Output Current Limit                      | $V_{OUT} = 0V$                                                                    |             | 625 |             | mA            |
| $e_N$            | Output Voltage Noise                      | $10\text{ Hz} \leq f \leq 100\text{ KHz}$<br>$I_{OUT} = 300\text{ mA}$            | 10          | 10  |             | $\mu V_{RMS}$ |
| PSRR             | Power Supply Rejection Ratio              | $f \leq 10\text{ KHz}$ , $I_{OUT} = 20\text{ mA}$                                 |             | 75  |             | dB            |
| $t_{STUP}$       | Startup Time                              | $I_{OUT} = 0\text{ mA}$ to $300\text{ mA}$ in Idle mode.                          |             | 35  |             | $\mu s$       |
| $V_{OS}$         | Start-up Overshoot                        | $I_{OUT} = 300\text{ mA}$ <sup>(4)</sup>                                          |             |     | <b>30</b>   | mV            |
| $C_{OUT}$        | External Output Capacitance for Stability | <sup>(4)</sup>                                                                    | <b>0.5</b>  | 1   | <b>20</b>   | $\mu F$       |

(1) Min and Max limits are specified by design, test or statistical analysis. Typical numbers are not verified, but do represent the most likely norm.

(2) The minimum input voltage equals  $V_{OUT}(\text{nom}) + 0.5V$  or  $2.5V$ , which ever is greater.

(3) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.

(4) This specification is guaranteed by design.



## LOW-INPUT LOW-OUTPUT LDO (LIL01, LIL02)

Unless otherwise noted,  $V_{IN1}=V_{IN2}=V_{IN3}=V_{INB1}=V_{INB2}=V_{INLIL01}=V_{INLIL02}=3.6V$ ;  $C_{LODX}=1\mu F$ ;  $C_{BUCKOUT}=C_{BUCKIN}=4.7\mu F$ ,  $C_{VIN1-3}=C_{VINLIL01}C_{VINLIL02}=2.2\mu F$ . Typical values and limits appearing in normal type apply for  $T_J=25^\circ C$ . Limits appearing in **boldface** type apply over the entire junction temperature range for operation,  $T_J = -40$  to  $+125^\circ C$ . <sup>(1)</sup>

| Symbol           | Parameter                                 | Conditions                                                    | Min        | Typ | Max        | Unit          |
|------------------|-------------------------------------------|---------------------------------------------------------------|------------|-----|------------|---------------|
| $V_{OUT}$        | LIL01 Output Voltage Accuracy             | $I_{OUT} = 1mA$ , $V_{OUT} = 1.8V$                            | -2         |     | +2         | %             |
|                  |                                           |                                                               | -3         |     | +3         |               |
|                  | LIL02 Output Voltage Accuracy             |                                                               | -3         |     | +3         |               |
|                  |                                           |                                                               | -4         |     | +4         |               |
| $\Delta V_{OUT}$ | Line Regulation                           | $V_{OUT} + 0.5V \leq V_{LIL0} \leq 4.5V$<br>$I_{OUT} = 1mA$   |            | 1   |            | mV            |
|                  | Load Regulation                           | $1 < I_{OUT} < 300 mA$                                        |            | 5   |            |               |
| $V_{DO}$         | Dropout Voltage                           | $I_{OUT} = 300 mA$<br>Nominal $V_{OUT} = 1.8V$ <sup>(2)</sup> |            | 230 | <b>310</b> | mV            |
| $I_{OUT}$        | Output Current                            |                                                               | <b>0</b>   |     | <b>300</b> | mA            |
| $I_{SLEEP}$      | Max Output Current in Sleep Mode          |                                                               |            |     | <b>1</b>   | mA            |
| $I_{SC}$         | Output Current Limit                      | $V_{OUT} = 0V$                                                |            | 670 |            | mA            |
| $e_N$            | Output Voltage Noise                      | $10 Hz \leq f \leq 100 KHz$<br>$I_{OUT} = 300 mA$             |            | 80  |            | $\mu V_{RMS}$ |
| PSRR             | Power Supply Rejection Ratio              | $f \leq 10 KHz$ , $I_{OUT} = 20 mA$                           |            | 60  |            | dB            |
| $t_{STUP}$       | Startup Time                              | $I_{OUT} = 0 mA$ to $300 mA$ in Idle mode.                    |            | 65  |            | $\mu s$       |
| $V_{OS}$         | Start-up Overshoot                        | <sup>(3)</sup>                                                |            |     | <b>30</b>  | mV            |
| $C_{OUT}$        | External Output Capacitance for Stability | <sup>(3)</sup>                                                | <b>0.5</b> | 1   | <b>20</b>  | $\mu F$       |

- (1) Min and Max limits are specified by design, test or statistical analysis. Typical numbers are not verified, but do represent the most likely norm.
- (2) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.
- (3) This specification is guaranteed by design.

## LP8725 CONTROL REGISTERS

**Table 8. Control Registers**

| ADDR | Register Name         | Bit 7          | Bit 6          | Bit 5       | Bit 4       | Bit 3       | Bit 2       | Bit 1       | Bit 0       |
|------|-----------------------|----------------|----------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 0x00 | <b>GENERAL</b>        | TIMESTEP       | SHORT_TIMESTEP | 0           | BUCK2_EN    | DVS2_V      | DVS1_V      | SLEEP_MODE  | BUCK1_EN    |
| 0x01 | <b>LDO1</b>           | LDO1_T[2]      | LDO1_T[1]      | LDO1_T[0]   | LDO1_V[4]   | LDO1_V[3]   | LDO1_V[2]   | LDO1_V[1]   | LDO1_V[0]   |
| 0x02 | <b>LDO2</b>           | LDO2_T[2]      | LDO2_T[1]      | LDO2_T[0]   | LDO2_V[4]   | LDO2_V[3]   | LDO2_V[2]   | LDO2_V[1]   | LDO2_V[0]   |
| 0x03 | <b>LDO3</b>           | LDO3_T[2]      | LDO3_T[1]      | LDO3_T[0]   | LDO3_V[4]   | LDO3_V[3]   | LDO3_V[2]   | LDO3_V[1]   | LDO3_V[0]   |
| 0x04 | <b>LDO4</b>           | LDO4_T[2]      | LDO4_T[1]      | LDO4_T[0]   | LDO4_V[4]   | LDO4_V[3]   | LDO4_V[2]   | LDO4_V[1]   | LDO4_V[0]   |
| 0x05 | <b>LDO5</b>           | LDO5_T[2]      | LDO5_T[1]      | LDO5_T[0]   | LDO5_V[4]   | LDO5_V[3]   | LDO5_V[2]   | LDO5_V[1]   | LDO5_V[0]   |
| 0x06 | <b>LIL01</b>          | LIL01_T[2]     | LIL01_T[1]     | LIL01_T[0]  | LIL01_V[4]  | LIL01_V[3]  | LIL01_V[2]  | LIL01_V[1]  | LIL01_V[0]  |
| 0x07 | <b>LIL02</b>          | LIL02_T[2]     | LIL02_T[1]     | LIL02_T[0]  | LIL02_V[4]  | LIL02_V[3]  | LIL02_V[2]  | LIL02_V[1]  | LIL02_V[0]  |
| 0x08 | <b>BUCK1 V1</b>       | BUCK1_T[2]     | BUCK1_T[1]     | BUCK1_T[0]  | BUCK1_V1[4] | BUCK1_V1[3] | BUCK1_V1[2] | BUCK1_V1[1] | BUCK1_V1[0] |
| 0x09 | <b>BUCK1 V2</b>       | BUCK1_CL[1]    | BUCK1_CL[0]    | 0           | BUCK1_V2[4] | BUCK1_V2[3] | BUCK1_V2[2] | BUCK1_V2[1] | BUCK1_V2[0] |
| 0x0A | <b>BUCK2 V1</b>       | BUCK2_T[2]     | BUCK2_T[1]     | BUCK2_T[0]  | BUCK2_V1[4] | BUCK2_V1[3] | BUCK2_V1[2] | BUCK2_V1[1] | BUCK2_V1[0] |
| 0x0B | <b>BUCK2 V2</b>       | BUCK2_CL[1]    | BUCK2_CL[0]    | 0           | BUCK2_V2[4] | BUCK2_V2[3] | BUCK2_V2[2] | BUCK2_V2[1] | BUCK2_V2[0] |
| 0x0C | <b>BUCK CONTROL</b>   | BK2_FLAG MASK  | BK1_FLAG MASK  | PWM_BUCK2   | PDN_BUCK2   | 0           | 0           | PWM_BUCK1   | PDN_BUCK1   |
| 0x0D | <b>LDO CONTROL</b>    | LDO1_FLAG MASK | LIL02_EN       | LIL01_EN    | LDO5_EN     | LDO4_EN     | LDO3_EN     | LDO2_EN     | LDO1_EN     |
| 0x0E | <b>PULL DOWN BITS</b> | APU_TSD        | PDN_LIL02      | PDN_LIL01   | PDN_LDO5    | PDN_LDO4    | PDN_LDO3    | PDN_LDO2    | PDN_LDO1    |
| 0x0F | <b>STATUS BITS</b>    | REVISION[3]    | REVISION[2]    | REVISION[1] | REVISION[0] | LDO1_OKN    | B2_OKN      | B1_OKN      | TSD         |

**Table 9. Control Register Defaults**

| ADDR | LP8725 Defaults: DEFSEL state |           | LP8725-A Defaults: DEFSEL state |           | LP8725-B Defaults: DEFSEL state |           |
|------|-------------------------------|-----------|---------------------------------|-----------|---------------------------------|-----------|
|      | VIN1                          | GND       | VIN1                            | GND       | VIN1                            | GND       |
| 0x00 | 0101 1001                     | 0101 1001 | 0000 0000                       | 0101 0001 | 1101 1101                       | 1101 1101 |
| 0x01 | 1001 1001                     | 0011 0101 | 0001 0101                       | 1001 1001 | 1011 0101                       | 1010 1100 |
| 0x02 | 1000 1100                     | 0011 1001 | 0001 1101                       | 0111 1001 | 1111 1001                       | 1111 1001 |
| 0x03 | 1011 1111                     | 0101 1001 | 1111 1111                       | 0111 1001 | 1111 1001                       | 1111 1001 |
| 0x04 | 1001 1111                     | 0101 1001 | 0011 1101                       | 1001 1001 | 1110 0000                       | 1110 0000 |
| 0x05 | 1001 1001                     | 0011 1001 | 0001 1001                       | 1001 1001 | 1110 0000                       | 1110 0000 |
| 0x06 | 1010 1000                     | 0011 1111 | 0001 0000                       | 1011 0000 | 1111 0111                       | 1111 0111 |
| 0x07 | 0100 1000                     | 0000 1000 | 0010 0100                       | 1011 0000 | 1101 1111                       | 1101 1111 |
| 0x08 | 0000 0100                     | 0000 1000 | 1110 0110                       | 0000 1010 | 0000 1000                       | 0000 1000 |
| 0x09 | 1100 1000                     | 1100 0100 | 1100 0100                       | 1100 1000 | 1100 1000                       | 1100 1000 |
| 0x0A | 0101 0001                     | 0011 0001 | 1110 0110                       | 0000 1010 | 1001 0001                       | 1001 0001 |
| 0x0B | 1001 0001                     | 1001 0001 | 1000 0100                       | 1000 1000 | 1001 0001                       | 1001 0001 |
| 0x0C | 0111 1111                     | 0001 0001 | 1101 0001                       | 1101 0001 | 0001 0001                       | 0001 0001 |

**Table 9. Control Register Defaults (continued)**

| ADDR | LP8725 Defaults: DEFSEL state |           | LP8725-A Defaults: DEFSEL state |           | LP8725-B Defaults: DEFSEL state |           |
|------|-------------------------------|-----------|---------------------------------|-----------|---------------------------------|-----------|
|      | VIN1                          | GND       | VIN1                            | GND       | VIN1                            | GND       |
| 0x0D | 0111 1111                     | 0111 1111 | 1111 1011                       | 1111 1111 | 0100 0001                       | 0100 0001 |
| 0x0E | 0111 1111                     | 0111 1111 | 0111 1111                       | 0111 1111 | 0111 1111                       | 0111 1111 |
| 0x0F | 0000 0000                     | 0000 0000 | 0000 0000                       | 0000 0000 | 0000 0000                       | 0000 0000 |

| ADDR | LP8725-C Defaults: DEFSEL state |           | LP8725-D Defaults: DEFSEL state |           |
|------|---------------------------------|-----------|---------------------------------|-----------|
|      | VIN1                            | GND       | VIN1                            | GND       |
| 0x00 | 1101 1101                       | 1101 1101 | 1001 1101                       | 1001 1101 |
| 0x01 | 1001 0101                       | 1001 0101 | 1111 1001                       | 1111 1001 |
| 0x02 | 1001 1001                       | 1001 1001 | 1110 1100                       | 1110 1100 |
| 0x03 | 1011 1001                       | 1011 1001 | 0100 1100                       | 0100 1100 |
| 0x04 | 1011 0100                       | 1011 0100 | 1111 1101                       | 1111 1101 |
| 0x05 | 0101 1111                       | 0101 1111 | 1110 0000                       | 1110 1100 |
| 0x06 | 1000 1000                       | 1000 1000 | 0101 1101                       | 0101 1101 |
| 0x07 | 1000 1000                       | 1000 1000 | 0101 1101                       | 0101 1101 |
| 0x08 | 0000 1000                       | 0000 1000 | 0000 1010                       | 0000 1010 |
| 0x09 | 1100 1000                       | 1100 1000 | 1100 1010                       | 1100 1010 |
| 0x0A | 0101 0001                       | 0101 0001 | 0101 0001                       | 0101 0001 |
| 0x0B | 1001 0001                       | 1001 0001 | 1101 0001                       | 1101 0001 |
| 0x0C | 0001 0001                       | 0001 0001 | 0001 0001                       | 0001 0001 |
| 0x0D | 0111 1111                       | 0111 1111 | 0110 0100                       | 0110 0100 |
| 0x0E | 0111 1111                       | 0111 1111 | 0111 1111                       | 0111 1111 |
| 0x0F | 0000 0000                       | 0000 0000 | 0000 0000                       | 0000 0000 |

**Table 10. Register 0X00**

| Addr | Register | Bit 7    | Bit 6          | Bit 5 | Bit 4    | Bit 3  | Bit2   | Bit 1      | Bit 0    |
|------|----------|----------|----------------|-------|----------|--------|--------|------------|----------|
| 0x00 | GENERAL  | TIMESTEP | SHORT_TIMESTEP |       | BUCK2_EN | DVS2_V | DVS1_V | SLEEP_MODE | BUCK1_EN |

|                            |                                                                                                                                                                                                                                             |  |  |  |  |                                                                                                                 |  |  |  |
|----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|-----------------------------------------------------------------------------------------------------------------|--|--|--|
| BUCK1_EN<br>BUCK2_EN       | BUCK1, BUCK2 enable control                                                                                                                                                                                                                 |  |  |  |  |                                                                                                                 |  |  |  |
|                            | In STANDBY mode<br>1: During next STARTUP sequence will be enabled.<br>0: During next STARTUP sequence will be NOT enabled<br>For proper operation output timing having “111 - NO startup” should have corresponding enable bit 0 (disable) |  |  |  |  | In IDLE mode the bit has immediate effect.<br>1: Enable<br>0: Disable                                           |  |  |  |
| SLEEP_MODE                 | LDO Sleep Control<br>1: SLEEP mode<br>0: normal                                                                                                                                                                                             |  |  |  |  |                                                                                                                 |  |  |  |
| DVS1_V                     | 1: drive buck voltage to value stored in BUCK1_V1[4:0]<br>0: Buck output voltage controlled by external DVS pin.                                                                                                                            |  |  |  |  |                                                                                                                 |  |  |  |
| DVS2_V                     | 1: drive buck voltage to value stored in BUCK2_V1[4:0]<br>0: Buck output voltage to value stored in BUCK2_V2[4:0]                                                                                                                           |  |  |  |  |                                                                                                                 |  |  |  |
| SHORT_TIMESTEP<br>TIMESTEP | TIMESTEP = 0                                                                                                                                                                                                                                |  |  |  |  | TIMESTEP = 1                                                                                                    |  |  |  |
|                            | SHORT_TIMESTEP = 0 — time step t <sub>s</sub> = 32 μs<br>SHORT_TIMESTEP = 1 — time step t <sub>s</sub> = 64 μs                                                                                                                              |  |  |  |  | SHORT_TIMESTEP = 0 — time step t <sub>s</sub> = 128 μs<br>SHORT_TIMESTEP = 1— time step t <sub>s</sub> = 256 μs |  |  |  |

**Table 11. Registers 0x01-0x05, 0x06-0x07, 0x08-0x0B**

| Addr | Register   | Bit 7       | Bit 6       | Bit 5      | Bit 4       | Bit 3       | Bit 2       | Bit 1       | Bit 0       |
|------|------------|-------------|-------------|------------|-------------|-------------|-------------|-------------|-------------|
| 0x01 | LDO1 O/P   | LDO1_T[2]   | LDO1_T[1]   | LDO1_T[0]  | LDO1_V[4]   | LDO1_V[3]   | LDO1_V[2]   | LDO1_V[1]   | LDO1_V[0]   |
| 0x02 | LDO2 O/P   | LDO2_T[2]   | LDO2_T[1]   | LDO2_T[0]  | LDO2_V[4]   | LDO2_V[3]   | LDO2_V[2]   | LDO2_V[1]   | LDO2_V[0]   |
| 0x03 | LDO3 O/P   | LDO3_T[2]   | LDO3_T[1]   | LDO3_T[0]  | LDO3_V[4]   | LDO3_V[3]   | LDO3_V[2]   | LDO3_V[1]   | LDO3_V[0]   |
| 0x04 | LDO4 O/P   | LDO4_T[2]   | LDO4_T[1]   | LDO4_T[0]  | LDO4_V[4]   | LDO4_V[3]   | LDO4_V[2]   | LDO4_V[1]   | LDO4_V[0]   |
| 0x05 | LDO5 O/P   | LDO5_T[2]   | LDO5_T[1]   | LDO5_T[0]  | LDO5_V[4]   | LDO5_V[3]   | LDO5_V[2]   | LDO5_V[1]   | LDO5_V[0]   |
| 0x06 | LIL01 O/P  | LIL01_T[2]  | LIL01_T[1]  | LIL01_T[0] | LIL01_V[4]  | LIL01_V[3]  | LIL01_V[2]  | LIL01_V[1]  | LIL01_V[0]  |
| 0x07 | LIL02 O/P  | LIL02_T[2]  | LIL02_T[1]  | LIL02_T[0] | LIL02_V[4]  | LIL02_V[3]  | LIL02_V[2]  | LIL02_V[1]  | LIL02_V[0]  |
| 0x08 | BUCK1 O/P1 | BUCK1_T[2]  | BUCK1_T[1]  | BUCK1_T[0] | BUCK1_V1[4] | BUCK1_V1[3] | BUCK1_V1[2] | BUCK1_V1[1] | BUCK1_V1[0] |
| 0x09 | BUCK1 O/P2 | BUCK1_CL[1] | BUCK1_CL[0] |            | BUCK1_V2[4] | BUCK1_V2[3] | BUCK1_V2[2] | BUCK1_V2[1] | BUCK1_V2[0] |
| 0x0A | BUCK2 O/P1 | BUCK2_T[2]  | BUCK2_CL[2] | BUCK2_T[0] | BUCK2_V1[4] | BUCK2_V1[3] | BUCK2_V1[2] | BUCK2_V1[1] | BUCK2_V1[0] |
| 0x0B | BUCK2 O/P2 | BUCK2_CL[1] | BUCK2_CL[0] |            | BUCK2_V2[4] | BUCK2_V2[3] | BUCK2_V2[2] | BUCK2_V2[1] | BUCK2_V2[0] |

| Registers 0x01 - 0x05 | Output Voltage Selection |       |       |       |       |       |       |       |
|-----------------------|--------------------------|-------|-------|-------|-------|-------|-------|-------|
| LDO1_V[4:0]           | 00000                    | 1.20V | 01000 | 1.60V | 10000 | 2.10V | 11000 | 2.75V |
| LDO2_V[4:0]           | 00001                    | 1.25V | 01001 | 1.65V | 10001 | 2.20V | 11001 | 2.80V |
| LDO3_V[4:0]           | 00010                    | 1.30V | 01010 | 1.70V | 10010 | 2.30V | 11010 | 2.85V |
| LDO4_V[4:0]           | 00011                    | 1.35V | 01011 | 1.75V | 10011 | 2.40V | 11011 | 2.90V |
| LDO5_V[4:0]           | 00100                    | 1.40V | 01100 | 1.80V | 10100 | 2.50V | 11100 | 2.95V |
|                       | 00101                    | 1.45V | 01101 | 1.85V | 10101 | 2.60V | 11101 | 3.00V |
|                       | 00110                    | 1.50V | 01110 | 1.90V | 10110 | 2.65V | 11110 | 3.10V |
|                       | 00111                    | 1.55V | 01111 | 2.00V | 10111 | 2.70V | 11111 | 3.30V |

| Registers 0x06 - 0x07 | Output Voltage Selection |       |       |       |       |       |       |       |
|-----------------------|--------------------------|-------|-------|-------|-------|-------|-------|-------|
| LIL01_V[4:0]          | 00000                    | 0.80V | 01000 | 1.20V | 10000 | 1.80V | 11000 | 2.60V |
| LIL02_V[4:0]          | 00001                    | 0.85V | 01001 | 1.25V | 10001 | 1.90V | 11001 | 2.70V |
|                       | 00010                    | 0.90V | 01010 | 1.30V | 10010 | 2.00V | 11010 | 2.80V |
|                       | 00011                    | 0.95V | 01011 | 1.35V | 10011 | 2.10V | 11011 | 2.85V |
|                       | 00100                    | 1.00V | 01100 | 1.40V | 10100 | 2.20V | 11100 | 2.90V |
|                       | 00101                    | 1.05V | 01101 | 1.50V | 10101 | 2.30V | 11101 | 3.00V |
|                       | 00110                    | 1.10V | 01110 | 1.60V | 10110 | 2.40V | 11110 | 3.10V |
|                       | 00111                    | 1.15V | 01111 | 1.70V | 10111 | 2.50V | 11111 | 3.30V |

| Registers 0x08 - 0x0B | Output Voltage Selection |       |       |       |       |       |       |       |
|-----------------------|--------------------------|-------|-------|-------|-------|-------|-------|-------|
| BUCK1_V[4:0]          | 00000                    | 0.80V | 01000 | 1.20V | 10000 | 1.75V | 11000 | 2.40V |
| BUCK2_V[4:0]          | 00001                    | 0.85V | 01001 | 1.25V | 10001 | 1.80V | 11001 | 2.50V |
|                       | 00010                    | 0.90V | 01010 | 1.30V | 10010 | 1.85V | 11010 | 2.60V |
|                       | 00011                    | 0.95V | 01011 | 1.35V | 10011 | 1.90V | 11011 | 2.70V |
|                       | 00100                    | 1.00V | 01100 | 1.40V | 10100 | 2.00V | 11100 | 2.80V |
|                       | 00101                    | 1.05V | 01101 | 1.50V | 10101 | 2.10V | 11101 | 2.85V |
|                       | 00110                    | 1.10V | 01110 | 1.60V | 10110 | 2.20V | 11110 | 2.90V |
|                       | 00111                    | 1.15V | 01111 | 1.70V | 10111 | 2.30V | 11111 | 3.00V |

| Registers 0x01 - 0x08, 0x0A                                                                                                             | Startup Delay Selection                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LDO1_T[2:0]<br>LDO2_T[2:0]<br>LDO3_T[2:0]<br>LDO4_T[2:0]<br>LDO5_T[2:0]<br>LILO1_T[2:0]<br>LILO2_T[2:0]<br>BUCK1_T[2:0]<br>BUCK2_T[2:0] | 000 - startup delay 0<br>001 - startup delay = 1 * time step $t_s$<br>010 - startup delay = 2 * time step $t_s$<br>011 - startup delay = 3 * time step $t_s$<br>100 - startup delay = 4 * time step $t_s$<br>101 - startup delay = 5 * time step $t_s$<br>110 - startup delay = 6 * time step $t_s$<br>111 - NO startup<br>For proper startup operation "NO startup" <111> should have the corresponding enable bit in registers 0x00 & 0x0D set to 0 (disable) |

| Registers 0x09, 0x0B           | Buck Current Limit Selection                                                                                                                                                   |
|--------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BUCK1_CL[1:0]<br>BUCK2_CL[1:0] | 00 - 460 mA peak (250 mA max $I_{OUT}$ )<br>01 - 780 mA peak (450 mA max $I_{OUT}$ )<br>10 - 1050 mA peak (600 mA max $I_{OUT}$ )<br>11 - 1370 mA peak (800 mA max $I_{OUT}$ ) |

| Register 0x0C                  |                                                                                                    |
|--------------------------------|----------------------------------------------------------------------------------------------------|
| PDN_BUCK1<br>PDN_BUCK2         | Pull-down BUCK1/2:<br>1 - Pull down enabled<br>0 - Pull down disabled                              |
| PWM_BUCK1<br>PWM_BUCK2         | 1 - BUCK1/2 is forced to work in PWM mode<br>0 - BUCK1/2 works in automatic ECO/PWM selection mode |
| BK1_FLAG MASK<br>BK2_FLAG MASK | 1 - Mask the BUCK OK flag<br>0 - No masking of BUCK OK flag                                        |

| Register 0x0D                                                               | LDO Enable Control                                                                                                             |                                                                         |
|-----------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------|
| LDO1_EN<br>LDO2_EN<br>LDO3_EN<br>LDO4_EN<br>LDO5_EN<br>LILO1_EN<br>LILO2_EN | In STANDBY mode:<br>1 - During next STARTUP sequence will be enabled.<br>0 - During next startup sequence will be NOT enabled. | In IDLE mode the bit has immediate effect.<br>1 - Enable<br>0 - Disable |
| LDO1_FLAG MASK                                                              | 1 - Mask the LDO1 OK flag<br>0 - No masking of LDO1 OK flag                                                                    |                                                                         |

| Register 0x0E                                                               | Pull Down                                                                                                                                                                                                                                                                                                                                            |
|-----------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PDNLDO1<br>PDNLDO2<br>PDNLDO3<br>PDNLDO4<br>PDNLDO5<br>PDNLILO1<br>PDNLILO2 | LDO pull-down control<br>1 - Pull down enabled<br>0 - Pull down disabled                                                                                                                                                                                                                                                                             |
| APU_TSD                                                                     | This bit defines either to reset registers or not before the PMU automatically starts startup sequence from Thermal Shutdown after cooling down if EN-pin is High.<br>1 - No change to registers - content stays the same as before Thermal Shutdown.<br>0 - If CONFIG = '1' Reset registers to default values before startup from Thermal Shutdown. |

**Table 12. Register 0x0F (Read Only Register)**

| Addr                         | Register | Bit 7                                                                            | Bit 6       | Bit 5       | Bit 4       | Bit 3        | Bit 2  | Bit 1  | Bit 0 |
|------------------------------|----------|----------------------------------------------------------------------------------|-------------|-------------|-------------|--------------|--------|--------|-------|
| 0x10                         | STATUS   | REVISION[3]                                                                      | REVISION[2] | REVISION[1] | REVISION[0] | LDO1_OK<br>N | B2_OKN | B1_OKN | TSD   |
| TSD                          |          | 1 - Device is in Thermal Shutdown<br>0 - Device is NOT in Thermal Shutdown       |             |             |             |              |        |        |       |
| B1_OKN<br>B2_OKN<br>LDO1_OKN |          | 1 - Output voltage not in regulation<br>0 - Output voltage in regulation         |             |             |             |              |        |        |       |
| REVISION[3:0]                |          | LP8725 Mask set revision.<br>To be incremented, whenever the mask set is edited. |             |             |             |              |        |        |       |

## OPERATION DESCRIPTION

### Device Information

Using voltage mode architecture with synchronous rectification, the LP8725 has the ability to deliver up to 800 mA per DC-DC convertor depending on the input voltage and output voltage, ambient temperature, and the inductor chosen.

There are two modes of operation depending on the current required - PWM (Pulse Width Modulation), and ECO. The device operates in PWM mode at load currents of approximately 75 mA (typ.) or higher. Lighter output current loads cause the device to automatically switch into ECO mode for reduced current consumption.

### Circuit Operation

The DC-DC convertor operates as follows. During the first portion of each switching cycle, the control block in the turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of  $(V_{IN} - V_{OUT})/L$ , by storing energy in a magnetic field. During the second portion of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of  $-V_{OUT}/L$ .

The output filter stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load. The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at the SW pin to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

### PWM Operation

During PWM operation the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve excellent load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward inversely proportional to the input voltage is introduced. While in PWM mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. Then the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.

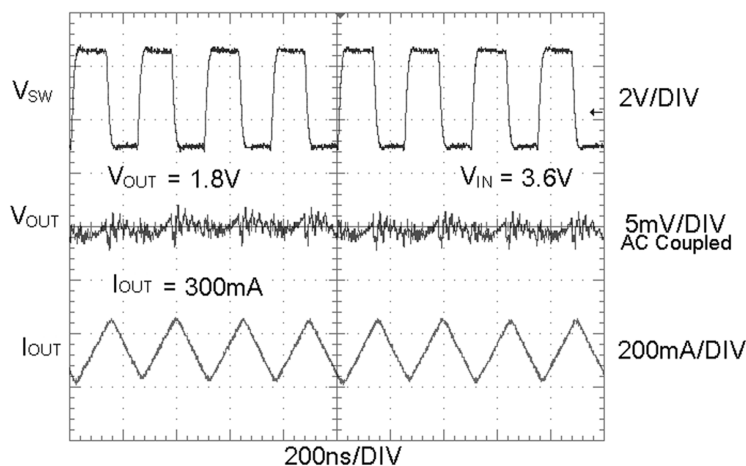


Figure 13. Typical PWM Operation

## Internal Synchronous Rectification

While in PWM mode, the DC-DC converter uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

## Current Limiting

A current limit feature allows the DC-DC converter to protect itself and external components during overload conditions. PWM mode implements current limit using an internal comparator that trips at 1.05A (typ.) assuming  $I_{OUT} = 600\text{ mA}$ . If the output is shorted to ground and output voltage becomes lower than 0.3V (typ.), the device enters a timed current limit mode where the switching frequency will be one fourth, and NFET synchronous rectifier is disabled, thereby preventing excess current and thermal runaway.

The current limit for each DC-DC converter is selectable via serial interface by registers 0x09 bits 6, 7 and 0x0B bits 6, 7. The current limit selected should be ~ 1.5x to 2x greater than the output current required.

## ECO Mode Operation

By default the DC-DC converter will be in Auto (ECO/PWM) Mode. By doing so the part switches from ECO (Economy) state to PWM (Pulse Width Modulation) state based on output load current. At light loads (less than 75mA approx) the converter enters ECO mode. In this mode the part operates with low  $I_q$ . During ECO operation the converter positions the output voltage slightly higher (+30mV typ.) than the nominal output voltage in PWM operation. Because the reference is set higher, the output voltage increases to reach the target voltage when the part goes from sleep state to switching state. Once this voltage is reached the converter enters sleep mode, thereby reducing switching losses and improving light load efficiency. The output voltage ripple is slightly higher in ECO mode (30mV p-p typ.).

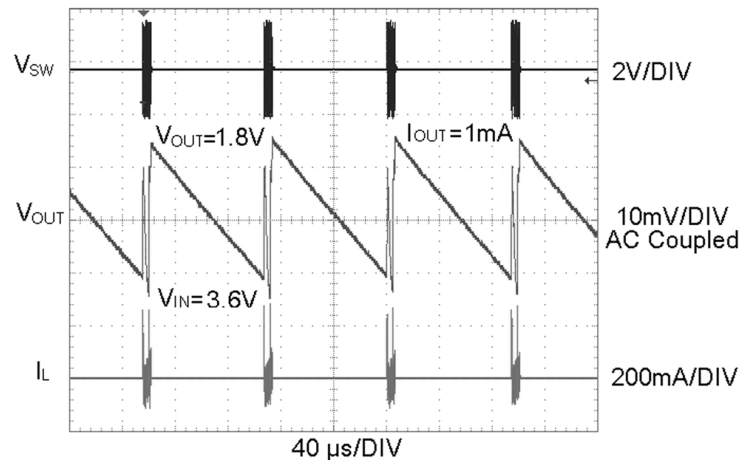


Figure 14. Typical ECO Operation

Note that ground noise may impact quiescent current in ECO mode and care at board layout is important to minimize this risk. See section on layout guidelines.

## Startup

The LP8725 bucks have a 'soft-start' feature to limit the in-rush current. This prevents large current spikes and voltage overshoot and also limits the cases in which the inductor may saturate. At or close to 0V the inrush current to the capacitor (and load) is limited to its short circuit protection limit of typically 500 mA. Above a threshold of around 150 mV, the current limit is increased to the buck's peak current limit set by the control registers. (For a 600 mA max load this is set to approx. 1050 mA.)

While in short-circuit protection, the output switches off, but will continue to attempt to restart. If the total capacitance on the buck output is large or if the inductor value drops too low, the threshold might never be reached, so the buck may not start. See [Inductor Selection](#) and [Output Capacitor Selection](#) sections.



## Stability

The stability of the buck is optimized for the 4.7  $\mu\text{F}$  capacitors recommended in the datasheet. Either too small or too large a capacitance can cause an oscillation at the output and/or excessive ringing during load transients. It is advisable not to exceed a total of 15  $\mu\text{F}$  capacitance at the output. See [Table 14](#) for recommended output capacitors.

See also the recommended inductors table ([Table 13](#)) as stability may be compromised by the use of inductors whose actual value may change significantly from its nominal value due to the operating conditions. This may be the case for the smaller case size chip inductors.

## APPLICATION INFORMATION

### Inductor Selection

DC bias current characteristics of inductors must be considered. Different manufacturers follow different saturation current rating specifications, so attention must be given to details. DC bias curves should be requested from them as part of the inductor selection process.

**Minimum value of inductance to guarantee good performance is 0.5  $\mu$ H at 1.5A ( $I^{LIM}$  typ.) bias current over the ambient temp range.** The inductor's DC resistance should be less than 0.1 $\Omega$  for good efficiency at high current condition. The inductor AC loss (resistance) also affects conversion efficiency. Higher Q factor at switching frequency usually gives better efficiency at light load to medium load instead. [Table 13](#) lists suggested inductors and suppliers.

### Input Capacitor Selection

A ceramic input capacitor of 4.7 $\mu$ F, 6.3V/10V is sufficient for most applications. Place the input capacitor as close as possible to the  $V_{IN}$  pin and GND pin of the device. A larger value or higher voltage rating may be used to improve input voltage filtering. Use X7R, X5R or B types, do not use Y5V or F.

**Minimum input capacitance to guarantee good performance is 4.7  $\mu$ F at maximum input voltage DC bias including tolerances and over ambient temp range.** The input filter capacitor supplies current to the PFET (high-side) switch in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select an input filter capacitor with sufficient ripple current rating. The input current ripple can be calculated as:

$$I_{RMS} = I_{OUTMAX} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times 1 - \frac{V_{OUT}}{V_{IN}} + \frac{r^2}{12}} \quad (1)$$

$$\text{where } r = \frac{(V_{in} - V_{out}) \times V_{out}}{L \times f \times I_{outmax} \times V_{in}} \quad (2)$$

### Output Capacitor Selection

Use a 4.7 $\mu$ F, 6.3V ceramic capacitor, X7R, X5R or B types, do not use Y5V or F. DC bias voltage characteristics of ceramic capacitors must be considered. DC bias characteristics vary from manufacturer to manufacturer and DC bias curves should be requested from them as part of the capacitor selection process. The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

**Minimum output capacitance to guarantee good performance is 2.2  $\mu$ F at the output voltage DC bias including tolerances and over ambient temp range.** The output voltage ripple is caused by the charging and discharging of the output capacitor and also due to its ESR and can be calculated as:

$$\text{Voltage peak to peak ripple due to capacitance} = V_{PP-C} = \frac{I_{RIPPLE}}{4 \times f \times C}$$

$$\text{Voltage peak-to-peak ripple due to ESR} = V_{PP-ESR} = (2 \times I_{RIPPLE}) \times R_{ESR}$$

Because these two components are out of phase the rms value can be used to get an approximate value of peak-to-peak ripple.

$$\text{Voltage peak-to-peak ripple, root mean squared} = V_{PP-RMS} = \sqrt{V_{PP-C}^2 + V_{PP-ESR}^2}$$

Note that the output ripple is dependent on the current ripple and the equivalent series resistance of the output capacitor (ESR). The RESR is frequency dependent (as well as temperature dependent); make sure the value used for calculations is at the switching frequency of the part.

[Table 14](#) lists suggested capacitors and suppliers.

**Table 13. Suggested Inductors and Suppliers**

| Model          | Vendor    | Dimensions LxWxH (mm)  | DCR (mΩ) |
|----------------|-----------|------------------------|----------|
| LQM2HPN 1R0MG0 | Murata    | 2.5 x 2.0 x 1.0 (Max)  | 55       |
| MIPSZ2520D1R0  | FDK       | 2.5 x 2.0 x 1.0 (Max)  | 90       |
| MIPSZ2012D1R0  | FDK       | 2.0 x 1.25 x 1.0 (Max) | 90       |
| LPS3010-102NLC | Coilcraft | 3.3 x 3.3 x 1.0 (Max)  | 85       |

**Table 14. Suggested Capacitors and Suppliers**

| Model                                           | Type    | Vendor | Voltage Rating | Case Size Inch (mm) |
|-------------------------------------------------|---------|--------|----------------|---------------------|
| 4.7 μF for C <sub>IN</sub> and C <sub>OUT</sub> |         |        |                |                     |
| C1608X5R0J475K                                  | Ceramic | TDK    | 6.3            | 0603 (1608)         |
| C1608X5R1A475K                                  | Ceramic | TDK    | 10             | 0603 (1608)         |

## Dynamic Voltage Scaling

Buck 1 and Buck 2 can be switched between two output values stored in registers 0x08 and 0x09 for Buck1 and 0x0A and 0x0B for Buck2.

For Buck 2 output this control is achieved by changing the DVS2\_V bit in the GENERAL register 0x00 (bit 3).

| DVS2_V       | OUTPUT   |               |
|--------------|----------|---------------|
| Reg0x00 Bit3 |          |               |
| 0            | BUCK2_V2 | Reg 0x0B[4-0] |
| 1            | BUCK2_V1 | Reg 0x0A[4-0] |

For Buck 1 this control can be either via the external DVS pin or via the DVS1\_V bit in the GENERAL register 0x00 (bit 2). The control configurations are shown in the following table.

| DVS1         | DVS pin | OUTPUT   |               |
|--------------|---------|----------|---------------|
| Reg0x00 Bit2 |         |          |               |
| 0            | 0       | BUCK1_V2 | Reg 0x09[4-0] |
| 0            | 1       | BUCK1_V1 | Reg 0x08[4-0] |
| 1            | 0       | BUCK1_V2 | Reg 0x09[4-0] |
| 1            | 1       | BUCK1_V1 | Reg 0x08[4-0] |

## LDO Information

There are all together 7 LDOs in LP8725 grouped as

- DIGITAL;
- ANALOG; and
- LOW INPUT LOW OUTPUT (LILO)

All LDOs can be programmed through serial interface for different output voltage values, which are summarized in the output voltage selection tables.

At the PMU power on, LDOs startup according to the selected startup sequence and the default voltages. See STARTUP and SHUTDOWN Sequences for details.

For stability all LDOs need to have external capacitors C<sub>OUT</sub> connected to the output with recommended value of 1μF. It is important to select the type of capacitor whose capacitance will in no case (voltage, temperature, etc) be outside of limits specified in the LDO electrical characteristics.

## Analog-Type LDOs

The analog LDOs are optimized for supplying analog loads having ULTRA LOW NOISE (10  $\mu$ V<sub>RMS</sub> for  $I_{OUT} > 5\text{mA}$ ) and excellent PSRR (70 dB at 10 kHz) performance. They can be programmed through serial interface for different output voltage values.

For fast discharging of output capacitors in shutdown, the LDOs may be connected to a 300 $\Omega$  pull down resistor to output.

In sleep mode quiescent current is lowered down to 30  $\mu$ A for energy saving. In this mode these LDOs should not loaded more than 3-5 mA of output current.

## Digital-Type LDOs

The Digital LDOs are optimized for dynamic performance for fast changing digital loads whilst consuming very little quiescent current  $\sim 20 \mu\text{A}$ . They can be programmed through serial interface for different output voltage values.

For fast discharging of output capacitors in shutdown, the LDOs may be connected to a 300 $\Omega$  pull down resistor to output.

In sleep mode quiescent current is lowered down to 10  $\mu$ A for energy saving. In this mode these LDOs should not loaded more than 3-5 mA of output current.

## LILO-Type LDOs

The LILO-type LDO is optimized for low output voltage and for good dynamic performance to supply different fast changing (digital) loads. These LDOs can be operated as digital LDOs also albeit with lower PSRR and Noise performance.

An innovative design of the all the LDOs reduces sensitivity to the placement of the output capacitor. The output capacitor may not be placed as close as possible to the output pin, like on conventional LDOs. The general purpose LDOs do not need output capacitor close to the PMU. If a (1  $\mu$ F or more) capacitor is attached to a circuit load, customer may skip the output capacitor at the PMU.

## I<sup>2</sup>C-Compatible Serial Bus Interface

### Interface Bus Overview

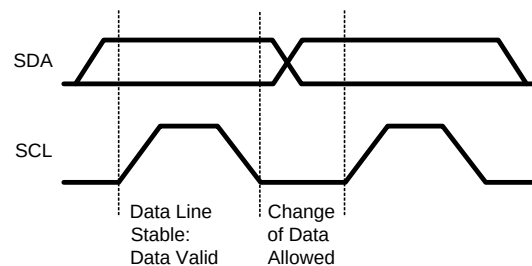
The I<sup>2</sup>C-compatible synchronous serial interface provides access to the programmable functions and registers on the device.

This protocol uses a two-wire interface for bi-directional communications between the ICs connected to the bus. The two interface lines are the Serial Data Line (SDA), and the Serial Clock Line (SCL). These lines should be connected to a positive supply, via a pull-up resistor of 1.5 K $\Omega$  and remain HIGH even when the bus is idle.

Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the serial clock (SCL).

### Data Transactions

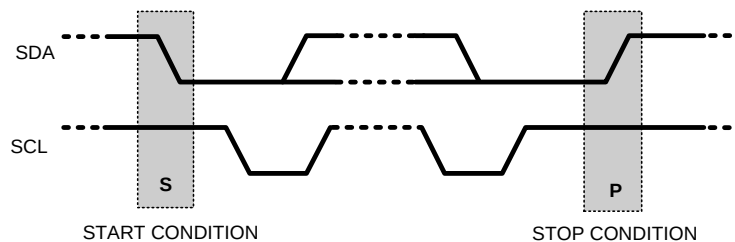
One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

**Figure 15. Bit Transfer**

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow. The following sections provide further details of this process.

### Start and Stop

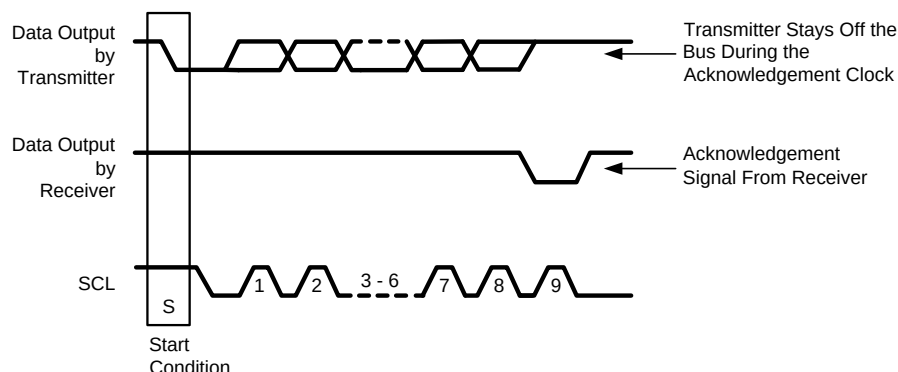
The Master device on the bus always generates the Start and Stop Conditions (control codes). After a Start Condition is generated, the bus is considered busy and it retains this status until a certain time after a Stop Condition is generated. A high-to-low transition of the data line (SDA) while the clock (SCL) is high indicates a Start Condition. A low-to-high transition of the SDA line while the SCL is high indicates a Stop Condition.

**Figure 16. Start and Stop Conditions**

In addition to the first Start Condition, a repeated Start Condition can be generated in the middle of a transaction. This allows another device to be accessed, or a register read cycle.

### Acknowledge Cycle

The Acknowledge Cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device. The master generates the acknowledge clock pulse on the ninth clock pulse of the byte transfer. The transmitter releases the SDA line (permits it to go high) to allow the receiver to send the acknowledge signal. The receiver must pull down the SDA line during the acknowledge clock pulse and ensure that SDA remains low during the high period of the clock pulse, thus signaling the correct reception of the last data byte and its readiness to receive the next byte.



**Figure 17. Bus Acknowledge Cycle**

### "Acknowledge after Every Byte" Rule

The master generates an acknowledge clock pulse after each byte transfer. The receiver sends an acknowledge signal after every byte received.

There is one exception to the "acknowledge after every byte" rule.

When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging ("negative acknowledge") the last byte clocked out of the slave. This "negative acknowledge" still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

### Addressing Transfer Formats

Each device on the bus has a unique slave address. The LP8725 operates as a slave device. Slave address is selectable by CONFIG and DEFSEL pins.

For the actual slave addresses, see [Table 1](#).

Before any data is transmitted, the master transmits the address of the slave being addressed. The slave device should send an acknowledge signal on the SDA line, once it recognizes its address.

The slave address is the first seven bits after a Start Condition. The direction of the data transfer (R/W) depends on the bit sent after the slave address the eighth bit.

When the slave address is sent, each device in the system compares this slave address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending upon the state of the R/W bit (1:read, 0:write), the device acts as a transmitter or a receiver.

### Control Register Write Cycle

- Master device generates start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = '0').
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.
- Slave sends acknowledge signal.
- If master will send further data bytes the control register address will be incremented by one after acknowledge signal.
- Write cycle ends when the master creates stop condition.

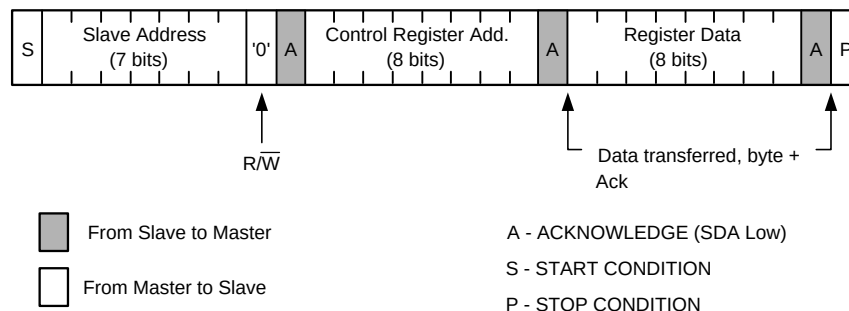
### Control Register Read Cycle

- Master device generates a start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = '0').
- Slave device sends acknowledge signal if the slave address is correct.

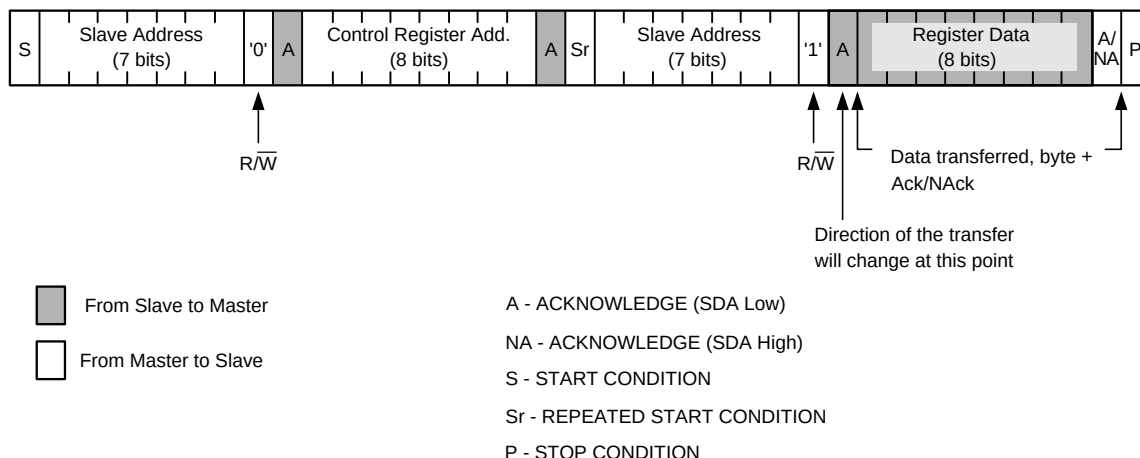
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master device generates repeated start condition.
- Master sends the slave address (7 bits) and the data direction bit (r/w = "1").
- Slave sends acknowledge signal if the slave address is correct.
- Slave sends data byte from addressed register.
- If the master device sends acknowledge signal, the control register address will be incremented by one. Slave device sends data byte from addressed register.
- Read cycle ends when the master does not generate acknowledge signal after data byte and generates stop condition.

|                                          | Address Mode                                                                                                                                                                                                                                                         |
|------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Data Read                                | <Start Condition><br><Slave Address><r/w = '0'>[Ack]<br><Register Addr.>[Ack]<br><Repeated Start Condition><br><Slave Address><r/w = '1'>[Ack]<br>[Register Data]<Ack or NAck><br>... additional reads from subsequent register address possible<br><Stop Condition> |
| Data Write                               | <Start Condition><br><Slave Address><r/w = '0'>[Ack]<br><Register Addr.>[Ack]<br><Register Data>[Ack]<br>... additional writes to subsequent register address possible<br><Stop Condition>                                                                           |
| < > Data from master [ ] Data from slave |                                                                                                                                                                                                                                                                      |

### Register Read and Write Detail



**Figure 18. Register Write Format**



**Figure 19. Register Read Format**

## Layout Guidelines

As for all DC-DC buck regulators board layout is very important to ensure best performance.

The 4.7  $\mu$ F input capacitors should be placed first, as near to VINB1/2 pin and GNDB1/2 as possible. VINB1/2 are the voltage rails for the high-side power FETs. GNDB1/2 are the return paths for the low-side power FETs. The input capacitors should have their associated pads very near the pins that they will decouple. These capacitors are important in sourcing charge during switching events. In this device we have the two buck inputs side by side but we recommend that separate traces are taken to each device pin to ensure this proper decoupling. This can be seen in the example layout shown in the layout scheme below.

The 4.7  $\mu$ F output capacitors should be the next components to be placed in conjunction with the inductor. The switch node should be kept as small as possible but otherwise the inductor placement is least sensitive to layout variation. Best performance of the LP8725 will be realized by maintaining tight physical coupling of the grounds of the input capacitor, output capacitor and GND pin for each switcher. The inductor should be placed in a way that best allows the switching node, output node, and track to the load circuit to be routed easily.

The grounding is very important and any additional resistance/inductance should be minimized. A ground polygon and/or plane should be used to tie all capacitor grounds together and directly to the buck GNDs. See the layout scheme below as an example.

Finally, the feedback nets should be routed, where possible route this away from any switching nodes and tie into the output node of the regulator. The FB lines should closely match the GND routing to reduce the inductive loop of this pair. The FB and GND lines make up a high-side and low-side sense connection to maintain the accuracy of the switcher outputs. If the FB line should cross the switching trace make this as close to perpendicular as possible.

Low impedance power connections should be maintained for all of these connections. Care should also be given to the ground routing for input lines and output lines to minimize inductive loops, normally this should be taken care of by suitable ground planes.

As this is a dual buck device there are a number of aspects to be aware of. The switchers are almost a complete mirror image of one another on the part which leads to the possibility of symmetrical placement and layout about the part. Symmetrical layout will give best matching between the two buck devices. However we recommend that the inputs are kept separate into the device. There are some compromises that have to be considered. In the case of our example we have used vias to route the VINB12 and VINB2 to allow the close placement of the input capacitors. The switch node must also be routed via layer2 on the board. Here we have placed a number of vias to reduce any additional impedance.



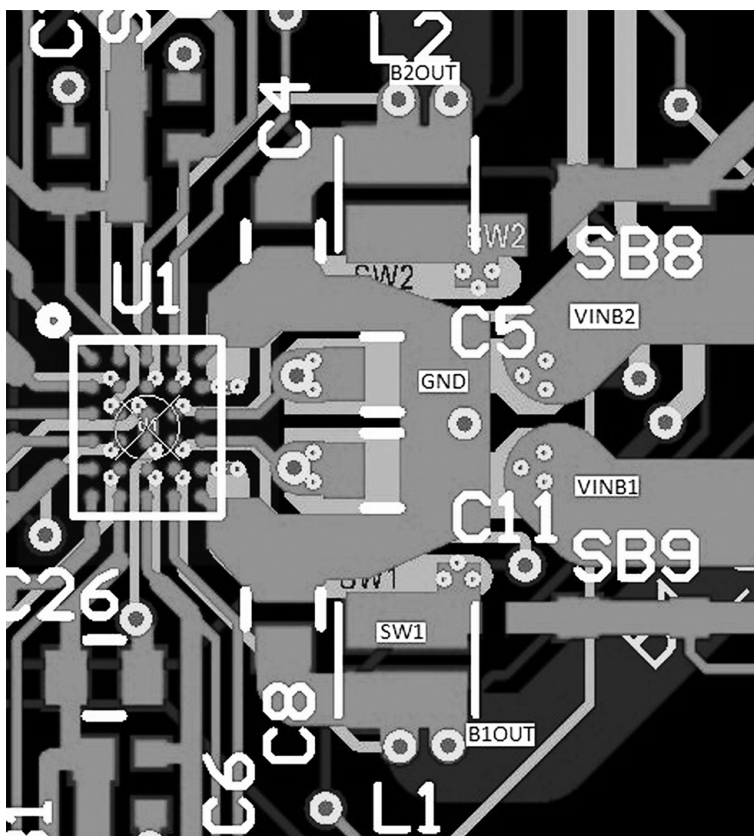


Figure 20. Layout Scheme used on Eval Board

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| LP8725TLE-A/NOPB | NRND          | DSBGA        | YZR                | 30   | 250            | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 85    | V023                    |                         |
| LP8725TLE-B/NOPB | NRND          | DSBGA        | YZR                | 30   | 250            | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 85    | V028                    |                         |
| LP8725TLE-C/NOPB | ACTIVE        | DSBGA        | YZR                | 30   | 250            | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 85    | V040                    | <a href="#">Samples</a> |
| LP8725TLE-D/NOPB | NRND          | DSBGA        | YZR                | 30   | 250            | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   |              | V031                    |                         |
| LP8725TLE/NOPB   | NRND          | DSBGA        | YZR                | 30   | 250            | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 85    | 8725                    |                         |
| LP8725TLX-A/NOPB | NRND          | DSBGA        | YZR                | 30   | 3000           | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 85    | V023                    |                         |
| LP8725TLX-B/NOPB | NRND          | DSBGA        | YZR                | 30   | 3000           | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 85    | V028                    |                         |
| LP8725TLX-C/NOPB | ACTIVE        | DSBGA        | YZR                | 30   | 3000           | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 85    | V040                    | <a href="#">Samples</a> |
| LP8725TLX-D/NOPB | ACTIVE        | DSBGA        | YZR                | 30   | 3000           | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   |              | V031                    | <a href="#">Samples</a> |
| LP8725TLX/NOPB   | ACTIVE        | DSBGA        | YZR                | 30   | 3000           | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 85    | 8725                    | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

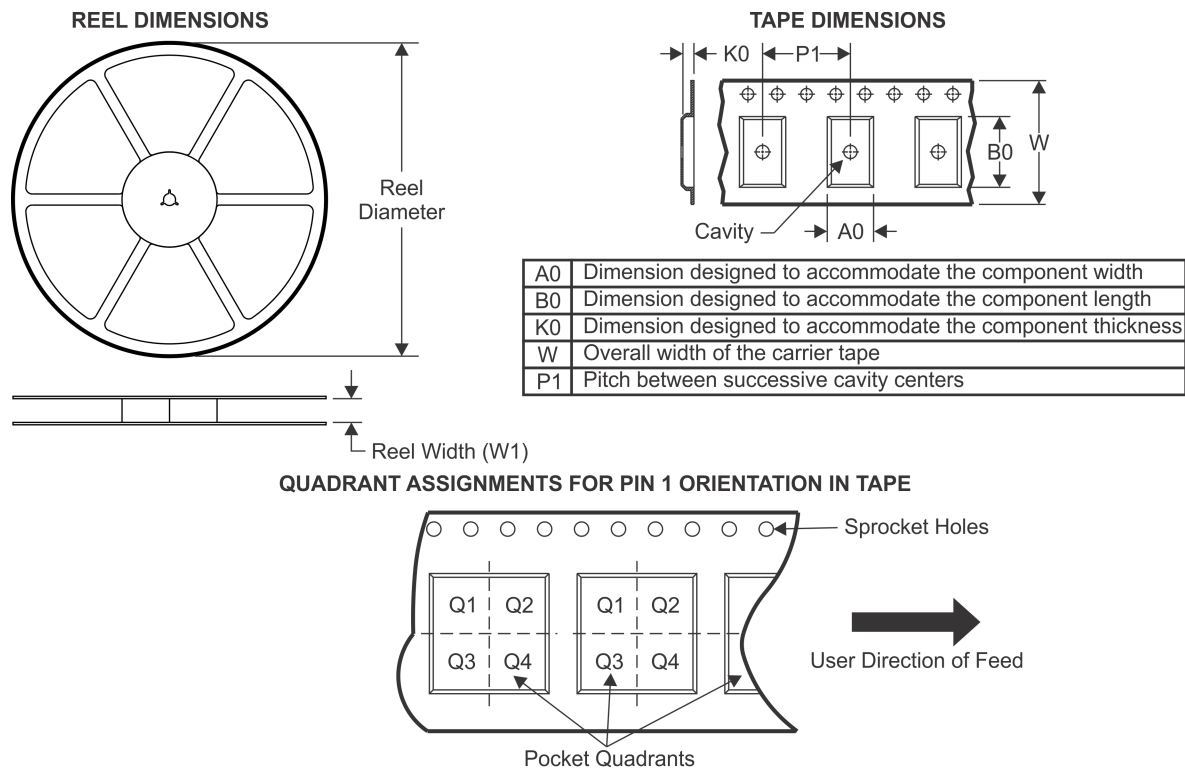
<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

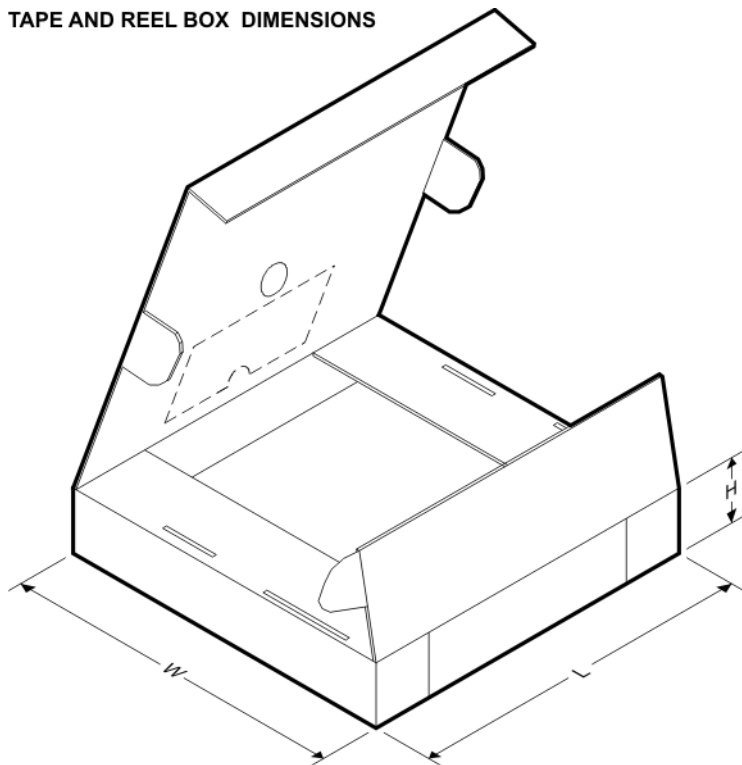
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LP8725TLE-A/NOPB | DSBGA        | YZR             | 30   | 250  | 178.0              | 8.4                | 2.74    | 3.15    | 0.76    | 4.0     | 8.0    | Q1            |
| LP8725TLE-B/NOPB | DSBGA        | YZR             | 30   | 250  | 178.0              | 8.4                | 2.74    | 3.15    | 0.76    | 4.0     | 8.0    | Q1            |
| LP8725TLE-C/NOPB | DSBGA        | YZR             | 30   | 250  | 178.0              | 8.4                | 2.74    | 3.15    | 0.76    | 4.0     | 8.0    | Q1            |
| LP8725TLE-D/NOPB | DSBGA        | YZR             | 30   | 250  | 178.0              | 8.4                | 2.74    | 3.15    | 0.76    | 4.0     | 8.0    | Q1            |
| LP8725TLE/NOPB   | DSBGA        | YZR             | 30   | 250  | 178.0              | 8.4                | 2.74    | 3.15    | 0.76    | 4.0     | 8.0    | Q1            |
| LP8725TLX-A/NOPB | DSBGA        | YZR             | 30   | 3000 | 178.0              | 8.4                | 2.74    | 3.15    | 0.76    | 4.0     | 8.0    | Q1            |
| LP8725TLX-B/NOPB | DSBGA        | YZR             | 30   | 3000 | 178.0              | 8.4                | 2.74    | 3.15    | 0.76    | 4.0     | 8.0    | Q1            |
| LP8725TLX-C/NOPB | DSBGA        | YZR             | 30   | 3000 | 178.0              | 8.4                | 2.74    | 3.15    | 0.76    | 4.0     | 8.0    | Q1            |
| LP8725TLX-D/NOPB | DSBGA        | YZR             | 30   | 3000 | 178.0              | 8.4                | 2.74    | 3.15    | 0.76    | 4.0     | 8.0    | Q1            |
| LP8725TLX/NOPB   | DSBGA        | YZR             | 30   | 3000 | 178.0              | 8.4                | 2.74    | 3.15    | 0.76    | 4.0     | 8.0    | Q1            |

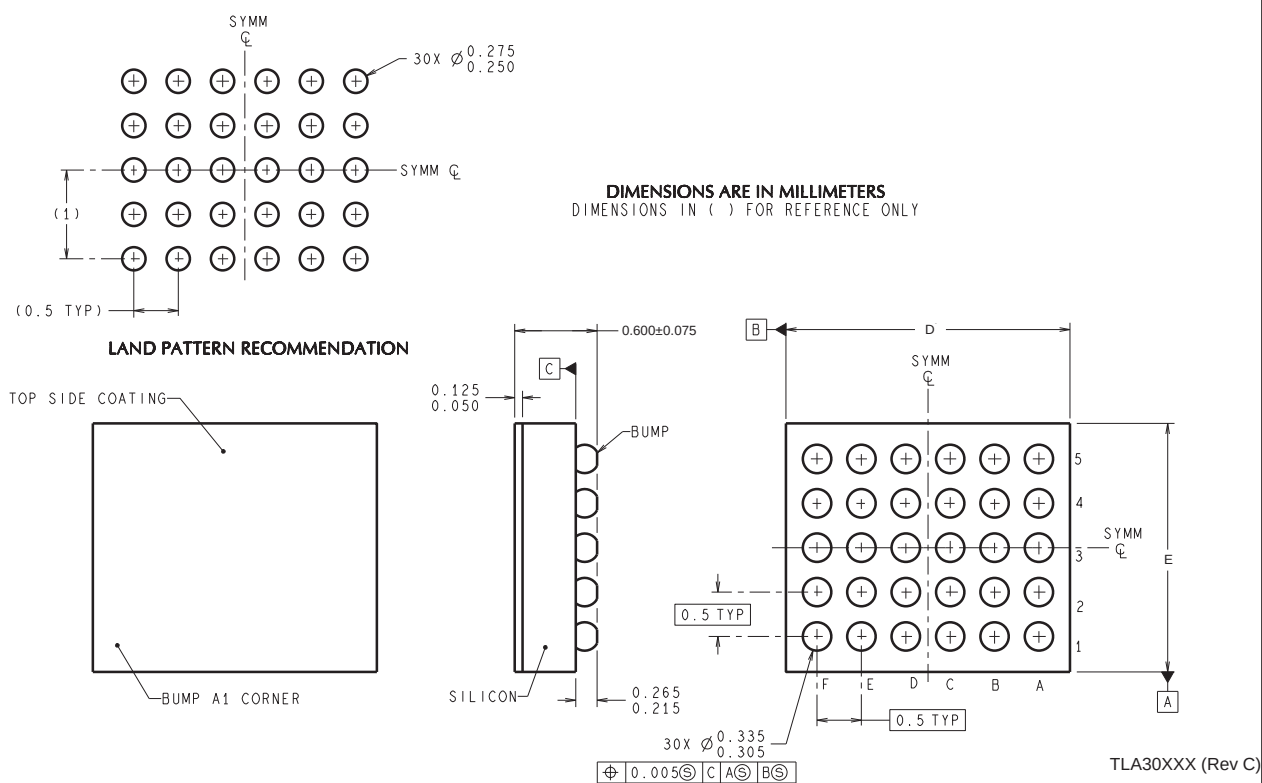
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LP8725TLE-A/NOPB | DSBGA        | YZR             | 30   | 250  | 210.0       | 185.0      | 35.0        |
| LP8725TLE-B/NOPB | DSBGA        | YZR             | 30   | 250  | 210.0       | 185.0      | 35.0        |
| LP8725TLE-C/NOPB | DSBGA        | YZR             | 30   | 250  | 210.0       | 185.0      | 35.0        |
| LP8725TLE-D/NOPB | DSBGA        | YZR             | 30   | 250  | 210.0       | 185.0      | 35.0        |
| LP8725TLE/NOPB   | DSBGA        | YZR             | 30   | 250  | 210.0       | 185.0      | 35.0        |
| LP8725TLX-A/NOPB | DSBGA        | YZR             | 30   | 3000 | 210.0       | 185.0      | 35.0        |
| LP8725TLX-B/NOPB | DSBGA        | YZR             | 30   | 3000 | 210.0       | 185.0      | 35.0        |
| LP8725TLX-C/NOPB | DSBGA        | YZR             | 30   | 3000 | 210.0       | 185.0      | 35.0        |
| LP8725TLX-D/NOPB | DSBGA        | YZR             | 30   | 3000 | 210.0       | 185.0      | 35.0        |
| LP8725TLX/NOPB   | DSBGA        | YZR             | 30   | 3000 | 210.0       | 185.0      | 35.0        |

YZR0030



D: Max = 2.99 mm, Min = 2.93 mm

E: Max = 2.59 mm, Min = 2.53 mm

4215057/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  
B. This drawing is subject to change without notice.

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View LP8725TLE-B/NOPB on WIN SOURCE](#)

 [Texas Instruments](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management