THE DATASHEET OF

LT1010CN8

Fast ±150mA Power Buffer

FTEATURES

- 20MHz Bandwidth
- 75V/µs Slew Rate
- Drives ±10V Into 75Ω
- 5mA Quiescent Current
- Drives Capacitive Loads > 1µF
- Current and Thermal Limit
- Operates from Single Supply ≥ 4.5V
- Very Low Distortion Operation
- Available in 8-Pin miniDIP, Plastic TO-220 and Tiny 3mm × 3mm × 0.75mm 8-Pin DFN Packages

APPLICATIONS

- Boost Op Amp Output
- Isolate Capacitive Loads
- Drive Long Cables
- Audio Amplifiers
- Video Amplifiers
- Power Small Motors
- Operational Power Supply
- FET Driver

DESCRIPTION

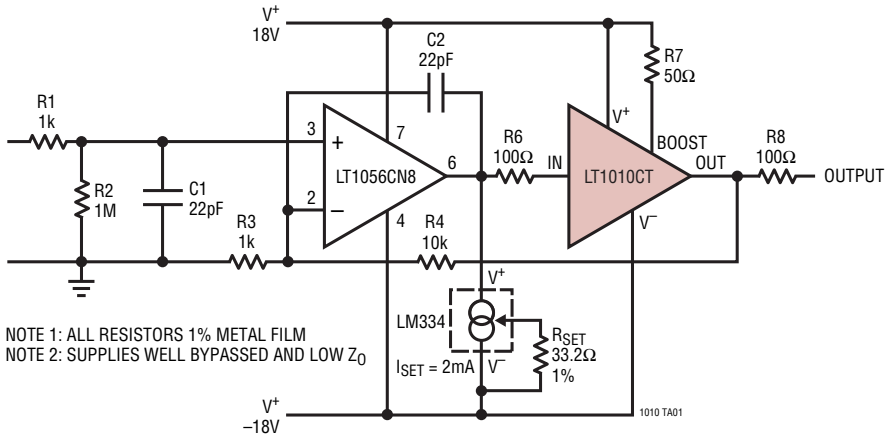
The LT®1010 is a fast, unity-gain buffer that can increase the output capability of existing IC op amps by more than an order of magnitude. This easy-to-use part makes fast amplifiers less sensitive to capacitive loading and reduces thermal feedback in precision DC amplifiers.

Designed to be incorporated within the feedback loop, the buffer can isolate almost any reactive load. Speed can be improved with a single external resistor. Internal operating currents are essentially unaffected by the supply voltage range. Single supply operation is also practical.

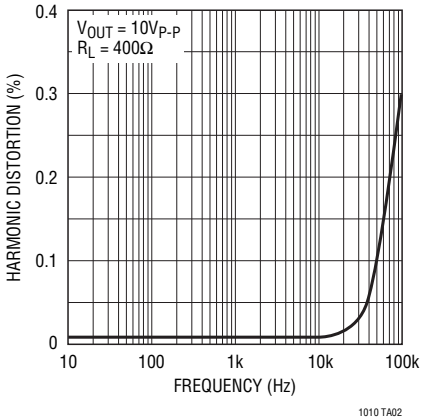
This monolithic IC is supplied in 8-pin miniDIP, plastic TO-220 and 8-pin DFN packages. The low thermal resistance power package is an aid in reducing operating junction temperatures.

TYPICAL APPLICATION

Very Low Distortion Buffered Preamplifier



NOTE 1: ALL RESISTORS 1% METAL FILM
NOTE 2: SUPPLIES WELL BYPASSED AND LOW Z_O



ABSOLUTE MAXIMUM RATINGS

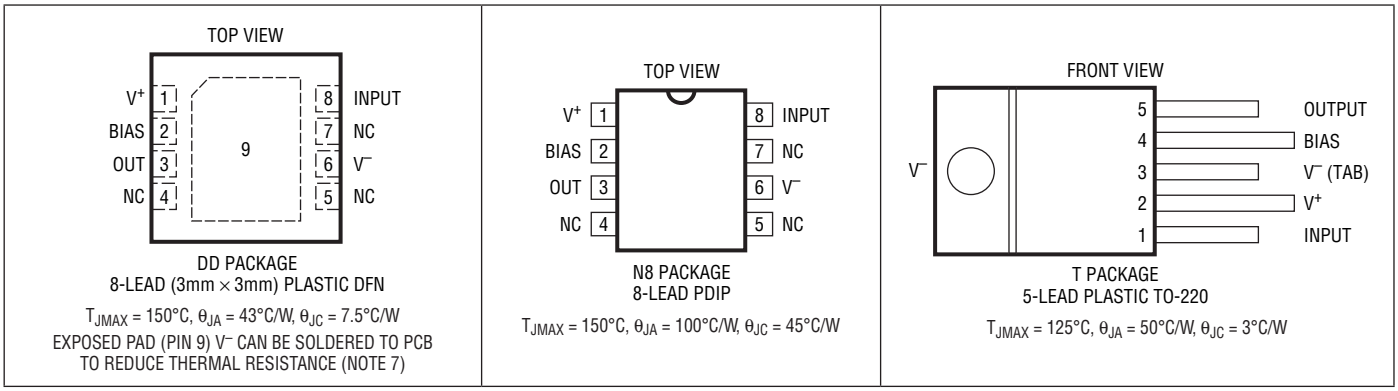
(Note 1)

Total Supply Voltage .....±22V
Continuous Output Current (Note 2) ..... ±150mA
Input Current (Note 3)..... ±40mA
Junction Temperature Range
LT1010C..... 0°C to 125°C
Storage Temperature Range.....–65°C to 150°C
Lead Temperature (Soldering, 10 sec) .....300°C

PRECONDITIONING

100% Thermal Limit Burn In–LT1010CT

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT1010CDD#PBF	LT1010CDD#TRPBF	LBWZ	8-Lead (3mm × 3mm) Plastic DFN	0°C to 100°C
LT1010CN8#PBF	LT1010CN8#TRPBF	LTC1010CN8	8-Lead PDIP	0°C to 100°C
LT1010CT#PBF	LT1010CT#TRPBF	LTC1010CT	5-Lead Plastic TO-220	0°C to 100°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING**	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LT1010CDD	LT1010CDD#TR	LBWZ	8-Lead (3mm × 3mm) Plastic DFN	0°C to 100°C
LT1010CN8	LT1010CN8#TR	LTC1010CN8	8-Lead PDIP	0°C to 100°C
LT1010CT	LT1010CT#TR	LTC1010CT	5-Lead Plastic TO-220	0°C to 100°C
OBSOLETE PACKAGE				

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (See Note 4. Typical values in curves.)

SYMBOL	PARAMETER	CONDITIONS (Note 4)		MIN	TYP	MAX	UNITS
V_{OS}	Output Offset Voltage	(Note 4)		0		150	mV
			●	–20		220	mV
		V_S = ±15V, V_{IN} = 0V		20		100	mV
I_B	Input Bias Current	I_{OUT} = 0mA		0		250	µA
		I_{OUT} ≤ 150mA		0		500	µA
			●	0		800	µA
A_V	Large-Signal Voltage Gain		●	0.995		1.00	V/V
R_{OUT}	Output Resistance	I_{OUT} = ±1mA		5		10	Ω
		I_{OUT} = ±150mA		5		10	Ω
			●			12	Ω
	Slew Rate	V_S = ±15V, V_{IN} = ±10V, V_{OUT} = ±8V, R_L = 100Ω		75			V/µs
V_{SOS}^+	Positive Saturation Offset	I_{OUT} = 0 (Note 5)				1.0	V
			●			1.1	V
V_{SOS}^-	Negative Saturation Offset	I_{OUT} = 0 (Note 5)				0.2	V
			●			0.3	V
R_{SAT}	Saturation Resistance	I_{OUT} = ±150mA (Note 5)				22	Ω
			●			28	Ω
V_{BIAS}	Bias Terminal Voltage	R_{BIAS} = 20Ω (Note 6)		700		840	mV
			●	560		880	mV
I_S	Supply Current	I_{OUT} = 0, I_{BIAS} = 0				9	mA
			●			10	mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Dissipation must be based on a thermal resistance. See Application Information for power dissipation.

Note 3: In current limit or thermal limit, input current increases sharply with input-output differentials greater than 8V; so input current must be limited. Input current also rises rapidly for input voltages 8V above V^+ or 0.5V below V^-.

Note 4: Specifications apply for 4.5V ≤ V_S ≤ 40V, V^- + 0.5V ≤ V_{IN} ≤ V^+ – 1.5V and I_{OUT} = 0, unless otherwise stated. Temperature range is 0°C ≤ T_C ≤ 100°C.

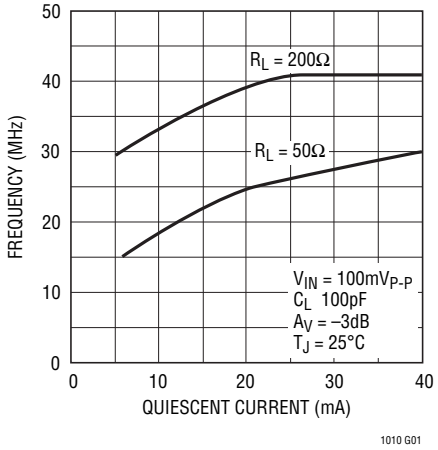
Note 5: The output saturation characteristics are measured with 100mV output clipping. See Applications Information for determining available output swing and input drive requirements for a given load.

Note 6: The output stage quiescent current can be increased by connecting a resistor between the BIAS pin and V^+. The increase is equal to the bias terminal voltage divided by this resistance.

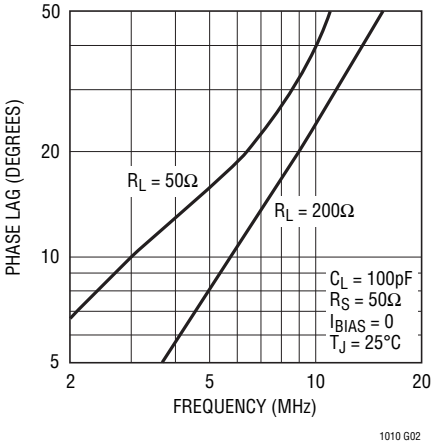
Note 7: Thermal resistance varies depending upon the amount of PC board metal attached to the pin (Pin 9) of the device. θ_{JA} is specified for a certain amount of 1oz copper metal trace connecting to Pin 9 as described in the thermal resistance tables in the Applications Information section.

TYPICAL PERFORMANCE CHARACTERISTICS

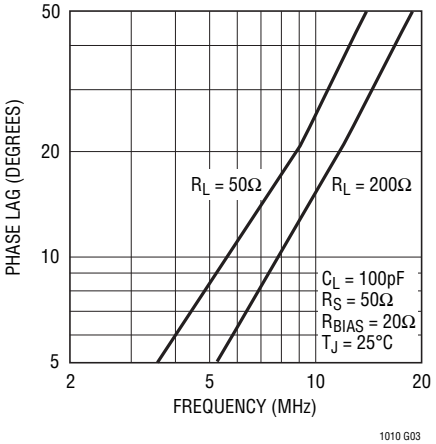
Bandwidth



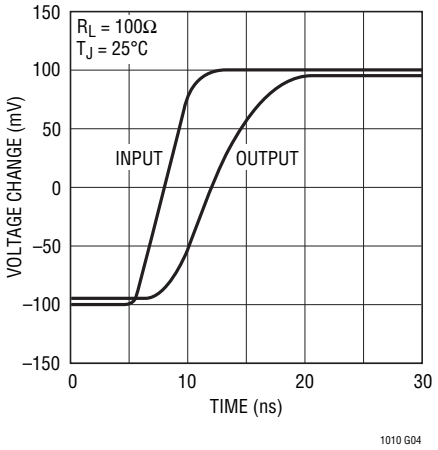
Phase Lag



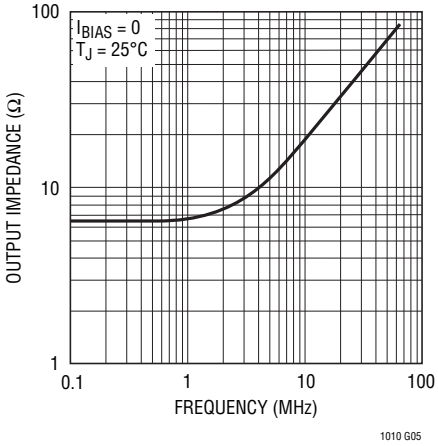
Phase Lag



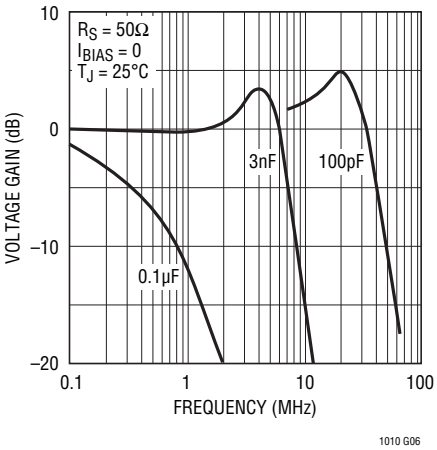
Small-Step Response



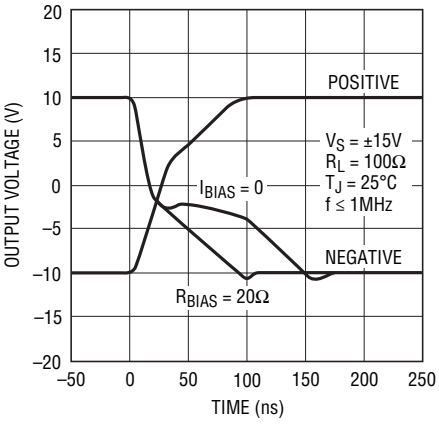
Output Impedance



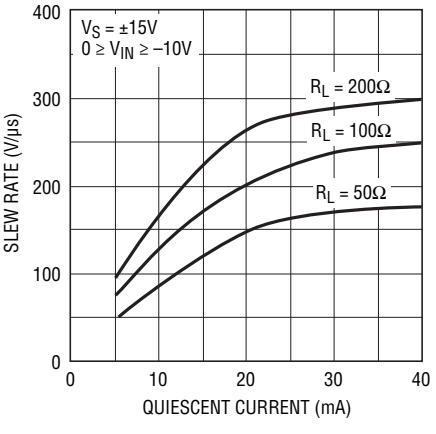
Capacitive Loading



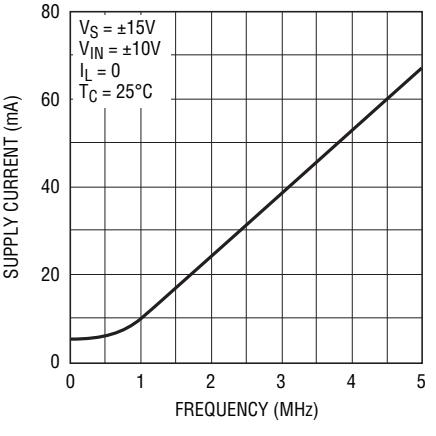
Slew Response



Negative Slew Rate

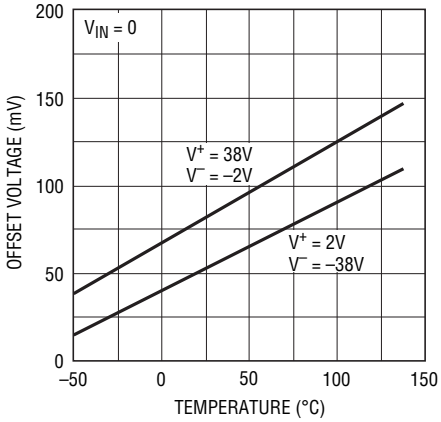


Supply Current



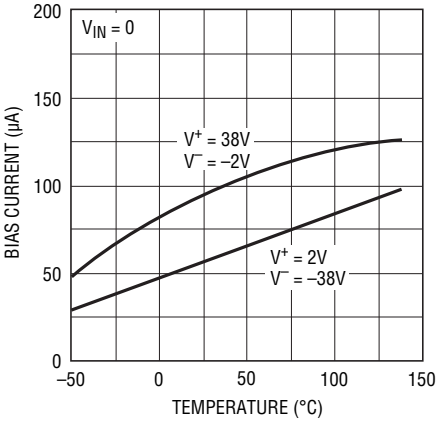
TYPICAL PERFORMANCE CHARACTERISTICS

Output Offset Voltage



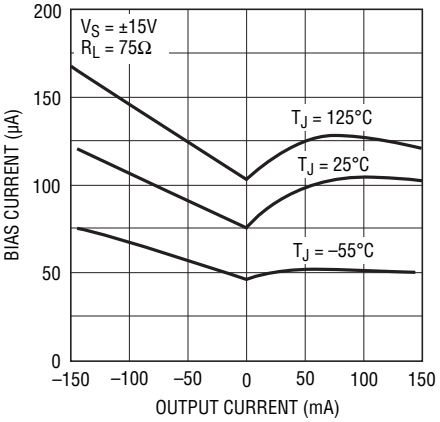
1010 G10

Input Bias Current



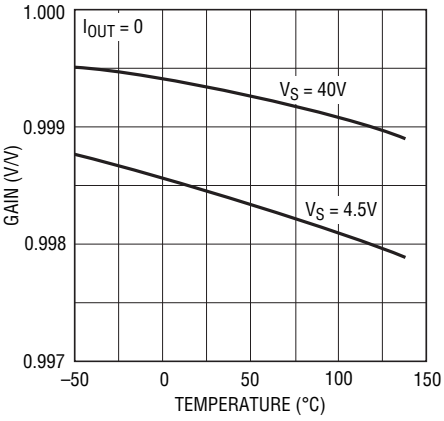
1010 G11

Input Bias Current



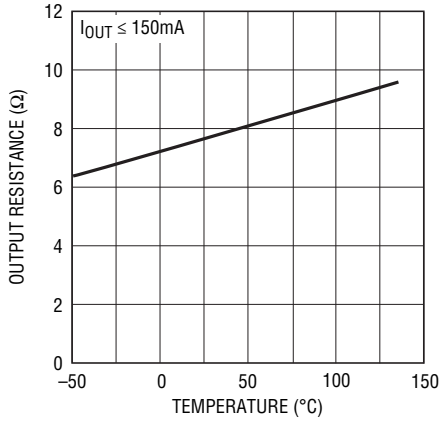
1010 G12

Voltage Gain



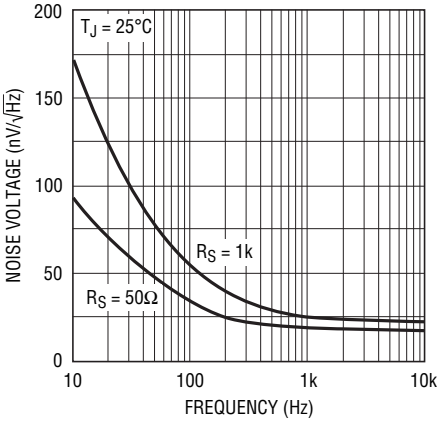
1010 G13

Output Resistance



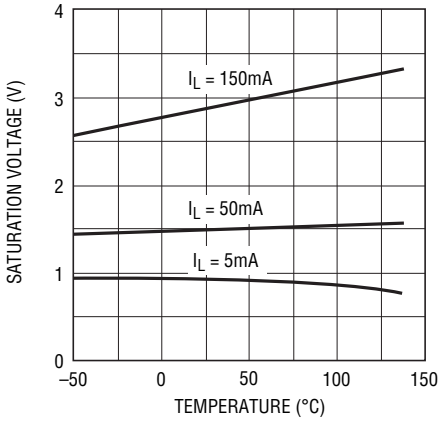
1010 G14

Output Noise Voltage



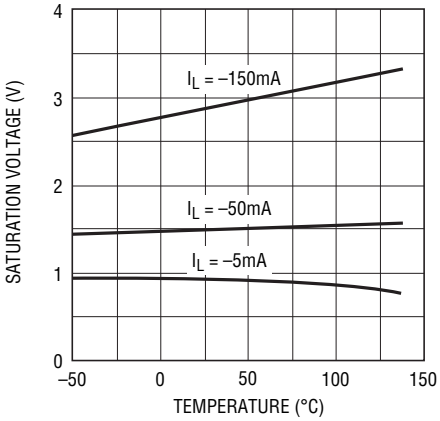
1010 G15

Positive Saturation Voltage



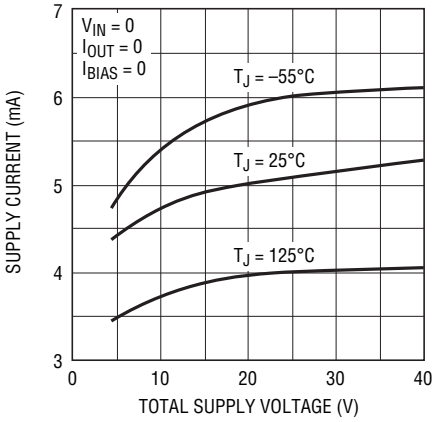
1010 G16

Negative Saturation Voltage



1010 G17

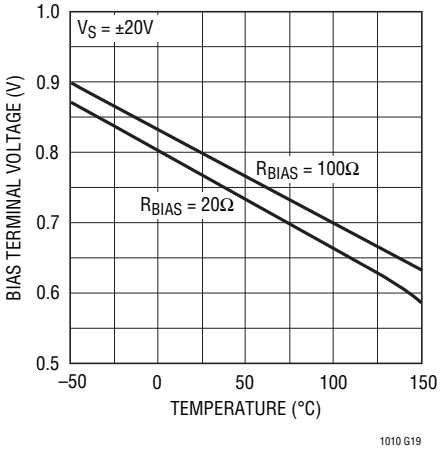
Supply Current



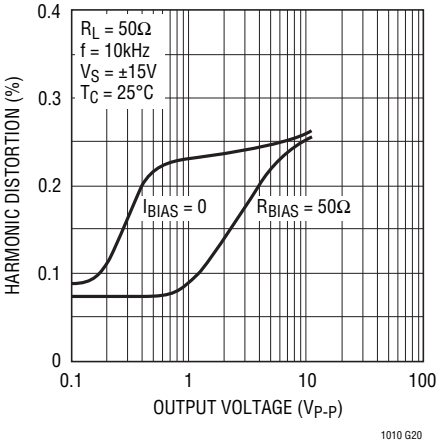
1010 G18

TYPICAL PERFORMANCE CHARACTERISTICS

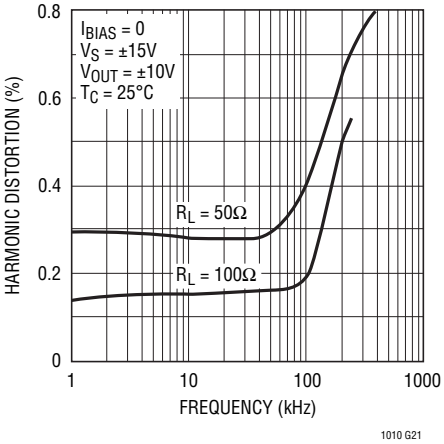
Bias Terminal Voltage



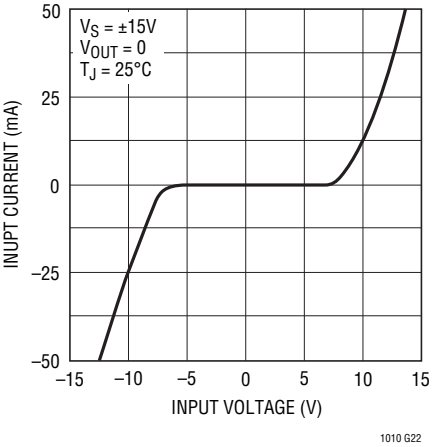
Total Harmonic Distortion



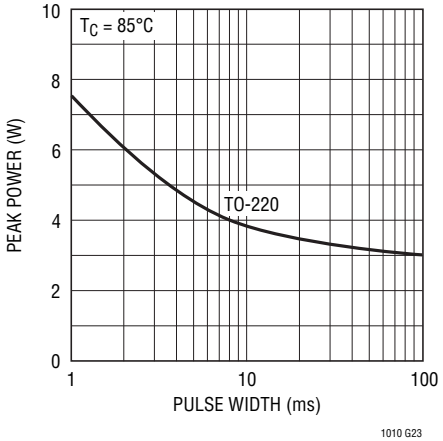
Total Harmonic Distortion



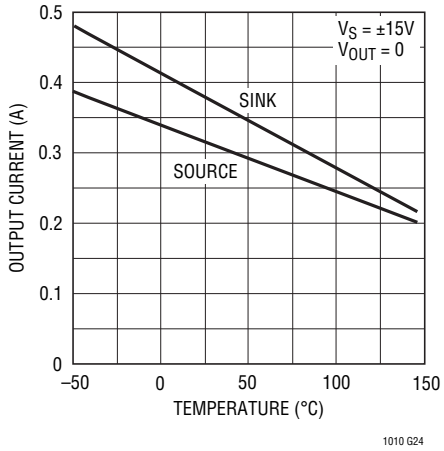
Shorted Input Characteristics



Peak Power Capability



Peak Output Current



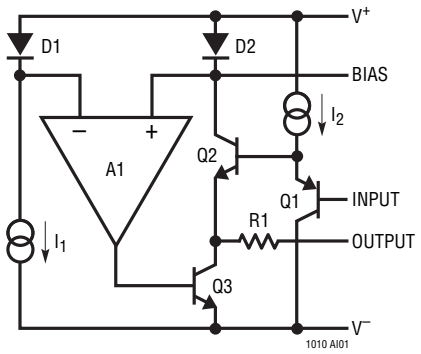
APPLICATIONS INFORMATION

General

These notes briefly describe the LT1010 and how it is used; a detailed explanation is given elsewhere.[1] Emphasis here will be on practical suggestions that have resulted from working extensively with the part over a wide range of conditions. A number of applications are also outlined that demonstrate the usefulness of the buffer beyond that of driving a heavy load.

Design Concept

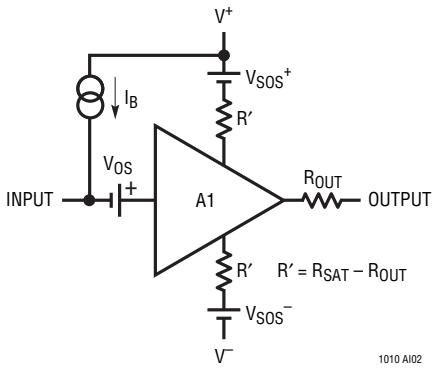
The schematic below describes the basic elements of the buffer design. The op amp drives the output sink transistor, Q3, such that the collector current of the output follower, Q2, never drops below the quiescent value (determined by I_1 and the area ratio of D1 and D2). As a result, the high frequency response is essentially that of a simple follower even when Q3 is supplying the load current. The internal feedback loop is isolated from the effects of capacitive loading by a small resistor in the output lead.



The scheme is not perfect in that the rate of rise of sink current is noticeably less than for source current. This can be mitigated by connecting a resistor between the bias terminal and V+, raising quiescent current. A feature of the final design is that the output resistance is largely independent of the follower quiescent current or the output load current. The output will also swing to the negative rail, which is particularly useful with single supply operation.

Equivalent Circuit

Below 1MHz, the LT1010 is quite accurately represented by the equivalent circuit shown here for both small- and large-signal operation. The internal element, A1, is an idealized buffer with the unloaded gain specified for the LT1010. Otherwise, it has zero offset voltage, bias current and output resistance. Its output also saturates to the internal supply terminals.[2]



Loaded voltage gain can be determined from the unloaded gain, A_V, the output resistance, R_{OUT}, and the load resistance, R_L, using:

$$A_{VL} = \frac{A_V R_L}{R_{OUT} + R_L}$$

Maximum positive output swing is given by:

$$V_{OUT}^{+} = \frac{(V^+ - V_{SOS^+})R_L}{R_{SAT} + R_L}$$

The input swing required for this output is:

$$V_{IN}^{+} = V_{OUT}^{+}\left(1 + \frac{R_{OUT}}{R_L}\right) - V_{OS} + \Delta V_{OS}$$

where ΔV_{OS} is the 100mV clipping specified for the saturation measurements. Negative output swing and input drive requirements are similarly determined.

Supply Bypass

The buffer is no more sensitive to supply bypassing than slower op amps as far as stability is concerned. The 0.1µF disc ceramic capacitors usually recommended for op amps are certainly adequate for low frequency work. As always, keeping the capacitor leads short and using

[1] R. J. Widlar, "Unique IC Buffer Enhances Op Amp Designs; Tames Fast Amplifiers," *Linear Technology Corp.* TP-1, April, 1984.
[2] See electrical characteristics section for guaranteed limits.

APPLICATIONS INFORMATION

a ground plane is prudent, especially when operating at high frequencies.

The buffer slew rate can be reduced by inadequate supply bypass. With output current changes much above 100mA/µs, using 10µF solid tantalum capacitors on both supplies is good practice, although bypassing from the positive to the negative supply may suffice.

When used in conjunction with an op amp and heavily loaded (resistive or capacitive), the buffer can couple into supply leads common to the op amp causing stability problems with the overall loop and extended settling time. Adequate bypassing can usually be provided by 10µF solid tantalum capacitors. Alternately, smaller capacitors could be used with decoupling resistors. Sometimes the op amp has much better high frequency rejection on one supply, so bypass requirements are less on this supply.

Power Dissipation

In many applications the LT1010 will require heat sinking. Thermal resistance, junction to still air is 50°C/W for the TO-220 package and 100°C/W for the miniDIP package. Circulating air, a heat sink or mounting the package to a printed circuit board will reduce thermal resistance.

In DC circuits, buffer dissipation is easily computed. In AC circuits, signal waveshape and the nature of the load determine dissipation. Peak dissipation can be several times average with reactive loads. It is particularly important to determine dissipation when driving large load capacitance.

With AC loading, power is divided between the two output transistors. This reduces the effective thermal resistance, junction to case is 3°C/W for the TO-220 package as long as the peak rating of neither output transistor is exceeded. The typical curves indicate the peak dissipation capabilities of one output transistor.

Overload Protection

The LT1010 has both instantaneous current limit and thermal overload protection. Foldback current limiting has not been used, enabling the buffer to drive complex loads without limiting. Because of this, it is capable of power dissipation in excess of its continuous ratings.

Normally, thermal overload protection will limit dissipation and prevent damage. However, with more than 30V across the conducting output transistor, thermal limiting is not quick enough to ensure protection in current limit. The thermal protection is effective with 40V across the conducting output transistor as long as the load current is otherwise limited to 150mA.

Drive Impedance

When driving capacitive loads, the LT1010 likes to be driven from a low source impedance at high frequencies. Certain low power op amps (e.g., the LM10) are marginal in this respect. Some care may be required to avoid oscillations, especially at low temperatures.

Bypassing the buffer input with more than 200pF will solve the problem. Raising the operating current also works.

Parallel Operation

Parallel operation provides reduced output impedance, more drive capability and increased frequency response under load. Any number of buffers can be directly paralleled as long as the increased dissipation in individual units caused by mismatches of output resistance and offset voltage is taken into account.

When the inputs and outputs of two buffers are connected together, a current, ΔI_{OUT}, flows between the outputs:

$$\Delta I_{OUT} = \frac{V_{OS1} - V_{OS2}}{R_{OUT1} + R_{OUT2}}$$

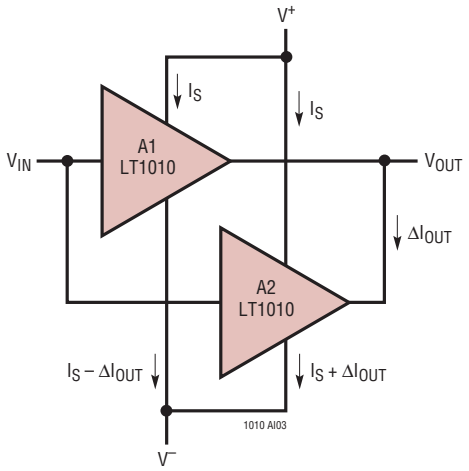
where V_{OS} and R_{OUT} are the offset voltage and output resistance of the respective buffers.

Normally, the negative supply current of one unit will increase and the other decrease, with the positive supply current staying the same. The worst-case ($V_{IN} \rightarrow V^+$) increase in standby dissipation can be assumed to be $\Delta I_{OUT} V_T$, where V_T is the total supply voltage.

Offset voltage is specified worst case over a range of supply voltages, input voltage and temperature. It would be unrealistic to use these worst-case numbers above because paralleled units are operating under identical conditions.

APPLICATIONS INFORMATION

The offset voltage specified for V_S = ±15V, V_{IN} = 0V and T_A = 25°C will suffice for a worst-case condition.



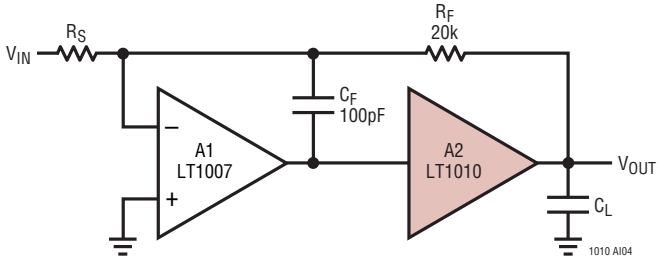
Output load current will be divided based on the output resistance of the individual buffers. Therefore, the available output current will not quite be doubled unless output resistances are matched. As for offset voltage, the 25°C limits should be used for worst-case calculations.

Parallel operation is not thermally unstable. Should one unit get hotter than its mates, its share of the output and its standby dissipation will decrease.

As a practical matter, parallel connection needs only some increased attention to heat sinking. In some applications, a few ohms equalization resistance in each output may be wise. Only the most demanding applications should require matching, and then just of output resistance at 25°C.

Isolating Capacitive Loads

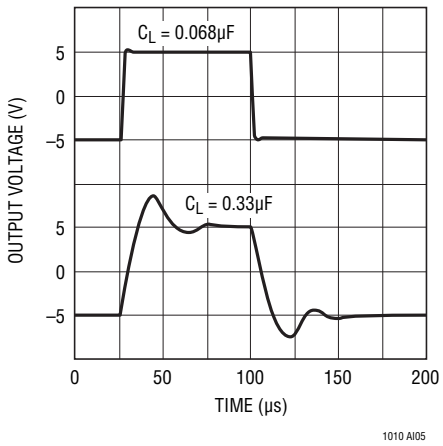
The inverting amplifier below shows the recommended method of isolating capacitive loads. Noninverting amplifiers are handled similarly.



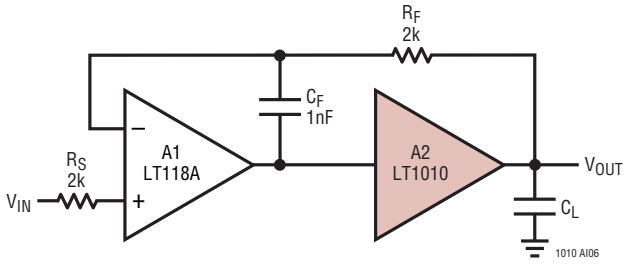
At lower frequencies, the buffer is within the feedback loop so that its offset voltage and gain errors are negligible. At higher frequencies, feedback is through C_F, so that phase shift from the load capacitance acting against the buffer output resistance does not cause loop instability.

Stability depends upon the R_FC_F time constant or the closed-loop bandwidth. With an 80kHz bandwidth, ringing is negligible for C_L = 0.068µF and damps rapidly for C_L = 0.33µF. The pulse response is shown in the graph.

Pulse Response



Small-signal bandwidth is reduced by C_F, but considerable isolation can be obtained without reducing it below the power bandwidth. Often, a bandwidth reduction is desirable to filter high frequency noise or unwanted signals.



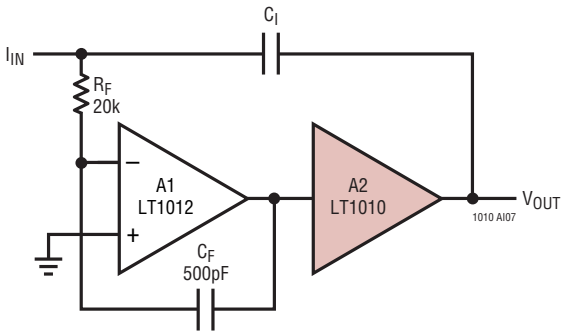
The follower configuration is unique in that capacitive load isolation is obtained without a reduction in small-signal bandwidth, although the output impedance of the buffer comes into play at high frequencies. The precision unity-gain buffer above has a 10MHz bandwidth without capacitive loading, yet it is stable for all load capacitance to over 0.3µF, again determined by R_FC_F.

APPLICATIONS INFORMATION

This is a good example of how fast op amps can be made quite easy to use by employing an output buffer.

Integrator

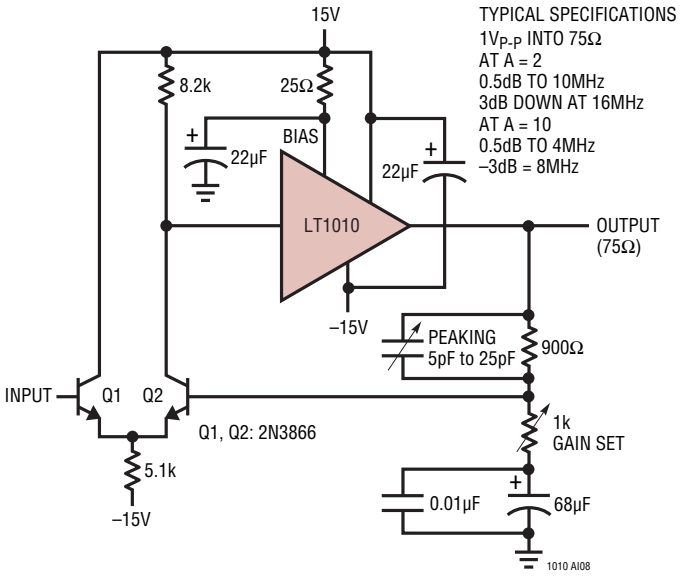
A lowpass amplifier can be formed just by using large C_F in the inverter described earlier, as long as the increasing closed-loop output impedance above the cutoff frequency is not a problem and the op amp is capable of supplying the required current at the summing junction.

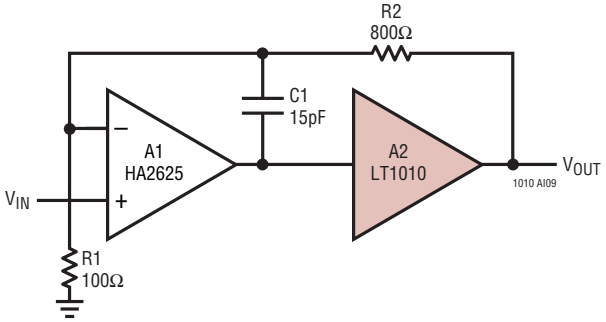


If the integrating capacitor must be driven from the buffer output, the circuit above can be used to provide capacitive load isolation. As before, the stability with large capacitive loads is determined by R_FC_F.

Wideband Amplifiers

This simple circuit provides an adjustable gain video amplifier that will drive $1V_{P-P}$ into 75Ω. The differential pair provides gain with the LT1010 serving as an output stage. Feedback is arranged in the conventional manner, although the 68µF-0.01µF combination limits DC gain to unity for all gain settings. For applications sensitive to NTSC requirements, dropping the 25Ω output stage bias value will aid performance.

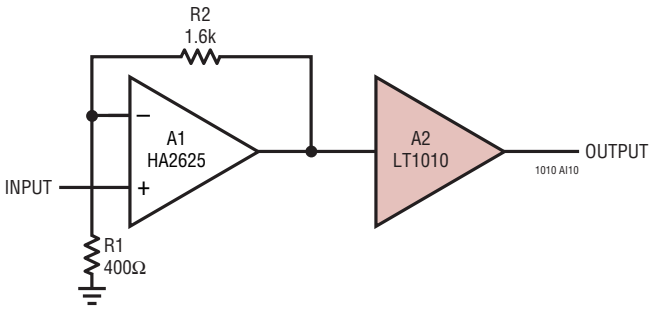




This shows the buffer being used with a wideband amplifier that is not unity-gain stable. In this case, C1 cannot be used to isolate large capacitive loads. Instead, it has an optimum value for a limited range of load capacitances.

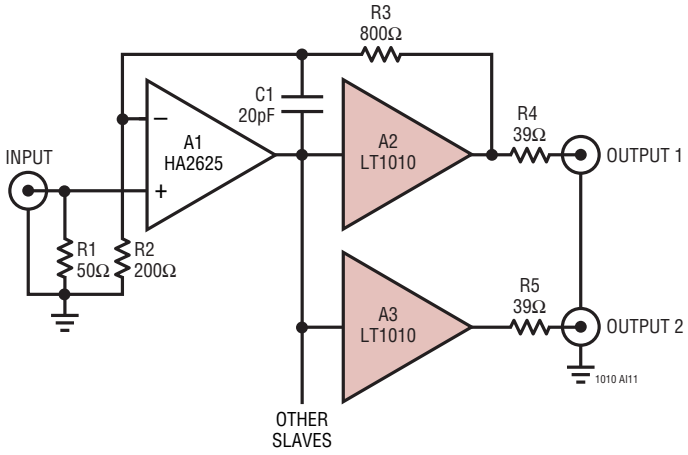
The buffer can cause stability problems in circuits like this. With the TO-220 packages, behavior can be improved by raising the quiescent current with a 20Ω resistor from the bias terminal to V^+. Alternately, devices in the miniDIP can be operated in parallel.

It is possible to improve capacitive load stability by operating the buffer class A at high frequencies. This is done by using quiescent current boost and bypassing the bias terminal to $V^–$ with more than 0.02µF.



Putting the buffer outside the feedback loop as shown here will give capacitive load isolation, with large output capacitors only reducing bandwidth. Buffer offset, referred to the op amp input, is divided by the gain. If the load resistance is known, gain error is determined by the output resistance tolerance. Distortion is low.

APPLICATIONS INFORMATION



The 50Ω video line splitter here puts feedback on one buffer with the others slaved. Offset and gain accuracy of slaves depend on their matching with master.

When driving long cables, including a resistor in series with the output should be considered. Although it reduces gain, it does isolate the feedback amplifier from the effects of unterminated lines which present a resonant load.

When working with wideband amplifiers, special attention should *always* be paid to supply bypassing, stray capacitance and keeping leads short. Direct grounding of test probes, rather than the usual ground lead, is absolutely necessary for reasonable results.

The LT1010 has slew limitations that are not obvious from standard specifications. Negative slew is subject to glitching, but this can be minimized with quiescent current boost. The appearance is always worse with fast rise signal generators than in practical applications.

Track and Hold

The 5MHz track and hold shown here has a 400kHz power bandwidth driving ±10V. A buffered input follower drives the hold capacitor, C4, through Q1, a low resistance FET switch. The positive hold command is supplied by TTL logic with Q3 level shifting to the switch driver, Q2. The output is buffered by A3.

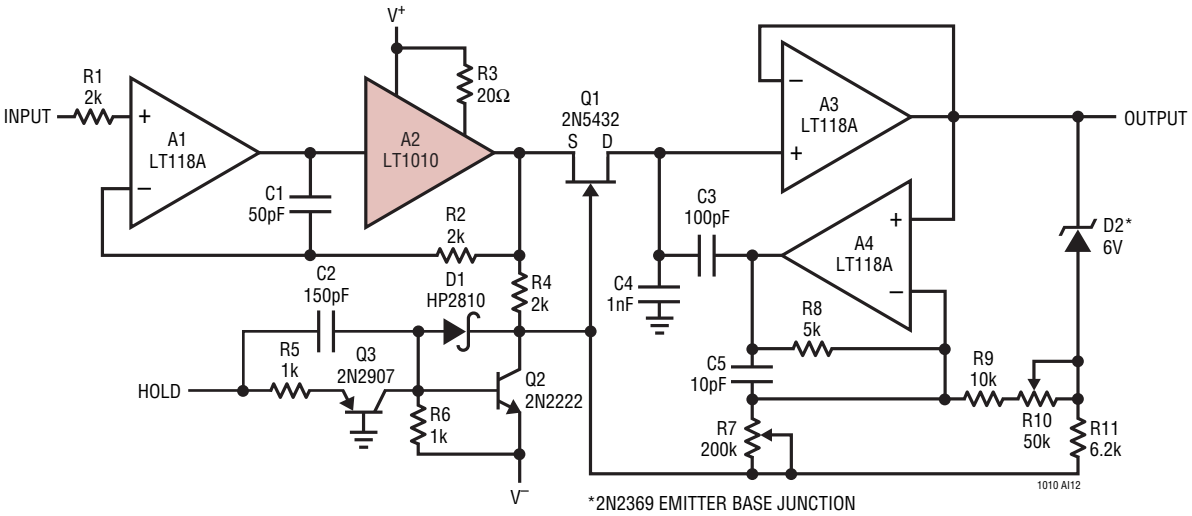
When the gate is driven to V^- for HOLD, it pulls charge out of the hold capacitor. A compensating charge is put into the hold capacitor through C3. The step into hold is made independent of the input level with R7 and adjusted to zero with R10.

Since internal dissipation can be quite high when driving fast signals into a capacitive load, using a buffer in a power package is recommended. Raising buffer quiescent current to 40mA with R3 improves frequency response.

This circuit is equally useful as a fast acquisition sample and hold. An LT1056 might be used for A3 to reduce drift in hold because its lower slew rate is not usually a problem in this application.

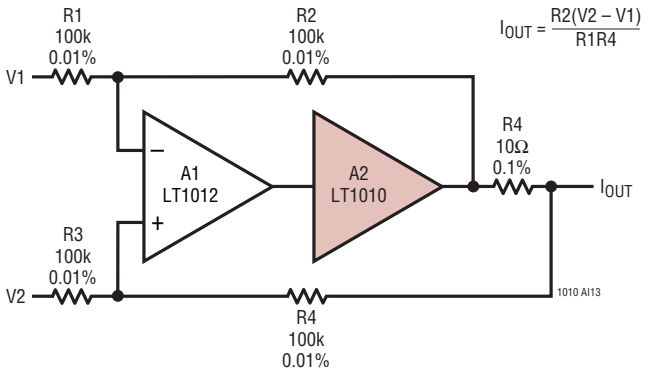
Current Sources

A standard op amp voltage to current converter with a buffer to increase output current is shown here. As usual,

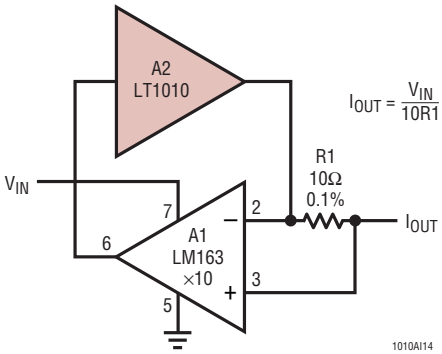


APPLICATIONS INFORMATION

excellent matching of the feedback resistors is required to get high output resistance. Output is bidirectional.



This circuit uses an instrumentation amplifier to eliminate the matched resistors. The input is not high impedance and must be driven from a low impedance source like an op amp. Reversal of output sense can be obtained by grounding Pin 7 of the LM163 and driving Pin 5.

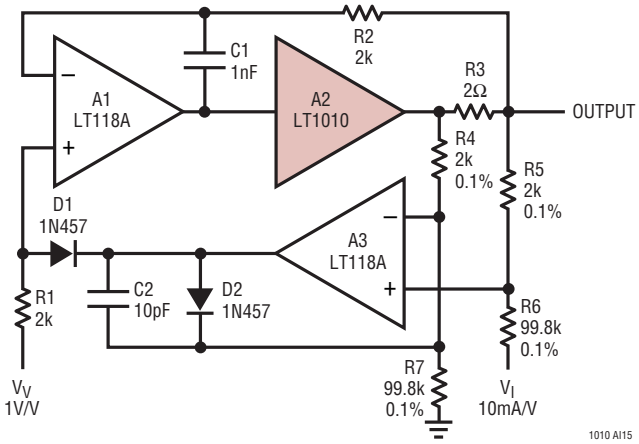


Output resistances of several megohms can be obtained with both circuits. This is impressive considering the ±150mA output capability. High frequency output characteristics will depend on the bandwidth and slew rate of the amplifiers. Both these circuits have an equivalent output capacitance of about 30nF.

Voltage/Current Regulator

This circuit regulates the output voltage at V_V until the load current reaches a value programmed by V_I. For heavier loads, it is a precision current regulator.

With output currents below the current limit, the current regulator is disconnected from the loop by D1 with D2 keeping its output out of saturation. This output clamp



enables the current regulator to get control of the output current from the buffer current limit within a microsecond for an instantaneous short.

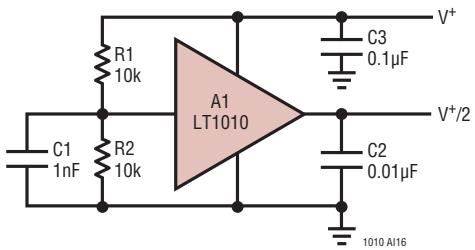
In the voltage regulation mode, A1 and A2 act as a fast voltage follower using the capacitive load isolation technique described earlier. Load transient recovery as well as capacitive load stability are determined by C1. Recovery from short circuit is clean.

Bidirectional current limit can be obtained by adding another op amp connected as a complement to A3.

Supply Splitter

Dual supply op amps and comparators can be operated from a single supply by creating an artificial ground at half the supply voltage. The supply splitter shown here can source or sink 150mA.

The output capacitor, C2, can be made as large as necessary to absorb current transients. An input capacitor is also used on the buffer to avoid high frequency instability that can be caused by high source impedance.

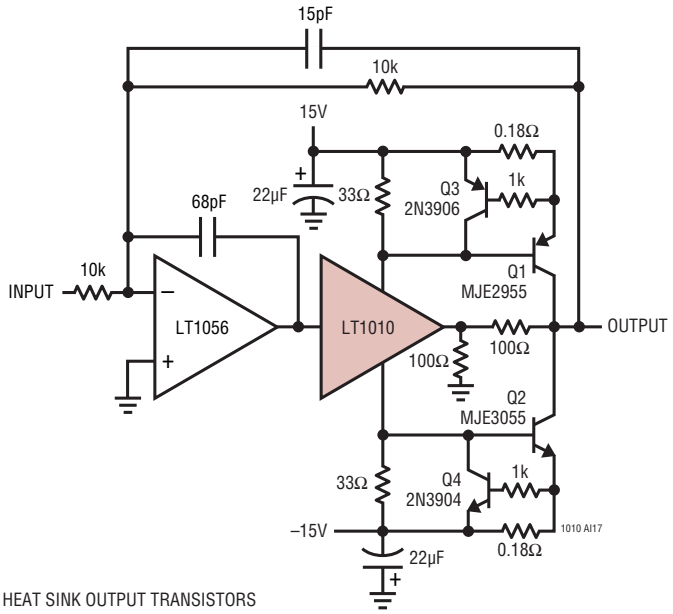


APPLICATIONS INFORMATION

High Current Booster

The circuit below uses a discrete stage to get 3A output capacity. The configuration shown provides a clean, quick way to increase LT1010 output power. It is useful for high current loads such as linear actuator coils in disk drives.

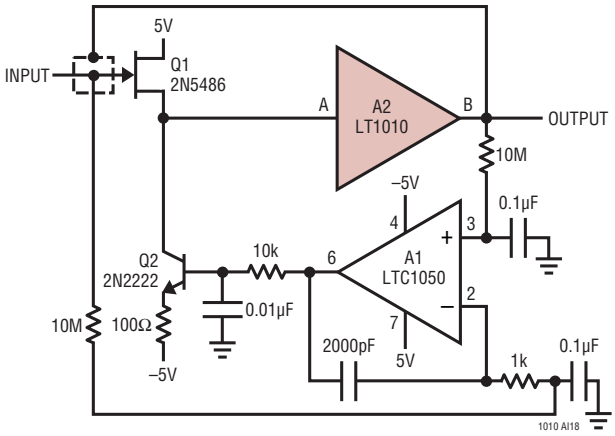
The 33Ω resistors sense the LT1010's supply current with the grounded 100Ω resistor supplying a load for the LT1010. The voltage drop across the 33Ω resistors biases Q1 and Q2. Another 100Ω value closes a local feedback loop, stabilizing the output stage. Feedback to the LT1056 control amplifier is via the 10k value. Q3 and Q4, sensing across the 0.18Ω units, furnish current limiting at about 3.3A.



HEAT SINK OUTPUT TRANSISTORS

Wideband FET Input Stabilized Buffer

The figure below shows a highly stable unity-gain buffer with good speed and high input impedance. Q1 and Q2 constitute a simple, high speed FET input buffer. Q1 functions as a source follower with the Q2 current source load setting the drain-source channel current. The LT1010 buffer provides output drive capability for cables or whatever load is required. Normally, this open-loop configuration would be quite drifty because there is no DC feedback. The LTC®1050 contributes this function to stabilize the circuit. It does this by comparing the filtered circuit output to a



similarly filtered version of the input signal. The amplified difference between these signals is used to set Q2's bias, and hence, Q1's channel current. This forces Q1's V_{GS} to whatever voltage is required to match the circuit's input and output potentials. The 2000pF capacitor at A1 provides stable loop compensation. The RC network in A1's output prevents it from seeing high speed edges coupled through Q2's collector-base junction. A2's output is also fed back to the shield around Q1's gate lead, bootstrapping the circuit's effective input capacitance down to less than 1pF.

Gain-Trimmable Wideband FET Amplifier

A potential difficulty with the previous circuit is that the gain is not quite unity. The figure labeled A on the next page maintains high speed and low bias while achieving a true unity-gain transfer function.

This circuit is somewhat similar except that the Q2-Q3 stage takes gain. A2 DC stabilizes the input-output path and A1 provides drive capability. Feedback is to Q2's emitter from A1's output. The 1k adjustment allows the gain to be precisely set to unity. With the LT1010, output stage slew and full power bandwidth ($1V_{P-P}$) are 100V/µs and 10MHz respectively. –3dB bandwidth exceeds 35MHz. At A = 10 (e.g., 1k adjustment set at 50Ω), full power bandwidth stays at 10MHz while the –3dB point falls to 22MHz.

With the optional discrete stage, slew exceeds 1000V/µs and full power bandwidth ($1V_{P-P}$) is 18MHz. –3dB bandwidth is 58MHz. At A = 10, full power is available to 10MHz, with the –3dB point at 36MHz.

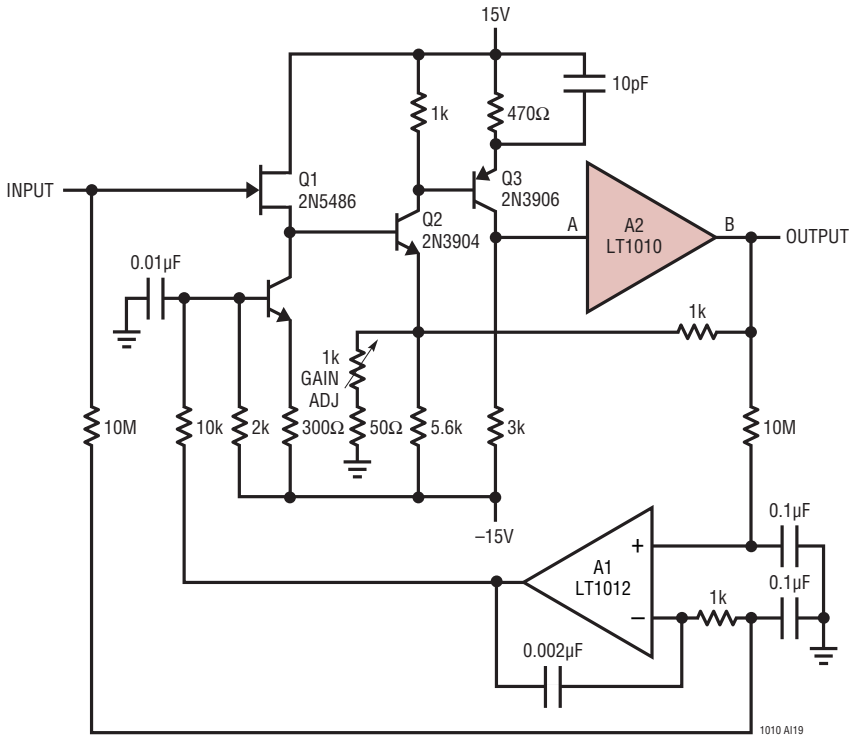
APPLICATIONS INFORMATION

Figures A and B show response with both output stages. The LT1010 is used in Figure A (Trace A = input, Trace B = output). Figure B uses the discrete stage and is slightly faster. Either stage provides more than adequate performance for driving video cable or data converters and the LT1012 maintains DC stability under all conditions.

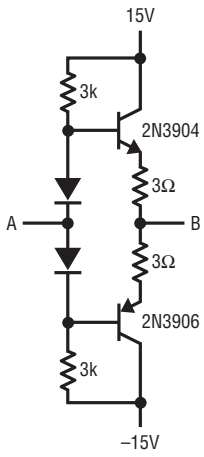
Thermal Considerations for the MiniDIP Package

The miniDIP package requires special thermal considerations since it is not designed to dissipate much power. Be aware that for applications requiring large output currents, another package should be used.

Gain-Trimmable Wideband FET Amplifier



(A)



(B)

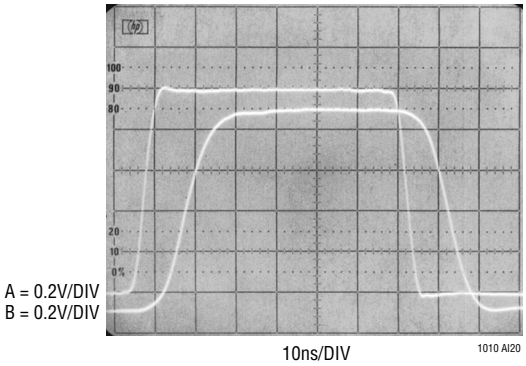


Figure A. Waveforms Using LT1010

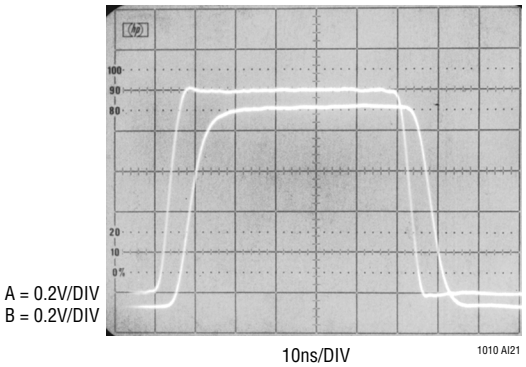


Figure B. Waveforms Using Discrete Stage

APPLICATIONS INFORMATION

Typical thermal calculations for the miniDIP package are detailed in the following paragraphs.

For 4.8mA supply current (typical at 50°C, 30V supply voltage—see supply current graphs) to the LT1010 at ±15V, P_D = power dissipated in the part is equal to:

(30V)(0.0048A) = 0.144W

The rise in junction is then:

(0.144W)(100°C/W—This is θ_{JA} for the N package)

= 14.4°C.

This means that the junction temperature in 50°C ambient air without driving any current into a load is:

14.4°C + 50°C = 64.4°C

Using the LT1010 to drive 8V DC into a 200Ω load using ±15V power supplies dissipates P_D in the LT1010 where:

$$P_D = \frac{\left(V^+ - V_{OUT}\right)\left(V_{OUT}\right)}{R_L}$$

$$= \frac{(15V - 8V)(8V)}{200\Omega} = 0.280W$$

This causes the LT1010 junction temperature to rise another (0.280W)(100°C/W) = 28°C.

This heats the junction to 64.4°C + 28°C = 92.4°C.

An example of 1MHz operation further shows the limitations of the N (or miniDIP) package. For ±15V operation:

PD at I_L = 0 at 1MHz* = (10mA)(30V) = 0.30W

This power dissipation causes the junction to heat from 50°C (ambient in this example) to 50°C + (0.3W)(100°C/W) = 80°C. Driving $2V_{RMS}$ of 1MHz signal into a 200Ω load causes an additional

$$P_D = \left(\frac{2V}{200\Omega}\right) \bullet (15 - 2) = 0.130W$$

to be dissipated, resulting in another (0.130W)(100°C/W) = 13°C rise in junction temperature to 80°C + 13°C = 93°C.

Thermal Resistance of DFN Package

For surface mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by power devices.

The following table lists thermal resistance for several different board sizes and copper areas. All measurements were taken in still air on 3/32" FR-4 board with one ounce copper.

Table 1. DFN Measured Thermal Resistance

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE	BACKSIDE		
2500 sq mm	2500 sq mm	2500 sq mm	40°C/W
1000 sq mm	2500 sq mm	2500 sq mm	45°C/W
225 sq mm	2500 sq mm	2500 sq mm	50°C/W
100 sq mm	2500 sq mm	2500 sq mm	62°C/W

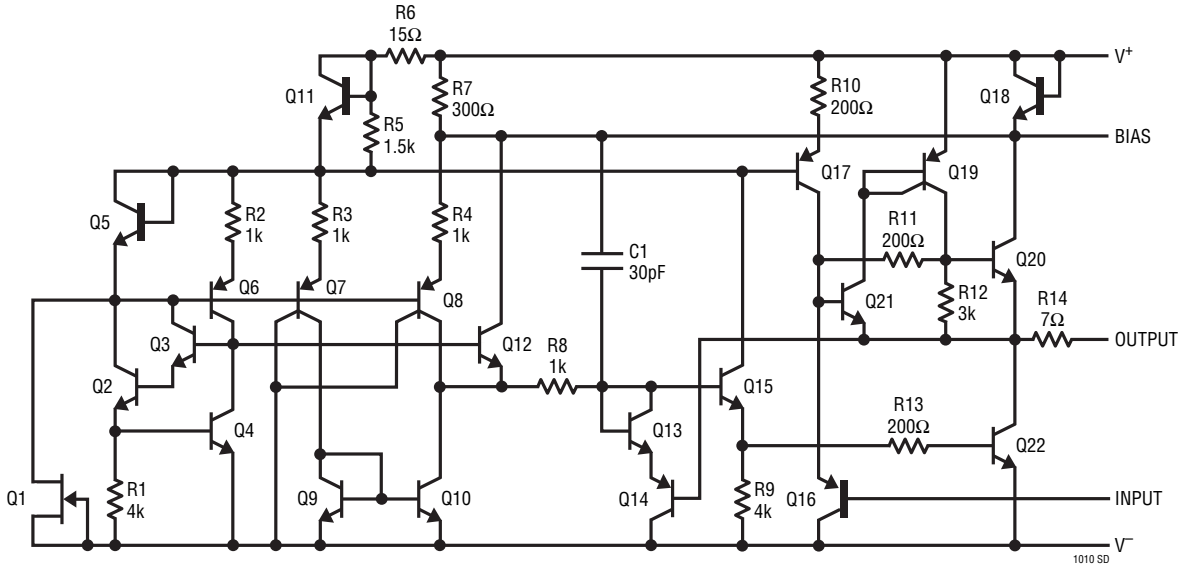
For the DFN package, the thermal resistance junction-to-case (θ_{JC}), measured at the Exposed Pad on the back of the die, is 7.5°C/W.

Continuous operation at the maximum supply voltage and maximum load current is not practical due to thermal limitations. Transient operation at the maximum supply is possible. The approximate thermal time constant for a 2500sq mm 3/32" FR-4 board with maximum topside and backside area for one ounce copper is 3 seconds. This time constant will increase as more thermal mass is added (i.e., vias, larger board and other components).

For an application with transient high power peaks, average power dissipation can be used for junction temperature calculations as long as the pulse period is significantly less than the thermal time constant of the device and board.

*See Supply Current vs Frequency graph.

SCHEMATIC DIAGRAM (Excluding protection circuits)



DEFINITION OF TERMS

Output Offset Voltage: The output voltage measured with the input grounded (split supply operation).

Input Bias Current: The current out of the input terminal.

Large-Signal Voltage Gain: The ratio of the output voltage change to the input voltage change over the specified input voltage range.*

Output Resistance: The ratio of the change in output voltage to the change in load current producing it.*

Output Saturation Voltage: The voltage between the output and the supply rail at the limit of the output swing toward that rail.

Saturation Offset Voltage: The output saturation voltage with no load.

Saturation Resistance: The ratio of the change in output saturation voltage to the change in current producing it, going from no load to full load.*

Slew Rate: The average time rate of change of output voltage over the specified output range with an input step between the specified limits.

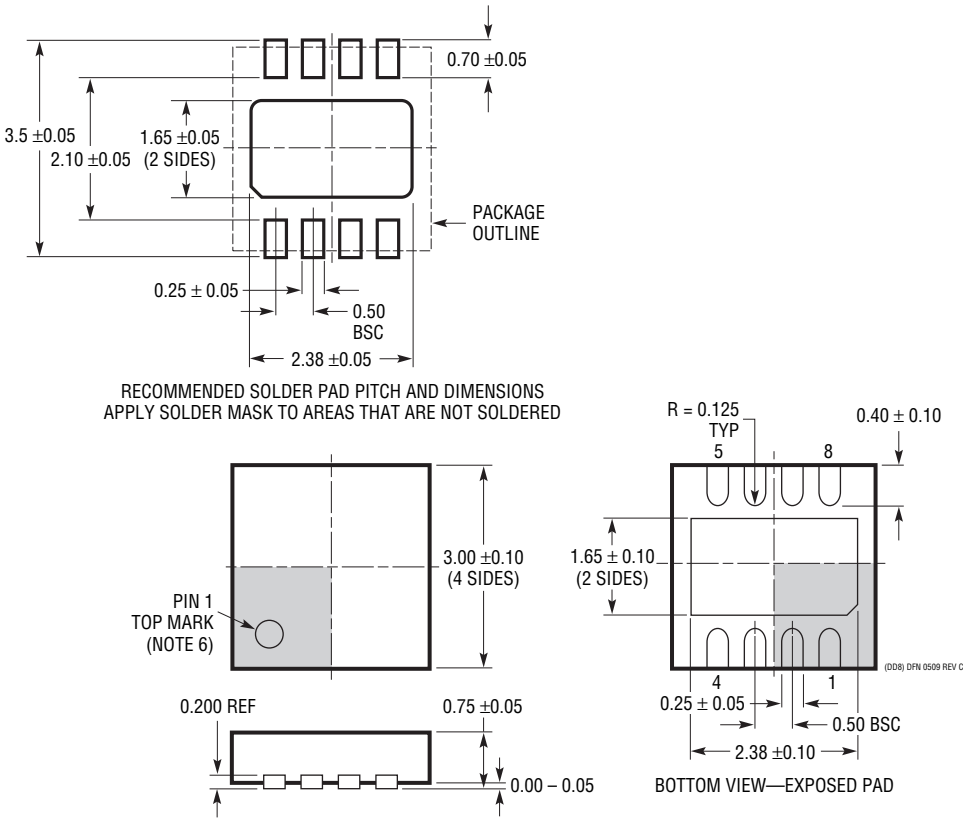
Bias Terminal Voltage: The voltage between the bias terminal and V^+.

Supply Current: The current at either supply terminal with no output loading.

*Pulse measurements (~1ms) as required to minimize thermal effects.

PACKAGE DESCRIPTION

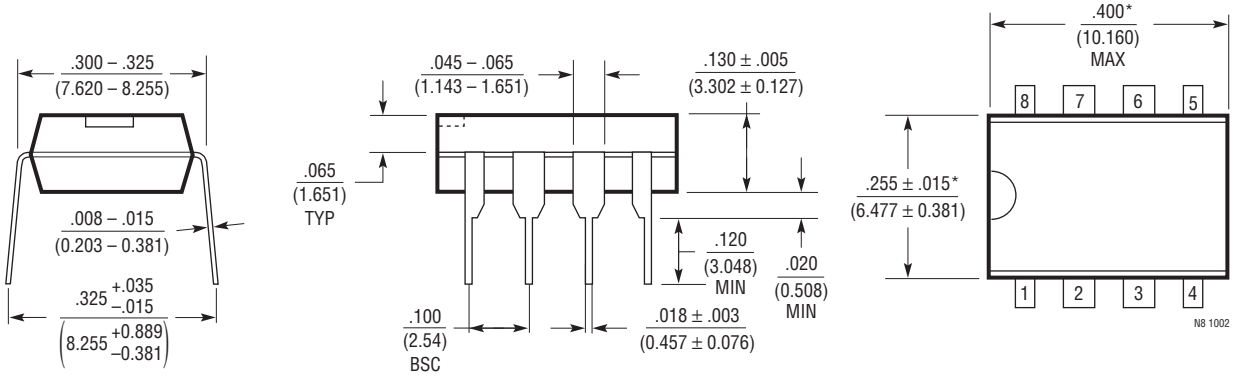
DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

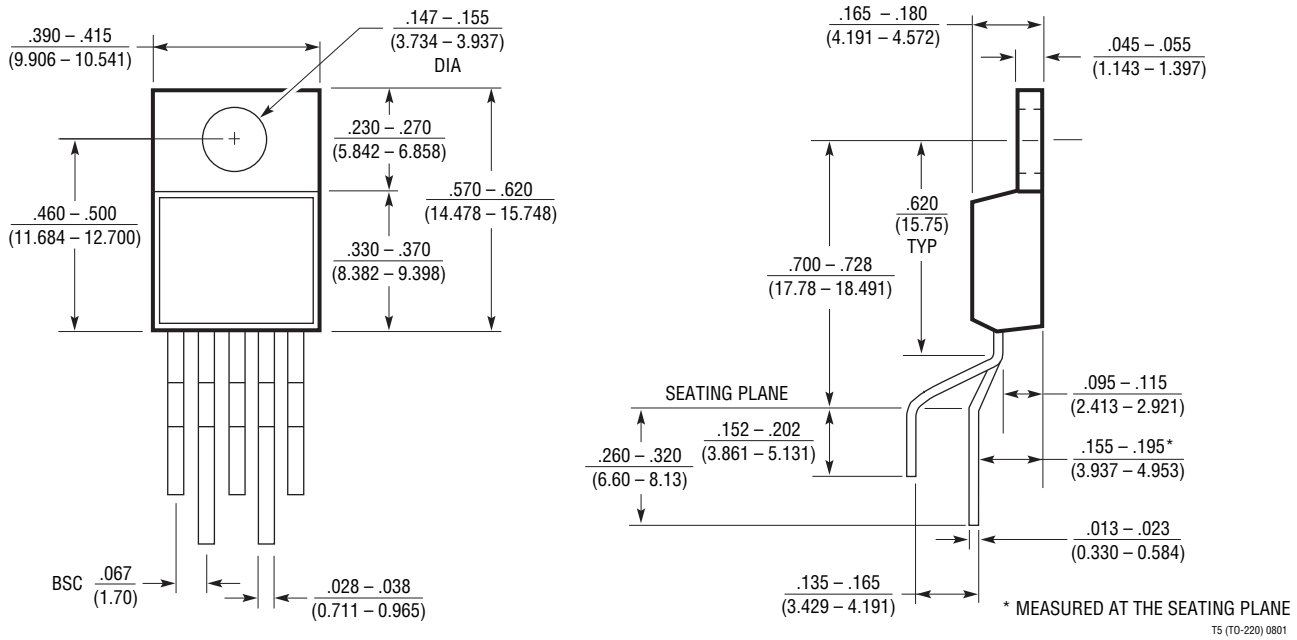
PACKAGE DESCRIPTION

N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

T Package
5-Lead Plastic TO-220 (Standard)
(Reference LTC DWG # 05-08-1421)



REVISION HISTORY (Revision history begins at Rev E)

REV	DATE	DESCRIPTION	PAGE NUMBER
E	5/11	Revised temperature ranges and values in Absolute Maximum Ratings and Pin Configuration sections	2
		Revised Notes 2 and 4 in Electrical Characteristics section	3
		Updated temperature values in Power Dissipation, Thermal Considerations for the MiniDIP Package, and Thermal Resistance of DFN Package sections of the Applications Information section	8, 15

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1206	250mA, 60MHz Current Feedback Amplifier	900V/µs, Excellent Video Characteristics
LT1210	1.1A, 35MHz Current Feedback Amplifier	900V/µs Slew Rate, Stable with Large Capacitive Loads
LT1795	Dual 500mA, 50MHz CFA	500mA I_{OUT} ADSL Driver
LT1886	Dual 700MHz, 200mA Op Amp	DSL Driver

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT 0511 REV E • PRINTED IN USA

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View LT1010CN8 on WIN SOURCE
- Linear Technology Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management