THE DATASHEET OF

LT1801IS8#PBF

www.win-source.net 0086-755-83957316

Dual/Quad 80MHz, 25V/µs Low Power Rail-to-Rail Input and Output Precision Op Amps

FEATURES

- **Gain Bandwidth Product: 80MHz**
- **Input Common Mode Range Includes Both Rails**
- **Output Swings Rail-to-Rail**
- **Low Voltage Operation: Single or Split Supplies 2.3V to 12.6V**
- **Low Quiescent Current: 2mA/Amplifier Max**
- **Input Offset Voltage: 350µV Max**
- **Input Bias Current: 250nA Max**
- 3mm × 3mm × 0.8mm DFN Package
- Large Output Current: 50mA Typ
- Low Voltage Noise: 8.5nV/√Hz Typ
- Slew Rate: 25V/µs Typ
- Common Mode Rejection: 105dB Typ
- Power Supply Rejection: 97dB Typ
- Open-Loop Gain: 85V/mV Typ
- Operating Temperature Range: –40°C to 85°C
- LT1801 is Available in 8-Lead SO, MS8 and DFN Packages
- LT1802 is Available in 14-Lead SO Package

APPLICATIONS

- Low Voltage, High Frequency Signal Processing
- Driving A/D Converters
- Rail-to-Rail Buffer Amplifiers
- Active Filters
- Video Line Driver

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DESCRIPTION

The LT®1801/LT1802 are dual/quad, low power, high speed rail-to-rail input and output operational amplifiers with excellent DC performance. The LT1801/LT1802 feature reduced supply current, lower input offset voltage, lower input bias current and higher DC gain than other devices with comparable bandwidth.

Typically, the LT1801/LT1802 have an input offset voltage of less than 100µV, an input bias current of less than 50nA and an open-loop gain of 85 thousand.

The LT1801/LT1802 have an input range that includes both supply rails and an output that swings within 20mV of either supply rail to maximize the signal dynamic range in low supply applications.

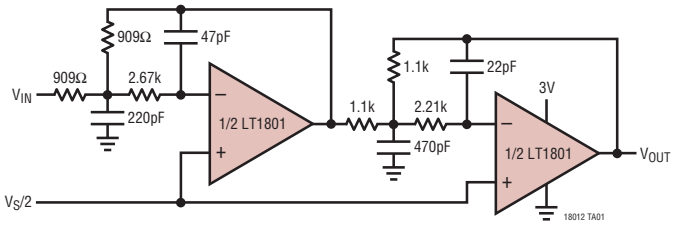
The LT1801/LT1802 maintain their performance for supplies from 2.3V to 12.6V and are specified at 3V, 5V and ±5V supplies. The inputs can be driven beyond the supplies without damage or phase reversal of the output.

The LT1801 is available in the MS8, SO-8 and the 3mm × 3mm × 0.8mm dual fine pitch leadless package (DFN) with the standard dual op amp pinout. The LT1802 features the standard quad op amp configuration and is available in the 14-pin plastic SO package. The LT1801/LT1802 can be used as plug-in replacements for many op amps to improve input/output range and performance.

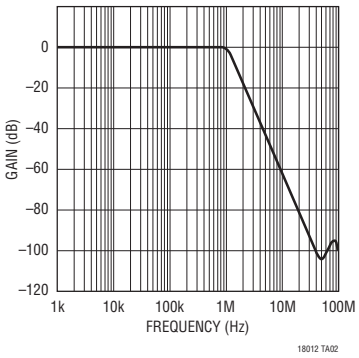
For a single version of these amplifiers, see the LT1800 data sheet.

TYPICAL APPLICATION

3V, 1MHz, 4th Order Butterworth Filter



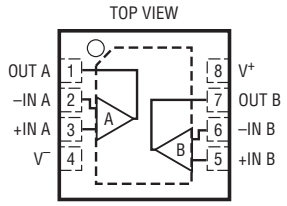
1MHz Filter Frequency Response



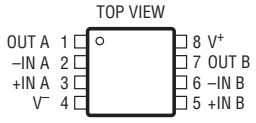
ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V_S^- to V_S^+) 12.6V
Input Current (Note 2) ..... ±10mA
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range (Note 4) ..–40°C to 85°C
Specified Temperature Range (Note 5) ....–40°C to 85°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Maximum Junction Temperature (DD Package).... 125°C
Storage Temperature (DD Package)..... –65°C to 125°C
Lead Temperature MSOP, SOIC
(Soldering, 10 sec)..... 300°C

PIN CONFIGURATION

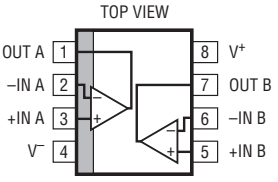


DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 160°C/W, (Note 10)
EXPOSED PAD INTERNALLY CONNECTED TO V^-.
(PCB CONNECTION OPTIONAL)



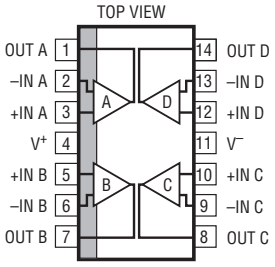
MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 250°C/W, (Note 10)



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 190°C/W, (Note 10)



S PACKAGE
14-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 160°C/W, (Note 10)

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	OPERATING TEMPERATURE RANGE
LT1801CDD#PBF	LT1801CDD#TRPBF	LAAM	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LT1801IDD#PBF	LT1801IDD#TRPBF	LAAM	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LT1801CMS8#PBF	LT1801CMS8#TRPBF	LTYR	8-Lead Plastic MSOP	–40°C to 85°C
LT1801IMS8#PBF	LT1801IMS8#TRPBF	LTYS	8-Lead Plastic MSOP	–40°C to 85°C
LT1801CS8#PBF	LT1801CS8#TRPBF	1801	8-Lead Plastic SO	–40°C to 85°C
LT1801IS8#PBF	LT1801IS8#TRPBF	1801I	8-Lead Plastic SO	–40°C to 85°C
LT1802CS#PBF	LT1802CS#TRPBF	LT1802CS	14-Lead Plastic SO	–40°C to 85°C
LT1802IS#PBF	LT1802IS#TRPBF	LT1802IS	14-Lead Plastic SO	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = 0V V_{CM} = 0V (MS8) V_{CM} = 0V (DD) V_{CM} = V_S		75 140 175 0.5	350 500 800 3	µV µV µV mV
ΔV_{OS}	Input Offset Shift	V_{CM} = 0V to V_S – 1.5V		20	185	µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	V_{CM} = 0V V_{CM} = 0V (MS8) V_{CM} = 0V (DD)		100 150 280	650 900 1200	µV µV µV
I_B	Input Bias Current	V_{CM} = 1V V_{CM} = V_S		25 500	250 1500	nA nA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	V_{CM} = 1V V_{CM} = V_S		25 25	350 500	nA nA
I_{OS}	Input Offset Current	V_{CM} = 1V V_{CM} = V_S		25 25	200 200	nA nA
	Input Noise Voltage	0.1Hz to 10Hz		1.4		μV_{P-P}
e_n	Input Noise Voltage Density	f = 10kHz		8.5		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 10kHz		1		$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance			2		pF
A_{VOL}	Large-Signal Voltage Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k at V_S/2 V_S = 5V, V_O = 1V to 4V, R_L = 100Ω at V_S/2 V_S = 3V, V_O = 0.5V to 2.5V, R_L = 1k at V_S/2	35 3.5 30	85 8 85		V/mV V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = 0V to 3.5V V_S = 3V, V_{CM} = 0V to 1.5V	85 78	105 97		dB dB
	CMRR Match (Channel-to-Channel) (Note 9)	V_S = 5V, V_{CM} = 0V to 3.5V V_S = 3V, V_{CM} = 0V to 1.5V	79 72	105 97		dB dB
	Input Common Mode Range		0		V_S	V
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 10V, V_{CM} = 0V	78	97		dB
	PSRR Match (Channel-to-Channel) (Note 9)	V_S = 2.5V to 10V, V_{CM} = 0V	72	97		dB
	Minimum Supply Voltage (Note 6)			2.3	2.5	V
V_{OL}	Output Voltage Swing Low (Note 7)	No Load I_{SINK} = 5mA I_{SINK} = 20mA		16 85 225	60 200 500	mV mV mV
V_{OH}	Output Voltage Swing High (Note 7)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 20mA		18 120 450	60 250 800	mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3V	20 20	45 40		mA mA
I_S	Supply Current per Amplifier			1.6	2	mA
GBW	Gain Bandwidth Product	Frequency = 2MHz	40	80		MHz
SR	Slew Rate	V_S = 5V, A_V = –1, R_L = 1k, V_O = 1V to 4V	12.5	25		V/µs
FPBW	Full Power Bandwidth	V_S = 5V, A_V = 1, V_O = $4V_{P-P}$		2		MHz
HD	Harmonic Distortion	V_S = 5V, A_V = 1, R_L = 1k, V_O = $2V_{P-P}$, f_C = 500kHz		–75		dBc
t_S	Settling Time	0.01%, V_S = 5V, V_{STEP} = 2V, A_V = 1, R_L = 1k		250		ns
ΔG	Differential Gain (NTSC)	V_S = 5V, A_V = 2, R_L = 150Ω		0.35		%
Δθ	Differential Phase (NTSC)	V_S = 5V, A_V = 2, R_L = 150Ω		0.4		Deg

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range of 0°C < T_A < 70°C. V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = 0V V_{CM} = 0V (MS8) V_{CM} = 0V (DD) V_{CM} = V_S	● ● ● ●		125 140 290 0.6	500 650 950 3.5	µV µV µV mV
ΔV_{OS}	Input Offset Shift	V_{CM} = 0V to V_S – 1.5V	●		30	275	µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	V_{CM} = 0V V_{CM} = 0V (MS8) V_{CM} = 0V (DD)	● ● ●		200 200 275	850 1250 1500	µV µV µV
V_{OS} TC	Input Offset Voltage Drift (Note 8)		●		1.5	5	µV/°C
I_B	Input Bias Current	V_{CM} = 1V V_{CM} = V_S – 0.2V	● ●		50 550	300 2000	nA nA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	V_{CM} = 1V V_{CM} = V_S – 0.2V	● ●		25 25	400 600	nA nA
I_{OS}	Input Offset Current	V_{CM} = 1V V_{CM} = V_S – 0.2V	● ●		25 25	300 300	nA nA
A_{VOL}	Large-Signal Voltage Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k at V_S/2 V_S = 5V, V_O = 1V to 4V, R_L = 100Ω at V_S/2 V_S = 3V, V_O = 0.5V to 2.5V, R_L = 1k at V_S/2	● ● ●	25 2.5 20	75 6 75		V/mV V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = 0V to 3.5V V_S = 3V, V_{CM} = 0V to 1.5V	● ●	82 74	101 93		dB dB
	CMRR Match (Channel-to-Channel) (Note 9)	V_S = 5V, V_{CM} = 0V to 3.5V V_S = 3V, V_{CM} = 0V to 1.5V	● ●	76 68	101 93		dB dB
	Input Common Mode Range		●	0		V_S	V
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 10V, V_{CM} = 0V	●	74	91		dB
	PSRR Match (Channel-to-Channel) (Note 9)	V_S = 2.5V to 10V, V_{CM} = 0V	●	68	91		dB
	Minimum Supply Voltage (Note 6)		●		2.3	2.5	V
V_{OL}	Output Voltage Swing Low (Note 7)	No Load I_{SINK} = 5mA I_{SINK} = 20mA	● ● ●		18 100 300	80 225 600	mV mV mV
V_{OH}	Output Voltage Swing High (Note 7)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 20mA	● ● ●		25 150 600	80 300 950	mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3V	● ●	20 15	40 30		mA mA
I_S	Supply Current per Amplifier		●		2	2.8	mA
GBW	Gain Bandwidth Product	Frequency = 2MHz	●	35	75		MHz
SR	Slew Rate	V_S = 5V, A_V = –1, R_L = 1k, V_O = 1V to 4V	●	11	22		V/µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range of $-40°C < T_A < 85°C$. V_S = 5V, 0V; V_S = 3V, 0V; $V_{CM} = V_{OUT}$ = half supply, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = 0V V_{CM} = 0V (MS8) V_{CM} = 0V (DD) $V_{CM} = V_S$	● ● ● ●		175 200 320 0.75	700 850 1150 4	µV µV µV mV
ΔV_{OS}	Input Offset Shift	V_{CM} = 0V to V_S – 1.5V	●		30	300	µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	V_{CM} = 0V V_{CM} = 0V (MS8) V_{CM} = 0V (DD)	● ● ●		200 280 320	1250 1600 1800	µV µV µV
V_{OS} TC	Input Offset Voltage Drift (Note 8)		●		1.5	5	µV/°C
I_B	Input Bias Current	 $V_{CM} = V_S$ – 0.2V	● ●		50 600	400 2250	nA nA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	V_{CM} = 1V $V_{CM} = V_S$ – 0.2V	● ●		25 25	450 700	nA nA
I_{OS}	Input Offset Current	V_{CM} = 1V $V_{CM} = V_S$ – 0.2V	● ●		25 25	350 350	nA nA
A_{VOL}	Large-Signal Voltage Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k at $V_S/2$ V_S = 5V, V_O = 1.5V to 3.5V, R_L = 100Ω at $V_S/2$ V_S = 3V, V_O = 0.5V to 2.5V, R_L = 1k at $V_S/2$	● ● ●	20 2 17.5	65 6 65		V/mV V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = 0V to 3.5V V_S = 3V, V_{CM} = 0V to 1.5V	● ●	81 73	101 93		dB dB
	CMRR Match (Channel-to-Channel) (Note 9)	V_S = 5V, V_{CM} = 0V to 3.5V V_S = 3V, V_{CM} = 0V to 1.5V	● ●	75 67	101 93		dB dB
	Input Common Mode Range		●	0		V_S	V
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 10V, V_{CM} = 0V	●	73	90		dB
	PSRR Match (Channel-to-Channel) (Note 9)	V_S = 2.5V to 10V, V_{CM} = 0V	●	67	90		dB
	Minimum Supply Voltage (Note 6)	$V_{CM} = V_O$ = 0.5V	●		2.3	2.5	V
V_{OL}	Output Voltage Swing Low (Note 7)	No Load I_{SINK} = 5mA I_{SINK} = 10mA	● ● ●		15 105 170	90 250 400	mV mV mV
V_{OH}	Output Voltage Swing High (Note 7)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 10mA	● ● ●		25 150 300	90 350 700	mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3V	● ●	12.5 12.5	30 30		mA mA
I_S	Supply Current per Amplifier		●		2.1	3	mA
GBW	Gain Bandwidth Product	Frequency = 2MHz	●	25	70		MHz
SR	Slew Rate	V_S = 5V, A_V = –1, R_L = 1k, V_O = 1V to 4V	●	9	18		V/µs

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = \pm5V$, $V_{CM} = 0V$, $V_{OUT} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V_S^-$ $V_{CM} = V_S^-$ (MS8) $V_{CM} = V_S^-$ (DD) $V_{CM} = V_S^+$		150 180 260 0.7	600 750 1050 3.5	µV µV µV mV
ΔV_{OS}	Input Offset Shift	$V_{CM} = V_S^-$ to $V_S^+ - 1.5V$		30	475	µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	$V_{CM} = V_S^-$ $V_{CM} = V_S^-$ (MS8) $V_{CM} = V_S^-$ (DD)		150 275 325	1000 1300 1600	µV µV µV
I_B	Input Bias Current	$V_{CM} = V_S^- + 1V$ $V_{CM} = V_S^+$		25 400	250 1500	nA nA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	$V_{CM} = V_S^- + 1V$ $V_{CM} = V_S^+$		20 20	350 500	nA nA
I_{OS}	Input Offset Current	$V_{CM} = V_S^- + 1V$ $V_{CM} = V_S^+$		20 20	250 250	nA nA
	Input Noise Voltage	0.1Hz to 10Hz		1.4		$\mu V/_{P-P}$
e_n	Input Noise Voltage Density	f = 10kHz		8.5		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 10kHz		1		$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance	f = 100kHz		2		pF
A_{VOL}	Large-Signal Voltage Gain	$V_O = -4V$ to 4V, $R_L = 1k$ $V_O = -2V$ to 2V, $R_L = 100\Omega$	25 2.5	70 7		V/mV V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = V_S^-$ to 3.5V	85	109		dB
	CMRR Match (Channel-to-Channel) (Note 9)	$V_{CM} = V_S^-$ to 3.5V	79	109		dB
	Input Common Mode Range		V_S^-		V_S^+	V
PSRR	Power Supply Rejection Ratio	$V_S^+ = 2.5V$ to 10V, $V_S^- = 0V$	78	97		dB
	PSRR Match (Channel-to-Channel) (Note 9)	$V_S^+ = 2.5V$ to 10V, $V_S^- = 0V$	72	97		dB
V_{OL}	Output Voltage Swing Low (Note 7)	No Load $I_{SINK} = 5mA$ $I_{SINK} = 20mA$		15 90 225	70 200 500	mV mV mV
V_{OH}	Output Voltage Swing High (Note 7)	No Load $I_{SOURCE} = 5mA$ $I_{SOURCE} = 20mA$		20 130 450	80 260 850	mV mV mV
I_{SC}	Short-Circuit Current		25	50		mA
I_S	Supply Current per Amplifier			1.8	3	mA
GBW	Gain Bandwidth Product	Frequency = 2MHz		70		MHz
FPBW	Full Power Bandwidth	$V_O = 8V_{P-P}$		0.9		MHz
SR	Slew Rate	$A_V = -1$, $R_L = 1k$, $V_O = \pm4V$, Measured at $V_O = \pm2V$		20		V/µs
HD	Harmonic Distortion	$A_V = 1$, $R_L = 1k$, $V_O = 2V_{P-P}$, $f_C = 500kHz$		–75		dBc
t_S	Settling Time	0.01%, $V_{STEP} = 5V$, $A_V = 1V$, $R_L = 1k$		300		ns
ΔG	Differential Gain (NTSC)	$A_V = 2$, $R_L = 150\Omega$		0.35		%
$\Delta\theta$	Differential Phase (NTSC)	$A_V = 2$, $R_L = 150\Omega$		0.2		deg

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range of 0°C < T_A < 70°C. V_S = ±5V, V_{CM} = 0V, V_{OUT} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V_S^-$ $V_{CM} = V_S^-$ (MS8) $V_{CM} = V_S^-$ (DD) $V_{CM} = V_S^+$	● ● ● ●		200 220 290 0.75	800 1000 1300 4	µV µV µV mV
ΔV_{OS}	Input Offset Shift	$V_{CM} = V_S^-$ to $V_S^+ - 1.5V$	●		45	675	µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	$V_{CM} = V_S^-$ $V_{CM} = V_S^-$ (MS8) $V_{CM} = V_S^-$ (DD)	● ● ●		240 300 340	1500 1700 1950	µV µV µV
V_{OS} TC	Input Offset Voltage Drift (Note 8)		●		1.5	5	µV/°C
I_B	Input Bias Current	$V_{CM} = V_S^- + 1V$ $V_{CM} = V_S^+ - 0.2V$	● ●		30 450	300 2000	nA nA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	$V_{CM} = V_S^- + 1V$ $V_{CM} = V_S^+ - 0.2V$	● ●		25 25	400 700	nA nA
I_{OS}	Input Offset Current	$V_{CM} = V_S^- + 1V$ $V_{CM} = V_S^+ - 0.2V$	● ●		25 25	300 300	nA nA
A_{VOL}	Large-Signal Voltage Gain	V_O = –4V to 4V, R_L = 1k V_O = –2V to 2V, R_L = 100Ω	● ●	15 2	55 5		V/mV V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = V_S^-$ to 3.5V	●	82	105		dB
	CMRR Match (Channel-to-Channel) (Note 9)	$V_{CM} = V_S^-$ to 3.5V	●	76	105		dB
	Input Common Mode Range		●	V_S^-		V_S^+	V
PSRR	Power Supply Rejection Ratio	V_S^+ = 2.5V to 10V, V_S^- = 0V	●	74	91		dB
	PSRR Match (Channel-to-Channel) (Note 9)	V_S^+ = 2.5V to 10V, V_S^- = 0V	●	68	93		dB
V_{OL}	Output Voltage Swing Low (Note 7)	No Load I_{SINK} = 5mA I_{SINK} = 20mA	● ● ●		17 105 250	80 250 575	mV mV mV
V_{OH}	Output Voltage Swing High (Note 7)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 20mA	● ● ●		25 150 600	90 310 975	mV mV mV
I_{SC}	Short-Circuit Current		●	22.5	45		mA
I_S	Supply Current per Amplifier		●		2.4	4	mA
GBW	Gain Bandwidth Product	Frequency = 2MHz	●		70		MHz
SR	Slew Rate	A_V = –1, R_L = 1k, V_O = ±4V, Measured at V_O = ±2V	●		20		V/µs

The ● denotes the specifications which apply over the temperature range of –40°C < T_A < 85°C. V_S = ±5V, V_{CM} = 0V, V_{OUT} = 0V, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V_S^-$ $V_{CM} = V_S^-$ (MS8) $V_{CM} = V_S^-$ (DD) $V_{CM} = V_S^+$	● ● ● ●		350 350 350 0.75	1000 1200 1500 5	µV µV µV mV
ΔV_{OS}	Input Offset Shift	$V_{CM} = V_S^-$ to $V_S^+ - 1.5V$	●		50	750	µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	$V_{CM} = V_S^-$ $V_{CM} = V_S^-$ (MS8) $V_{CM} = V_S^-$ (DD)	● ● ●		280 380 410	1700 1900 2100	µV µV µV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range of $-40°C < T_A < 85°C$. $V_S = \pm5V$, $V_{CM} = 0V$, $V_{OUT} = 0V$, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS} TC	Input Offset Voltage Drift (Note 8)		●		1.5	5	μV/°C
I_B	Input Bias Current	$V_{CM} = V_S^- + 1V$ $V_{CM} = V_S^+ - 0.2V$	● ●		50 450	400 2250	nA nA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	$V_{CM} = V_S^- + 1V$ $V_{CM} = V_S^+ - 0.2V$	● ●		25 25	450 700	nA nA
I_{OS}	Input Offset Current	$V_{CM} = V_S^- + 1V$ $V_{CM} = V_S^+ - 0.2V$	● ●		25 25	350 350	nA nA
A_{VOL}	Large-Signal Voltage Gain	$V_O = -4V$ to $4V$, $R_L = 1k$ $V_O = -1V$ to $1V$, $R_L = 100\Omega$	● ●	12.5 2	55 5		V/mV V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = V_S^-$ to 3.5V	●	81	104		dB
	CMRR Match (Channel-to-Channel) (Note 9)	$V_{CM} = V_S^-$ to 3.5V	●	75	104		dB
	Input Common Mode Range		●	V_S^-		V_S^+	V
PSRR	Power Supply Rejection Ratio	$V_S^+ = 2.5V$ to $10V$, $V_S^- = 0V$	●	73	90		dB
	PSRR Match (Channel-to-Channel) (Note 9)	$V_S^+ = 2.5V$ to $10V$, $V_S^- = 0V$	●	67	90		dB
V_{OL}	Output Voltage Swing Low (Note 7)	No Load $I_{SINK} = 5mA$ $I_{SINK} = 10mA$	● ● ●		20 110 180	100 275 400	mV mV mV
V_{OH}	Output Voltage Swing High (Note 7)	No Load $I_{SOURCE} = 5mA$ $I_{SOURCE} = 10mA$	● ● ●		30 150 300	110 350 700	mV mV mV
I_{SC}	Short-Circuit Current		●	12.5	30		mA
I_S	Supply Current per Amplifier		●		2.6	4.5	mA
GBW	Gain Bandwidth Product	Frequency = 2MHz	●		65		MHz
SR	Slew Rate	$A_V = -1$, $R_L = 1k$, $V_O = \pm4V$, Measured at $V_O = \pm2V$	●		15		V/μs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by back-to-back diodes. If the differential input voltage exceeds 1.4V, the input current should be limited to less than 10mA. It is not 100% tested.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: The LT1801C/LT1801I and LT1802C/LT1802I are guaranteed functional over the temperature range of –40°C to 85°C.

Note 5: The LT1801C/LT1802C are guaranteed to meet specified performance from 0°C to 70°C. The LT1801C/LT1802C are designed, characterized and expected to meet specified performance from –40°C to 85°C but are not tested or QA sampled at these temperatures. The LT1801I/LT1802I are guaranteed to meet specified performance from –40°C to 85°C.

Note 6: Minimum supply voltage is guaranteed by power supply rejection ratio test.

Note 7: Output voltage swings are measured between the output and power supply rails.

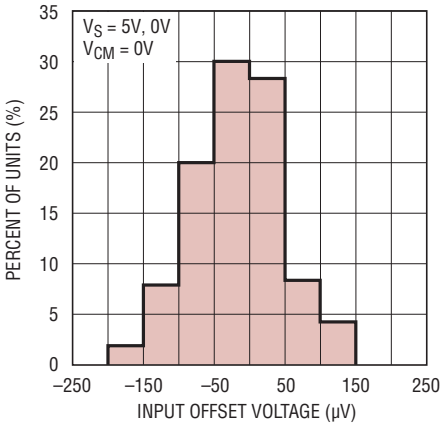
Note 8: This parameter is not 100% tested.

Note 9: Matching parameters are the difference between amplifiers A and D and between B and C on the LT1802; between the two amplifiers on the LT1801.

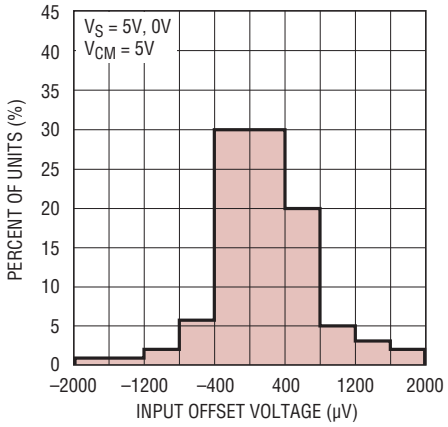
Note 10: Thermal resistance (θ_{JA}) varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads. If desired, the thermal resistance can be substantially reduced by connecting Pin 4 of the SO-8 and MS8, Pin 11 of the SO-14 or the underside metal of the DD package to a larger metal area (V_S^- trace).

TYPICAL PERFORMANCE CHARACTERISTICS

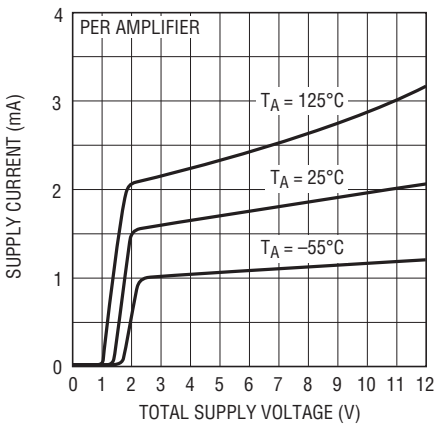
V_{OS} Distribution, V_{CM} = 0V (PNP Stage)



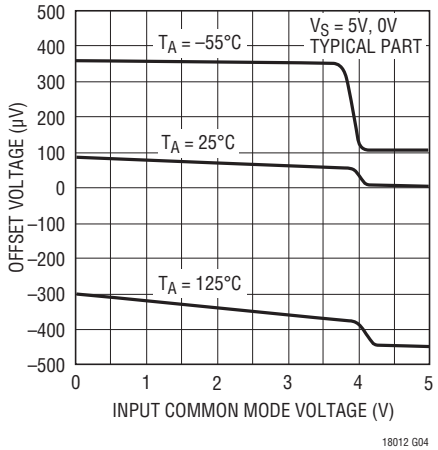
V_{OS} Distribution, V_{CM} = 5V (NPN Stage)



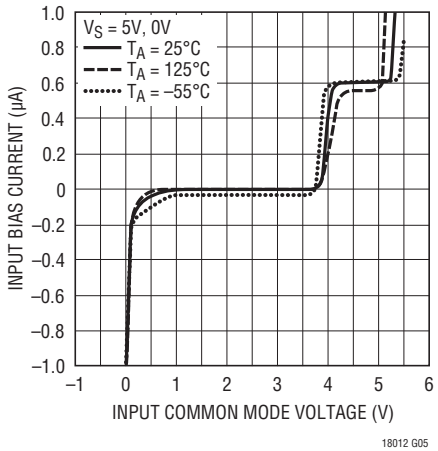
Supply Current vs Supply Voltage



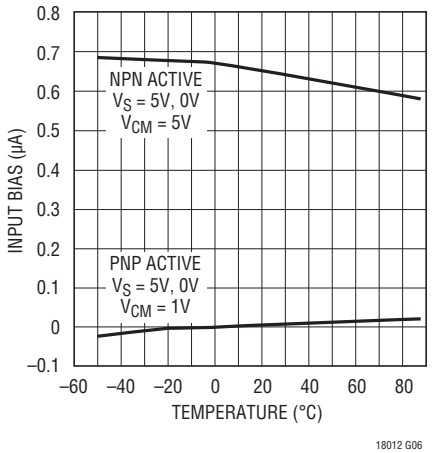
Offset Voltage vs Input Common Mode Voltage



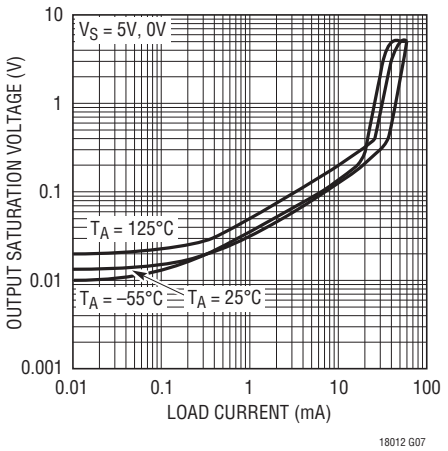
Input Bias Current vs Common Mode Voltage



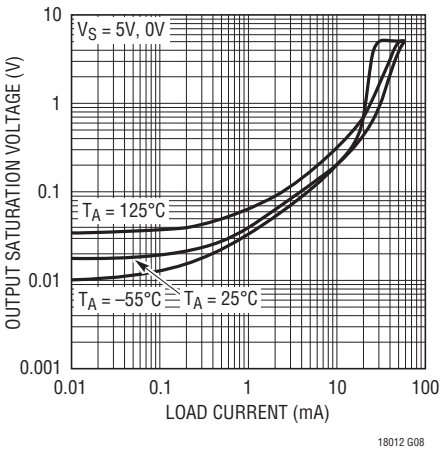
Input Bias Current vs Temperature



Output Saturation Voltage vs Load Current (Output Low)

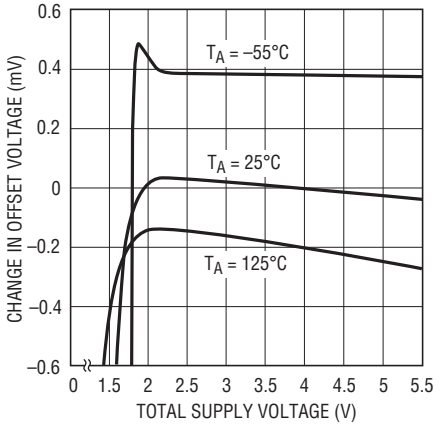


Output Saturation Voltage vs Load Current (Output High)

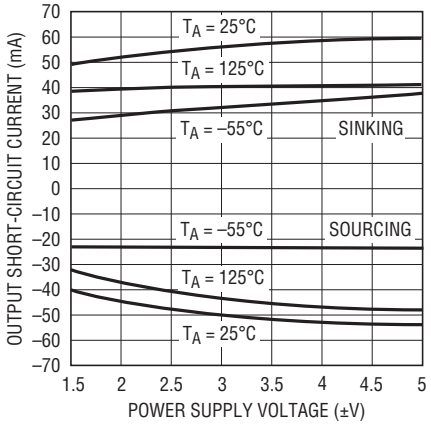


TYPICAL PERFORMANCE CHARACTERISTICS

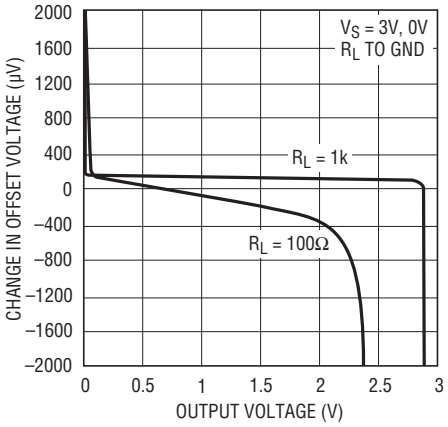
Minimum Supply Voltage



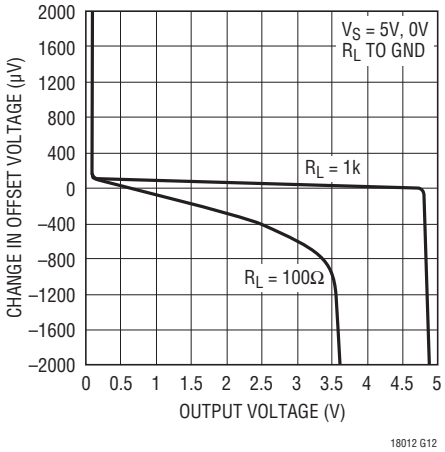
Output Short-Circuit Current vs Power Supply Voltage



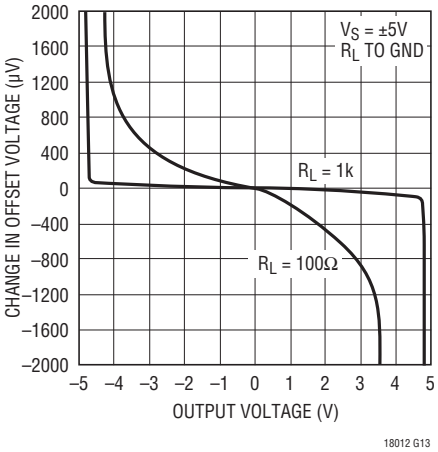
Open-Loop Gain



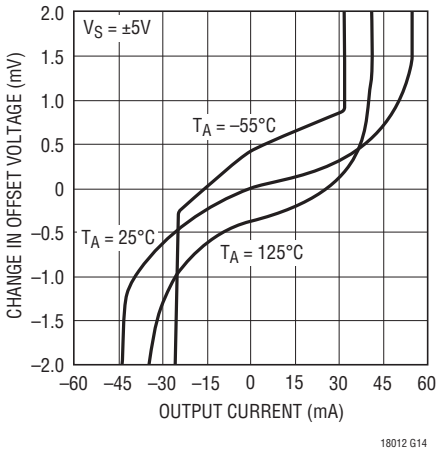
Open-Loop Gain



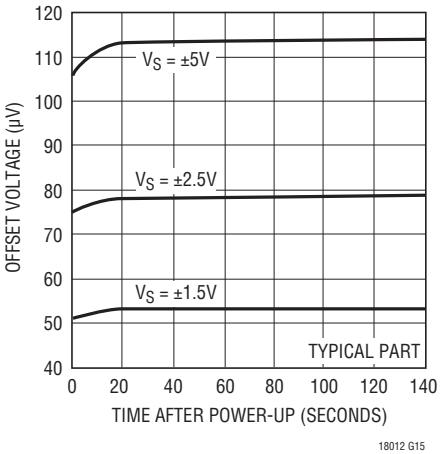
Open-Loop Gain



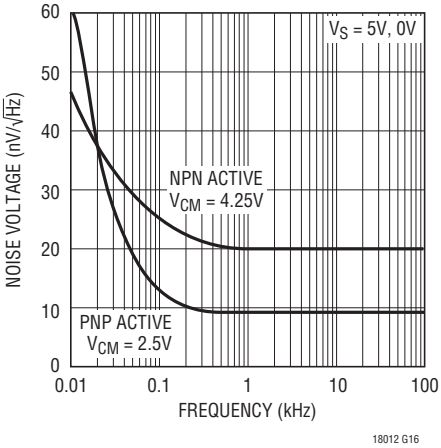
Offset Voltage vs Output Current



Warm-Up Drift vs Time

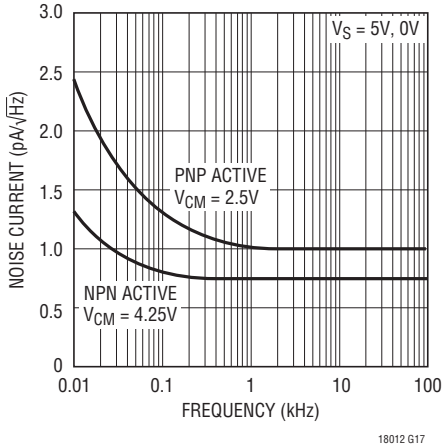


Input Noise Voltage vs Frequency

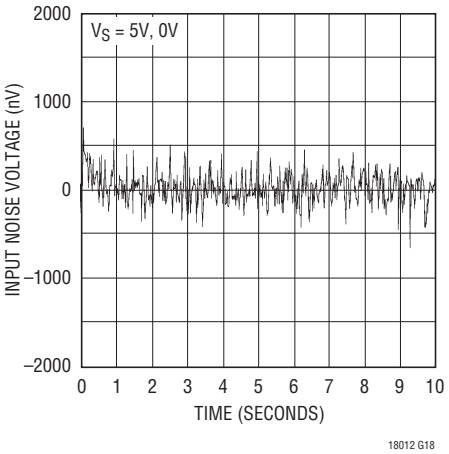


TYPICAL PERFORMANCE CHARACTERISTICS

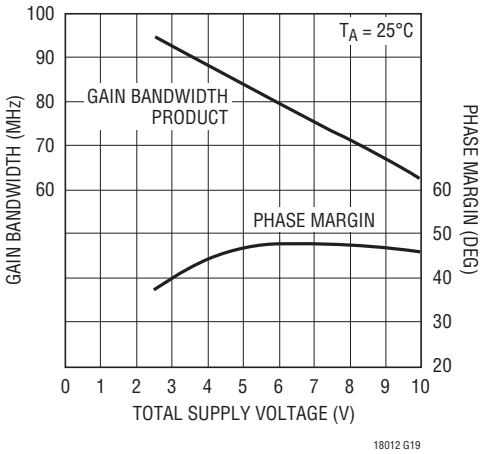
Input Current Noise vs Frequency



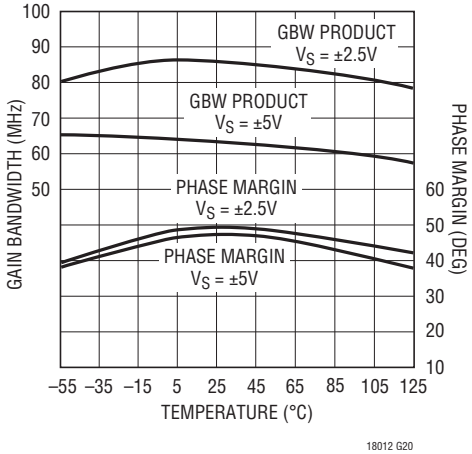
0.1Hz to 10Hz Input Voltage



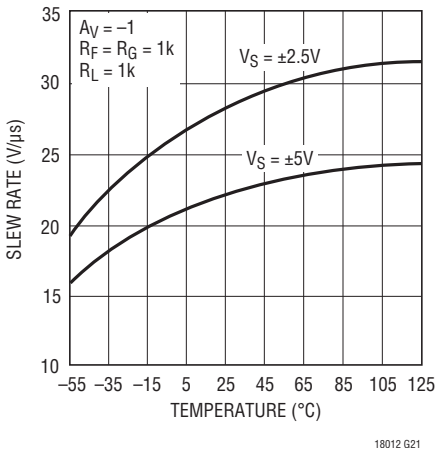
Gain Bandwidth and Phase Margin vs Supply Voltage



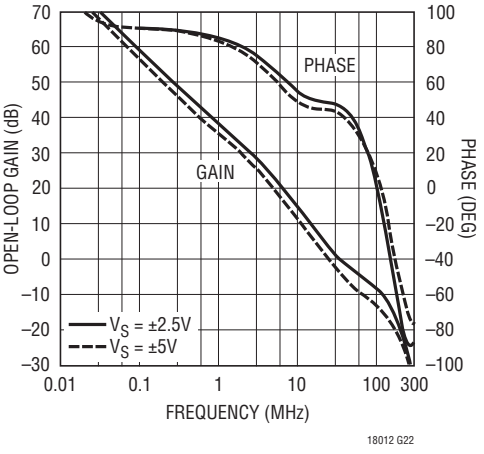
Gain Bandwidth and Phase Margin vs Temperature



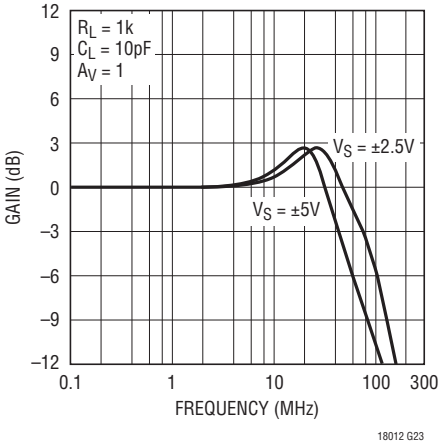
Slew Rate vs Temperature



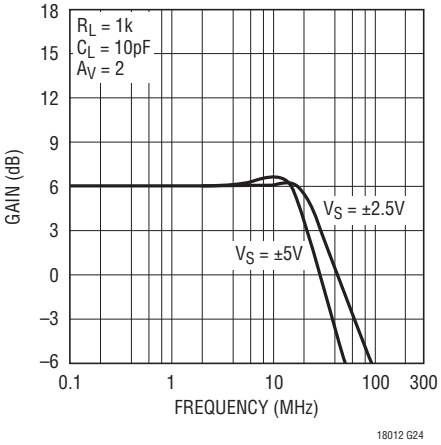
Gain and Phase vs Frequency



Gain vs Frequency (A_V = 1)

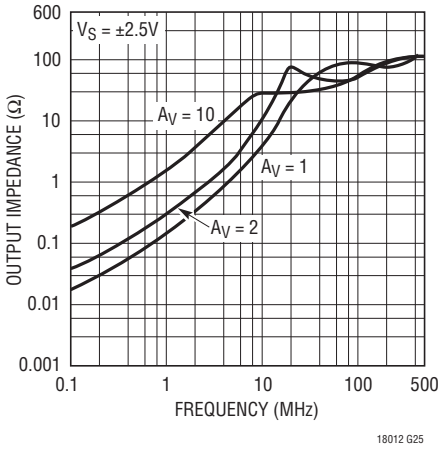


Gain vs Frequency (A_V = 2)

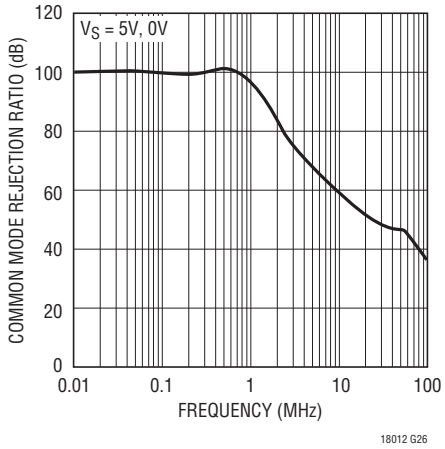


TYPICAL PERFORMANCE CHARACTERISTICS

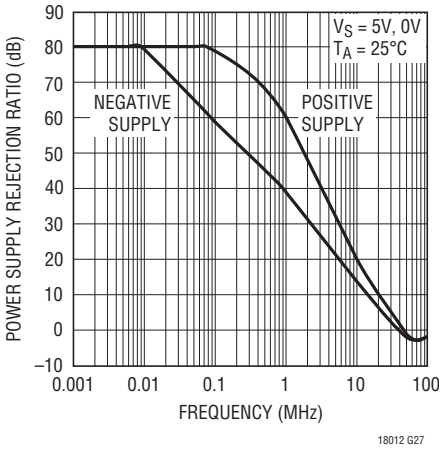
Output Impedance vs Frequency



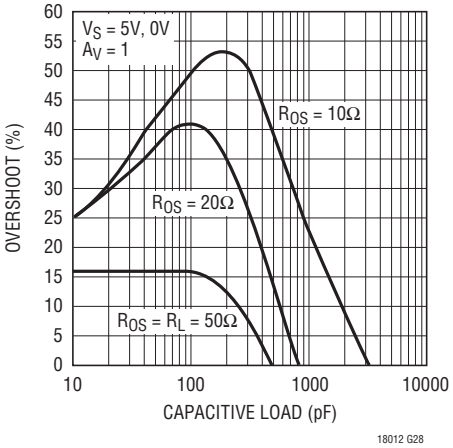
Common Mode Rejection Ratio vs Frequency



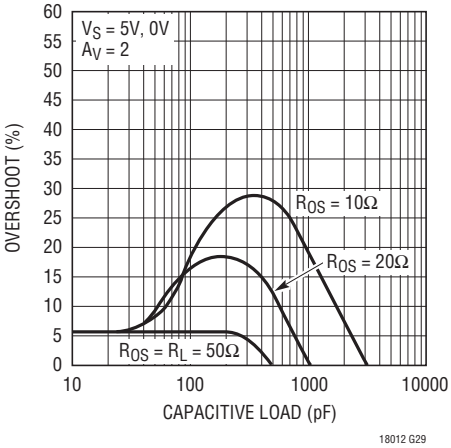
Power Supply Rejection Ratio vs Frequency



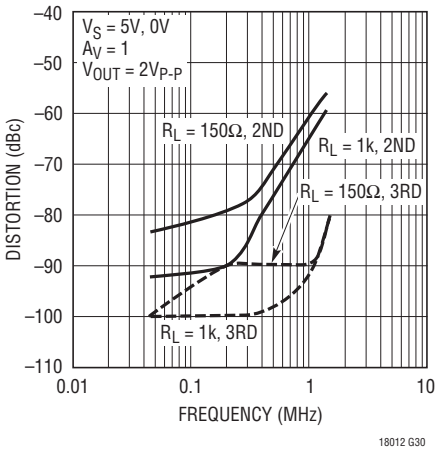
Series Output Resistor vs Capacitive Load



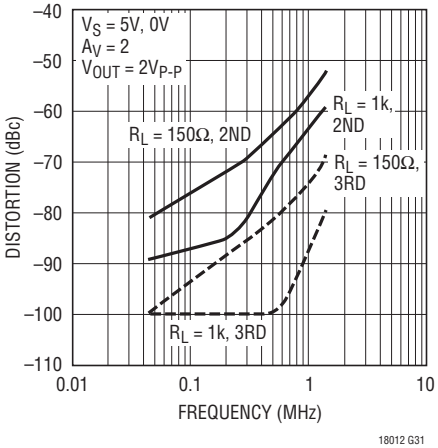
Series Output Resistor vs Capacitive Load



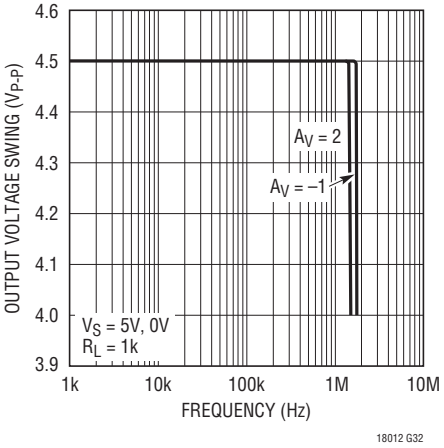
Distortion vs Frequency



Distortion vs Frequency

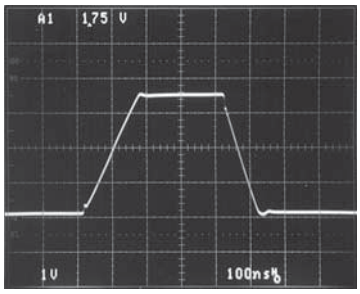


Maximum Undistorted Output Signal vs Frequency



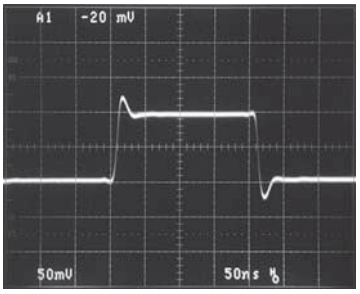
TYPICAL PERFORMANCE CHARACTERISTICS

5V Large-Signal Response



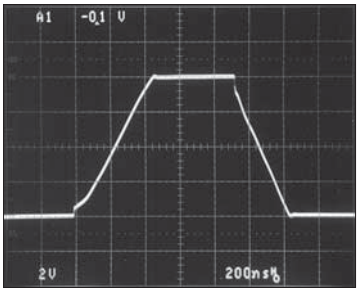
V_S = 5V, 0V 100ns/DIV 18012 G33
A_V = 1
R_L = 1k

5V Small-Signal Response



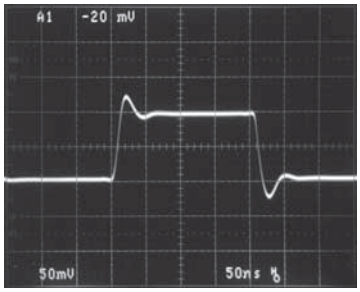
V_S = 5V, 0V 50ns/DIV 18012 G34
A_V = 1
R_L = 1k

±5V Large-Signal Response



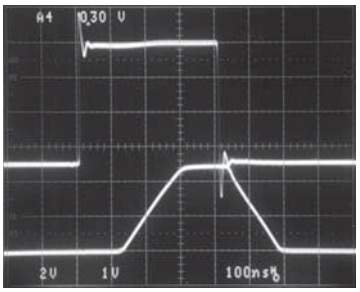
V_S = ±5V 200ns/DIV 18012 G35
A_V = 1
R_L = 1k

±5V Small-Signal Response



V_S = ±5V 50ns/DIV 18012 G36
A_V = 1
R_L = 1k

Output Overdriven Recovery



V_S = 5V, 0V 100ns/DIV 18012 G37
A_V = 2
R_L = 1k

APPLICATIONS INFORMATION

Circuit Description

The LT1801/LT1802 have an input and output signal range that covers from the negative power supply to the positive power supply. Figure 1 depicts a simplified schematic of the amplifier. The input stage is comprised of two differential amplifiers, a PNP stage Q1/Q2 and an NPN stage Q3/Q4 that are active over the different ranges of common mode input voltage. The PNP differential pair is active between the negative supply to approximately 1.2V below the positive supply. As the input voltage moves closer toward the positive supply, the transistor Q5 will steer the tail current I_1 to the current mirror Q6/Q7, activating the NPN differential pair and the PNP pair becomes inactive for the rest of the input common mode range up to the positive supply. Also at the input stage, devices Q17 to Q19 act to cancel the bias current of the PNP input pair. When Q1-Q2 are active, the current in Q16 is controlled to be the same as the current in Q1-Q2, thus the base current of Q16 is nominally equal to the base current of the input devices. The base current of Q16 is then mirrored by devices Q17-Q19 to cancel the base current of the input devices Q1-Q2.

A pair of complementary common emitter stages Q14/Q15 that enable the output to swing from rail to rail constructs the output stage. The capacitors C2 and C3 form the local feedback loops that lower the output impedance at high frequency. These devices are fabricated on Linear Technology's proprietary high speed complementary bipolar process.

Power Dissipation

The LT1801 amplifier is offered in a small package, SO-8, which has a thermal resistance of 190°C/W, θ_{JA}. So there is a need to ensure that the die's junction temperature should not exceed 150°C. Junction temperature T_J is calculated from the ambient temperature T_A, power dissipation P_D and thermal resistance θ_{JA}:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

The power dissipation in the IC is the function of the supply voltage, output voltage and the load resistance. For a given supply voltage, the worst-case power dissipation P_{DMAX} occurs at the maximum supply current and the

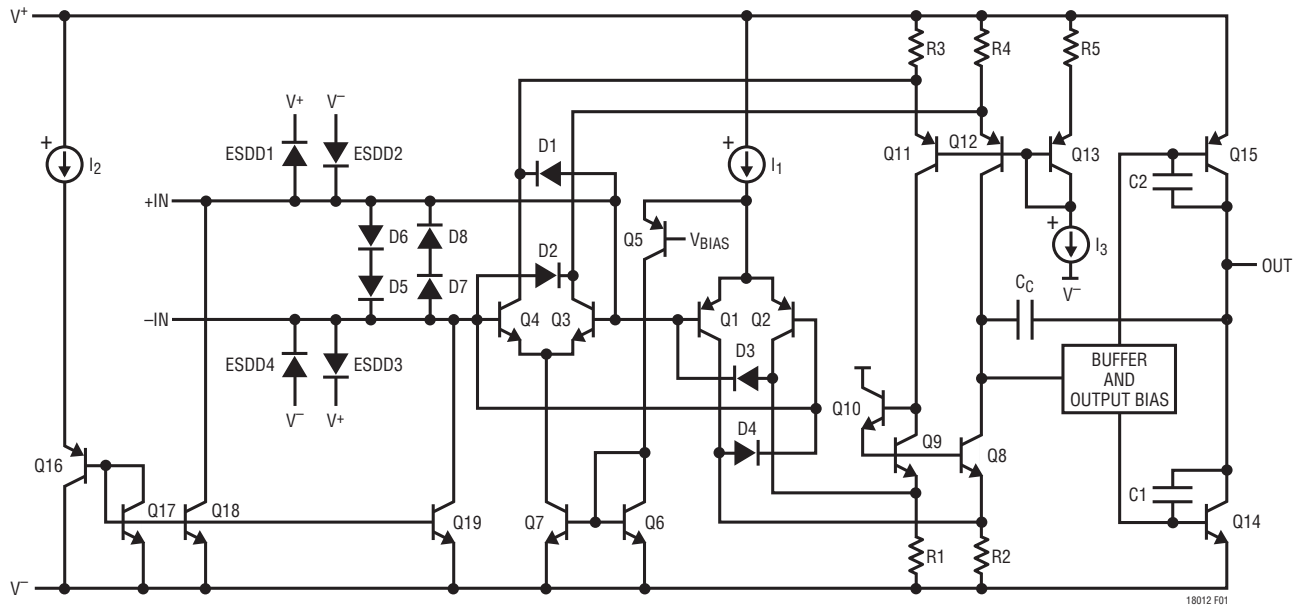


Figure 1. LT1801/LT1802 Simplified Schematic Diagram

APPLICATIONS INFORMATION

output voltage is at half of either supply voltage (or the maximum swing is less than 1/2 supply voltage). P_{DMAX} is given by:

$$P_{DMAX} = (V_S \bullet I_{SMAX}) + (V_S/2)^2/R_L$$

Example: An LT1801 in an SO-8 package operating on ±5V supplies and driving a 50Ω load, the worst-case power dissipation is given by:

$$P_{DMAX} = (10 \bullet 4.5mA) + (2.5)^2/50 = 0.045 + 0.125 = 0.17W$$

If both amplifiers are loaded simultaneously, then the total power dissipation is 0.34W.

The maximum ambient temperature that the part is allowed to operate is:

$$T_A = T_J - (P_{DMAX} \bullet 190°C/W)$$
$$= 150°C - (0.34W \bullet 190°C/W) = 85°C$$

Input Offset Voltage

The offset voltage will change depending upon which input stage is active. The PNP input stage is active from the negative supply rail to 1.2V from the positive supply rail, then the NPN input stage is activated for the remaining input range up to the positive supply rail during which the PNP stage remains inactive. The offset voltage is typically less than 75µV in the range that the PNP input stage is active.

Input Bias Current

The LT1801/LT1802 employ a patent-pending technique to trim the input bias current to less than 250nA for the input common mode voltage of 0.2V above negative supply rail to 1.2V of the positive rail. The low input offset voltage and low input bias current of the LT1801/LT1802 provide precision performance especially for high source impedance applications.

Output

The LT1801/LT1802 can deliver a large output current, so the short-circuit current limit is set around 50mA to prevent damage to the device. Attention must be paid to keep the junction temperature of the IC below the absolute maximum rating of 150°C (refer to the Power Dissipation section) when the output is continuously short circuited. The output of the amplifier has reverse-biased diodes connected to each supply. If the output is forced beyond either supply, unlimited current will flow through these diodes. If the current is transient and limited to several hundred mA and the total supply voltage is less than 12.6V, the absolute maximum rating, no damage will occur to the device.

Overdrive Protection

When the input voltage exceeds the power supplies, two pairs of crossing diodes D1 to D4 will prevent the output from reversing polarity. If the input voltage exceeds either power supply by 700mV, diode D1/D2 or D3/D4 will turn on to keep the output at the proper polarity. For the phase reversal protection to perform properly, the input current must be limited to less than 10mA. If the amplifier is severely overdriven, an external resistor should be used to limit the overdrive current.

The LT1801/LT1802's input stages are also protected against a large differential input voltage of 1.4V or higher by a pair of back-back diodes D5/D8 to prevent the emitter-base breakdown of the input transistors. The current in these diodes should be limited to less than 10mA when they are active. The worst-case differential input voltage usually occurs when the input is driven while the output is shorted to ground in a unity gain configuration. In addition, the amplifier is protected against ESD strikes up to 3kV on all pins by a pair of protection diodes on each pin that are connected to the power supplies as shown in Figure 1.

APPLICATIONS INFORMATION

Capacitive Load

The LT1801/LT1802 are optimized for high bandwidth, low power and precision applications. They can drive a capacitive load of about 75pF in a unity-gain configuration, and more for higher gain. When driving a larger capacitive load, a resistor of 10Ω to 50Ω should be connected between the output and the capacitive load to avoid ringing or oscillation. The feedback should still be taken from the output so that the resistor will isolate the capacitive load to ensure stability. Graphs on capacitive loads indicate the transient response of the amplifier when driving capacitive load with a specified series resistor.

Feedback Components

When feedback resistors are used to set up gain, care must be taken to ensure that the pole formed by the feedback resistors and the total capacitance at the inverting input does not degrade stability. For instance, the LT1801/LT1802 in a noninverting gain of 2, setup with two 5k resistors and a capacitance of 5pF (part plus PC board) will probably oscillate. The pole is formed at 12.7MHz that will reduce phase margin by 57 degrees when the crossover frequency of the amplifier is around 20MHz. A capacitor of 5pF or higher connected across the feedback resistor will eliminate any ringing or oscillation.

TYPICAL APPLICATIONS

Single 3V Supply, 1MHz, 4th Order Butterworth Filter

The circuit shown on the first page of this data sheet makes use of the low voltage operation and the wide bandwidth of the LT1801 to create a DC accurate 1MHz 4th order lowpass filter powered from a 3V supply. The amplifiers are configured in the inverting mode for the lowest distortion and the output can swing rail-to-rail for maximum dynamic range. Also on the first page of this data sheet, the graph displays the frequency response of the filter. Stopband attenuation is greater than 100dB at 50MHz. With a 2.25V_{P-P}, 250kHz input signal, the filter has harmonic distortion products of less than –85dBc. Worst case output offset voltage is less than 6mV.

Fast 1A Current Sense Amplifier

A simple, fast current sense amplifier in Figure 2 is suitable for quickly responding to out-of-range currents. The circuit amplifies the voltage across the 0.1Ω sense resistor by a gain of 20, resulting in a conversion gain of 2V/A. The –3dB bandwidth of the circuit is 4MHz, and the uncertainty due to V_{OS} and I_B is less than 4mA. The minimum output voltage is 60mV, corresponding to 30mA. The large-signal response of the circuit is shown in Figure 3.

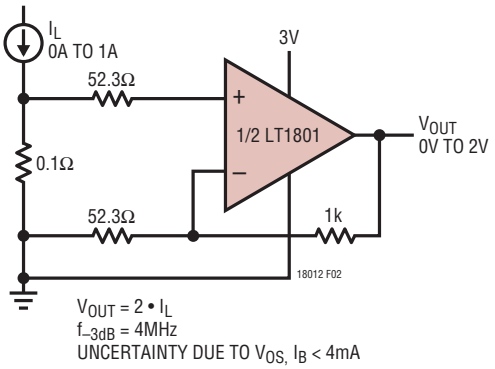


Figure 2. Fast 1A Current Sense

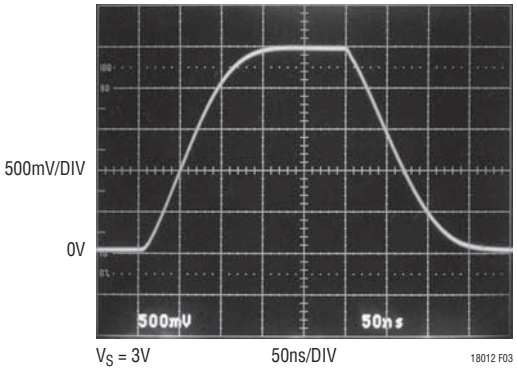


Figure 3. Current Sense Amplifier Large-Signal Response

TYPICAL APPLICATIONS

Single Supply 1A Laser Driver Amplifier

Figure 4 shows the LT1801 used in a 1A laser driver application. One of the reasons the LT1801 is well suited to this control task is that its 2.3V operation ensures that it will be awaked during power-up and operated before the circuit can otherwise cause significant current to flow in the 2.1V threshold laser diode. Driving the noninverting input of the LT1801 to a voltage V_{IN} will control the turning on of the high current NPN transistor, FMMT619 and the laser diode. A current equal to V_{IN}/R1 flows through the laser diode. The LT1801 low offset voltage and low input bias current allows it to control the current that flows through the laser diode precisely. The overall circuit is a 1A per volt V-to-I converter. Frequency compensation components R2 and C1 are selected for fast but zero-overshoot time domain response to avoid overcurrent conditions in the laser. The time domain response of this circuit, measured at R1 and given a 500mV 230ns input pulse, is shown in Figure 5. While the circuit is capable of 1A operation, the laser diode and the transistor are thermally limited due to power dissipation, so they must be operated at low duty cycles.

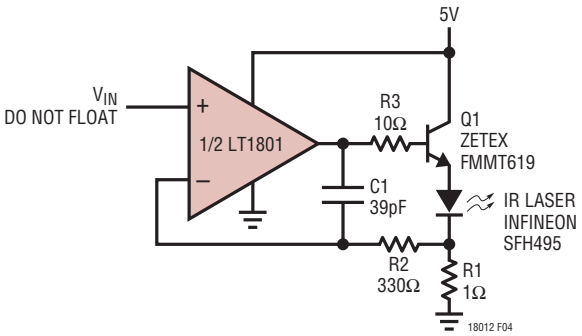


Figure 4. Single Supply 1A Laser Driver Amplifier

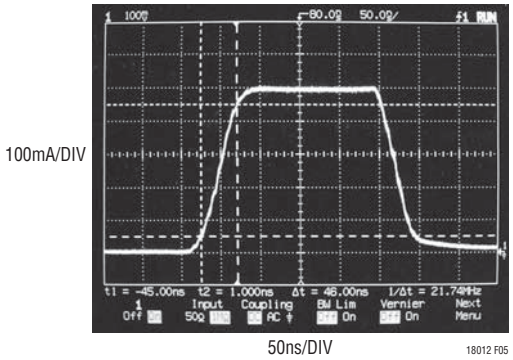
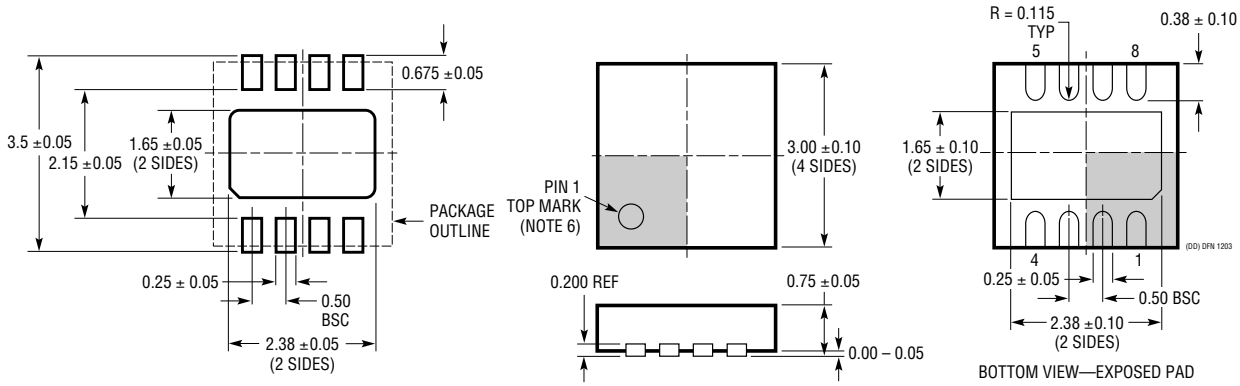


Figure 5. 500mA Pulse Response

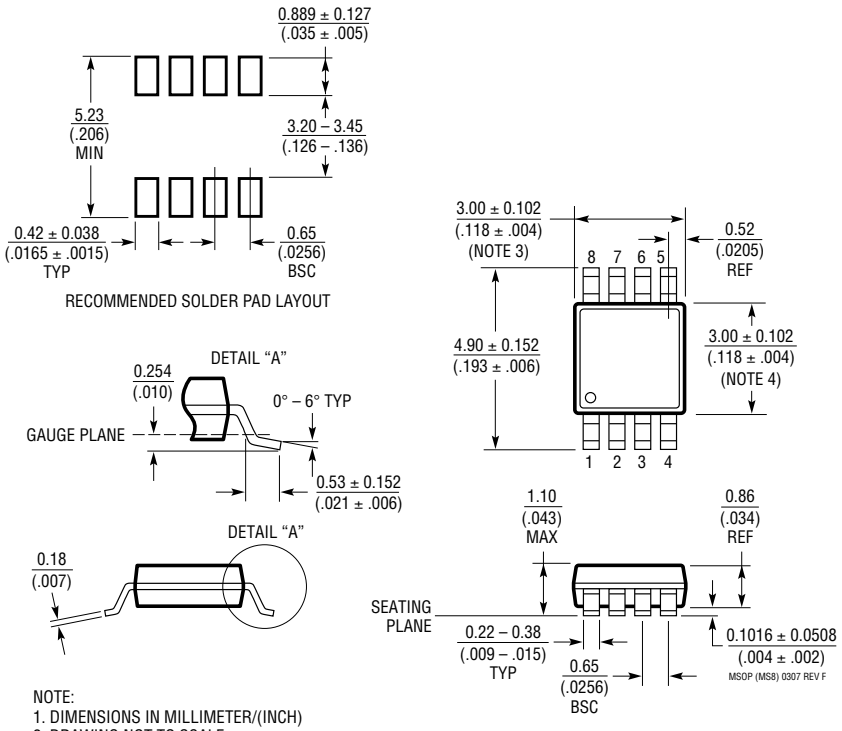
PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

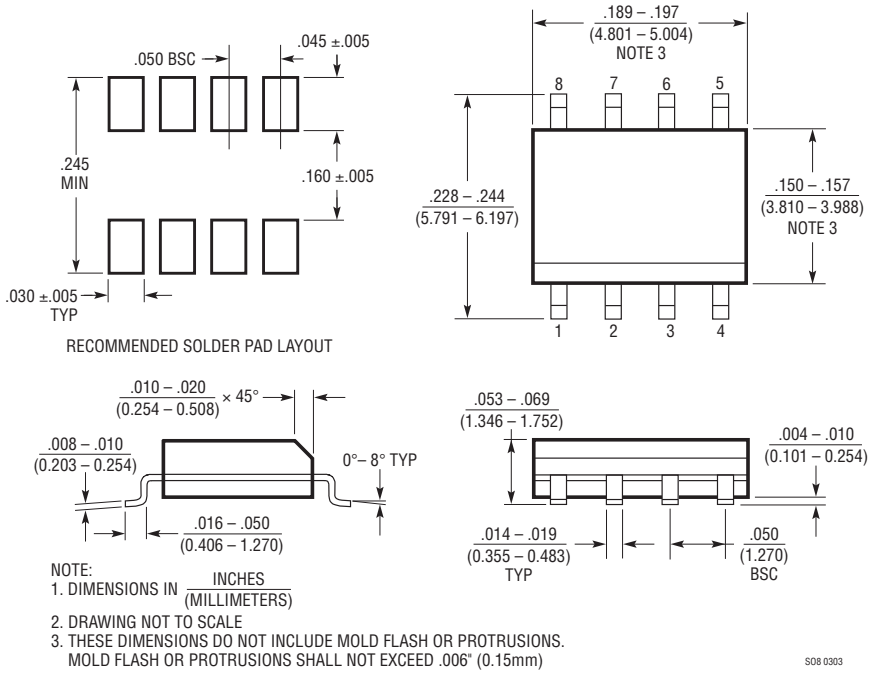
MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev F)



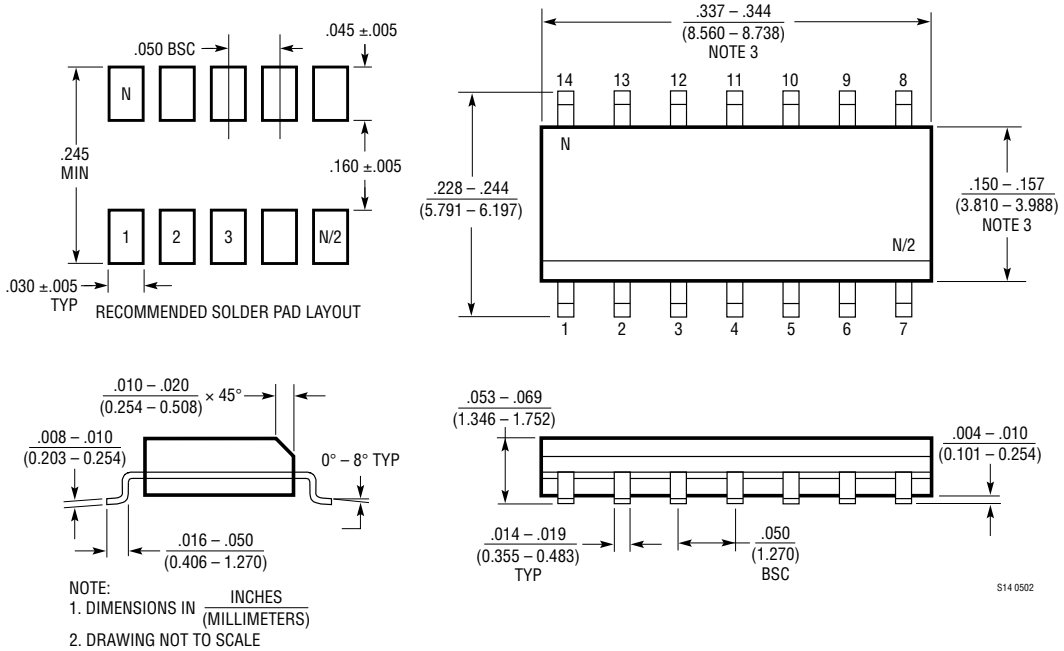
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



S Package
14-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Low Power High Voltage Amplifier

Certain materials used in optical applications have characteristics that change due to the presence and strength of a DC electric field. The voltage applied across these materials should be precisely controlled to maintain desired properties, sometimes as high as 100's of volts. The materials are not conductive and represent a capacitive load.

The circuit of Figure 6 shows the LT1801 used in an amplifier capable of a 250V output swing and providing precise DC output voltage. When no signal is present, the op amp output sits at about mid-supply. Transistors Q1 and Q3 create bias voltages for Q2 and Q4, which are forced into a low quiescent current by degeneration resistors R4 and R5. When a transient signal arrives at V_{IN}, the op amp output moves and causes the current in Q2 or Q4 to change depending on the signal polarity. The current, limited by the clipping of the LT1801 output and the 3kΩ of total emitter degeneration, is mirrored to the output devices to drive the capacitive load. The LT1801 output then returns to near mid-supply, providing the precise DC output voltage to the load. The attention to limit the current of the output devices minimizes power dissipation thus allowing for dense layout, and inherits better reliability. Figure 7 shows the time domain response of the amplifier providing a 200V output swing into a 100pF load.

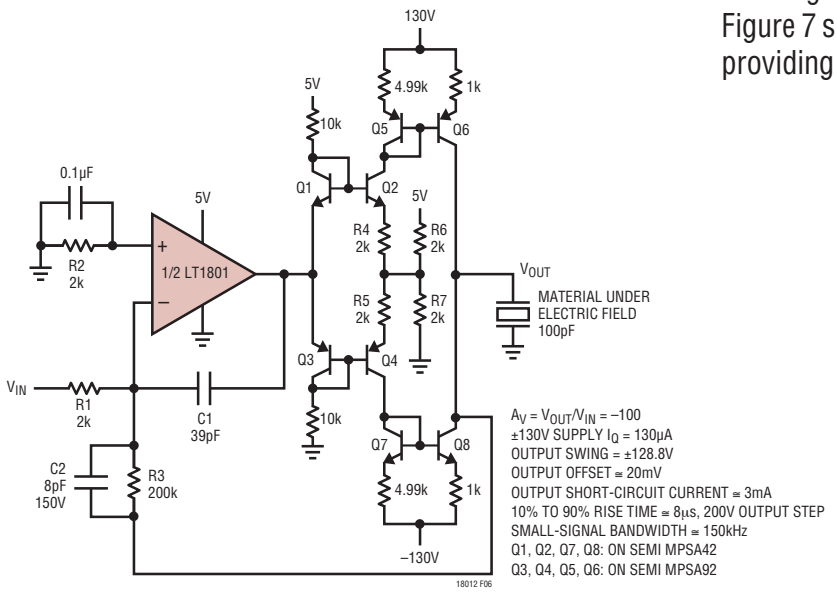


Figure 6. Low Power, High Voltage Amplifier

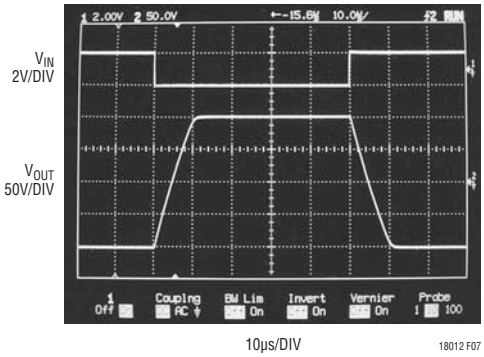


Figure 7. Large-Signal Time Domain Response of the Amplifier

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1399	Triple 300MHz Current Feedback Amplifier	0.1dB Gain Flatness to 150MHz, Shutdown
LT1498/LT1499	Dual/Quad 10MHz, 6V/µs Rail-to-Rail Input and Output C-Load™ Op Amps	High DC Accuracy, 475µV $V_{OS(MAX)}$, 4µV/°C Max Drift
LT1630/LT1631	Dual/Quad 30MHz, 10V/µs Rail-to-Rail Input and Output Op Amps	High DC Accuracy, 525µV $V_{OS(MAX)}$, 70mA Output Current, Max Supply Current 4.4mA per Amplifier
LT1800	80MHz, 25V/µs Low Power Rail-to-Rail Input/Output Precision Op Amp	Single Version of LT1801/LT1802
LT1806/LT1807	Single/Dual 325MHz, 140V/µs Rail-to-Rail Input and Output Op Amps	High DC Accuracy, 550µV $V_{OS(MAX)}$, Low Noise 3.5nV/√Hz, Low Distortion –80dB at 5MHz, Power-Down (LT1806)
LT1809/LT1810	Single/Dual 180MHz Rail-to-Rail Input/Output Op Amps	350V/µs Slew Rate, Low Distortion –90dBc at 5MHz, Power-Down (LT1809)

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