THE DATASHEET OF

LT1961EMS8E#PBF

1.5A, 1.25MHz Step-Up Switching Regulator

FEATURES

- **1.5A Switch in a Small MSOP Package**
- **Constant 1.25MHz Switching Frequency**
- **Wide Operating Voltage Range: 3V to 25V**
- **High Efficiency 0.2Ω Switch**
- **1.2V Feedback Reference Voltage**
- **±2% Overall Output Voltage Tolerance**
- Uses Low Profile Surface Mount External Components
- Low Shutdown Current: 6µA
- Synchronizable from 1.5MHz to 2MHz
- Current-Mode Loop Control
- Constant Maximum Switch Current Rating at All Duty Cycles*
- Thermally Enhanced Exposed Pad 8-Lead Plastic MSOP Package

APPLICATIONS

- DSL Modems
- Portable Computers
- Battery-Powered Systems
- Distributed Power

DESCRIPTION

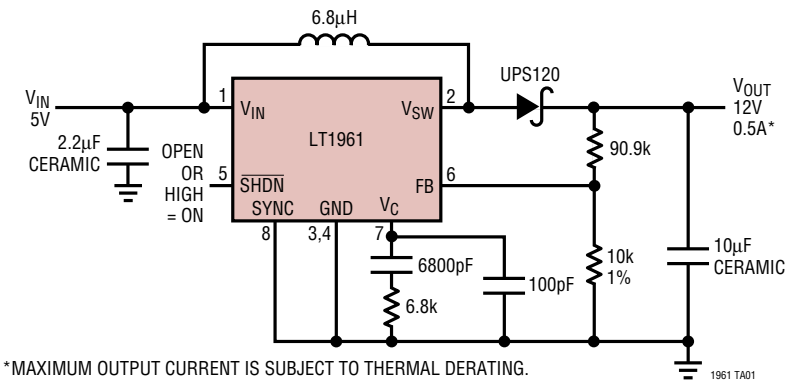
The LT®1961 is a 1.25MHz monolithic boost switching regulator. A high efficiency 1.5A, 0.2Ω switch is included on the die together with all the control circuitry required to complete a high frequency, current-mode switching regulator. Current-mode control provides fast transient response and excellent loop stability.

New design techniques achieve high efficiency at high switching frequencies over a wide operating voltage range. A low dropout internal regulator maintains consistent performance over a wide range of inputs from 24V systems to Li-Ion batteries. An operating supply current of 1mA maintains high efficiency, especially at lower output currents. Shutdown reduces quiescent current to 6µA. Maximum switch current remains constant at all duty cycles. Synchronization allows an external logic level signal to increase the internal oscillator from 1.5MHz to 2MHz.

The LT1961 is available in an exposed pad, 8-pin MSOP package. Full cycle-by-cycle switch current limit protection and thermal shutdown are provided. High frequency operation allows the reduction of input and output filtering components and permits the use of chip inductors.

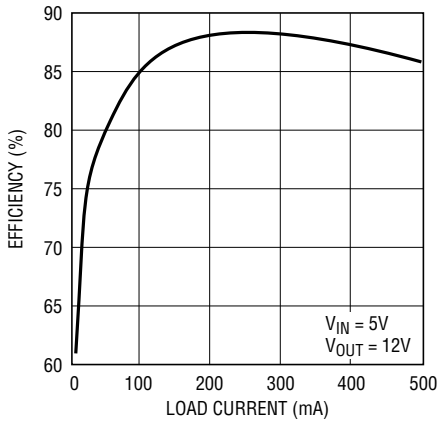
TYPICAL APPLICATION

5V to 12V Boost Converter



*MAXIMUM OUTPUT CURRENT IS SUBJECT TO THERMAL DERATING.

Efficiency vs Load Current

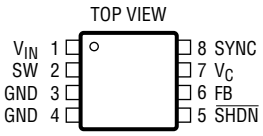


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Voltage 25V
Switch Voltage 35V
$\overline{SHDN}$ Pin 25V
FB Pin Current 1mA
SYNC Pin Current 1mA
Operating Junction Temperature Range (Note 2)
LT1961E, LT1961I ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



MS8E PACKAGE
8-LEAD PLASTIC MSOP

GROUND PAD CONNECTED
TO LARGE COPPER AREA

T_{JMAX} = 125°C, θ_{JA} = 50°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT1961EMS8E#PBF	LT1961EMS8E#TRPBF	LTQY	8-Lead Plastic MSOP	–40°C to 125°C
LT1961IMS8E#PBF	LT1961IMS8E#TRPBF	LTQY	8-Lead Plastic MSOP	–40°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LT1961EMS8E	LT1961EMS8E#TR	LTQY	8-Lead Plastic MSOP	–40°C to 125°C
LT1961IMS8E	LT1961IMS8E#TR	LTQY	8-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *Temperature grades are identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V, V_C = 0.8V, $\overline{SHDN}$, SYNC and switch open unless otherwise noted.

PARAMETER	CONDITION		MIN	TYP	MAX	UNITS
Recommended Operating Voltage		●	3		25	V
Maximum Switch Current Limit		●	1.5	2	3	A
Oscillator Frequency	3.3V < V_{IN} < 25V	●	1		1.5	MHz
Switch On Voltage Drop	I_{SW} = 1.5A	●		310	500	mV
V_{IN} Undervoltage Lockout	(Note 3)	●	2.47	2.6	2.73	V
V_{IN} Supply Current	I_{SW} = 0A	●		0.9	1.3	mA
V_{IN} Supply Current/I_{SW}	I_{SW} = 1.5A			27		mA/A
Shutdown Supply Current	$V_{\overline{SHDN}}$ = 0V, V_{IN} = 25V, V_{SW} = 25V	 ●		6	20 45	µA µA
Feedback Voltage	3V < V_{IN} < 25V, 0.4V < V_C < 0.9V	 ●	1.182 1.176	1.2	1.218 1.224	V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V, V_C = 0.8V, $\overline{SHDN}$, SYNC and switch open unless otherwise noted.

PARAMETER	CONDITION		MIN	TYP	MAX	UNITS
FB Input Current		●	0	–0.2	–0.4	µA
FB to V_C Voltage Gain	0.4V < V_C < 0.9V		150	350		
FB to V_C Transconductance	ΔI_{VC} = ±10µA	●	500	850	1300	µMho
V_C Pin Source Current	V_{FB} = 1V	●	–85	–120	–165	µA
V_C Pin Sink Current	V_{FB} = 1.4V	●	70	110	165	µA
V_C Pin to Switch Current Transconductance				2.4		A/V
V_C Pin Minimum Switching Threshold	Duty Cycle = 0%			0.3		V
V_C Pin 1.5A I_{SW} Threshold				0.9		V
Maximum Switch Duty Cycle	V_C = 1.2V, I_{SW} = 100mA V_C = 1.2V, I_{SW} = 1A, 25°C ≤ T_A ≤ 125°C V_C = 1.2V, I_{SW} = 1A, T_A ≤ 25°C	●	80 75 70	90 80 75		% % %
$\overline{SHDN}$ Threshold Voltage		●	1.28	1.35	1.42	V
$\overline{SHDN}$ Input Current (Shutting Down)	$\overline{SHDN}$ = 60mV Above Threshold	●	–7	–10	–13	µA
$\overline{SHDN}$ Threshold Current Hysteresis	$\overline{SHDN}$ = 100mV Below Threshold		4	7	10	µA
SYNC Threshold Voltage				1.5	2.2	V
SYNC Input Frequency			1.5		2	MHz
SYNC Pin Resistance	I_{SYNC} = 1mA			20		kΩ

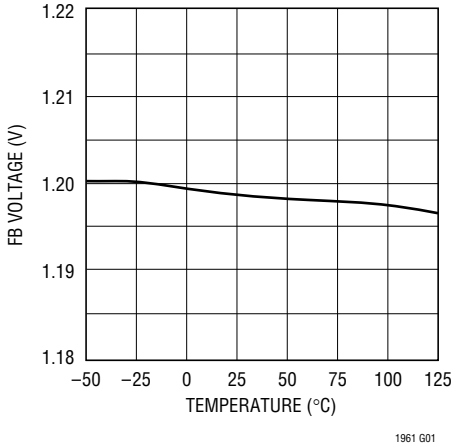
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT1961E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT1961I is guaranteed over the – 40ºC to 125ºC operating junction temperature range.

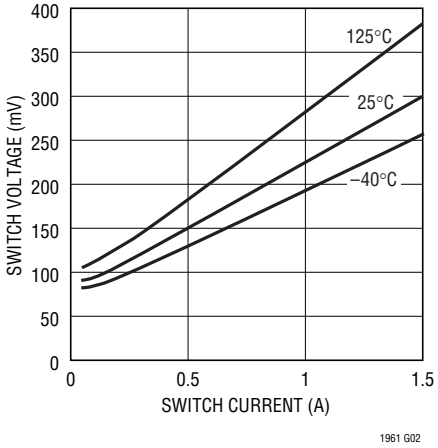
Note 3: Minimum input voltage is defined as the voltage where the internal regulator enters lockout. Actual minimum input voltage to maintain a regulated output will depend on output voltage and load current. See Applications Information.

TYPICAL PERFORMANCE CHARACTERISTICS

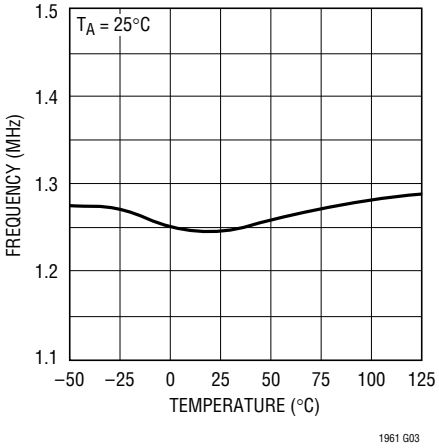
FB vs Temperature



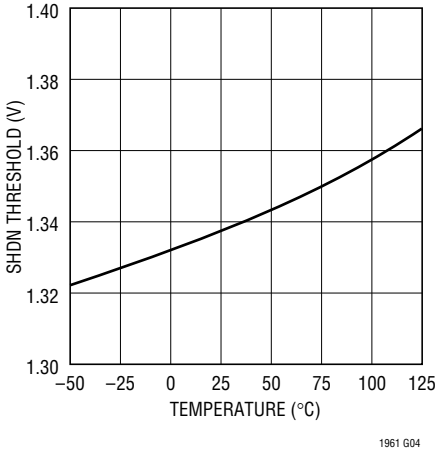
Switch On Voltage Drop



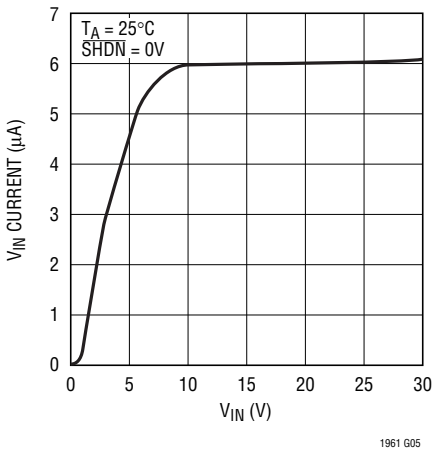
Oscillator Frequency



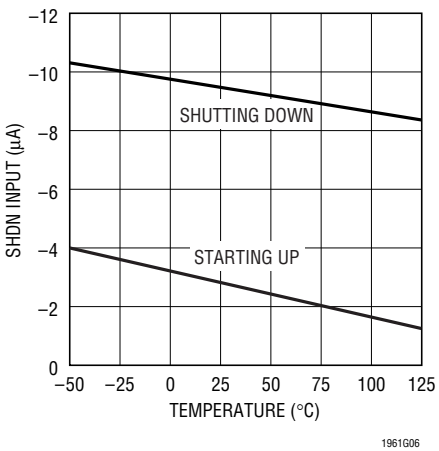
$\overline{SHDN}$ Threshold vs Temperature



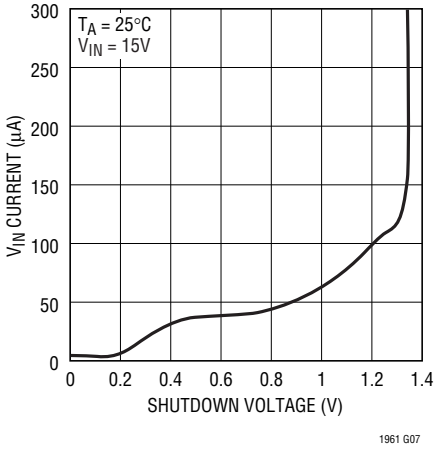
$\overline{SHDN}$ Supply Current vs V_{IN}



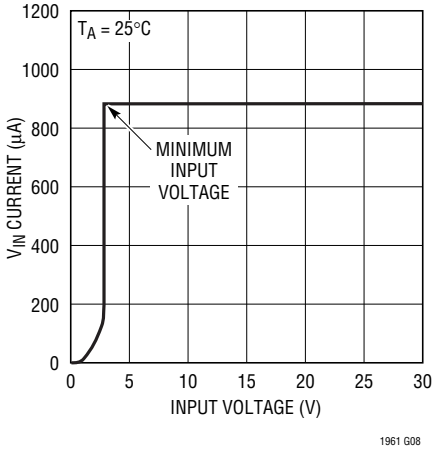
$\overline{SHDN}$ I_P Current vs Temperature



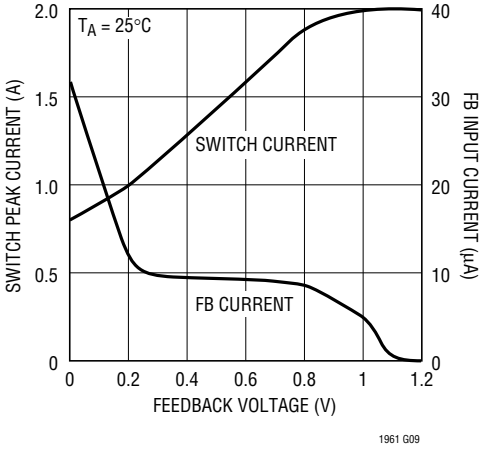
$\overline{SHDN}$ Supply Current



Input Supply Current



Current Limit Foldback



PIN FUNCTIONS

FB: The feedback pin is used to set output voltage using an external voltage divider that generates 1.2V at the pin with the desired output voltage. If required, the current limit can be reduced during start up when the FB pin is below 0.5V (see the Current Limit Foldback graph in the Typical Performance Characteristics section). An impedance of less than 5kΩ at the FB pin is needed for this feature to operate.

V_{IN}: This pin powers the internal circuitry and internal regulator. Keep the external bypass capacitor close to this pin.

GND: Short GND pins 3 and 4 and the exposed pad on the PCB. The GND is the reference for the regulated output, so load regulation will suffer if the "ground" end of the load is not at the same voltage as the GND of the IC. This condition occurs when the load current flows through the metal path between the GND pins and the load ground point. Keep the ground path short between the GND pins and the load and use a ground plane when possible. Keep the path between the input bypass and the GND pins short. The exposed pad should be attached to a large copper area to improve thermal resistance.

V_{SW}: The switch pin is the collector of the on-chip power NPN switch and has large currents flowing through it. Keep the traces to the switching components as short as possible to minimize radiation and voltage spikes.

SYNC: The sync pin is used to synchronize the internal oscillator to an external signal. It is directly logic compatible and can be driven with any signal between 20% and 80% duty cycle. The synchronizing range is equal to *initial* operating frequency, up to 2MHz. See Synchronization section in Applications Information for details. When not in use, this pin should be grounded.

$\overline{SHDN}$: The shutdown pin is used to turn off the regulator and to reduce input drain current to a few microamperes. The 1.35V threshold can function as an accurate undervoltage lockout (UVLO), preventing the regulator from operating until the input voltage has reached a predetermined level. Float or pull high to put the regulator in the operating mode.

V_C: The V_C pin is the output of the error amplifier and the input of the peak switch current comparator. It is normally used for frequency compensation, but can do double duty as a current clamp or control loop override. This pin sits at about 0.3V for very light loads and 0.9V at maximum load.

BLOCK DIAGRAM

The LT1961 is a constant frequency, current-mode boost converter. This means that there is an internal clock and two feedback loops that control the duty cycle of the power switch. In addition to the normal error amplifier, there is a current sense amplifier that monitors switch current on a cycle-by-cycle basis. A switch cycle starts with an oscillator pulse which sets the R_S flip-flop to turn the switch on. When switch current reaches a level set by the inverting input of the comparator, the flip-flop is reset and the switch turns off. Output voltage control is obtained by using the output of the error amplifier to set the switch current trip point. This technique means that the error amplifier commands current to be delivered to the output rather than voltage. A voltage fed system will have low phase shift up to the resonant frequency of the inductor and output capacitor, then an abrupt 180° shift will occur. The current fed system will have 90° phase shift at a much lower frequency, but will not have the additional 90° shift until well beyond the LC resonant frequency. This makes it much easier to frequency compensate the feedback loop and also gives much quicker transient response.

A comparator connected to the shutdown pin disables the internal regulator, reducing supply current.

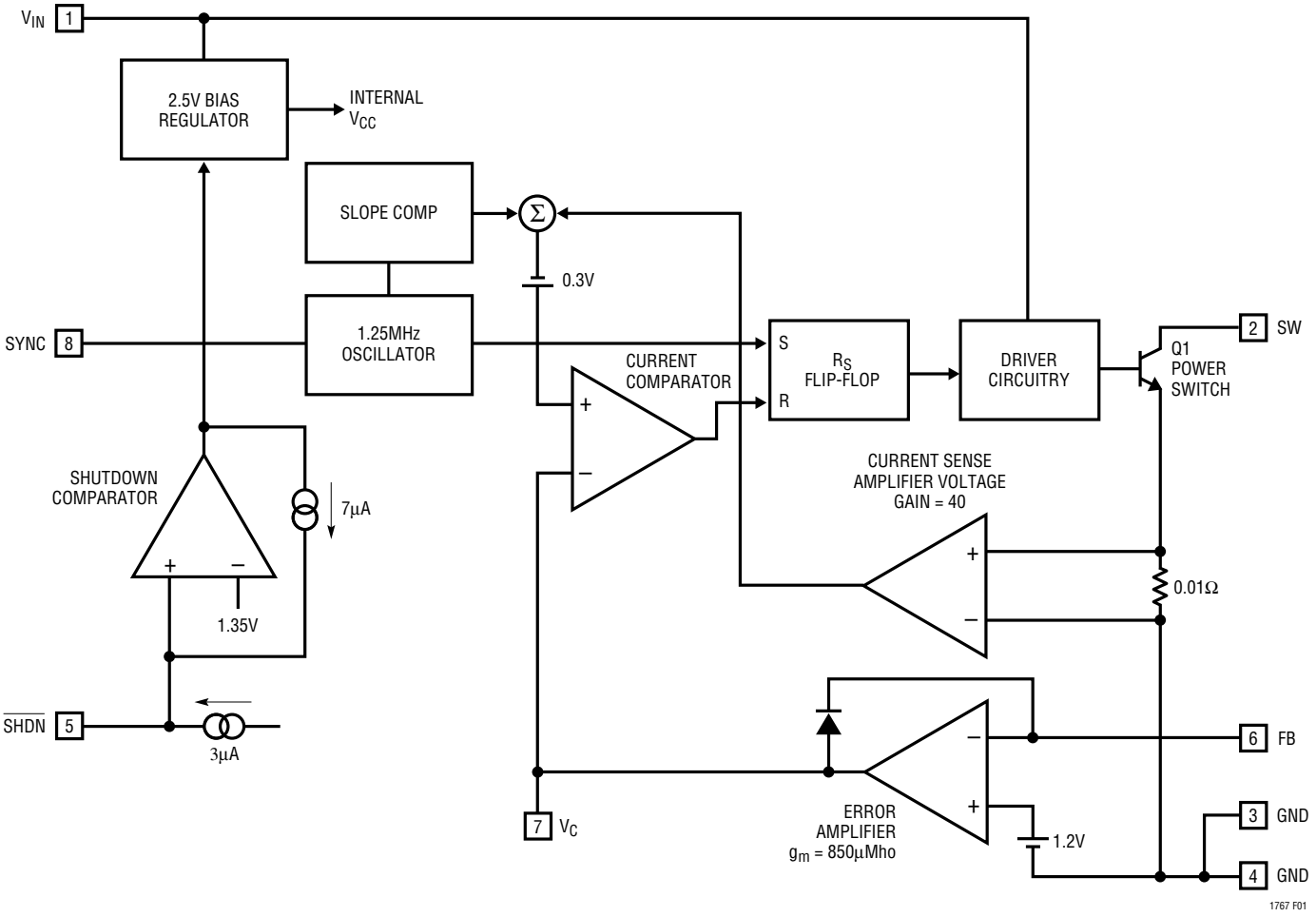


Figure 1. Block Diagram

APPLICATIONS INFORMATION

FB RESISTOR NETWORK

The suggested resistance (R2) from FB to ground is 10k 1%. This reduces the contribution of FB input bias current to output voltage to less than 0.2%. The formula for the resistor (R1) from V_{OUT} to FB is:

$$R1 = \frac{R2\left(V_{OUT} - 1.2\right)}{1.2 - R2(0.2\mu A)}$$

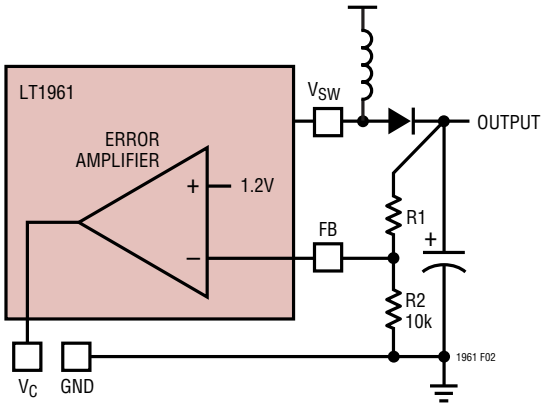


Figure 2. Feedback Network

OUTPUT CAPACITOR

Step-up regulators supply current to the output in pulses. The rise and fall times of these pulses are very fast. The output capacitor is required to reduce the voltage ripple this causes. The RMS ripple current can be calculated from:

$$I_{RIPPLE(RMS)} = I_{OUT}\sqrt{\left(V_{OUT} - V_{IN}\right)/V_{IN}}$$

The LT1961 will operate with both ceramic and tantalum output capacitors. Ceramic capacitors are generally chosen for their small size, very low ESR (effective series resistance), and good high frequency operation, reducing output ripple voltage. Their low ESR removes a useful zero in the loop frequency response, common to tantalum capacitors. To compensate for this, the V_C loop compensation pole frequency must typically be reduced by a factor of 10. Typical ceramic output capacitors are in the 1µF to 10µF range. Since the absolute value of capacitance defines the pole frequency of the output stage, an X7R or X5R type ceramic, which have good temperature stability, is recommended.

Tantalum capacitors are usually chosen for their bulk capacitance properties, useful in high transient load applications. ESR rather than absolute value defines output ripple at 1.25MHz. Values in the 22µF to 100µF range are generally needed to minimize ESR and meet ripple current ratings. Care should be taken to ensure the ripple ratings are not exceeded.

Table 1. Surface Mount Solid Tantalum Capacitor ESR and Ripple Current

E Case Size	ESR (Max, Ω)	Ripple Current (A)
AVX TPS, Sprague 593D	0.1 to 0.3	0.7 to 1.1
AVX TAJ	0.7 to 0.9	0.4
D Case Size		
AVX TPS, Sprague 593D	0.1 to 0.3	0.7 to 1.1
C Case Size		
AVX TPS	0.2 (typ)	0.5 (typ)

INPUT CAPACITOR

Unlike the output capacitor, RMS ripple current in the input capacitor is normally low enough that ripple current rating is not an issue. The current waveform is triangular, with an RMS value given by:

$$I_{RIPPLE(RMS)} = \frac{0.29\left(V_{IN}\right)\left(V_{OUT} - V_{IN}\right)}{\left(L\right)\left(f\right)\left(V_{OUT}\right)}$$

At higher switching frequency, the energy storage requirement of the input capacitor is reduced so values in the range of 1µF to 4.7µF are suitable for most applications. Y5V or similar type ceramics can be used since the absolute value of capacitance is less important and has no significant effect on loop stability. If operation is required close to the minimum input voltage required by either the output or the LT1961, a larger value may be necessary. This is to prevent excessive ripple causing dips below the minimum operating voltage resulting in erratic operation.

APPLICATIONS INFORMATION

INDUCTOR CHOICE AND MAXIMUM OUTPUT CURRENT

When choosing an inductor, there are 2 conditions that limit the minimum inductance; required output current, and avoidance of subharmonic oscillation. The maximum output current for the LT1961 in a standard boost converter configuration with an infinitely large inductor is:

$$I_{OUT(MAX)} = 1.5A\frac{V_{IN} \bullet \eta}{V_{OUT}}$$

Where η = converter efficiency (typically 0.87 at high current).

As the value of inductance is reduced, ripple current increases and $I_{OUT(MAX)}$ is reduced. The minimum inductance for a required output current is given by:

$$L_{MIN} = \frac{V_{IN}(V_{OUT} - V_{IN})}{2V_{OUT}(f)\left(1.5 - \frac{(V_{OUT})(I_{OUT})}{V_{IN} \bullet \eta}\right)}$$

The second condition, avoidance of subharmonic oscillation, must be met if the operating duty cycle is greater than 50%. The slope compensation circuit within the LT1961 prevents subharmonic oscillation for inductor ripple currents of up to $0.7A_{P-P}$, defining the minimum inductor value to be:

$$L_{MIN} = \frac{V_{IN}(V_{OUT} - V_{IN})}{0.7V_{OUT}(f)}$$

These conditions define the absolute minimum inductance. However, it is generally recommended that to prevent excessive output noise, and difficulty in obtaining stability, the ripple current is no more than 40% of the average inductor current. Since inductor ripple is:

$$I_{P-P\ RIPPLE} = \frac{V_{IN}(V_{OUT} - V_{IN})}{V_{OUT}(L)(f)}$$

The recommended minimum inductance is:

$$L_{MIN} = \frac{(V_{IN})^2(V_{OUT} - V_{IN})}{0.4(V_{OUT})^2(I_{OUT})(f)}$$

The inductor value may need further adjustment for other factors such as output voltage ripple and filtering requirements. Remember also, inductance can drop significantly with DC current and manufacturing tolerance.

The inductor must have a rating greater than its peak operating current to prevent saturation resulting in efficiency loss. Peak inductor current is given by:

$$I_{LPEAK} = \frac{(V_{OUT})(I_{OUT})}{V_{IN} \bullet \eta} + \frac{V_{IN}(V_{OUT} - V_{IN})}{2V_{OUT}(L)(f)}$$

Also, consideration should be given to the DC resistance of the inductor. Inductor resistance contributes directly to the efficiency losses in the overall converter.

Suitable inductors are available from Coilcraft, Coiltronics, Dale, Sumida, Toko, Murata, Panasonic and other manufactures.

Table 2

PART NUMBER	VALUE (uH)	$I_{SAT(DC)}$ (Amps)	DCR (Ω)	HEIGHT (mm)
Coiltronics				
TP1-2R2	2.2	1.3	0.188	1.8
TP2-2R2	2.2	1.5	0.111	2.2
TP3-4R7	4.7	1.5	0.181	2.2
TP4- 100	10	1.5	0.146	3.0
Murata				
LQH1C1R0M04	1.0	0.51	0.28	1.8
LQH3C1R0M24	1.0	1.0	0.06	2.0
LQH3C2R2M24	2.2	0.79	0.1	2.0
LQH4C1R5M04	1.5	1	0.09	2.6
Sumida				
CD73- 100	10	1.44	0.080	3.5
CDRH4D18-2R2	2.2	1.32	0.058	1.8
CDRH5D18-6R2	6.2	1.4	0.071	1.8
CDRH5D28-100	10	1.3	0.048	2.8
Coilcraft				
1008PS-272M	2.7	1.3	0.14	2.7
LPO1704-222M	2.2	1.6	0.12	1.0
LPO1704-332M	3.3	1.3	0.16	1.0

APPLICATIONS INFORMATION

CATCH DIODE

The suggested catch diode (D1) is a UPS120 or 1N5818 Schottky. It is rated at 1A average forward current and 20V/30V reverse voltage. Typical forward voltage is 0.5V at 1A. The diode conducts current only during switch off time. Peak reverse voltage is equal to regulator output voltage. Average forward current in normal operation is equal to output current.

SHUTDOWN AND UNDERVOLTAGE LOCKOUT

Figure 4 shows how to add undervoltage lockout (UVLO) to the LT1961. Typically, UVLO is used in situations where the input supply is *current limited*, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. UVLO prevents the regulator from operating at source voltages where these problems might occur.

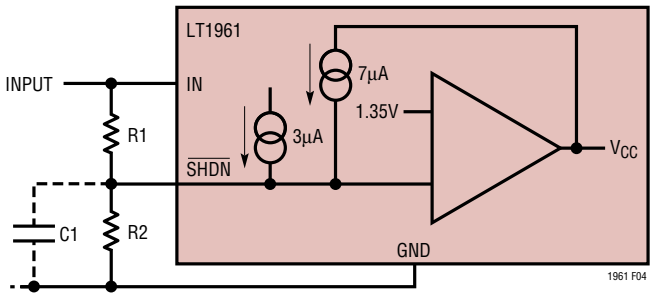


Figure 4. Undervoltage Lockout

An internal comparator will force the part into shutdown below the minimum V_{IN} of 2.6V. This feature can be used to prevent excessive discharge of battery-operated systems. If an adjustable UVLO threshold is required, the shutdown pin can be used. The threshold voltage of the shutdown pin comparator is 1.35V. A 3µA internal current source defaults the open pin condition to be operating (see Typical Performance Graphs). Current hysteresis is added above the SHDN threshold. This can be used to set voltage hysteresis of the UVLO using the following:

$$R1 = \frac{V_H - V_L}{7\mu A}$$

$$R2 = \frac{1.35V}{\frac{\left(V_H - 1.35V\right)}{R1} + 3\mu A}$$

V_H – Turn-on threshold

V_L – Turn-off threshold

Example: switching should not start until the input is above 4.75V and is to stop if the input falls below 3.75V.

V_H = 4.75V

V_L = 3.75V

$$R1 = \frac{4.75V - 3.75V}{7\mu A} = 143k$$

$$R2 = \frac{1.35V}{\frac{\left(4.75V - 1.35V\right)}{143k} + 3\mu A} = 50.4k$$

Keep the connections from the resistors to the $\overline{SHDN}$ pin short and make sure that the interplane or surface capacitance to the switching nodes are minimized. If high resistor values are used, the $\overline{SHDN}$ pin should be bypassed with a 1nF capacitor to prevent coupling problems from the switch node.

APPLICATIONS INFORMATION

SYNCHRONIZATION

The SYNC pin, is used to synchronize the internal oscillator to an external signal. The SYNC input must pass from a logic level low, through the maximum synchronization threshold with a duty cycle between 20% and 80%. The input can be driven directly from a logic level output. The synchronizing range is equal to *initial* operating frequency up to 2MHz. This means that *minimum* practical sync frequency is equal to the worst-case *high* self-oscillating frequency (1.5MHz), not the typical operating frequency of 1.25MHz. Caution should be used when synchronizing above 1.7MHz because at higher sync frequencies the amplitude of the internal slope compensation used to prevent subharmonic switching is reduced. Higher inductor values will tend to eliminate this problem. See Frequency Compensation section for a discussion of an entirely different cause of subharmonic switching before assuming that the cause is insufficient slope compensation. Application Note 19 has more details on the theory of slope compensation.

LAYOUT CONSIDERATIONS

As with all high frequency switchers, when considering layout, care must be taken to achieve optimal electrical, thermal and noise performance. For maximum efficiency, switch rise and fall times are typically in the nanosecond range. To prevent noise both radiated and conducted, the high speed switching current path, shown in Figure 5, must be kept as short as possible. This is implemented in the suggested layout of Figure 6. Shortening this path will also reduce the parasitic trace inductance of approximately 25nH/inch. At switch off, this parasitic inductance produces a flyback spike across the LT1961 switch. When operating at higher currents and output voltages, with poor layout, this spike can generate voltages across the LT1961 that may exceed its absolute maximum rating. A ground plane should always be used under the switcher circuitry to prevent interplane coupling and overall noise.

The V_C and FB components should be kept as far away as possible from the switch node. The LT1961 pinout has been designed to aid in this. The ground for these components should be separated from the switch current path. Failure to do so will result in poor stability or subharmonic like oscillation.

Board layout also has a significant effect on thermal resistance. The exposed pad is the copper plate that runs under the LT1961 die. This is the best thermal path for heat out of the package. Soldering the pad onto the board will reduce die temperature and increase the power capability of the LT1961. Provide as much copper area as possible around this pad. Adding multiple solder filled feedthroughs under and around the pad to the ground plane will also help. Similar treatment to the catch diode and inductor terminations will reduce any additional heating effects.

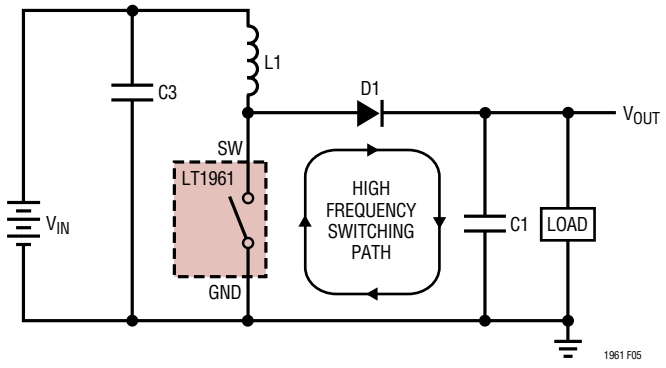
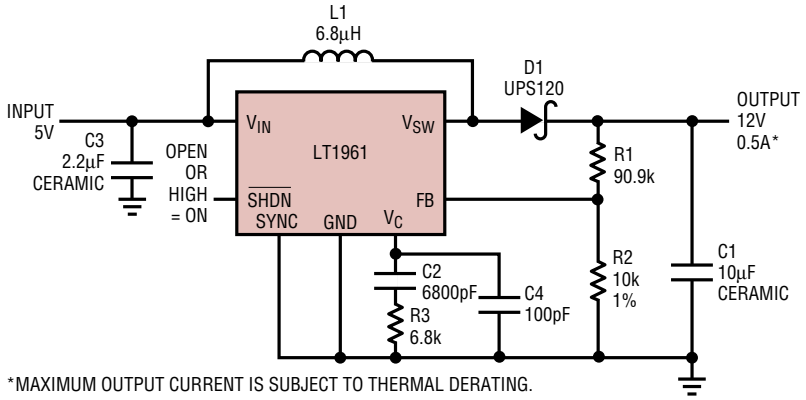


Figure 5. High Speed Switching Path

APPLICATIONS INFORMATION



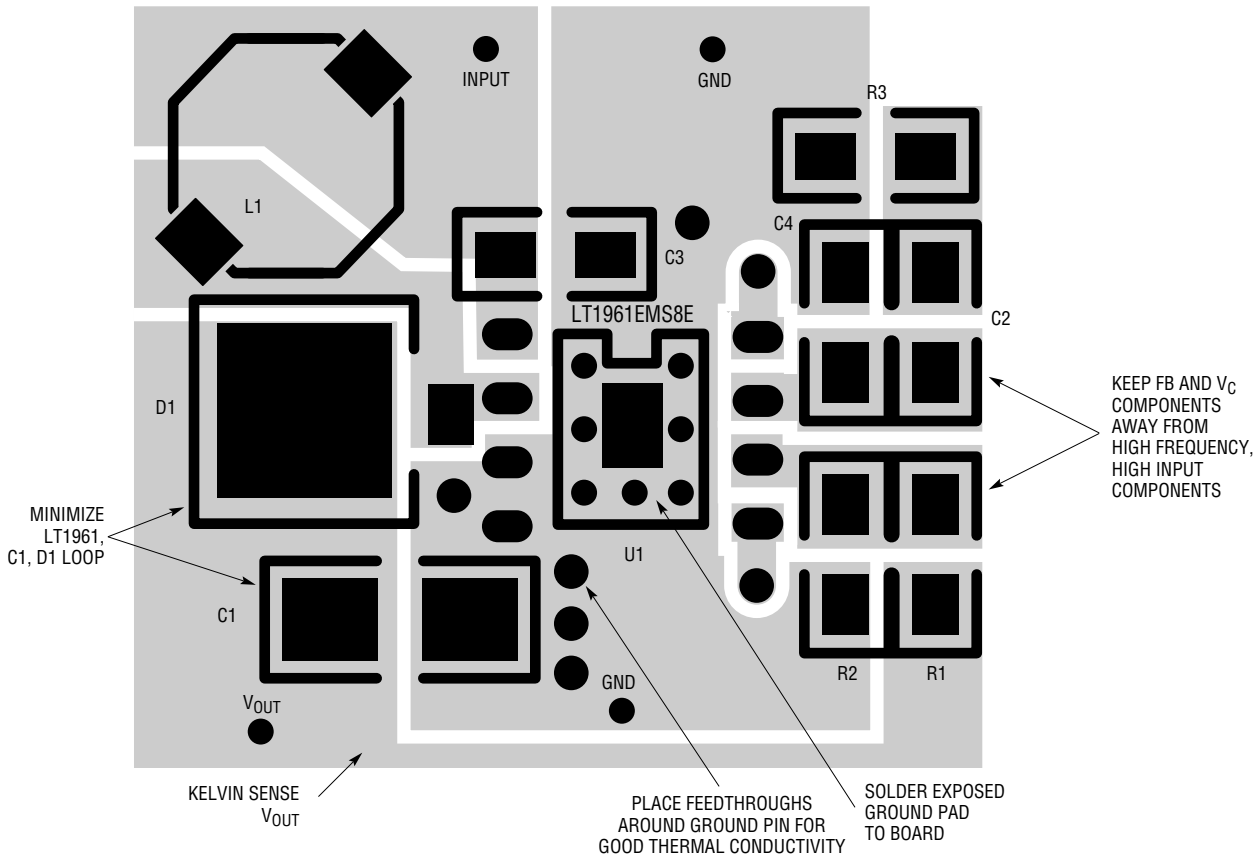


Figure 6. Typical Application and Suggested Layout (Topside Only Shown)

APPLICATIONS INFORMATION

THERMAL CALCULATIONS

Power dissipation in the LT1961 chip comes from four sources: switch DC loss, switch AC loss, drive current, and input quiescent current. The following formulas show how to calculate each of these losses. These formulas assume continuous mode operation, so they should not be used for calculating efficiency at light load currents.

$$\text{DC, duty cycle} = \frac{(V_{OUT} - V_{IN})}{V_{OUT}}$$

$$I_{SW} = \frac{(V_{OUT})(I_{OUT})}{V_{IN}}$$

Switch loss:

$$P_{SW} = (DC)(I_{SW})^2(R_{SW}) + 17n\left(I_{SW}\right)\left(V_{OUT}\right)\left(f\right)$$

V_{IN} loss:

$$P_{VIN} = \frac{(V_{IN})(I_{SW})(DC)}{50} + 1mA(V_{IN})$$

R_{SW} = Switch resistance ($\approx$0.27Ω hot)

Example: V_{IN} = 5V, V_{OUT} = 12V and I_{OUT} = 0.5A

Total power dissipation = 0.23 + 0.31 + 0.07 + 0.005 = 0.62W

Thermal resistance for LT1961 package is influenced by the presence of internal or backside planes. With a full plane under the package, thermal resistance will be about 50°C/W. To calculate die temperature, use the appropriate thermal resistance number and add in worst-case ambient temperature:

$$T_J = T_A + \theta_{JA}\,(P_{TOT})$$

If a true die temperature is required, a measurement of the SYNC to GND pin resistance can be used. The SYNC pin resistance across temperature must first be calibrated, with no device power, in an oven. The same measurement can then be used in operation to indicate the die temperature.

FREQUENCY COMPENSATION

Loop frequency compensation is performed on the output of the error amplifier (V_C pin) with a series RC network. The main pole is formed by the series capacitor and the output impedance ($\approx$500kΩ) of the error amplifier. The pole falls in the range of 2Hz to 20Hz. The series resistor creates a "zero" at 1kHz to 5kHz, which improves loop stability and transient response. A second capacitor, typically one-tenth the size of the main compensation capacitor, is sometimes used to reduce the switching frequency ripple on the V_C pin. V_C pin ripple is caused by output voltage ripple attenuated by the output divider and multiplied by the error amplifier. Without the second capacitor, V_C pin ripple is:

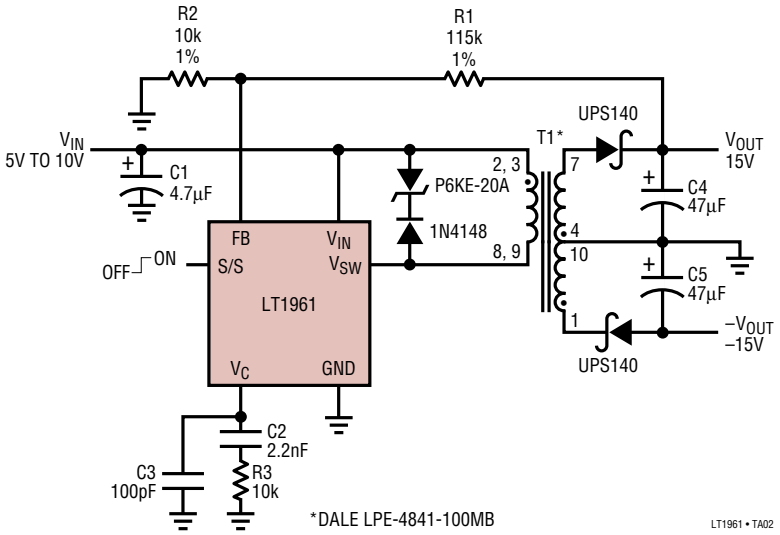
$$V_C \text{ Pin Ripple} = \frac{1.2(V_{RIPPLE})(g_m)(R_C)}{(V_{OUT})}$$

V_{RIPPLE} = Output ripple (V_{P-P})
g_m = Error amplifier transconductance ($\approx$850μmho)
R_C = Series resistor on V_C pin
V_{OUT} = DC output voltage

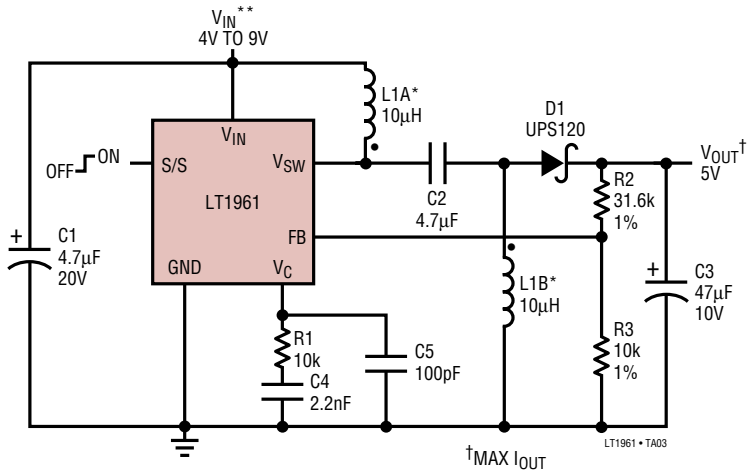
To prevent irregular switching, V_C pin ripple should be kept below 50mV_{P-P}. Worst-case V_C pin ripple occurs at maximum output load current and will also be increased if poor quality (high ESR) output capacitors are used. The addition of a 47pF capacitor on the V_C pin reduces switching frequency ripple to only a few millivolts. A low value for R_C will also reduce V_C pin ripple, but loop phase margin may be inadequate.

TYPICAL APPLICATIONS

Dual Output Flyback Converter



4V-9V_{IN} to 5V_{OUT} SEPIC Converter**



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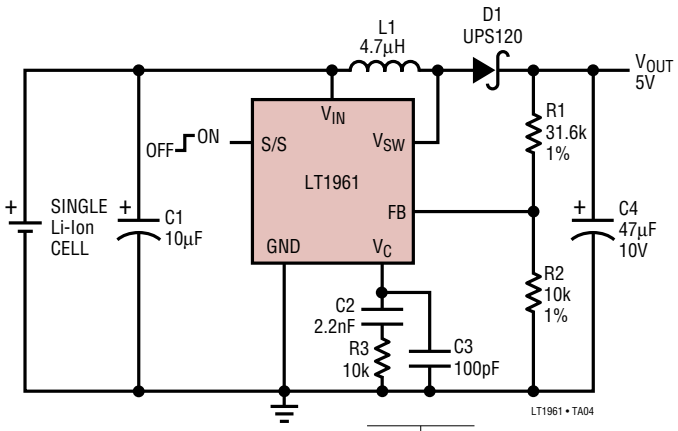
** INPUT VOLTAGE MAY BE GREATER OR LESS THAN OUTPUT VOLTAGE

†MAX I_{OUT}

I_{OUT}	V_{IN}
0.59A	4V
0.65A	5V
0.70A	6V
0.74A	7V
0.80A	9V

TYPICAL APPLICATIONS

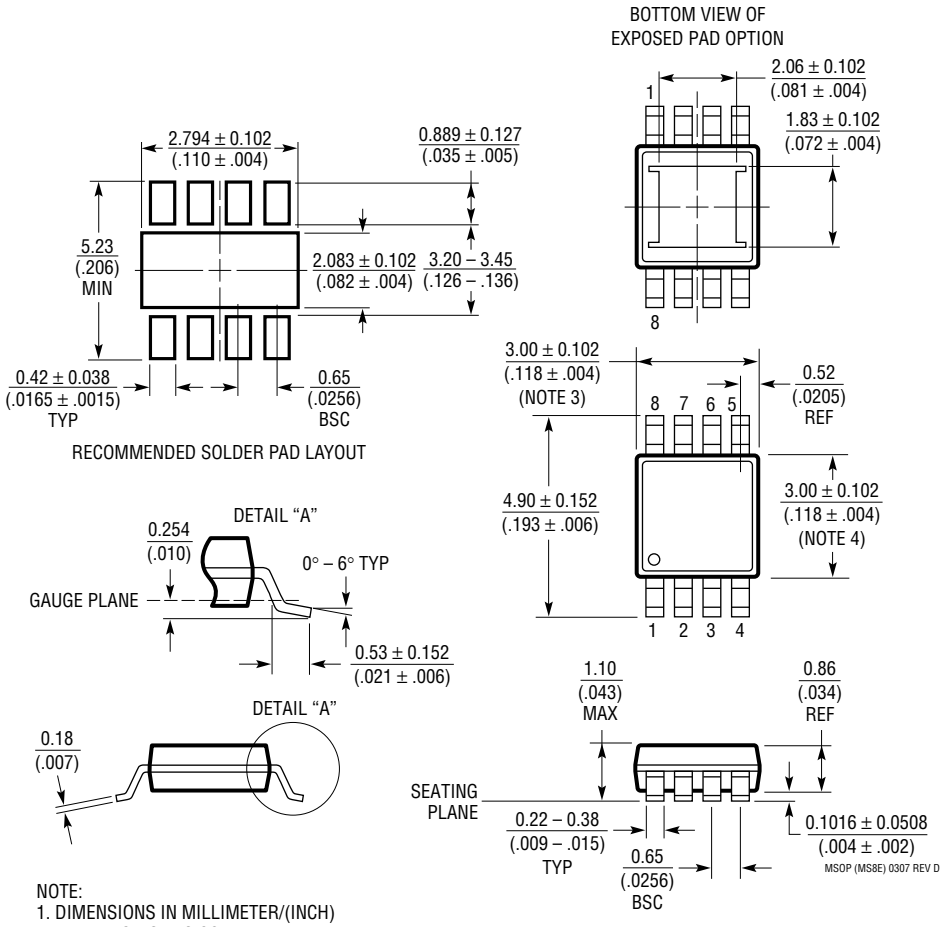
Single Li-Ion Cell to 5V



I_{OUT}	V_{IN}
0.75A	2.7V
0.93A	3.3V
1.0A	3.6V

PACKAGE DESCRIPTION

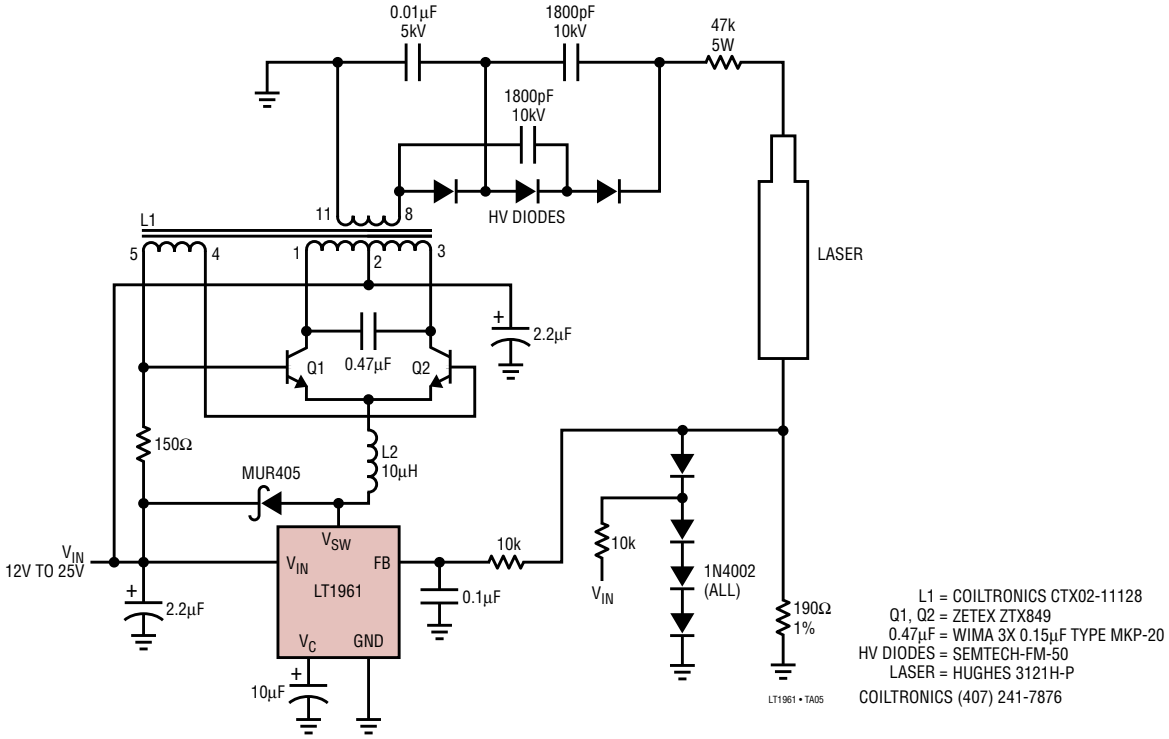
MS8E Package
8-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1662 Rev D)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

High Voltage Laser Power Supply



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1308A	600kHz, 2A, Step-Up Regulator	30V Switch, V_{IN} = 1V to 6V, Low Battery Comparator, S8 Package
LT1310	4.5MHz, 1.5A Step-Up with Phase Lock Loop	34V Switch, V_{IN} = 2.75V to 18V, V_{OUT} up to 35V, MS10E Package
LT1370	High Efficiency DC/DC Converter	42V Switch, 6A, 500kHz Switch, DD-Pak, TO-220 Package
LT1371	High Efficiency DC/DC Converter	35V Switch, 3A, 500kHz Switch, DD-Pak, TO-220 Package
LT1372/LT1377	500kHz and 1MHz High Efficiency 1.5A Switching Regulators	Boost Topology, $V_{IN(MIN)}$ = 2.7V, S8 Package
LT1946/LT1946A	1.2MHz/2.7MHz, 1.5A, Monolithic Step-Up Regulator	V_{IN} = 2.6V to 16V, V_{OUT} up to 34V, Integrated SS, MS8 Package
LTC3400/ LTC3400B	1.2MHz, 600mA, Synchronous Step-Up	V_{IN} = 0.85V to 5V, V_{OUT} to 5.5V, Up to 95% Efficiency, ThinSOT Package
LTC3401	Single Cell, High Current (1A), Micropower, Synchronous 3MHz Step-Up DC/DC Converter	V_{IN} = 0.85V to 5V, V_{OUT} to 5.5V, Up to 97% Efficiency Synchronizable, Oscillator from 100kHz to 3MHz, MS10 Package
LTC3402	Single Cell, High Current (2A), Micropower, Synchronous 3MHz Step-Up DC/DC Converter	V_{IN} = 0.85V to 5V, V_{OUT} to 5.5V, Up to 95% Efficiency Synchronizable, Oscillator from 100kHz to 3MHz, MS10 Package
LTC3405/ LTC3405A	1.5MHz High Efficiency, I_{OUT} = 300mA, Monolithic Synchronous Step-Down Regulator	V_{IN} = 2.5V to 5.5V, V_{OUT} to 0.8V, Up to 95% Efficiency, 100% Duty Cycle, I_Q = 20µA, ThinSOT Package

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