THE DATASHEET OF

LTC1149CS-5#TRPBF

High Efficiency Synchronous Step-Down Switching Regulators

FEATURES

- **Operation to 48V Input Voltage**
- **Ultrahigh Efficiency: Up to 95%**
- **Current Mode Operation for Excellent Line and Load Transient Response**
- High Efficiency Maintained over Wide Current Range
- Logic-Controlled Micropower Shutdown
- Short-Circuit Protection
- Very Low Dropout Operation: 100% Duty Cycle
- Synchronous FET Switching for High Efficiency
- Adaptive Nonoverlap Gate Drives
- Available in 16-Pin Narrow SO Package

APPLICATIONS

- Notebook and Palmtop Computers
- Portable Instruments
- Battery-Operated Digital Devices
- Industrial Power Distribution
- Avionics Systems
- Telecom Power Supplies

DESCRIPTION

The LTC®1149 series is a family of synchronous step-down switching regulator controllers featuring automatic Burst Mode™ operation to maintain high efficiencies at low output currents. These devices drive external complementary power MOSFETs at switching frequencies up to 250kHz using a constant off-time current-mode architecture.

Special onboard regulation and level-shift circuitry allow operation at input voltages from dropout to 48V (60V absolute max). The constant off-time architecture maintains constant ripple current in the inductor, easing the design of wide input range converters. Current mode operation provides excellent line and load transient response. The operating current level is user-programmable via an external current sense resistor.

The LTC1149 series incorporates automatic power saving Burst Mode operation when load currents drop below the level required for continuous operation. Standby power is reduced to only about 8mW at V_{IN} = 12V. In shutdown, both MOSFETs are turned off.

TYPICAL APPLICATION

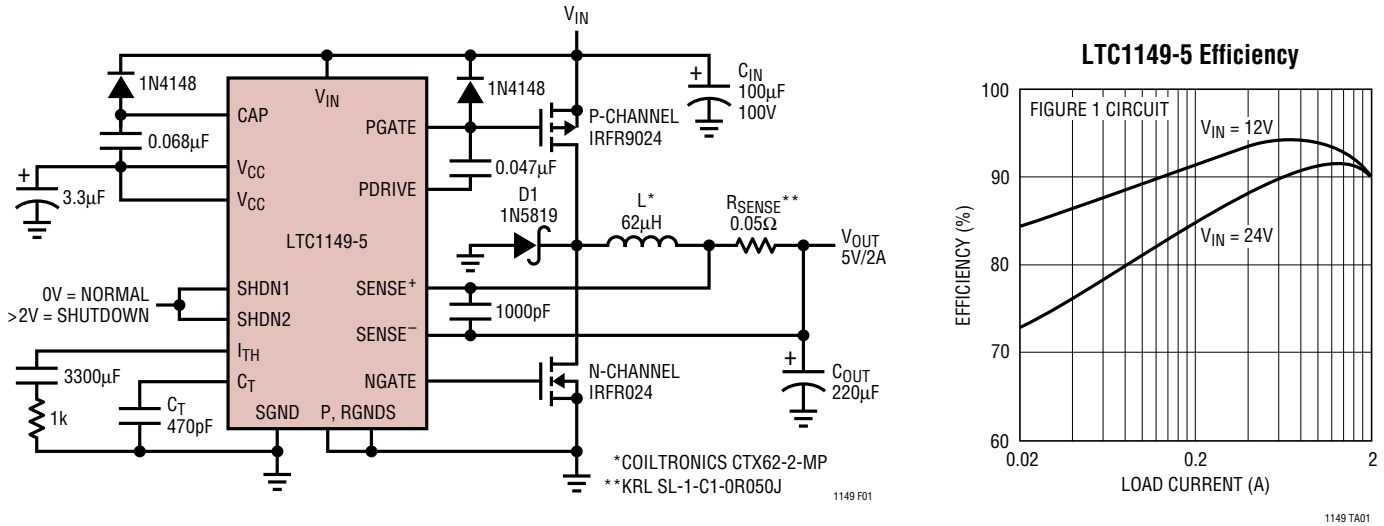
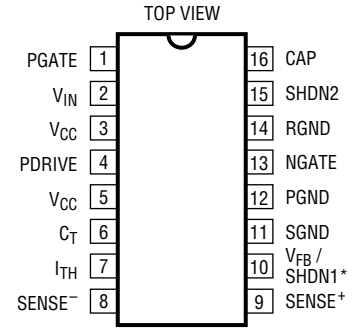


Figure 1. High Efficiency Step-Down Regulator

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (Pin 2) ..... –15V to 60V
V_{CC} Output Current (Pin 3) 50mA
V_{CC} Input Voltage (Pin 5) 16V
Continuous Output Current (Pins 4, 13) 50mA
Sense Voltages (Pins 8, 9)
  $V_{IN} \geq 12.7V$ ..... 13V to –0.3V
  $V_{IN} < 12.7V$ ..... (V_{CC} + 0.3V) to –0.3V
Shutdown Voltages (Pins 10, 15) 7V
Operating Temperature Range ..... 0°C to 70°C
Extended Commercial
Temperature Range ..... –40°C to 85°C
Junction Temperature (Note 1) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE 16-LEAD PDIP
S PACKAGE 16-LEAD PLASTIC SO

*FIXED OUTPUT VERSIONS

T_{JMAX} = 125°C, θ_{JA} = 70°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 110°C/W (S)

ORDER PART NUMBER

LTC1149CN
LTC1149CN-3.3
LTC1149CN-5
LTC1149CS
LTC1149CS-3.3
LTC1149CS-5

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, V_{10} = 0V (Note 2), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{10}	Feedback Voltage (LTC1149 Only)	V_{IN} = 9V	●	1.21	1.25	1.29	V
I_{10}	Feedback Current (LTC1149 Only)		●		0.2	1	µA
V_{OUT}	Regulated Output Voltage V_{IN} = 9V LTC1149-3.3 I_{LOAD} = 700mA LTC1149-5 I_{LOAD} = 700mA		 ● ●	 3.23 4.9	 3.33 5.05	 3.43 5.2	 V V
ΔV_{OUT}	Output Voltage Line Regulation	V_{IN} = 9V to 48V, I_{LOAD} = 50mA		–40	0	40	mV
	Output Voltage Load Regulation LTC1149-3.3 LTC1149-5	 5mA < I_{LOAD} < 2A 5mA < I_{LOAD} < 2A	 ● ●		 40 60	 65 100	 mV mV
	Burst Mode Output Ripple	I_{LOAD} = 0A			50		mV_{P-P}
I_2	Input DC Supply Current (Note 3) Normal Mode Burst Mode Shutdown	 V_{IN} = 12V V_{IN} = 48V V_{IN} = 12V V_{IN} = 48V V_{IN} = 12V, V_{15} = 2V V_{IN} = 48V, V_{15} = 2V			 2.0 2.2 0.6 0.8 135 300	 2.8 3.0 0.9 1.1 170 390	 mA mA mA mA µA µA
V_{CC}	Internal Regulator Voltage (Sets MOSFET Gate Drive Levels)	V_{IN} = 12V to 48V I_3 = 20mA	●	9.75	10.25	11	V
$V_2 – V_3$	V_{CC} Dropout Voltage	V_{IN} = 5V, I_3 = 10mA			200	250	mV
$V_{IN} – V_1$	P-Gate to Source Voltage (Off)	V_{IN} = 12V V_{IN} = 48V	● ●	–0.2 –0.2	0 0		V V

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, V_{10} = 0V (Note 2), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_9 - V_8$	Current Sense Threshold Voltage LTC1149	 V_8 = 5V, V_{10} = 1.32V (Forced) $V_8 = V_{OUT} - 100mV$	 ●	 130	 25 150	 170	 mV mV
	LTC1149-3.3	V_8 = 3.5V (Forced) $V_8 = V_{OUT} - 100mV$	 ●	 130	 25 150	 170	 mV mV
	LTC1149-5	V_8 = 5.3V (Forced) $V_8 = V_{OUT} - 100mV$	 ●	 130	 25 150	 170	 mV mV
V_{10}	Shutdown 1 Threshold LTC1149-3.3, LTC1149-5			 0.5	 0.8	 2	 V
V_{15}	Shutdown 2 Threshold			0.8	1.4	2	V
I_{15}	Shutdown 2 Input Current	V_{15} = 5V			18	25	µA
I_6	C_T Pin Discharge Current	V_{OUT} In Regulation, V_{SENSE}^- = V_{OUT} V_{OUT} = 0V		50	70 2	90 10	µA µA
t_{OFF}	Off-Time (Note 4)	C_T = 390pF, I_{LOAD} = 700mA		4	5	6	µs
t_r, t_f	Driver Output Transition Times	C_L = 3000pF (Pins 4, 13), V_{IN} = 6V			100	200	ns

–40°C ≤ T_A ≤ 85°C (Note 5), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{10}	Feedback Voltage LTC1149 Only			1.2	1.25	1.3	V
V_{OUT}	Regulated Output Voltage LTC1149-3.3 LTC1149-5	V_{IN} = 9V I_{LOAD} = 700mA I_{LOAD} = 700mA		 3.17 4.85	 3.33 5.05	 3.43 5.2	 V V
I_2	Input DC Supply Current (Note 3) Normal Mode	 V_{IN} = 12V V_{IN} = 48V		 	 2.0 2.2	 3.2 3.5	 mA mA
	Burst Mode	V_{IN} = 12V V_{IN} = 48V			0.6 0.8	1.05 1.30	mA mA
	Shutdown	V_{IN} = 12V, V_{15} = 2V V_{IN} = 48V, V_{15} = 2V			135 300	230 520	µA µA
V_{CC}	Internal Regulator Voltage (Sets MOSFET Gate Drive Levels)	V_{IN} = 12V to 48V I_3 = 20mA		9.75	10.25	11	V
$V_9 - V_8$	Current Sense Threshold Voltage	Low Threshold (Forced) High Threshold (Forced)		 125	 25 150	 175	 mV mV
V_{15}	Shutdown 2 Threshold			0.8	1.4	2	V
t_{OFF}	Off-Time (Note 4)	C_T = 390pF, I_{LOAD} = 700mA, V_{IN} = 10V		3.8	5	6	µs

The ● denotes specifications which apply over the full operating temperature range.

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LTC1149CN, LTC1149CN-3.3, LTC1149CN-5: $T_J = T_A + (P_D)(70°C/W)$

LTC1149CS, LTC1149CS-3.3, LTC1149CS-5: $T_J = T_A + (P_D)(110°C/W)$

Note 2: Pin 10 is a shutdown pin on the LTC1149-3.3 and LTC1149-5 fixed output voltage versions and must be at ground potential for testing.

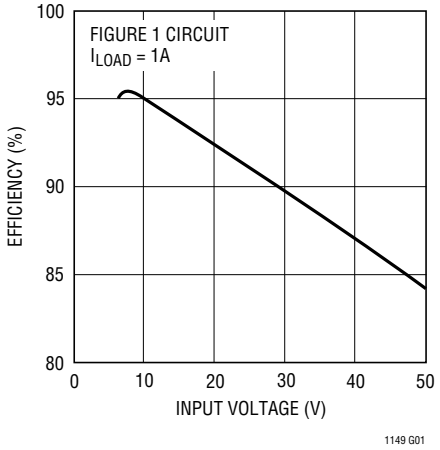
Note 3: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. The allowable operating frequency may be limited by power dissipation at high input voltages. See Typical Performance Characteristics and Applications Information.

Note 4: In applications where R_{SENSE} is placed at ground potential, the off-time increases approximately 40%.

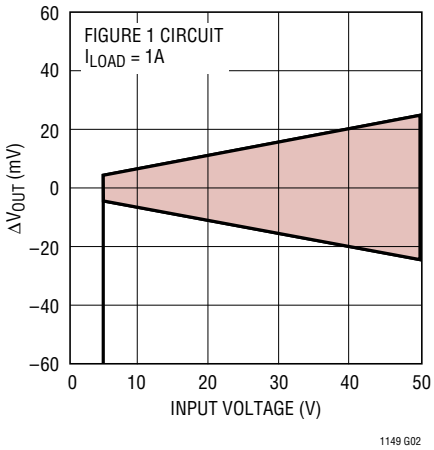
Note 5: The LTC1149, LTC1149-3.3, and LTC1149-5 are not tested and not quality assurance sampled at –40°C and 85°C. These specifications are guaranteed by design and/or correlation.

TYPICAL PERFORMANCE CHARACTERISTICS

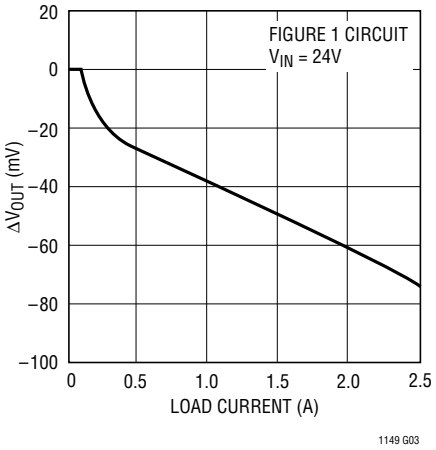
Efficiency vs Input Voltage



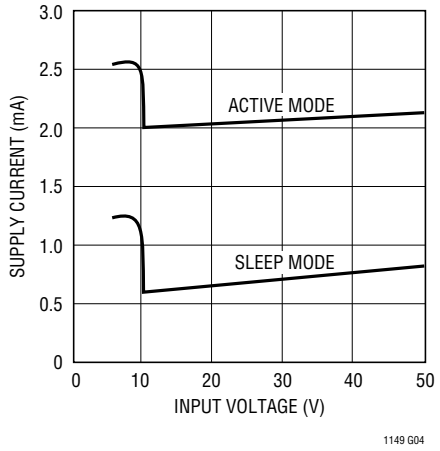
Line Regulation



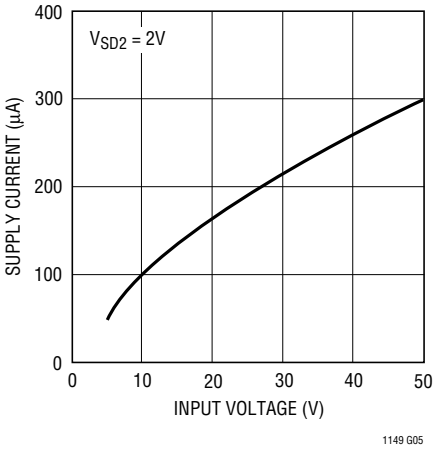
Load Regulation



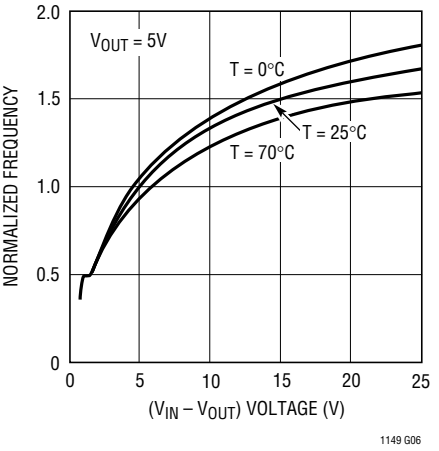
DC Supply Current



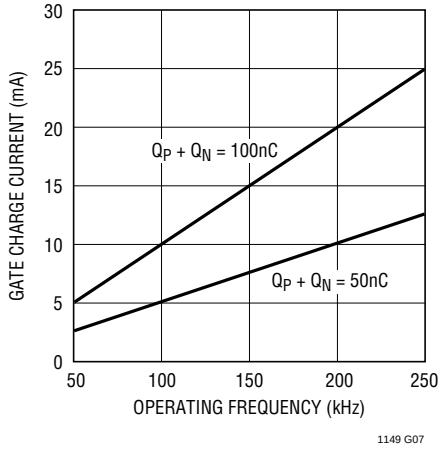
Supply Current in Shutdown



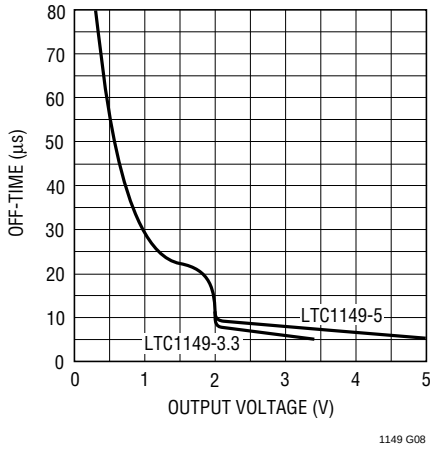
Operating Frequency vs (V_{IN} – V_{OUT})



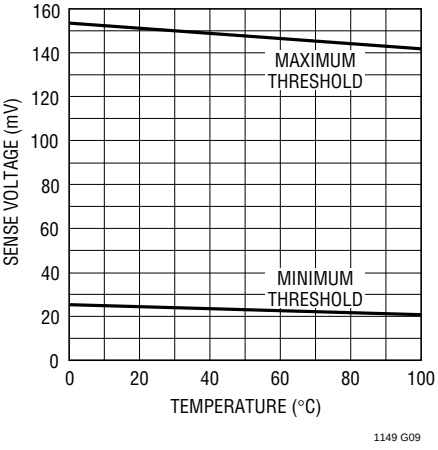
Gate Charge Supply Current



Off-Time vs V_{OUT}



Current Sense Threshold Voltage



PIN FUNCTIONS

PGATE (Pin 1): Level-Shifted Gate Drive Signal for Top P-Channel MOSFET. The voltage swing at Pin 1 is from V_{IN} to $V_{IN} – V_{CC}$.

V_{IN} (Pin 2): Main Supply Input Pin.

V_{CC} (Pin 3): Output Pin of Low Dropout 10V Regulator. *Pin 3 is not protected against DC short circuits.*

PDRIVE (Pin 4): High Current Gate Drive for Top P-Channel MOSFET. The voltage swing at Pin 4 is from V_{CC} to ground.

V_{CC} (Pin 5): Regulated 10V Input for Driver and Control Supplies. Must be closely decoupled to power ground.

C_T (Pin 6): External capacitor C_T from Pin 6 to ground sets the operating frequency. (The frequency is also dependent on the ratio V_{OUT}/V_{IN}.)

I_{TH} (Pin 7): Gain Amplifier Decoupling Point. The current comparator threshold increases with the Pin 7 voltage.

SENSE$^–$ (Pin 8): Connects to internal resistive divider which sets the output voltage in LTC1149-3.3 and LTC1149-5 versions. Pin 8 is also the (–) input for the current comparator.

SENSE$^+$ (Pin 9): The (+) Input for the Current Comparator. A built-in offset between Pins 8 and 9 in conjunction with R_{SENSE} sets the current trip threshold.

SHDN1/V_{FB} (Pin 10): In fixed output voltage versions, Pin 10 serves as a shutdown pin for the control circuitry only (V_{CC} is not affected). Taking Pin 10 of the LTC1149-3.3 or LTC1149-5 high holds both MOSFETs off. Must be at ground potential for normal operation.

For the LTC1149 adjustable version, Pin 10 serves as the feedback pin from an external resistive divider used to set the output voltage.

SGND (Pin 11): Small-Signal Ground. Must be routed separately from other grounds to the (–) terminal of C_{OUT}.

PGND (Pin 12): Driver Power Ground. Connects to source of N-channel MOSFET and the (–) terminal of C_{IN}.

NGATE (Pin 13): High Current Drive for Bottom N-channel MOSFET. The voltage swing at Pin 13 is from ground to V_{CC}.

RGND (Pin 14): Low Dropout Regulator Ground. Connects to power ground.

SHDN2 (Pin 15): Master Shutdown Pin. Taking Pin 15 high shuts down V_{CC} and all control circuitry; requires a logic signal with t_r, $t_f < 1\mu s$.

CAP (Pin 16): Charge Compensation Pin. A capacitor from Pin 16 to V_{CC} provides the charge required by the P-drive level-shift capacitor during supply transitions. *The Pin 16 capacitor must be larger than the Pin 4 capacitor.*

OPERATION (Refer to Functional Diagram)

The LTC1149 series uses a current mode, constant off-time architecture to synchronously switch an external pair of complementary power MOSFETs. Operating frequency is set by an external capacitor at the timing capacitor, Pin 6.

The output voltage is sensed either by an internal voltage divider connected to SENSE$^–$, Pin 8 (LTC1149-3.3 and LTC1149-5) or an external divider returned to V_{FB} Pin 10 (LTC1149). A voltage comparator V, and a gain block G, compare the divided output voltage with a reference voltage of 1.25V. To optimize efficiency, the LTC1149 series automatically switches between two modes of operation, burst and continuous. The voltage comparator is the primary control element for Burst Mode operation, while the gain block controls the output voltage in continuous mode.

A low dropout 10V regulator provides the operating voltage V_{CC} for the MOSFET drivers and control circuitry. The driver outputs at Pins 4 and 13 are referenced to ground, which fulfills the N-channel MOSFET gate drive requirement. The P-channel gate drive at Pin 1 must be referenced to the main supply input V_{IN}, which is accomplished by level-shifting the Pin 4 signal via an internal 500k resistor and external capacitor.

During the switch "ON" cycle in continuous mode, current comparator C monitors the voltage between Pins 8 and 9 connected across an external shunt in series with the inductor. When the voltage across the shunt reaches its threshold value, the PGATE output is switched to V_{IN}, turning off the P-channel MOSFET. The timing capacitor connected to Pin 6 is now allowed to discharge at a rate determined by the off-time controller. The discharge

OPERATION (Refer to Functional Diagram)

current is made proportional to the output voltage (measured by Pin 8) to model the inductor current, which decays at a rate which is also proportional to the output voltage. While the timing capacitor is discharging, the NGATE output is high, turning on the N-channel MOSFET.

When the voltage on the timing capacitor has discharged past V_{TH1}, comparator T trips, setting the flip-flop. This causes the NGATE output to go low (turning off the N-channel MOSFET) and the PGATE output to also go low (turning the P-channel MOSFET back on). The cycle then repeats.

As the load current increases, the output voltage decreases slightly. This causes the output of the gain stage to increase the current comparator threshold, thus tracking the load current.

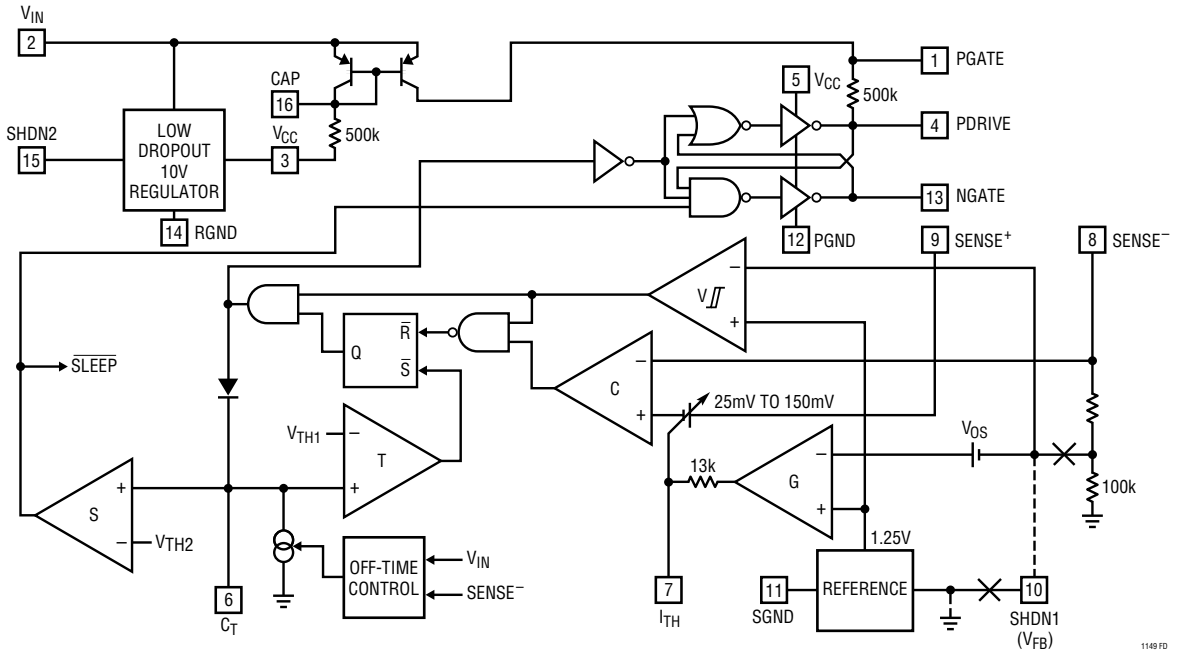
The sequence of events for Burst Mode operation is very similar to continuous operation with the cycle interrupted by the voltage comparator. When the output voltage is at or above the desired regulated value, the P-channel MOSFET is held off by comparator V and the timing capacitor continues to discharge below V_{TH1}. When the timing capacitor discharges past V_{TH2}, voltage comparator S trips, causing the internal $\overline{SLEEP}$ line to go low and the N-channel MOSFET to turn off.

The circuit now enters sleep mode with both power MOSFETs turned off. In sleep mode, much of the circuitry is turned off, dropping the supply current from several milliamperes (with the MOSFETs switching) to 600µA. When the output capacitor has discharged by the amount of hysteresis in comparator V, the P-channel MOSFET is again turned on and this process repeats. To avoid the operation of the current loop interfering with Burst Mode operation, a built-in offset is incorporated in the gain stage. This prevents the current comparator threshold from increasing until the output voltage has dropped below a minimum threshold.

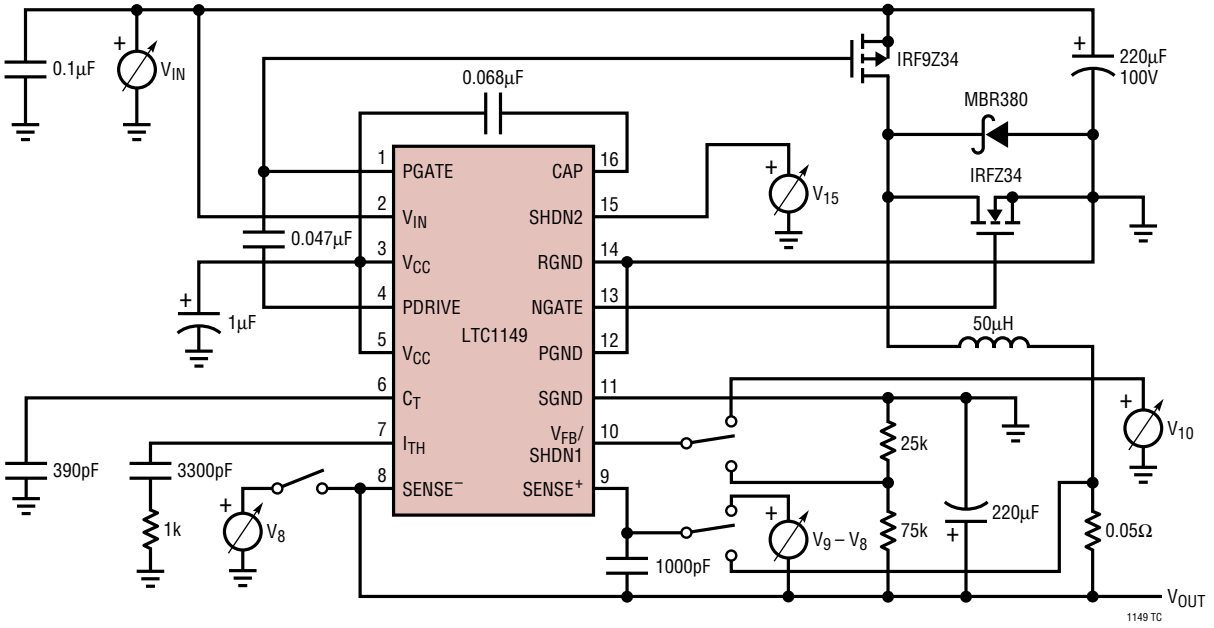
To prevent both the external MOSFETs from ever being turned on at the same time, feedback is incorporated to sense the state of the driver output pins. Before the N-gate output can go high, the P-drive output must also be high. Likewise, the P-drive output is prevented from going low when the N-gate output is high.

Using constant off-time architecture, the operating frequency is a function of the input voltage. To minimize the frequency variation as dropout is approached, the off-time controller increases the discharge current as V_{IN} drops below V_{OUT} + 1.5V. In dropout the P-channel MOSFET is turned on continuously.

FUNCTIONAL DIAGRAM Pin 10 connection shown for LTC1149-3.3 and LTC1149-5; changes create LTC1149.



TEST CIRCUIT



APPLICATIONS INFORMATION

Typical Application Circuit

The basic LTC1149 series application circuit is shown in Figure 1. External component selection is driven by the input voltage and output load requirement, and begins with the selection of R_{SENSE}. Once R_{SENSE} is known, C_T and L can be chosen. Next, the power MOSFETs and D1 are selected. Finally, C_{IN} and C_{OUT} are selected and the loop is compensated. The circuit shown in Figure 1 can be configured for operation up to an input voltage of 48V. If the application does not require greater than 15V operation, then the LTC1148 should be used.

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. The LTC1149 series current comparator has a threshold range which extends from a minimum of 25mV/R_{SENSE} to a maximum of 150mV/R_{SENSE}. The current comparator threshold sets the peak of the inductor ripple current, yielding a maximum output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current. *For proper Burst Mode operation, $I_{RIPPLE(P-P)}$ must be less than or equal to the minimum current comparator threshold.*

Since efficiency generally increases with ripple current, the maximum allowable ripple current is assumed, i.e., $I_{RIPPLE(P-P)}$ = 25mV/R_{SENSE} (see C_T and L Selection for Operating Frequency). Solving for R_{SENSE} and allowing a margin for variations in the LTC1149 series and external component values yields:

$$R_{SENSE} = \frac{100mV}{I_{MAX}}$$

A graph for selecting R_{SENSE} versus maximum output current is given in Figure 2. The LTC1149 series works well with values of R_{SENSE} from 0.02Ω to 0.2Ω.

The load current below which Burst Mode operation commences, I_{BURST}, and the peak short-circuit current, $I_{SC(PK)}$, both track I_{MAX}. Once R_{SENSE} has been chosen, I_{BURST} and $I_{SC(PK)}$ can be predicted from the following equations:

$$I_{BURST} \approx \frac{15mV}{R_{SENSE}}$$

$$I_{SC(PK)} = \frac{150mV}{R_{SENSE}}$$

APPLICATIONS INFORMATION

The LTC1149 series automatically extends t_{OFF} during a short circuit to allow sufficient time for the inductor current to decay between switch cycles. The resulting ripple current causes the average short-circuit current $I_{SC(AVG)}$ to be reduced to approximately I_{MAX}.

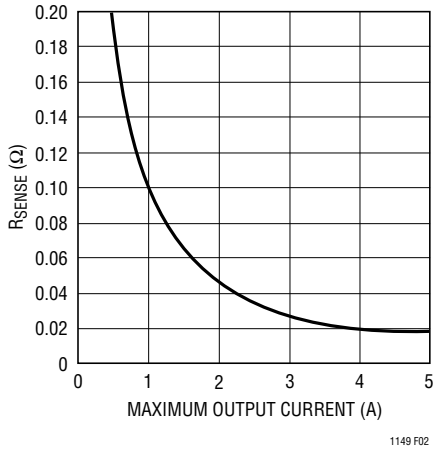


Figure 2. R_{SENSE} vs Maximum Output Current

L and C_T Selection for Operating Frequency

The LTC1149 series uses a constant off-time architecture with t_{OFF} determined by an external timing capacitor C_T. Each time the P-channel MOSFET switch turns on, the voltage on C_T is reset to approximately 3.3V. During the off-time, C_T is discharged by a current which is proportional to V_{OUT}. The voltage on C_T is analogous to the current in inductor L, which likewise decays at a rate proportional to V_{OUT}. Thus the inductor value must track the timing capacitor value.

The value of C_T is calculated from the desired continuous mode operating frequency, f:

$$C_T = \frac{(7.8)(10^{-5})}{f}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

A graph for selecting C_T versus frequency including the effects of input voltage is given in Figure 3.

As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations). The complete expression for operating frequency is given by:

$$f = \frac{1}{t_{OFF}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where:

$$t_{OFF} = (1.3)(10^4)(C_T)\left(\frac{V_{REG}}{V_{OUT}}\right)$$

V_{REG} is the desired output voltage (i.e., 5V, 3.3V), while V_{OUT} is the actual output voltage. Thus $V_{REG}/V_{OUT} = 1$ when in regulation.

Note that as V_{IN} decreases, the frequency decreases. When the input to output voltage differential drops below 1.5V, the LTC1149 series reduces t_{OFF} by increasing the discharge current in C_T. This prevents audible operation prior to dropout.

Once the frequency has been set by C_T, the inductor L must be chosen to provide no more than 25mV/R_{SENSE} of peak-to-peak inductor ripple current. This results in a minimum required inductor value of:

$$L_{MIN} = (5.1)(10^5)(R_{SENSE})(C_T)(V_{REG})$$

As the inductor value is increased from the minimum value, the ESR requirements for the output capacitor are eased at the expense of efficiency. If too small an inductor is used, the inductor current will decrease past zero and change polarity. A consequence of this is that the LTC1149 series may not enter Burst Mode operation and efficiency will be severely degraded at low currents.

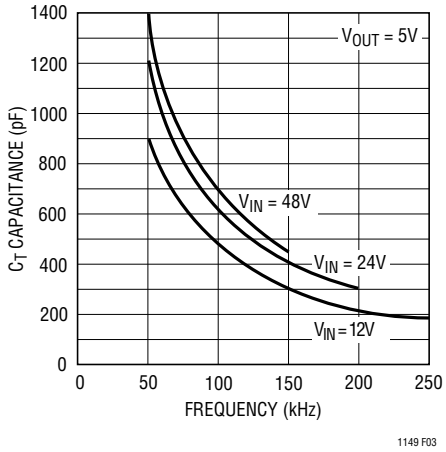


Figure 3. Timing Capacitor Selection

APPLICATIONS INFORMATION

Inductor Core Selection

Once the minimum value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy, or Kool Mμ® cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses increase.

Ferrite designs have very low core loss, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple which can cause Burst Mode operation to be falsely triggered in the LTC1149 series. Do not allow the core to saturate!

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, new surface mount designs available from Coiltronics do not increase the height significantly.

P-Channel MOSFET Selection

Two external power MOSFETs must be selected for use with the LTC1149 series: a P-channel MOSFET for the main switch, and an N-channel MOSFET for the synchronous switch.

The minimum input voltage determines whether standard threshold or logic-level threshold MOSFETs must be used. For $V_{IN} > 8V$, standard threshold MOSFETs ($V_{GS(TH)} < 4V$) may be used. If V_{IN} is expected to drop below 8V, logic-level threshold MOSFETs ($V_{GS(TH)} < 2.5V$) are strongly recommended. When logic-level MOSFETs are used, the absolute maximum V_{GS} rating for the MOSFETs must be greater than the LTC1149 series internal regulator voltage V_{CC}.

Selection criteria for the P-channel MOSFET include the on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS}, input voltage and maximum output current. When the LTC1149 is operating in continuous mode, the duty cycle for the P-channel MOSFET is given by:

$$\text{P-Ch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

The P-channel MOSFET dissipation at maximum output current is given by:

$$\text{P-Ch } P_D = \frac{V_{OUT}}{V_{IN}} (I_{MAX})^2 (1 + \partial_P)\, R_{DS(ON)} + K(V_{IN})^2 (I_{MAX})(C_{RSS})(f)$$

where ∂ is the temperature dependency of $R_{DS(ON)}$ and K is a constant related to the gate drive current. Note the two distinct terms in the equation. The first gives the I^2R losses, which are highest at low input voltages, while the second gives the transition losses, which are highest at high input voltages. For $V_{IN} < 24V$, the high current efficiency generally improves with larger MOSFETs (although gate charge losses begin eating into the gains. See Efficiency Considerations). For $V_{IN} > 24V$, the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{RSS} actually provides higher efficiency. This is illustrated in the Design Example section.

The term $(1 + \partial)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but $\partial = 0.007/°C$ can be used as an approximation for low voltage MOSFETs. C_{RSS} is usually specified in the MOSFET electrical characteristics. The constant K is much harder to pin down, but K = 5 can be used for the LTC1149 series to estimate the relative contributions of the two terms in the P-channel dissipation equation.

N-Channel MOSFET and D1 Selection

The same input voltage constraints apply to the N-channel MOSFET as to the P-channel with regard to when logic-level devices are required. However, the dissipation calculation is quite different. The duty cycle and dissipation for

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the N-channel MOSFET operating in continuous mode are given by:

$$\text{N-Ch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

$$\text{N-Ch } P_D = \frac{V_{IN} - V_{OUT}}{V_{IN}} (I_{MAX})^2 (1 + \partial_N) R_{DS(ON)}$$

where ∂ is the temperature dependency of $R_{DS(ON)}$. Note that there is no transition loss term in the N-channel dissipation equation because the drain-to-source voltage is always low when the N-channel MOSFET is turning on or off. The remaining I^2R losses are the greatest at high input voltage or during a short circuit, when the N-channel duty cycle is nearly 100%. Fortunately, low $R_{DS(ON)}$ N-channel MOSFETs are readily available which reduce losses to the point that heat sinking is not required, even during continuous short-circuit operation.

The Schottky diode D1 shown in Figure 1 only conducts during the dead-time between the conduction of the two power MOSFETs. D1's sole purpose in life is to prevent the body diode of the N-channel MOSFET from turning on and storing charge during the dead-time, which could cost as much as 1% in efficiency (although there are no other harmful effects if D1 is omitted). Therefore, D1 should be selected for a forward voltage of less than 0.7V when conducting I_{MAX}.

Finally, both MOSFETs and D1 must be selected for breakdown voltages higher than the maximum V_{IN}.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the P-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ Required } I_{RMS} \approx \frac{I_{MAX} [V_{OUT}(V_{IN} - V_{OUT})]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{MAX}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. An additional 0.1µF ceramic capacitor may also be required on V_{IN} for high frequency decoupling.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). The ESR of C_{OUT} must be less than twice the value of R_{SENSE} for proper operation of the LTC1149 series:

$$C_{OUT} \text{ Required ESR} < 2R_{SENSE}$$

Optimum efficiency is obtained by making the ESR equal to R_{SENSE}. As the ESR is increased up to $2R_{SENSE}$, the efficiency degrades by less than 1%. If the ESR is greater than $2R_{SENSE}$, the voltage ripple on the output capacitor will prematurely trigger Burst Mode operation, resulting in disruption of continuous mode and an efficiency hit which can be several percent.

Manufacturers such as Nichicon, Chemicon and Sprague should be considered for high performance capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR for its size, at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface mount applications multiple capacitors may have to be paralleled to meet the capacitance, ESR, or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. For example, if 200µF/10V is called for in an application requiring 3mm height, two AVX 100µF/10V (P/N TPSD 107K010) could be used. Consult the manufacturer for other specific recommendations.

At low supply voltages, a minimum value of C_{OUT} is suggested to prevent an abnormal low frequency operating mode (see Figure 4). When C_{OUT} is too small, the

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output ripple at low frequencies will be large enough to trip the voltage comparator. This causes the Burst Mode operation to be activated when the LTC1149 series would normally be in continuous operation. The effect is most pronounced with low values of R_{SENSE} and can be improved by operating at higher frequencies with lower values of L. The output remains in regulation at all times.

Checking Transient Response

Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $(\Delta I_{LOAD})(ESR)$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} until the regulator loop adapts to the current change and returns V_{OUT} to its steady state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing which would indicate a stability problem. The Pin 7 external components shown in the Figure 1 circuit will prove adequate compensation for most applications.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately $(25)(C_{LOAD})$. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

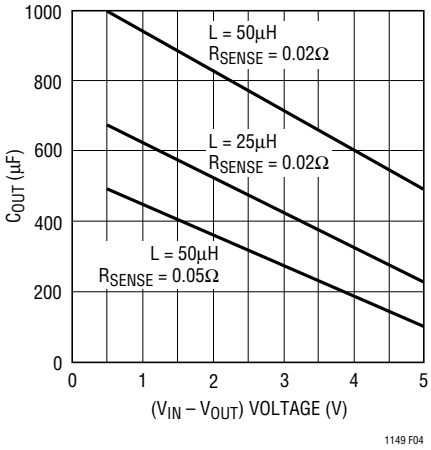

Figure 4. Minimum Suggested C_{OUT}

LTC1149 Adjustable Applications

When an output voltage other than 3.3V or 5V is required, the LTC1149 adjustable version is used with an external resistive divider from V_{OUT} to V_{FB} Pin 10. The regulated voltage is determined:

$$V_{OUT} = 1.25\left(1 + \frac{R2}{R1}\right)$$

In applications where V_{OUT} is greater than the LTC1149 internally regulated V_{CC} voltage, R_{SENSE} must be moved to

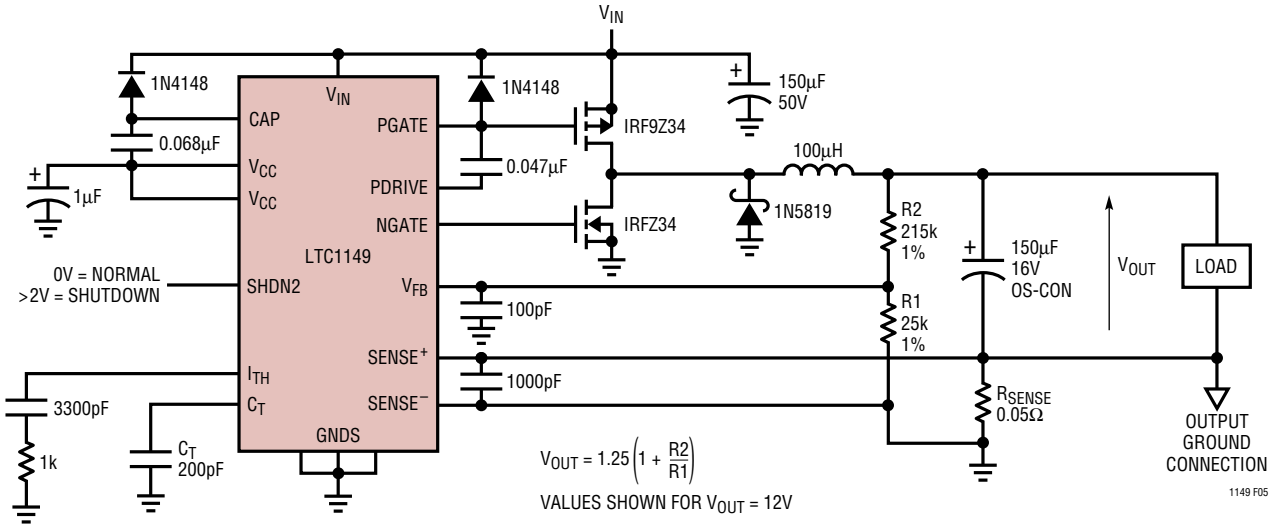

Figure 5. High Efficiency Step-Down Regulator with $V_{OUT} > V_{CC}$

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the ground side of the output to prevent the absolute maximum voltage ratings of the sense pins from being exceeded. This is shown in Figure 5. When the current sense comparator is operating at 0V common mode, the off-time increases approximately 40%, requiring the use of a smaller timing capacitor C_T.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%\text{Efficiency} = 100 - (L1 + L2 + L3 + ...)$$

where L1, L2, etc., are the individual losses as a percentage of input power. (For high efficiency circuits only small errors are incurred by expressing losses as a percentage of output power.)

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC1149 series circuits: 1) LTC1149 DC supply current, 2) MOSFET gate charge current, 3) I^2R losses and 4) P-channel transition losses.

1. The DC supply current is the current which flows into V_{IN} Pin 2 less the gate charge current. For V_{IN} = 12V the LTC1149 DC supply current is 0.6mA for no load, and increases proportionally with load up to 2mA after the LTC1149 series has entered continuous mode. Because the DC supply current is drawn from V_{IN}, the resulting loss increases with input voltage. For V_{IN} = 24V, the DC bias losses are generally less than 3% for load currents over 300mA. However, at very low load currents the DC bias current accounts for nearly all of the loss.
2. MOSFET gate charge current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} which is typically much larger than the DC supply current. In continuous mode, $I_{GATECHG} = f (Q_N + Q_P)$. The typical gate charge for a 0.1Ω N-channel power MOSFET is 25nC, and for a P-channel about twice that value. This results in $I_{GATECHG}$ = 7.5mA in 100kHz continuous operation, for a 5% to 10% typical mid-current loss with V_{IN} = 24V.

   Note that the gate charge loss increases directly with both input voltage and operating frequency. This is the principal reason why the highest efficiency circuits operate at moderate frequencies. Furthermore, it argues against using larger MOSFETs than necessary to control I^2R losses, since overkill can cost efficiency as well as money!
3. I^2R losses are easily predicted from the DC resistances of the MOSFET, inductor and current shunt. In continuous mode all of the output current flows through L and R_{SENSE}, but is "chopped" between the P-channel and N-channel MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)}$ = 0.1Ω, R_L = 0.15Ω and R_{SENSE} = 0.05Ω, then the total resistance is 0.3Ω. This results in losses ranging from 3% to 12% as the output current increases from 0.5A to 2A. I^2R losses cause the efficiency to roll-off at high output currents.
4. Transition losses apply only to the P-channel MOSFET, and only when operating at high input voltages (typically 24V or greater). Transition losses can be estimated from:

   $$\text{Transition Loss} \approx 5(V_{IN})^2(I_{MAX})(C_{RSS})(f)$$

For example, if V_{IN} = 48V, I_{MAX} = 2A, C_{RSS} = 300pF (a very large MOSFET) and f = 100kHz, the transition loss is 0.7W. A loss of this magnitude would not only kill efficiency but would probably require additional heat sinking for the MOSFET! See Design Example for further guidelines on how to select the P-channel MOSFET.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses, Schottky conduction losses during dead-time, and inductor core losses, generally account for less than 2% total additional loss.

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LTC1149 Package Dissipation

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC1149 series to be exceeded. The LTC1149 supply current is dominated by the gate charge supply current, which is given as a function of operating frequency in the Typical Performance Characteristics. The LTC1149 series junction temperature can be estimated by using the equations given in Note 1 of the Electrical Characteristics. For example, the LT1149CS is limited to less than 11mA from a 48V supply:

$T_J = 70°C + (11mA)(48V)(110°C/W)$
$= 128°C$ exceeds absolute maximum

To prevent the maximum junction temperature from being exceeded, the Pin 2 supply current must be checked in continuous mode when operating at the maximum V_{IN}.

Design Example

As a design example, assume V_{IN} = 24V, V_{OUT} = 5V, I_{MAX} = 2.5A and f = 100kHz. R_{SENSE}, C_T and L can immediately be calculated:

$$R_{SENSE} = \frac{100mV}{2.5} = 0.039\Omega$$

$$C_T = \frac{(7.8)(10^{-5})}{100kHz}\left(1 - \frac{5V}{24V}\right) = 620pF$$

$$L_{MIN} = (5.1)(10^5)(0.039\Omega)(620pF)(5V) = 62\mu H$$

Selection of the P-channel MOSFET involves doing calculations for different sized MOSFETs to determine the relative loss contributions. Taking an International Rectifier IRF9Z34 for example, $R_{DS(ON)}$ = 0.14Ω Max, Q_P = 35nC and C_{RSS} = 200pF ($V_{DS} = V_{IN}/2$). These values can be used to estimate the I^2R losses, transition losses and gate charge supply current losses:

Est. I^2R Loss (T_J = 100°C) =
$(5V/24V)(2.5)^2(1 + 0.5)0.14\Omega = 270mW$

Est. Transition Loss =
$5(24V)^2(2.5A)(200pF)(100kHz) = 145mW$

Est. Gate Charge Loss =
$(100kHz)(35nC)(24V) = 85mW$

The same calculations were repeated for a smaller device, the Motorola MTD2955 ($R_{DS(ON)}$ = 0.3Ω) and a larger one, the Harris RFP30P05 ($R_{DS(ON)}$ = 0.065Ω). The results are summarized in the table.

CONDITIONS V_{IN} = 24V, V_{OUT} = 5V F = 100kHz, I_{OUT} = 2.5A	P-CHANNEL MOSFET		
	MTD2955	**IRF9Z34**	**RFP30P05**
Est. I^2R Loss (100°C)	550mW	270mW	120mW
Est. Transition Loss	110mW	145mW	290mW
Est. Gate Charge Loss	60mW	85mW	240mW
Est. Total Loss	720mW	500mW	650mW

For this set of conditions, the midsized P-channel MOSFET actually produces the lowest total losses at I_{MAX}. The resulting efficiency differences will be even more pronounced at lower output currents. Note that only the I^2R and transition losses are dissipated in the MOSFET; the gate charge supply current loss is dissipated by the LTC1149 series.

Selection of the N-channel MOSFET is somewhat easier; it need only be sized for the anticipated I^2R losses at 100% duty cycle (worst-case assumption for short circuit.) The Siliconix Si9410, for example, has $R_{DS(ON)}$ = 0.03Ω Max and Q_N = 30nC. This will produce an I^2R loss of 250mW at 100°C and a gate charge supply current loss of 75mW. As with the P-channel device, the use of a larger MOSFET may actually result in lower midcurrent efficiency.

C_{IN} will require an RMS current rating of at least 1.25A at temperature, and C_{OUT} will require an ESR of 0.04Ω for optimum efficiency. The output capacitor ESR requirement can be fulfilled by a single OS-CON or by two or more surface mount tantalums in parallel.

Auxiliary Windings – Suppressing Burst Mode Operation

The LTC1149 synchronous switch removes the normal limitation that power must be drawn from the inductor primary winding in order to extract power from auxiliary windings. With synchronous switching, auxiliary outputs may be loaded without regard to the primary output load, providing that the loop remains in continuous mode operation.

Burst Mode operation can be suppressed at low output currents with a simple external network which cancels the

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25mV minimum current comparator threshold. This technique is also useful for eliminating audible noise from certain types of inductors in high current (I_{OUT} > 5A) applications when they are lightly loaded.

An external offset is put in series with the SENSE$^-$ pin to subtract from the built-in 25mV offset. An example of this technique is shown in Figure 6. Two 100Ω resistors are inserted in series with the leads from the sense resistor.

With the addition of R3, a current is generated through R1 causing an offset of:

$$V_{OFFSET} = V_{OUT}\left(\frac{R1}{R1 + R3}\right)$$

If V_{OFFSET} > 25mV, the minimum threshold will be cancelled and Burst Mode operation is prevented from occurring. Since V_{OFFSET} is constant, the maximum load current is also decreased by the same offset. Thus, to get back to the same I_{MAX}, the value of the sense resistor must be lower:

$$R_{SENSE} \approx \frac{75mV}{I_{MAX}}$$

To prevent noise spikes from erroneously tripping the current comparator, a 1000pF capacitor is needed across Pins 8 and 9.

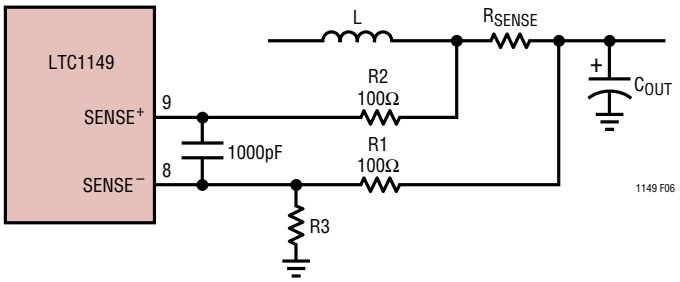

Figure 6. Suppressing Burst Mode Operation

Output Crowbar

An added feature to using an N-channel MOSFET as the synchronous switch is the ability to crowbar the output with the same MOSFET. Pulling the timing capacitor Pin 6 above 1.5V when the output voltage is greater than the desired regulated value, will turn on the N-channel MOSFET.

A fault condition which causes the output voltage to go above a maximum value can be detected by external circuitry. Turning on the N-channel MOSFET when this fault is detected will then force the system fuse to blow.

The N-channel MOSFET needs to be sized so it will safely handle this overcurrent condition. The typical delay from pulling the C_T Pin 6 high to when the NGATE Pin 13 goes high is 250ns. *Under shutdown conditions, the N-channel is held off and pulling Pin 6 high will not cause the output to be crowbarred.*

A small N-channel FET can be used as an interface between the overvoltage detect circuitry and the LTC1149 as shown in Figure 7.

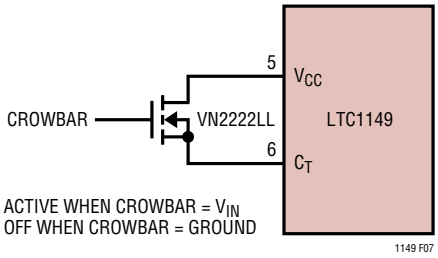

Figure 7. Output Crowbar Interface

Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1149 series. These items are also illustrated graphically in the layout diagram of Figure 8. Check the following in your layout:

1. Are the signal and power grounds segregated? The LTC1149 signal ground Pin 11 must connect separately to the (–) plate of C_{OUT}. The other ground Pins 12 and 14 should return to the source of the N-channel MOSFET, anode of the Schottky diode and (–) plate of C_{IN}, which should have as short lead lengths as possible.
2. Does the LTC1149 SENSE$^-$ Pin 8 connect to a point close to R_{SENSE} and the (+) plate of C_{OUT}? In adjustable applications, the resistive divider R1, R2 must be connected between the (+) plate of C_{OUT} and signal ground.
3. Are the SENSE$^-$ and SENSE$^+$ leads routed together with minimum PC trace spacing? The differential decoupling capacitor between Pins 8 and 9 should be as close as possible to the LTC1149. Up to 100Ω may be placed

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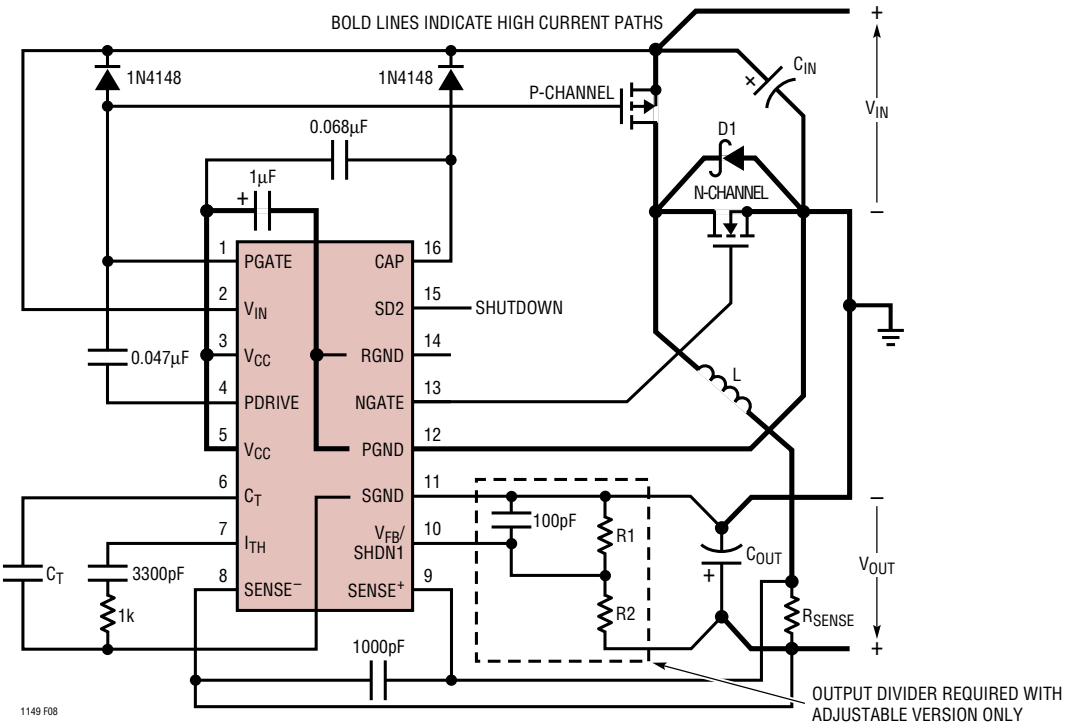

Figure 8. LTC1149 Series Layout Diagram (see Layout Checklist)

in series with each sense lead to help decouple Pins 8 and 9. However, when these resistors are used, the capacitor should be no larger than 1000pF.

4. Does the (+) plate of C_{IN} connect to the source of the P-channel MOSFET as closely as possible? An additional 0.1µF ceramic capacitor between V_{IN} and power ground may be required in some applications.
5. Is the V_{CC} decoupling capacitor connected closely between Pin 5 of the LTC1149 and power ground? This capacitor carries the MOSFET driver peak currents.
6. Is the SHDN1 Pin 10 (fixed output versions only) actively pulled to ground during normal operation? The SHDN1 pin is high impedance and must not be allowed to float. In adjustable versions, Pin 10 is the feedback pin and is very sensitive to pickup from the switch node. Care must be taken to isolate V_{FB} from possible capacitive coupling of the inductor switch signal.

Troubleshooting Hints

Since efficiency is critical to LTC1149 series applications, it is very important to verify that the circuit is functioning correctly in both continuous and Burst Mode operation. The waveform to monitor is the voltage on the timing capacitor Pin 6.

In continuous mode ($I_{LOAD} > I_{BURST}$) the voltage on Pin 6 should be a sawtooth with a $0.9V_{P-P}$ swing. This voltage should never dip below 2V as shown in Figure 9a.

When load currents are low ($I_{LOAD} < I_{BURST}$) Burst Mode operation should occur with the C_T pin waveform periodically falling to ground as shown in Figure 9b.

If Pin 6 is observed falling to ground at high output currents, it indicates poor decoupling or improper grounding. Refer to the Board Layout Checklist.

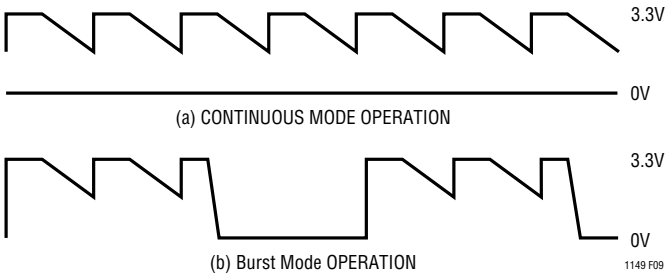

Figure 9. C_T Pin 6 Waveforms

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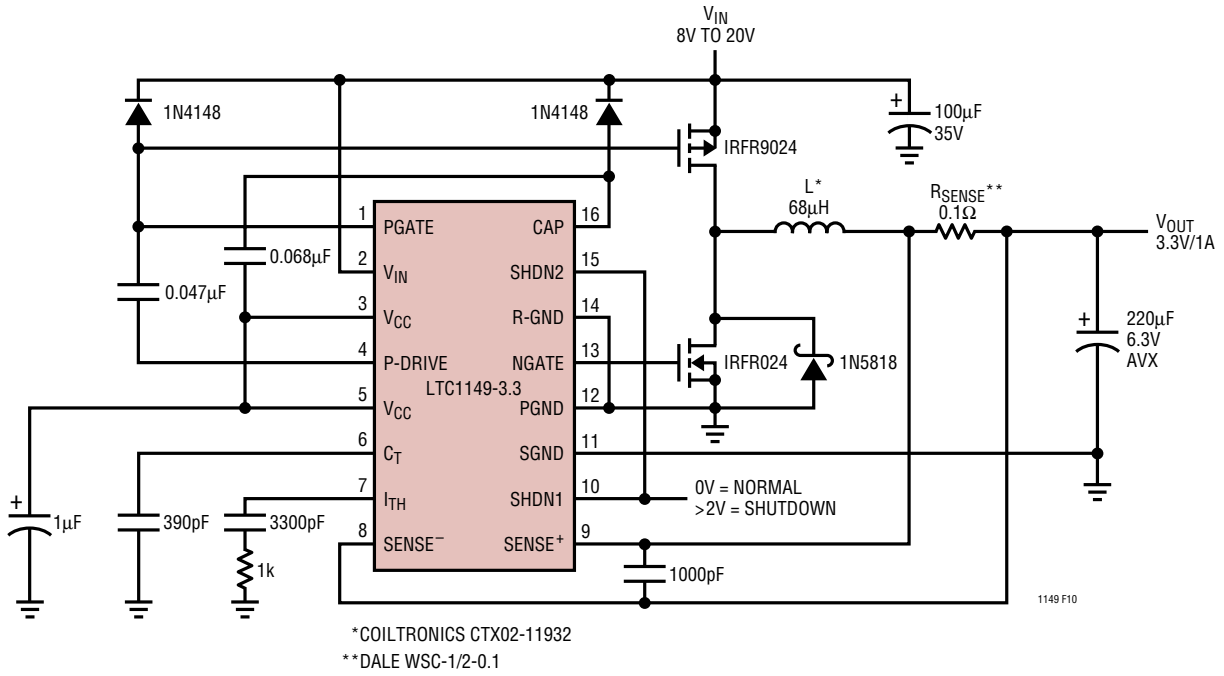

Figure 10. High Efficiency 8V to 20V Input 3.3V/1A Output Regulator

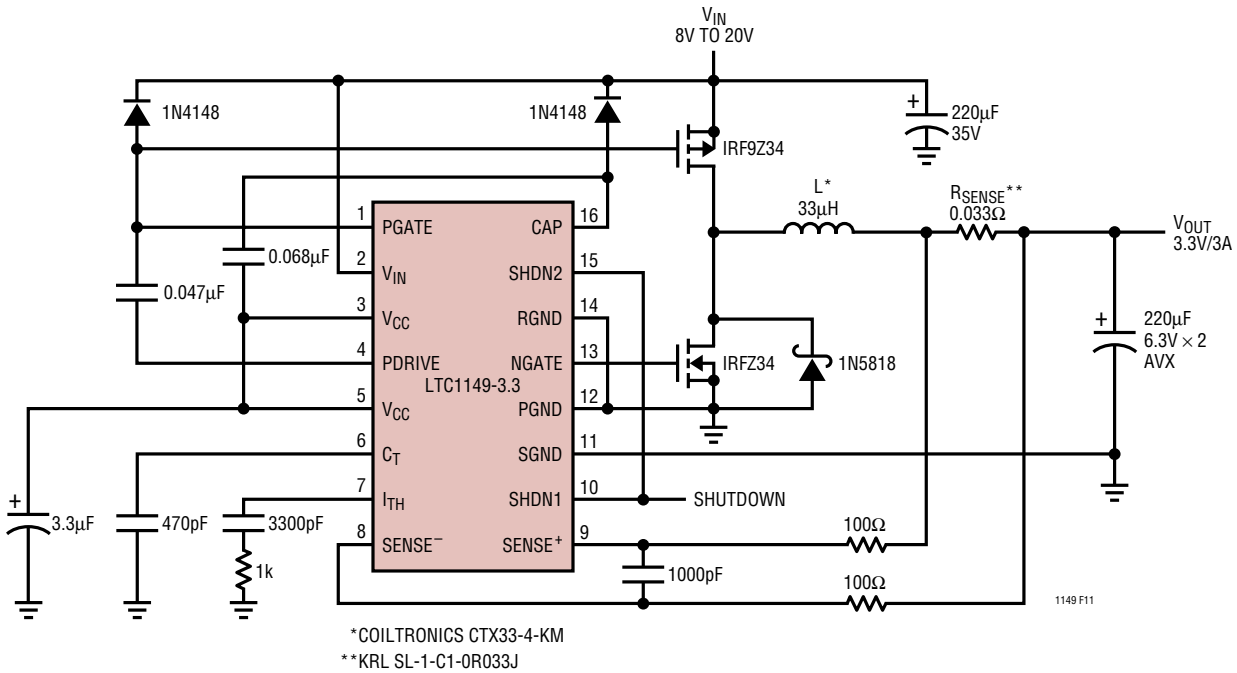

Figure 11. High Efficiency 8V to 20V Input 3.3V/3A Output Regulator

TYPICAL APPLICATIONS

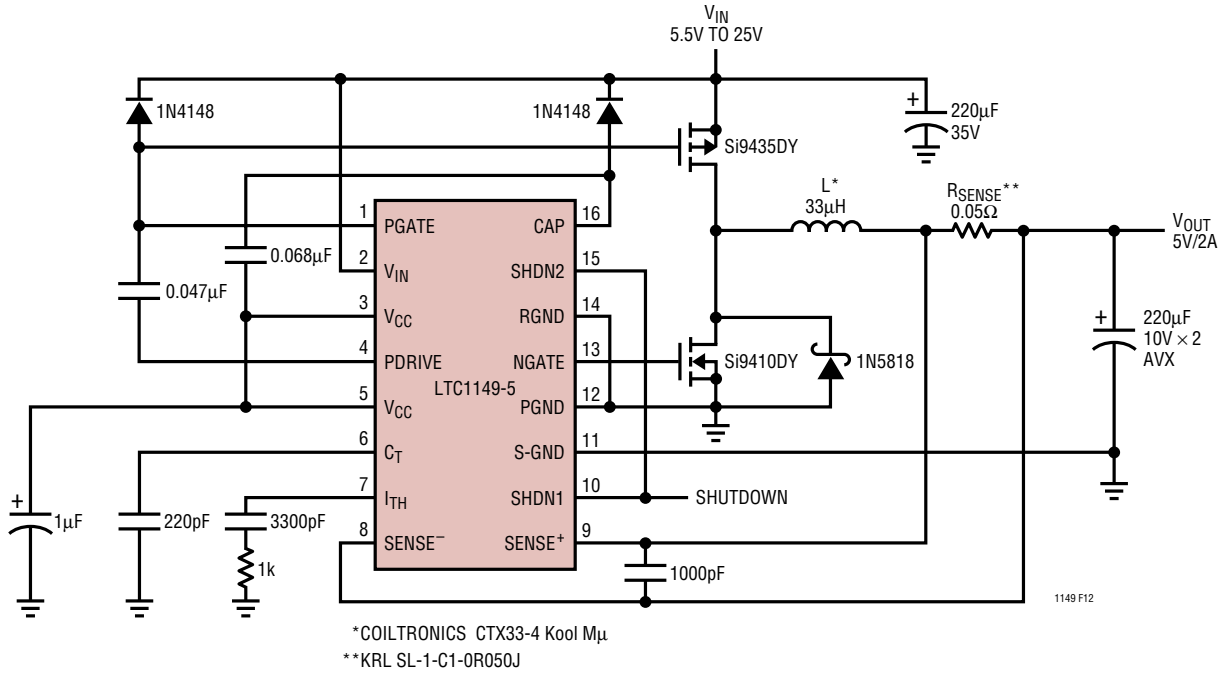

Figure 12. Ultra Wide Input Range (5.5V to 25V) High Efficiency 5V Regulator

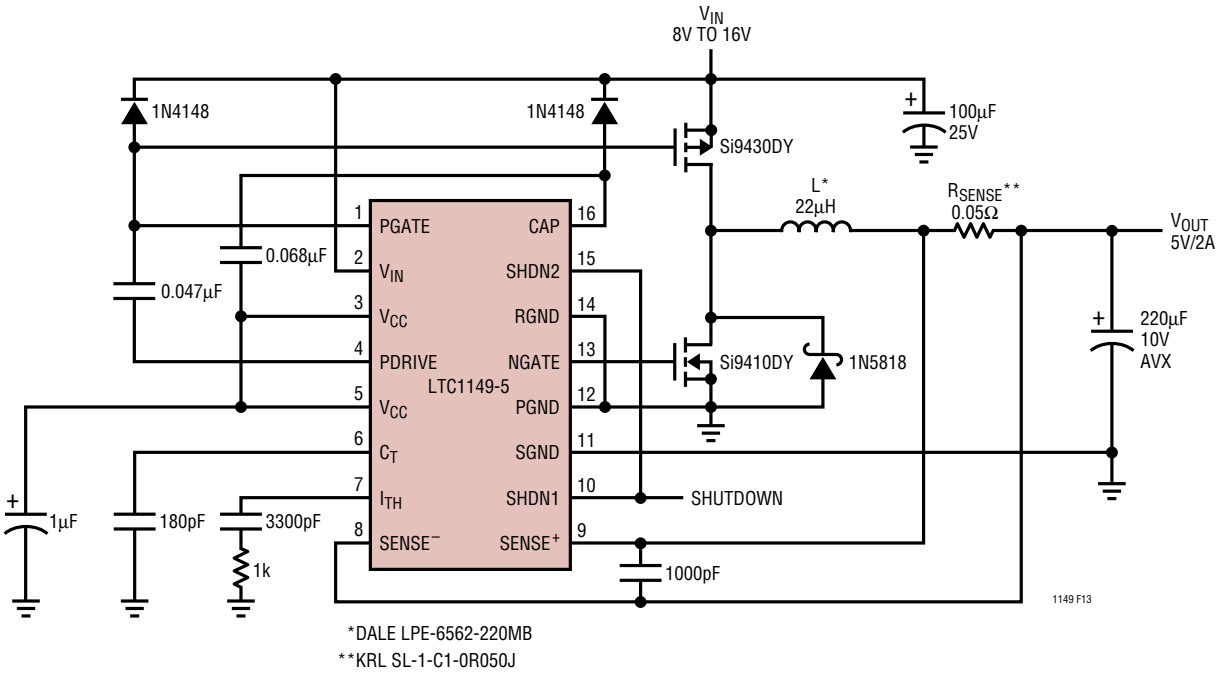

Figure 13. 250kHz High Efficiency 12V Input 5V/2A Output Regulator

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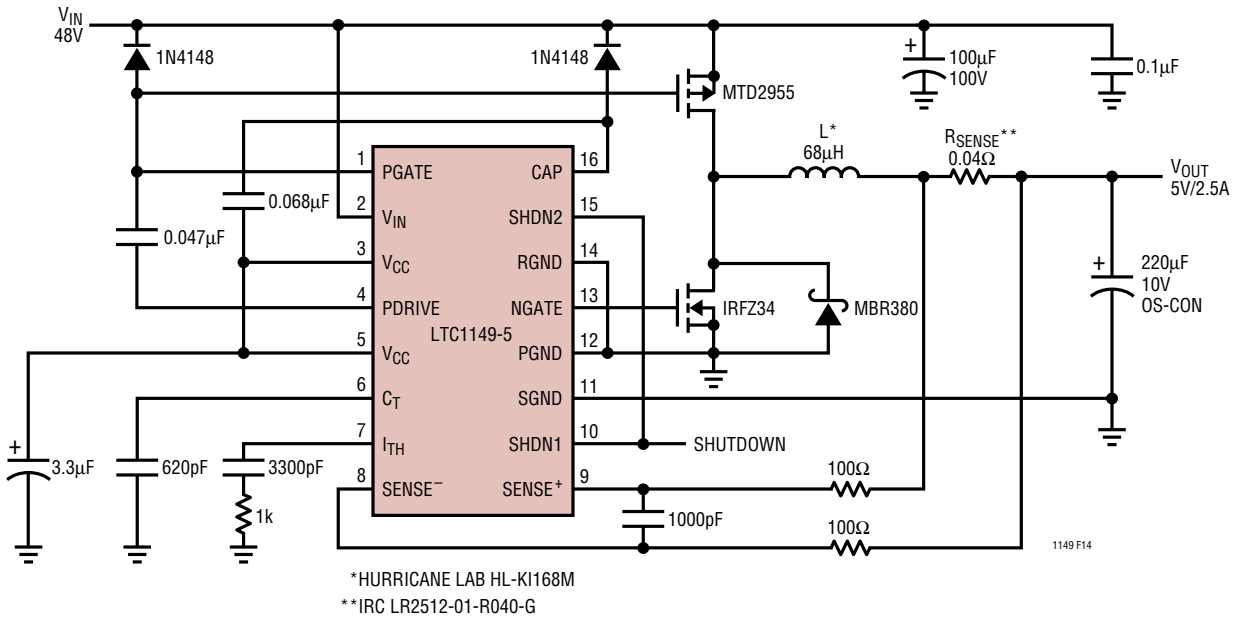

Figure 14. High Efficiency 48V Input 5V/2.5A Output Regulator

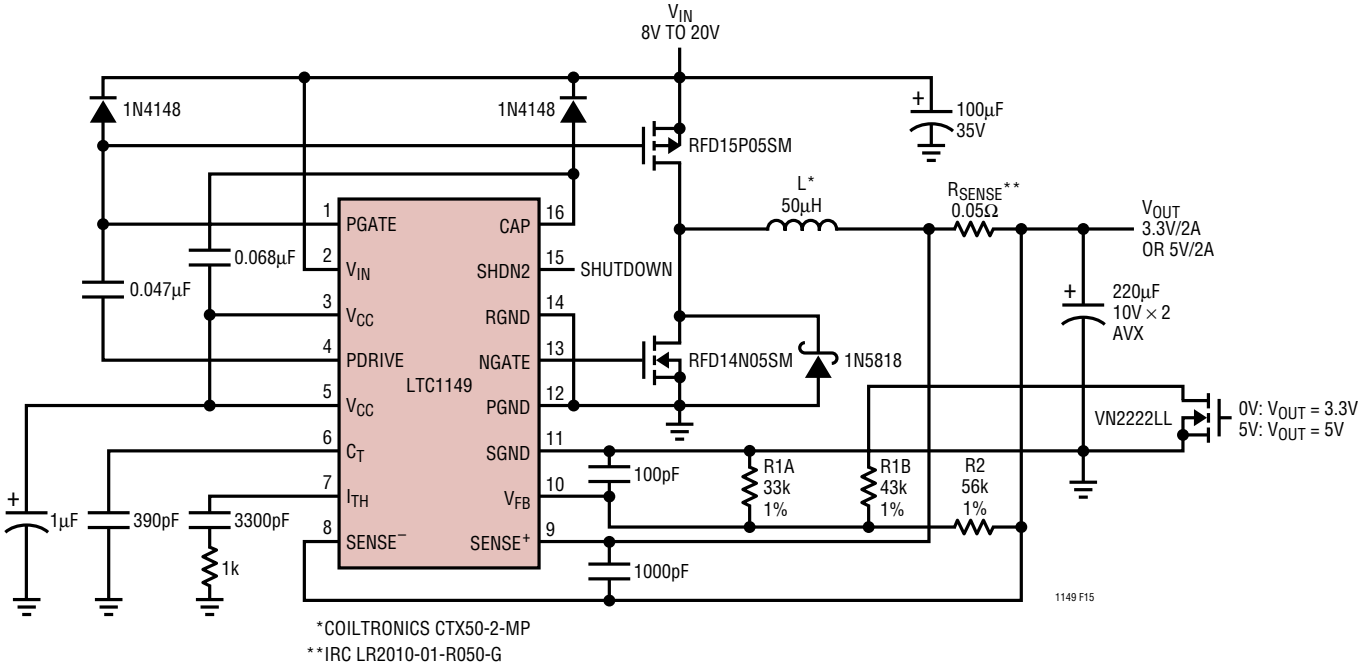

Figure 15. Logic Selectable 5V/2A or 3.3V/2A High Efficiency Regulator

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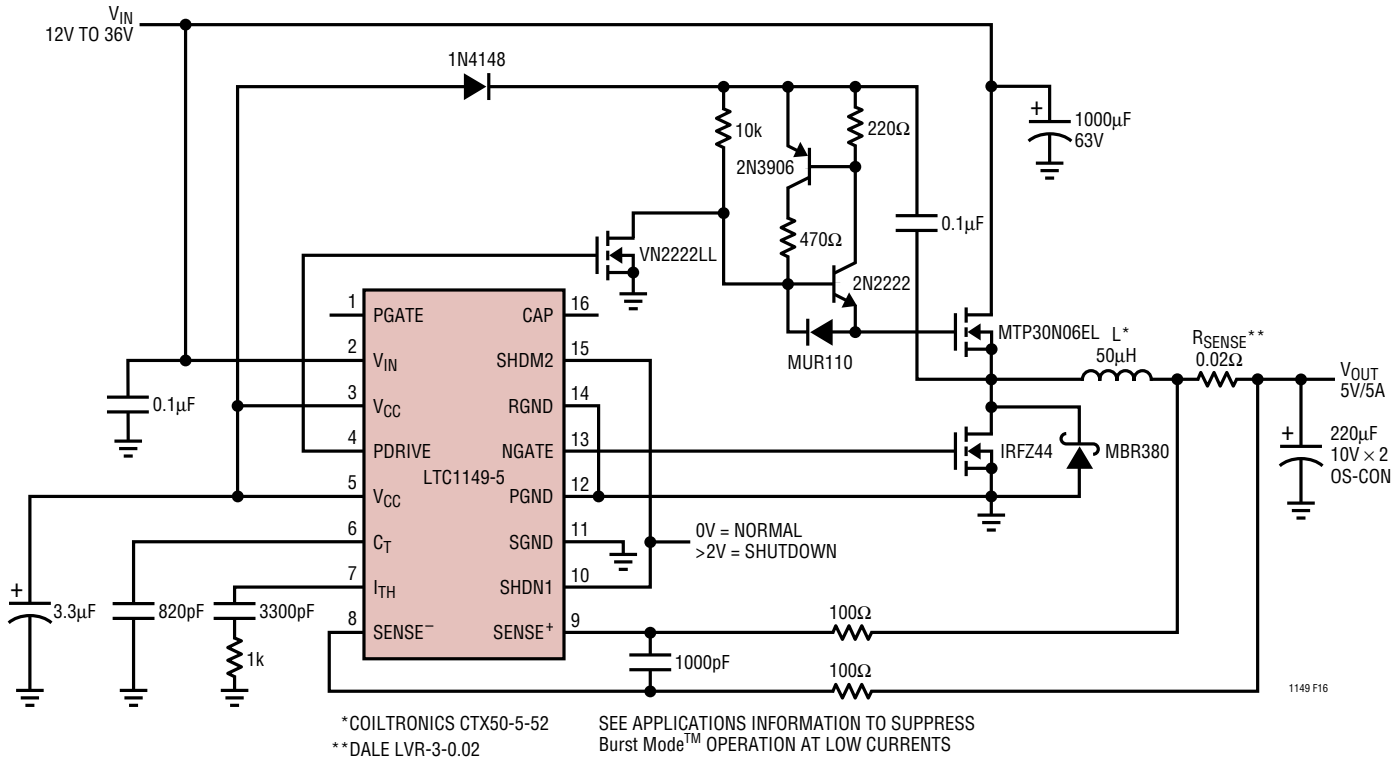
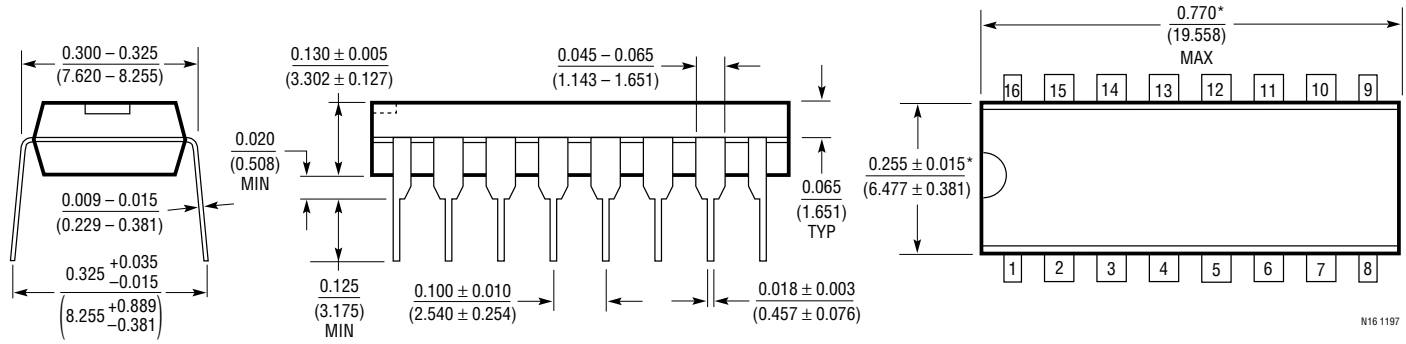


Figure 16. 25W High Efficiency Regulator Using N-Channel MOSFET Switches

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N Package
16-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

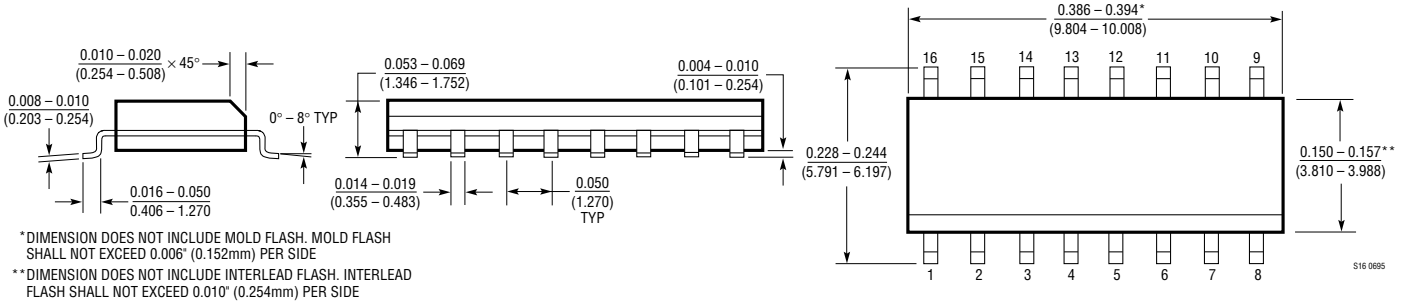


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

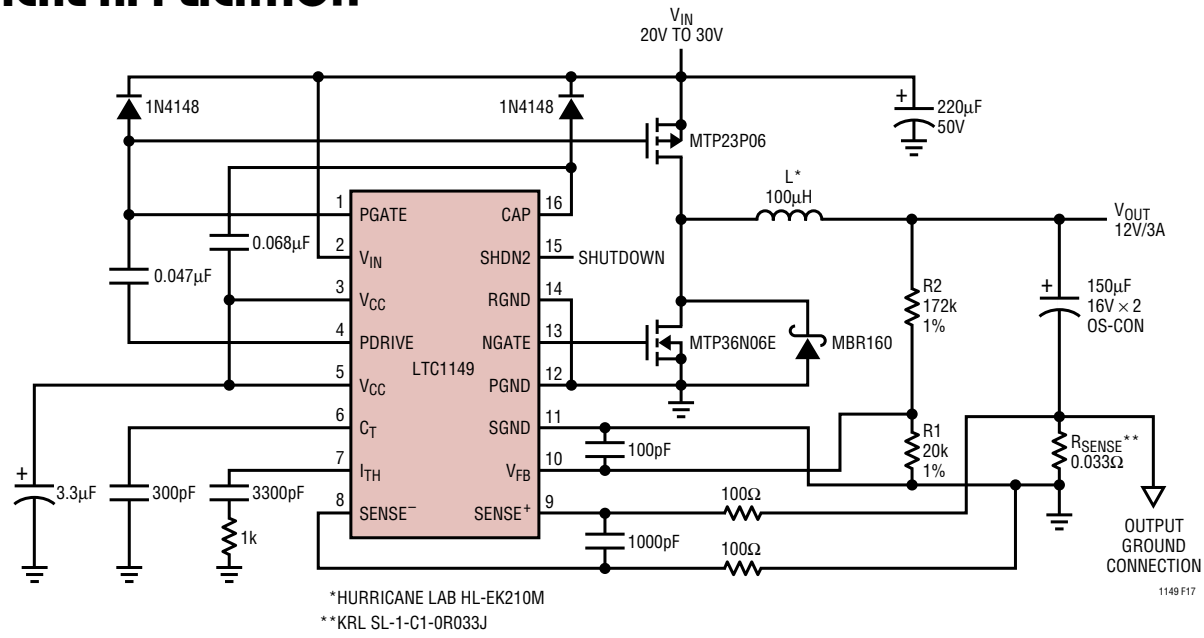
S Package
16-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION



*HURRICANE LAB HL-EK210M

**KRL SL-1-C1-0R033J

Figure 17. High Efficiency 24V Input 12V/3A Output Regulator

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1148HV	High Efficiency, Synchronous Step-Down Switching Regulator	4V < V_{IN} < 20V
LTC1159	High Efficiency, Synchronous Step-Down Switching Regulator	4V < V_{IN} < 40V, $I_{SHUTDOWN}$ = 20µA
LTC1435A	High Efficiency, Low Noise, Synchronous Switching Regulator	3.5V < V_{IN} < 36V, N-Channel Driver
LTC1438	Dual, Low Noise, Synchronous Switching Regulator	3.5V < V_{IN} < 36V, N-Channel Driver

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