THE DATASHEET OF

LTC1753CG#PBF

5-Bit Programmable Synchronous Switching Regulator Controller for Pentium® III Processor

FEATURES

- **5-Bit Digitally Programmable 1.3V to 3.5V Fixed Output Voltage, VRM 8.4 Compliant**
- Fast Transient Response: 0% to 100% Duty Cycle
- Phase Lead Compensation for Remote Sensing
- Overtemperature Protection
- Flags for Power Good and Overvoltage Fault
- 19A Output Current Capability from a 5V Supply
- Dual N-Channel MOSFET Synchronous Driver
- Initial Output Accuracy: ±1.5%
- Excellent Output Accuracy: ±2% Typ Over Line, Load and Temperature Variations
- High Efficiency: Over 95% Possible
- Adjustable Current Limit Without External Sense Resistors
- Available in 20-Lead SSOP and SW Packages

APPLICATIONS

- Power Supply for Pentium® III, AMD-K6®-2, SPARC, ALPHA and PA-RISC Microprocessors
- High Power 5V to 1.3V-3.5V Regulators

DESCRIPTION

The LTC®1753 is a high power, high efficiency switching regulator controller optimized for 5V input to a digitally programmable 1.3V-3.5V output. The internal 5-bit DAC programs the output voltage from 1.3V to 2.05V in 50mV increments and from 2.1V to 3.5V in 100mV increments. The precision internal reference and an internal feedback system provide an output accuracy of ±1.5% at room temperature and typically ±2% over temperature, load current and line voltage shifts. The LTC1753 uses a synchronous switching architecture with two external N-channel output devices, providing high efficiency and eliminating the need for a high power, high cost P-channel device. Additionally, it senses the output current across the on-resistance of the upper N-channel FET, providing an adjustable current limit without an external low value sense resistor.

The LTC1753 free-runs at 300kHz and can be synchronized to a faster external clock if desired. It provides a phase lead compensation scheme and under harsh loading conditions, the PWM duty cycle can be momentarily forced to 0% or 100% to reduce the output voltage recovery time.

TYPICAL APPLICATION

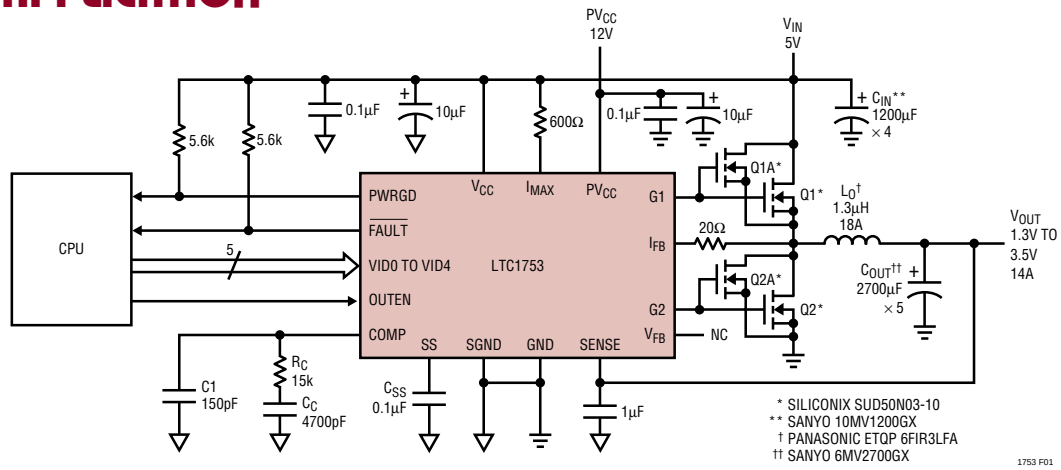


Figure 1. 5V to 1.3V-3.5V Supply Application

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage

V_{CC} 7V

PV_{CC} 14V

Input Voltage

I_{FB} (Note 2) ..... PV_{CC} + 0.3V

I_{MAX} ..... –0.3V to 9V

All Other Inputs ..... –0.3V to (V_{CC} + 0.3V)

Digital Output Voltage ..... –0.3V to 9V

I_{FB} Input Current (Notes 2, 3) ..... –100mA

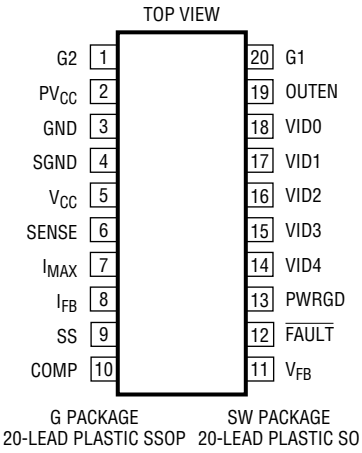
Junction Temperature ..... 125°C

Operating Temperature Range ..... 0°C to 70°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
20-LEAD PLASTIC SSOP

SW PACKAGE
20-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 100°C/ W (G)
T_{JMAX} = 125°C, θ_{JA} = 100°C/ W (SW)

ORDER PART NUMBER

LTC1753CG
LTC1753CSW

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, PV_{CC} = 12V, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	4.5		6	V
PV_{CC}	Supply Voltage for G1, G2		●			13.2	V
V_{FB}	Internal Feedback Voltage	1.3V Output Voltage 2.1V Initial Output Voltage 3.5V Initial Output Voltage			0.5 0.8 1.34		V V V
V_{OUT}	1.3V Initial Output Voltage 1.8V Initial Output Voltage 2.8V Initial Output Voltage 3.5V Initial Output Voltage 1.3V Initial Output Voltage 1.8V Initial Output Voltage 2.8V Initial Output Voltage 3.5V Initial Output Voltage	With Respect to Rated Output Voltage (Figure 2)	 ● ● ● ●	–20 (–1.5%) – 27 (–1.5%) – 42 (–1.5%) – 52 (–1.5%) –26 (–2%) – 36 (–2%) – 56 (–2%) – 70 (–2%)		20 (+1.5%) 27 (+1.5%) 42 (+1.5%) 52 (+1.5%) 26 (+2%) 36 (+2%) 56 (+2%) 70 (+2%)	mV mV mV mV mV mV mV mV
ΔV_{OUT}	Output Load Regulation Output Line Regulation	I_{OUT} = 0 to 14A (Figure 2) V_{IN} = 4.75V to 5.25V, I_{OUT} = 0 (Figure 2)			–5 ±1		mV mV
V_{PWRGD}	Positive Power Good Trip Point Negative Power Good Trip Point	% Above Output Voltage (Note 4) (Figure 2) % Below Output Voltage (Note 4) (Figure 2)	● ●	 –6	3 –3	6	% %
V_{FAULT}	$\overline{FAULT}$ Trip Point	% Above Output Voltage (Note 4) (Figure 2)	●	8	13	18	%
I_{CC}	Operating Supply Current Shutdown Supply Current	OUTEN = V_{CC} = 5V (Note 5)(Figure 3) OUTEN = 0, VID0 to VID4 Floating (Figure 3)	● ●		800 130	1200 250	µA µA
I_{PVCC}	Supply Current	PV_{CC} = 12V, OUTEN = V_{CC} (Note 6) (Figure 3) PV_{CC} = 12V, OUTEN = 0, VID0 to VID4 Floating			15 1		mA µA
f_{OSC}	Internal Oscillator Frequency	(Figure 4)	●	250	300	350	kHz
V_{SAWL}	V_{COMP} at Minimum Duty Cycle	(Note 11)			1.8		V
V_{SAWH}	V_{COMP} at Maximum Duty Cycle	(Note 11)			2.8		V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, PV_{CC} = 12V, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
G_{ERR}	Error Amplifier Open-Loop DC Gain	(Note 7)	●	40	54		dB
g_{mERR}	Error Amplifier Transconductance	(Note 7)	●	0.9	1.6	2.3	millimho
BW_{ERR}	Error Amplifier –3dB Bandwidth	COMP = Open (Note 11)			400		kHz
I_{IMAX}	I_{MAX} Sink Current	$V_{IMAX} = V_{CC}$	●	150	190	230	µA
I_{SS}	Soft-Start Source Current	V_{SS} = 0V, V_{IMAX} = 0V, $V_{IFB} = V_{CC}$	●	–16	–12	–8	µA
I_{SSIL}	Maximum Soft-Start Sink Current Under Current Limit	$V_{SENSE} = V_{OUT}$, $V_{IMAX} = V_{CC}$, V_{IFB} = 0V (Notes 8, 9), $V_{SS} = V_{CC}$	●	30	60	150	µA
I_{SSHIL}	Soft-Start Sink Current Under Hard Current Limit	V_{SENSE} = 0V, $V_{IMAX} = V_{CC}$, V_{IFB} = 0V	●	20	45		mA
t_{SSHIL}	Hard Current Limit Hold Time	V_{SENSE} = 0V, V_{IMAX} = 4V, $V_{IFB}\downarrow$ from 5V			500		µs
t_{PWRGD}	Power Good Response Time↑	$V_{SENSE}\uparrow$ from 0V to Rated V_{OUT}	●	0.5	1	2	ms
t_{PWRBAD}	Power Good Response Time↓	$V_{SENSE}\downarrow$ from Rated V_{OUT} to 0V	●	200	500	1000	µs
t_{FAULT}	$\overline{FAULT}$ Response Time	$V_{SENSE}\uparrow$ from Rated V_{OUT} to V_{CC}	●	200	500	1000	µs
V_{OTDD}	Overtemperature Driver Disable	OUTEN↓, VID0 to VID4 = 0 (Note 10) (Figure 3)	●	1.6	1.7	1.8	V
V_{SHDN}	Shutdown	OUTEN↓, VID0 to VID4 = 0 (Note 10) (Figure 3)	●			0.8	V
t_r, t_f	Driver Rise and Fall Time	(Figure 4)	●		90	150	ns
t_{NOL}	Driver Nonoverlap Time	(Figure 4)	●	30	100		ns
V_{IH}	VID0 to VID4 Input High Voltage		●	2			V
V_{IL}	VID0 to VID4 Input Low Voltage		●			0.8	V
R_{SENSE}	SENSE Input Resistance				108		kΩ
R_{VID}	VID0 to VID4 Internal Pull-Up Resistance		●	10	20		kΩ
V_{OL}	Digital Output Low Voltage	I_{SINK} = 1.6mA, Measured at PWRGD and $\overline{FAULT}$	●		0.1	0.4	V
I_{SINK}	Digital Output Sink Current		●			10	mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: When I_{FB} is taken below GND, it will be clamped by an internal diode. This pin can handle input currents greater than 100mA below GND without latchup. In the positive direction, it is not clamped to V_{CC} or PV_{CC}.

Note 3: All currents into device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: The Power Good and $\overline{FAULT}$ trip thresholds are tested at the 1.8V output voltage code. The Power Good and $\overline{FAULT}$ trip thresholds are guaranteed by design for all other output voltage codes to the same specification.

Note 5: The LTC1753 goes into the shutdown mode if VID0 to VID4 are floating. Due to the internal pull-up resistors, there will be an additional 0.25mA/pin if any of the VID0 to VID4 pins are pulled low.

Note 6: Supply current in normal operation is dominated by the current needed to charge and discharge the external FET gates. This will vary with the LTC1753 operating frequency, supply voltage and the external FETs used.

Note 7: The open-loop DC gain and transconductance from the SENSE pin to COMP pin will be $(G_{ERR})(1.26/3.3)$ and $(g_{mERR})(1.26/3.3)$ respectively.

Note 8: The current limiting amplifier can sink but cannot source current. Under normal (not current limited) operation, the output current will be zero.

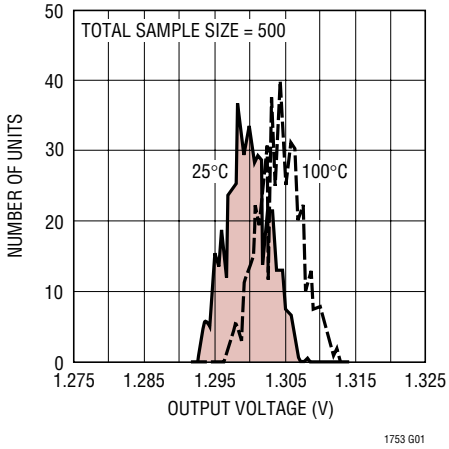
Note 9: Under typical soft current limit, the net soft-start discharge current will be 60µA (I_{SSIL}) + [–12µA(I_{SS})] ≅ 48µA. The soft-start sink-to-source current ratio is designed to be 5:1.

Note 10: When VID0 to VID4 are all HIGH, the LTC1753 will be forced to shut down internally. The OUTEN trip voltages are guaranteed by design for all other input codes.

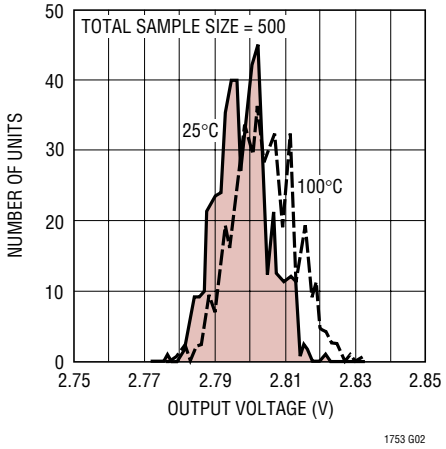
Note 11: This parameter is guaranteed by design and correlation and is not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS

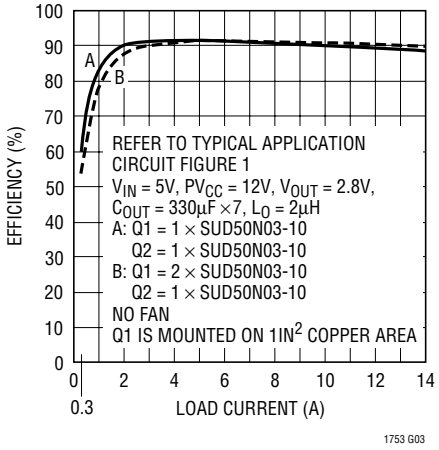
Typical 1.3V V_{OUT} Distribution



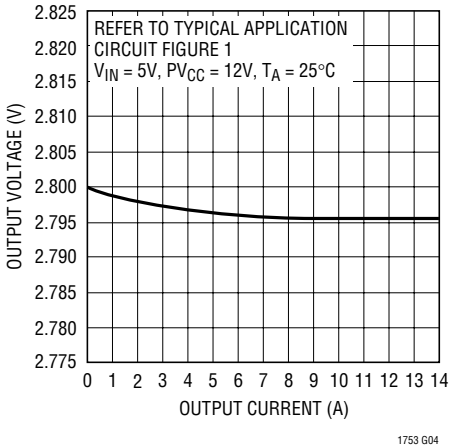
Typical 2.8V V_{OUT} Distribution



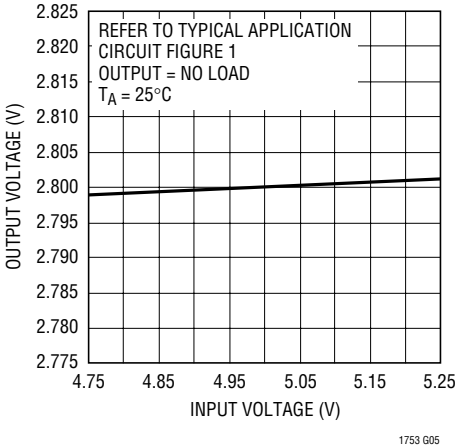
Efficiency vs Load Current



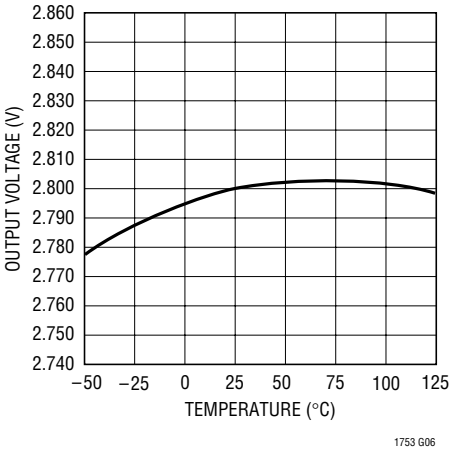
Load Regulation



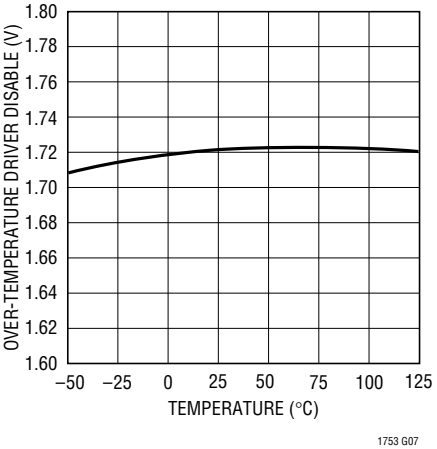
Line Regulation



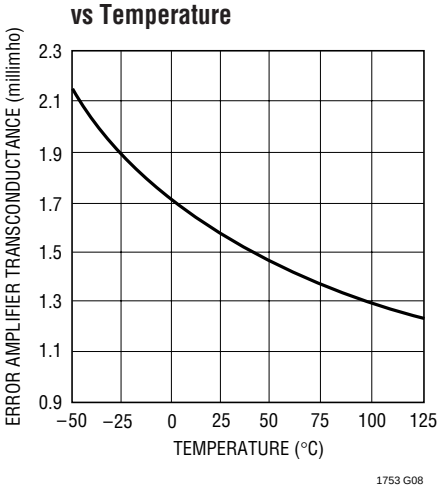
Output Temperature Drift



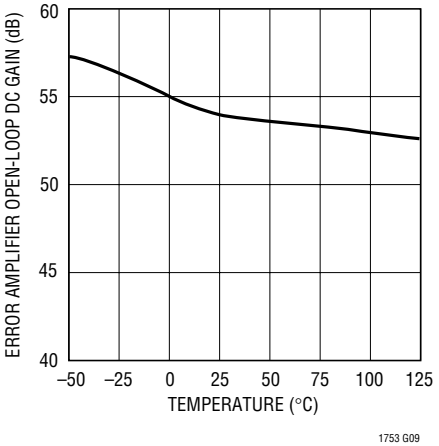
Overtemperature Driver Disable vs Temperature



Error Amplifier Transconductance vs Temperature

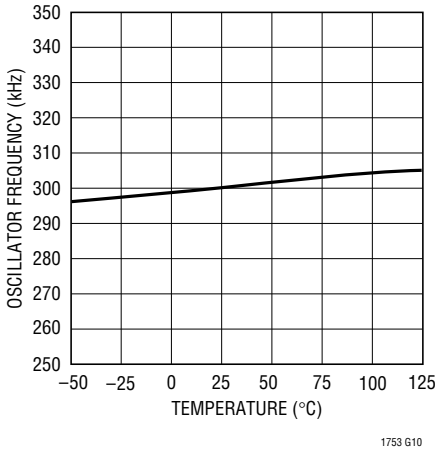


Error Amplifier Open-Loop DC Gain vs Temperature

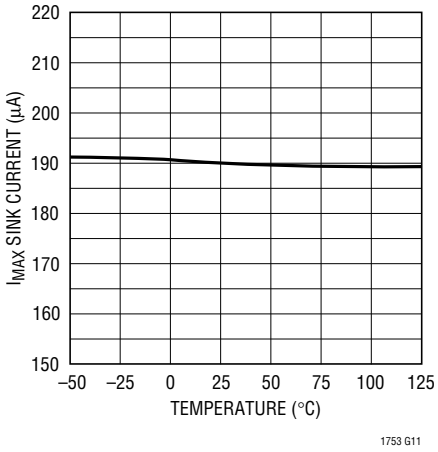


TYPICAL PERFORMANCE CHARACTERISTICS

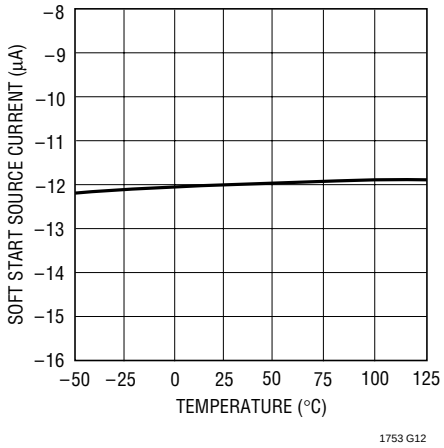
Oscillator Frequency vs Temperature



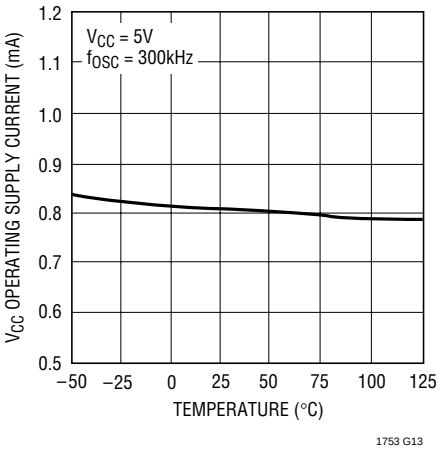
I_{MAX} Sink Current vs Temperature



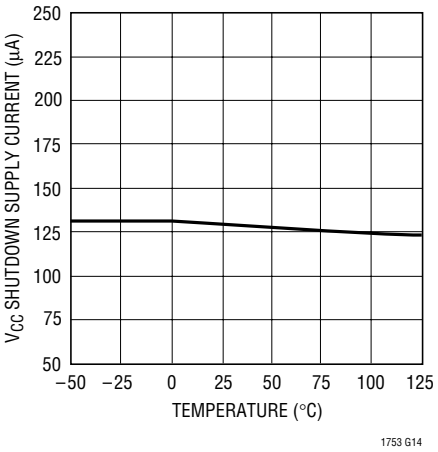
Soft-Start Source Current vs Temperature



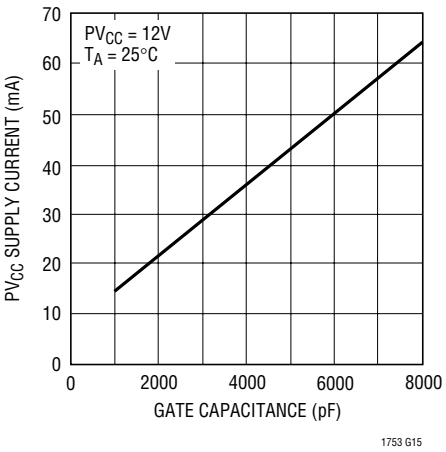
V_{CC} Operating Supply Current vs Temperature



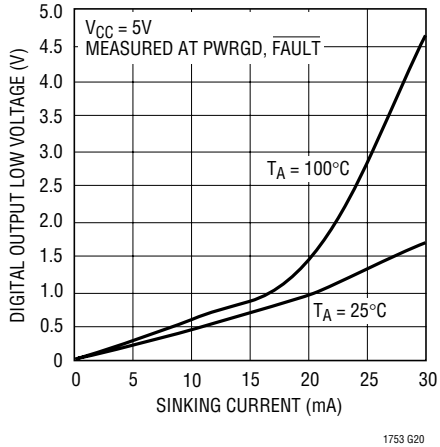
V_{CC} Shutdown Supply Current vs Temperature



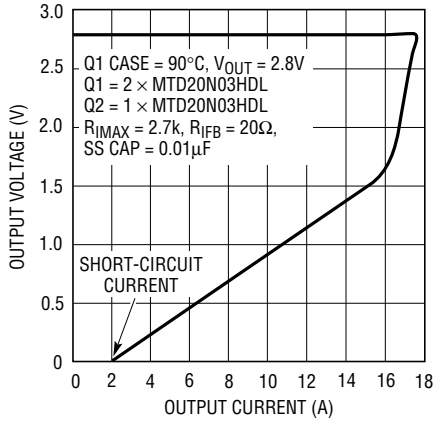
PV_{CC} Supply Current vs Gate Capacitance



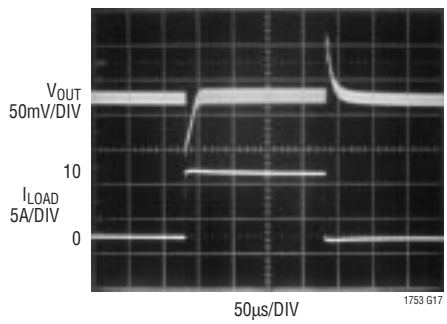
Digital Output Low Voltage vs Sink Current



Output Over Current Protection

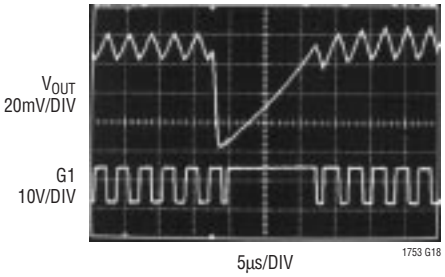


Transient Response, V_{OUT} = 2.8V

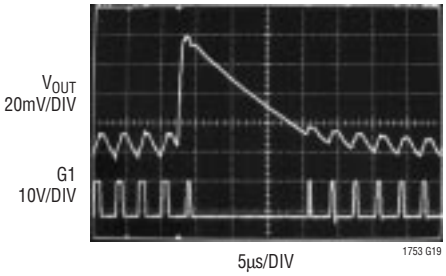


TYPICAL PERFORMANCE CHARACTERISTICS

Expanded View of Undershoot Illustrates 100% Duty Cycle Operation, V_{OUT} = 2.8V



Expanded View of Overshoot Illustrates 0% Duty Cycle Operation, V_{OUT} = 2.8V



PIN FUNCTIONS

G2 (Pin 1): Gate Drive for the Lower N-Channel MOSFET, Q2. This output will swing from PV_{CC} to GND. It will always be low when G1 is high or when the output is disabled. To prevent undershoot during a soft-start cycle, G2 is held low until G1 first goes high.

PV_{CC} (Pin 2): Power Supply for G1 and G2. PV_{CC} must be connected to a potential of at least V_{IN} + $V_{GS(ON)Q1}$. For normal applications, connect PV_{CC} to a 12V power supply or generate PV_{CC} using a simple charge pump.

GND (Pin 3): Power Ground. GND should be connected to a low impedance ground plane in close proximity to the source of Q2.

SGND (Pin 4): Signal Ground. SGND is connected to the low power internal circuitry and should be connected to the negative terminal of the output capacitor where it returns to the ground plane. GND and SGND should be shorted directly at the LTC1753.

V_{CC} (Pin 5): Power Supply. Power for the internal low power circuity. V_{CC} should be wired separately from the drain of Q1 if they share the same supply. A 10µF bypass capacitor is recommended from this pin to SGND.

SENSE (Pin 6): Output Voltage Pin. Connect to the positive terminal of the output capacitor. There is an internal 108k resistor connected from this pin to SGND. SENSE is a very sensitive pin; for optimum performance, connect an external 1µF capacitor from this pin to SGND. By connecting a small external resistor between the output capacitor and the SENSE pin, the initial output voltage can be raised slightly. Since the internal divider has a nominal impedance of 108kΩ, a 1100Ω series resistor will raise the nominal output voltage by 1%. If an external resistor is used, the value of the 1µF capacitor on the SENSE pin must be greatly reduced or loop phase margin will suffer. Set a time constant for the RC combination of approximately 0.1µs. So, for example, with a 1100Ω resistor, set C = 90pF. Use a standard 100pF capacitor. In addition, LTC recommends that the 1µF capacitor be connected from the top of the additional external resistor directly to SGND.

I_{MAX} (Pin 7): Current Limit Threshold. Current limit is set by the voltage drop across an external resistor connected between the drain of Q1 and I_{MAX}. There is a 190µA internal pull-down at I_{MAX}.

I_{FB} (Pin 8): Current Limit Sense Pin. Connect to the switching node between the source of Q1 and the drain of Q2. If I_{FB} drops below I_{MAX} when G1 is on, the LTC1753 will go into current limit. The current limit circuit can be disabled by floating I_{MAX} and shorting I_{FB} to V_{CC}.

SS (Pin 9): Soft-Start. Connect to an external capacitor to implement a soft-start function. During moderate overload conditions, the soft-start capacitor will be discharged slowly in order to reduce the duty cycle. In hard current limit, the soft-start capacitor will be forced low immediately and the LTC1753 will rerun a complete soft-start cycle. C_{SS} must be selected such that during power-up the current through Q1 will not exceed the current limit value.

PIN FUNCTIONS

COMP (Pin 10): External Compensation. The COMP pin is connected directly to the output of the error amplifier and the input of the PWM comparator. An RC + C network is used at this node to compensate the feedback loop to provide optimum transient response.

V_{FB} (Pin 11): Voltage Feedback. V_{FB} is the tap point of the internal resistor divider connected from SENSE to SGND. During rapid and heavy output loading conditions, a small capacitor between the SENSE and V_{FB} pin creates a feedforward path that reduces the transient recovery time. For applications where extremely low output ripple is required, low ESR capacitors are typically used. In this case, a small capacitor between SENSE and V_{FB} helps to compensate the switching loop. This pin can be left floating, but should be isolated from high current switching nodes.

$\overline{\text{FAULT}}$ (Pin 12): Overvoltage Fault. $\overline{\text{FAULT}}$ is an open-drain output. If V_{OUT} reaches 13% above the nominal output voltage, $\overline{\text{FAULT}}$ will go low and G1 and G2 will be disabled. Once triggered, the LTC1753 will remain in this state until the power supply is recycled or the OUTEN pin is toggled. If OUTEN = 0, $\overline{\text{FAULT}}$ floats or is pulled high by an external resistor.

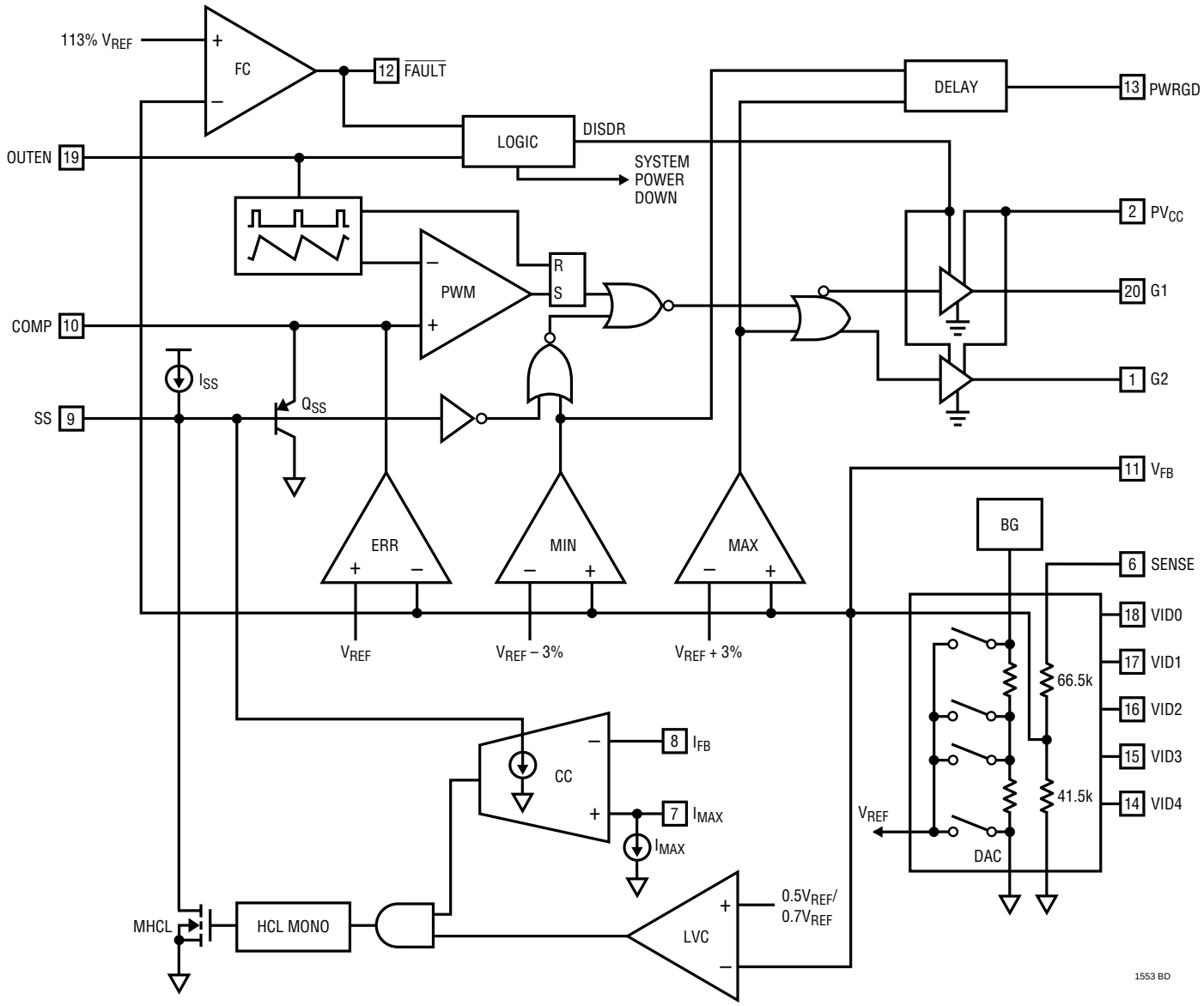
PWRGD (Pin 13): Power Good. This is an open-drain signal to indicate validity of output voltage. A high indicates that the output has settled to within ±3% of the rated output for more than 1ms. PWRGD will go low if the output is out of regulation for more than 500µs. If OUTEN = 0, PWRGD pulls low.

VID0, VID1, VID2, VID3, VID4 (Pins 18, 17, 16, 15, 14): Digital Voltage Select. TTL inputs used to set the regulated output voltage required by the processor (Table 2). There is an internal 20kΩ pull-up at each pin. When all five VID_n pins are high or floating, the chip will shut down.

OUTEN (Pin 19): Output Enable. TTL input which enables the output voltage. The external MOSFET temperature can be monitored with an external thermistor as shown in Figure 11. When the OUTEN input voltage drops below 1.7V, the drivers are internally disabled to prevent the MOSFETs from heating further. If OUTEN is less than 1.2V for longer than 30µs, the LTC1753 will enter shutdown mode. The internal oscillator can be synchronized to a faster external clock by applying the external clocking signal to the OUTEN pin. (See Applications Information.)

G1 (Pin 20): Gate Drive for the Upper N-Channel MOSFET, Q1. This output will swing from PV_{CC} to GND. It will always be low when G2 is high or the output is disabled.

BLOCK DIAGRAM



TEST CIRCUITS

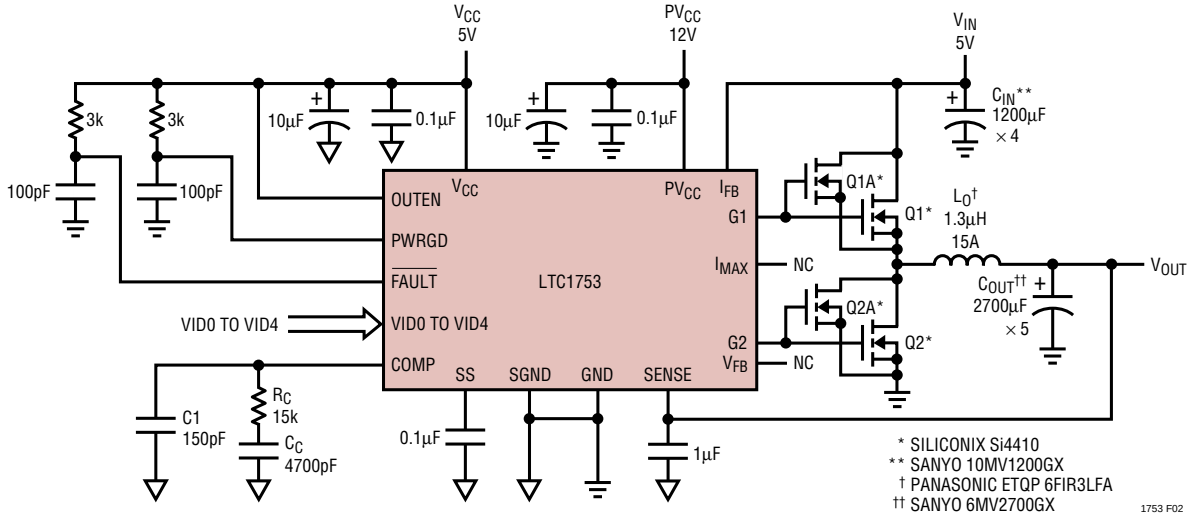


Figure 2

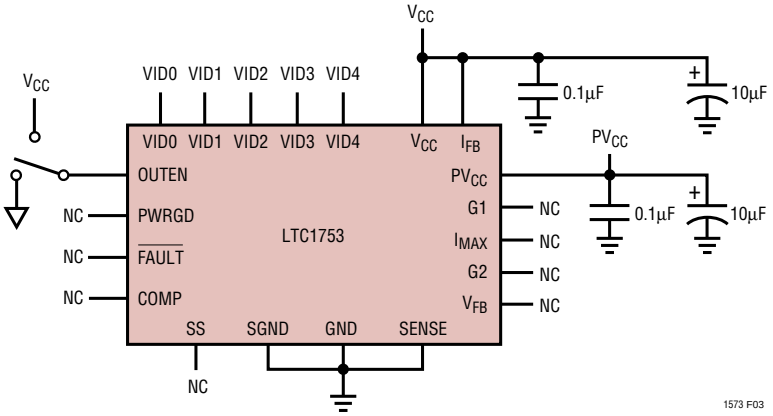


Figure 3

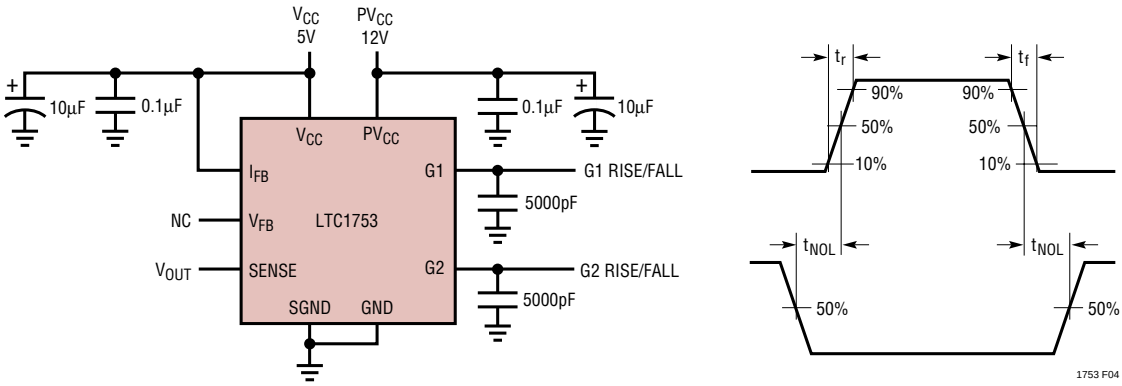


Figure 4

FUNCTION TABLES

Table 1. PWRGD and $\overline{FAULT}$ Logic

INPUT		OUTPUT*	
OUTEN	V_{SENSE}**	$\overline{FAULT}$	PWRGD
0	X	1	0
1	< 97%	1	0
1	> 97% < 103%	1	1
1	>103%	1	0
1	> 113%	0	0

Table 2. Rated Output Voltage

INPUT PIN					RATED OUTPUT VOLTAGE (V)
V_{ID4}	V_{ID3}	V_{ID2}	V_{ID1}	V_{ID0}	
0	1	1	1	1	1.30
0	1	1	1	0	1.35
0	1	1	0	1	1.40
0	1	1	0	0	1.45
0	1	0	1	1	1.50
0	1	0	1	0	1.55
0	1	0	0	1	1.60
0	1	0	0	0	1.65
0	0	1	1	1	1.70
0	0	1	1	0	1.75
0	0	1	0	1	1.80
0	0	1	0	0	1.85

Table 2. Rated Output Voltage (cont)

INPUT PIN					RATED OUTPUT VOLTAGE (V)
V_{ID4}	V_{ID3}	V_{ID2}	V_{ID1}	V_{ID0}	
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05
1	1	1	1	1	SHDN
1	1	1	1	0	2.1
1	1	1	0	1	2.2
1	1	1	0	0	2.3
1	1	0	1	1	2.4
1	1	0	1	0	2.5
1	1	0	0	1	2.6
1	1	0	0	0	2.7
1	0	1	1	1	2.8
1	0	1	1	0	2.9
1	0	1	0	1	3.0
1	0	1	0	0	3.1
1	0	0	1	1	3.2
1	0	0	1	0	3.3
1	0	0	0	1	3.4
1	0	0	0	0	3.5

* With external pull-up resistor
** With respect to the output voltage selected in Table 2
X Don't care

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OVERVIEW

The LTC1753 is a voltage feedback, synchronous switching regulator controller (see Block Diagram) designed for use in high power, low voltage step-down (buck) converters. It includes an on-chip DAC to control the output voltage, a PWM generator, a precision reference trimmed to ±1%, two high power MOSFET gate drivers and all the necessary feedback and control circuitry to form a complete switching regulator circuit.

The LTC1753 includes a current limit sensing circuit that uses the upper external power MOSFET as a current sensing element, eliminating the need for an external sense resistor. Once the current comparator, CC, detects an overcurrent condition, the duty cycle is reduced by discharging the soft-start capacitor through a voltage-controlled current source. Under severe overloads or output short circuit conditions, the chip will be repeatedly forced into soft-start until the short is removed, preventing the external components from being damaged. Under output overvoltage conditions, the MOSFET drivers will be disabled permanently until the chip power supply is recycled or the OUTEN pin is toggled.

OUTEN can optionally be connected to an external negative temperature coefficient (NTC) thermistor placed near the external MOSFETs or the microprocessor. Two threshold levels are provided internally. When OUTEN drops to 1.7V, the G1 and G2 pins will be forced low. If OUTEN is pulled below 1.2V, the LTC1753 will go into shutdown mode, cutting the supply current to a minimum. If thermal shutdown is not required, OUTEN can be connected to a

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conventional TTL enable signal. The free-running 300kHz PWM frequency can be synchronized to a faster external clock connected to OUTEN. Adjusting the oscillator frequency can add flexibility in the external component selection. See the Clock Synchronization section.

Output regulation can be monitored with the PWRGD pin which in turn monitors the internal MIN and MAX comparators. If the output is ±3% beyond the selected value for more than 500µs, the PWRGD output will be pulled low. Once the output has settled within ±3% of the selected value for more than 1ms, PWRGD will return high.

THEORY OF OPERATION

Primary Feedback Loop

The regulator output voltage at the SENSE pin is divided down internally by a resistor divider with a total resistance of approximately 108k. This divided down voltage is subtracted from a reference voltage supplied by the DAC output. The resulting error voltage is amplified by the error amplifier and the output is compared to the oscillator ramp waveform by the PWM comparator. This PWM signal controls the external MOSFETs through G1 and G2. The resulting chopped waveform is filtered by L_O and C_{OUT} closing the loop. Loop frequency compensation is achieved with an external RC + C network at the COMP pin, which is connected to the output node of the transconductance amplifier. In low output ripple voltage applications, low ESR output capacitors are typically used. Under this condition, a capacitor between the SENSE and V_{FB} pins helps compensate the switching loop. For heavy transient output loading applications, a small capacitor between the SENSE and V_{FB} pin acts as a feedforward path and helps reduce the transient recovery time.

MIN, MAX Feedback Loops

Two additional comparators in the feedback loop provide high speed fault correction in situations where the ERR amplifier may not respond quickly enough. MIN compares the feedback signal V_{FB} to a voltage 3% below the internal reference. If V_{FB} is lower than the threshold of this comparator, the MIN comparator overrides the ERR amplifier and forces the loop to 100% duty cycle. Similarly, the MAX comparator forces the output to 0% duty cycle if V_{FB} is more than 3% above the internal reference. To prevent these two comparators from triggering due to noise, output voltage ripple must be controlled with sufficient output bypassing to prevent jitter. In addition, the MIN and MAX comparators' response times are deliberately controlled so that they take about one microsecond to respond. These two comparators help prevent extreme output perturbations with fast output transients, while allowing the main feedback loop to be optimally compensated for stability.

Soft-Start and Current Limit

The LTC1753 includes a soft-start circuit which is used for initial start-up and during current limit operation. The SS pin requires an external capacitor to GND with the value determined by the required soft-start time. An internal 12µA current source is included to charge the external SS capacitor. During start-up, the COMP pin is clamped to a diode drop above the voltage at the SS pin. This prevents the error amplifier, ERR, from forcing the loop to 100% duty cycle. The LTC1753 will begin to operate at low duty cycle as the SS pin rises above about 1.2V ($V_{COMP} \approx 1.8V$). As SS continues to rise, Q_{SS} turns off and the error amplifier begins to regulate the output. The MIN comparator is disabled when soft-start is active to prevent it from overriding the soft-start function.

The LTC1753 includes yet another feedback loop to control operation in current limit. Just before every falling edge of G1, the current comparator, CC, samples and holds the voltage drop measured across the external MOSFET, Q1, at the I_{FB} pin. CC compares the voltage at I_{FB} to the voltage at the I_{MAX} pin. As the peak current rises, the measured voltage across Q1 increases due to the drop across the $R_{DS(ON)}$ of Q1. When the voltage at I_{FB} drops below I_{MAX}, indicating that Q1's drain current has exceeded the maximum level, CC starts to pull current out of the external soft-start capacitor, cutting the duty cycle and controlling the output current level. The CC comparator pulls current out of the SS pin in proportion to the voltage difference between I_{FB} and I_{MAX}. Under minor overload conditions, the SS pin will fall gradually, creating a time delay before current limit takes effect. Very short, mild

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Table 3. Recommended R_{IMAX} Resistor (kΩ) vs Maximum Operating Load Current and External MOSFET Q1

MAXIMUM OPERATING LOAD CURRENT (A)	Si4410	Si4410 (TWO IN PARALLEL)	SUD50N03	MTD20N03 (TWO IN PARALLEL)
8	820	430	680	1k
10	1.2k	560	820	1.2k
12	—	680	1k	1.5k
14	—	820	1.2k	1.8k
16	—	910	1.5k	2.0k
18	—	1.2k	—	2.2k

overloads may not affect the output voltage at all. More significant overload conditions will allow the SS pin to reach a steady state, and the output will remain at a reduced voltage until the overload is removed. Serious overloads will generate a large overdrive at CC, allowing it to pull SS down quickly and preventing damage to the output components.

By using the $R_{DS(ON)}$ of Q1 to measure the output current, the current limiting circuit eliminates an expensive discrete sense resistor that would otherwise be required. This helps minimize the number of components in the high current path. Due to switching noise and variation of $R_{DS(ON)}$, the actual current limit trip point is not highly accurate. The current limiting circuitry is primarily meant to prevent damage to the power supply circuitry during fault conditions. The exact current level where the limiting circuit begins to take effect will vary from unit to unit as the $R_{DS(ON)}$ of Q1 varies.

For a given current limit level, the external resistor from I_{MAX} to V_{IN} can be determined by:

$$R_{IMAX} = \frac{(I_{LMAX})(R_{DS(ON)Q1})}{I_{IMAX}}$$

where,

$$I_{LMAX} = I_{LOAD} + \frac{I_{RIPPLE}}{2}$$

I_{LOAD} = Maximum load current
I_{RIPPLE} = Inductor ripple current

$$= \frac{(V_{IN} - V_{OUT})(V_{OUT})}{(f_{OSC})(L_O)(V_{IN})}$$

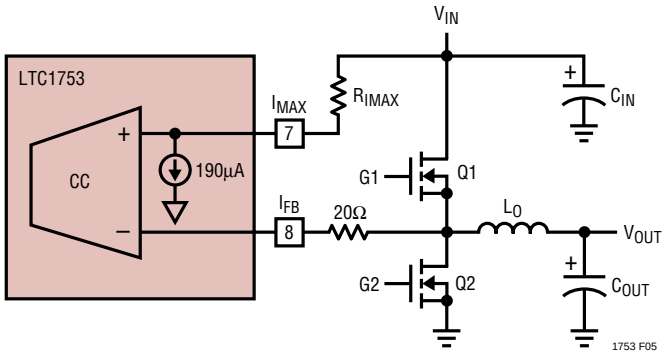

Figure 5. Current Limit Setting

f_{OSC} = LTC1753 oscillator frequency = 300kHz
L_O = Inductor value
$R_{DS(ON)Q1}$ = Hot on-resistance of Q1 at I_{LMAX}
I_{IMAX} = Internal 190µA sink current at I_{MAX}

OUTEN and Thermistor Input

The LTC1753 includes a low power shutdown mode, controlled by the logic at the OUTEN pin. A high at OUTEN allows the part to operate normally. A low level at OUTEN stops all internal switching, pulls COMP and SS to ground internally and turns Q1 and Q2 off. PWRGD is pulled low, and $\overline{FAULT}$ is left floating. In shutdown, the LTC1753 quiescent current drops to about 130µA. The residual current is used to keep the thermistor sensing circuit at OUTEN alive. Note that the leakage current of the external MOSFETs may add to the total shutdown current consumed by the circuit, especially at elevated temperatures.

OUTEN is designed with two thresholds to allow it to also be utilized for overtemperature protection. The power MOSFET operating temperature can be monitored with an external negative temperature coefficient (NTC) thermistor

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mounted next to the external MOSFET which is expected to run the hottest—often the high-side device, Q1. Electrically, the thermistor should form a voltage divider with another resistor, R1, connected to V_{CC}. Their midpoint should be connected to OUTEN (see Figure 6). As the temperature increases, the OUTEN pin voltage is reduced. Under normal operating conditions, the OUTEN pin should stay above 1.7V and all circuits will function normally. If the temperature gets abnormally high, the OUTEN pin voltage will eventually drop below 1.7V, the LTC1753 disables both FET drivers. If OUTEN decreases below 1.2V, the LTC1753 enters shutdown mode. To activate any of these three modes, the OUTEN voltage must drop below the respective threshold for longer than 30µs.

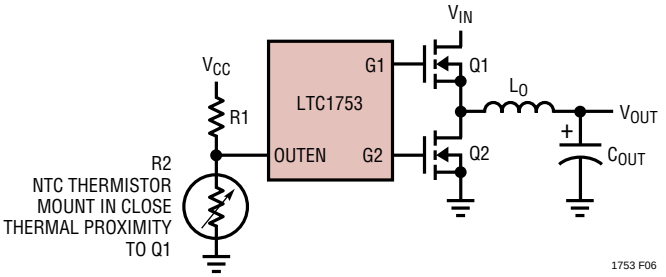

Figure 6. OUTEN Pin as a Thermistor Input

Clock Synchronization

The internal oscillator can be synchronized to an external clock by applying the external clocking signal to the OUTEN pin. The synchronizing range extends from the initial operating frequency up to 500kHz. If the external frequency is much higher than the natural free-running frequency, the peak-to-peak sawtooth amplitude within the LTC1753 will decrease. Since the loop gain is inversely proportional to the amplitude of the sawtooth, the compensation network may need to be adjusted slightly. Note that the temperature sensing circuitry does not operate when external synchronization is used.

MOSFET Gate Drive

Power for the internal MOSFET drivers is supplied by PV_{CC}. This supply must be above the input supply voltage by at least one power MOSFET $V_{GS(ON)}$ for efficient operation. For a typical application, PV_{CC} should be connected to a 12V power supply.

If the OUTEN pin is low, G1 and G2 are both held low to prevent output voltage undershoot. As V_{CC} and PV_{CC} power up from a 0V condition, an internal undervoltage lockout circuit prevents G1 and G2 from going high until V_{CC} reaches about 3.5V. If V_{CC} powers up while PV_{CC} is at ground potential, the SS is forced to ground potential internally. SS clamps the COMP pin low and prevents the drivers from turning on. On power-up or recovery from thermal shutdown, the drivers are designed such that G2 is held low until G1 first goes high.

Power MOSFETs

Two N-channel power MOSFETs are required for most LTC1753 circuits. Logic level MOSFETs should be used and they should be selected based on on-resistance and GATE threshold voltage considerations. $R_{DS(ON)}$ should be chosen based on input and output voltage, allowable power dissipation and maximum required output current. GATE threshold voltages for logic level MOSFETs are lower than standard MOSFETs. A MOSFET whose $R_{DS(ON)}$ is rated at V_{GS} = 4.5V does not necessarily have a logic level MOSFET GATE threshold voltage. Using standard MOSFETs instead of logic level MOSFETs can cause start-up problems, especially if PV_{CC} is derived from a charge pump scheme. In a typical LTC1753 buck converter circuit the average inductor current is equal to the output load current. This current is always flowing through either Q1 or Q2 with the power dissipation split up according to the duty cycle:

$$DC(Q1) = \frac{V_{OUT}}{V_{IN}}$$

$$DC(Q2) = 1 - \frac{V_{OUT}}{V_{IN}} = \frac{(V_{IN} - V_{OUT})}{V_{IN}}$$

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The $R_{DS(ON)}$ required for a given conduction loss can now be calculated by rearranging the relation $P = I^2R$.

$$R_{DS(ON)Q1} = \frac{P_{MAX(Q1)}}{[DC(Q1)](I_{MAX})^2} = \frac{(V_{IN})[P_{MAX(Q1)}]}{(V_{OUT})(I_{MAX})^2}$$

$$R_{DS(ON)Q2} = \frac{P_{MAX(Q2)}}{[DC(Q2)](I_{MAX})^2} = \frac{(V_{IN})[P_{MAX(Q2)}]}{(V_{IN} - V_{OUT})(I_{MAX})^2}$$

P_{MAX} should be calculated based primarily on required efficiency or allowable thermal dissipation. A typical high efficiency circuit designed with a 5V input and a 2.8V, 11.2A output might allow no more than 4% efficiency loss at full load for each MOSFET. Assuming roughly 90% efficiency at this current level, this gives a P_{MAX} value of:

[(2.8)(11.2A/0.9)(0.04)] = 1.39W per FET

and a required $R_{DS(ON)}$ of:

$$R_{DS(ON)Q1} = \frac{(5V)(1.39W)}{(2.8V)(11.2A)^2} = 0.019\Omega$$

$$R_{DS(ON)Q2} = \frac{(5V)(1.39W)}{(5V - 2.8V)(11.2A)^2} = 0.025\Omega$$

Note also that while the required $R_{DS(ON)}$ values suggest large MOSFETs, the dissipation numbers are only 1.39W per device or less—large TO-220 packages and heat sinks are not necessarily required in high efficiency applications. Siliconix Si4410DY or International Rectifier IRF7413 (both in SO-8) or Siliconix SUD50N03 or Motorola MTD20N03HDL (both in D PAK) are small footprint surface mount devices with $R_{DS(ON)}$ values below 0.03Ω at 5V of gate drive that work well in LTC1753 circuits. With higher output voltages, the $R_{DS(ON)}$ of Q1 may need to be significantly lower than that for Q2. These conditions can often be met by paralleling two MOSFETs for Q1 and using a single device for Q2. Note that using a higher P_{MAX} value

Table 4. Recommended MOSFETs for LTC1753 Applications

PARTS	$R_{DS(ON)}$ AT 25°C (mΩ)	RATED CURRENT (A)	TYPICAL INPUT CAPACITANCE C_{ISS} (pF)	θ_{JC} (°C/W)	T_{JMAX} (°C)
Siliconix SUD50N03-10 D-PAK	19	15 at 25°C 10 at 100°C	3200	1.8	175
Siliconix Si4410DY SO-8	20	10 at 25°C 8 at 75°C	2700	—	150
ON Semiconductor MTD20N03HDL D PAK	35	20 at 25°C 16 at 100°C	880	1.67	150
Fairchild FDS6670A SO-8	8	13 at 25°C	3200	25	150
Fairchild FDS6680 SO-8	10	11.5 at 25°C	2070	25	150
ON Semiconductor MTB75N03HDL DD PAK	7.5	75 at 25°C 59 at 100°C	4025	1.0	150
IR IRL3103S DD PAK	14	56 at 25°C 40 at 100°C	1600	1.8	175
IR IRLZ44 TO-220	28	50 at 25°C 36 at 100°C	3300	1.0	175
Fuji 2SK1388 TO-220	37	35 at 25°C	1750	2.08	150

Note: Please refer to the manufacturer's data sheet for testing conditions and detail information.

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in the $R_{DS(ON)}$ calculations will generally decrease MOSFET cost and circuit efficiency while increasing MOSFET heat sink requirements.

Inductor Selection

The inductor is often the largest component in the LTC1753 design and should be chosen carefully. Inductor value and type should be chosen based on output slew rate requirements, output ripple requirements and expected peak current. Inductor value is primarily controlled by the required current slew rate. The maximum rate of rise of current in the inductor is set by its value, the input-to-output voltage differential and the maximum duty cycle of the LTC1753. In a typical 5V input, 2.8V output application, the maximum current slew rate will be:

$$DC_{MAX}\frac{(V_{IN}-V_{OUT})}{L}=\frac{1.83}{L}\quad\frac{A}{\mu s}$$

where L is the inductor value in μH. With proper frequency compensation, the combination of the inductor and output capacitor will determine the transient recovery time. In general, a smaller value inductor will improve transient response at the expense of increased output ripple voltage and inductor core saturation rating. A 2μH inductor would have a 0.9A/μs rise time in this application, resulting in a 5.5μs delay in responding to a 5A load current step. During this 5.5μs, the difference between the inductor current and the output current must be made up by the output capacitor, causing a temporary voltage droop at the output. To minimize this effect, the inductor value should usually be in the 1μH to 5μH range for most typical 5V input LTC1753 circuits. To optimize performance, different combinations of input and output voltages and expected loads may require different inductor values.

Once the required value is known, the inductor core type can be chosen based on peak current and efficiency requirements. Peak current in the inductor will be equal to the maximum output load current plus half of the peak-to-peak inductor ripple current. Ripple current is set by the inductor value, the input and output voltage and the operating frequency. The ripple current is approximately equal to:

$$I_{RIPPLE}=\frac{(V_{IN}-V_{OUT})(V_{OUT})}{(f_{OSC})(L_O)(V_{IN})}$$

f_{OSC} = LTC1753 oscillator frequency = 300kHz
L_O = Inductor value

Solving this equation with our typical 5V to 2.8V application with a 2μH inductor, we get:

$$\frac{(2.2)(0.56)}{(300kHz)(2\mu H)}=2A_{P\text{-}P}$$

Peak inductor current at 11.2A load:

$$11.2A+\frac{2A}{2}=12.2A$$

The ripple current should generally be between 10% and 40% of the output current. The inductor must be able to withstand this peak current without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss. Note that in circuits not employing the current limit function, the current in the inductor may rise above this maximum under short circuit or fault conditions; the inductor should be sized accordingly to withstand this additional current. Inductors with gradual saturation characteristics are often the best choice.

Input and Output Capacitors

A typical LTC1753 design puts significant demands on both the input and the output capacitors. During constant load operation, a buck converter like the LTC1753 draws square waves of current from the input supply at the switching frequency. The peak current value is equal to the output load current plus 1/2 peak-to-peak ripple current, and the minimum value is zero. Most of this current is supplied by the input bypass capacitor. The resulting RMS current flow in the input capacitor will heat it up, causing premature capacitor failure in extreme cases. Maximum RMS current occurs with 50% PWM duty cycle, giving an RMS current value equal to $I_{OUT}/2$. A low ESR input capacitor with an adequate ripple current rating must be used to ensure reliable operation.

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Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours (three months) lifetime at rated temperature. Further derating of the input capacitor ripple current beyond the manufacturer's specification is recommended to extend the useful life of the circuit. Lower operating temperature will have the largest effect on capacitor longevity.

The output capacitor in a buck converter sees much less ripple current under steady-state conditions than the input capacitor. Peak-to-peak current is equal to that in the inductor, usually 10% to 40% of the total load current. Output capacitor duty places a premium not on power dissipation but on ESR. During an output load transient, the output capacitor must supply all of the additional load current demanded by the load until the LTC1753 can adjust the inductor current to the new value. Output capacitor ESR results in a step in the output voltage equal to the ESR value multiplied by the change in load current. An 11A load step with a 0.05Ω ESR output capacitor will result in a 550mV output voltage shift; this is 19.6% of the output voltage for a 2.8V supply! Because of the strong relationship between output capacitor ESR and output load transient response, the output capacitor is usually chosen for ESR, not for capacitance value; a capacitor with suitable ESR will usually have a larger capacitance value than is needed for energy storage.

Electrolytic capacitors rated for use in switching power supplies with specified ripple current ratings and ESR can be used effectively in LTC1753 applications. OS-CON electrolytic capacitors from Sanyo and other manufacturers give excellent performance and have a very high performance/size ratio for electrolytic capacitors. Surface mount applications can use either electrolytic or dry tantalum capacitors. Tantalum capacitors must be surge tested and specified for use in switching power supplies. Low cost, generic tantalums are known to have very short lives followed by explosive deaths in switching power supply applications. AVX TPS series surface mount devices are popular surge tested tantalum capacitors that work well in LTC1753 applications.

A common way to lower ESR and raise ripple current capability is to parallel several capacitors. A typical LTC1753 application might exhibit 5A input ripple current. Sanyo OS-CON part number 10SA220M (220µF/10V) capacitors feature 2.3A allowable ripple current at 85°C; three in parallel at the input (to withstand the input ripple current) will meet the above requirements. Similarly, AVX TPSE337M006R0100 (330µF/6V) have a rated maximum ESR of 0.1Ω; seven in parallel will lower the net output capacitor ESR to 0.014Ω. For low cost application, Sanyo MV-GX series of capacitors can be used with acceptable performance. The small size, low profile Sanyo OS-CON 4SP820M comes with extremely low ESR (typically 0.008Ω at room temperature). This is an excellent choice for output capacitor usage. However, due to the low ESR, it requires attention to frequency compensation. Refer to the Feedback Loop Compensation section for details.

Feedback Loop Compensation

The LTC1753 voltage feedback loop is compensated at the COMP pin, attached to the output node of the internal g_m error amplifier. The feedback loop can generally be compensated properly with an RC + C network from COMP to GND as shown in Figure 7a.

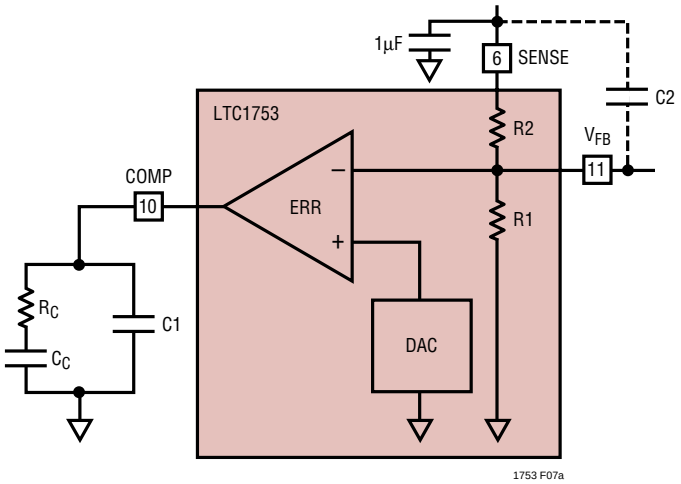

Figure 7a. Compensation Pin Hook-Up

Loop stability is affected by the values of the inductor, output capacitor, output capacitor ESR, FET $R_{DS(ON)}$, error amplifier transconductance and error amplifier compensation network. The inductor and the output capacitor create a double pole at the frequency:

$$f_{LC} = \frac{1}{2\pi\sqrt{(L_O)(C_{OUT})}}$$

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The ESR of the output capacitor forms a zero at the frequency:

$$f_{ESR} = \frac{1}{2\pi(ESR)(C_{OUT})}$$

The compensation network at the error amplifier output is to provide enough phase margin at the 0dB crossover frequency for the overall closed-loop transfer function. The zero and pole from the compensation network are:

$$f_Z = \frac{1}{2\pi(R_C)(C_C)} \text{ and } f_P = \frac{1}{2\pi(R_C)(C1)} \text{ respectively.}$$

Figure 7b shows the Bode plot of the overall transfer function.

The compensation value used in this design is based on the following criteria: $f_{SW} = 12f_{CO}$, $f_Z = f_{LC}$ and $f_P = 5f_{CO}$. At the loop crossover frequency f_{CO}, the attenuation due the LC filter and the input resistor divider is compensated by the gain of the PWM modulator and the gain of the error amplifier $(g_{mERR})(R_C)$.

When low ESR output capacitors (Sanyo OS-CON) are used, the ESR zero can be high enough in frequency that it provides little phase boost at the loop crossover frequency. Therefore, inadequate phase margin is obtained for the system. This causes loop stability problems and poor load transient response despite the improvement in output voltage ripple.

To resolve this problem, a small capacitor can be connected between the SENSE and V_{FB} pins to create a pole-zero pair in the loop compensation. The zero location is prior to the pole location and thus, phase lead can be added to boost the phase margin at the loop crossover frequency. The pole and zero locations are located at:

$$f_{ZC2} = \frac{1}{2\pi(R2)(C2)} \text{ and } f_{PC2} = \frac{1}{2\pi(R12)(C2)}$$

where R12 is the parallel combination resistance of R1 and R2. Choose C2 so that the zero is located at a lower frequency compared to f_{CO} and the pole location is high enough that the closed loop has enough phase margin for stability. Figure 7c shows the Bode plot using phase lead compensation around the LTC1753 internal resistor divider network.

Although a mathematical approach to frequency compensation can be used, the added complication of input and/or output filters, unknown capacitor ESR, and gross operating point changes with input voltage, load current variations, all suggest a more practical empirical method. This can be done by injecting a transient current at the load and using an RC network box to iterate toward the final compensation values, or by obtaining the optimum loop

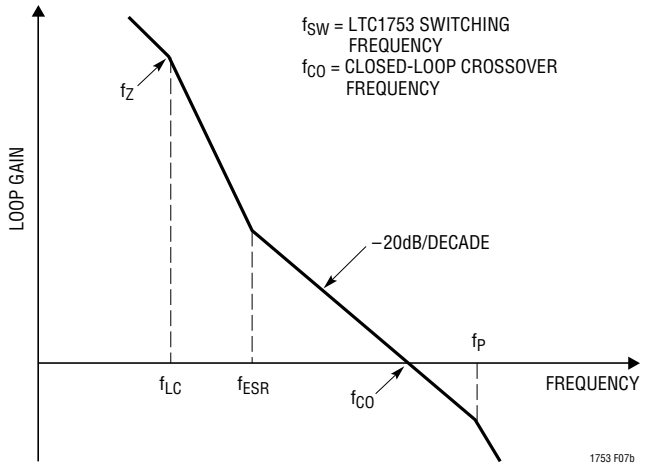

Figure 7b. Bode Plot of the LTC1753 Overall Transfer Function

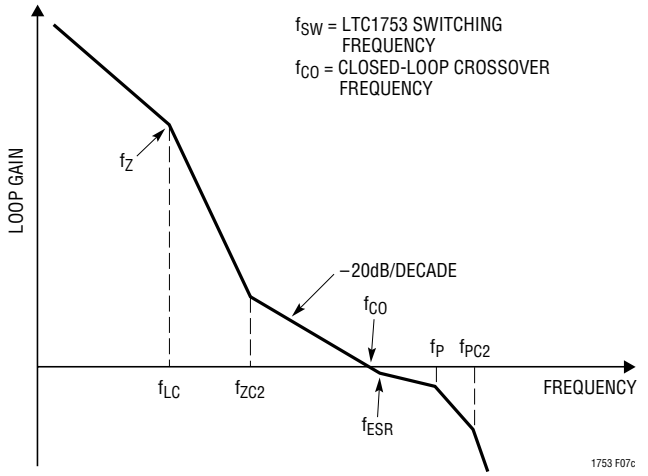

Figure 7c. Bode Plot of the LTC1753 Overall Transfer Function Using a Low ESR Output Capacitor

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response using a network analyzer to find the actual loop poles and zeros.

Table 5 shows the suggested compensation components for 5V input applications based on the inductor and output capacitor values. The values were calculated using multiple paralleled 330µF AVX TPS series surface mount tantalum capacitors as the output capacitor. The optimum component values might deviate from the suggested values slightly because of board layout and operating condition differences.

Table 5. Suggested Compensation Network for 5V Input Application Using Multiple Paralleled 330µF AVX TPS Output Capacitors

L_O (µH)	C_O (µF)	R_C (kΩ)	C_C (µF)	C1 (pF)
1	990	1.8	0.022	680
1	1980	3.6	0.01	330
1	4950	9.1	0.01	120
2.7	990	5.1	0.01	220
2.7	1980	10	0.01	120
2.7	4950	24	0.0047	47
5.6	990	10	0.01	120
5.6	1980	20	0.0047	56
5.6	4950	51	0.0033	22

An alternate output capacitor is the Sanyo MV-GX series. Using multiple parallel 1500µF Sanyo MV-GX capacitors for the output capacitor, Table 6 shows the suggested compensation component value for a 5V input application based on the inductor and output capacitor values.

Table 6. Suggested Compensation Network for 5V Input Application Using Multiple Paralleled 1500µF Sanyo MV-GX Output Capacitors

L_O (µH)	C_O (µF)	R_C (kΩ)	C_C (µF)	C1 (pF)
1	4500	4.3	0.022	270
1	6000	5.6	0.015	220
1	9000	8.2	0.01	150
2.7	4500	11	0.01	100
2.7	6000	15	0.01	82
2.7	9000	22	0.01	56
5.6	4500	24	0.01	56
5.6	6000	30	0.0047	39
5.6	9000	47	0.0047	27

Table 7 shows the suggested compensation component value for a 5V application based on the Sanyo OS-CON 4SP820M low ESR output capacitors

Table 7. Suggested Compensation Network for 5V Input Application Using Multiple Paralleled 820µF Sanyo OS-CON 4SP820M Output Capacitors

L_O (µH)	C_O (µF)	R_C (kΩ)	C_C (µF)	C1 (pF)	C2 (pF)
1	1640	5.6	0.01	220	270
1	2460	9.1	0.0047	150	270
1	4100	15	0.0047	82	270
2.7	1640	16	0.0047	82	270
2.7	2460	24	0.0033	56	270
2.7	4100	39	0.0022	33	270
5.6	1640	33	0.0033	39	270
5.6	2460	47	0.0022	27	270
5.6	4100	82	0.0022	15	270

Remote Sense Considerations

In some installations such as Intel Slot 2 designs, the regulator is by necessity a relatively long distance from the load. It is desirable in these instances to connect the regulator sense connection at the load rather than directly at the regulator output. This forces the supply voltage to be regulated at the load which, after all, is the desired point to control. In most cases no problems will be encountered as a result of doing this. However, care must be exercised if the power path is long or the capacitance at the load is very large.

The power distribution path has some finite amount of inductance. There will also be a significant amount of capacitance at the load as the local bypass. These two circuit elements constitute a second order, lowpass filter and the SENSE lead connects to the output of this filter. As is true for any LC filter, there is 180° of phase shift at a frequency beyond the double pole. If the resonant frequency of the filter falls below the regulator's feedback loop crossover frequency, the loop will likely oscillate.

There are a couple of measures that may be taken to alleviate this problem. The first is to minimize the inductance of the power path. Therefore, it is desirable to make the power trace as wide as possible and as short as

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possible. It should also be located as close as possible above (or below) the power ground plane. Some of the phase shift problem can be solved by taking the AC feedback locally at the regulator output while still taking the DC feedback at the point of load. This permits accurate DC regulation while still maintaining reasonable phase margin. This is done by connecting the top of phase lead capacitor, C2, locally at the regulator output while connecting the SENSE pin to the load. The corner frequency $1/(2\pi \bullet R2 \bullet C2)$ must be significantly less than the resonant frequency of the parasitic inductance and the output capacitance $1/(2\pi \bullet \sqrt{L_{DIST} \bullet C_{LOAD}})$. Certain board layouts may require R_{C2}, a small series resistor, to decrease the slew rate of the feedforward path. In general, an empirical approach to compensating this type of loop will be best since it will be very difficult to estimate the parasitic inductance of the power path analytically. It should be noted that if the circuit can have a wide range of output capacitance, this can be dangerous technique to employ since the double-pole frequency will move as the load capacitance changes. Be sure to verify stability with all possible combinations of output capacitance.

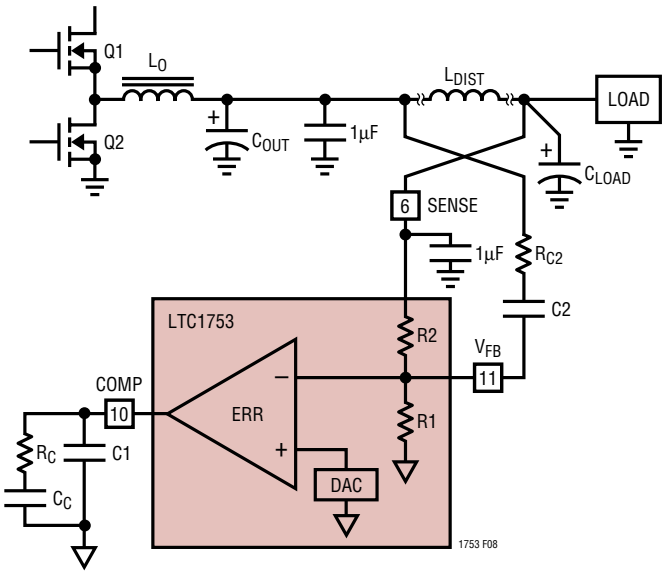

Figure 8. Feedback Connections for Remote Sense Applications

VID0 to VID4, PWRGD and $\overline{\text{FAULT}}$

The digital inputs (VID0 to VID4) program the internal DAC which in turn controls the output voltage. These digital input controls are intended to be static and are not designed for high speed switching. Forcing V_{OUT} to step from a high to a low voltage by changing the VID_n pins quickly can cause $\overline{\text{FAULT}}$ to trip.

Figure 9 shows the relationship between the V_{OUT} voltage, PWRGD and $\overline{\text{FAULT}}$. To prevent PWRGD from interrupting the CPU unnecessarily, the LTC1753 has a built-in t_{PWRBAD} delay to prevent noise at the SENSE pin from toggling PWRGD. The internal time delay is designed to take about 500µs for PWRGD to go low and 1ms for it to recover. Once PWRGD goes low, the internal circuitry watches for the output voltage to exceed 113% of the rated voltage. If this happens, $\overline{\text{FAULT}}$ will be triggered. Once $\overline{\text{FAULT}}$ is triggered, G1 and G2 will be forced low immediately and the LTC1753 will remain in this state until V_{CC} power supply is recycled or OUTEN is toggled.

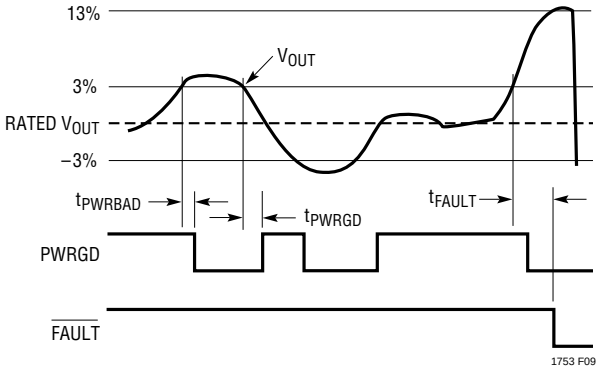

Figure 9. PWRGD and $\overline{\text{FAULT}}$

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LAYOUT CONSIDERATIONS

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1753. These items are also illustrated graphically in the layout diagram of Figure 10. The thicker lines show the high current paths. Note that at 10A current levels or above, current density in the PC board itself is a serious concern. Traces carrying high current should be as wide as possible. For example, a PCB fabricated with 2oz copper requires a minimum trace width of 0.15" to carry 10A.

1. In general, layout should begin with the location of the power devices. Be sure to orient the power circuitry so that a clean power flow path is achieved. Conductor widths should be maximized and lengths minimized. After you are satisfied with the power path, the control circuitry should be laid out. It is much easier to find routes for the relatively small traces in the control circuits than it is to find circuitous routes for high current paths.
2. The GND and SGND pins should be shorted directly at the LTC1753. This helps to minimize internal ground disturbances in the LTC1753 and prevents differences in ground potential from disrupting internal circuit operation. This connection should then tie into the ground plane at a single point, preferably at a fairly quiet point in the circuit such as close to the output capacitors. This is not always practical, however, due to physical constraints. Another reasonably good point to make this connection is between the output capacitors and the source connection of the low side FET Q2. Do not tie this single point ground in the trace run between the low side FET source and the input capacitor ground, as this area of the ground plane will be very noisy.
3. The small signal resistors and capacitors for frequency compensation and soft-start should be located very close to their respective pins and the ground ends connected to the signal ground pin through a separate trace. Do not connect these parts to the ground plane!
4. The V_{CC} and PV_{CC} decoupling capacitors should be as close to the LTC1753 as possible. The 10µF bypass capacitors shown at V_{CC} and PV_{CC} will help provide optimum regulation performance.
5. The (+) plate of C_{IN} should be connected as close as possible to the drain of the upper MOSFET. An additional 1µF ceramic capacitor between V_{IN} and power ground is recommended.
6. The SENSE and V_{FB} pins are very sensitive to pickup from the switching node. Care should be taken to isolate SENSE and V_{FB} from possible capacitive coupling to the inductor switching signal. A 1µF is required between the SENSE pin and the SGND pin next to the LTC1753.

   If PWRGD or $\overline{FAULT}$ are in the wrong logic state for nonobvious reasons, check the layout of the SENSE and V_{FB} traces carefully. The 1µF capacitor should be mounted as close to the SENSE pin as possible. In addition, if feedforward compensation is in use, a resistor in series with the feedforward capacitor might be required. Finally, a low value resistor may be placed between the output voltage and the SENSE pin (and the 1µF capacitor). This RC will help filter high frequency spikes.
7. OUTEN is a high impedance input and should be externally pulled up to a logic HIGH for normal operation.
8. Kelvin sense I_{MAX} and I_{FB} at Q1's drain and source pins.

APPLICATIONS INFORMATION

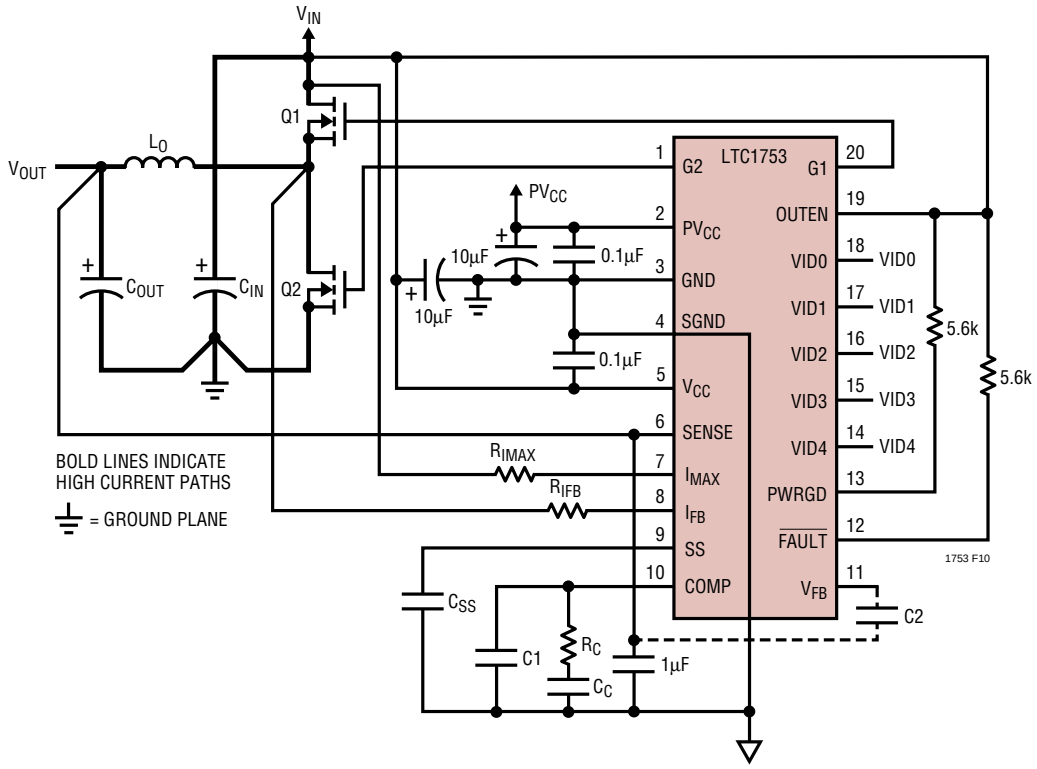
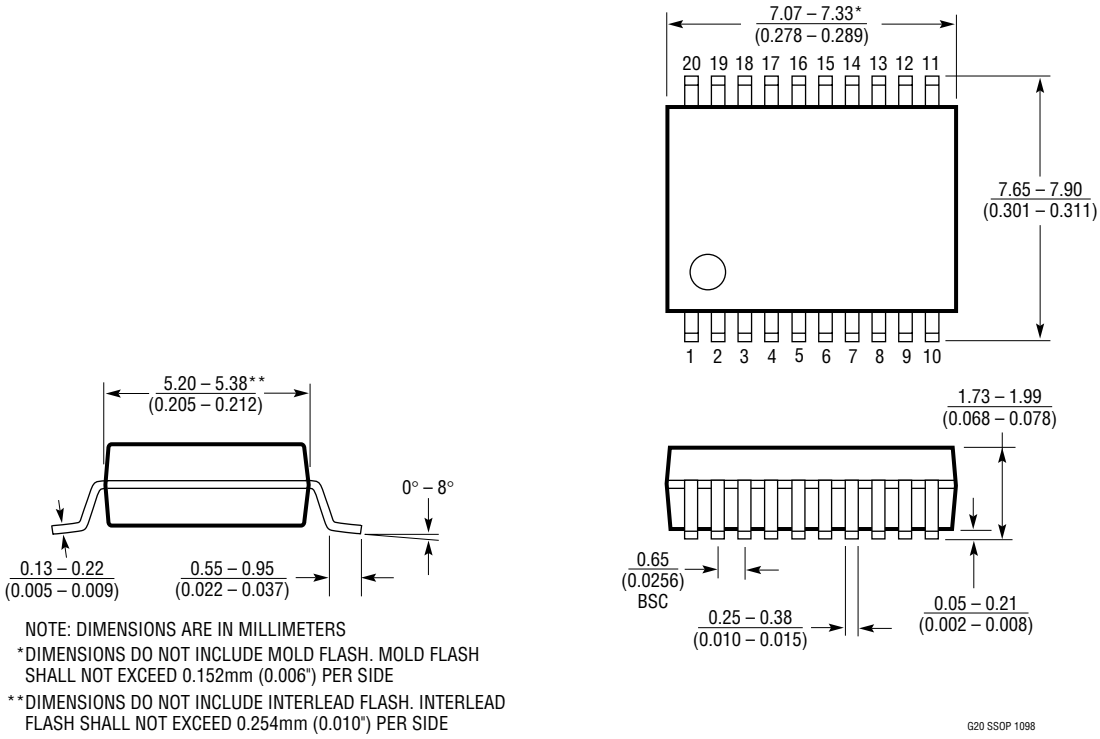


Figure 10. LTC1753 Layout Diagram

PACKAGE DESCRIPTION

G Package
20-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



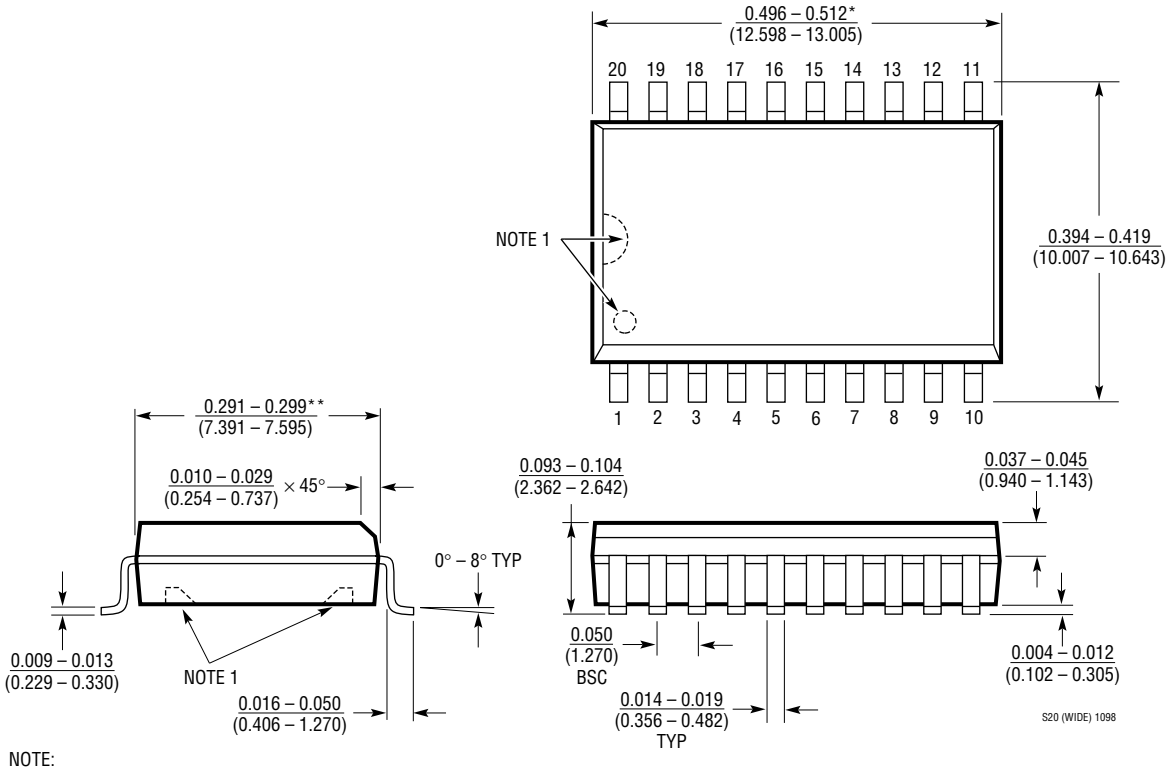
NOTE: DIMENSIONS ARE IN MILLIMETERS

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.152mm (0.006") PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.254mm (0.010") PER SIDE

PACKAGE DESCRIPTION

SW Package
20-Lead Plastic Small Outline (Wide 0.300)
(LTC DWG # 05-08-1620)



NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

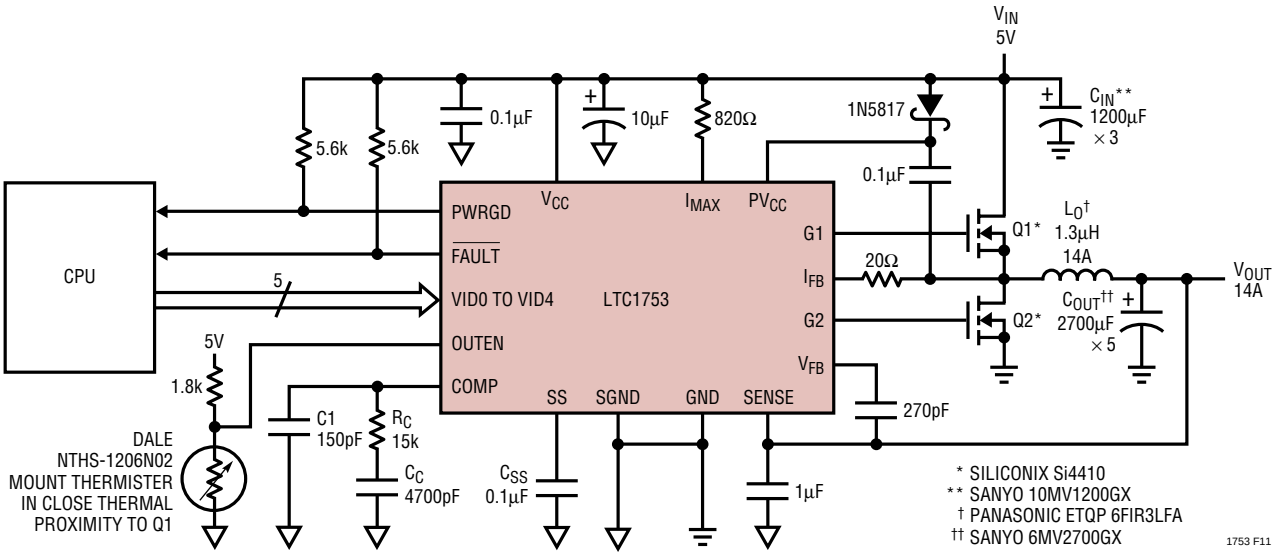


Figure 11. Single Supply LTC1753 5V to 1.3V-3.5V Application with Thermal Monitor

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1530	High Power Synchronous Step-Down Controller	SO-8 with Current Limit, No R_{SENSE}™ Saves Space, Fixed Frequency Ideal for 5V to 3.3V or Lower
LTC1628	Dual High Efficiency Low Noise Synchronous Step-Down Switching Regulator	Constant Frequency, Standby 5V and 3.3V LDOs, 3.5V ≤ V_{IN} ≤ 36V
LTC1553L	5-Bit Programmable Synchronous Switching Regulator Controller for Pentium II Processor	DAC Code Conforms to the Intel Pentium II Processor VRM8.2 DC/DC Converter Specification
LT1585-1.5	Fixed 1.5V, 4.6A and 5A Low Dropout, Fast Response GTL+ Regulators	GTL+ Power Supplies
LTC1629	PolyPhase™ High Efficiency Controller	Expandable Up to 12 Phases, 28-Lead SSOP, Up to 200A
LTC1703	2-Phase, Dual Synchronous Controller with VID	Mobile VID Code, Each Output Up to 15A, V_{IN} = 5V for I/O and Core
LTC1706-81	5-Bit VID Programmer	Desktop Pentium III Processors, V_{IN} ≤ 7V
LTC1709	High Efficiency, Synchronous Step-Down Switching Regulator with 5-Bit VID	Current Mode, V_{IN} to 36V, I_{OUT} Up to 42A
LTC1735	High Efficiency Low Noise Synchronous Step-Down Switching Regulator	Drives Synchronous N-Channel FETs, V_{IN} ≤ 36V
LTC1772	SOT-23 Step-Down Controller	100% Duty Cycle, Up to 4A, 2.2V to 9.8V V_{IN}
LTC1873	Dual 550kHz Synchronous 2-Phase Switching Regulator Controller with 5-Bit VID	Desktop VID Codes, I_{OUT} Up to 25A on Each Channel, 28-Lead SSOP
LTC1929	2-Phase, High Efficiency, Synchronous Step-Down Switching Regulator	Current Mode Ensures Accurate Current Sensing, V_{IN} Up to 36V, I_{OUT} Up to 42A, 28-Lead SSOP

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