



**THE DATASHEET OF  
LTC2902-1CGN#TRPBF**





## ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2, 3)

V1, V2, V3, V4, V <sub>PG</sub> .....	-0.3V to 7V
RST (LTC2902-1) .....	-0.3V to 7V
RST (LTC2902-2) .....	-0.3V to (V2 + 0.3V)
COMPX, RDIS .....	-0.3V to 7V
T0, T1 .....	-0.3V to (V <sub>CC</sub> + 0.3V)
CRT .....	-0.3V to (V <sub>CC</sub> + 0.3V)
V <sub>REF</sub> .....	-0.3V to (V <sub>CC</sub> + 0.3V)
Reference Load Current (I <sub>VREF</sub> ) .....	±1mA
V4 Input Current (-ADJ Mode) .....	-1mA
Operating Temperature Range	
LTC2902-1C/LTC2902-2C .....	0°C to 70°C
LTC2902-1I/LTC2902-2I .....	-40°C to 85°C
Storage Temperature Range .....	-65°C to 150°C
Lead Temperature (Soldering, 10 sec) .....	300°C

## PACKAGE/ORDER INFORMATION

<p>GN PACKAGE 16-LEAD PLASTIC SSOP T<sub>JMAX</sub> = 125°C, θ<sub>JA</sub> = 130°C/W</p>	ORDER PART NUMBER
	LTC2902-1CGN LTC2902-2CGN LTC2902-1IGN LTC2902-2IGN
	GN16 PART MARKING
	29021 29022 29021I 29022I

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T<sub>A</sub> = 25°C. V<sub>CC</sub> = 5V, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V <sub>RT50</sub>	5V, 5% Reset Threshold	V1 Input Threshold	● 4.600	4.675	4.750	V
	5V, 7.5% Reset Threshold		● 4.475	4.550	4.625	V
	5V, 10% Reset Threshold		● 4.350	4.425	4.500	V
	5V, 12.5% Reset Threshold		● 4.225	4.300	4.375	V
V <sub>RT33</sub>	3.3V, 5% Reset Threshold	V1, V2 Input Threshold	● 3.036	3.086	3.135	V
	3.3V, 7.5% Reset Threshold		● 2.954	3.003	3.053	V
	3.3V, 10% Reset Threshold		● 2.871	2.921	2.970	V
	3.3V, 12.5% Reset Threshold		● 2.789	2.838	2.888	V
V <sub>RT30</sub>	3V, 5% Reset Threshold	V2 Input Threshold	● 2.760	2.805	2.850	V
	3V, 7.5% Reset Threshold		● 2.685	2.730	2.775	V
	3V, 10% Reset Threshold		● 2.610	2.655	2.700	V
	3V, 12.5% Reset Threshold		● 2.535	2.580	2.625	V
V <sub>RT25</sub>	2.5V, 5% Reset Threshold	V2, V3 Input Threshold	● 2.300	2.338	2.375	V
	2.5V, 7.5% Reset Threshold		● 2.238	2.275	2.313	V
	2.5V, 10% Reset Threshold		● 2.175	2.213	2.250	V
	2.5V, 12.5% Reset Threshold		● 2.113	2.150	2.188	V
V <sub>RT18</sub>	1.8V, 5% Reset Threshold	V3, V4 Input Threshold	● 1.656	1.683	1.710	V
	1.8V, 7.5% Reset Threshold		● 1.611	1.638	1.665	V
	1.8V, 10% Reset Threshold		● 1.566	1.593	1.620	V
	1.8V, 12.5% Reset Threshold		● 1.521	1.548	1.575	V
V <sub>RT15</sub>	1.5V, 5% Reset Threshold	V3, V4 Input Threshold	● 1.380	1.403	1.425	V
	1.5V, 7.5% Reset Threshold		● 1.343	1.365	1.388	V
	1.5V, 10% Reset Threshold		● 1.305	1.328	1.350	V
	1.5V, 12.5% Reset Threshold		● 1.268	1.290	1.313	V
V <sub>RTA</sub>	ADJ, 5% Reset Threshold	V3, V4 Input Threshold	● 0.492	0.500	0.508	V
	ADJ, 7.5% Reset Threshold		● 0.479	0.487	0.494	V
	ADJ, 10% Reset Threshold		● 0.466	0.473	0.481	V
	ADJ, 12.5% Reset Threshold		● 0.453	0.460	0.467	V

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 5\text{V}$ , unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$V_{RTAN}$	–ADJ Reset Threshold	V4 Input Threshold	●	–18	0	18	mV
$V_{CC}$	Minimum Internal Operating Voltage	$\overline{\text{RST}}$ , COMPX in Correct Logic State; V <sub>CC</sub> Rising Prior to Program	●		1	V	
$V_{CCMINP}$	Minimum Required for Programming	V <sub>CC</sub> Rising	●		2.42	V	
$V_{CCMINC}$	Minimum Required for Comparators	V <sub>CC</sub> Falling	●		2.32	V	
$V_{REF}$	Reference Voltage	V <sub>CC</sub> ≥ 2.3V, I <sub>VREF</sub> = ±1mA, C <sub>REF</sub> ≤ 1000pF T0 Low, T1 Low T0 Low, T1 High T0 High, T1 Low T0 High, T1 High	●	1.192	1.210	1.228	V
			●	1.160	1.178	1.195	V
			●	1.128	1.146	1.163	V
			●	1.096	1.113	1.130	V
$V_{PG}$	Programming Voltage Range	V <sub>CC</sub> ≥ V <sub>CCMINP</sub>	●	0	V <sub>REF</sub>	V	
I <sub>VPG</sub>	V <sub>PG</sub> Input Current	V <sub>PG</sub> = V <sub>REF</sub>	●		±20	nA	
I <sub>V1</sub>	V1 Input Current	V1 = 5V, I <sub>VREF</sub> = 12μA, (Note 4)	●	43	75	μA	
I <sub>V2</sub>	V2 Input Current	V2 = 3.3V	●	0.8	2	μA	
I <sub>V3</sub>	V3 Input Current	V3 = 2.5V V3 = 0.55V (ADJ Mode)	●	–15	0.52	1.2	μA nA
I <sub>V4</sub>	V4 Input Current	V4 = 1.8V V4 = 0.55V (ADJ Mode) V4 = –0.05V (–ADJ Mode)	●	–15	0.34	0.8	μA nA nA
I <sub>CRT(UP)</sub>	CRT Pull-Up Current	V <sub>CRT</sub> = 0V	●	–1.4	–2	–2.6	μA
I <sub>CRT(DN)</sub>	CRT Pull-Down Current	V <sub>CRT</sub> = 1.3V	●	10	20	30	μA
t <sub>RST</sub>	Reset Time-Out Period	C <sub>RT</sub> = 1500pF	●	5	7	9	ms
t <sub>UV</sub>	V <sub>X</sub> Undervoltage Detect to $\overline{\text{RST}}$ or COMPX	V <sub>X</sub> Less Than Reset Threshold V <sub>RTX</sub> by More Than 1%		150			μs
$V_{OL}$	Output Voltage Low $\overline{\text{RST}}$ , COMPX	I <sub>SINK</sub> = 2.5mA; V1 = 3V, V2 = 3V; V3, V4 = 0V; V <sub>PG</sub> = 0V	●	0.15	0.4	V	
		I <sub>SINK</sub> = 100μA; V2 = 1V; V1, V3, V4 = 0V	●	0.05	0.3	V	
		I <sub>SINK</sub> = 100μA; V1 = 1V; V2, V3, V4 = 0V	●	0.05	0.3	V	
$V_{OH}$	Output Voltage High $\overline{\text{RST}}$ , COMPX (Note 5)	I <sub>SOURCE</sub> = 1μA	●	V2 – 1		V	
$V_{OH}$	Output Voltage High $\overline{\text{RST}}$ (LTC2902-2) (Note 6)	I <sub>SOURCE</sub> = 200μA	●	0.8 • V2		V	

### Digital Inputs T0, T1, RDIS

$V_{IL}$	T0, T1 Low Level Input Voltage	V <sub>CC</sub> = 3.3V to 5.5V	●		0.3V <sub>CC</sub>	V
$V_{IH}$	T0, T1 High Level Input Voltage	V <sub>CC</sub> = 3.3V to 5.5V	●	0.7V <sub>CC</sub>		V
I <sub>INTOL</sub>	T0, T1 Input Current	T0 = 0V, T1 = V <sub>CC</sub>	●	±0.1	±1	μA
$V_{IL}$	$\overline{\text{RDIS}}$ Input Threshold Low	V <sub>CC</sub> = 3.3V to 5.5V	●	0.4		V
$V_{IH}$	$\overline{\text{RDIS}}$ Input Threshold High	V <sub>CC</sub> = 3.3V to 5.5V	●		1.6	V
I <sub>RDIS</sub>	$\overline{\text{RDIS}}$ Pull-Up Current	V <sub>RDIS</sub> = 0V		–10		μA

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** All voltage values are with respect to GND.

**Note 3:** The greater of V1, V2 is the internal supply voltage (V<sub>CC</sub>).

**Note 4:** Under static no-fault conditions, V1 will necessarily supply quiescent current. If at any time V2 is larger than V1, V2 must be capable of supplying the quiescent current, programming (transient) current and reference load current.

**Note 5:** The output pins  $\overline{\text{RST}}$  and COMPX have internal pull-ups to V2 of typically 6μA. However, external pull-up resistors may be used when faster rise times are required or for V<sub>OH</sub> voltages greater than V2.

**Note 6:** The push-pull  $\overline{\text{RST}}$  output pin on the LTC2902-2 is *actively* pulled up to V2.

## TEST CIRCUITS

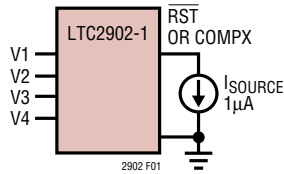


Figure 1.  $\overline{\text{RST}}$ , COMPX  $V_{OH}$  Test

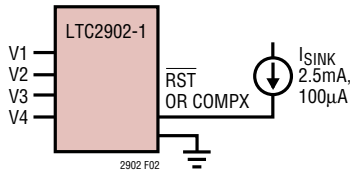


Figure 2.  $\overline{\text{RST}}$ , COMPX  $V_{OL}$  Test

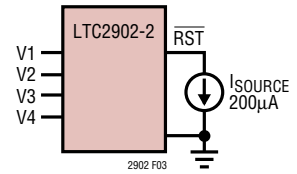
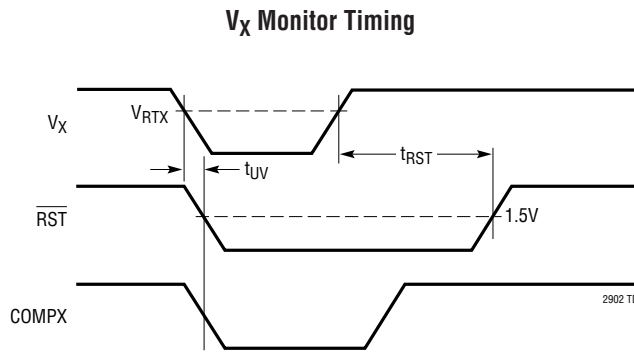


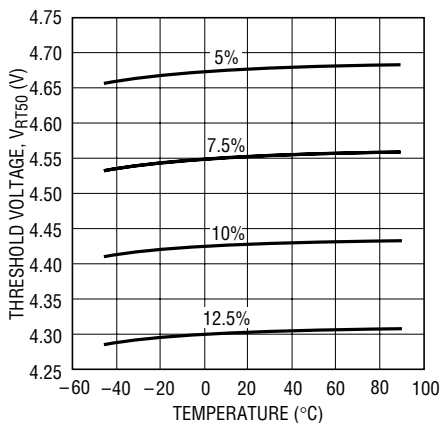
Figure 3. Active Pull-Up  $\overline{\text{RST}}$   $V_{OH}$  Test

## TIMING DIAGRAM



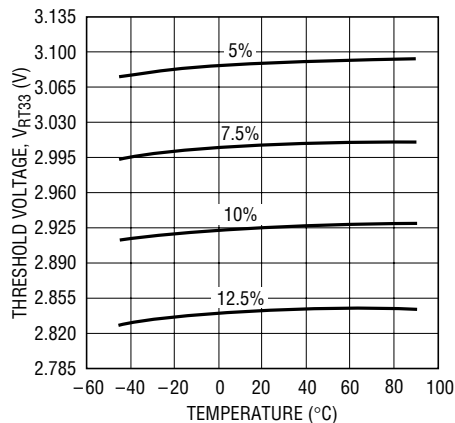
## TYPICAL PERFORMANCE CHARACTERISTICS

5V Threshold Voltage vs Temperature



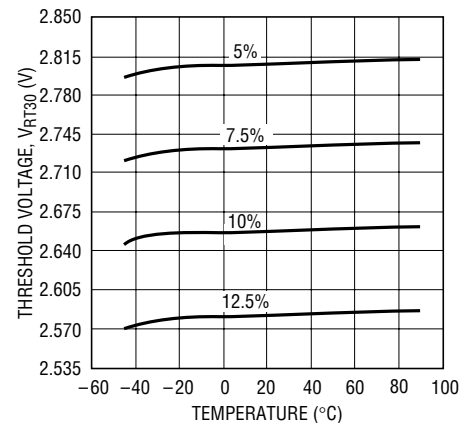
2902 G01

3.3V Threshold Voltage vs Temperature



2902 G02

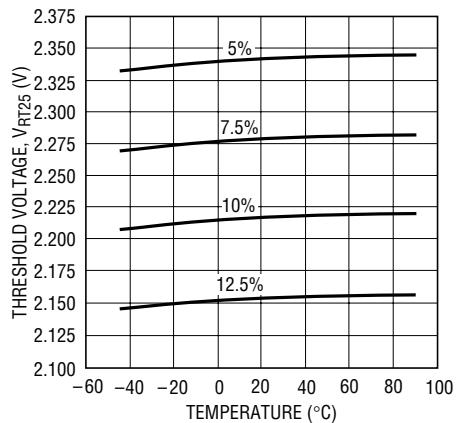
3V Threshold Voltage vs Temperature



2902 G03

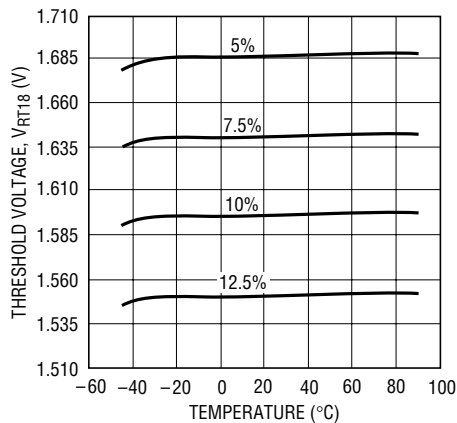
# TYPICAL PERFORMANCE CHARACTERISTICS

**2.5V Threshold Voltage vs Temperature**



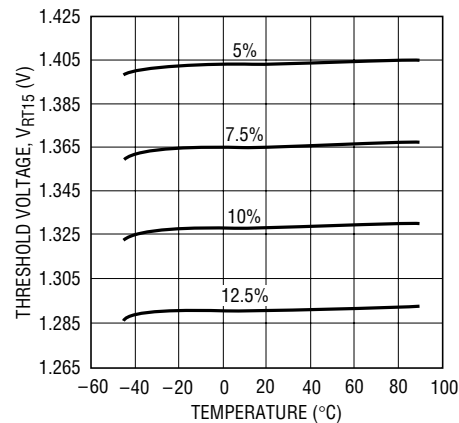
2902 G04

**1.8V Threshold Voltage vs Temperature**



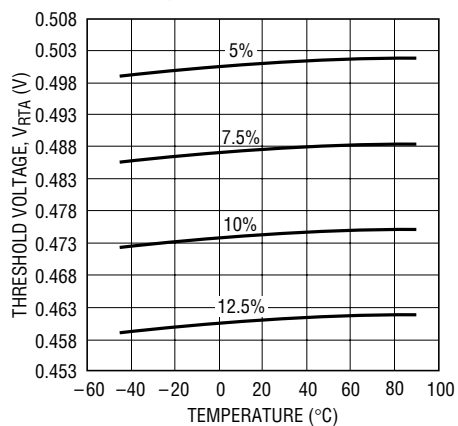
2902 G05

**1.5V Threshold Voltage vs Temperature**



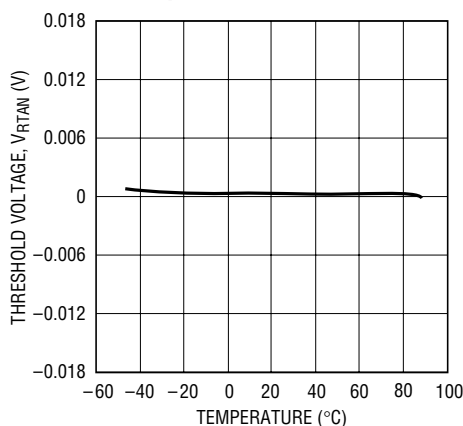
2902 G06

**ADJ Threshold Voltage vs Temperature**



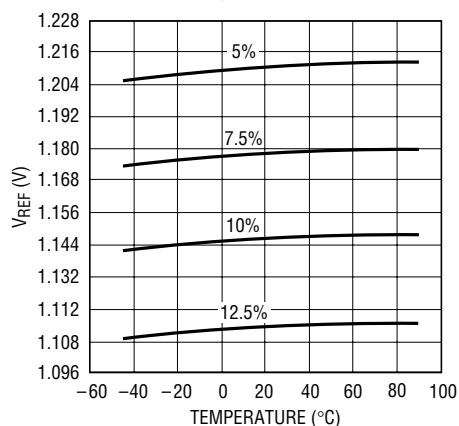
2902 G07

**-ADJ Threshold Voltage vs Temperature**



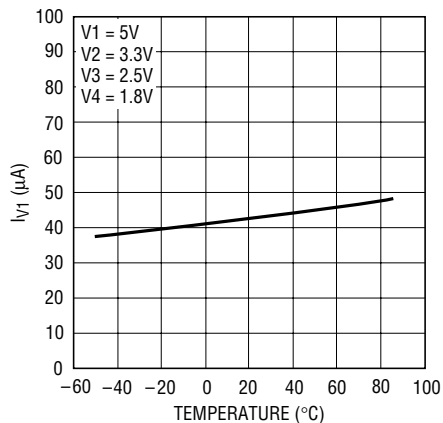
2902 G08

**V\_REF vs Temperature**



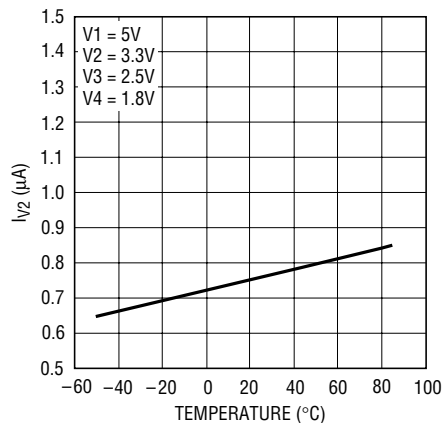
2902 G09

**I\_V1 vs Temperature**



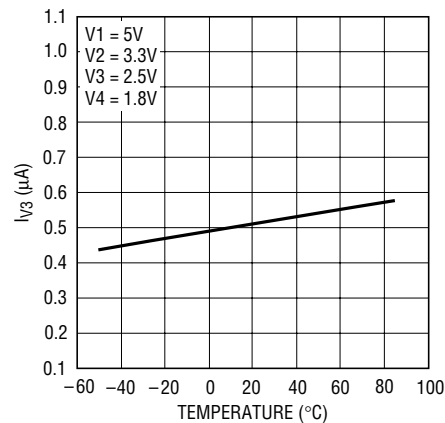
2902 G10

**I\_V2 vs Temperature**



2902 G11

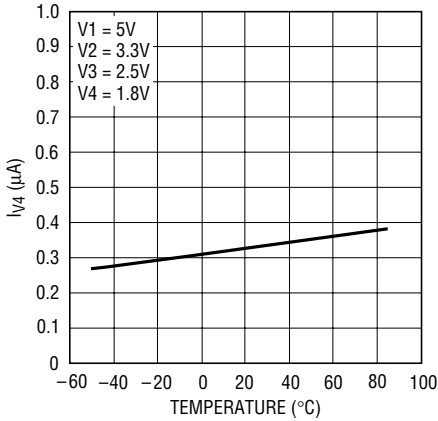
**I\_V3 vs Temperature**



2902 G12

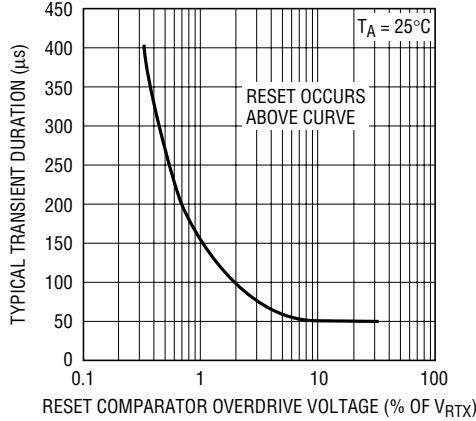
# TYPICAL PERFORMANCE CHARACTERISTICS

**$I_{V4}$  vs Temperature**



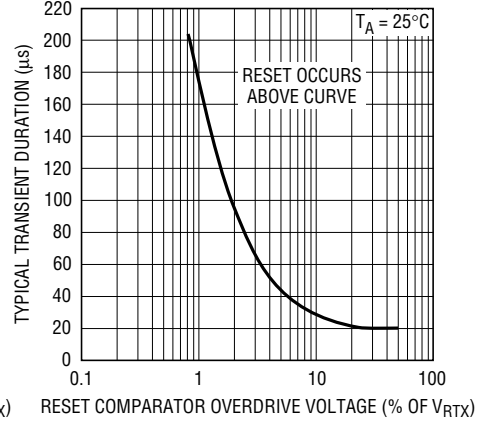
2902 G13

**Typical Transient Duration vs Comparator Overdrive (V1, V2)**



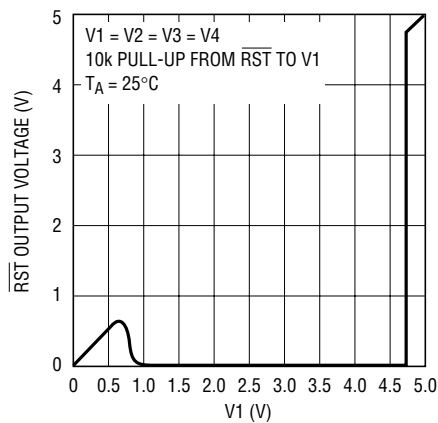
2902 G14

**Typical Transient Duration vs Comparator Overdrive (V3, V4)**



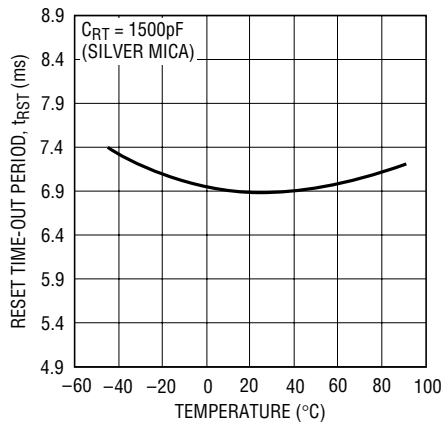
2902 G25

**RST Output Voltage vs V1,  $V_{PG} = 0V$**



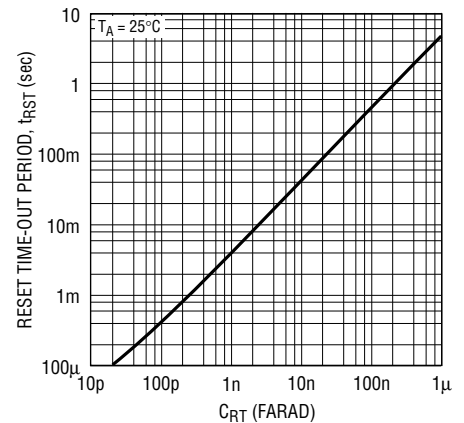
2902 G15

**Reset Time-Out Period vs Temperature**



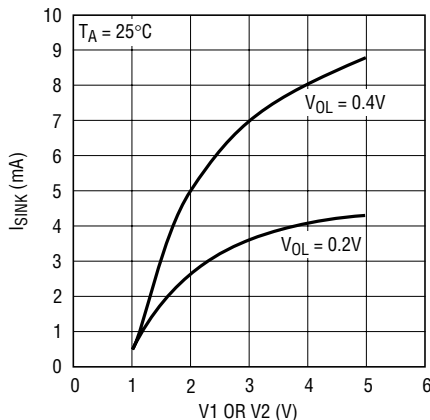
2902 G16

**Reset Time-Out Period vs Capacitance**



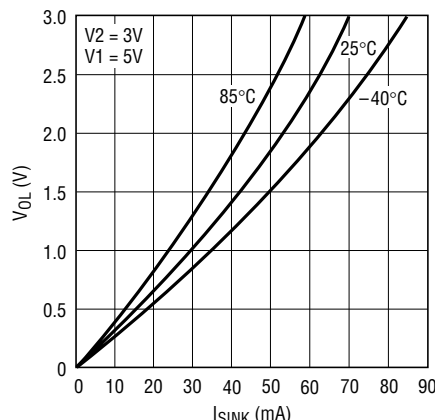
2902 G17

**RST, COMPX  $I_{SINK}$  vs Supply Voltage**



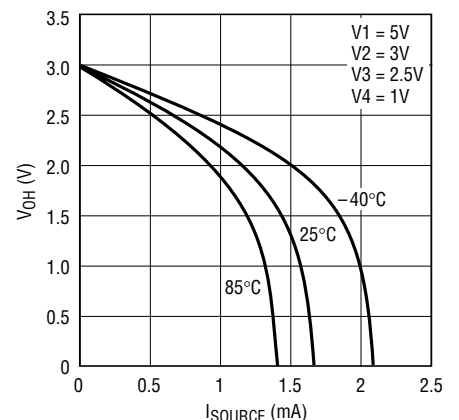
2902 G18

**RST, COMPX Voltage Output Low vs Output Sink Current**



2902 G19

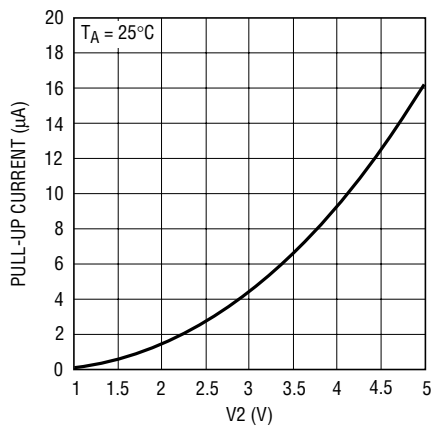
**RST High Level Output Voltage vs Output Source Current (LTC2902-2)**



2902 G20

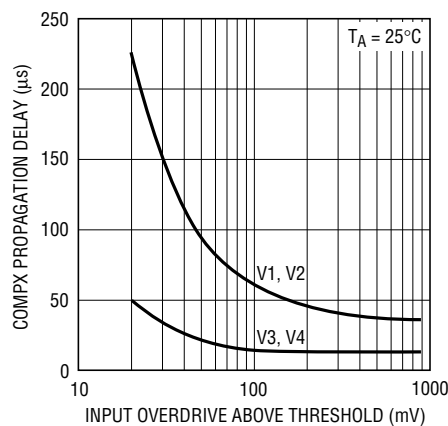
## TYPICAL PERFORMANCE CHARACTERISTICS

**COMPX Pull-Up Current vs V2 (COMPX Held at 0V)**



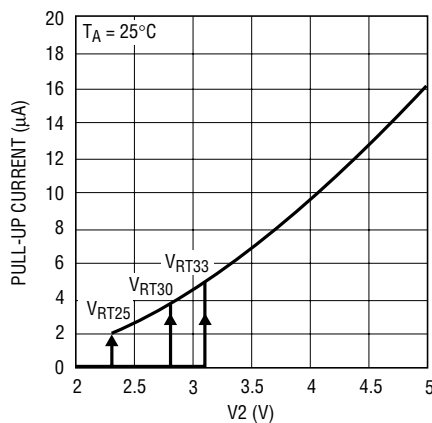
2902 G21

**COMPX Propagation Delay vs Input Overdrive Above Threshold**



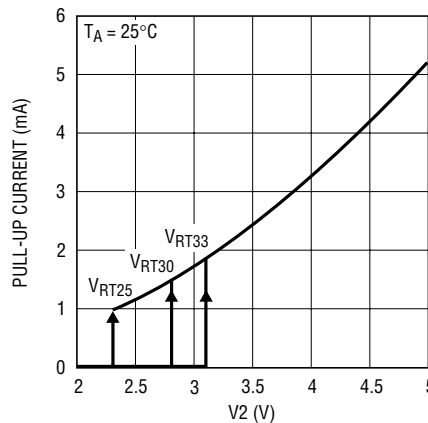
2902 G22

**RST Pull-Up Current vs V2 (LTC2902-1)**



2902 G23

**RST Pull-Up Current vs V2 (LTC2902-2)**



2902 G24

## PIN FUNCTIONS

**COMP3 (Pin 1):** Comparator Output 3. Nondelayed, active high logic output with weak pull-up to V2. Pulls high when V3 is above reset threshold. May be pulled greater than V2 using external pull-up.

**COMP1 (Pin 2):** Comparator Output 1. Nondelayed, active high logic output with weak pull-up to V2. Pulls high when V1 is above reset threshold. May be pulled greater than V2 using external pull-up.

**V3 (Pin 3):** Voltage Input 3. Select from 2.5V, 1.8V, 1.5V or ADJ. See Table 1 for details.

**V1 (Pin 4):** Voltage Input 1. Select from 5V or 3.3V. See Table 1 for details. The greater of (V1, V2) is also  $V_{CC}$  for the chip. Bypass this pin to ground with a 0.1µF (or greater) capacitor.

**CRT (Pin 5):** Reset Delay Time Programming Pin. Attach an external capacitor ( $C_{RT}$ ) to GND to set a reset delay time of 4.6ms/nF. Leaving the pin open generates a minimum delay of approximately 50µs. A 47nF capacitor will generate a 216ms reset delay time.

## PIN FUNCTIONS

**$\overline{\text{RST}}$  (Pin 6):** Reset Logic Output. Active low with weak pull-up to V2 (LTC2902-1) or active pull-up to V2 (LTC2902-2). Pulls low when any voltage input is below the reset threshold and held low for programmed delay time after all voltage inputs are above threshold. May be pulled above V2 using an external pull-up (LTC2902-1 only).

**T0 (Pin 7):** Digital Input for Supply Tolerance Selection (5%, 7.5%, 10% or 12.5%). Used in conjunction with T1 (Pin 9). See Applications Information for tolerance selection chart (Table 4).

**$\overline{\text{RDIS}}$  (Pin 8):** Digital Input for  $\overline{\text{RST}}$  Disable. A low input on this pin forces the  $\overline{\text{RST}}$  output to V2 (or pull-up voltage). Useful for determining supply margins without issuing reset command to processor. A weak internal pull-up allows pin to be left floating for normal monitor operation.

**T1 (Pin 9):** Digital Input for Supply Tolerance Selection (5%, 7.5%, 10% or 12.5%). Used in conjunction with T0 (Pin 7). See Applications Information for tolerance selection chart (Table 4).

**GND (Pin 10):** Ground.

**V<sub>PG</sub> (Pin 11):** Voltage Threshold Combination Select Input. Connect to an external 1% resistive divider between V<sub>REF</sub> and GND to select 1 of 16 combinations of preset and/or  $\pm$ adjustable voltage thresholds (see Table 1). Do not add capacitance on the V<sub>PG</sub> pin.

**V<sub>REF</sub> (Pin 12):** Buffered Reference Voltage. A 1.210V nominal reference used for programming voltage (V<sub>PG</sub>) and for the offset of negative adjustable applications. The buffered reference can source and sink up to 1mA. The reference can drive a bypass capacitor of up to 1000pF without oscillation.

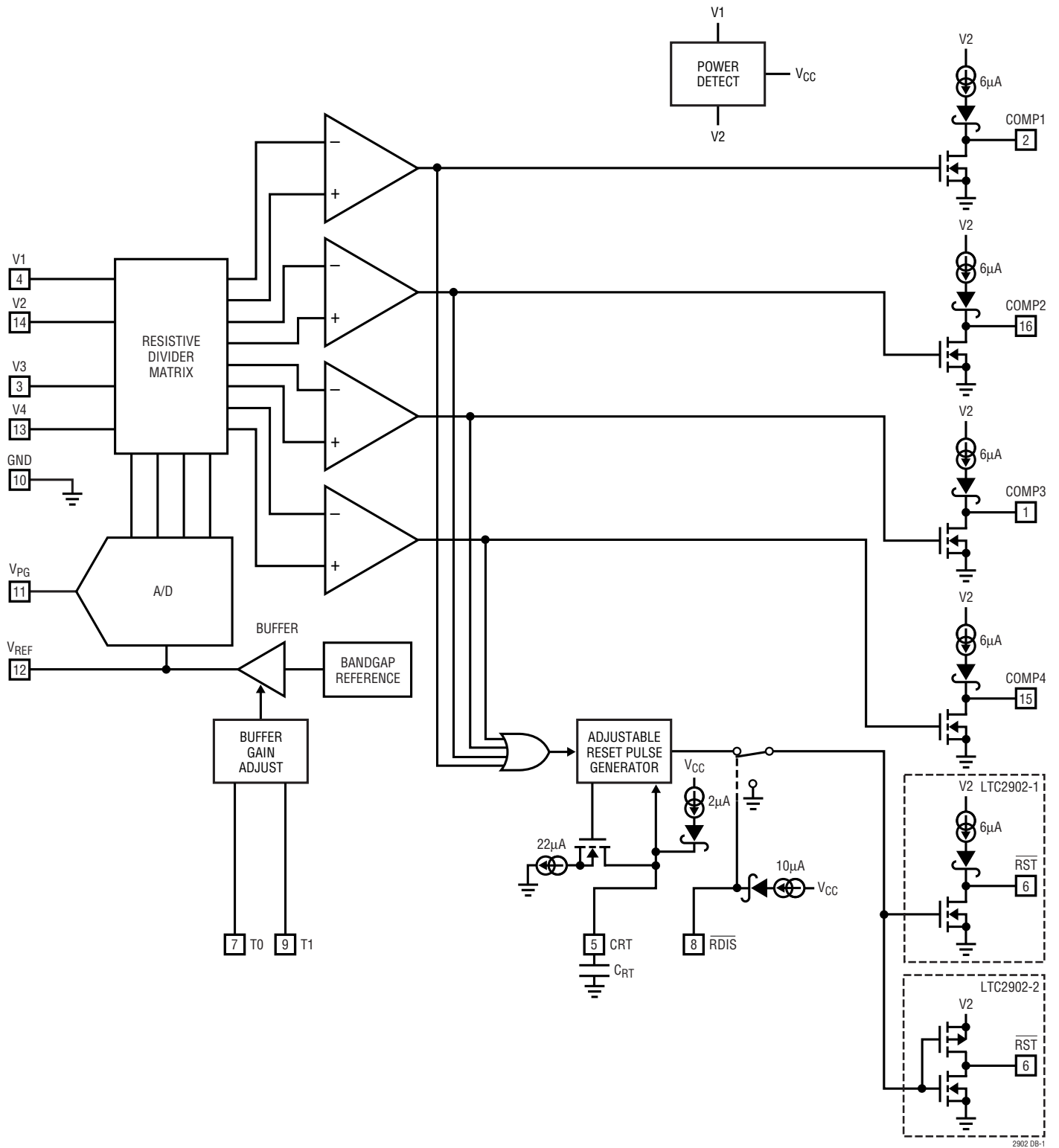
**V4 (Pin 13):** Voltage Input 4. Select from 1.8V, 1.5V, ADJ or  $-\text{ADJ}$ . See Table 1 for details.

**V2 (Pin 14):** Voltage Input 2. Select from 3.3V, 3V or 2.5V. See Table 1 for details. The greater of (V1, V2) is also V<sub>CC</sub> for chip. Bypass this pin to ground with a 0.1 $\mu$ F (or greater) capacitor. All logic outputs (COMP1,  $\overline{\text{COMP2}}$ , COMP3, COMP4) are weakly pulled up to V2.  $\overline{\text{RST}}$  is weakly pulled up to V2 in the LTC2902-1 and  $\overline{\text{RST}}$  is actively pulled up to V2 in the LTC2902-2.

**COMP4 (Pin 15):** Comparator Output 4. Nondelayed, active high logic output with weak pull-up to V2. Pulls high when V4 is above reset threshold. May be pulled greater than V2 using external pull-up.

**COMP2 (Pin 16):** Comparator Output 2. Nondelayed, active high logic output with weak pull-up to V2. Pulls high when V2 is above reset threshold. May be pulled greater than V2 using external pull-up.

**BLOCK DIAGRAM**



2902 DB-1

## APPLICATIONS INFORMATION

### Power-Up

On power-up, the larger of V1 or V2 will power the drive circuits for the  $\overline{\text{RST}}$  and the COMPX pins. This ensures that the  $\overline{\text{RST}}$  and COMPX outputs will be low as soon as V1 or V2 reaches 1V. The  $\overline{\text{RST}}$  and COMPX outputs will remain low until the part is programmed. After programming, if any one of the  $V_X$  inputs is below its programmed threshold,  $\overline{\text{RST}}$  will be a logic low. Once all the  $V_X$  inputs rise above their thresholds, an internal timer is started and  $\overline{\text{RST}}$  is released after the programmed delay time. If  $V_{CC} < (V3 - 1)$  and  $V_{CC} < 2.4V$ , the V3 input impedance will be low (1k $\Omega$  typ).

### Monitor Programming

The LTC2902 input voltage combination is selected by placing the recommended resistor divider from  $V_{REF}$  to GND and connecting the tap point to  $V_{PG}$ , as shown in Figure 4. Table 1 offers recommended 1% resistor values for the various modes. The last column in Table 1 specifies optimum  $V_{PG}/V_{REF}$  ratios ( $\pm 0.01$ ) to be used when programming with a ratiometric DAC.

During power-up, once V1 or V2 reaches 2.4V (max), the monitor enters a programming period of approximately 150 $\mu\text{s}$  during which the voltage on the  $V_{PG}$  pin is sampled and the monitor is configured to the desired input combination. Do not add capacitance to the  $V_{PG}$  pin. Immediately after programming, the comparators are enabled and supply monitoring will begin.

### Supply Monitoring

The LTC2902 is a low power, high accuracy programmable quad supply monitoring circuit with four nondelayed monitor outputs, a common reset output and selectable supply thresholds. Reset timing is adjustable using an external capacitor. Single pin programming selects 1 of 16 input voltage monitor combinations. Two digital inputs select one of four supply tolerances (5%, 7.5%, 10% or 12.5%). All four voltage inputs must be above predetermined thresholds for the reset not to be invoked. The LTC2902 will assert the reset and comparator outputs during power-up, power-down and brownout conditions on any one of the voltage inputs.

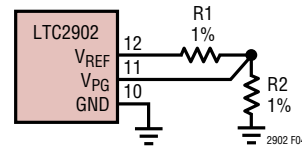


Figure 4. Monitor Programming

Table 1. Voltage Threshold Programming

MODE	V1 (V)	V2 (V)	V3 (V)	V4 (V)	R1 (k $\Omega$ )	R2 (k $\Omega$ )	$\frac{V_{PG}}{V_{REF}}$
0	5.0	3.3	ADJ	ADJ	Open	Short	0.000
1	5.0	3.3	ADJ	-ADJ	93.1	9.53	0.094
2	3.3	2.5	ADJ	ADJ	86.6	16.2	0.156
3	3.3	2.5	ADJ	-ADJ	78.7	22.1	0.219
4	3.3	2.5	1.5	ADJ	71.5	28.0	0.281
5	5.0	3.3	2.5	ADJ	66.5	34.8	0.344
6	5.0	3.3	2.5	1.8	59.0	40.2	0.406
7	5.0	3.3	2.5	1.5	53.6	47.5	0.469
8	5.0	3.0	2.5	ADJ	47.5	53.6	0.531
9	5.0	3.0	ADJ	ADJ	40.2	59.0	0.594
10	3.3	2.5	1.8	1.5	34.8	66.5	0.656
11	3.3	2.5	1.8	ADJ	28.0	71.5	0.719
12	3.3	2.5	1.8	-ADJ	22.1	78.7	0.781
13	5.0	3.3	1.8	-ADJ	16.2	86.6	0.844
14	5.0	3.3	1.8	ADJ	9.53	93.1	0.906
15	5.0	3.0	1.8	ADJ	Short	Open	1.000

The inverting inputs on the V3 and/or V4 comparators are set to 0.5V when the positive adjustable modes are selected and with T0 and T1 low (5% tolerance) (Figure 5). The tap point on an external resistive divider, connected between the positive voltage being sensed and ground, is connected to the high impedance noninverting inputs (V3, V4). The trip voltage is calculated from:

$$V_{TRIP} = 0.5V \left( 1 + \frac{R3}{R4} \right)$$

Once the resistor divider is set in the 5% tolerance mode, there is no need to change the divider for the other tolerance modes (7.5%, 10%, 12.5%) because the internal reference is scaled accordingly, moving the trip point in -2.5% increments.

## APPLICATIONS INFORMATION

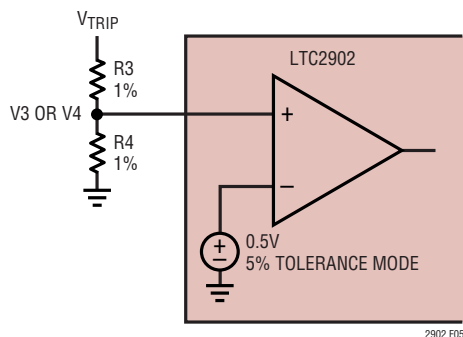


Figure 5. Setting the Positive Adjustable Trip Point

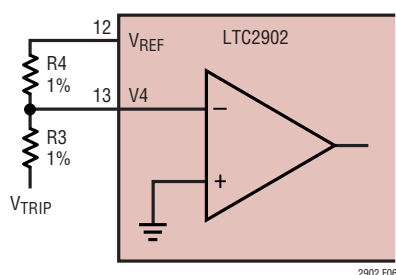


Figure 6. Setting the Negative Adjustable Trip Point

In the negative adjustable mode, the noninverting input on the V4 comparator is connected to ground (Figure 6). The tap point on an external resistive divider, connected between the negative voltage being sensed and the  $V_{REF}$  pin, is connected to the high impedance inverting input (V4).  $V_{REF}$  provides the necessary level shift required to operate at ground. The trip voltage is calculated from:

$$V_{TRIP} = -V_{REF} \left( \frac{R3}{R4} \right); V_{REF} = 1.210V$$

T0, T1 Low (5% Tolerance Mode)

Once the resistor divider is set in the 5% tolerance mode, there is no need to change the divider for the other tolerance modes (7.5%, 10%, 12.5%) because  $V_{REF}$  is scaled accordingly, moving the trip point in  $-2.5\%$  increments.

In a negative adjustable application, the minimum value for R4 is limited by the sourcing capability of  $V_{REF}$  ( $\pm 1\text{mA}$ ). With no other load on  $V_{REF}$ , R4 (minimum) is:

$$1.21V \div 1\text{mA} = 1.21\text{k}\Omega$$

Tables 2 and 3 offer suggested 1% resistor values for various adjustable applications.

Table 2. Suggested 1% Resistor Values for the ADJ Inputs

$V_{SUPPLY}$ (V)	$V_{TRIP}$ (V)	R3 (k $\Omega$ )	R4 (k $\Omega$ )
12	11.25	2150	100
10	9.4	1780	100
8	7.5	1400	100
7.5	7	1300	100
6	5.6	1020	100
5	4.725	845	100
3.3	3.055	511	100
3	2.82	464	100
2.5	2.325	365	100
1.8	1.685	237	100
1.5	1.410	182	100
1.2	1.120	124	100
1	0.933	86.6	100
0.9	0.840	68.1	100

Table 3. Suggested 1% Resistor Values for the -ADJ Input

$V_{SUPPLY}$ (V)	$V_{TRIP}$ (V)	R3 (k $\Omega$ )	R4 (k $\Omega$ )
-2	-1.87	187	121
-5	-4.64	464	121
-5.2	-4.87	487	121
-10	-9.31	931	121
-12	-11.30	1130	121

Although all four supply monitor comparators have built-in glitch immunity, bypass capacitors on V1 and V2 are recommended because the greater of V1 or V2 is also the  $V_{CC}$  for the chip. Filter capacitors on the V3 and V4 inputs are allowed.

### Power-Down

On power-down, once any of the  $V_X$  inputs drop below their threshold,  $\overline{RST}$  and COMPX are held at a logic low. A logic low of 0.4V is guaranteed until both V1 and V2 drop below 1V. If the bandgap reference becomes invalid ( $V_{CC} < 2V$  typ), the part will reprogram once  $V_{CC}$  rises above 2.4V (max).

### Monitor Output Rise and Fall Time Estimation

All of the outputs ( $\overline{RST}$ , COMPX) have strong pull-down capability. If the external load capacitance ( $C_{LOAD}$ ) for a

## APPLICATIONS INFORMATION

particular output is known, output fall time (10% to 90%) is estimated using:

$$t_{\text{FALL}} \approx 2.2 \cdot R_{\text{PD}} \cdot C_{\text{LOAD}}$$

where  $R_{\text{PD}}$  is the on-resistance of the internal pull-down transistor. The typical performance curve ( $V_{\text{OL}}$  vs  $I_{\text{SINK}}$ ) demonstrates that the pull-down current is somewhat linear versus output voltage. Using the 25°C curve,  $R_{\text{PD}}$  is estimated to be approximately 40Ω. Assuming a 150pF load capacitance, the fall time is about 13.2ns.

Although the outputs are considered to be “open-drain,” they do have a weak pull-up capability (see COMPX or RST Pull-Up Current vs V2 curve). Output rise time (10% to 90%) is estimated using:

$$t_{\text{RISE}} \approx 2.2 \cdot R_{\text{PU}} \cdot C_{\text{LOAD}}$$

where  $R_{\text{PU}}$  is the on-resistance of the pull-up transistor. The on-resistance as a function of the V2 voltage at room temperature is estimated using:

$$R_{\text{PU}} = \frac{6 \cdot 10^5}{V_2 - 1} \Omega$$

with  $V_2 = 3.3\text{V}$ ,  $R_{\text{PU}}$  is about 260k. Using 150pF for load capacitance, the rise time is 86μs. If the output needs to pull up faster and/or to a higher voltage, a smaller external pull-up resistor may be used. Using a 10k pull-up resistor, the rise time is reduced to 3.3μs for a 150pF load capacitance.

The LTC2902-2 has an active pull-up to V2 on the  $\overline{\text{RST}}$  output. The typical performance curve ( $\overline{\text{RST}}$  Pull-Up Current vs V2 curve) demonstrates that the pull-up current is somewhat linear versus the V2 voltage and  $R_{\text{PU}}$  is estimated to be approximately 625Ω. A 150pF load capacitance makes the rise time about 206ns.

### Selecting the Reset Timing Capacitor

The reset time-out period is adjustable in order to accommodate a variety of microprocessor applications. The reset time-out period,  $t_{\text{RST}}$ , is adjusted by connecting a capacitor,  $C_{\text{RT}}$ , between the CRT pin and ground. The value of this capacitor is determined by:

$$C_{\text{RT}} = t_{\text{RST}} \cdot 217 \cdot 10^{-9}$$

with  $C_{\text{RT}}$  in Farads and  $t_{\text{RST}}$  in seconds. The  $C_{\text{RT}}$  value per millisecond of delay can also be expressed as  $C_{\text{RT}}/\text{ms} = 217$  (pF/ms).

Leaving the CRT pin unconnected will generate a minimum reset time-out of approximately 50μs. Maximum reset time-out is limited by the largest available low leakage capacitor. The accuracy of the time-out period will be affected by capacitor leakage (the nominal charging current is 2μA) and capacitor tolerance. A low leakage ceramic capacitor is recommended.

### Tolerance Programming and the RESET Disable

Using the two digital inputs T0 and T1, the user can program the global supply tolerance for the LTC2902 (5%, 7.5%, 10%, 12.5%). The larger tolerances provide more headroom by lowering the trip thresholds.

**Table 4. Tolerance Programming**

T0	T1	TOLERANCE (%)	V <sub>REF</sub> (V)
Low	Low	5	1.210
Low	High	7.5	1.178
High	Low	10	1.146
High	High	12.5	1.113

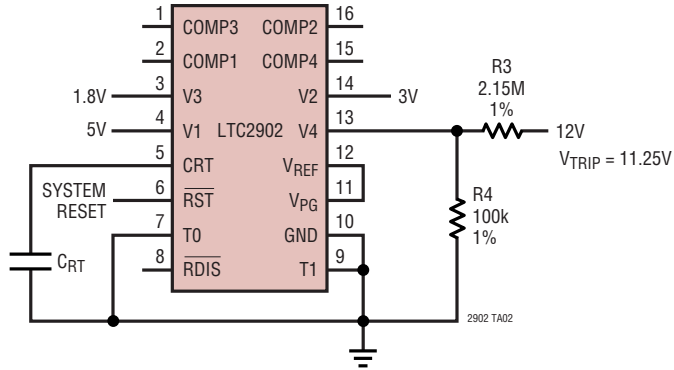
Under conventional operation,  $\overline{\text{RST}}$  and COMPX will go low when  $V_X$  is below its threshold. At any time, the  $\overline{\text{RDIS}}$  pin can be pulled low, overriding the reset operation and forcing the  $\overline{\text{RST}}$  pin high. This feature is useful when determining supply margins under processor control since the reset command will not be invoked. The  $\overline{\text{RDIS}}$  pin is connected to a weak internal pull-up to  $V_{\text{CC}}$  (10μA typ), allowing the pin to be left floating if unused.

### Ensuring $\overline{\text{RST}}$ Valid for $V_{\text{CC}}$ Down to 0V (LTC2902-2)

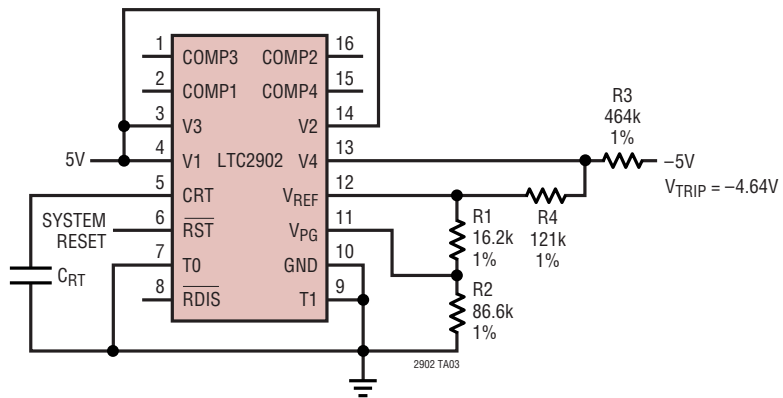
When  $V_{\text{CC}}$  is below 1V the  $\overline{\text{RST}}$  pull-down capability is drastically reduced. The  $\overline{\text{RST}}$  pin may float to undetermined voltages when connected to high impedance (such as CMOS logic inputs). The addition of a pull-down resistor from  $\overline{\text{RST}}$  to ground will provide a path for stray charge and/or leakage currents. The resistor value should be small enough to provide effective pull-down without excessively loading the pull-up circuitry. Too large a value may not pull down well enough. A 100k resistor from  $\overline{\text{RST}}$  to ground is satisfactory for most applications.

TYPICAL APPLICATIONS

**Quad Supply Monitor, 5% Tolerance**  
**5V, 3V, 1.8V, 12V (ADJ)**

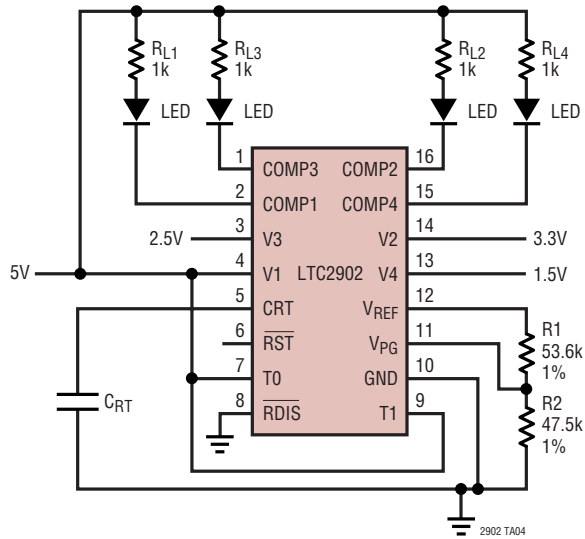


**5V, -5V Monitor with Unused V2, V3 Inputs Pulled**  
**Above Trip Thresholds (5% Tolerance)**



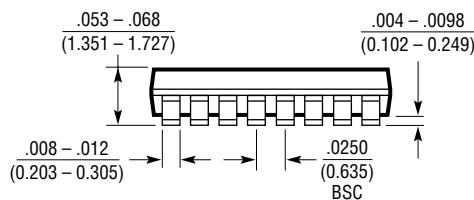
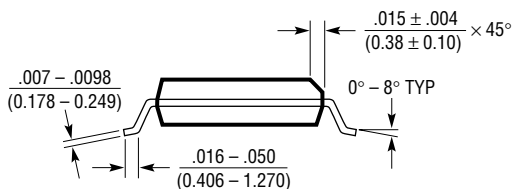
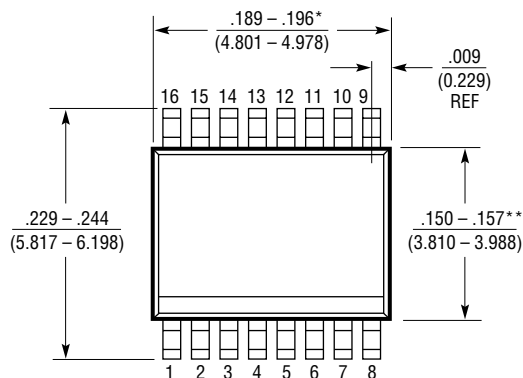
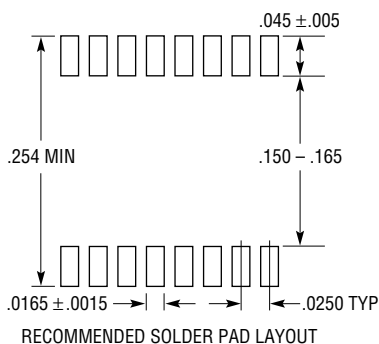
**TYPICAL APPLICATIONS**

**Quad Supply Monitor with LED Undervoltage Indicators,  
12.5% Tolerance, Reset Disabled  
5V, 3.3V, 2.5V, 1.5V**



# PACKAGE DESCRIPTION

## GN Package 16-Lead Plastic SSOP (Narrow .150 Inch) (Reference LTC DWG # 05-08-1641)



**NOTE:**

1. CONTROLLING DIMENSION: INCHES

2. DIMENSIONS ARE IN  $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$

3. DRAWING NOT TO SCALE

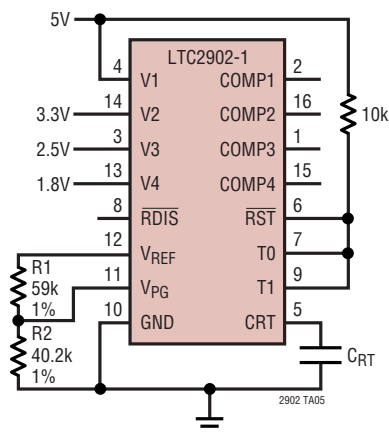
\*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

\*\*DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 0502

## TYPICAL APPLICATION

**Quad Supply Monitor with Hysteresis**  
**5% Tolerance (Supplies Rising)**  
**12.5% Tolerance (After RST Goes High)**



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC690	5V Supply Monitor, Watchdog Timer and Battery Backup	4.65V Threshold
LTC694-3.3	3.3V Supply Monitor, Watchdog Timer and Battery Backup	2.9V Threshold
LTC699	5V Supply Monitor and Watchdog Timer	4.65V Threshold
LTC1232	5V Supply Monitor, Watchdog Timer and Push-Button Reset	4.37V/4.62V Threshold
LTC1326	Micropower Precision Triple Supply Monitor for 5V, 3.3V and ADJ	4.725V, 3.118V, 1V Thresholds ( $\pm 0.75\%$ )
LTC1326-2.5	Micropower Precision Triple Supply Monitor for 2.5V, 3.3V and ADJ	2.363V, 3.118V, 1V Thresholds ( $\pm 0.75\%$ )
LTC1536	Precision Triple Supply Monitor for PCI Applications	Meets PCI $t_{FAIL}$ Timing Specifications
LTC1726-2.5	Micropower Triple Supply Monitor for 2.5V, 3.3V and ADJ	Adjustable $\overline{RESET}$ and Watchdog Time-Outs
LTC1726-5	Micropower Triple Supply Monitor for 5V, 3.3V and ADJ	Adjustable $\overline{RESET}$ and Watchdog Time-Outs
LTC1727-2.5/LTC1727-5	Micropower Triple Supply Monitor with Open-Drain Reset	Individual Monitor Outputs in MSOP
LTC1728-1.8/LTC1728-3.3	Micropower Triple Supply Monitor with Open-Drain Reset	5-Lead SOT-23 Package
LTC1728-2.5/LTC1728-5	Micropower Triple Supply Monitor with Open-Drain Reset	5-Lead SOT-23 Package
LTC1985-1.8	Micropower Triple Supply Monitor with Push-Pull Reset Output	5-Lead SOT-23 Package
LTC2900	Programmable Quad Supply Monitor	Adjustable $\overline{RESET}$ , 10-Lead MSOP Package
LTC2901	Programmable Quad Supply Monitor	Adjustable $\overline{RESET}$ and Watchdog Timer, 16-Lead SSOP Package

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- ⊖ [View LTC2902-1CGN#TRPBF on WIN SOURCE](#)
- ⊖ [Linear Technology Information](#)

## Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management