THE DATASHEET OF

LTC3612EUDC#PBF

www.win-source.net 0086-755-83957316

3A, 4MHz Monolithic Synchronous Step-Down DC/DC Converter

FEATURES

- **3A Output Current**
- **2.25V to 5.5V Input Voltage Range**
- **Low Output Ripple Burst Mode® Operation: I_Q = 70µA**
- **±1% Output Voltage Accuracy**
- **Output Voltage Down to 0.6V**
- **High Efficiency: Up to 95%**
- Low Dropout Operation: 100% Duty Cycle
- Shutdown Current: ≤1µA
- Adjustable Switching Frequency: Up to 4MHz
- Optional Active Voltage Positioning (AVP) with Internal Compensation
- Selectable Pulse-Skipping/Forced Continuous/ Burst Mode Operation with Adjustable Burst Clamp
- Programmable Soft-Start
- Inputs for Start-Up Tracking or External Reference
- DDR Memory Mode, I_{OUT} = ±1.5A
- Available in Thermally Enhanced 20-Pin (3mm × 4mm) QFN and TSSOP Packages

APPLICATIONS

- Point-of-Load Supplies
- Distributed Power Supplies
- Portable Computer Systems
- DDR Memory Termination
- Handheld Devices

DESCRIPTION

The LTC®3612 is a low quiescent current monolithic synchronous buck regulator using a current mode, constant frequency architecture. The no-load DC supply current in sleep mode is only 70µA while maintaining the output voltage (Burst Mode operation) at no load, dropping to zero current in shutdown. The 2.25V to 5.5V input supply voltage range makes the LTC3612 ideally suited for single Li-Ion as well as fixed low voltage input applications. 100% duty cycle capability provides low dropout operation, extending the operating time in battery-powered systems.

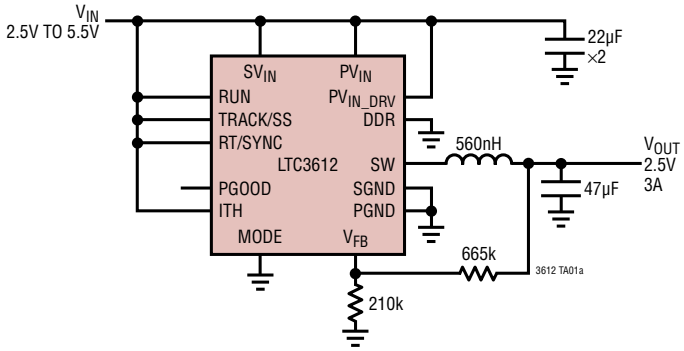
The operating frequency is externally programmable up to 4MHz, allowing the use of small surface mount inductors. For switching noise-sensitive applications, the LTC3612 can be synchronized to an external clock at up to 4MHz.

Forced continuous mode operation in the LTC3612 reduces noise and RF interference. Adjustable compensation allows the transient response to be optimized over a wide range of loads and output capacitors.

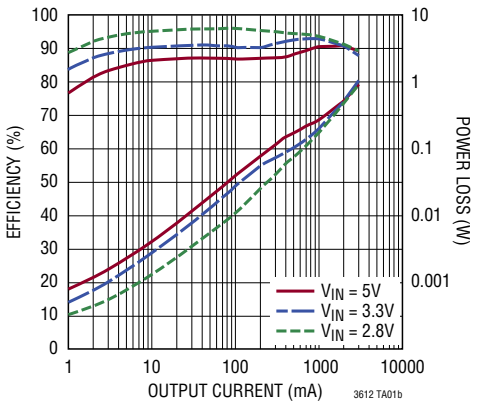
The internal synchronous switch increases efficiency and eliminates the need for an external catch diode, saving external components and board space. The LTC3612 is offered in a leadless 20-pin 3mm × 4mm QFN or a thermally enhanced 20-pin TSSOP package.

, LT, LTC, LTM, Burst Mode, Linear Technology and the Linear logo are registered trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners. Protected by U.S. Patents, including 6580258, 5481178, 5994885, 6304066, 6498466, 6611131.

TYPICAL APPLICATION



Efficiency and Power Loss vs Load Current

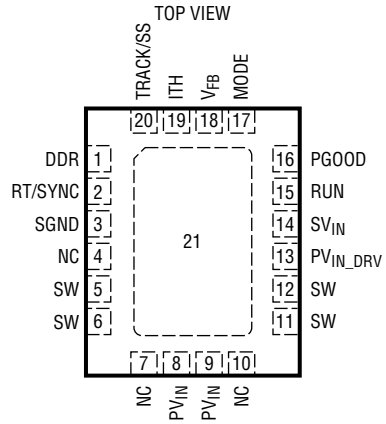


ABSOLUTE MAXIMUM RATINGS (Note 1)

PV_{IN}, SV_{IN}, PV_{IN_DRV} Voltages ..... –0.3V to 6V
SW Voltage .....–0.3V to (PV_{IN} + 0.3V)
ITH, RT/SYNC Voltages..... –0.3V to (SV_{IN} + 0.3V)
DDR, TRACK/SS Voltages..... –0.3V to (SV_{IN} + 0.3V)
MODE, RUN, V_{FB} Voltages ..... –0.3V to (SV_{IN} + 0.3V)
PGOOD Voltage..... –0.3V to 6V

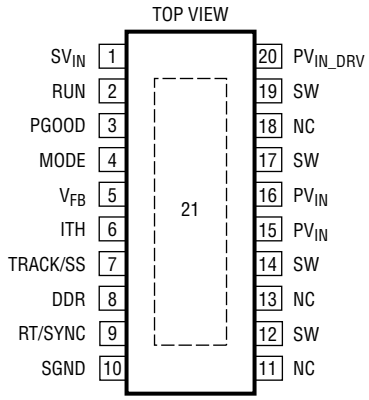
Operating Junction Temperature Range
(Notes 2, 11)..... –55°C to 150°C
Storage Temperature..... –65°C to 150°C
Reflow Peak Body Temperature (QFN) ..... 260°C
Lead Temperature (Soldering, 10 sec)
TSSOP ..... 300°C

PIN CONFIGURATION



UDC PACKAGE
20-LEAD (3mm × 4mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 21) IS PGND, MUST BE SOLDERED TO PCB



FE PACKAGE
20-LEAD PLASTIC TSSOP

T_{JMAX} = 150°C, θ_{JA} = 38°C/W
EXPOSED PAD (PIN 21) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3612EUDC#PBF	LTC3612EUDC#TRPBF	LDQT	20-Lead (3mm × 4mm) Plastic QFN	–40°C to 125°C
LTC3612IUDC#PBF	LTC3612IUDC#TRPBF	LDQT	20-Lead (3mm × 4mm) Plastic QFN	–40°C to 125°C
LTC3612HUDC#PBF	LTC3612HUDC#TRPBF	LDQT	20-Lead (3mm × 4mm) Plastic QFN	–40°C to 150°C
LTC3612MPUDC#PBF	LTC3612MPUDC#TRPBF	LDQT	20-Lead (3mm × 4mm) Plastic QFN	–55°C to 150°C
LTC3612EFE#PBF	LTC3612EFE#TRPBF	LTC3612FE	20-Lead Plastic TSSOP	–40°C to 125°C
LTC3612IFE#PBF	LTC3612IFE#TRPBF	LTC3612FE	20-Lead Plastic TSSOP	–40°C to 125°C
LTC3612HFE#PBF	LTC3612HFE#TRPBF	LTC3612FE	20-Lead Plastic TSSOP	–40°C to 150°C
LTC3612MPFE#PBF	LTC3612MPFE#TRPBF	LTC3612FE	20-Lead Plastic TSSOP	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 3.3V, RT/SYNC = SV_{IN}, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Voltage Range		●	2.25		5.5	V
V_{UVLO}	Undervoltage Lockout Threshold	SV_{IN} Ramping Down SV_{IN} Ramping Up	● ●	1.7		 2.25	V V
V_{FB}	Feedback Voltage Internal Reference	(Notes 3, 4) $V_{TRACK/SS}$ = SV_{IN}, V_{DDR} = 0V 0°C < T_J < 85°C –40°C < T_J < 125°C –55°C < T_J < 150°C	 ● ●	 0.594 0.591 0.589	 0.6 	 0.606 0.609 0.611	 V V V
	Feedback Voltage External Reference (Note 7)	(Notes 3, 4) $V_{TRACK/SS}$ = 0.3V, V_{DDR} = SV_{IN}		0.289	0.3	0.311	V
		(Notes 3, 4) $V_{TRACK/SS}$ = 0.5V, V_{DDR} = SV_{IN}		0.489	0.5	0.511	V
I_{FB}	Feedback Input Current	V_{FB} = 0.6V	●			±30	nA
$\Delta V_{LINEREG}$	Line Regulation	SV_{IN} = PV_{IN} = 2.25V to 5.5V (Notes 3, 4) TRACK/SS = SV_{IN}	●			0.2	%/V
$\Delta V_{LOADREG}$	Load Regulation	ITH from 0.5V to 0.9V (Notes 3, 4) V_{ITH} = SV_{IN} (Note 5)				0.25 2.6	% %
I_S	Active Mode	V_{FB} = 0.5V, V_{MODE} = SV_{IN} (Note 6)			1100		µA
	Sleep Mode	V_{FB} = 0.7V, V_{MODE} = 0V, ITH = SV_{IN} (Note 5)			70	100	µA
		V_{FB} = 0.7V, V_{MODE} = 0V (Note 4)			120	160	µA
	Shutdown	SV_{IN} = PV_{IN} = 5.5V, V_{RUN} = 0V			0.1	1	µA
$R_{DS(ON)}$	Top Switch On-Resistance	PV_{IN} = 3.3V (Note 10)			70		mΩ
	Bottom Switch On-Resistance	PV_{IN} = 3.3V (Note 10)			45		mΩ
I_{LIM}	Top Switch Current Limit	Sourcing (Note 8), V_{FB} = 0.5V Duty Cycle <35% Duty Cycle = 100%		 5.2 3.7	 6 	 6.8 	 A A
	Bottom Switch Current Limit	Sinking (Note 8), V_{FB} = 0.7V, Forced Continuous Mode		–3	–4	–5	A
$g_{m(EA)}$	Error Amplifier Transconductance	–5µA < I_{ITH} < 5µA (Note 4)			200		µS
I_{EAO}	Error Amplifier Max Output Current	(Note 4)			±30		µA
t_{SS}	Internal Soft-Start Time	V_{FB} from 0.06V to 0.54V, TRACK/SS = SV_{IN}		0.65	1	1.5	ms
$V_{TRACK/SS}$	Enable Internal Soft-Start	(Note 7)		0.62			V
t_{TRACK/SS_DIS}	Soft-Start Discharge Time at Start-Up			70			µs
$R_{ON(TRACK/SS_DIS)}$	TRACK/SS Pull-Down Resistor at Start-Up					200	Ω
f_{OSC}	Oscillator Frequency	RT/SYNC = 370k	●	0.8	1	1.2	MHz
	Internal Oscillator Frequency	$V_{RT/SYNC}$ = SV_{IN}	●	1.8	2.25	2.7	MHz
f_{SYNC}	Synchronization Frequency			0.3		4	MHz
$V_{RT/SYNC}$	SYNC Level High			1.2			V
	SYNC Level Low			.		0.3	V
$I_{SW(LKG)}$	Switch Leakage Current	SV_{IN} = PV_{IN} = 5.5V, V_{RUN} = 0V			0.1	1	µA
V_{DDR}	DDR Option Enable Voltage			SV_{IN} – 0.3			V
V_{MODE} (Note 9)	Internal Burst Mode Operation					0.3	V
	Pulse-Skipping Mode			SV_{IN} – 0.3			V
	Forced Continuous Mode			1.1		SV_{IN} • 0.58	V
	External Burst Mode Operation			0.45		0.8	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 3.3V, RT/SYNC = SV_{IN}, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PGOOD	Power Good Voltage Windows	TRACK/SS = SV_{IN}, Entering Window					
		V_{FB} Ramping Up		–3.5	–6		%
		V_{FB} Ramping Down		3.5	6		%
		TRACK/SS = SV_{IN}, Leaving Window					
		V_{FB} Ramping Up			9	11	%
		V_{FB} Ramping Down			–9	–11	%
t_{PGOOD}	Power Good Blanking Time	Entering and Leaving Window		70	105	140	µs
R_{PGOOD}	Power Good Pull-Down On-Resistance			8	17	33	Ω
V_{RUN}	RUN Voltage	Input High	●	1			V
		Input Low	●			0.4	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3612 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3612E is guaranteed to meet performance specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3612I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LTC3612H is guaranteed to meet specifications over the –40°C to 150°C operating temperature range. The LTC3612MP is guaranteed and tested to meet specifications over the full –55°C to 150°C operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature
(T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA}),$$

where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: This parameter is tested in a feedback loop which servos V_{FB} to the midpoint for the error amplifier (V_{ITH} = 0.75V).

Note 4: External compensation on ITH pin.

Note 5: Tying the ITH pin to SV_{IN} enables the internal compensation and AVP mode.

Note 6: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

Note 7: See description of the TRACK/SS pin in the Pin Functions section.

Note 8: In sourcing mode the average output current is flowing out of SW pin. In sinking mode the average output current is flowing into the SW Pin.

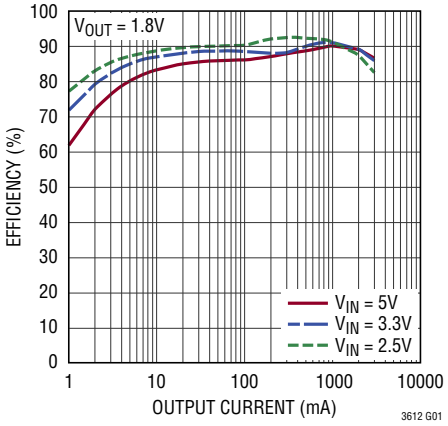
Note 9: See description of the MODE pin in the Pin Functions section.

Note 10: Guaranteed by correlation and design to wafer level measurements for QFN packages.

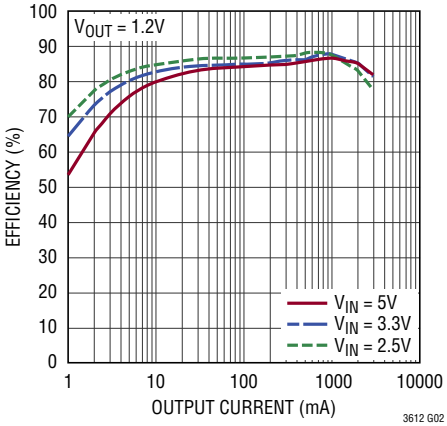
Note 11: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS V_{IN} = 3.3V, RT/SYNC = SV_{IN}, unless otherwise noted.

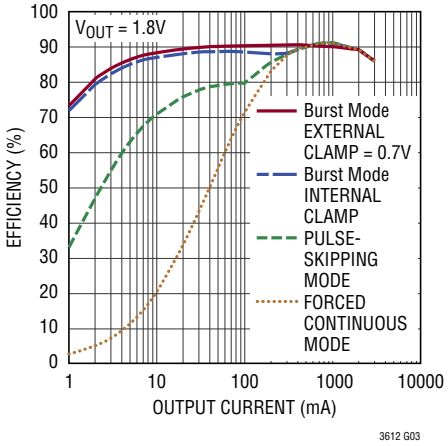
Efficiency vs Load Current (V_{MODE} = 0V)



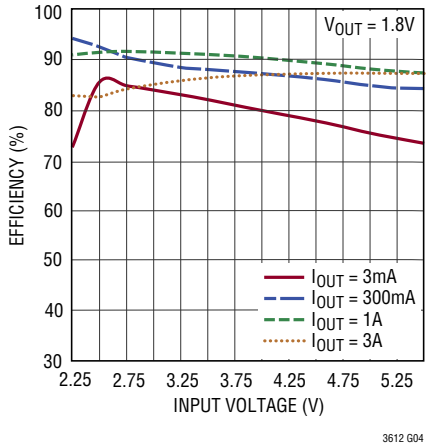
Efficiency vs Load Current (V_{MODE} = 0V)



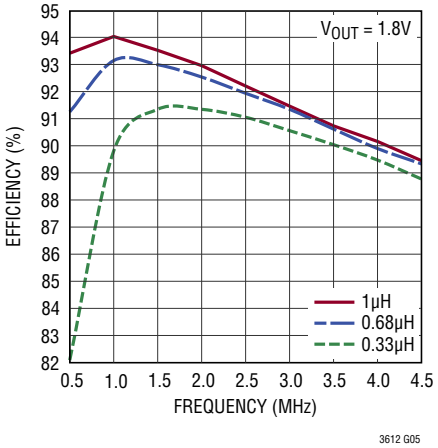
Efficiency vs Load Current



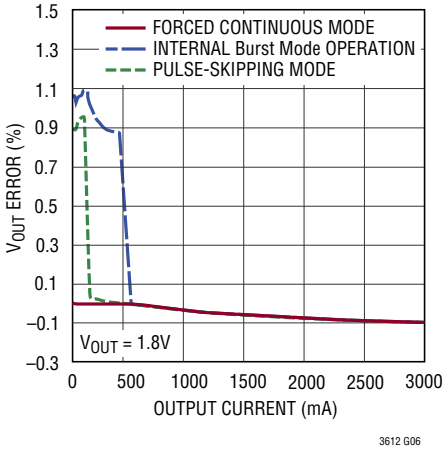
Efficiency vs Input Voltage (V_{MODE} = 0V)



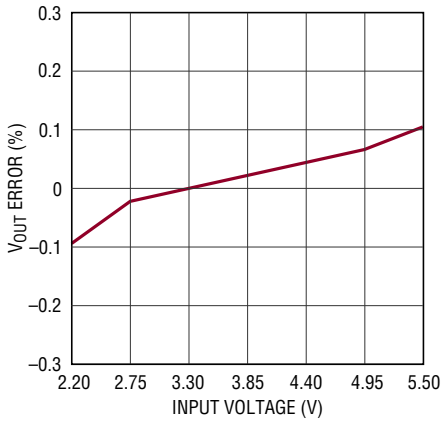
Efficiency vs Frequency (V_{MODE} = 0V), I_{OUT} = 1A



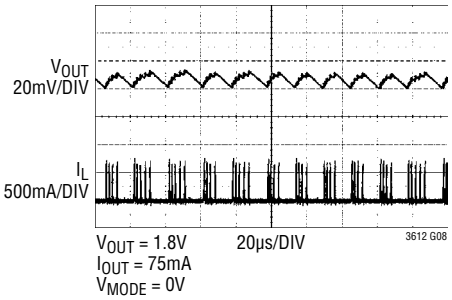
Load Regulation



Line Regulation

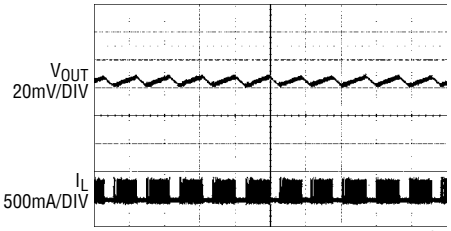


Burst Mode Operation



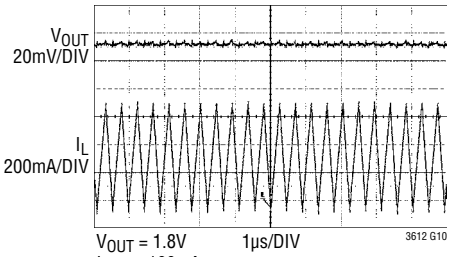
TYPICAL PERFORMANCE CHARACTERISTICS V_{IN} = 3.3V, RT/SYNC = SV_{IN}, unless otherwise noted.

Pulse-Skipping Mode Operation



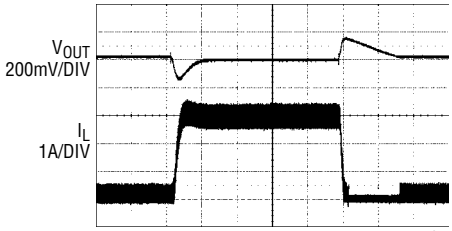
V_{OUT} = 1.8V 20µs/DIV
I_{OUT} = 75mA
V_{MODE} = 3.3V

Forced Continuous Mode Operation



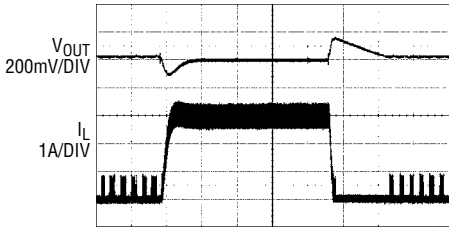
V_{OUT} = 1.8V 1µs/DIV
I_{OUT} = 100mA
V_{MODE} = 1.5V

Load Step Transient in Pulse-Skipping Mode



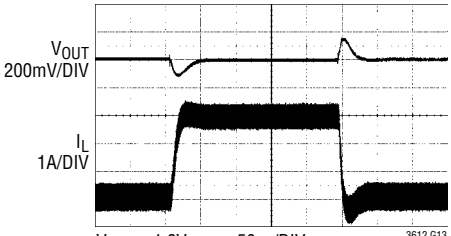
V_{OUT} = 1.8V 50µs/DIV
I_{LOAD} = 100mA TO 3A
V_{MODE} = 3.3V
COMPENSATION FIGURE 1

Load Step Transient in Burst Mode Operation



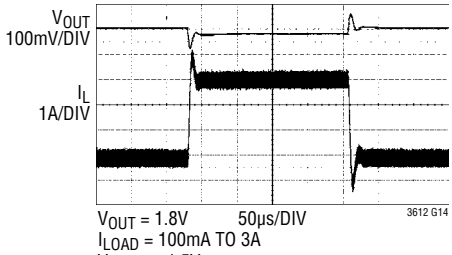
V_{OUT} = 1.8V 50µs/DIV
I_{LOAD} = 100mA TO 3A
V_{MODE} = 0V
COMPENSATION FIGURE 1

Load Step Transient in Forced Continuous Mode without AVP Mode



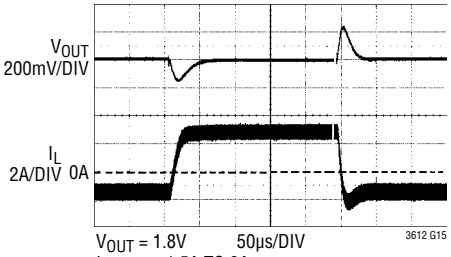
V_{OUT} = 1.8V 50µs/DIV
I_{LOAD} = 100mA TO 3A
V_{MODE} = 1.5V
COMPENSATION FIGURE 1

Load Step Transient in Forced Continuous Mode with AVP Mode



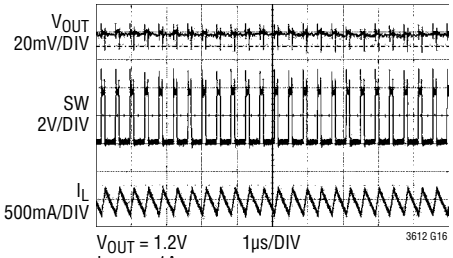
V_{OUT} = 1.8V 50µs/DIV
I_{LOAD} = 100mA TO 3A
V_{MODE} = 1.5V
V_{ITH} = V_{IN}
OUTPUT CAPACITOR VALUE FIGURE 1

Load Step Transient in Forced Continuous Mode Sourcing and Sinking Current



V_{OUT} = 1.8V 50µs/DIV
I_{LOAD} = –1.5A TO 3A
V_{MODE} = 1.5V
COMPENSATION FIGURE 1

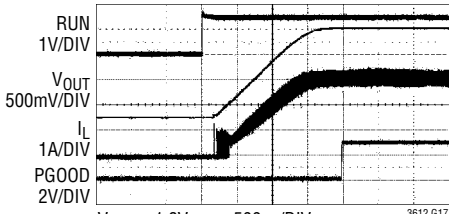
Sinking Current



V_{OUT} = 1.2V 1µs/DIV
I_{OUT} = –1A
V_{MODE} = 1.5V

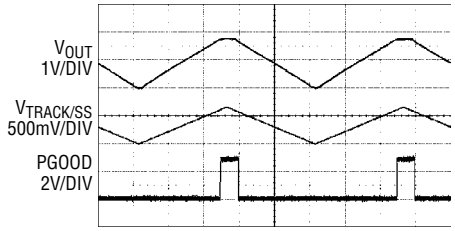
TYPICAL PERFORMANCE CHARACTERISTICS V_{IN} = 3.3V, RT/SYNC = SV_{IN}, unless otherwise noted.

Internal Start-Up in Forced Continuous Mode



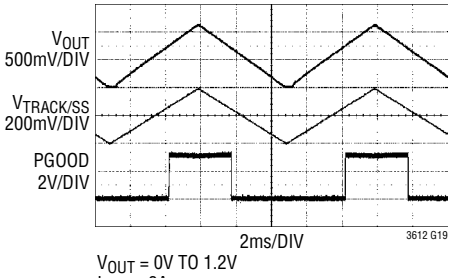
V_{OUT} = 1.8V 500µs/DIV
I_{OUT} = 3A
V_{MODE} = 1.5V

Tracking Up/Down in Forced Continuous Mode, DDR Pin Tied to 0V



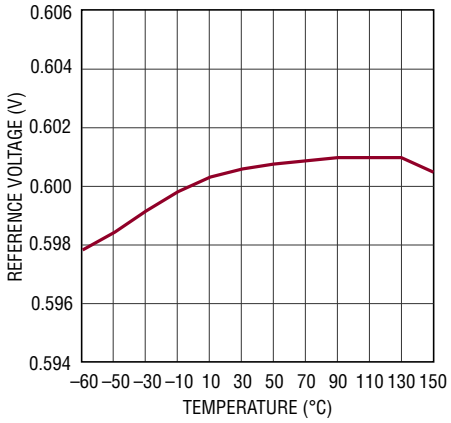
V_{OUT} = 0V TO 1.8V
I_{OUT} = 3A
$V_{TRACK/SS}$ = 0V TO 0.7V
V_{MODE} = 1.5V
V_{DDR} = 0V

Tracking Up/Down in Forced Continuous Mode, DDR Pin Tied to SV_{IN}

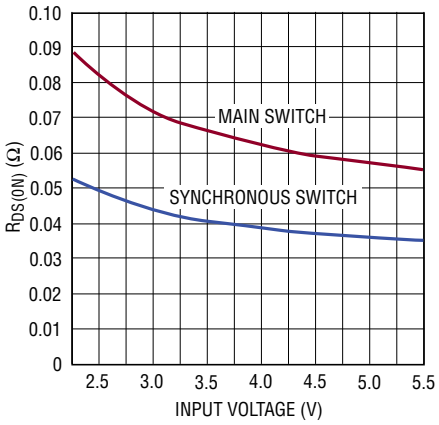


V_{OUT} = 0V TO 1.2V
I_{OUT} = 3A
$V_{TRACK/SS}$ = 0V TO 0.4V
V_{MODE} = 1.5V
V_{DDR} = 3.3V

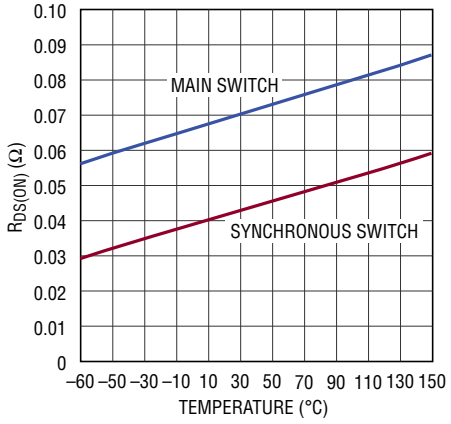
Reference Voltage vs Temperature



Switch On-Resistance vs Input Voltage

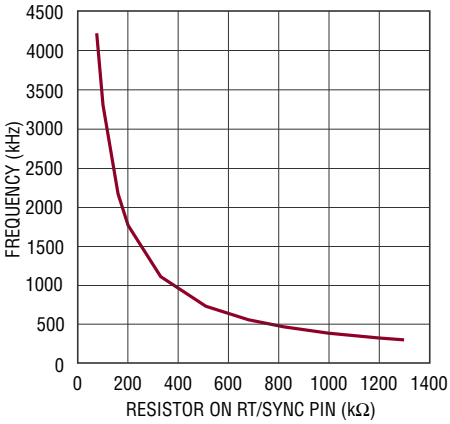


Switch On-Resistance vs Temperature

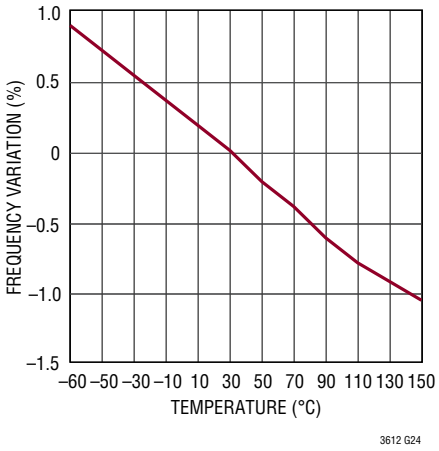


TYPICAL PERFORMANCE CHARACTERISTICS V_{IN} = 3.3V, RT/SYNC = SV_{IN}, unless otherwise noted.

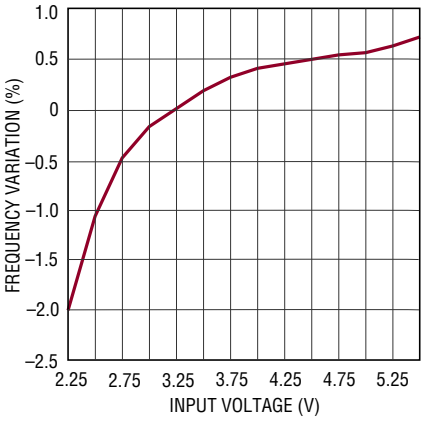
Frequency vs Resistor on RT/SYNC Pin



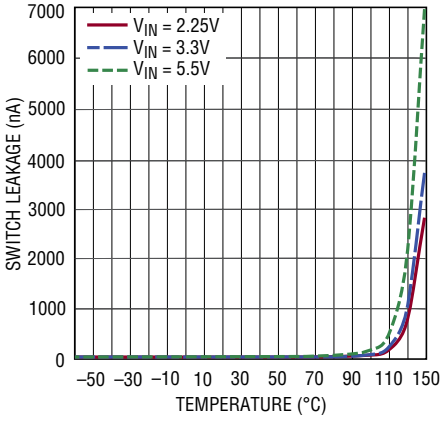
Frequency vs Temperature



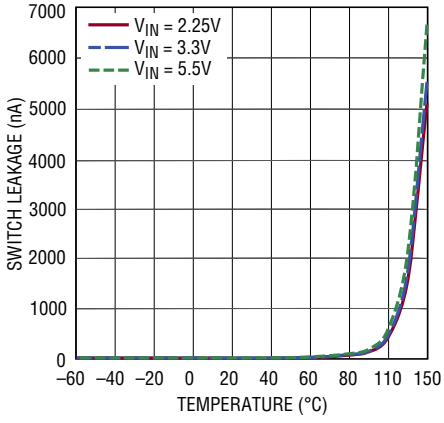
Frequency vs Input Voltage



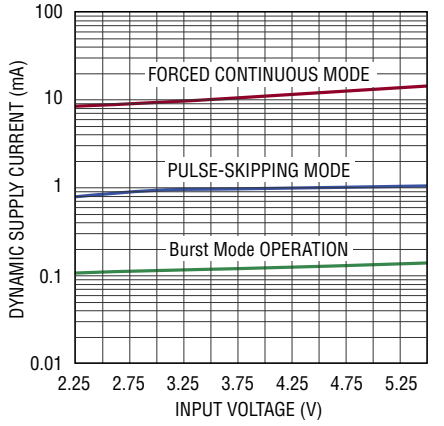
Switch Leakage vs Temperature, Main Switch



Switch Leakage vs Temperature, Synchronous Switch

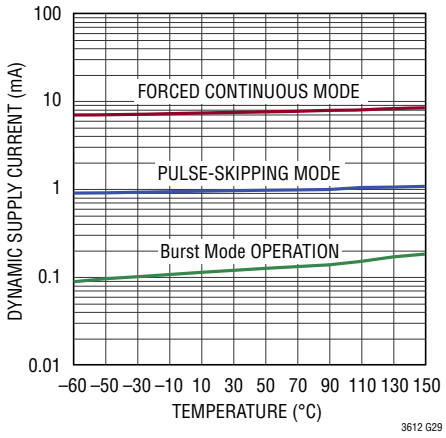


Dynamic Supply Current vs Input Voltage without AVP Mode

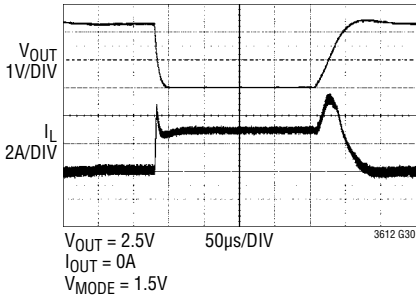


TYPICAL PERFORMANCE CHARACTERISTICS V_{IN} = 3.3V, RT/SYNC = SV_{IN}, unless otherwise noted.

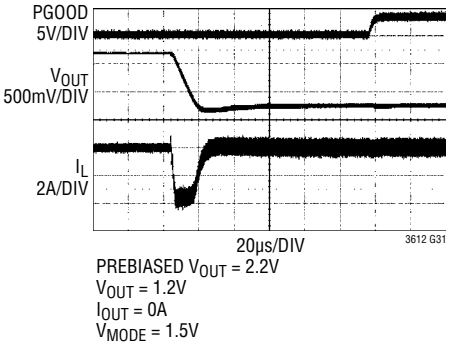
Dynamic Supply Current vs Temperature without AVP Mode



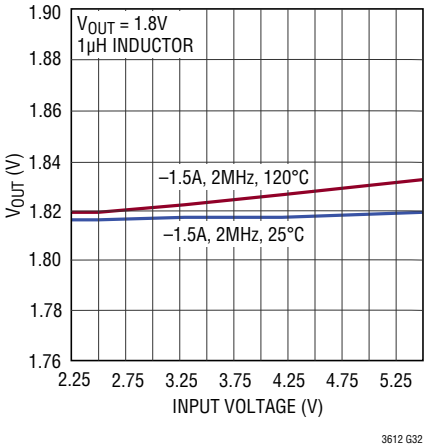
V_{OUT} Short to GND, Forced Continuous Mode



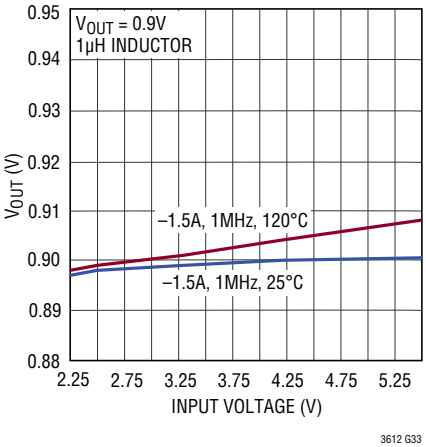
Start-Up from Shutdown with Prebiased Output (Forced Continuous Mode)



Output Voltage During Sinking vs Input Voltage



Output Voltage During Sinking vs Input Voltage



PIN FUNCTIONS (QFN/FE)

DDR (Pin 1/Pin 8): DDR Mode Pin. Tying the DDR pin to SV_{IN} selects DDR mode and TRACK/SS can be used as an external reference input. If DDR is tied to SGND, the internal 0.6V reference will be used.

RT/SYNC (Pin 2/Pin 9): Oscillator Frequency. This pin provides three ways of setting the constant switching frequency:

1. Connecting a resistor from RT/SYNC to ground will set the switching frequency based on the resistor value.
2. Driving the RT/SYNC pin with an external clock signal will synchronize the LTC3612 to the applied frequency. The slope compensation is automatically adapted to the external clock frequency.
3. Tying the RT/SYNC pin to SV_{IN} enables the internal 2.25MHz oscillator frequency.

SGND (Pin 3/Pin 10): Signal Ground. All small-signal and compensation components should connect to this ground, which in turn should connect to PGND at a single point.

NC (Pins 4, 7, 10/Pins 11, 13, 18): Can be connected to ground or left open.

SW (Pins 5, 6, 11, 12/Pins 12, 14, 17, 19): Switch Node. Connection to the inductor. This pin connects to the drains of the internal synchronous power MOSFET switches.

PV_{IN} (Pins 8, 9/Pins 15, 16): Power Input Supply. PV_{IN} connects to the source of the internal P-channel power MOSFET. This pin is independent of SV_{IN} and may be connected to the same voltage or to a lower voltage supply.

PV_{IN_DRV} (Pin 13/Pin 20): Internal Gate Driver Input Supply. This pin must be connected to PV_{IN}.

SV_{IN} (Pin 14/Pin 1): Signal Input Supply. This pin powers the internal control circuitry and is monitored by the undervoltage lockout comparator.

RUN (Pin 15/Pin 2): Enable Pin. Forcing this pin to ground shuts down the LTC3612. In shutdown, all functions are disabled and the chip draws <1µA of supply current.

PGOOD (Pin 16/Pin 3): Power Good. This open-drain output is pulled down to SGND on start-up and while the FB voltage is outside the power good voltage window. If the FB voltage increases and stays inside the power good window for more than 105µs the PGOOD pin is released. If the FB voltage leaves the power good window for more than 105µs the PGOOD pin is pulled down.

In DDR mode (DDR = V_{IN}), the power good window moves in relation to the actual TRACK/SS pin voltage. During up/down tracking the PGOOD pin is always pulled down.

In shutdown the PGOOD output will actively pull down and may be used to discharge the output capacitors via an external resistor.

MODE (Pin 17/Pin 4): Mode Selection. Tying the MODE pin to SV_{IN} or SGND enables pulse-skipping mode or Burst Mode operation (with an internal Burst Mode clamp), respectively. If this pin is held at slightly higher than half of SV_{IN}, forced continuous mode is selected. Connecting this pin to an external voltage selects Burst Mode operation with the burst clamp set to the pin voltage. See the Operation section for more details.

V_{FB} (Pin 18/Pin 5): Voltage Feedback Input Pin. Senses the feedback voltage from the external resistive divider across the output.

ITH (Pin 19/Pin 6): Error Amplifier Compensation. The current comparator's threshold increases with this control voltage. Tying this pin to SV_{IN} enables internal compensation and AVP mode.

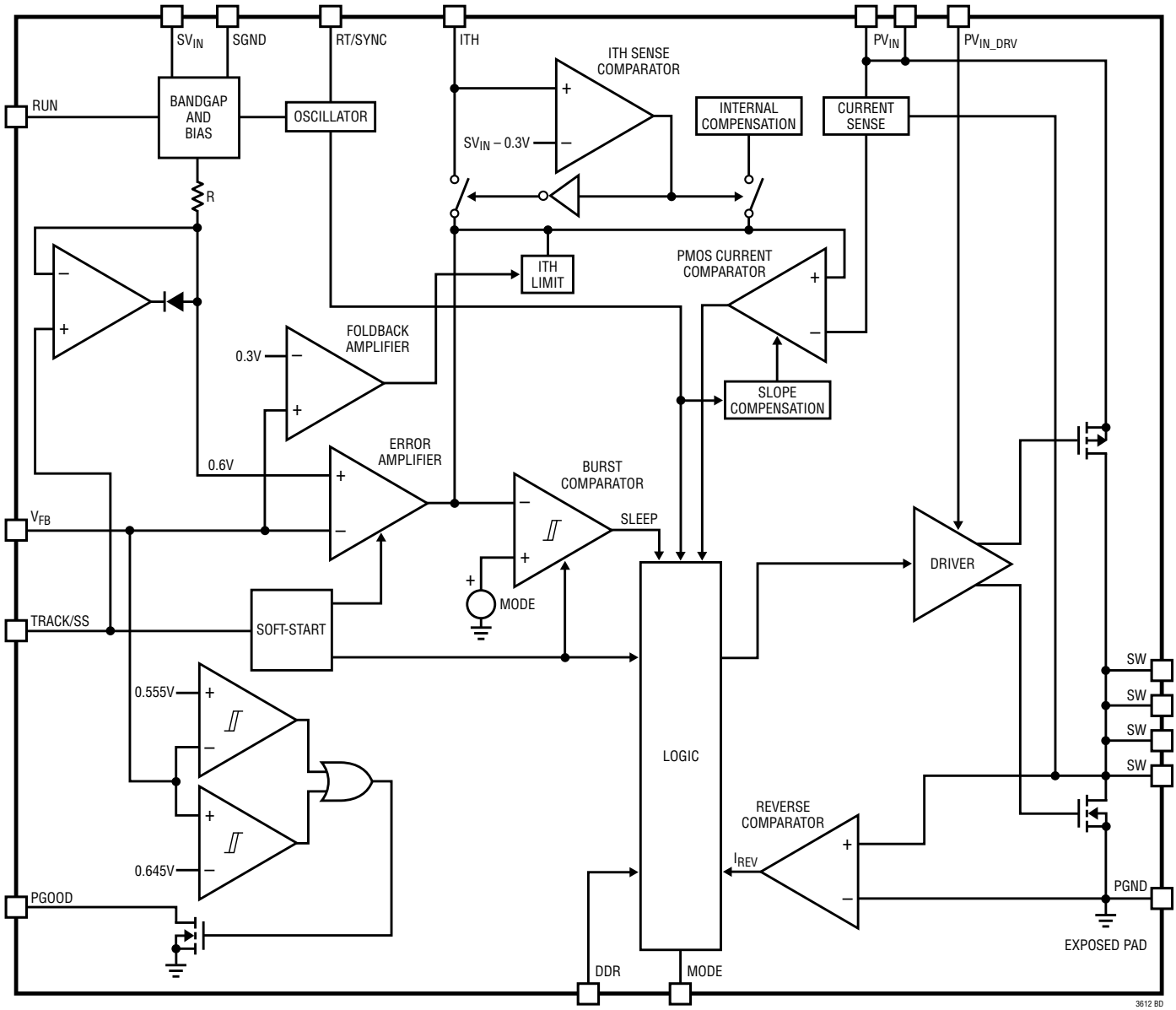
TRACK/SS (Pin 20/Pin 7): Track/External Soft-Start/External Reference. Start-up behavior is programmable with the TRACK/SS pin:

1. Tying this pin to SV_{IN} selects the internal soft-start circuit.
2. External soft-start timing can be programmed with a capacitor to ground and a resistor to SV_{IN}.
3. TRACK/SS can be used to force the LTC3612 to track the start-up behavior of another supply.

The pin can also be used as external reference input. See the Applications Information section for more information.

PGND (Pin 21/Pin 21): Power Ground. The exposed pad connects to the source of the internal N-channel power MOSFET. This pin should be connected close to the (–) terminal of C_{IN} and C_{OUT} and soldered to PCB ground for rated thermal performance.

FUNCTIONAL BLOCK DIAGRAM



OPERATION

Main Control Loop

The LTC3612 is a monolithic, constant frequency, current mode step-down DC/DC converter. During normal operation, the internal top power switch (P-channel MOSFET) is turned on at the beginning of each clock cycle. Current in the inductor increases until the current comparator trips and turns off the top power switch. The peak inductor current at which the current comparator trips is controlled by the voltage on the ITH pin. The error amplifier adjusts the voltage on the ITH pin by comparing the feedback signal from a resistor divider on the V_{FB} pin with an internal 0.6V reference. When the load current increases, it causes a reduction in the feedback voltage relative to the reference. The error amplifier raises the ITH voltage until the average inductor current matches the new load current. Typical voltage range for the ITH pin is from 0.1V to 1.05V with 0.45V corresponding to zero current.

When the top power switch shuts off, the synchronous power switch (N-channel MOSFET) turns on until either the bottom current limit is reached or the next clock cycle begins. The bottom current limit is typically set at –4A for forced continuous mode and 0A for Burst Mode operation and pulse-skipping mode.

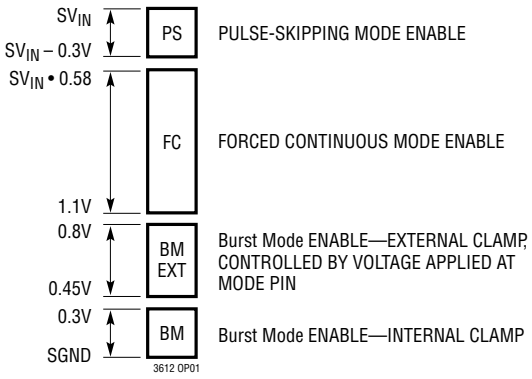
The operating frequency defaults to 2.25MHz when RT/SYNC is connected to SV_{IN}, or can be set by an external resistor connected between the RT/SYNC pin and ground, or by a clock signal applied to the RT/SYNC pin. The switching frequency can be set from 300kHz to 4MHz.

Overvoltage and undervoltage comparators pull the PGOOD output low if the output voltage varies typically more than ±7.5% from the set point.

Mode Selection

The MODE pin is used to select one of four different operating modes:

Mode Selection Voltage



Burst Mode Operation—Internal Clamp

Connecting the MODE pin to SGND enables Burst Mode operation with an internal clamp. In Burst Mode operation the internal power switches operate intermittently at light loads. This increases efficiency by minimizing switching losses. During the intervals when the switches are idle, the LTC3612 enters sleep state where many of the internal circuits are disabled to save power. During Burst Mode operation, the minimum peak inductor current is internally clamped and the voltage on the ITH pin is monitored by the burst comparator to determine when sleep mode is enabled and disabled. When the average inductor current is greater than the load current, the voltage on the ITH pin drops. As the ITH voltage falls below the internal clamp, the burst comparator trips and enables sleep mode. During sleep mode, the power MOSFETs are held off and the load current is solely supplied by the output capacitor. When the output voltage drops, the top power switch is turned back on and the internal circuits are re-enabled. This process repeats at a rate that is dependent on the load current.

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Burst Mode Operation—External Clamp

Connecting the MODE pin to a voltage in the range of 0.45V to 0.8V enables Burst Mode operation with external clamp. During this mode of operation the minimum voltage on the ITH pin is externally set by the voltage on the MODE pin. It is recommended to use Burst Mode operation with an internal clamp for temperatures above 85°C ambient.

Pulse-Skipping Mode Operation

Pulse-skipping mode is similar to Burst Mode operation, but the LTC3612 does not disable power to the internal circuitry during sleep mode. This improves output voltage ripple but uses more quiescent current, compromising light load efficiency.

Tying the MODE pin to SV_{IN} enables pulse-skipping mode. As the load current decreases, the peak inductor current will be determined by the voltage on the ITH pin until the ITH voltage drops below the voltage level corresponding to 0A. At this point, the peak inductor current is determined by the minimum on-time of the current comparator. If the load demand is less than the average of the minimum on-time inductor current, switching cycles will be skipped to keep the output voltage in regulation.

Forced Continuous Mode

In forced continuous mode the inductor current is constantly cycled which creates a minimum output voltage ripple at all output current levels.

Connecting the MODE pin to a voltage in the range of 1.1V to SV_{IN} • 0.58 will enable forced continuous mode operation.

At light loads, forced continuous mode operation is less efficient than Burst Mode or pulse-skipping operation, but may be desirable in some applications where it is necessary to keep switching harmonics out of the signal band.

Forced continuous mode must be used if the output is required to sink current.

Dropout Operation

As the input supply voltage approaches the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle, eventually reaching 100% duty cycle. The output voltage will then be determined by the input voltage minus the voltage drop across the internal P-channel MOSFET and the inductor.

Low Supply Operation

The LTC3612 is designed to operate down to an input supply voltage of 2.25V. An important consideration at low input supply voltages is that the $R_{DS(ON)}$ of the P-channel and N-channel power switches increases. The user should calculate the power dissipation when the LTC3612 is used at 100% duty cycle with low input voltages to ensure that thermal limits are not exceeded. See the Typical Performance Characteristics graphs.

Short-Circuit Protection

The peak inductor current at which the current comparator shuts off the top power switch is controlled by the voltage on the ITH pin.

If the output current increases, the error amplifier raises the ITH pin voltage until the average inductor current matches the new load current. In normal operation the LTC3612 clamps the maximum ITH pin voltage at approximately 1.05V which corresponds typically to 6A peak inductor current.

When the output is shorted to ground, the inductor current decays very slowly during a single switching cycle. The LTC3612 uses two techniques to prevent current runaway from occurring.

OPERATION

If the output voltage drops below 50% of its nominal value, the clamp voltage at ITH pin is lowered causing the maximum peak inductor current to decrease gradually with the output voltage. When the output voltage reaches 0V the clamp voltage at the ITH pin drops to 40% of the clamp voltage during normal operation. The short-circuit peak inductor current is determined by the minimum on-time of the LTC3612, the input voltage and the inductor value. This foldback behavior helps in limiting the peak inductor current when the output is shorted to ground. It is disabled during internal or external soft-start and tracking up/down operation (see the Applications Information section).

A secondary limit is also imposed on the valley inductor current. If the inductor current measured through the bottom MOSFET increases beyond 6A typical, the top power MOSFET will be held off and switching cycles will be skipped until the inductor current is reduced.

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The basic LTC3612 application circuit is shown in Figure 1.

Operating Frequency

Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values.

Operation at lower frequencies improves efficiency by reducing internal gate charge losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

The operating frequency of the LTC3612 is determined by an external resistor that is connected between the RT/SYNC pin and ground. The value of the resistor sets the ramp current that is used to charge and discharge an internal timing capacitor within the oscillator and can be calculated by using the following equation:

$$R_T = \frac{3.82 \bullet 10^{11} Hz}{f_{OSC}(Hz)} \Omega - 16k\Omega$$

Although frequencies as high as 4MHz are possible, the minimum on-time of the LTC3612 imposes a minimum limit on the operating duty cycle. The minimum on-time is typically 60ns; therefore, the minimum duty cycle is equal to 100 • 60ns • f_{OSC}(Hz)%.

Tying the RT/SYNC pin to SV_{IN} sets the default internal operating frequency to 2.25MHz ±20%.

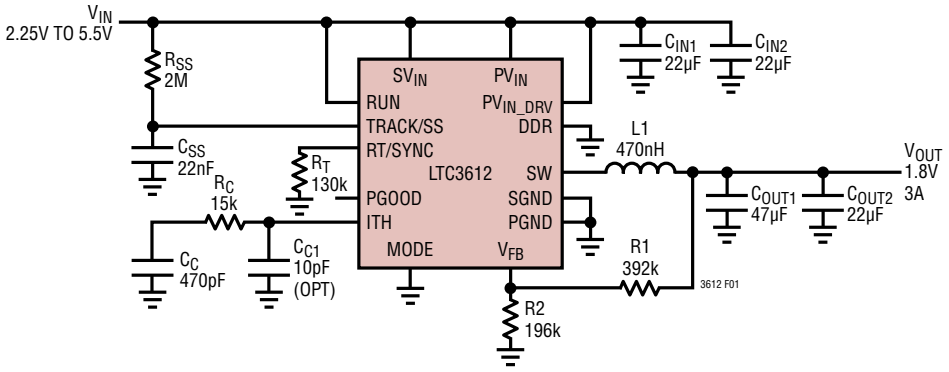

Figure 1. 1.8V, 3A Step-Down Regulator

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Frequency Synchronization

The LTC3612's internal oscillator can be synchronized to an external frequency by applying a square wave clock signal to the RT/SYNC pin. During synchronization, the top switch turn-on is locked to the falling edge of the external frequency source. The synchronization frequency range is 300kHz to 4MHz. During synchronization all operation modes can be selected.

It is recommended that the regulator is powered down (RUN pin to ground) before removing the clock signal on the RT/SYNC pin in order to reduce inductor current ripple.

AC coupling should be used if the external clock generator cannot provide a continuous clock signal throughout start-up, operation and shutdown of the LTC3612. The size of capacitor C_{SYNC} depends on parasitic capacitance on the RT/SYNC pin and is typically in the range of 10pF to 22pF

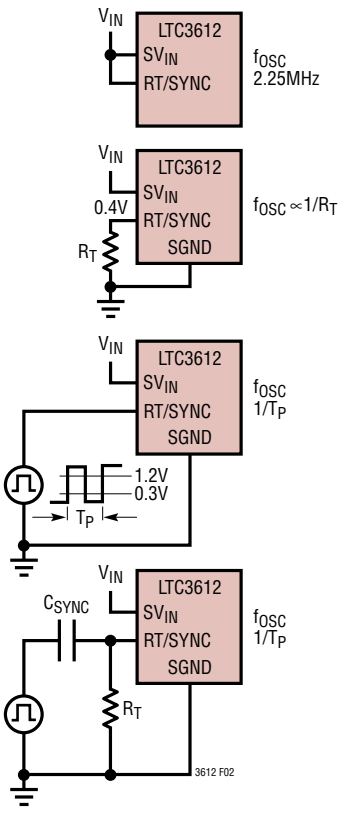

Figure 2. Setting the Switching Frequency

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance:

$$\Delta I_L = \left(\frac{V_{OUT}}{f_{SW} \bullet L}\right) \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Having a lower ripple current reduces the core losses in the inductor, the ESR losses in the output capacitors and the output voltage ripple. A reasonable starting point for selecting the ripple current is $\Delta I_L = 0.3 \bullet I_{OUT(MAX)}$. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L = \left(\frac{V_{OUT}}{f_{SW} \bullet \Delta I_{L(MAX)}}\right) \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The inductor value will also have an effect on Burst Mode operation. The transition to low current operation begins when the peak inductor current falls below a level set by the burst clamp. Lower inductor values result in higher ripple current which causes this to occur at lower load currents. This causes a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to increase.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for fixed inductor value, but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore, copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," meaning that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in

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inductor ripple current and consequently output voltage ripple. Do not allow a ferrite core to saturate and select external inductors respecting the temperature range of the application!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and do not radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. Table 1 shows some typical surface mount inductors that work well in LTC3612 applications.

Input Capacitor (C_{IN}) Selection

In continuous mode, the source current of the top P-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current must be used at V_{IN}.

The maximum RMS capacitor current is given by:

$$I_{RMS} = I_{OUT(MAX)} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \sqrt{\left(\frac{V_{IN}}{V_{OUT}} - 1\right)}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Generally select the capacitors respecting the temperature range of the application! Several capacitors may also be paralleled to meet size or height requirements in the design.

Output Capacitor (C_{OUT}) Selection

The selection of C_{OUT} is typically driven by the required ESR to minimize voltage ripple and load step transients (low ESR ceramic capacitors are discussed in the next section). Typically, once the ESR requirement is satisfied,

Table 1. Representative Surface Mount Inductors

INDUCTANCE (µH)	DCR (mΩ)	MAX CURRENT (A)	DIMENSIONS (mm)	HEIGHT (mm)
Vishay IHLP-2525AH-01 Series				
0.33	7	12	6.7 × 7	1.8
0.47	9	11	6.7 × 7	1.8
0.68	13	9	6.7 × 7	1.8
0.82	15	8	6.7 × 7	1.8
1.0	18	7	6.7 × 7	1.8
Vishay IHLP-1616BZ-01 Series				
0.22	8	24	4.3 × 4.7	2
0.47	18	11.5	4.3 × 4.7	2
1.00	37	8.5	4.3 × 4.7	2
Sumida CDMC6D28 Series				
0.3	3.2	15.4	6.7 × 7.25	3
0.47	4.2	13.6	6.7 × 7.25	3
0.68	5.4	11.3	6.7 × 7.25	3
1	8.8	8.8	6.7 × 7.25	3
NEC/Tokin MPLC0730L Series				
0.47	4.5	16.6	6.9 × 7.7	3.0
0.75	7.5	12.2	6.9 × 7.7	3.0
1.0	9.0	10.6	6.9 × 7.7	3.0
Cooper HCP0703 Series				
0.22	2.8	23	7 × 7.3	3.0
0.47	4.2	17	7 × 7.3	3.0
0.68	5.5	15	7 × 7.3	3.0
0.82	8.0	13	7 × 7.3	3.0
1.0	10.0	11	7 × 7.3	3.0
1.5	9.6	61	6.9 × 7.3	3.2
Würth Elektronik WE-HC744312 Series				
0.25	2.5	18	7 × 7.7	3.8
0.47	3.4	16	7 × 7.7	3.8
0.72	7.5	12	7 × 7.7	3.8
1.0	9.5	11	7 × 7.7	3.8
1.5	10.5	9	7 × 7.7	3.8
Coilcraft DO1813H Series				
0.33	4	10	8.9 × 6.1	5
0.56	10	7.7	8.9 × 6.1	5
Coilcraft v Series				
0.27	0.1	14	7.5 × 6.7	3
0.35	0.1	11	7.5 × 6.7	3
0.4	0.1	8	7.5 × 6.7	3

APPLICATIONS INFORMATION

the capacitance is adequate for filtering. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \le \Delta I_L \bullet \left(ESR + \frac{1}{8 \bullet f_{SW} \bullet C_{OUT}} \right)$$

where f_{OSC} = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

In surface mount applications, multiple capacitors may have to be paralleled to meet the capacitance, ESR or RMS current handling requirement of the application. Aluminum electrolytic, special polymer, ceramic and dry tantalum capacitors are all available in surface mount packages.

Tantalum capacitors have the highest capacitance density, but can have higher ESR and must be surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can often be used in extremely cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability.

Ceramic Input and Output Capacitors

Ceramic capacitors have the lowest ESR and can be cost effective, but also have the lowest capacitance density, high voltage and temperature coefficients, and exhibit audible piezoelectric effects. In addition, the high-Q of ceramic capacitors along with trace inductance can lead to significant ringing.

They are attractive for switching regulator use because of their very low ESR, but great care must be taken when using only ceramic input and output capacitors.

Ceramic capacitors are prone to temperature effects which require the designer to check loop stability over the operating temperature range. To minimize their large temperature and voltage coefficients, only X5R or X7R ceramic capacitors should be used.

When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the V_{IN} pin. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, the ringing at the input can be large enough to damage the part.

Since the ESR of a ceramic capacitor is so low, the input and output capacitor must instead fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation components and the output capacitor size. Typically, 3 to 4 cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. The output droop, V_{DROOP}, is usually about 2 to 4 times the linear drop of the first cycle; however, this behavior can vary depending on the compensation component values. Thus, a good place to start is with the output capacitor size of approximately:

$$C_{OUT} \approx \frac{3.5 \bullet \Delta I_{OUT}}{f_{SW} \bullet V_{DROOP}}$$

This is only an approximation; more capacitance may be needed depending on the duty cycle and load step requirements.

In most applications, the input capacitor is merely required to supply high frequency bypassing, since the impedance to the supply is very low.

Output Voltage Programming

The output voltage is set by an external resistive divider according to the following equation:

$$V_{OUT} = 0.6 \bullet \left(1 + \frac{R1}{R2} \right) V$$

The resistive divider allows pin V_{FB} to sense a fraction of the output voltage, as shown in Figure 1.

APPLICATIONS INFORMATION

Burst Clamp Programming

If the voltage on the MODE pin is less than 0.8V, Burst Mode operation is enabled.

If the voltage on the MODE pin is less than 0.3V, the internal default burst clamp level is selected. The minimum voltage on the ITH pin is typically 525mV (internal clamp).

If the voltage is between 0.45V and 0.8V, the voltage on the MODE pin (V_{BURST}) is equal to the minimum voltage on the ITH pin (external clamp) and determines the burst clamp level I_{BURST} (typically from 0A to 3.5A).

When the ITH voltage falls below the internal (or external) clamp voltage, the sleep state is enabled.

As the output load current drops, the peak inductor current decreases to keep the output voltage in regulation. When the output load current demands a peak inductor current that is less than I_{BURST}, the burst clamp will force the peak inductor current to remain equal to I_{BURST} regardless of further reductions in the load current.

Since the average inductor current is greater than the output load current, the voltage on the ITH pin will decrease. When the ITH voltage drops, sleep mode is enabled in which both power switches are shut off along with most of the circuitry to minimize power consumption. All circuitry is turned back on and the power switches resume operation when the output voltage drops out of regulation. The value for I_{BURST} is determined by the desired amount of output voltage ripple. As the value of I_{BURST} increases, the sleep period between pulses and the output voltage ripple increase. Note that for very high V_{BURST} voltage settings, the power good comparator may trip, since the output ripple may get bigger than the power good window.

Pulse-skipping mode, which is a compromise between low output voltage ripple and efficiency, can be implemented by connecting MODE to SV_{IN}. This sets I_{BURST} to 0A. In this condition, the peak inductor current is limited by the minimum on-time of the current comparator. The lowest output voltage ripple is achieved while still operating discontinuously. During very light output loads, pulse skipping allows only a few switching cycles to skip while maintaining the output voltage in regulation.

Internal and External Compensation

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD(ESR)}$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. The availability of the ITH pin allows the transient response to be optimized over a wide range of output capacitance.

The ITH external components (R_C and C_C) shown in Figure 1 provide adequate compensation as a starting point for most applications. The values can be modified slightly to optimize transient response once the final PCB layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system. The external capacitor, C_{C1}, (Figure 1) is not needed for loop stability, but it helps filter out any high frequency noise that may couple onto that node. The general purpose buck regulator application in the Typical Applications section uses a faster compensation to improve load step response.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. More output capacitance may be required depending on the duty cycle and load step requirements.

APPLICATIONS INFORMATION

AVP Mode

Fast load transient response, limited board space and low cost are typical requirements of microprocessor power supplies. A microprocessor has typical full load step with very fast slew rate. The voltage at the microprocessor must be held to about ±0.1V of nominal in spite of these load current steps. Since the control loop cannot respond this fast, the output capacitors must supply the load current until the control loop can respond.

Normally, several capacitors in parallel are required to meet microprocessor transient requirements. Capacitor ESR and ESL primarily determine the amount of droop or overshoot in the output voltage.

Consider the LTC3612 without AVP with a bank of tantalum output capacitors. If a load step with very fast slew rate occurs, the voltage excursion will be seen in both directions, for full load to minimum load transient and for the minimum load to full load transient.

If the ITH pin is tied to SV_{IN}, the active voltage positioning (AVP) mode and internal compensation are selected.

AVP mode intentionally compromises load regulation by reducing the gain of the feedback circuit, resulting in an output voltage that varies with load current. When the load current suddenly increases, the output voltage starts from a level slightly higher than nominal so the output voltage can droop more and stay within the specified voltage range. When the load current suddenly decreases the output voltage starts at a level lower than nominal so the output voltage can have more overshoot and stay within the specified voltage range (see Figures 3 and 4).

The benefit is a lower peak-to-peak output voltage deviation for a given load step without having to increase the output filter capacitance. Alternatively, the output voltage filter capacitance can be reduced while maintaining the same peak to peak transient response. Due to the reduced loop gain in AVP mode, no external compensation is required.

DDR Mode

The LTC3612 can both source and sink current if the MODE pin is configured to forced continuous mode.

Current sinking is typically limited to 1.5A, for 1MHz frequency and a 1µH inductor, but can be lower at higher frequencies and low output voltages. If higher ripple current can be tolerated, smaller inductor values can increase the sink current limit. See the Typical Performance Characteristics curves for more information.

In addition, tying the DDR pin to SV_{IN}, lower external reference voltage and tracking output voltage between channels are possible. See the Output Voltage Tracking and External Reference Input sections.

Soft-Start

The RUN pin provides a means to shut down the LTC3612. Tying the RUN pin to SGND places the LTC3612 in a low quiescent current shutdown state (I_Q < 1µA).

The LTC3612 is enabled by pulling the RUN pin high. However, the applied voltage must not exceed SV_{IN}. In some applications, the RUN signal is generated within another power domain and is driven high while the SV_{IN} and PV_{IN} is still 0V. In this case, it's required to limit the current into

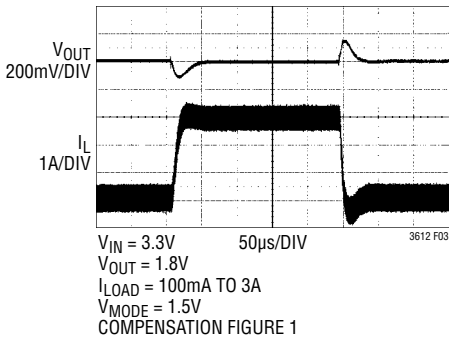


Figure 3. Load Step Transient Forced Continuous Mode (AVP Inactive)

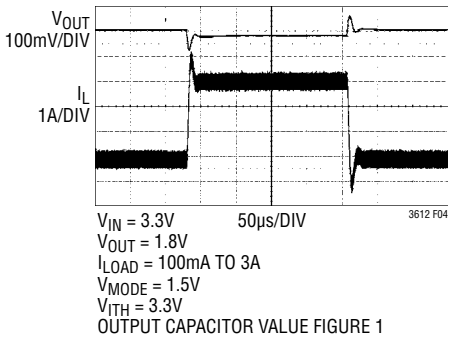


Figure 4. Load Step Transient Forced Continuous Mode with AVP Mode

APPLICATIONS INFORMATION

the RUN pin by either adding a 1MΩ resistor or a 100kΩ resistor, plus a Schottky diode, to SV_{IN}. After pulling the RUN pin high, the chip enters a soft start-up state. This type of soft start-up behavior is set by the TRACK/SS pin:

1. Tying TRACK/SS to SV_{IN} selects the internal soft-start circuit. This circuit ramps the output voltage to the final value within 1ms.
2. If a longer soft-start period is desired, it can be set externally with a resistor and capacitor on the TRACK/SS pin, as shown in Figure 1. The TRACK/SS pin reduces the value of the internal reference at V_{FB} until TRACK/SS is pulled above 0.6V. The external soft-start duration can be calculated by using the following formula:

$$t_{SS} = R_{SS} \bullet C_{SS} \bullet \ln\left(\frac{SV_{IN}}{SV_{IN} - 0.6V}\right)$$

3. The TRACK/SS pin can be used to track the output voltage of another supply.

Each time the RUN pin is tied high and the LTC3612 is turned on, the TRACK/SS pin is internally pulled down for ten microseconds in order to discharge the external capacitor. This discharging time is typically adequate for capacitors up to about 33nF. If a larger capacitor is required, connect the external soft-start resistor to the RUN pin.

Regardless of either internal or external soft-start state, the MODE pin is ignored and soft-start will always be in pulse-skipping mode. In addition, the PGOOD pin is kept low and foldback of the switching frequency is disabled.

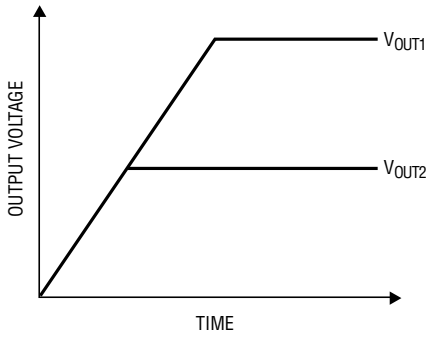
Output Voltage Tracking Input

If the DDR pin is not tied to SV_{IN}, once $V_{TRACK/SS}$ exceeds 0.6V, the run state is entered and the MODE selection, power good and current foldback circuits are enabled.

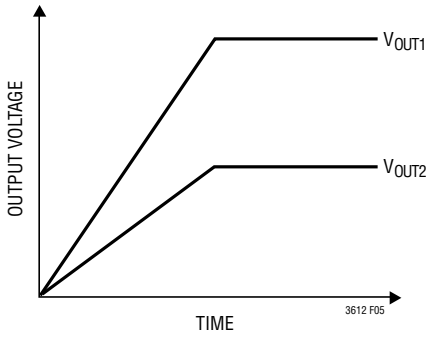
In the run state, the TRACK/SS pin can be used for tracking down/up the output voltage of another supply. If the $V_{TRACK/SS}$ drops below 0.6V, the LTC3612 enters the down tracking state and V_{OUT} is referenced to the TRACK/SS voltage. If the TRACK/SS pin drops below 0.2V, the switching frequency is reduced to ensure that the minimum duty cycle limit does not prevent the output from following the TRACK/SS pin. The run state will resume if $V_{TRACK/SS}$ again exceeds 0.6V and V_{OUT} is referenced to the internal precision reference (see Figure 7).

Through the TRACK/SS pin, the output voltage can be set up for either coincident or ratiometric tracking, as shown in Figure 5.

To implement the coincident tracking behavior in Figure 5a, connect an extra resistive divider to the output of the master channel and connect its midpoint to the TRACK/SS pin for the slave channel. The ratio of this divider should be selected to be the same as that of the slave channel's feedback divider (Figure 6a). In this tracking mode, the master channel's output must be set higher than slave channel's output. To implement the ratiometric tracking behavior in Figure 5b, different resistor divider values must be used as specified in Figure 6b.



(5a) Coincident Tracking



(5b) Ratiometric Tracking

Figure 5. Two Different Modes of Output Voltage Tracking

APPLICATIONS INFORMATION

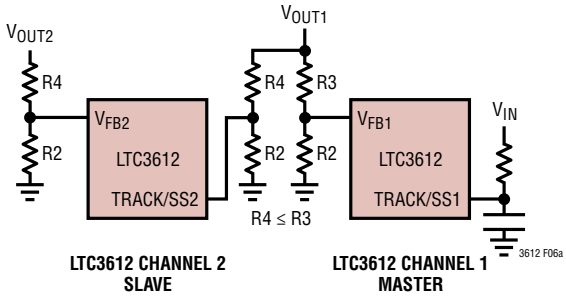


Figure 6a. Set-Up for Coincident Tracking

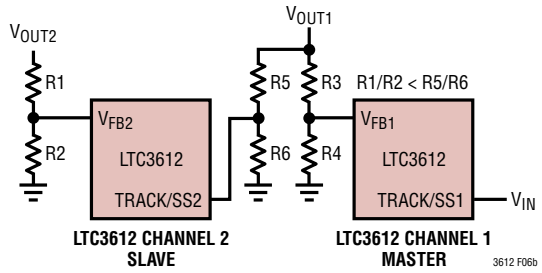


Figure 6b. Set-Up for Ratiometric Tracking

For coincident start-up, the voltage value at the TRACK/SS pin for the slave channel needs to reach the final reference value after the internal soft-start time (around 1ms). The master start-up time needs to be adjusted with an external capacitor and resistor to ensure this.

External Reference Input (DDR Mode)

If the DDR pin is tied to SV_{IN} (DDR mode), the run state is entered when $V_{TRACK/SS}$ exceeds 0.3V and tracking down behavior is possible if the $V_{TRACK/SS}$ voltage is below 0.6V.

This allows TRACK/SS to be used as an external reference between 0.3V and 0.6V if desired. During the run state in DDR mode, the power good window moves in relation to the actual TRACK/SS pin voltage if the voltage value is between 0.3V and 0.6V. Note: if TRACK/SS voltage is 0.6V, either the tracking circuit or the internal reference can be used.

During up/down tracking the output current foldback is disabled and the PGOOD pin is always pulled down (see Figure 8).

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: V_{IN} quiescent current and I^2R losses. The V_{IN} quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is usually of no consequence.

1. The V_{IN} quiescent current is due to two components: the DC bias current as given in the Electrical Characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is the current out of V_{IN} due to gate charge, and it is typically larger than the DC bias current. Both the DC bias and gate charge losses are proportional to V_{IN}; thus, their effects will be more pronounced at higher supply voltages.
2. I^2R losses are calculated from the resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode the average output current flowing through inductor L is “chopped” between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

APPLICATIONS INFORMATION

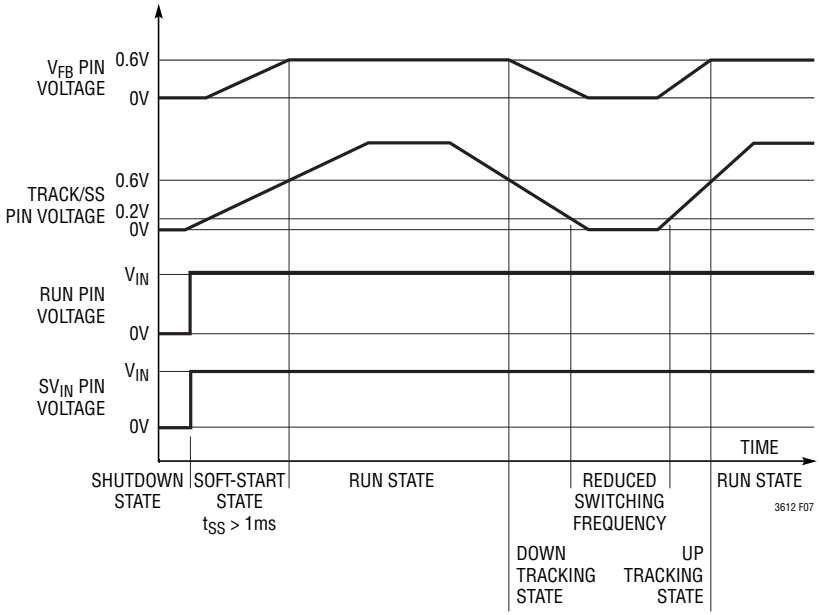


Figure 7. DDR Pin Not Tied to S_{VIN}

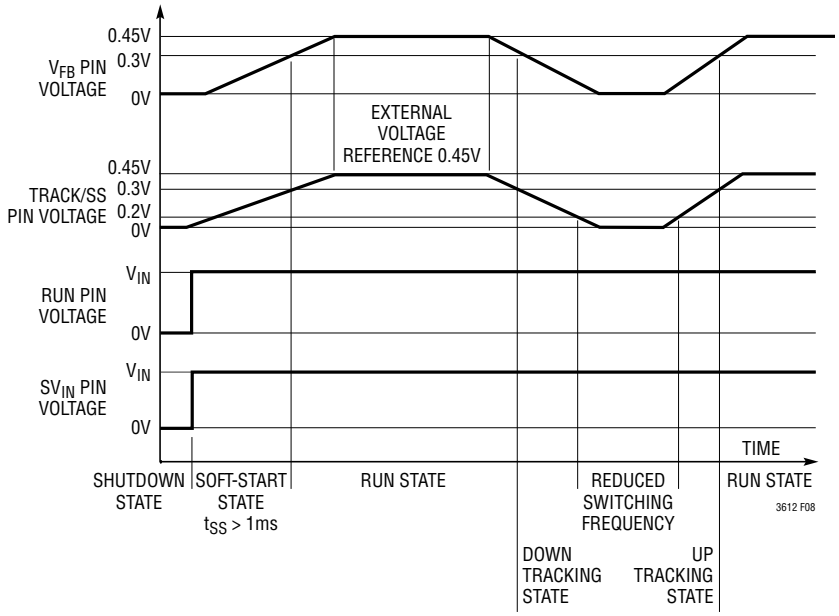


Figure 8. DDR Pin Tied to SV_{IN}. Example DDR Application

APPLICATIONS INFORMATION

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. To obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

Thermal Considerations

In most applications, the LTC3612 does not dissipate much heat due to its high efficiency.

However, in applications where the LTC3612 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 160°C, both power switches will be turned off and the SW node will become high impedance.

To prevent the LTC3612 from exceeding the maximum junction temperature, some thermal analysis is required. The temperature rise is given by:

$$T_{RISE} = (P_D)(\theta_{JA})$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature. The junction temperature, T_J, is given by:

$$T_J = T_A + T_{RISE}$$

where T_A is the ambient temperature.

As an example, consider the case when the LTC3612 is in dropout at an input voltage of 3.3V with a load current of 3A at an ambient temperature of 70°C. From the Typical Performance Characteristics graph of Switch Resistance, the $R_{DS(ON)}$ resistance of the P-channel switch is 0.075Ω. Therefore, power dissipated by the part is:

$$P_D = (I_{OUT})^2 \bullet R_{DS(ON)} = 675mW$$

For the QFN package, the θ_{JA} is 43°C/W.

Therefore, the junction temperature of the regulator operating at 70°C ambient temperature is approximately:

$$T_J = 0.675W \bullet 43°C/W + 70°C = 99°C$$

We can safely assume that the actual junction temperature will not exceed the absolute maximum junction temperature of 125°C.

Note that for very low input voltage, the junction temperature will be higher due to increased switch resistance, $R_{DS(ON)}$. It is not recommended to use full load current for high ambient temperature and low input voltage.

To maximize the thermal performance of the LTC3612 the Exposed Pad should be soldered to a ground plane. See the PCB Layout Board Checklist.

Design Example

As a design example, consider using the LTC3612 in an application with the following specifications:

V_{IN} = 2.25V to 5.5V, V_{OUT} = 1.8V, $I_{OUT(MAX)}$ = 3A, $I_{OUT(MIN)}$ = 100mA, f = 2.6MHz.

Efficiency is important at both high and low load current, so Burst Mode operation will be utilized.

First, calculate the timing resistor:

$$R_T = \frac{3.82 \bullet 10^{11} Hz}{2.6MHz}\Omega - 16k\Omega = 130k\Omega$$

Next, calculate the inductor value for about 30% ripple current at maximum V_{IN}:

$$L = \left(\frac{1.8V}{2.6MHz \bullet 1A}\right) \bullet \left(1 - \frac{1.8V}{5.5V}\right) = 0.466\mu H$$

Using a standard value of 0.47µH inductor results in a maximum ripple current of:

$$\Delta I_L = \left(\frac{1.8V}{2.6MHz \bullet 0.47\mu H}\right) \bullet \left(1 - \frac{1.8V}{5.5V}\right) = 0.99A$$

APPLICATIONS INFORMATION

C_{OUT} will be selected based on the ESR that is required to satisfy the output voltage ripple requirement and the bulk capacitance needed for loop stability. For this design, a 68µF (or 47µF plus 22µF) ceramic capacitor is used with a X5R or X7R dielectric.

C_{IN} should be sized for a maximum current rating of:

$$I_{RMS} = 3A \bullet \frac{1.8V}{3.6V} \bullet \sqrt{\left(\frac{3.6V}{1.8V} - 1\right)} = 1.5A_{RMS}$$

Decoupling the PV_{IN} with two 22µF capacitors, is adequate for most applications.

If we set R2 = 196k, the value of R1 can now be determined by solving the following equation.

$$R1 = 196k \bullet \left(\frac{1.8V}{0.6V} - 1\right)$$

A value of 392k will be selected for R1.

Finally, define the soft start-up time choosing the proper value for the capacitor and the resistor connected to TRACK/SS. If we set minimum t_{SS} = 5ms and a resistor of 2M, the following equation can be solved with the maximum SV_{IN} = 5.5V :

$$C_{SS} = \frac{5ms}{2M \bullet \ln\left(\frac{5.5V}{5.5V - 0.6V}\right)} = 21.6nF$$

The standard value of 22nF guarantees the minimum soft-start up time of 5ms.

Figure 1 shows the schematic for this design example.

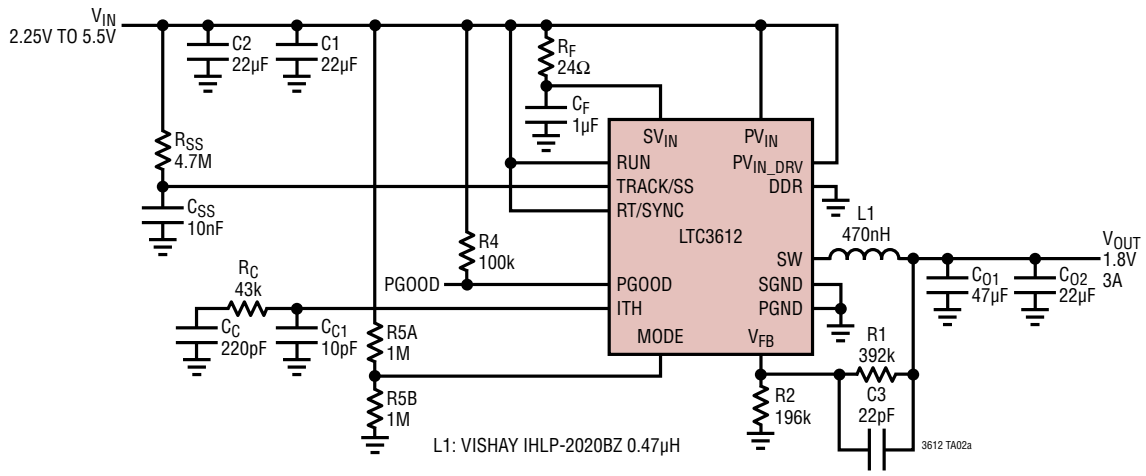
PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3612:

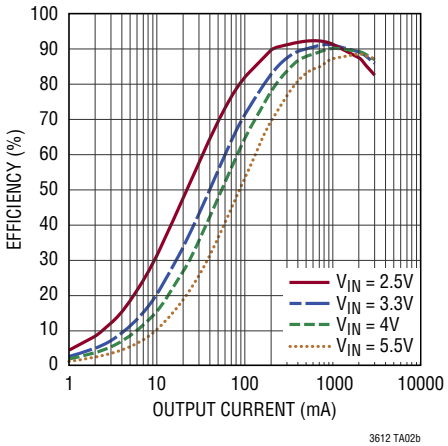
1. A ground plane is recommended. If a ground plane layer is not used, the signal and power grounds should be segregated with all small-signal components returning to the SGND pin at one point which is then connected to the PGND pin close to the LTC3612.
2. Connect the (+) terminal of the input capacitor(s), C_{IN}, as close as possible to the PV_{IN} pin, and the (–) terminal as close as possible to the exposed pad, PGND. This capacitor provides the AC current into the internal power MOSFETs.
3. Keep the switching node, SW, away from all sensitive small-signal nodes.
4. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. Connect the copper areas to PGND (exposed pad) for best performance.
5. Connect the V_{FB} pin directly to the feedback resistors. The resistor divider must be connected between V_{OUT} and SGND.

TYPICAL APPLICATIONS

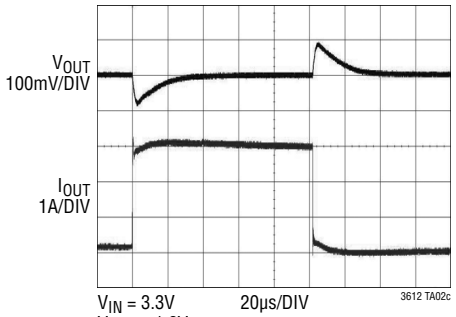
General Purpose Buck Regulator Using Ceramic Capacitors, 2.25MHz



Efficiency vs Output Current



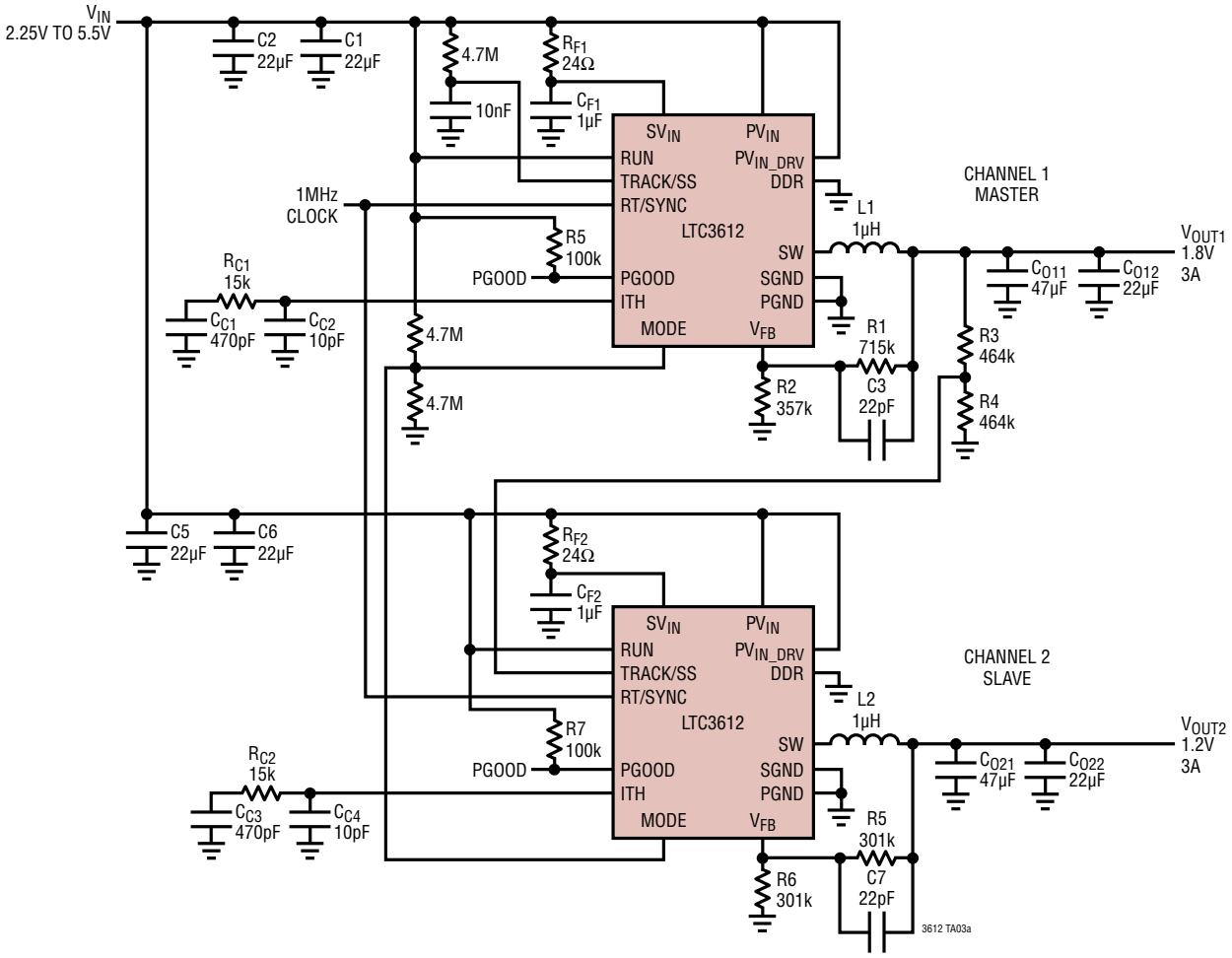
Load Step Response in Forced Continuous Mode



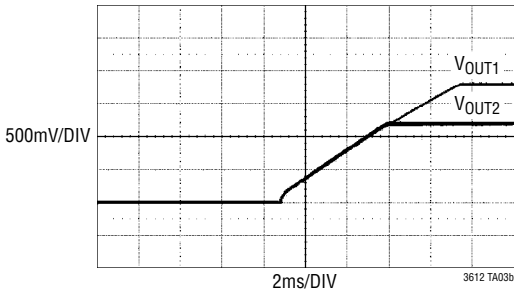
VIN = 3.3V 20µs/DIV
VOUT = 1.8V
IOUT = 100mA TO 3A
VMODE = 1.5V

TYPICAL APPLICATIONS

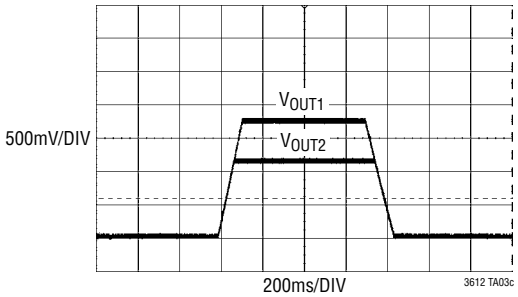
Master and Slave for Coincident Tracking Outputs Using a 1MHz External Clock



Coincident Start-Up

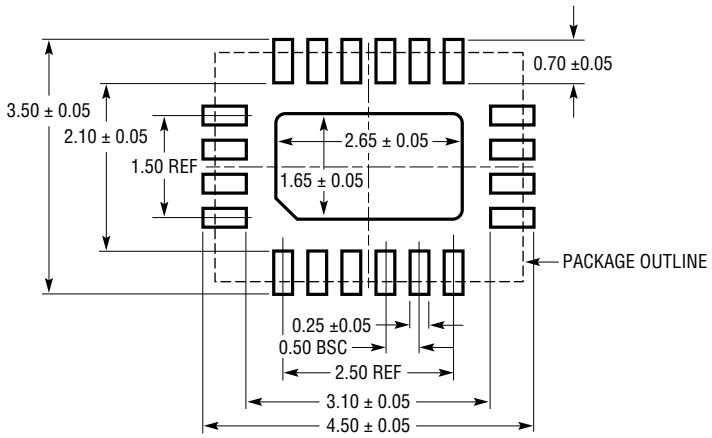


Coincident Tracking Up/Down

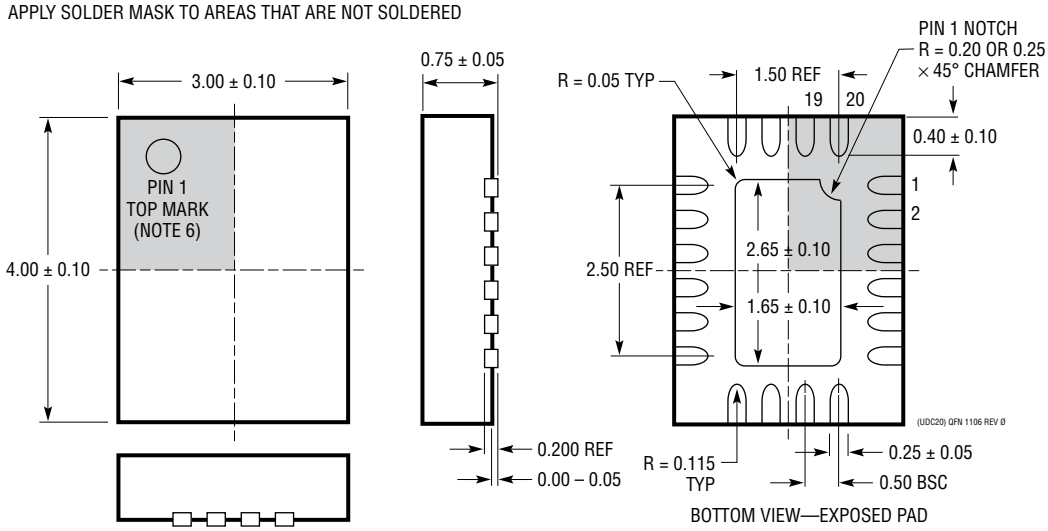


PACKAGE DESCRIPTION

UDC Package
20-Lead Plastic QFN (3mm × 4mm)
(Reference LTC DWG # 05-08-1742 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

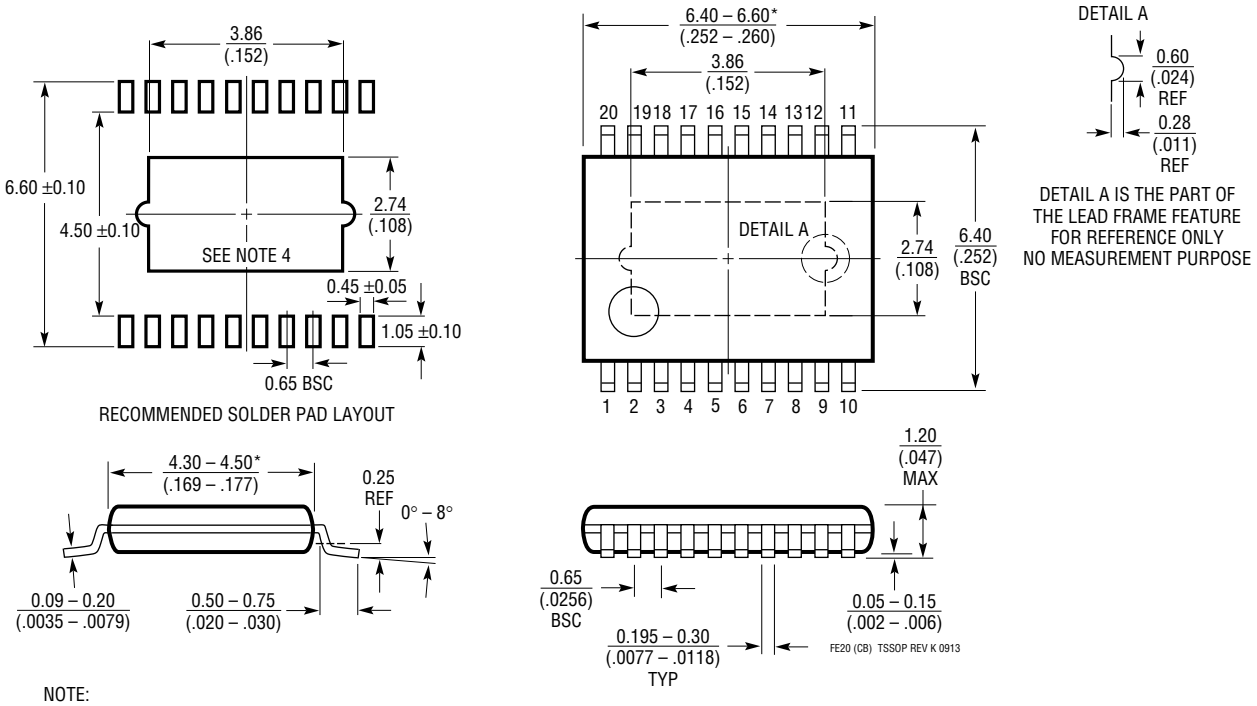


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev K)
Exposed Pad Variation CB



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY

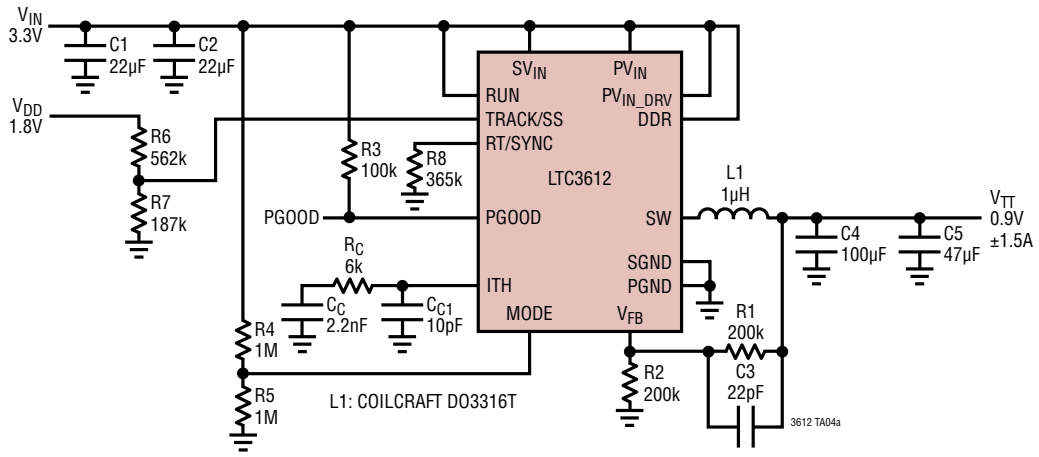
REV	DATE	DESCRIPTION	PAGE NUMBER
A	08/10	Updated Temperature Range in Order Information	2
		Edited Electrical Characteristics table and updated Note 2	3, 4
		Updated text in graphs G19, G31	7, 9
		Updated Pin 16/Pin 3 and Pin 21/Pin 21 text	10
		Updated Functional Block Diagram	11
		Updated Burst Mode Operation—External Clamp section	13
		Updated Internal and External Compensation section	18
		Updated Soft-Start section	19
		Updated Timing Resistor equation in Design Example section	23
		Updated TA02a and TA02c in Typical Applications	25
		Updated Related Parts	30
B	12/13	Add H and MP grades and applicable temperature range refs	throughout
		Revised Typical Performance Characteristics graphs	7-9
		Revised inductor and input capacitor sections	15-16
C	11/14	Changed Minimum Spec for Top Switch Current Limit (Duty Cycle = 100%)	3

LINEAR TECHNOLOGY

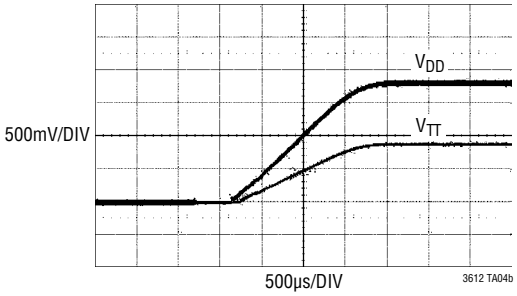
Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

DDR Termination with Ratiometric Tracking of V_{DD}, 1MHz



Ratiometric Start-Up



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3614	5.5V, 4A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter with Tracking and DDR	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} < 1µA, 3mm × 5mm QFN-24 Package
LTC3616	5.5V, 6A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter with Tracking and DDR	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} < 1µA, 3mm × 5mm QFN-24 Package
LTC3601	15V, 1.5A (I_{OUT}), Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4.5V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 300µA, I_{SD} < 1µA, MSOP-16E and 3mm × 3mm QFN-16 Packages
LTC3603	15V, 2.5A, Synchronous Step-Down DC/DC Converter	92% Efficiency, V_{IN}: 4.5V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} < 1µA, 4mm × 4mm QFN-16 Package
LTC3605	15V, 5A (I_{OUT}), Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 2mA, I_{SD} < 15µA, 4mm × 4mm QFN-24 Package
LTC3412A	5.5V, 3A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} < 1µA, TSSOP-16E and 4mm × 4mm QFN-16 Packages
LTC3413	5.5V, 3A (I_{OUT} Sink/Source), 2MHz, Monolithic Synchronous Regulator for DDR/QDR Memory Termination	90% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = V_{REF}/2, I_Q = 280µA, I_{SD} < 1µA, TSSOP-16E Package

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