Ordering number : ENA1443A

# LV5761V

**Bi-CMOS LSI**

# 1-channel Step-down Switching Regulator

ON Semiconductor®

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## Overview

The LV5761V is a 1-channel step-down switching regulator.

## Functions

- 1 channel step-down switching regulator controller.
- Frequency decrease function at pendent.
- Load-independent soft start circuit.
- ON/OFF function.
- Built-in pulse-by-pulse OCP circuit. It is detected by using ON resistance of an external MOS.
- Synchronous rectification.
- Current mode control.
- Synchronous drive by external signal.

## Specifications

### Absolute Maximum Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| supply voltage | $V_{IN}$ max | | 45 | V |
| Allowable Power dissipation | Pd max | Mounted on a specified board. * | 0.74 | W |
| Operating temperature | Topr | | -40 to +85 | °C |
| Storage temperature | Tstg | | -55 to +150 | °C |

* Specified board: 114.3mm × 76.1mm × 1.6mm, glass epoxy board

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

### Recommended Operating Range at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage range | $V_{IN}$ | | 8.5 to 42 | V |
| Error amplifier input voltage | | | 0 to 1.6 | V |

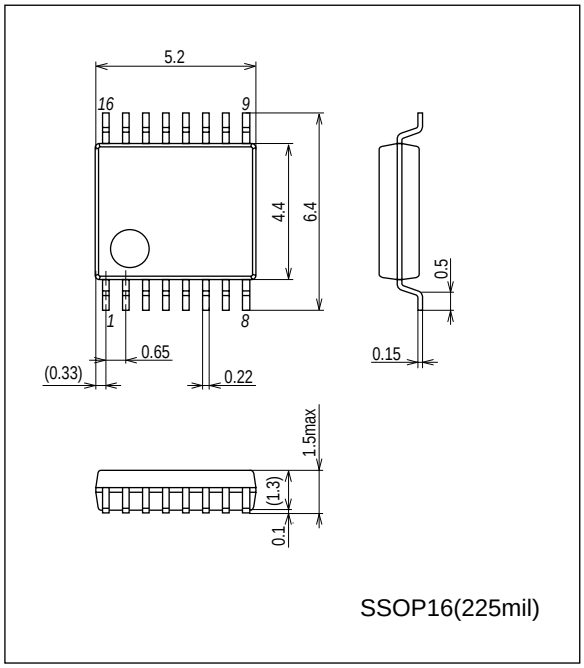
**Electrical Characteristics** at Ta = 25°C, $V_{IN}$ = 12V

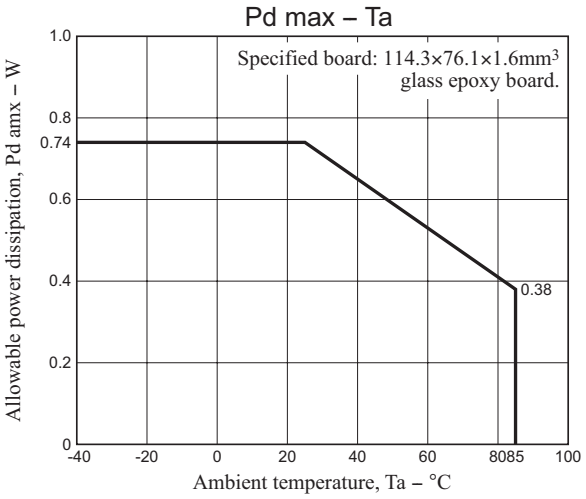
| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| **Reference voltage block** | | | | | | |
| Internal reference voltage | Vref | Including offset of E/A | 0.654 | 0.67 | 0.686 | V |
| 5V power supply | $V_{DD}$ | $I_{OUT}$ = 0 to 5mA | 4.7 | 5.2 | 5.7 | V |
| **Triangular waveform oscillator block** | | | | | | |
| Oscillation frequency | $F_{OSC}$ | RT = 220kΩ | 110 | 125 | 140 | kHz |
| Frequency variation | $F_{OSC\ DV}$ | $V_{IN}$ = 8 to 42V | | 1 | | % |
| Oscillation frequency fold back detection voltage | $V_{OSC\ FB}$ | FB voltage detection after SS ends | | 0.1 | | V |
| Oscillatory frequency after fold back | $F_{OSC\ FB}$ | | | $1/3F_{OSC}$ | | kHz |
| **ON/OFF circuit block** | | | | | | |
| IC start-up voltage | $V_{EN}$ on | | 2.5 | 3.0 | 3.5 | V |
| IC off voltage | $V_{EN}$ off | | 1.0 | 1.2 | 1.4 | V |
| **Soft start circuit block** | | | | | | |
| Soft start source current | $I_{SS}$ SC | EN > 3.5V | 4 | 5 | 6 | µA |
| Soft start sink current | $I_{SS}$ SK | EN < 1V, $V_{DD}$ = 5V | | 2 | | mA |
| **UVLO circuit block** | | | | | | |
| UVLO lock release voltage | $V_{UVLO}$ | | 7.5 | 8.0 | 8.5 | V |
| UVLO hysteresis | $V_{UVLO\ H}$ | | | 0.7 | | V |
| **OCP circuit block** | | | | | | |
| OCP charge current | $I_{OCP}$ | | | 5 | | µA |
| **Error amplifier** | | | | | | |
| Input bias current | $I_{EA\ IN}$ | | | | 100 | nA |
| Error amplifier transconductance | $G_{EA}$ | | 1000 | 1400 | 1800 | µA/V |
| Sink output current | $I_{EA\ OSK}$ | FB = 1.0V | | -100 | | µA |
| Source output current | $I_{EA\ OSC}$ | FB = 0V | | 100 | | µA |
| Current detection amplifier gain | GISNS | | | 1.5 | | |
| **over current limiter circuit block** | | | | | | |
| Reference current 1 | $I_{LIM}1$ | MODE = L (GND) | -10% | 18.5 | +10% | µA |
| Reference current 2 | $I_{LIM}2$ | MODE = H ($V_{IN}$) | -10% | 37.0 | +10% | µA |
| Over current detection comparator offset voltage | $V_{LIM\ OFS}$ | | -5 | | +5 | mA |
| Over current detection comparator common mode input range | | | $V_{IN}$-0.45 | | $V_{IN}$ | V |
| **PWM comparator** | | | | | | |
| Input threshold voltage (fosc = 125kHz) | Vt max | Duty cycle = DMAX | 0.9 | 1.0 | 1.1 | V |
| | Vt0 | Duty cycle = 0% | 0.4 | 0.5 | 0.6 | V |
| Maximum ON duty | DMAX | | 80 | 85 | 90 | % |
| **Output block** | | | | | | |
| Output stage ON resistance (the upper side) | $R_{ONH}$ | | | 5 | | Ω |
| Output stage ON resistance (the under side) | $R_{ONL}$ | | | 5 | | Ω |
| Output stage ON current (the upper side) | $I_{ONH}$ | | 240 | | | mA |
| Output stage ON current (the under side) | $I_{ONL}$ | | 240 | | | mA |
| **The whole device** | | | | | | |
| Standby current | $I_{CCS}$ | EN < 1V | | | 10 | µA |
| Mean consumption current | $I_{CCA}$ | EN > 3V | | 3 | | mA |

## Package Dimensions

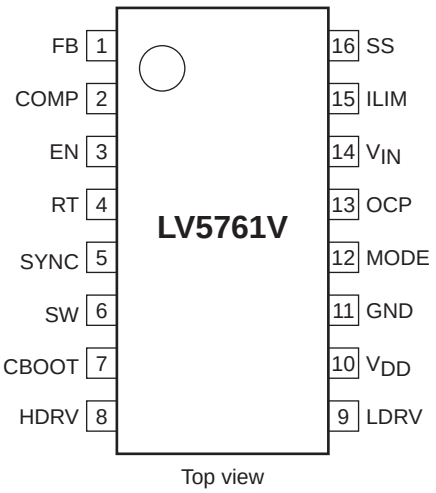
unit : mm (typ)

3178B

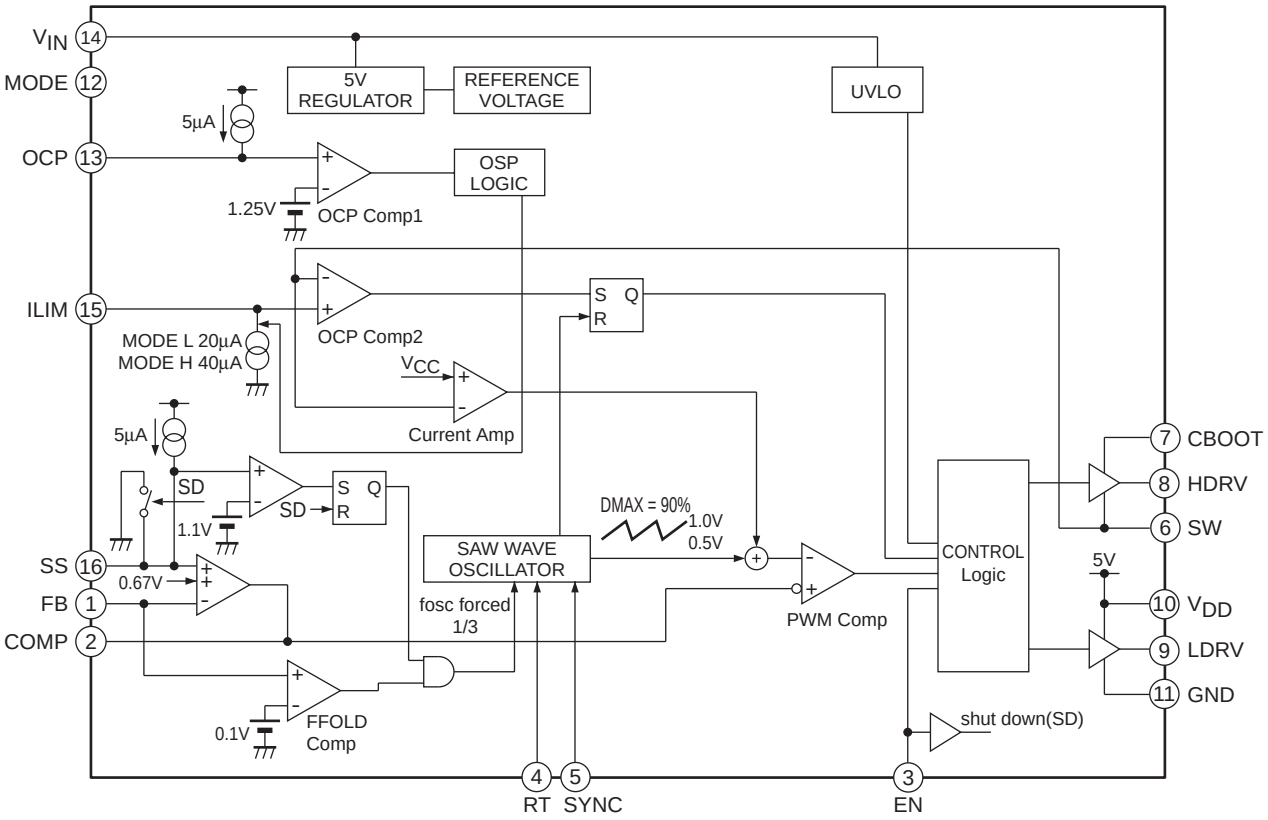



## Pin Assignment



## Block Diagram



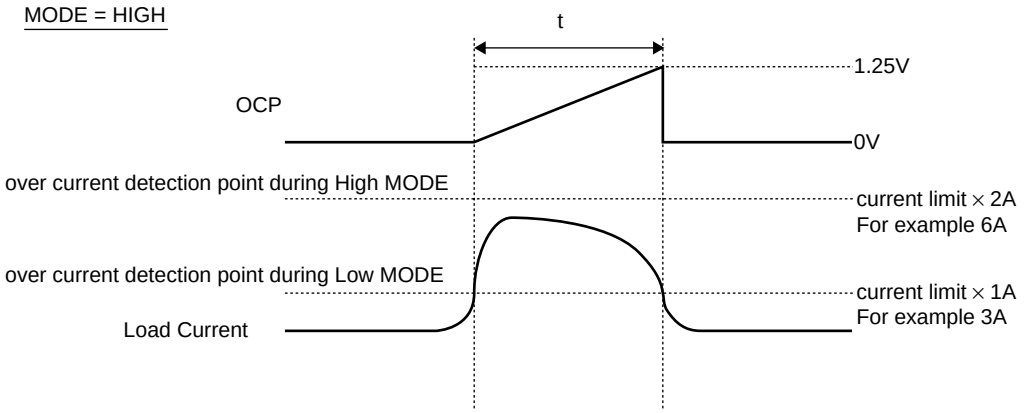

## Pin Function

| Pin No. | Pin name | Description |
|---|---|---|
| 14 | $V_{IN}$ | Power supply pin. This pin is monitored by UVLO function. When the voltage of this pin becomes 8V or more by UVLO function, The IC starts and the soft start function operates. |
| 11 | GND | Ground pin. Each reference voltage is based on the voltage of the ground pin. |
| 10 | $V_{DD}$ | Power supply pin for an external the lower MOS-FET gate drive. |
| 7 | CBOOT | Bootstrap capacity connection pin. This pin becomes a GATE drive power supply of an external NchMOSFET. Connect a bypath capacitor between CBOOT and SW. |
| 6 | SW | Pin to connect with switching node. The source of NchMOSFET connects to this pin. |
| 5 | SYNC | External synchronous signal input pin. |
| 9 | LDRV | An external the lower MOSFET gate drive pin. |
| 8 | HDRV | An external the upper MOSFET gate drive pin. |
| 1 | FB | Error amplifier reverse input pin. By operating the converter, the voltage of this pin becomes 0.67V. The voltage in which the output voltage is divided by an external resistance is applied to this pin. Moreover, when this pin voltage becomes 0.1V or less after a soft start ends, the oscillatory frequency becomes 1/3. |
| 2 | COMP | Error amplifier output pin. Connect a phase compensation circuit between this pin and GND. |
| 16 | SS | Pin to connect a capacitor for soft start. A capacitor for soft start is charged by using the voltage of about 5μA. This pin ends the soft start period by using the voltage of about 1.1V and the frequency fold back function becomes active. |
| 15 | ILIM | Reference current pin for current detection. The sink current of about 20μA flows to this pin when Low level (GND) is set to the MODE pin. Also, the sink current of about 40μA flows to this pin when High level ($V_{IN}$) is set to the MODE pin. When a resistance is connected between this pin and $V_{IN}$ outside and the voltage applied to the SW pin is lower than the voltage of the terminal side of the resistance, the upper NchMOSFET is off by operating the current limiter comparator. This operation is reset with respect to each PWM pulse. |
| 3 | EN | ON/OFF pin. |
| 13 | OCP | Pin to set the time of the timer (during double the over current detection point) Connect a capacitor between this pin and GND. OCP charge current : 5μA |
| 4 | RT | Pin to set the oscillation frequency. Connect a resistance between this pin and GND. |
| 12 | MODE | Pin to switch the over current detection point. Set by the low level (GND) of the ILIM pin. Set by the high level ($V_{IN}$) of the OCP pin. When this MODE pin is set to the high level and the point of the over current detection is set by using the ILIM pin is exceeded, the value becomes double the original value. Also, when the MODE pin is set to the low level, the point of the over current detection remains an original value. |

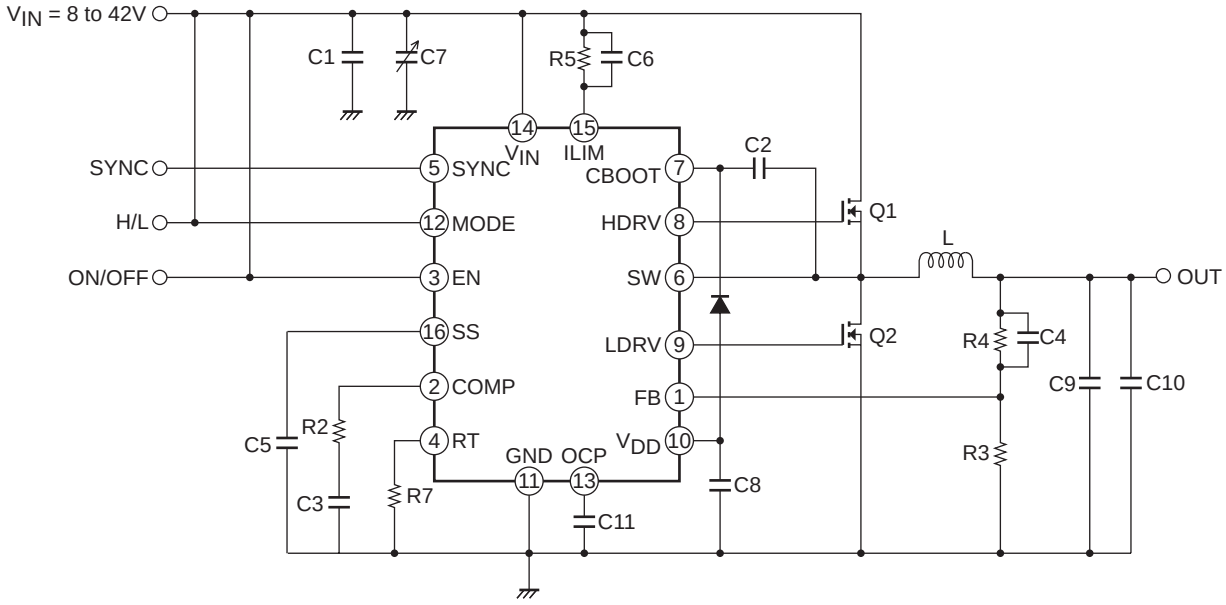
### Timing Chart

When the MODE pin is set to the high level and the point of the over current detection is set by using the ILIM pin is exceeded, the value becomes double the original value.
Also, when the MODE pin is set to the low level, the point of over current detection remains an original value.

Timing chart of the over current detection point switching is as below.




## Sample Application Circuit



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