THE DATASHEET OF

M45PE20-VMN6TP

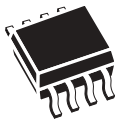
www.win-source.net 0086-755-83957316

M45PE20

2-Mbit, page-erasable serial flash memory with byte alterability and a 75 MHz SPI bus interface

Features

- SPI bus compatible serial interface
- 75 MHz clock rate (maximum)
- 2.7 V to 3.6 V single supply voltage
- 2-Mbit, page-erasable flash memory
- Page size: 256 bytes
  - Page write in 11 ms (typical)
  - Page program in 0.8 ms (typical)
  - Page erase in 10 ms (typical)
- Sector erase (512 Kbits)
- Hardware write protection of the bottom sector (64 Kbytes)
- Electronic signature
  - JEDEC standard two-byte signature (4012h)
  - Unique ID code (UID) with 16 bytes read-only, available upon customer request only in the T9HX process
- Deep power-down mode 1 µA (typical)
- More than 100 000 write cycles
- More than 20 years data retention
- Packages
  - ECOPACK® (RoHS compliant)



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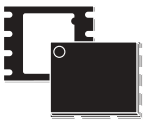

VFQFPN8 (MP)
(MLP8)

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1 Description

The M45PE20 is a 2-Mbit (256 Kbits ×8) serial paged flash memory accessed by a high speed SPI-compatible bus.

The memory can be written or programmed 1 to 256 bytes at a time, using the page write or page program instruction. The page write instruction consists of an integrated page erase cycle followed by a page program cycle.

The memory is organized as 4 sectors, each containing 256 pages. Each page is 256 bytes wide. Thus, the whole memory can be viewed as consisting of 1024 pages, or 262,144 bytes.

The memory can be erased a page at a time, using the page erase instruction, or a sector at a time, using the sector erase instruction.

Important note

This datasheet details the functionality of the M45PE20 devices, based on the previous T7X process or based on the current T9HX process (available since August 2007). Delivery of parts operating with a maximum clock rate of 75 MHz starts from week 8 of 2008.

Figure 1. Logic diagram

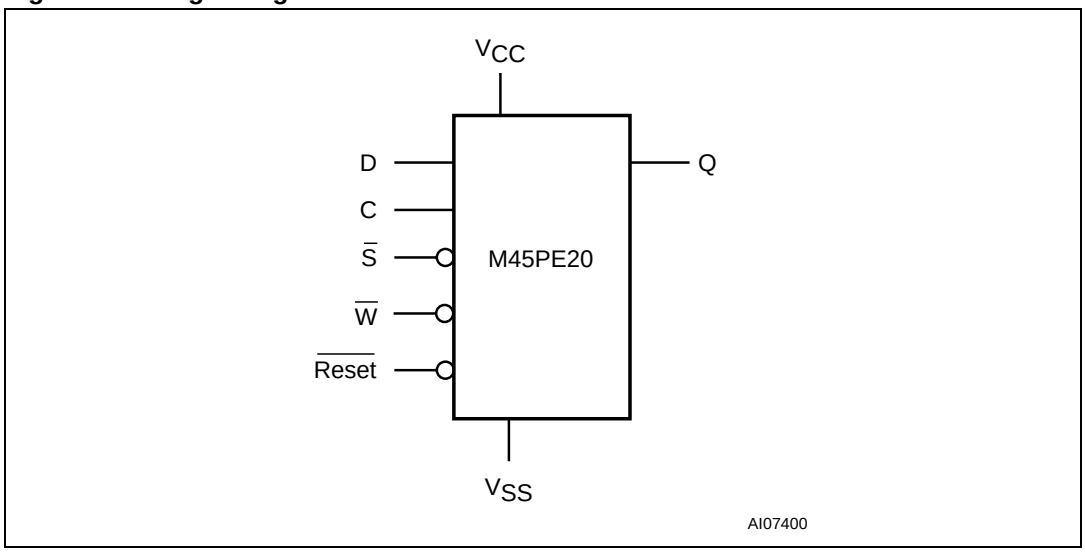
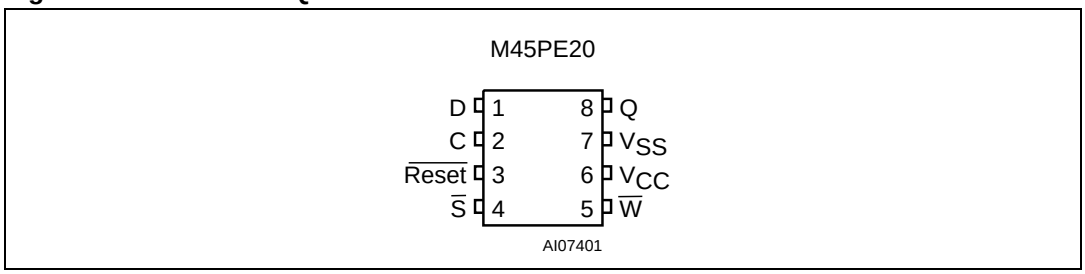


Figure 2. SO and VFQFPN connections



1. There is an exposed central pad on the underside of the VFQFPN package. This is pulled, internally, to V_{SS}, and must not be allowed to be connected to any other voltage or signal line on the PCB.
2. See *Package mechanical* section for package dimensions, and how to identify pin-1.

Table 1. Signal names

Signal name	Function	Direction
C	Serial Clock	Input
D	Serial data input	Input
Q	Serial data output	Output
$\overline{S}$	Chip Select	Input
$\overline{W}$	Write Protect	Input
$\overline{Reset}$	Reset	Input
V_{CC}	Supply voltage	
V_{SS}	Ground	

2 Signal descriptions

2.1 Serial data output (Q)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

2.2 Serial data input (D)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of Serial Clock (C).

2.3 Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at serial data input (D) are latched on the rising edge of Serial Clock (C). Data on serial data output (Q) changes after the falling edge of Serial Clock (C).

2.4 Chip Select ($\overline{S}$)

When this input signal is High, the device is deselected and serial data output (Q) is at high impedance. Unless an internal read, program, erase or write cycle is in progress, the device will be in the standby power mode (this is not the deep power-down mode). Driving Chip Select ($\overline{S}$) Low selects the device, placing it in the active power mode.

After power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

2.5 Reset ($\overline{Reset}$)

The Reset ($\overline{Reset}$) input provides a hardware reset for the memory. In this mode, the outputs are high impedance.

When Reset ($\overline{Reset}$) is driven High, the memory is in the normal operating mode. When Reset ($\overline{Reset}$) is driven Low, the memory will enter the reset mode, provided that no internal operation is currently in progress. Driving Reset ($\overline{Reset}$) Low while an internal operation is in progress has no effect on that internal operation (a write cycle, program cycle, or erase cycle).

2.6 Write Protect ($\overline{W}$)

This input signal puts the device in the hardware protected mode, when Write Protect ($\overline{W}$) is connected to V_{SS}, causing the first 256 pages of memory to become read-only by protecting them from write, program and erase operations. When Write Protect ($\overline{W}$) is connected to V_{CC}, the first 256 pages of memory behave like the other pages of memory.

2.7 V_{CC} supply voltage

V_{CC} is the supply voltage.

2.8 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

3 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

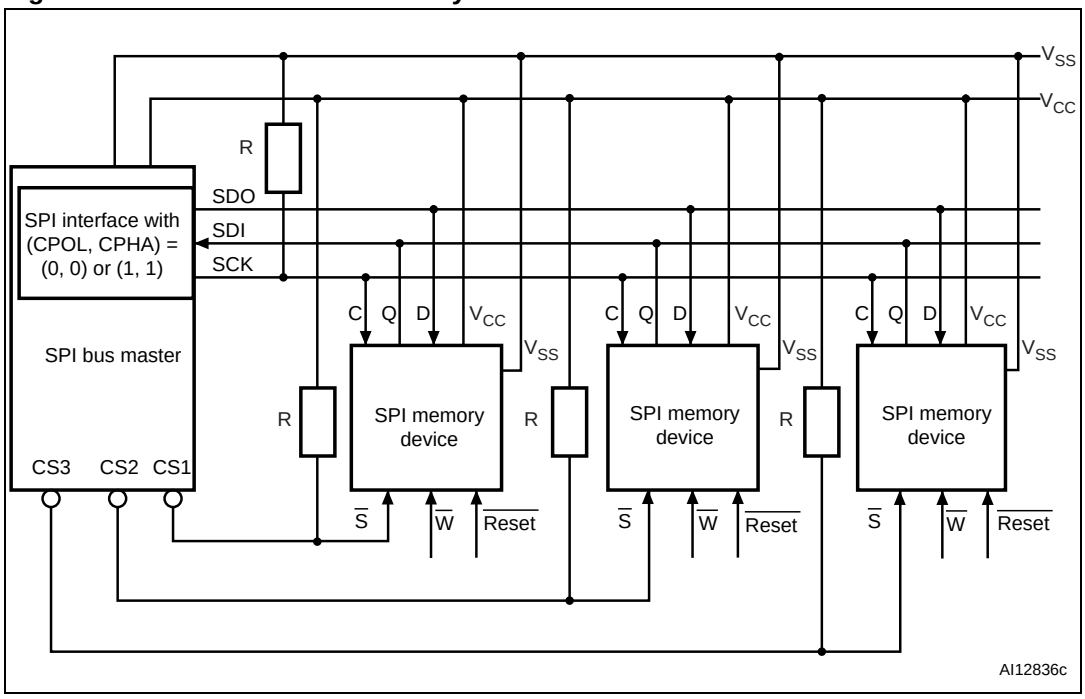
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in *Figure 4*, is the clock polarity when the bus master is in standby mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 3. Bus master and memory devices on the SPI bus

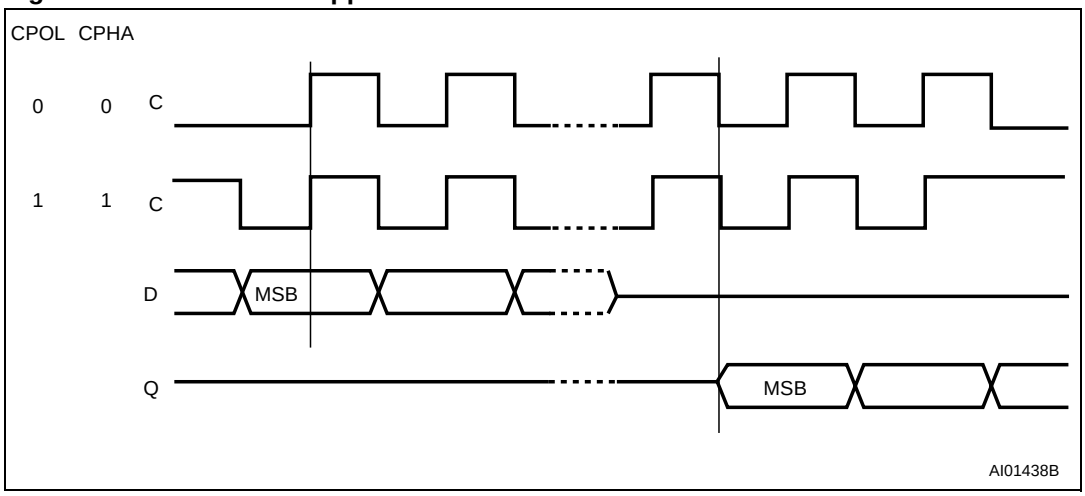


1. The Write Protect ($\overline{W}$) signal should be driven, High or Low as appropriate.

Figure 3 shows an example of three devices connected to an MCU, on an SPI bus. Only one device is selected at a time, so only one device drives the serial data output (Q) line at a time, the other devices are high impedance. Resistors R (represented in *Figure 3*) ensure that the M45PE20 is not selected if the bus master leaves the $\overline{S}$ line in the high impedance state. As the bus master may enter a state where all inputs/outputs are in high impedance at the same time (for example, when the bus master is reset), the clock line (C) must be connected to an external pull-down resistor so that, when all inputs/outputs become high impedance, the $\overline{S}$ line is pulled High while the C line is pulled Low (thus ensuring that $\overline{S}$ and C do not become High at the same time, and so, that the t_{SHCH} requirement is met). The typical value of R is 100 kΩ, assuming that the time constant $R*C_p$ (C_p = parasitic capacitance of the bus line) is shorter than the time during which the bus master leaves the SPI bus in high impedance.

Example: C_p = 50 pF, that is R*C_p = 5 µs <=> the application must ensure that the bus master never leaves the SPI bus in the high impedance state for a time period shorter than 5 µs.

Figure 4. SPI modes supported



4 Operating features

4.1 Sharing the overhead of modifying data

To write or program one (or more) data bytes, two instructions are required: write enable (WREN), which is one byte, and a page write (PW) or page program (PP) sequence, which consists of four bytes plus data. This is followed by the internal cycle (of duration t_{PW} or t_{PP}).

To share this overhead, the page write (PW) or page program (PP) instruction allows up to 256 bytes to be programmed (changing bits from ‘1’ to ‘0’) or written (changing bits to ‘0’ or ‘1’) at a time, provided that they lie in consecutive addresses on the same page of memory.

4.2 An easy way to modify data

The page write (PW) instruction provides a convenient way of modifying data (up to 256 contiguous bytes at a time), and simply requires the start address, and the new data in the instruction sequence.

The page write (PW) instruction is entered by driving Chip Select ($\overline{S}$) Low, and then transmitting the instruction byte, three address bytes (A23-A0) and at least one data byte, and then driving Chip Select ($\overline{S}$) High. While Chip Select ($\overline{S}$) is being held Low, the data bytes are written to the data buffer, starting at the address given in the third address byte (A7-A0). When Chip Select ($\overline{S}$) is driven High, the write cycle starts. The remaining, unchanged, bytes of the data buffer are automatically loaded with the values of the corresponding bytes of the addressed memory page. The addressed memory page then automatically put into an erase cycle. Finally, the addressed memory page is programmed with the contents of the data buffer.

All of this buffer management is handled internally, and is transparent to the user. The user is given the facility of being able to alter the contents of the memory on a byte-by-byte basis.

For optimized timings, it is recommended to use the page write (PW) instruction to write all consecutive targeted bytes in a single sequence versus using several page write (PW) sequences with each containing only a few bytes (see *Section 6.7: Page write (PW)*, *Table 14: AC characteristics (50 MHz operation)*, and *Table 15: AC characteristics (75 MHz operation, T9HX (0.11 µm) process)*).

4.3 A fast way to modify data

The page program (PP) instruction provides a fast way of modifying data (up to 256 contiguous bytes at a time), provided that it only involves resetting bits to 0 that had previously been set to '1'.

This might be:

- when the designer is programming the device for the first time
- when the designer knows that the page has already been erased by an earlier page erase (PE) or sector erase (SE) instruction. This is useful, for example, when storing a fast stream of data, having first performed the erase cycle when time was available
- when the designer knows that the only changes involve resetting bits to '0' that are still set to '1'. When this method is possible, it has the additional advantage of minimizing the number of unnecessary erase operations, and the extra stress incurred by each page.

For optimized timings, it is recommended to use the page program (PP) instruction to program all consecutive targeted bytes in a single sequence versus using several page program (PP) sequences with each containing only a few bytes (see *Section 6.8: Page program (PP)*, *Table 14: AC characteristics (50 MHz operation)*, and *Table 15: AC characteristics (75 MHz operation, T9HX (0.11 µm) process)*).

4.4 Polling during a write, program or erase cycle

A further improvement in the write, program or erase time can be achieved by not waiting for the worst case delay (t_{PW}, t_{PP}, t_{PE}, or t_{SE}). The write in progress (WIP) bit is provided in the status register so that the application program can monitor its value, polling it to establish when the previous cycle is complete.

4.5 Reset

An internal power on reset circuit helps protect against inadvertent data writes. Addition protection is provided by driving Reset ($\overline{\text{Reset}}$) Low during the power-on process, and only driving it High when V_{CC} has reached the correct voltage level, V_{CC}(min).

4.6 Active power, standby power and deep power-down modes

When Chip Select ($\overline{S}$) is Low, the device is selected, and in the active power mode.

When Chip Select ($\overline{S}$) is High, the device is deselected, but could remain in the active power mode until all internal cycles have completed (program, erase, write). The device then goes in to the standby power mode. The device consumption drops to I_{CC1}.

The deep power-down mode is entered when the specific instruction (the deep power-down (DP) instruction) is executed. The device consumption drops further to I_{CC2}. The device remains in this mode until another specific instruction (the release from deep power-down and read electronic signature (RES) instruction) is executed.

All other instructions are ignored while the device is in the deep power-down mode. This can be used as an extra software protection mechanism, when the device is not in active use, to protect the device from inadvertent write, program or erase instructions.

4.7 Status register

The status register contains two status bits that can be read by the read status register (RDSR) instruction. See *Section 6.4: Read status register (RDSR)* for a detailed description of the status register bits.

4.8 Protection modes

The environments where non-volatile memory devices are used can be very noisy. No SPI device can operate correctly in the presence of excessive noise. To help combat this, the M45PE20 features the following data protection mechanisms:

- Power on reset and an internal timer (t_{PUW}) can provide protection against inadvertent changes while the power supply is outside the operating specification
- Program, erase and write instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events:
  - Power-up
  - Reset ($\overline{\text{Reset}}$) driven Low
  - Write disable (WRDI) instruction completion
  - Page write (PW) instruction completion
  - Page program (PP) instruction completion
  - Page erase (PE) instruction completion
  - Sector erase (SE) instruction completion
- The hardware protected mode is entered when Write Protect ($\overline{W}$) is driven Low, causing the first 256 pages of memory to become read-only. When Write Protect ($\overline{W}$) is driven High, the first 256 pages of memory behave like the other pages of memory
- The Reset ($\overline{\text{Reset}}$) signal can be driven Low to protect the contents of the memory during any critical time, not just during power-up and power-down
- In addition to the low power consumption feature, the deep power-down mode offers extra software protection from inadvertent write, program and erase instructions while the device is not in active use.

5 Memory organization

The memory is organized as:

- 1024 pages (256 bytes each).
- 262,144 bytes (8 bits each)
- 4 sectors (512 Kbits, 65536 bytes each)

Each page can be individually:

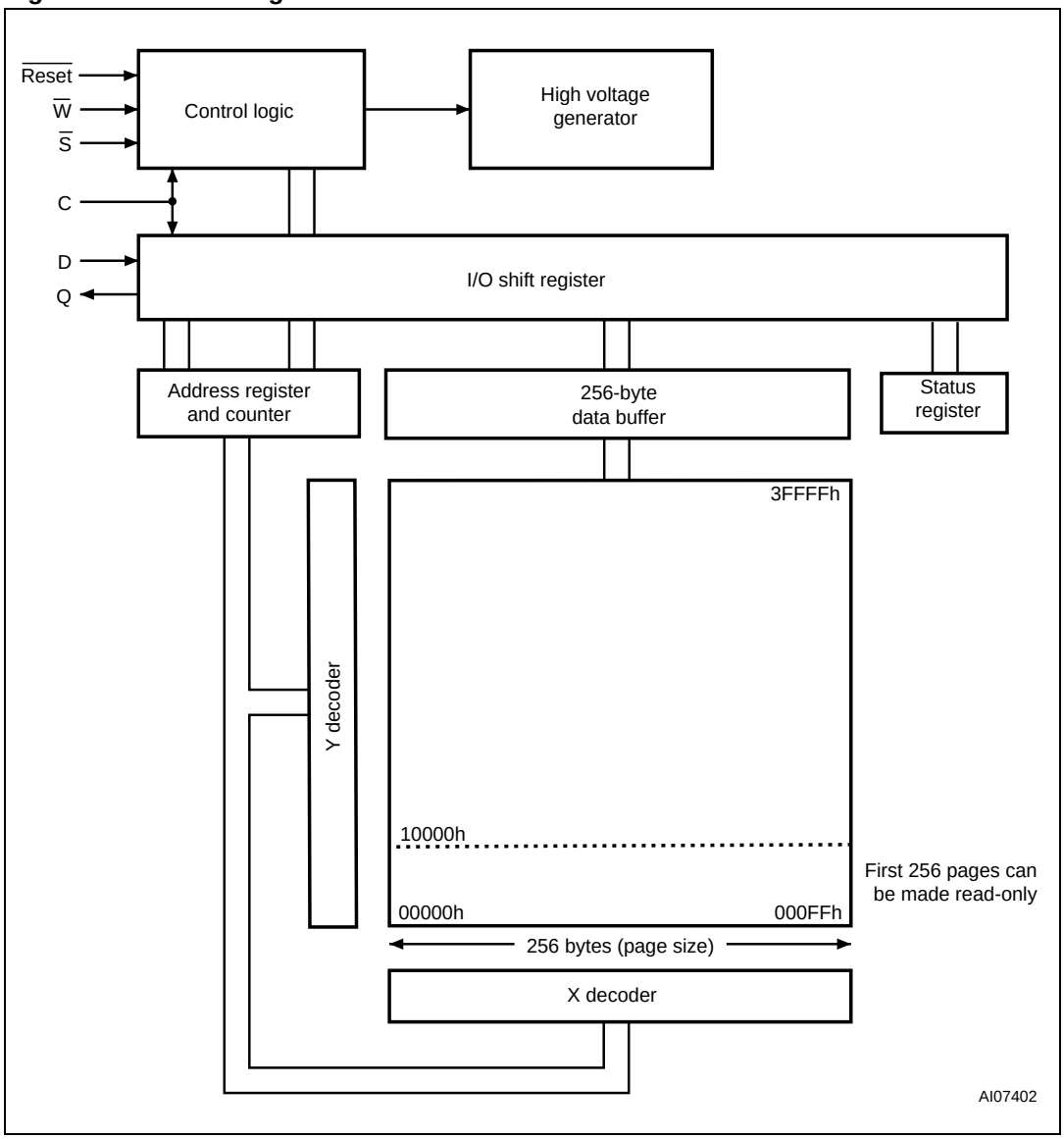
- programmed (bits are programmed from ‘1’ to ‘0’)
- erased (bits are erased from ‘0’ to ‘1’)
- written (bits are changed to either ‘0’ or ‘1’)

The device is page or sector erasable (bits are erased from ‘0’ to ‘1’).

Table 2. Memory organization

Sector	Address range	
3	30000h	3FFFFh
2	20000h	2FFFFh
1	10000h	1FFFFh
0	00000h	0FFFFh

Figure 5. Block diagram



6 Instructions

All instructions, addresses and data are shifted in and out of the device, most significant bit first.

Serial data input (D) is sampled on the first rising edge of Serial Clock (C) after Chip Select ($\overline{S}$) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on serial data input (D), each bit being latched on the rising edges of Serial Clock (C).

The instruction set is listed in *Table 3*.

Every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none.

In the case of a read data bytes (READ), read data bytes at higher speed (FAST_READ) or read status register (RDSR) instruction, the shifted-in instruction sequence is followed by a data-out sequence. Chip Select ($\overline{S}$) can be driven High after any bit of the data-out sequence is being shifted out.

In the case of a page write (PW), page program (PP), page erase (PE), sector erase (SE), write enable (WREN), write disable (WRDI), deep power-down (DP) or release from deep power-down (RDP) instruction, Chip Select ($\overline{S}$) must be driven High exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Select ($\overline{S}$) must driven High when the number of clock pulses after Chip Select ($\overline{S}$) being driven Low is an exact multiple of eight.

All attempts to access the memory array during a write cycle, program cycle or erase cycle are ignored, and the internal write cycle, program cycle or erase cycle continues unaffected.

Table 3. Instruction set

Instruction	Description	One-byte instruction code		Address bytes	Dummy bytes	Data bytes
WREN	Write enable	0000 0110	06h	0	0	0
WRDI	Write disable	0000 0100	04h	0	0	0
RDID	Read identification	1001 1111	9Fh	0	0	1 to 3
RDSR	Read status register	0000 0101	05h	0	0	1 to ∞
READ	Read data bytes	0000 0011	03h	3	0	1 to ∞
FAST_READ	Read data bytes at higher speed	0000 1011	0Bh	3	1	1 to ∞
PW	Page write	0000 1010	0Ah	3	0	1 to 256
PP	Page program	0000 0010	02h	3	0	1 to 256
PE	Page erase	1101 1011	DBh	3	0	0
SE	Sector erase	1101 1000	D8h	3	0	0
DP	Deep power-down	1011 1001	B9h	0	0	0
RDP	Release from deep power-down	1010 1011	ABh	0	0	0

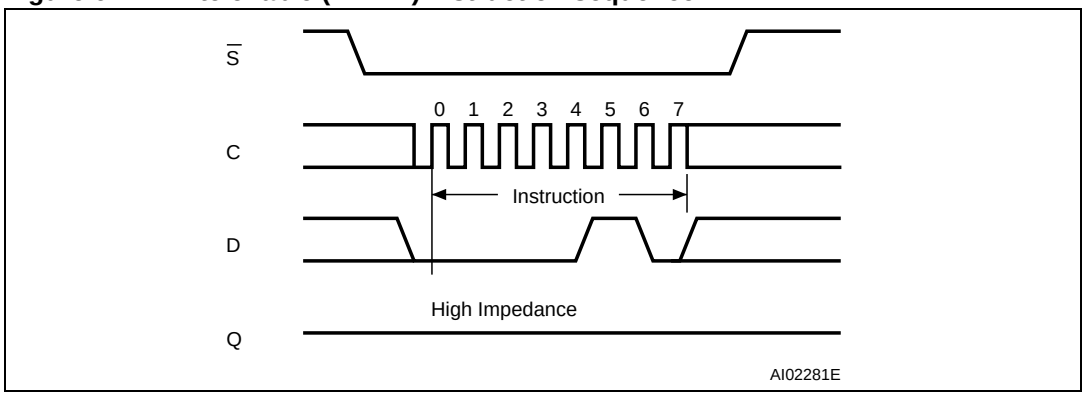
6.1 Write enable (WREN)

The write enable (WREN) instruction (*Figure 6*) sets the write enable latch (WEL) bit.

The write enable latch (WEL) bit must be set prior to every page write (PW), page program (PP), page erase (PE), and sector erase (SE) instruction.

The write enable (WREN) instruction is entered by driving Chip Select ($\overline{S}$) Low, sending the instruction code, and then driving Chip Select ($\overline{S}$) High.

Figure 6. Write enable (WREN) instruction sequence



6.2 Write disable (WRDI)

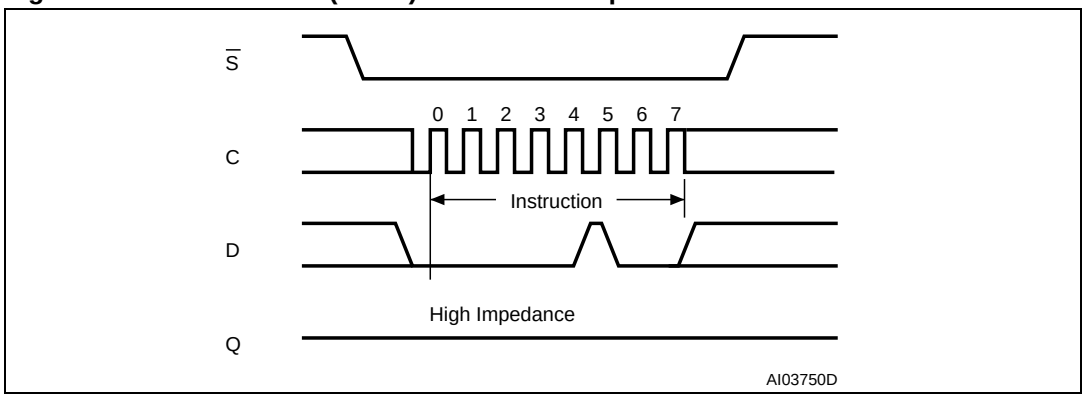
The write disable (WRDI) instruction (*Figure 7*) resets the write enable latch (WEL) bit.

The write disable (WRDI) instruction is entered by driving Chip Select ($\overline{S}$) Low, sending the instruction code, and then driving Chip Select ($\overline{S}$) High.

The write enable latch (WEL) bit is reset under the following conditions:

- Power-up
- Write disable (WRDI) instruction completion
- Page write (PW) instruction completion
- Page program (PP) instruction completion
- Page erase (PE) instruction completion
- Sector erase (SE) instruction completion

Figure 7. Write disable (WRDI) instruction sequence



6.3 Read identification (RDID)

The read identification (RDID) instruction allows to read the device identification data:

- Manufacturer identification (1 byte)
- Device identification (2 bytes)
- A unique ID code (UID) (17 bytes, of which 16 available upon customer request)[a].

The manufacturer identification is assigned by JEDEC, and has the value 20h for Numonyx. The device identification is assigned by the device manufacturer, and indicates the memory type in the first byte (40h), and the memory capacity of the device in the second byte (12h). The UID contains the length of the following data in the first byte (set to 10h), and 16 bytes of the optional customized factory data (CFD) content. The CFD bytes are read-only and can be programmed with customers data upon their demand. If the customers do not make requests, the devices are shipped with all the CFD bytes programmed to zero (00h).

Any read identification (RDID) instruction while an erase or program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

The device is first selected by driving Chip Select ($\overline{S}$) Low. Then, the 8-bit instruction code for the instruction is shifted in. After this, the 24-bit device identification, stored in the memory, the 8-bit CFD length followed by 16 bytes of CFD content will be shifted out on serial data output (Q). Each bit is shifted out during the falling edge of Serial Clock (C).

The instruction sequence is shown in *Figure 8*.

The read identification (RDID) instruction is terminated by driving Chip Select ($\overline{S}$) High at any time during data output.

When Chip Select ($\overline{S}$) is driven High, the device is put in the standby power mode. Once in the standby power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

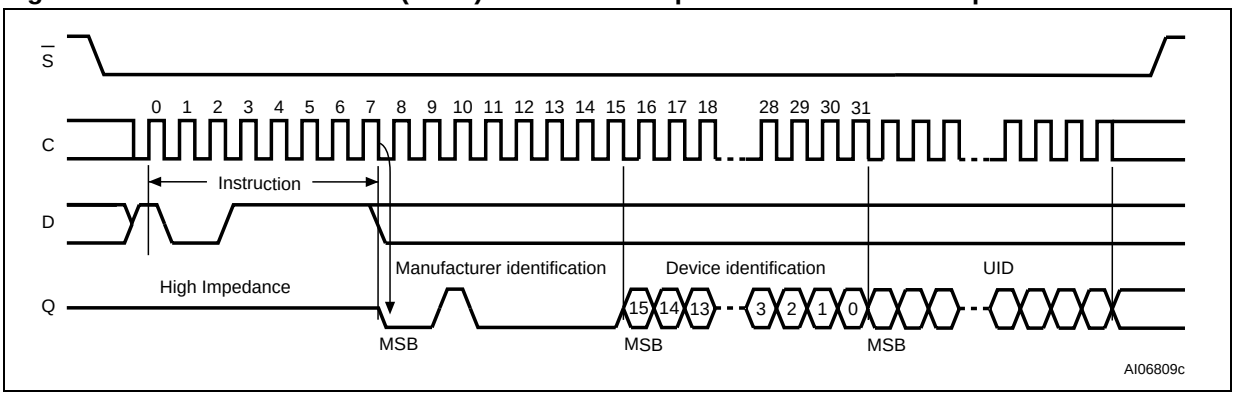
Table 4. Read identification (RDID) data-out sequence

Manufacturer identification	Device Identification		UID[1]	
	Memory type	Memory capacity	CFD length	CFD content
20h	40h	12h	10h	16 bytes

1. The unique ID code is available only in the T9HX process (see *Important note on page 6*).

a. The 17 bytes of unique ID code are available only in the T9HX process (see *Important note on page 6*).

Figure 8. Read identification (RDID) instruction sequence and data-out sequence



1. The unique ID code is available only in the T9HX process (see *Important note on page 6*).

6.4 Read status register (RDSR)

The read status register (RDSR) instruction allows the status register to be read. The status register may be read at any time, even while a program, erase or write cycle is in progress. When one of these cycles is in progress, it is recommended to check the write in progress (WIP) bit before sending a new instruction to the device. It is also possible to read the status register continuously, as shown in *Figure 9*.

The status bits of the status register are as follows:

6.4.1 WIP bit

The write in progress (WIP) bit indicates whether the memory is busy with a write, program or erase cycle. When set to ‘1’, such a cycle is in progress, when reset to ‘0’ no such cycle is in progress.

6.4.2 WEL bit

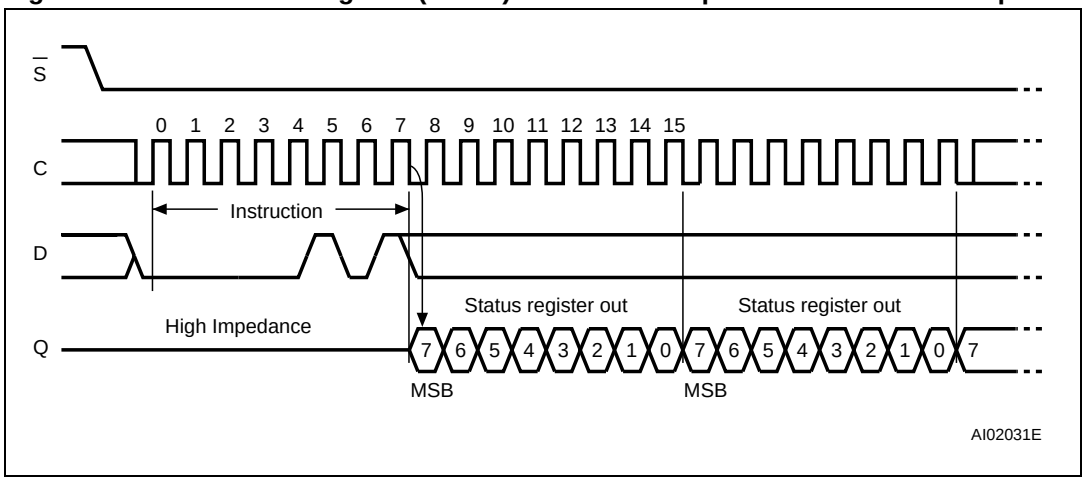
The write enable latch (WEL) bit indicates the status of the internal write enable latch. When set to ‘1’ the internal write enable latch is set, when set to ‘0’ the internal write enable latch is reset and no write, program or erase instruction is accepted.

Table 5. Status register format

b7							b0
0	0	0	0	0	0	WEL(1)	WIP(1)

1. WEL and WIP are volatile read-only bits (WEL is set and reset by specific instructions; WIP is automatically set and reset by the internal logic of the device).

Figure 9. Read status register (RDSR) instruction sequence and data-out sequence



6.5 Read data bytes (READ)

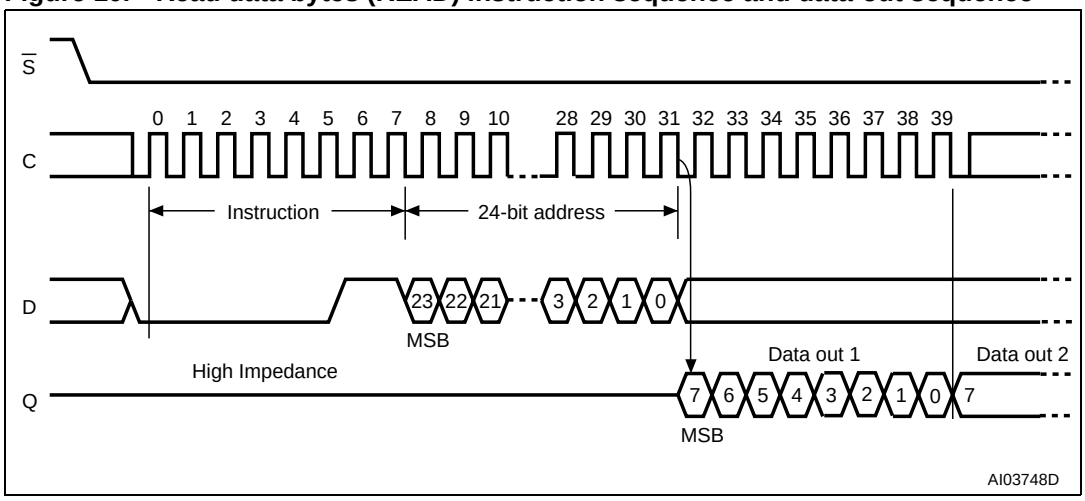
The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the read data bytes (READ) instruction is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on serial data output (Q), each bit being shifted out, at a maximum frequency f_R, during the falling edge of Serial Clock (C).

The instruction sequence is shown in *Figure 10*.

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single read data bytes (READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The read data bytes (READ) instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) can be driven High at any time during data output. Any read data bytes (READ) instruction, while an erase, program or write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 10. Read data bytes (READ) instruction sequence and data-out sequence



1. Address bits A23 to A18 are don't care.

6.6 Read data bytes at higher speed (FAST_READ)

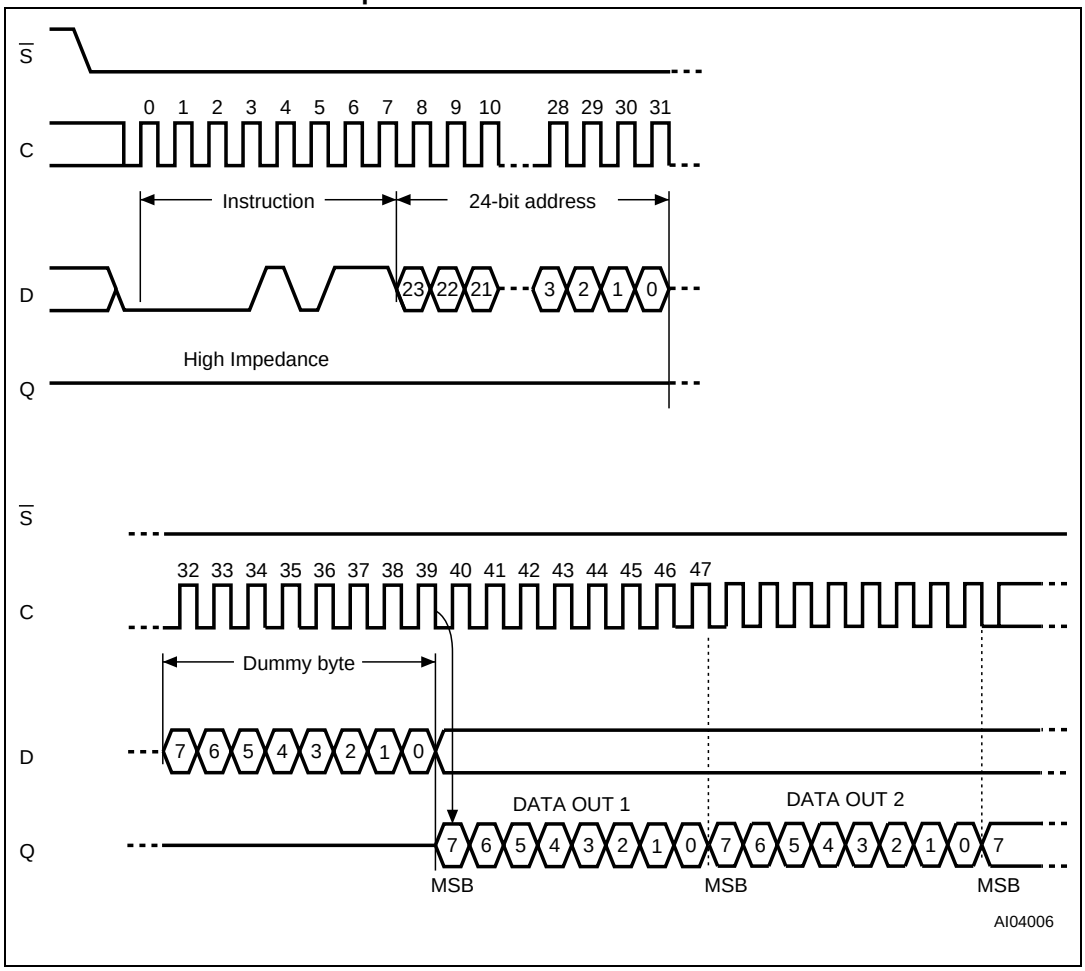
The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the read data bytes at higher speed (FAST_READ) instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on serial data output (Q), each bit being shifted out, at a maximum frequency f_C, during the falling edge of Serial Clock (C).

The instruction sequence is shown in *Figure 11*.

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single read data bytes at higher speed (FAST_READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The read data bytes at higher speed (FAST_READ) instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) can be driven High at any time during data output. Any read data bytes at higher speed (FAST_READ) instruction, while an erase, program or write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 11. Read data bytes at higher speed (FAST_READ) instruction sequence and data-out sequence



1. Address bits A23 to A18 are don't care.

6.7 Page write (PW)

The page write (PW) instruction allows bytes to be written in the memory. Before it can be accepted, a write enable (WREN) instruction must previously have been executed. After the write enable (WREN) instruction has been decoded, the device sets the write enable latch (WEL).

The page write (PW) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, three address bytes and at least one data byte on serial data input (D). The rest of the page remains unchanged if no power failure occurs during this write cycle.

The page write (PW) instruction performs a page erase cycle even if only one byte is updated.

If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data exceeding the addressed page boundary wrap round, and are written from the start address of the same page (the one whose 8 least significant address bits (A7-A0) are all zero). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 12*.

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be written correctly within the same page. If less than 256 Data bytes are sent to device, they are correctly written at the requested addresses without having any effects on the other bytes of the same page.

For optimized timings, it is recommended to use the page write (PW) instruction to write all consecutive targeted bytes in a single sequence versus using several page write (PW) sequences with each containing only a few bytes (see *Table 14: AC characteristics (50 MHz operation)* and *Table 15: AC characteristics (75 MHz operation, T9HX (0.11 µm) process)*).

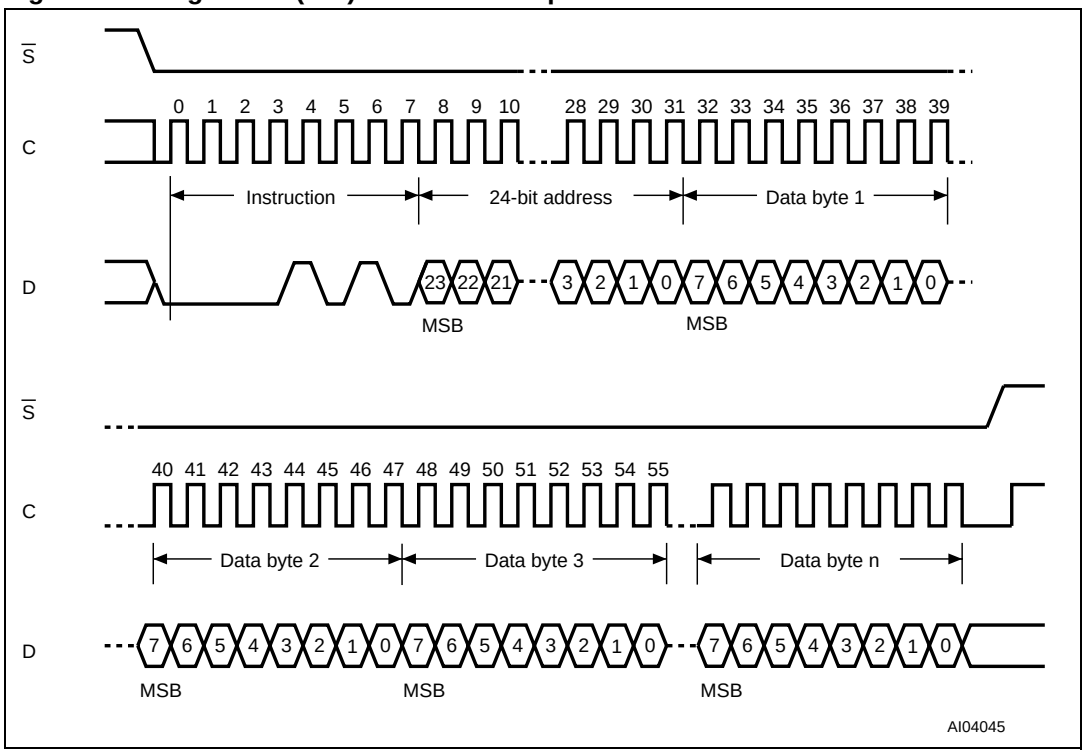
Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the page write (PW) instruction is not executed.

As soon as Chip Select ($\overline{S}$) is driven High, the self-timed page write cycle (whose duration is t_{PW}) is initiated. While the page write cycle is in progress, the status register may be read to check the value of the write in progress (WIP) bit. The write in progress (WIP) bit is 1 during the self-timed page write cycle, and is 0 when it is completed. At some unspecified time before the cycle is complete, the write enable latch (WEL) bit is reset.

A page write (PW) instruction applied to a page that is hardware protected is not executed.

Any page write (PW) instruction, while an erase, program or write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 12. Page write (PW) instruction sequence



1. Address bits A23 to A18 are don't care.
2. $1 \leq n \leq 256$.

6.8 Page program (PP)

The page program (PP) instruction allows bytes to be programmed in the memory (changing bits from ‘1’ to ‘0’, only). Before it can be accepted, a write enable (WREN) instruction must previously have been executed. After the write enable (WREN) instruction has been decoded, the device sets the write enable latch (WEL).

The page program (PP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, three address bytes and at least one data byte on serial data input (D). If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data exceeding the addressed page boundary wrap round, and are programmed from the start address of the same page (the one whose 8 least significant address bits (A7-A0) are all zero). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 13*.

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

For optimized timings, it is recommended to use the page program (PP) instruction to program all consecutive targeted bytes in a single sequence versus using several page program (PP) sequences with each containing only a few bytes (see *Table 14: AC characteristics (50 MHz operation)* and *Table 15: AC characteristics (75 MHz operation, T9HX (0.11 µm) process)*).

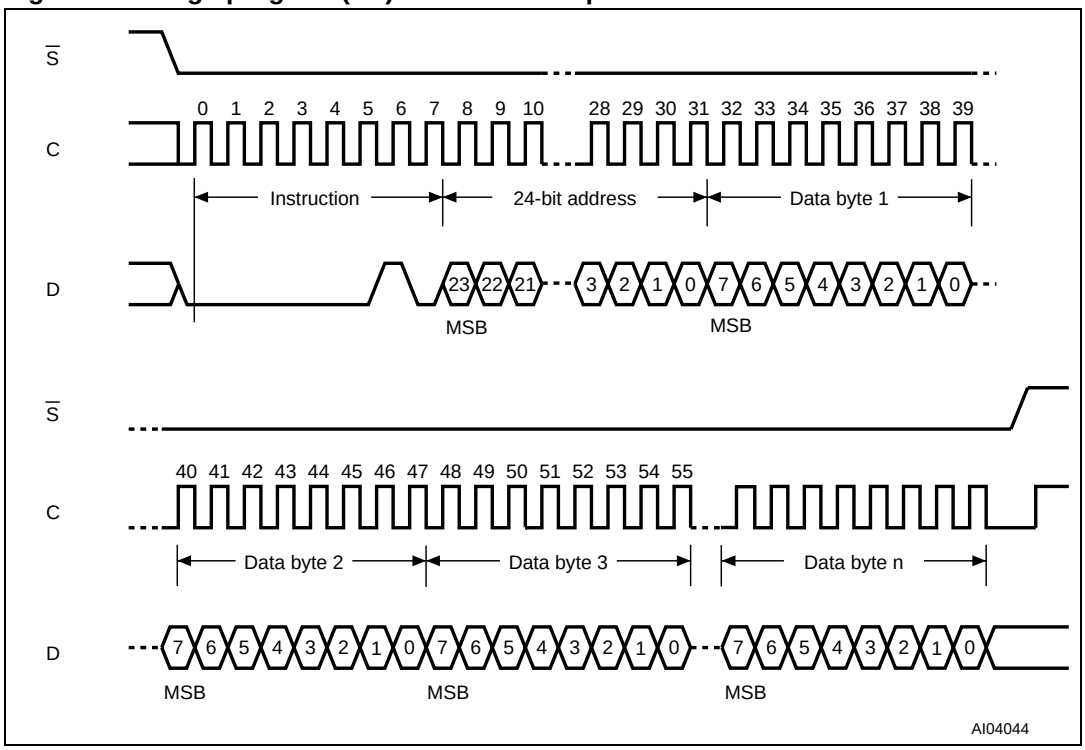
Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the page program (PP) instruction is not executed.

As soon as Chip Select ($\overline{S}$) is driven High, the self-timed page program cycle (whose duration is t_{PP}) is initiated. While the page program cycle is in progress, the status register may be read to check the value of the write in progress (WIP) bit. The write in progress (WIP) bit is 1 during the self-timed page program cycle, and is 0 when it is completed. At some unspecified time before the cycle is complete, the write enable latch (WEL) bit is reset.

A page program (PP) instruction applied to a page that is hardware protected is not executed.

Any page program (PP) instruction, while an erase, program or write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 13. Page program (PP) instruction sequence



1. Address bits A23 to A18 are don't care.
2. $1 \leq n \leq 256$.

6.9 Page erase (PE)

The page erase (PE) instruction sets to ‘1’ (FFh) all bits inside the chosen page. Before it can be accepted, a write enable (WREN) instruction must previously have been executed. After the write enable (WREN) instruction has been decoded, the device sets the write enable latch (WEL).

The page erase (PE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, and three address bytes on serial data input (D). Any address inside the page is a valid address for the page erase (PE) instruction. Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

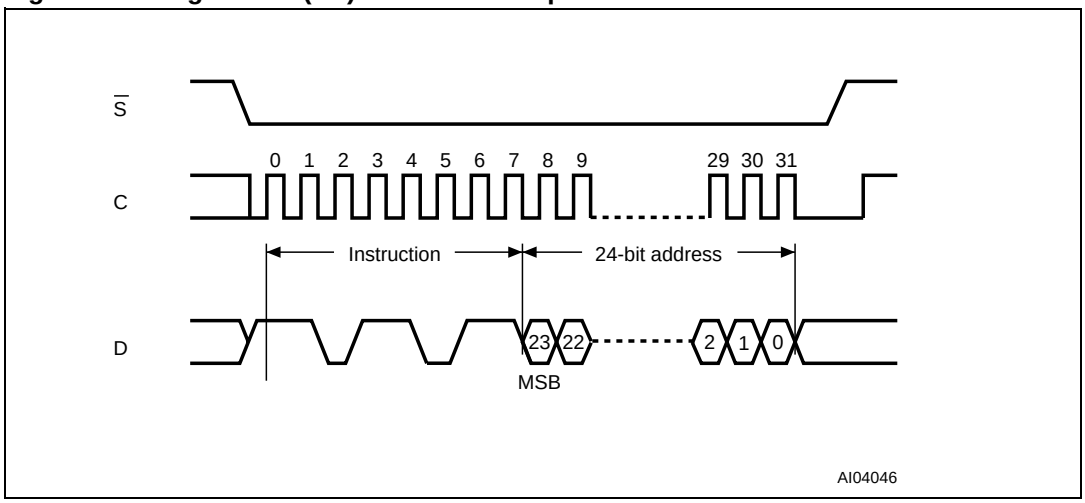
The instruction sequence is shown in *Figure 14*.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the page erase (PE) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed page erase cycle (whose duration is t_{PE}) is initiated. While the page erase cycle is in progress, the status register may be read to check the value of the write in progress (WIP) bit. The write in progress (WIP) bit is 1 during the self-timed page erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is complete, the write enable latch (WEL) bit is reset.

A page erase (PE) instruction applied to a page that is hardware protected is not executed.

Any page erase (PE) instruction, while an erase, program or write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 14. Page erase (PE) instruction sequence



1. Address bits A23 to A18 are don’t care.

6.10 Sector erase (SE)

The sector erase (SE) instruction sets to '1' (FFh) all bits inside the chosen sector. Before it can be accepted, a write enable (WREN) instruction must previously have been executed. After the write enable (WREN) instruction has been decoded, the device sets the write enable latch (WEL).

The sector erase (SE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, and three address bytes on serial data input (D). Any address inside the sector (see *Table 2*) is a valid address for the sector erase (SE) instruction. Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

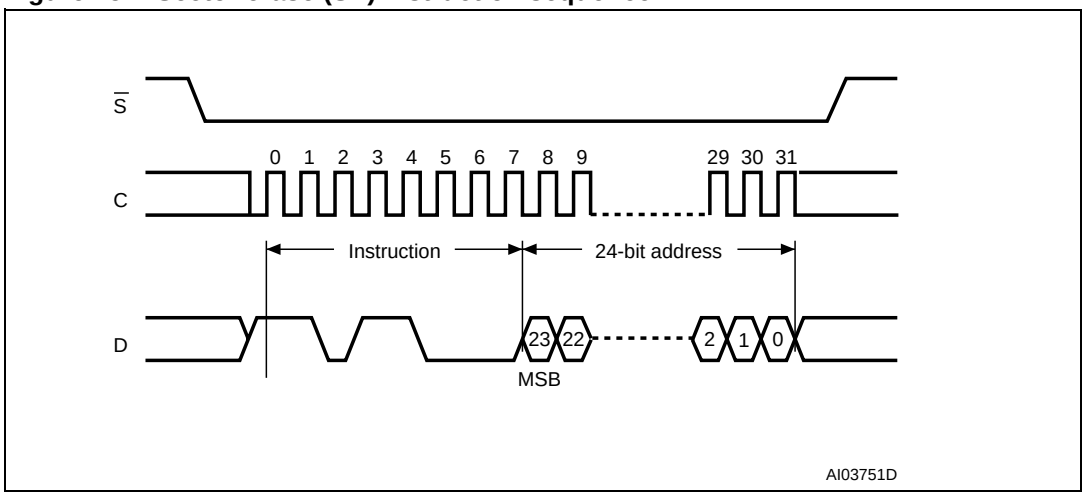
The instruction sequence is shown in *Figure 15*.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the sector erase (SE) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed sector erase cycle (whose duration is t_{SE}) is initiated. While the sector erase cycle is in progress, the status register may be read to check the value of the write in progress (WIP) bit. The write in progress (WIP) bit is 1 during the self-timed sector erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is complete, the write enable latch (WEL) bit is reset.

A sector erase (SE) instruction applied to a sector that contains a page that is hardware protected is not executed.

Any sector erase (SE) instruction, while an erase, program or write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 15. Sector erase (SE) instruction sequence



1. Address bits A23 to A18 are don't care.

6.11 Deep power-down (DP)

Executing the deep power-down (DP) instruction is the only way to put the device in the lowest consumption mode (the deep power-down mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all write, program and erase instructions.

Driving Chip Select ($\overline{S}$) High deselects the device, and puts the device in the standby power mode (if there is no internal cycle currently in progress). But this mode is not the deep power-down mode. The deep power-down mode can only be entered by executing the deep power-down (DP) instruction, to reduce the standby current (from I_{CC1} to I_{CC2}, as specified in *Table 11: DC characteristics*).

Once the device has entered the deep power-down mode, all instructions are ignored except the release from deep power-down (RDP) instruction. This releases the device from this mode.

The deep power-down mode automatically stops at power-down, and the device always powers-up in the standby power mode.

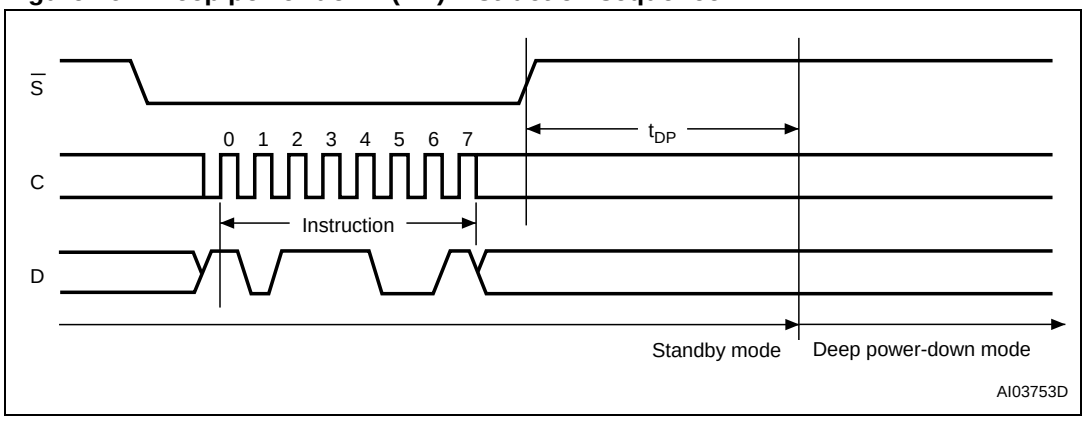
The deep power-down (DP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on serial data input (D). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 16*.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the deep power-down (DP) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the deep power-down mode is entered.

Any deep power-down (DP) instruction, while an erase, program or write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 16. Deep power-down (DP) instruction sequence



6.12 Release from deep power-down (RDP)

Once the device has entered the deep power-down mode, all instructions are ignored except the release from deep power-down (RDP) instruction. Executing this instruction takes the device out of the deep power-down mode.

The release from deep power-down (RDP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on serial data input (D). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

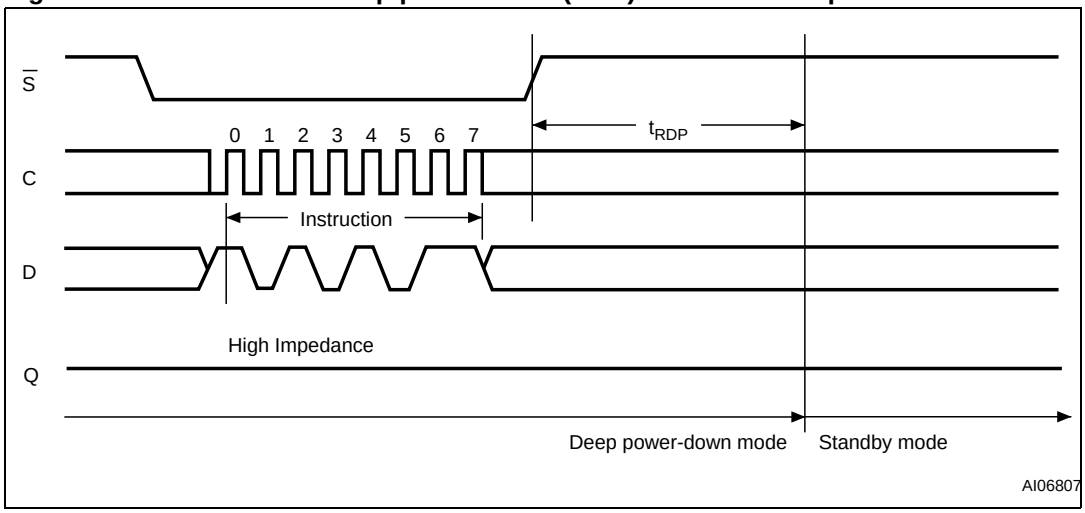
The instruction sequence is shown in *Figure 17*.

The release from deep power-down (RDP) instruction is terminated by driving Chip Select ($\overline{S}$) High. Sending additional clock cycles on Serial Clock (C), while Chip Select ($\overline{S}$) is driven Low, cause the instruction to be rejected, and not executed.

After Chip Select ($\overline{S}$) has been driven High, followed by a delay, t_{RDP}, the device is put in the standby power mode. Chip Select ($\overline{S}$) must remain High at least until this period is over. The device waits to be selected, so that it can receive, decode and execute instructions.

Any release from deep power-down (RDP) instruction, while an erase, program or write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 17. Release from deep power-down (RDP) instruction sequence



7 Power-up and power-down

At power-up and power-down, the device must not be selected (that is Chip Select ($\overline{S}$) must follow the voltage applied on V_{CC}) until V_{CC} reaches the correct value:

- V_{CC}(min) at power-up, and then for a further delay of t_{VSL}
- V_{SS} at power-down

A safe configuration is provided in *Section 3: SPI modes*.

To avoid data corruption and inadvertent write operations during power-up, a power on reset (POR) circuit is included. The logic inside the device is held reset while V_{CC} is less than the power on reset (POR) threshold value, V_{WI} – all operations are disabled, and the device does not respond to any instruction.

Moreover, the device ignores all write enable (WREN), page write (PW), page program (PP), page erase (PE) and sector erase (SE) instructions until a time delay of t_{PUW} has elapsed after the moment that V_{CC} rises above the V_{WI} threshold. However, the correct operation of the device is not guaranteed if, by this time, V_{CC} is still below V_{CC}(min). No write, program or erase instructions should be sent until the later of:

- t_{PUW} after V_{CC} passed the V_{WI} threshold
- t_{VSL} after V_{CC} passed the V_{CC}(min) level

These values are specified in *Table 6*.

If the delay, t_{VSL}, has elapsed, after V_{CC} has risen above V_{CC}(min), the device can be selected for read instructions even if the t_{PUW} delay is not yet fully elapsed.

As an extra protection, the Reset ($\overline{Reset}$) signal can be driven Low for the whole duration of the power-up and power-down phases.

At power-up, the device is in the following state:

- The device is in the standby power mode (not the deep power-down mode).
- The write enable latch (WEL) bit is reset.
- The write in progress (WIP) bit is reset.

Normal precautions must be taken for supply rail decoupling, to stabilize the V_{CC} supply. Each device in a system should have the V_{CC} rail decoupled by a suitable capacitor close to the package pins (generally, this capacitor is of the order of 100 nF).

At power-down, when V_{CC} drops from the operating voltage, to below the power on reset (POR) threshold value, V_{WI}, all operations are disabled and the device does not respond to any instruction (the designer needs to be aware that if a power-down occurs while a write, program or erase cycle is in progress, some data corruption can result).

Figure 18. Power-up timing

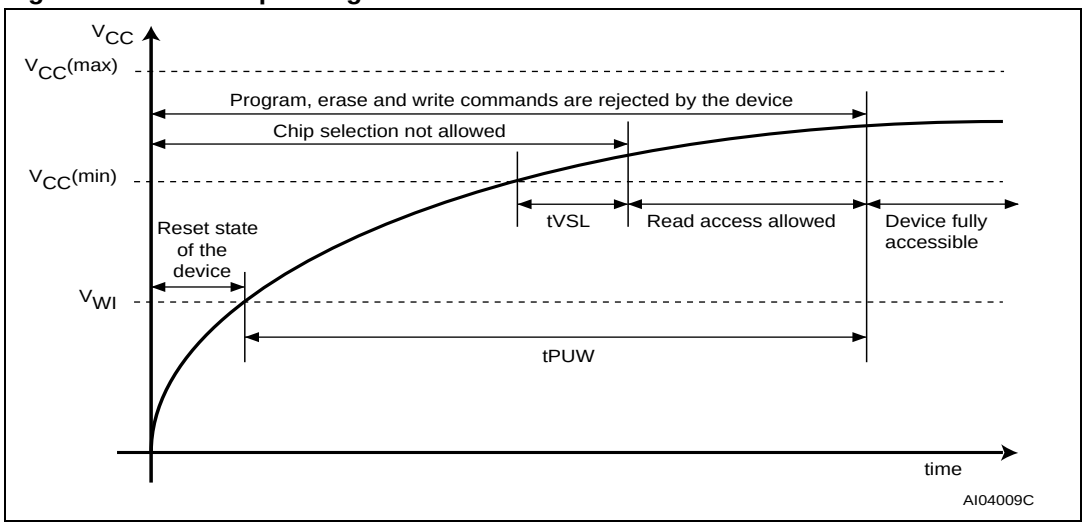


Table 6. Power-up timing and V_{WI} threshold

Symbol	Parameter	Min	Max	Unit
t_{VSL}(1)	V_{CC}(min) to $\overline{S}$ low	30		µs
t_{PUW}(1)	Time delay before the first write, program or erase instruction	1	10	ms
V_{WI}(1)	Write inhibit voltage	1.5	2.5	V

1. These parameters are characterized only, over the temperature range –40 °C to +85 °C.

8 Initial delivery state

The device is delivered with the memory array erased: all bits are set to ‘1’ (each byte contains FFh). All usable status register bits are ‘0’.

9 Maximum ratings

Stressing the device outside the ratings listed in *Table 7: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability (refer to quality documents for further details).

Table 7. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	See note (1)		°C
V_{IO}	Input and output voltage (with respect to ground)	–0.6	V_{CC} + 0.6	V
V_{CC}	Supply voltage	–0.6	4.0	V
V_{ESD}	Electrostatic discharge voltage (human body model)(2)	–2000	2000	V

1. Compliant with JEDEC Std J-STD-020C (for small body, Sn-Pb or Pb assembly), the ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)

10 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 8. Operating conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage	2.7	3.6	V
T_A	Ambient operating temperature	–40	85	°C

Table 9. AC measurement conditions

Symbol	Parameter	Min	Max	Unit
C_L	Load capacitance	30		pF
	Input rise and fall times		5	ns
	Input pulse voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input and output timing reference voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V

1. Output Hi-Z is defined as the point where data out is no longer driven.

Figure 19. AC measurement I/O waveform

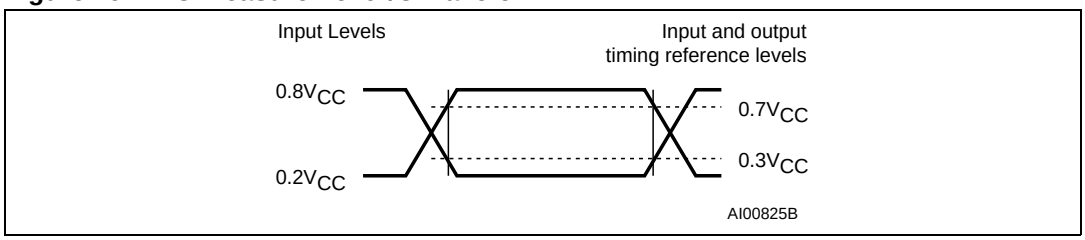


Table 10. Capacitance

Symbol	Parameter	Test condition	Min	Max	Unit
C_{OUT}	Output capacitance (Q)	V_{OUT} = 0 V		8	pF
C_{IN}	Input capacitance (other pins)	V_{IN} = 0 V		6	pF

1. Sampled only, not 100% tested, at T_A=25 °C and a frequency of 33 MHz.

Table 11. DC characteristics

Symbol	Parameter	Test condition (in addition to those in *Table 8*)	Min	Max	Unit
I_{LI}	Input leakage current			± 2	µA
I_{LO}	Output leakage current			± 2	µA
I_{CC1}	Standby current (standby and reset modes)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		50	µA
I_{CC2}	Deep power-down current	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		10	µA
I_{CC3}	Operating current (FAST_READ)	C = 0.1V_{CC} / 0.9.V_{CC} at 33 MHz, Q = open		4	mA
		C = 0.1V_{CC} / 0.9.V_{CC} at 75 MHz, Q = open		12	
I_{CC4}	Operating current (PW)	$\overline{S}$ = V_{CC}		15	mA
I_{CC5}	Operating current (SE)	$\overline{S}$ = V_{CC}		15	mA
V_{IL}	Input low voltage		– 0.5	0.3V_{CC}	V
V_{IH}	Input high voltage		0.7V_{CC}	V_{CC}+0.4	V
V_{OL}	Output low voltage	I_{OL} = 1.6 mA		0.4	V
V_{OH}	Output high voltage	I_{OH} = –100 µA	V_{CC}–0.2		V

Table 12. AC characteristics (25 MHz operation)

Test conditions specified in *Table 8* and *Table 9*						
Symbol	**Alt.**	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
f_C	f_C	Clock frequency for the following instructions: FAST_READ, PW, PP, PE, SE, DP, RDP, WREN, WRDI, RDSR	D.C.		25	MHz
f_R		Clock frequency for read instructions	D.C.		20	MHz
t_{CH}(1)	t_{CLH}	Clock High time	18			ns
t_{CL}(1)	t_{CLL}	Clock Low time	18			ns
		Clock slew rate(2) (peak to peak)	0.03			V/ns
t_{SLCH}	t_{CSS}	$\overline{S}$ active setup time (relative to C)	10			ns
t_{CHSL}		$\overline{S}$ not active hold time (relative to C)	10			ns
t_{DVCH}	t_{DSU}	Data in setup time	5			ns
t_{CHDX}	t_{DH}	Data in hold time	5			ns
t_{CHSH}		$\overline{S}$ active hold time (relative to C)	10			ns
t_{SHCH}		$\overline{S}$ not active setup time (relative to C)	10			ns
t_{SHSL}	t_{CSH}	$\overline{S}$ deselect time	200			ns
t_{SHQZ}(2)	t_{DIS}	Output disable time			15	ns
t_{CLQV}	t_V	Clock Low to Output Valid			15	ns
t_{CLQX}	t_{HO}	Output hold time	0			ns
t_{RLRH}(2)	t_{RST}	Reset pulse width	10			µs
t_{RHSL}	t_{REC}	Reset recovery time			3	µs
t_{SHRH}		Chip should have been deselected before reset is de-asserted	10			ns
t_{WHSL}		Write protect setup time	50			ns
t_{SHWL}		Write protect hold time	100			ns
t_{DP}(2)		$\overline{S}$ to deep power-down			3	µs
t_{RDP}(2)		$\overline{S}$ High to standby power mode			30	µs
t_{PW}(3)		Page write cycle time (256 bytes)		11	25	ms
		Page write cycle time (n bytes)		10.2+ n*0.8/256		
t_{PP}(3)		Page program cycle time (256 bytes)		1.2	5	ms
		Page program cycle time (n bytes)		0.4+ n*0.8/256		
t_{PE}		Page erase cycle time		10	20	ms
t_{SE}		Sector erase cycle time		1	5	s

1. $t_{CH} + t_{CL}$ must be greater than or equal to $1/ f_C$(max).
2. Value guaranteed by characterization, not 100% tested in production.
3. When using PP and PW instructions to update consecutive bytes, optimized timings are obtained with one sequence including all the bytes versus several sequences of only a few bytes ($1 \le n \le 256$).

Table 13. AC characteristics (33 MHz operation)

33 MHz only available for products marked since week 40 of 2005(1) Test conditions specified in *Table 8* and *Table 9*						
Symbol	**Alt.**	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
f_C	f_C	Clock frequency for the following instructions: FAST_READ, PW, PP, PE, SE, DP, RDP, WREN, WRDI, RDSR	D.C.		33	MHz
f_R		Clock frequency for read instructions	D.C.		20	MHz
t_{CH}(2)	t_{CLH}	Clock High time	13			ns
t_{CL}(2)	t_{CLL}	Clock Low time	13			ns
		Clock slew rate(3) (peak to peak)	0.03			V/ns
t_{SLCH}	t_{CSS}	$\overline{S}$ active setup time (relative to C)	10			ns
t_{CHSL}		$\overline{S}$ not active hold time (relative to C)	10			ns
t_{DVCH}	t_{DSU}	Data in setup time	3			ns
t_{CHDX}	t_{DH}	Data in hold time	5			ns
t_{CHSH}		$\overline{S}$ active hold time (relative to C)	5			ns
t_{SHCH}		$\overline{S}$ not active setup time (relative to C)	5			ns
t_{SHSL}	t_{CSH}	$\overline{S}$ deselect time	200			ns
t_{SHQZ}(3)	t_{DIS}	Output disable time			12	ns
t_{CLQV}	t_V	Clock Low to Output Valid			12	ns
t_{CLQX}	t_{HO}	Output hold time	0			ns
t_{THSL}		Top sector lock setup time	50			ns
t_{SHTL}		Top sector lock hold time	100			ns
t_{DP}(3)		$\overline{S}$ to deep power-down			3	µs
t_{RDP}(3)		$\overline{S}$ High to standby power mode			30	µs
t_{PW}(4)		Page write cycle time (256 bytes)		11	25	ms
		Page write cycle time (n bytes)		10.2+ n*0.8/256		
t_{PP}(4)		Page program cycle time (256 bytes)		1.2	5	ms
		Page program cycle time (n bytes)		0.4+ n*0.8/256		
t_{PE}		Page erase cycle time		10	20	ms
t_{SE}		Sector erase cycle time		1	5	s

1. Details of how to find the date of marking are given in application note, AN1995.
2. $t_{CH} + t_{CL}$ must be greater than or equal to $1/ f_C$.
3. Value guaranteed by characterization, not 100% tested in production.
4. When using PP and PW instructions to update consecutive bytes, optimized timings are obtained with one sequence including all the bytes versus several sequences of only a few bytes ($1 \le n \le 256$).

Table 14. AC characteristics (50 MHz operation)(1)

50 MHz preliminary data for T9HX technology(2) Test conditions specified in *Table 8* and *Table 9*						
Symbol	**Alt.**	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
f_C	f_C	Clock frequency for the following instructions: FAST_READ, PW, PP, PE, SE, DP, RDP, WREN, WRDI, RDSR, RDID	D.C.		50	MHz
f_R		Clock frequency for READ instructions	D.C.		33	MHz
t_{CH}(3)	t_{CLH}	Clock High time	9			ns
t_{CL}(3)	t_{CLL}	Clock Low time	9			ns
		Clock slew rate(4) (peak to peak)	0.1			V/ns
t_{SLCH}	t_{CSS}	$\overline{S}$ active setup time (relative to C)	5			ns
t_{CHSL}		$\overline{S}$ not active hold time (relative to C)	5			ns
t_{DVCH}	t_{DSU}	Data in setup time	2			ns
t_{CHDX}	t_{DH}	Data in hold time	5			ns
t_{CHSH}		$\overline{S}$ active hold time (relative to C)	5			ns
t_{SHCH}		$\overline{S}$ not active setup time (relative to C)	5			ns
t_{SHSL}	t_{CSH}	$\overline{S}$ deselect time	100			ns
t_{SHQZ}(4)	t_{DIS}	Output disable time			8	ns
t_{CLQV}	t_V	Clock Low to Output Valid			8	ns
t_{CLQX}	t_{HO}	Output hold time	0			ns
t_{WHSL}		Write protect setup time	50			ns
t_{SHWL}		Write protect hold time	100			ns
t_{DP}(4)		$\overline{S}$ to deep power-down			3	µs
t_{RDP}(4)		$\overline{S}$ High to standby mode			30	µs
t_{RLRH}(4)	t_{RST}	Reset pulse width			10	µs
t_{RHSL}	t_{REC}	Reset recovery time			3	µs
t_{SHRH}		Chip should have been deselected before reset is de-asserted			10	ns
t_{PW}(5)		Page write cycle time (256 bytes)		11	23	ms
t_{PP}(5)		Page program cycle time (256 bytes)		0.8	3	ms
		Page program cycle time (n bytes)		int(n/8) × 0.025		
t_{PE}		Page erase cycle time		10	20	ms
t_{SE}		Sector erase cycle time		1	5	s

1. Preliminary data.
2. Delivery of parts in T9HX process to start from August 2007.
3. $t_{CH} + t_{CL}$ must be greater than or equal to $1/ f_C$.
4. Value guaranteed by characterization, not 100% tested in production.
5. n = number of bytes to program. int(A) corresponds to the upper integer part of A. Examples: int(1/8) = 1, int(16/8) = 2, int(17/8) = 3.

Table 15. AC characteristics (75 MHz operation, T9HX (0.11 µm) process(1))(2)

Test conditions specified in *Table 8* and *Table 9*						
Symbol	**Alt.**	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
f_C	f_C	Clock frequency for the following instructions: FAST_READ, PW, PP, PE, SE, DP, RDP, WREN, WRDI, RDSR, RDID	D.C.		75	MHz
f_R		Clock frequency for read instructions	D.C.		33	MHz
t_{CH}(3)	t_{CLH}	Clock High time	6			ns
t_{CL}(3)	t_{CLL}	Clock Low time	6			ns
		Clock slew rate(4) (peak to peak)	0.1			V/ns
t_{SLCH}	t_{CSS}	$\overline{S}$ active setup time (relative to C)	5			ns
t_{CHSL}		$\overline{S}$ not active hold time (relative to C)	5			ns
t_{DVCH}	t_{DSU}	Data in setup time	2			ns
t_{CHDX}	t_{DH}	Data in hold time	5			ns
t_{CHSH}		$\overline{S}$ active hold time (relative to C)	5			ns
t_{SHCH}		$\overline{S}$ not active setup time (relative to C)	5			ns
t_{SHSL}	t_{CSH}	$\overline{S}$ deselect time	100			ns
t_{SHQZ}(4)	t_{DIS}	Output disable time			8	ns
t_{CLQV}	t_V	Clock Low to Output valid			8	ns
t_{CLQX}	t_{HO}	Output hold time	0			ns
t_{WHSL}(5)		Write protect setup time	20			ns
t_{SHWL}(5)		Write protect hold time	100			ns
t_{DP}(4)		$\overline{S}$ to deep power-down			3	µs
t_{RDP}(4)		$\overline{S}$ High to standby mode			30	µs
t_W		Write status register cycle time		3	15	ms
t_{PW}(6)		Page write cycle time (256 bytes)		11	23	ms
t_{PP}(6)		Page program cycle time (256 bytes)		0.8	3	ms
		Page program cycle time (n bytes)		int(n/8) × 0.025(7)		
t_{PE}		Page erase cycle time		10	20	ms
t_{SE}		Sector erase cycle time		1.5	5	s

1. See *Important note on page 6*.
2. Details of how to find the technology process in the marking are given in AN1995, see also *Section 12: Ordering information*.
3. $t_{CH} + t_{CL}$ must be greater than or equal to $1/ f_C$.
4. Value guaranteed by characterization, not 100% tested in production.
5. Only applicable as a constraint for a WRSR instruction when SRWD is set to ‘1’.
6. When using PP and PW instructions to update consecutive bytes, optimized timings are obtained with one sequence including all the bytes versus several sequences of only a few bytes ($1 \le n \le 256$).
7. int(A) corresponds to the upper integer part of A. For instance, int(12/8) = 2, int(32/8) = 4 int(15.3) =16.

Figure 20. Serial input timing

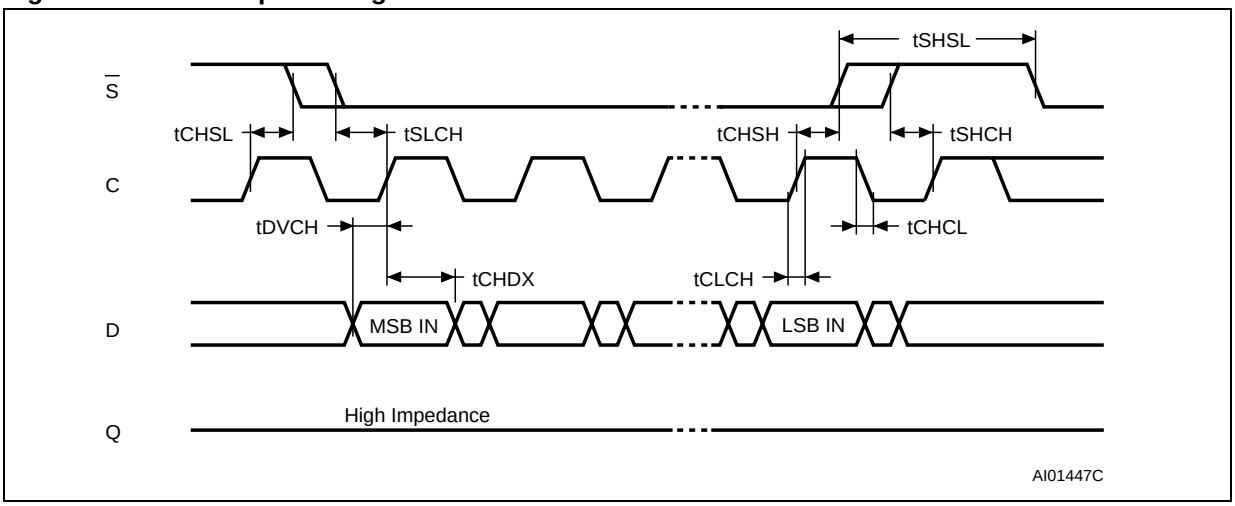


Figure 21. Write protect setup and hold timing

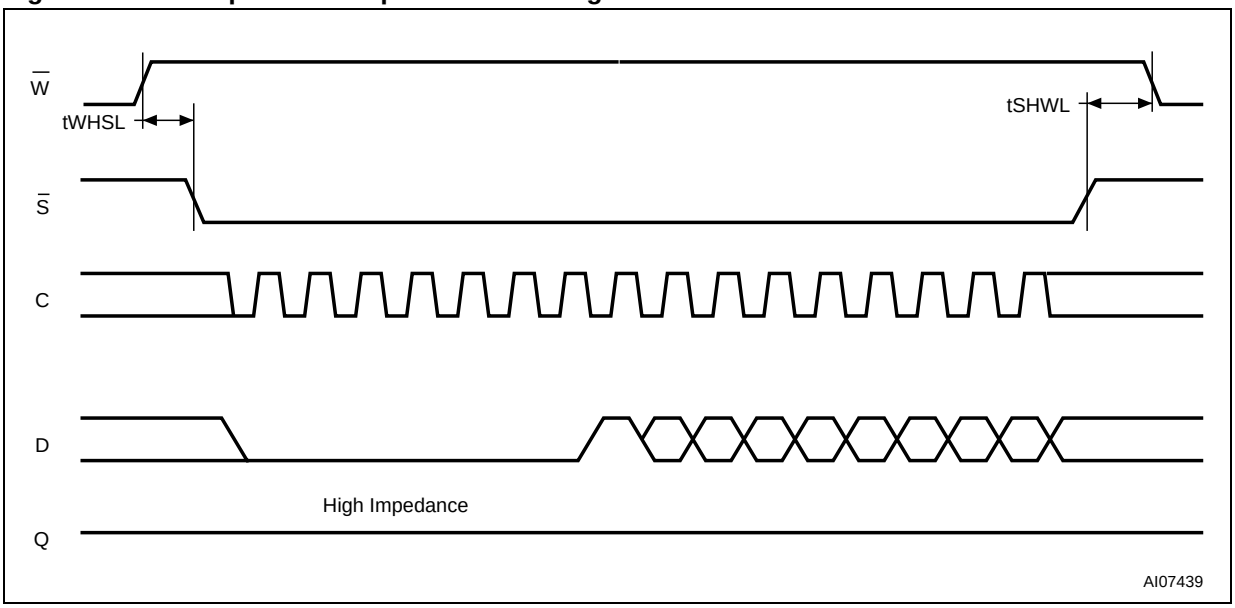


Figure 22. Output timing

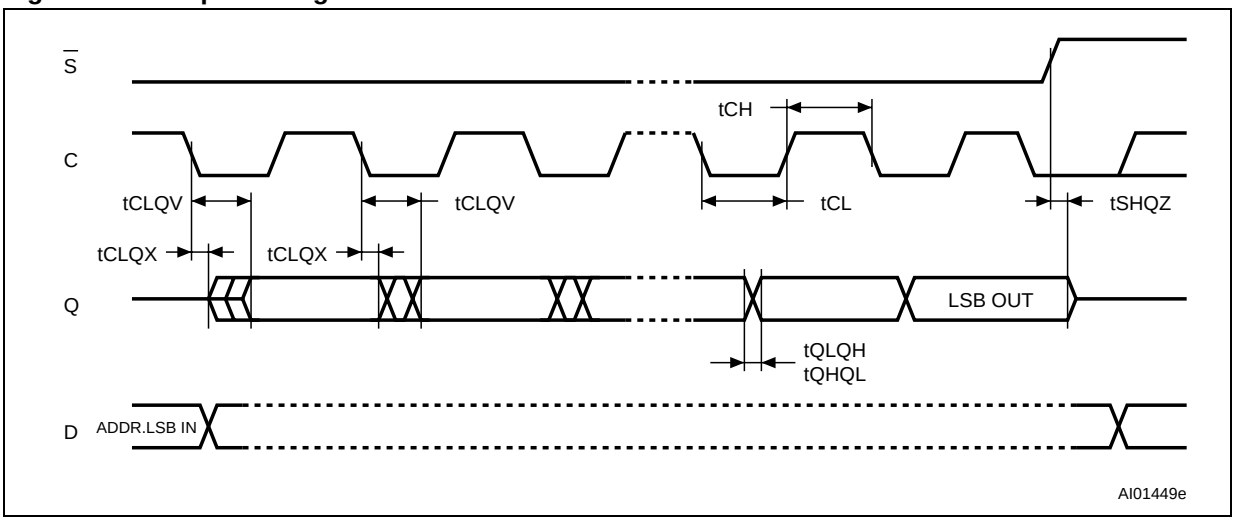
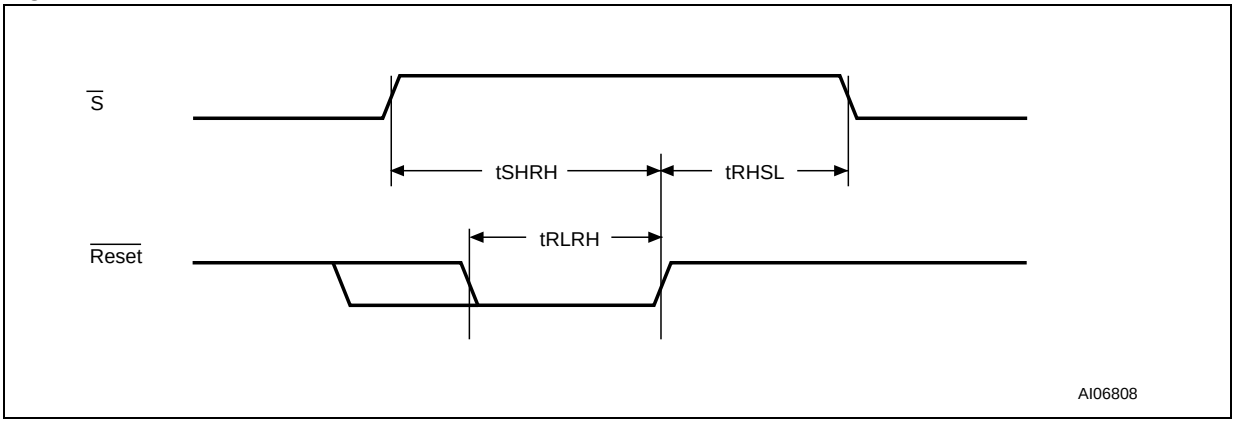


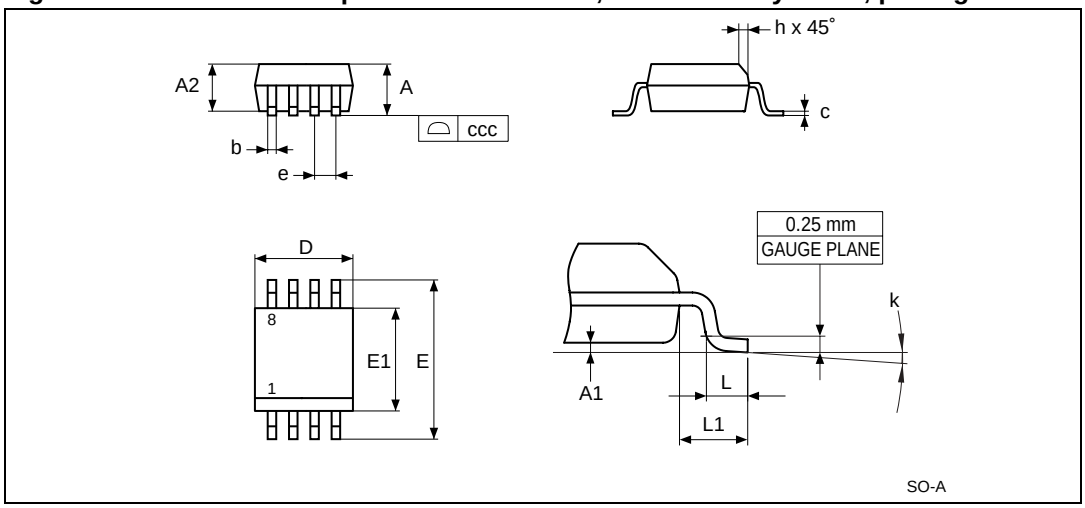
Figure 23. Reset AC waveforms



11 Package mechanical

To meet environmental requirements, Numonyx offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

Figure 24. SO8N – 8 lead plastic small outline, 150 mils body width, package outline

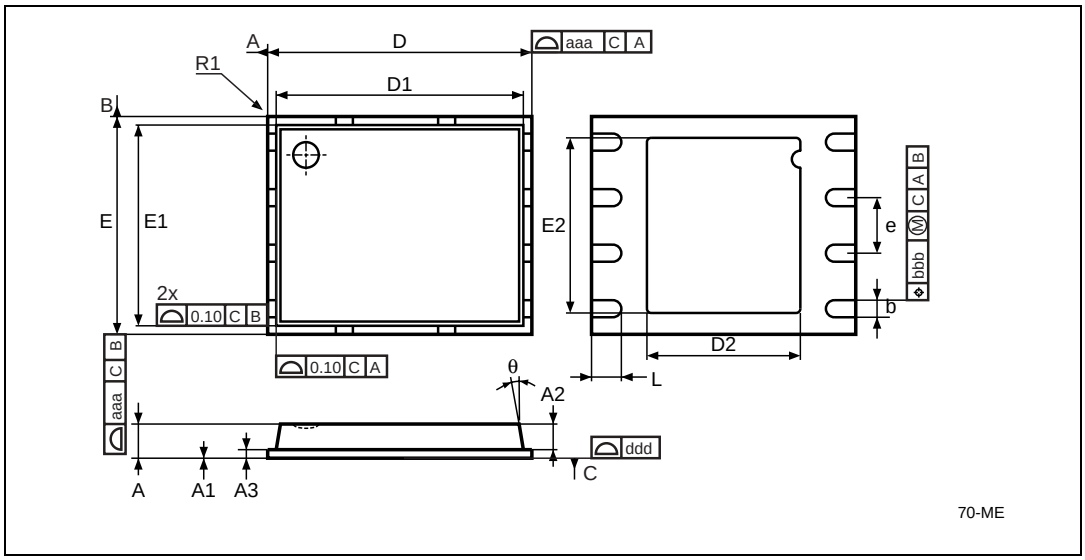


1. Drawing is not to scale.

Table 16. SO8N – 8 lead plastic small outline, 150 mils body width, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.069
A1		0.10	0.25		0.004	0.010
A2		1.25			0.049	
b		0.28	0.48		0.011	0.019
c		0.17	0.23		0.007	0.009
ccc			0.10			0.004
D	4.90	4.80	5.00	0.193	0.189	0.197
E	6.00	5.80	6.20	0.236	0.228	0.244
E1	3.90	3.80	4.00	0.154	0.150	0.157
e	1.27	–	–	0.050	–	–
h		0.25	0.50		0.010	0.020
k		0°	8°		0°	8°
L		0.40	1.27		0.016	0.050
L1	1.04			0.041		

Figure 25. MLP8, 8-lead very thin dual flat package no lead, 6 × 5 mm, package outline



1. Drawing is not to scale.

Table 17. MLP8, 8-lead very thin dual flat package no lead, 6 × 5 mm, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A	0.85	0.80	1.00	0.033	0.031	0.039
A1		0.00	0.05		0.000	0.002
A2	0.65			0.026		
A3	0.20			0.008		
b	0.40	0.35	0.48	0.016	0.014	0.019
D	6.00			0.236		
D1	5.75			0.226		
D2	3.40	3.20	3.60	0.134	0.126	0.142
E	5.00			0.197		
E1	4.75			0.187		
E2	4.00	3.80	4.30	0.157	0.150	0.169
e	1.27	–	–	0.050	–	–
R1	0.10	0.00		0.004	0.000	
L	0.60	0.50	0.75	0.024	0.020	0.029
Θ			12°			12°
aaa			0.15			0.006
bbb			0.10			0.004
ddd			0.05			0.002

12 Ordering information

Table 18. Ordering information scheme

Example: M45PE20 – V MP 6 T G

Device type

M45PE = serial flash memory for data storage

Device function

20 = 2-Mbit (256 Kbits ×8)

Operating voltage

V = V_{CC} = 2.7 V to 3.6 V

Package

MN = SO8 (150 mil width)

MP = VDFPN8 6 x 5 mm (MLP8)

Device grade

6 = Industrial temperature range, –40 to 85 °C.
Device tested with standard test flow

Option

blank = standard packing

T = tape and reel packing

Plating technology

P or G = ECOPACK® (RoHS compliant)

Note: For a list of available options (speed, package, etc.), for further information on any aspect of this device or when ordering parts operating at 75 MHz (0.11 µm technology, process digit '4'), please contact your nearest Numonyx sales office.

13 Revision history

Table 19. Document revision history

Date	Version	Changes
30-Apr-2003	1.0	Initial release.
04-Jun-2003	1.1	Description corrected of entering hardware protected mode ($\overline{W}$ must be driven, and cannot be left unconnected).
04-Dec-2003	1.2	V_{IO}(min) extended to –0.6 V, t_{PW}(typ) and t_{PP}(typ) improved. Table of contents, warning about exposed paddle on MLP8, and Pb-free options added. Change of naming for VDFPN8 package
21-Apr-2004	1.3	Soldering temperature information clarified for RoHS compliant devices. Device grade clarified.
22-Sep-2004	2	Document promoted to preliminary data. Minor wording changes. Device grade further clarified.
08-Oct-2004	3	Document promoted to full datasheet. No other changes.
4-Oct-2005	4	Added *Table 13: AC characteristics (33 MHz operation)*. *An easy way to modify data*, *A fast way to modify data*, *Page write (PW)* and *Page program (PP)* sections updated to explain optimal use of page write and page program instructions. Updated I_{CC3} values in *Table 11: DC characteristics*. Updated *Table 18*. ECOPACK® information added.
02-Feb-2007	5	Document reformatted. Small text changes. 50 MHz frequency added (*Table 14* added). *VCC supply voltage* and *VSS ground* descriptions added. *Figure 3: Bus master and memory devices on the SPI bus* modified and explanatory text added. V_{IO} max modified in *Table 7: Absolute maximum ratings*. At power-up, *The write in progress (WIP) bit is reset.* t_{SHQZ} end timing line modified in *Figure 22: Output timing*. Blank option removed below *Plating technology* in *Table 18: Ordering information scheme*. Small text changes. Package specifications updated (see *Section 11: Package mechanical*).
22-May-2008	6	Applied Numonyx branding. Removed ‘low voltage’ from the title. Updated the value for the maximum clock frequency (from 50 to 75 MHz) throughout the document. Added: *Table 15: AC characteristics (75 MHz operation, T9HX (0.11 µm) process)* and ECOPACK® text in *Section 11: Package mechanical*. Modified: *Table 11: DC characteristics*, *Figure 3: Bus master and memory devices on the SPI bus*, *Section 3: SPI modes*, and *Section 6.3: Read identification (RDID)*.

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