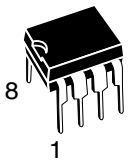
THE DATASHEET OF

M93C56-WMN6TP

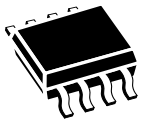
M93C86-x M93C76-x M93C66-x M93C56-x M93C46-x

16-Kbit, 8-Kbit, 4-Kbit, 2-Kbit and 1-Kbit (8-bit or 16-bit wide) MICROWIRE™ serial access EEPROM

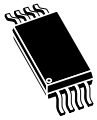
Datasheet - production data



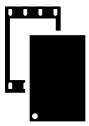
PDIP8 (BN)



SO8 (MN)



TSSOP8 (DW)
169 mil width



UFDFPN8 (MC)
2 x 3 mm

Features

- Industry standard MICROWIRE™ bus
- Single supply voltage:
  - 2.5 V to 5.5 V for M93Cx6-W
  - 1.8 V to 5.5 V for M93Cx6-R
- Dual organization: by word (x16) or byte (x8)
- Programming instructions that work on: byte, word or entire memory
- Self-timed programming cycle with auto-erase: 5 ms
- READY/$\overline{\text{BUSY}}$ signal during programming
- 2 MHz clock rate
- Sequential read operation
- Enhanced ESD/latch-up behavior
- More than 4 million write cycles
- More than 200-year data retention
- Packages
  - SO8, TSSOP8, UFDFPN8 packages: ECOPACK2®)
  - PDIP8 package: ECOPACK1®

Table 1. Device summary

Reference	Part number	Memory size	Supply voltage
M93C46-x	M93C46-W	1 Kbit	2.5 V to 5.5 V
	M93C46-R		1.8 V to 5.5 V
M93C56-x	M93C56-W	2 Kbit	2.5 V to 5.5 V
	M93C56-R		1.8 V to 5.5 V
M93C66-x	M93C66-W	4 Kbit	2.5 V to 5.5 V
	M93C66-R		1.8 V to 5.5 V
M93C76-x	M93C76-W	8 Kbit	2.5 V to 5.5 V
	M93C76-R		1.8 V to 5.5 V
M93C86-x	M93C86-W	16 Kbit	2.5 V to 5.5 V
	M93C86-R		1.8 V to 5.5 V

Contents

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1 Description

The M93C46 (1 Kbit), M93C56 (2 Kbit), M93C66 (4 Kbit), M93C76 (8 Kbit) and M93C86 (16 Kbit) are Electrically Erasable PROgrammable Memory (EEPROM) devices accessed through the MICROWIRE™ bus protocol. The memory array can be configured either in bytes (x8b) or in words (x16b).

The M93Cx6-W devices operate within a voltage supply range from 2.5 V to 5.5 V and the M93Cx6-R devices operate within a voltage supply range from 1.8 V to 5.5 V. All these devices operate with a clock frequency of 2 MHz (or less), over an ambient temperature range of - 40 °C / + 85 °C.

Table 2. Memory size versus organization

Device	Number of bits	Number of 8-bit bytes	Number of 16-bit words
M93C86	16384	2048	1024
M93C76	8192	1024	512
M93C66	4096	512	256
M93C56	2048	256	128
M93C46	1024	128	64

Figure 1. Logic diagram

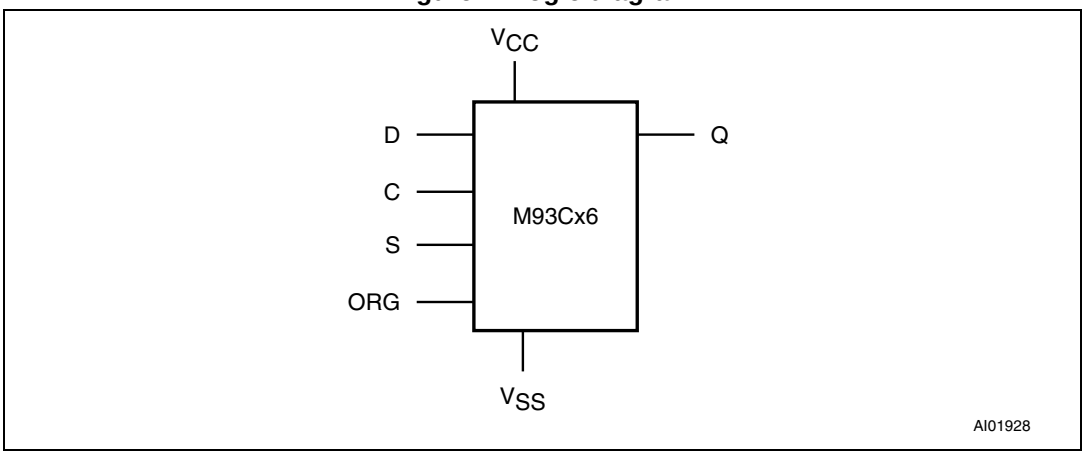
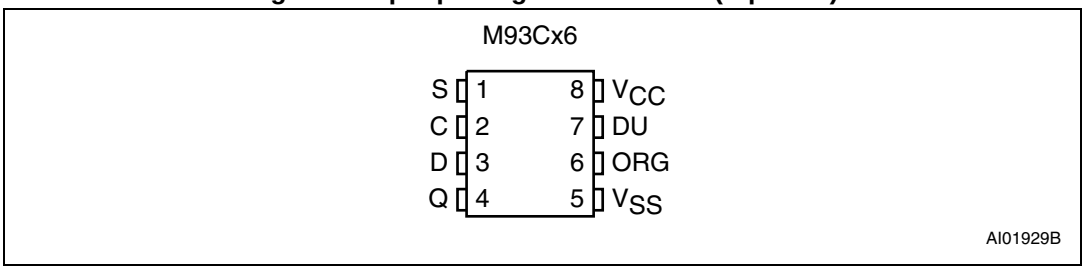


Table 3. Signal names

Signal name	Function	Direction
S	Chip Select	Input
D	Serial Data input	Input
Q	Serial Data output	Output
C	Serial Clock	Input
ORG	Organization Select	Input
V_{CC}	Supply voltage	-
V_{SS}	Ground	-

Figure 2. 8-pin package connections (top view)



1. See *Section 11: Package information* for package dimensions, and how to identify pin-1.
2. DU = Don't Use. The DU (do not use) pin does not contribute to the normal operation of the device. It is reserved for use by STMicroelectronics during test sequences. The pin may be left unconnected or may be connected to V_{CC} or V_{SS}.

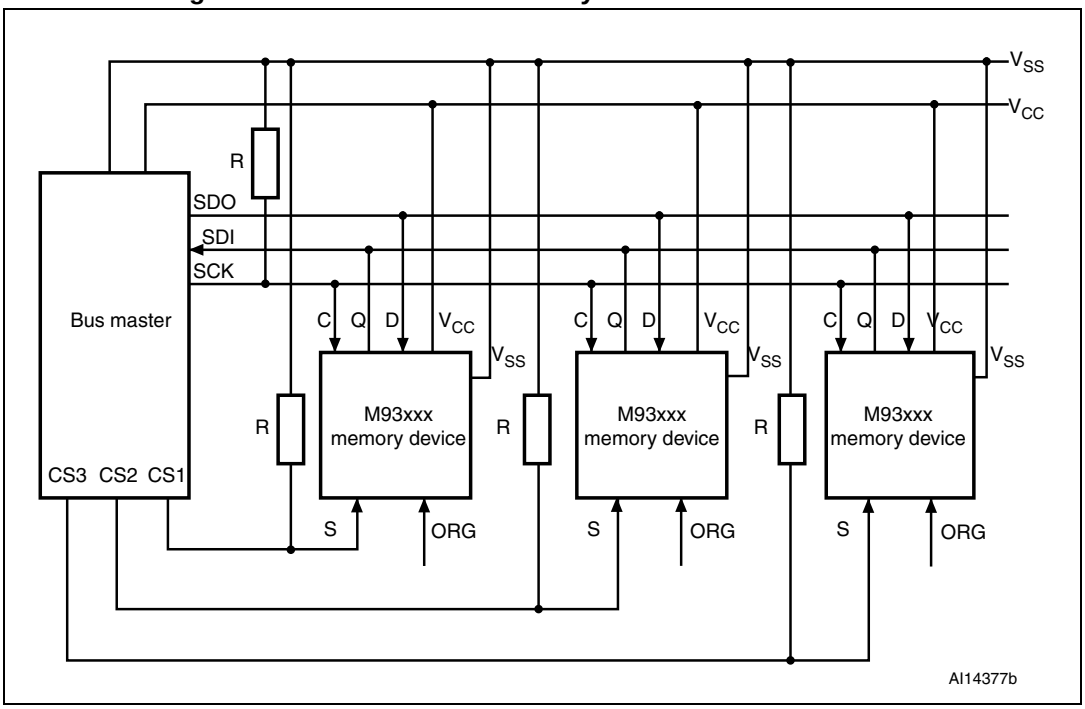
2 Connecting to the serial bus

Figure 3 shows an example of three memory devices connected to an MCU, on a serial bus. Only one device is selected at a time, so only one device drives the Serial Data output (Q) line at a time, the other devices are high impedance.

The pull-down resistor R (represented in *Figure 3*) ensures that no device is selected if the bus master leaves the S line in the high impedance state.

In applications where the bus master may be in a state where all inputs/outputs are high impedance at the same time (for example, if the bus master is reset during the transmission of an instruction), the clock line (C) must be connected to an external pull-down resistor so that, if all inputs/outputs become high impedance, the C line is pulled low (while the S line is pulled low): this ensures that C does not become high at the same time as S goes low, and so, that the t_{SLCH} requirement is met. The typical value of R is 100 kΩ

Figure 3. Bus master and memory devices on the serial bus



3 Operating features

3.1 Supply voltage (V_{CC})

3.1.1 Operating supply voltage (V_{CC})

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied. In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).

3.1.2 Power-up conditions

When the power supply is turned on, V_{CC} rises from V_{SS} to V_{CC}. During this time, the Chip Select (S) line is not allowed to float and should be driven to V_{SS}, it is therefore recommended to connect the S line to V_{SS} via a suitable pull-down resistor.

3.1.3 Power-up and device reset

In order to prevent inadvertent Write operations during power-up, a power on reset (POR) circuit is included. At power-up (continuous rise of V_{CC}), the device does not respond to any instruction until V_{CC} has reached the power on reset threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage defined in Operating conditions, in *Section 10: DC and AC parameters*).

When V_{CC} passes the POR threshold, the device is reset and is in the following state:

- Standby Power mode
- deselected (assuming that there is a pull-down resistor on the S line)

3.1.4 Power-down

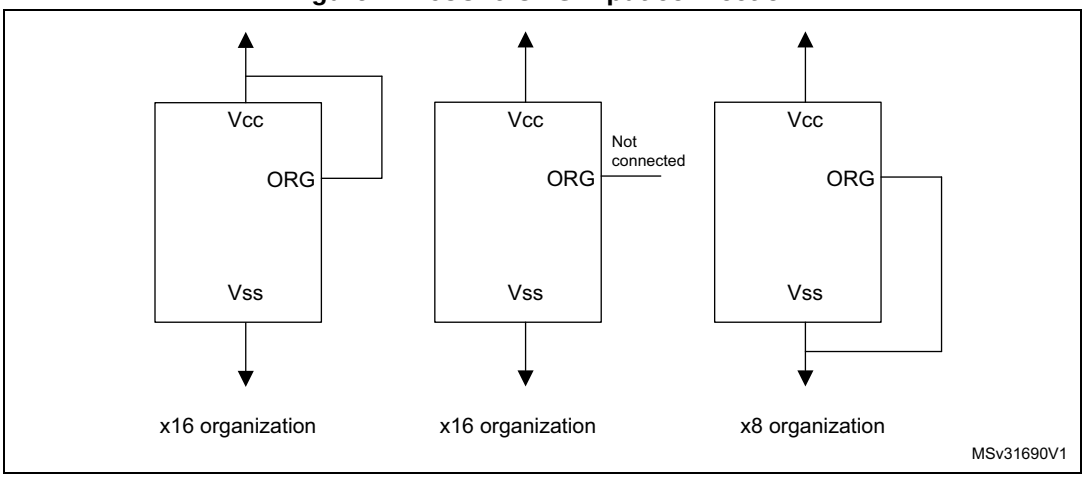
At power-down (continuous decrease in V_{CC}), as soon as V_{CC} drops from the normal operating voltage to below the power on reset threshold voltage, the device stops responding to any instruction sent to it.

During power-down, the device must be deselected and in the Standby Power mode (that is, there should be no internal Write cycle in progress).

4 Memory organization

The M93Cx6 memory is organized either as bytes (x8) or as words (x16). If Organization Select (ORG) is left unconnected (or connected to V_{CC}) the x16 organization is selected; when Organization Select (ORG) is connected to Ground (V_{SS}) the x8 organization is selected. When the M93Cx6 is in Standby mode, Organization Select (ORG) should be set either to V_{SS} or V_{CC} to reach the device minimum power consumption (as any voltage between V_{SS} and V_{CC} applied to ORG input may increase the device Standby current).

Figure 4. M93Cx6 ORG input connection



5 Instructions

The instruction set of the M93Cx6 devices contains seven instructions, as summarized in *Table 4* to *Table 6*. Each instruction consists of the following parts, as shown in *Figure 5: READ, WRITE, WEN, WDS sequences*:

- Each instruction is preceded by a rising edge on Chip Select Input (S) with Serial Clock (C) being held low.
- A start bit, which is the first '1' read on Serial Data Input (D) during the rising edge of Serial Clock (C).
- Two op-code bits, read on Serial Data Input (D) during the rising edge of Serial Clock (C). (Some instructions also use the first two bits of the address to define the op-code).
- The address bits of the byte or word that is to be accessed. For the M93C46, the address is made up of 6 bits for the x16 organization or 7 bits for the x8 organization (see *Table 4*). For the M93C56 and M93C66, the address is made up of 8 bits for the x16 organization or 9 bits for the x8 organization (see *Table 5*). For the M93C76 and M93C86, the address is made up of 10 bits for the x16 organization or 11 bits for the x8 organization (see *Table 6*).

The M93Cx6 devices are fabricated in CMOS technology and are therefore able to run as slow as 0 Hz (static input signals) or as fast as the maximum ratings specified in "AC characteristics" tables, in *Section 10: DC and AC parameters*.

Table 4. Instruction set for the M93C46

Instruction	Description	Start bit	Op-code	x8 origination (ORG = 0)			x16 origination (ORG = 1)		
				Address (1)	Data	Required clock cycles	Address (1)	Data	Required clock cycles
READ	Read Data from Memory	1	10	A6-A0	Q7-Q0	-	A5-A0	Q15-Q0	-
WRITE	Write Data to Memory	1	01	A6-A0	D7-D0	18	A5-A0	D15-D0	25
WEN	Write Enable	1	00	11X XXXX	-	10	11 XXXX	-	9
WDS	Write Disable	1	00	00X XXXX	-	10	00 XXXX	-	9
ERASE	Erase Byte or Word	1	11	A6-A0	-	10	A5-A0	-	9
ERAL	Erase All Memory	1	00	10X XXXX	-	10	10 XXXX	-	9
WRAL	Write All Memory with same Data	1	00	01X XXXX	D7-D0	18	01 XXXX	D15-D0	25

1. X = Don't Care bit.

Table 5. Instruction set for the M93C56 and M93C66

Instruction	Description	Start bit	Op-code	x8 origination (ORG = 0)			x16 origination (ORG = 1)		
				Address (1) (2)	Data	Required clock cycles	Address (1) (3)	Data	Required clock cycles
READ	Read Data from Memory	1	10	A8-A0	Q7-Q0	-	A7-A0	Q15-Q0	-
WRITE	Write Data to Memory	1	01	A8-A0	D7-D0	20	A7-A0	D15-D0	27
WEN	Write Enable	1	00	1 1XXX XXXX	-	12	11XX XXXX	-	11
WDS	Write Disable	1	00	0 0XXX XXXX	-	12	00XX XXXX	-	11
ERASE	Erase Byte or Word	1	11	A8-A0	-	12	A7-A0	-	11
ERAL	Erase All Memory	1	00	1 0XXX XXXX	-	12	10XX XXXX	-	11
WRAL	Write All Memory with same Data	1	00	0 1XXX XXXX	D7-D0	20	01XX XXXX	D15-D0	27

1. X = Don't Care bit.
2. Address bit A8 is not decoded by the M93C56.
3. Address bit A7 is not decoded by the M93C56.

Table 6. Instruction set for the M93C76 and M93C86

Instruction	Description	Start bit	Op-code	x8 Origination (ORG = 0)			x16 Origination (ORG = 1)		
				Address (1)(2)	Data	Required clock cycles	Address (1) (3)	Data	Required clock cycles
READ	Read Data from Memory	1	10	A10-A0	Q7-Q0	-	A9-A0	Q15-Q0	-
WRITE	Write Data to Memory	1	01	A10-A0	D7-D0	22	A9-A0	D15-D0	29
WEN	Write Enable	1	00	11X XXXX XXXX	-	14	11 XXXX XXXX	-	13
WDS	Write Disable	1	00	00X XXXX XXXX	-	14	00 XXXX XXXX	-	13
ERASE	Erase Byte or Word	1	11	A10-A0	-	14	A9-A0	-	13
ERAL	Erase All Memory	1	00	10X XXXX XXXX	-	14	10 XXXX XXXX	-	13
WRAL	Write All Memory with same Data	1	00	01X XXXX XXXX	D7-D0	22	01 XXXX XXXX	D15-D0	29

1. X = Don't Care bit.
2. Address bit A10 is not decoded by the M93C76.
3. Address bit A9 is not decoded by the M93C76.

5.1 Read Data from Memory

The Read Data from Memory (READ) instruction outputs data on Serial Data Output (Q). When the instruction is received, the op-code and address are decoded, and the data from the memory is transferred to an output shift register. A dummy 0 bit is output first, followed by the 8-bit byte or 16-bit word, with the most significant bit first. Output data changes are triggered by the rising edge of Serial Clock (C). The M93Cx6 automatically increments the internal address register and clocks out the next byte (or word) as long as the Chip Select Input (S) is held High. In this case, the dummy 0 bit is *not* output between bytes (or words) and a continuous stream of data can be read (the address counter automatically rolls over to 00h when the highest address is reached).

5.2 Erase and Write data

5.2.1 Write Enable and Write Disable

The Write Enable (WEN) instruction enables the future execution of erase or write instructions, and the Write Disable (WDS) instruction disables it. When power is first applied, the M93Cx6 initializes itself so that erase and write instructions are disabled. After a Write Enable (WEN) instruction has been executed, erasing and writing remains enabled until a Write Disable (WDS) instruction is executed, or until V_{CC} falls below the power-on reset threshold voltage. To protect the memory contents from accidental corruption, it is advisable to issue the Write Disable (WDS) instruction after every write cycle. The Read Data from Memory (READ) instruction is not affected by the Write Enable (WEN) or Write Disable (WDS) instructions.

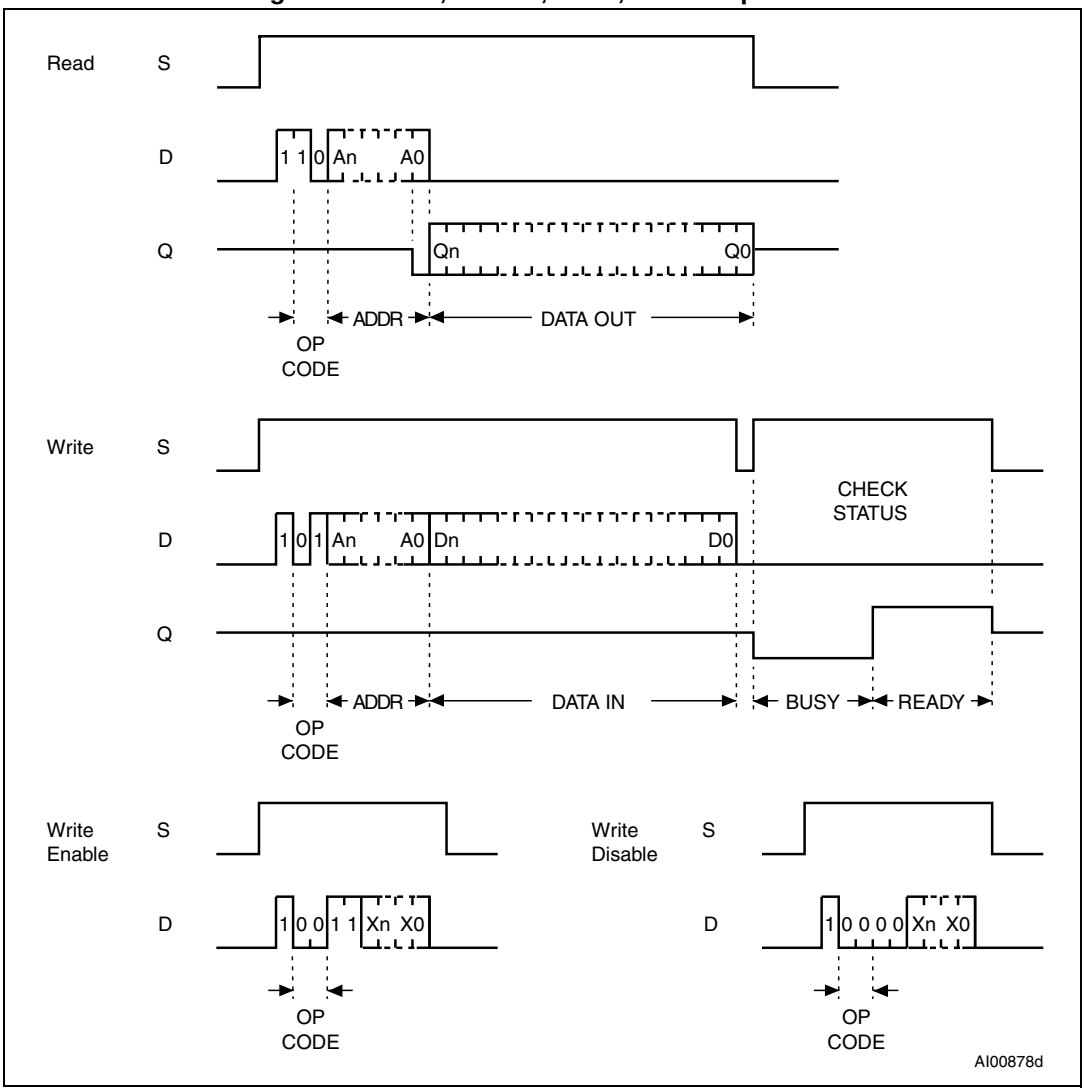
5.2.2 Write

For the Write Data to Memory (WRITE) instruction, 8 or 16 data bits follow the op-code and address bits. These form the byte or word that is to be written. As with the other bits, Serial Data Input (D) is sampled on the rising edge of Serial Clock (C).

After the last data bit has been sampled, the Chip Select Input (S) must be taken low before the next rising edge of Serial Clock (C). If Chip Select Input (S) is brought low before or after this specific time frame, the self-timed programming cycle will not be started, and the addressed location will not be programmed. The completion of the cycle can be detected by monitoring the READY/BUSY line, as described later in this document.

Once the Write cycle has been started, it is internally self-timed (the external clock signal on Serial Clock (C) may be stopped or left running after the start of a Write cycle). The Write cycle is automatically preceded by an Erase cycle, so it is unnecessary to execute an explicit erase instruction before a Write Data to Memory (WRITE) instruction.

Figure 5. READ, WRITE, WEN, WDS sequences

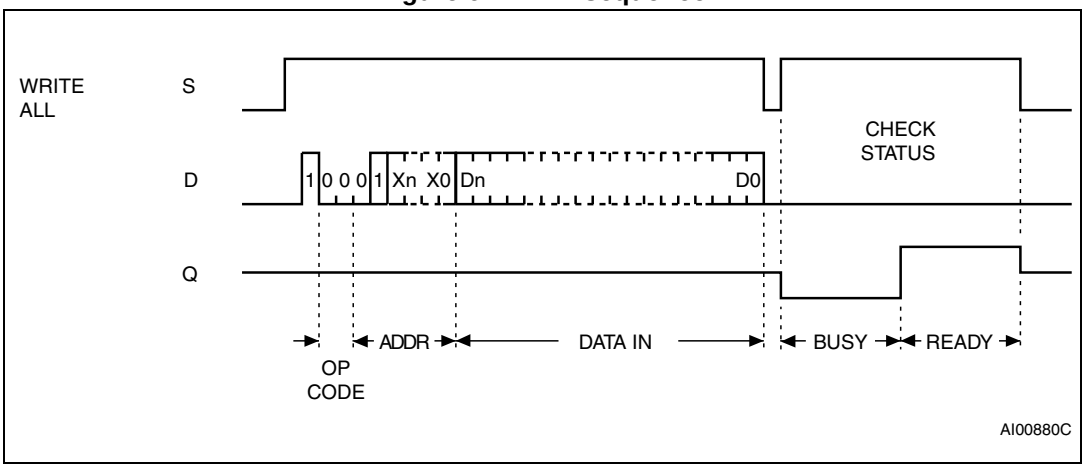


1. For the meanings of An, Xn, Qn and Dn, see *Table 4*, *Table 5* and *Table 6*.

5.2.3 Write All

As with the Erase All Memory (ERAL) instruction, the format of the Write All Memory with same Data (WRAL) instruction requires that a dummy address be provided. As with the Write Data to Memory (WRITE) instruction, the format of the Write All Memory with same Data (WRAL) instruction requires that an 8-bit data byte, or 16-bit data word, be provided. This value is written to all the addresses of the memory device. The completion of the cycle can be detected by monitoring the READY/BUSY line, as described next.

Figure 6. WRAL sequence

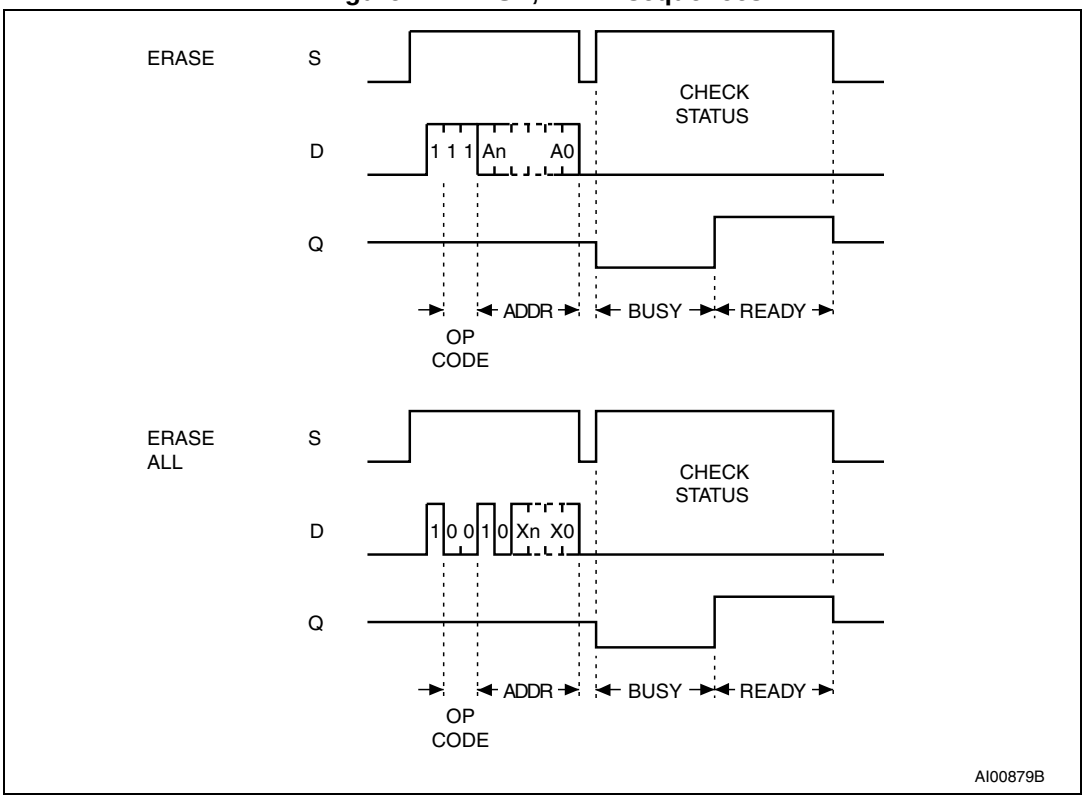


1. For the meanings of Xn and Dn, please see *Table 4*, *Table 5* and *Table 6*.

5.2.4 Erase Byte or Word

The Erase Byte or Word (ERASE) instruction sets the bits of the addressed memory byte (or word) to 1. Once the address has been correctly decoded, the falling edge of the Chip Select Input (S) starts the self-timed Erase cycle. The completion of the cycle can be detected by monitoring the READY/BUSY line, as described in *Section 6: READY/BUSY status*.

Figure 7. ERASE, ERAL sequences



1. For the meanings of An and Xn, please see *Table 4*, *Table 5* and *Table 6*.

5.2.5 Erase All

The Erase All Memory (ERAL) instruction erases the whole memory (all memory bits are set to 1). The format of the instruction requires that a dummy address be provided. The Erase cycle is conducted in the same way as the Erase instruction (ERASE). The completion of the cycle can be detected by monitoring the READY/BUSY line, as described in *Section 6: READY/BUSY status*.

6 READY/$\overline{\text{BUSY}}$ status

While the Write or Erase cycle is underway, for a WRITE, ERASE, WRAL or ERAL instruction, the Busy signal (Q=0) is returned whenever Chip Select input (S) is driven high. (Please note, though, that there is an initial delay, of t_{SLSH}, before this status information becomes available). In this state, the M93Cx6 ignores any data on the bus. When the Write cycle is completed, and Chip Select Input (S) is driven high, the Ready signal (Q=1) indicates that the M93Cx6 is ready to receive the next instruction. Serial Data Output (Q) remains set to 1 until the Chip Select Input (S) is brought low or until a new start bit is decoded.

7 Initial delivery state

The device is delivered with all bits in the memory array set to 1 (each byte contains FFh).

8 Clock pulse counter

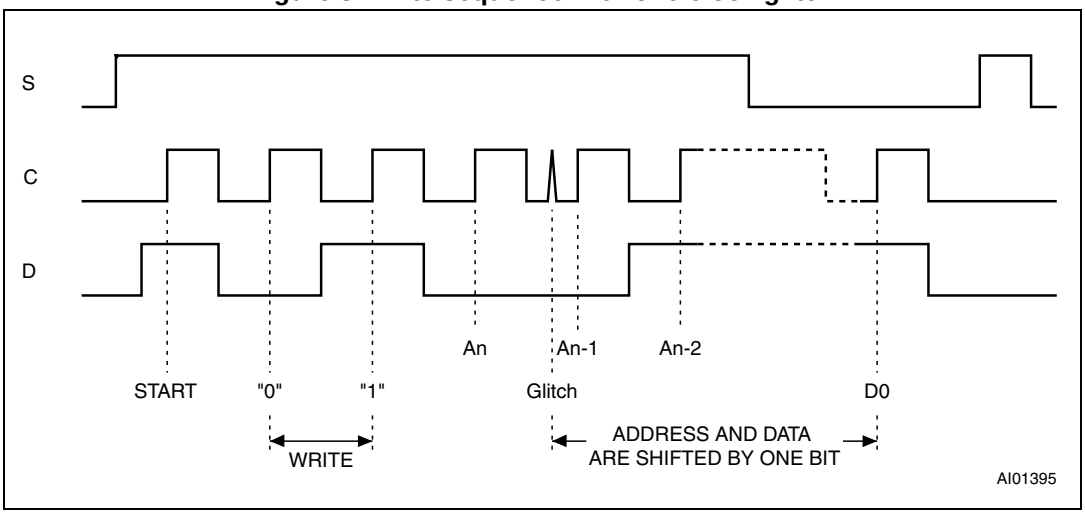
In a noisy environment, the number of pulses received on Serial Clock (C) may be greater than the number delivered by the master (the microcontroller). This can lead to a misalignment of the instruction of one or more bits (as shown in *Figure 8*) and may lead to the writing of erroneous data at an erroneous address.

To avoid this problem, the M93Cx6 has an on-chip counter that counts the clock pulses from the start bit until the falling edge of the Chip Select Input (S). If the number of clock pulses received is not the number expected, the WRITE, ERASE, ERAL or WRAL instruction is aborted, and the contents of the memory are not modified.

The number of clock cycles expected for each instruction, and for each member of the M93Cx6 family, are summarized in *Table 4: Instruction set for the M93C46* to *Table 6: Instruction set for the M93C76 and M93C86*. For example, a Write Data to Memory (WRITE) instruction on the M93C56 (or M93C66) expects 20 clock cycles (for the x8 organization) from the start bit to the falling edge of Chip Select Input (S). That is:

1 Start bit
+ 2 Op-code bits
+ 9 Address bits
+ 8 Data bits

Figure 8. Write sequence with one clock glitch



9 Maximum ratings

Stressing the device outside the ratings listed in the Absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute maximum ratings

Symbol	Parameter		Min.	Max.	Unit
	Ambient operating temperature		–40	130	°C
T_{STG}	Storage temperature		–65	150	°C
T_{LEAD}	Lead temperature during soldering	PDIP	-	260(1)	°C
		other packages	See note (2)		
V_{OUT}	Output range (Q = V_{OH} or Hi-Z)		–0.50	V_{CC}+0.5	V
V_{IN}	Input range		–0.50	V_{CC}+1	V
V_{CC}	Supply voltage		–0.50	6.5	V
V_{ESD}	Electrostatic discharge voltage (human body model)(3)		-	4000	V

1. T_{LEAD} max must *not* be applied for more than 10 s.
2. Compliant with JEDEC standard J-STD-020D (for small-body, Sn-Pb or Pb free assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS directive 2011/65/EU of July 2011).
3. Positive and negative pulses applied on pin pairs, according to the AEC-Q100-002 (compliant with ANSI/ESDA/JEDEC JS-001-2012), C1 = 100 pF, R1 = 1500 Ω, R2 = 500 Ω).

10 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.

Table 8. Operating conditions (M93Cx6-W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 9. Operating conditions (M93Cx6-R)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 10. Cycling performance(1)

Symbol	Parameter	Test conditions	Min.	Max.	Unit
Ncycle	Write cycle endurance	TA ≤ 25 °C, $V_{CC}(min) < V_{CC} < V_{CC}(max)$	-	4,000,000	Write cycle
		TA = 85 °C, $V_{CC}(min) < V_{CC} < V_{CC}(max)$	-	1,200,000	

1. Cycling performance for products identified by process letter K.

Table 11. Memory cell data retention(1)

Parameter	Test conditions	Min.	Unit
Data retention	TA = 55 °C	200	Year

1. For products identified by process letter K. The data retention behavior is checked in production, while the 200-year limit is defined from characterization and qualification results.

Table 12. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	100		pF
-	Input rise and fall times	-	50	ns
-	Input voltage levels	0.2 V_{CC} to 0.8 V_{CC}		V
-	Input timing reference voltages	0.3 V_{CC} to 0.7 V_{CC}		V
-	Output timing reference voltages	0.3 V_{CC} to 0.7 V_{CC}		V

Figure 9. AC testing input output waveforms

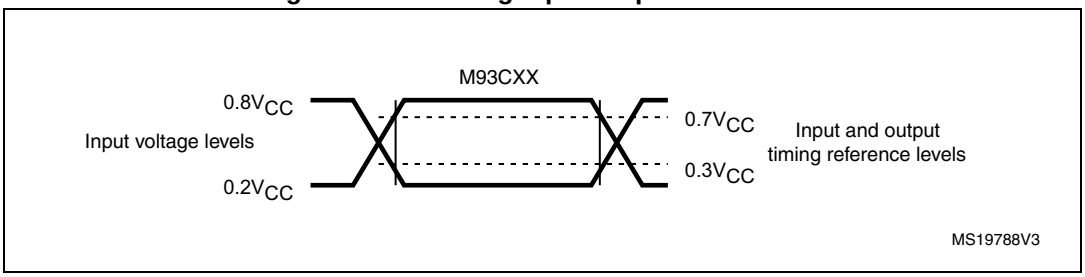


Table 13. Input and output capacitance

Symbol	Parameter	Test condition(1)	Min	Max	Unit
C_{OUT}	Output capacitance	V_{OUT} = 0V	-	8	pF
C_{IN}	Input capacitance	V_{IN} = 0V	-	6	pF

1. Sampled only, not 100% tested, at T_A = 25 °C and a frequency of 1 MHz.

Table 14. DC characteristics (M93Cx6-W, device grade 6)

Symbol	Parameter	Test condition (in addition to the conditions defined in *Table 8* and *Table 12*)	Min.	Max.	Unit
I_{LI}	Input leakage current	$0V \le V_{IN} \le V_{CC}$	-	±2.5	µA
I_{LO}	Output leakage current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z	-	±2.5	µA
I_{CC}	Operating supply current	V_{CC} = 5 V, S = V_{IH}, f = 2 MHz, Q = open	-	2	mA
		V_{CC} = 2.5 V, S = V_{IH}, f = 2 MHz, Q = open	-	1	mA
I_{CC1}	Standby supply current	V_{CC} = 2.5 V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}, pin7 = V_{CC}, V_{SS} or Hi-Z	-	2(1)	µA
		V_{CC} = 5.5 V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}, pin7 = VCC, V_{SS} or Hi-Z	-	3(2)	µA
V_{IL}	Input low voltage (D, C, S)	-	–0.45	0.2 V_{CC}	V
V_{IH}	Input high voltage (D, C, S)	-	0.7 V_{CC}	V_{CC} + 1	V
V_{OL}	Output low voltage (Q)	V_{CC} = 5 V, I_{OL} = 2.1 mA	-	0.4	V
		V_{CC} = 2.5 V, I_{OL} = 100 µA	-	0.2	V
V_{OH}	Output high voltage (Q)	V_{CC} = 5 V, I_{OH} = – 400 µA	0.8 V_{CC}	-	V
		V_{CC} = 2.5 V, I_{OH} = – 100 µA	V_{CC}–0.2	-	V

1. 5 µA for previous devices identified with the process letter G.
2. Tested only for current devices identified with the process letter K.

Table 15. DC characteristics (M93Cx6-R)

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{LI}	Input leakage current	$0V \le V_{IN} \le V_{CC}$	-	±2.5	µA
I_{LO}	Output leakage current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z	-	±2.5	µA
I_{CC}	Operating supply current	V_{CC} = 5 V, S = V_{IH}, f = 2 MHz, Q = open	-	2	mA
		V_{CC} = 1.8 V, S = V_{IH}, f = 1 MHz, Q = open	-	1	mA
I_{CC1}	Standby supply current	V_{CC} = 1.8 V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}, pin7 = V_{CC}, V_{SS} or Hi-Z	-	1(1)	µA
V_{IL}	Input low voltage (D, C, S)	-	–0.45	0.2 V_{CC}	V
V_{IH}	Input high voltage (D, C, S)	-	0.8 V_{CC}	V_{CC} + 1	V
V_{OL}	Output low voltage (Q)	V_{CC} = 1.8 V, I_{OL} = 100 µA	-	0.2	V
V_{OH}	Output high voltage (Q)	V_{CC} = 1.8 V, I_{OH} = –100 µA	V_{CC}–0.2	-	V

1. 2 µA for previous devices identified with process letter G.

Table 16. AC characteristics (M93Cx6-W, M93Cx6-R(1), device grade 6)

Test conditions specified in *Table 8* and *Table 12*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SK}	Clock frequency	D.C.	2	MHz
t_{SLCH}		Chip Select low to Clock high	50	-	ns
t_{SHCH}	t_{CSS}	Chip Select setup time	50	-	ns
t_{SLSH}(2)	t_{CS}	Chip Select low to Chip Select high	200	-	ns
t_{CHCL}(3)	t_{SKH}	Clock high time	200	-	ns
t_{CLCH}(3)	t_{SKL}	Clock low time	200	-	ns
t_{DVCH}	t_{DIS}	Data in setup time	50	-	ns
t_{CHDX}	t_{DIH}	Data in hold time	50	-	ns
t_{CLSH}	t_{SKS}	Clock setup time (relative to S)	50	-	ns
t_{CLSL}	t_{CSH}	Chip Select hold time	0	-	ns
t_{SHQV}	t_{SV}	Chip Select to READY/$\overline{\text{BUSY}}$ status	-	200	ns
t_{SLQZ}	t_{DF}	Chip Select low to output Hi-Z	-	100	ns
t_{CHQL}	t_{PD0}	Delay to output low	-	200	ns
t_{CHQV}	t_{PD1}	Delay to output valid	-	200	ns
t_W	t_{WP}	Erase or Write cycle time	-	5	ms

1. All M93Cx6-R devices operate with a clock frequency of 1MHz, as defined in *Table 17*. Only the new M93Cx6-R devices (identified with the process letter K) can operate with the 2 MHz timing values defined in this table.
2. Chip Select Input (S) must be brought low for a minimum of t_{SLSH} between consecutive instruction cycles.
3. $t_{CHCL} + t_{CLCH} \ge 1 / f_C$.

Table 17. AC characteristics (M93Cx6-R)(1)

Test conditions specified in *Table 9* and *Table 12*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SK}	Clock frequency	D.C.	1	MHz
t_{SLCH}		Chip Select low to Clock high	250	-	ns
t_{SHCH}	t_{CSS}	Chip Select setup time	50	-	ns
t_{SLSH}(2)	t_{CS}	Chip Select low to Chip Select high	250	-	ns
t_{CHCL}(3)	t_{SKH}	Clock high time	250	-	ns
t_{CLCH}(3)	t_{SKL}	Clock low time	250	-	ns
t_{DVCH}	t_{DIS}	Data in setup time	100	-	ns
t_{CHDX}	t_{DIH}	Data in hold time	100	-	ns
t_{CLSH}	t_{SKS}	Clock setup time (relative to S)	100	-	ns
t_{CLSL}	t_{CSH}	Chip Select hold time	0	-	ns
t_{SHQV}	t_{SV}	Chip Select to READY/$\overline{\text{BUSY}}$ status	-	400	ns
t_{SLQZ}	t_{DF}	Chip Select low to output Hi-Z	-	200	ns
t_{CHQL}	t_{PD0}	Delay to output low	-	400	ns
t_{CHQV}	t_{PD1}	Delay to output valid	-	400	ns
t_W	t_{WP}	Erase or Write cycle time	-	10	ms

1. The new M93Cx6-R devices identified with the process letter K can operate with a clock frequency of 2 MHz and an Erase (or Write) cycle of 5 ms, as shown in *Table 16*.
2. Chip Select Input (S) must be brought low for a minimum of t_{SLSH} between consecutive instruction cycles.
3. $t_{CHCL} + t_{CLCH} \geq 1 / f_C$.

Figure 10. Synchronous timing (Start and op-code input)

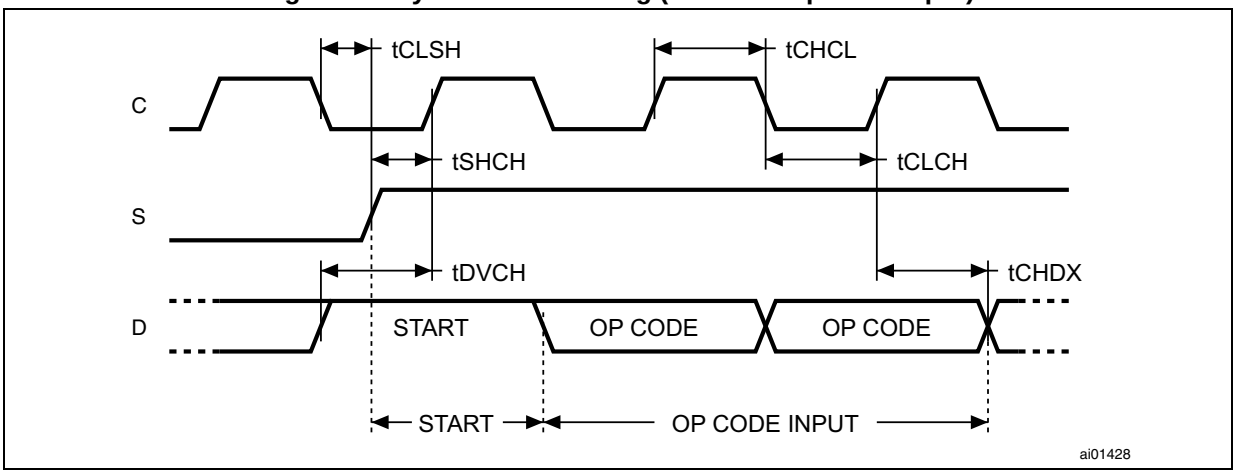


Figure 11. Synchronous timing (Read)

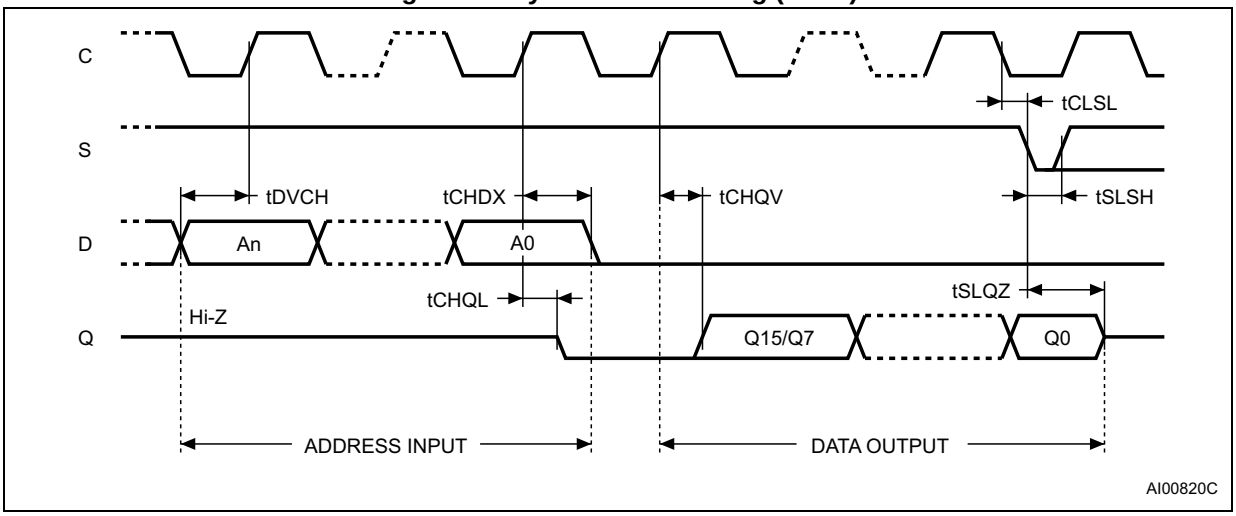
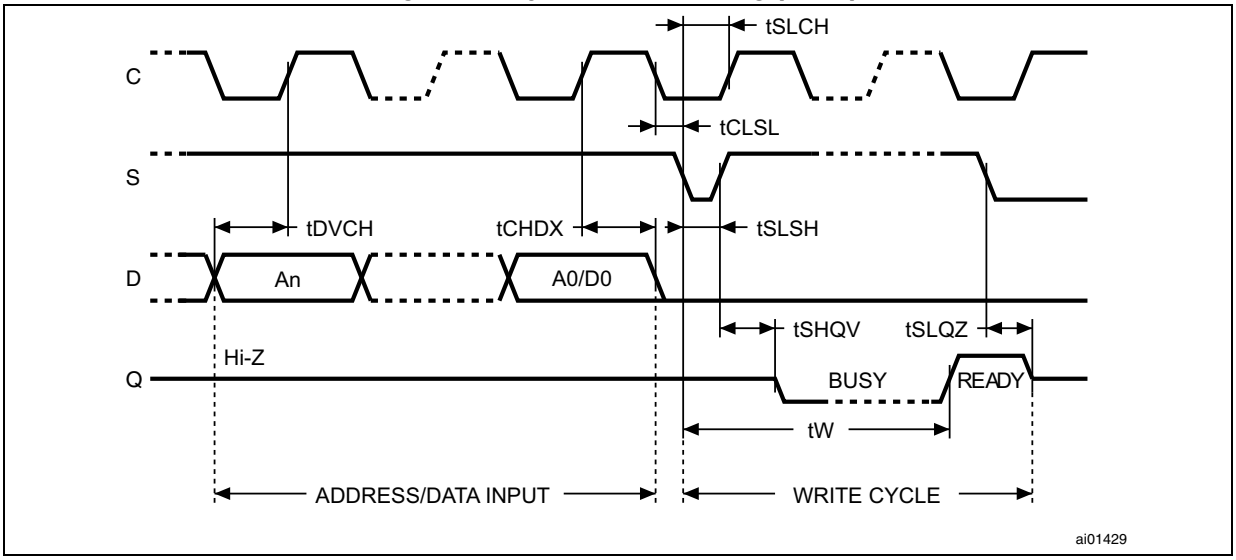


Figure 12. Synchronous timing (Write)

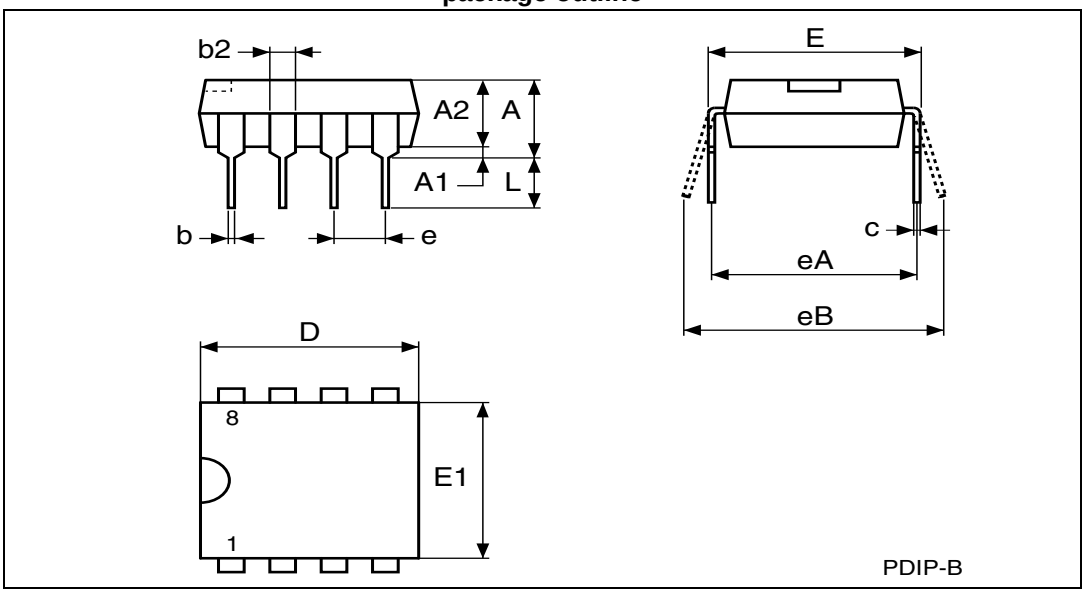


11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

11.1 PDIP8 package information

Figure 13. PDIP8 – 8 lead plastic dual in-line package, 300 mils body width, package outline



1. Drawing is not to scale.

Table 18. PDIP8 – 8 lead plastic dual in-line package, 300 mils body width, package mechanical data

Symbol	millimeters			inches(1)		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	-	-	5.33	-	-	0.2098
A1	-	0.38	-	-	0.015	-
A2	3.3	2.92	4.95	0.1299	0.115	0.1949
b	0.46	0.36	0.56	0.0181	0.0142	0.022
b2	1.52	1.14	1.78	0.0598	0.0449	0.0701
c	0.25	0.2	0.36	0.0098	0.0079	0.0142
D	9.27	9.02	10.16	0.365	0.3551	0.4
E	7.87	7.62	8.26	0.3098	0.3	0.3252
E1	6.35	6.1	7.11	0.25	0.2402	0.2799

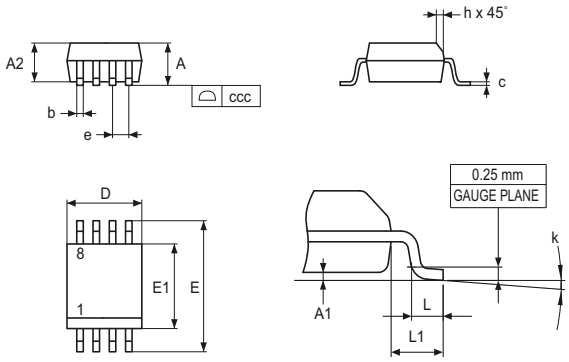
Table 18. PDIP8 – 8 lead plastic dual in-line package, 300 mils body width, package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Typ.	Min.	Max.	Typ.	Min.	Max.
e	2.54	-	-	0.1	-	-
eA	7.62	-	-	0.3	-	-
eB	-	-	10.92	-	-	0.4299
L	3.3	2.92	3.81	0.1299	0.115	0.15

1. Values in inches are converted from mm and rounded to 4 decimal digits.

11.2 SO8N package information

Figure 14. SO8N – 8-lead plastic small outline, 150 mils body width, package outline



1. Drawing is not to scale.

Table 19. SO8N – 8-lead plastic small outline, 150 mils body width, package mechanical data

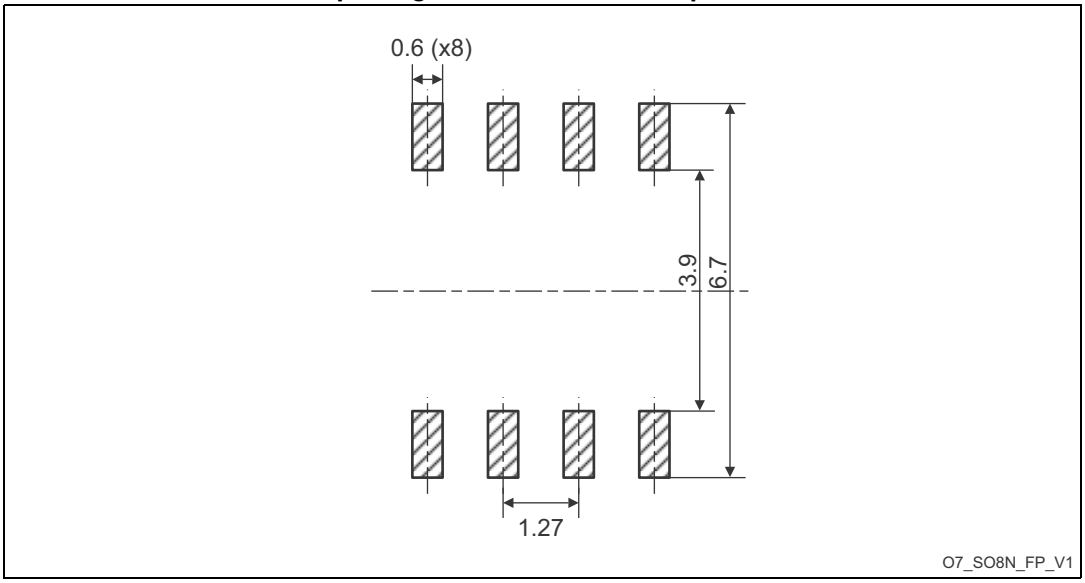
Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.750	-	-	0.0689
A1	0.100	-	0.250	0.0039	-	0.0098
A2	1.250	-	-	0.0492	-	-
b	0.280	-	0.480	0.0110	-	0.0189
c	0.170	-	0.230	0.0067	-	0.0091
D	4.800	4.900	5.000	0.1890	0.1929	0.1969
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1	3.800	3.900	4.000	0.1496	0.1535	0.1575
e	-	1.270	-	-	0.0500	-
h	0.250	-	0.500	0.0098	-	0.0197

Table 19. SO8N – 8-lead plastic small outline, 150 mils body width, package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
k	0°	-	8°	0°	-	8°
L	0.400	-	1.270	0.0157	-	0.0500
L1	-	1.040	-	-	0.0409	-
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.

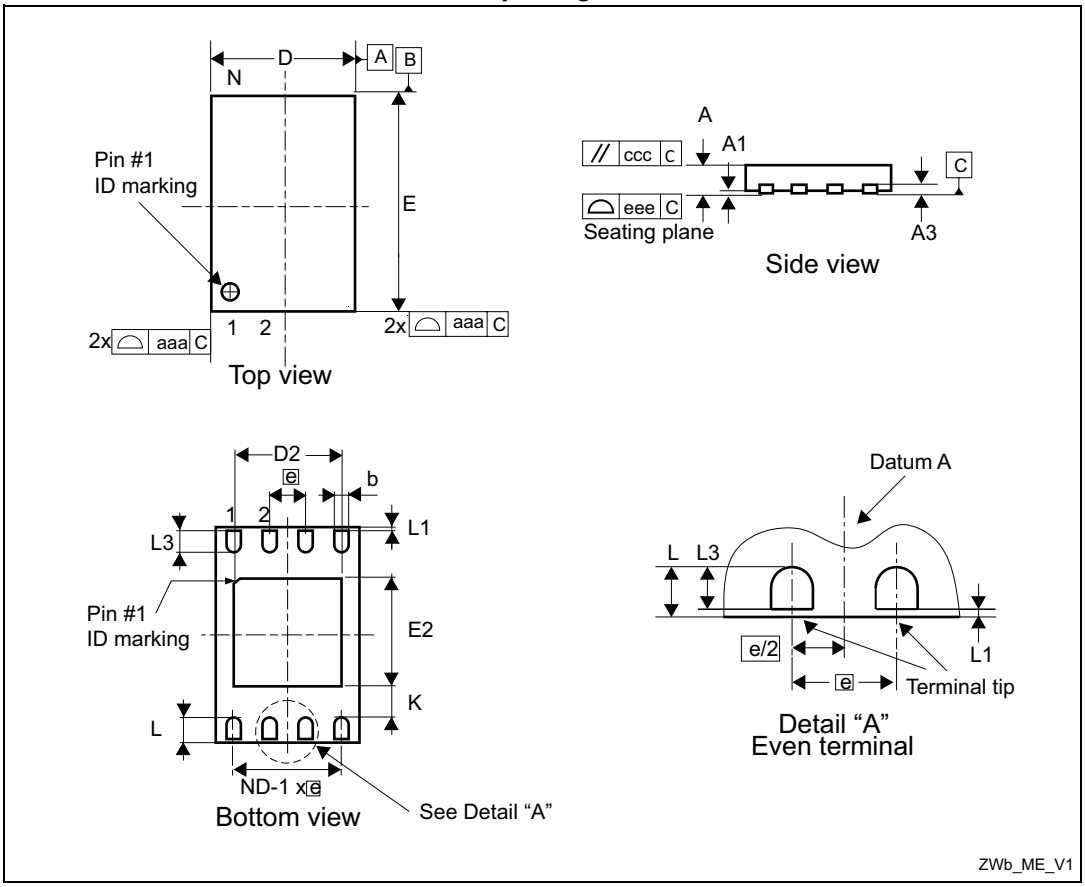
Figure 15. SO8N – 8-lead plastic small outline, 150 mils body width, package recommended footprint



1. Dimensions are expressed in millimeters.

11.3 UFDFN8 package information

Figure 16. UFDFN8 - 8-lead, 2 × 3 mm, 0.5 mm pitch ultra thin profile fine pitch dual flat package outline



1. Max. package warpage is 0.05 mm.
2. Exposed copper is not systematic and can appear partially or totally according to the cross section.
3. Drawing is not to scale.
4. The central pad (the area E2 by D2 in the above illustration) must be either connected to V_{SS} or left floating (not connected) in the end application.

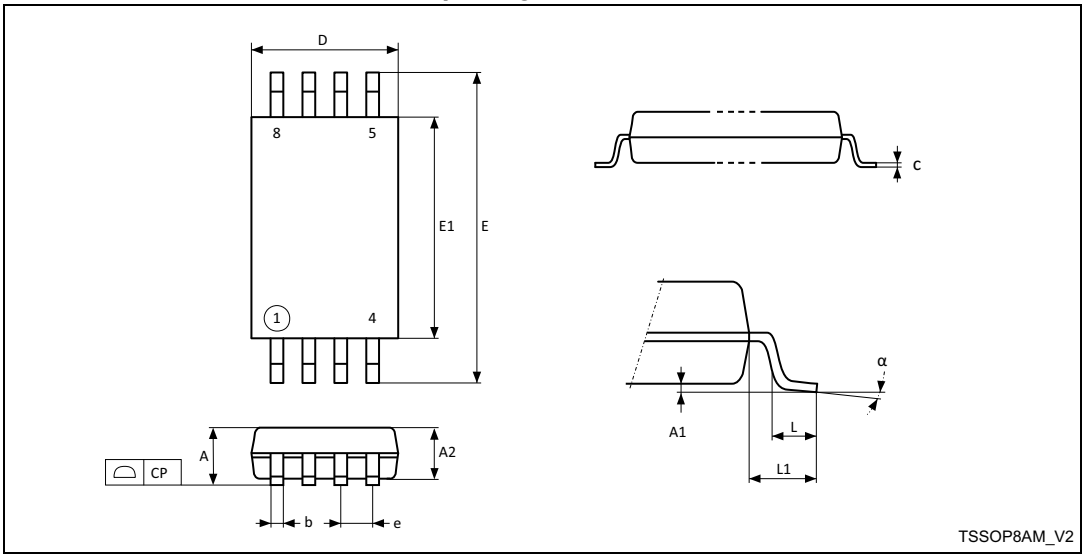
Table 20. UFDFN8 - 8-lead, 2 × 3 mm, 0.5 mm pitch ultra thin profile fine pitch dual flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.450	0.550	0.600	0.0177	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
b[2]	0.200	0.250	0.300	0.0079	0.0098	0.0118
D	1.900	2.000	2.100	0.0748	0.0787	0.0827
D2	1.200	-	1.600	0.0472	-	0.0630
E	2.900	3.000	3.100	0.1142	0.1181	0.1220
E2	1.200	-	1.600	0.0472	-	0.0630
e	-	0.500	-	0.0197		
K	0.300	-	-	0.0118	-	-
L	0.300	-	0.500	0.0118	-	0.0197
L1	-	-	0.150	-	-	0.0059
L3	0.300	-	-	0.0118	-	-
aaa	-	-	0.150	-	-	0.0059
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee[3]	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension b applies to plated terminal and is measured between 0.15 and 0.30 mm from the terminal tip.
3. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.

11.4 TSSOP8 package information

Figure 17.TSSOP8 – 8-lead thin shrink small outline, 3 x 4.4 mm, 0.5 mm pitch, package outline



1. Drawing is not to scale.

Table 21. TSSOP8 – 8-lead thin shrink small outline, 3 x 4.4 mm, 0.5 mm pitch, package mechanical data

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
CP	-	-	0.100	-	-	0.0039
D	2.900	3.000	3.100	0.1142	0.1181	0.1220
e	-	0.650	-	-	0.0256	-
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1	4.300	4.400	4.500	0.1693	0.1732	0.1772
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
α	0°	-	8°	0°	-	8°

1. Values in inches are converted from mm and rounded to four decimal digits.

12 Part numbering

Table 22. Ordering information scheme

Example: M93C86 – W MN 6 T P

Device type

M93 = MICROWIRE™ serial EEPROM

Device function

86 = 16 Kbit (2048 x 8)

76 = 8 Kbit (1024 x 8)

66 = 4 Kbit (512 x 8)

56 = 2 Kbit (256 x 8)

46 = 1 Kbit (128 x 8)

Operating voltage

W = V_{CC} = 2.5 to 5.5 V

R = V_{CC} = 1.8 to 5.5 V

Package

BN = PDIP8(1)

MN = SO8 (150 mils width)(2)

MC = UFDFPN8 2 x 3 mm (MLP8)(2)

DW = TSSOP8 (169 mils width)(2)

Device grade

6 = Industrial temperature range, –40 to 85 °C.
Device tested with standard test flow

Packing

blank = tube packing

T = tape and reel packing

Plating technology

P or G = ECOPACK2®

1. ECOPACK1®: RoHS-compliant.
2. ECOPACK2®: RoHS compliant and free of brominated, chlorinated and antimony-oxide flame retardants.

Engineering samples

Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

13 Revision history

Table 23. Document revision history

Date	Revision	Changes
01-Apr-2010	9	Modified footnote in *Table 14* and *Table 15 on page 23* Updated *Figure 14: UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, outline* and *Table 22: UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, data*
29-Apr-2010	10	Updated *Figure 31: Available M93C66-x products (package, voltage range, temperature grade)* UFDFPN option.
12-Apr-2011	11	Updated *Table 7: Absolute maximum ratings*, MLP8 package data in *Section 12: Package mechanical data* and process data in *Section 9: Clock pulse counter*. Deleted *Table 29: Available M93C46-x products (package, voltage range, temperature grade)*, *Table 30: Available M93C56-x products (package, voltage range, temperature grade)*, *Table 31: Available M93C66-x products (package, voltage range, temperature grade)*, *Table 32: Available M93C76-x products (package, voltage range, temperature grade)* and *Table 33: Available M93C86-x products (package, voltage range, temperature grade)*.
05-Oct-2011	12	Updated *Table 1: Device summary* and *Table 8: Operating conditions (M93Cx6)*. Modified footnote 2 in *Table 7*.
23-Apr-2013	13	Document reformatted. Updated: – Part number names – *Table 1: Device summary* and package figure on cover page – *Section 1: Description* – Introductory paragraph in *Section 9: Maximum ratings* – Note (2) under *Table 7: Absolute maximum ratings* – *Table 8: Operating conditions (M93Cx6)* and *Table 8: Operating conditions (M93Cx6-W)* – Introductory paragraph in *Section 11: Package information* – *Figure 15: UFDFPN8 8-lead Ultra thin Fine pitch Dual Flat Package No lead 2 x 3 mm, outline* and *Table 20: UFDFPN8 8-lead Ultra thin Fine pitch Dual Flat Package No lead x 3 mm, data* – *Table 22: Ordering information scheme* Renamed: – *Figure 2: 8-pin package connections (top view)* – *Table 16: AC characteristics (M93Cx6, device grade 6)* Deleted: – Section: Common I/O operation – Table: DC characteristics (M93Cx6, device grade 3), Table: DC characteristics (M93Cx6-W, device grade 3), and Table: AC characteristics (M93Cx6-W, device grade 3)

Table 23. Document revision history (continued)

Date	Revision	Changes
26-Oct-2013	14	Updated: – *Table 1: Device summary*: added “M93C46-R” and “M93C86-R”, deleted M93Cxx part numbers. – *Features*: Single supply voltage, write cycles and data retention – *Section 1: Description* – Note (2) under *Table 7: Absolute maximum ratings*. – *Section 10: DC and AC parameters*: updated the introduction and deleted tables related to M93Cxx part numbers. – *Figure 9: AC testing input output waveforms* – *Table 14: DC characteristics (M93Cx6-W, device grade 6)*, *Table 15: DC characteristics (M93Cx6-R)*, *Table 16: AC characteristics (M93Cx6-W, M93Cx6-R, device grade 6)* and *Table 17: AC characteristics (M93Cx6-R)*. – *Table 22: Ordering information scheme*. Added: – *Figure 4: M93Cx6 ORG input connection* – *Table 10: Cycling performance* and *Table 11: Memory cell data retention*.
15-Nov-2013	15	Removed Table 14 Cycling performance by byte
06-Nov-2015	16	Updated: – *Features* – *Table 1: Device summary*; – Notes of *Table 7: Absolute maximum ratings*; – *Table 22: Ordering information scheme* – *Table 11: Package information*
21-Dec-2015	17	Updated: – *Figure 16: UFDFN8 - 8-lead, 2 × 3 mm, 0.5 mm pitch ultra thin profile fine pitch dual flat package outline* – *Table 20: UFDFN8 - 8-lead, 2 × 3 mm, 0.5 mm pitch ultra thin profile fine pitch dual flat package mechanical data*

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