THE DATASHEET OF

MAX11359AETL+T

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MAX11359A

16-Bit Data-Acquisition System with ADC, DAC, UPIOs, RTC, Voltage Monitors, and Temp Sensor

General Description

The MAX11359A smart data-acquisition systems (DAS) is based on a 16-bit, sigma-delta analog-to-digital converter (ADC) and system-support functionality for a microprocessor (µP)-based system. The device integrates an ADC, DAC, operational amplifiers, internal selectable-voltage reference, temperature sensors, analog switches, a 32kHz oscillator, a real-time clock (RTC) with alarm, a high-frequency-locked loop (FLL) clock, four user-programmable I/Os, an interrupt generator, and 1.8V and 2.7V voltage monitors in a single chip.

The MAX11359A has dual 10:1 differential input multiplexers (muxes) that accept signal levels from 0 to AVDD. An on-chip 1x to 8x programmable-gain amplifier (PGA) allows measuring low-level signals and reduces external circuitry required.

The MAX11358B operates from a single +1.8V to +3.6V supply and consumes only 1.4mA in normal mode and only 6.1µA in sleep mode. The MAX11385B has one DACs with two uncommitted op amp.

The serial interface is compatible with either SPI/QSPI™ or MICROWIRE®, and is used to power up, configure, and check the status of all functional blocks.

The MAX11359A is available in a space-saving, 40-pin TQFN package and is specified over the commercial (0°C to +70°C) and the extended (-40°C to +85°C) temperature ranges.

Applications

Battery-Powered and Portable Devices
Electrochemical and Optical Sensors
Medical Instruments
Industrial Control
Data-Acquisition Systems

QSPI is a trademark of Motorola, Inc.
MICROWIRE is a registered trademark of National Semiconductor Corp.

Features

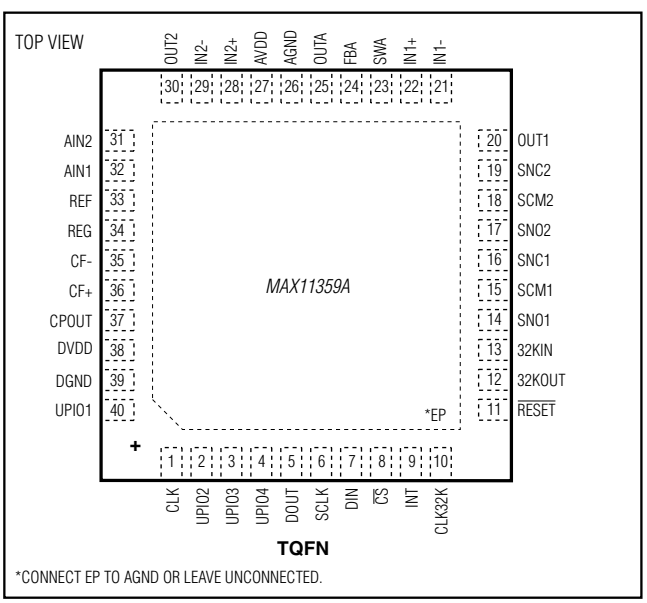
- **+1.8V to +3.6V Single-Supply Operation**
- **Multichannel 16-Bit Sigma-Delta ADC**
  - **10sps to 512sps Programmable Conversion Rate**
  - **Self and System Offset and Gain Calibration**
  - **PGA with Gains of 1, 2, 4, or 8**
  - **Unipolar and Bipolar Modes**
  - **10-Input Differential Multiplexer**
- **10-Bit Force-Sense DACs**
- **Uncommitted Op Amps**
- **Dual SPDT Analog Switches**
- **Selectable References**
  - **1.25V, 1.996V and 2.422V**
- **Internal Charge Pump**
- **System Support**
  - **Real-Time Clock and Alarm Register**
  - **Internal/External Temperature Sensor**
  - **Internal Oscillator with Clock Output**
  - **User-Programmable I/O and Interrupt Generator**
  - **V_{DD} Monitors**
- **SPI/QSPI/MICROWIRE, 4-Wire Serial Interface**
- **Space-Saving (6mm x 6mm x 0.75mm), 40-Pin TQFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX11359AETL+	-40°C to +85°C	40 TQFN-EP**
MAX11359ACTL+*	0°C to +70°C	40 TQFN-EP**

+Denotes a lead(Pb)-free/RoHS–compliant package.
**Future product—contact factory for availability.*
***EP = Exposed pad.*

Pin Configuration



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-4594; Rev 1; 1/12

ABSOLUTE MAXIMUM RATINGS

AVDD to AGND .....-0.3V to +4V
DVDD to DGND .....-0.3V to +4V
AVDD to DVDD .....-4V to +4V
AGND to DGND.....-0.3V to +0.3V
CLK32K to DGND .....-0.3V to (V_{DVDD} + 0.3V)
UPIO_ to DGND.....-0.3V to +4V
Digital Inputs to DGND .....-0.3V to +4V
Analog Inputs to AGND.....-0.3V to (V_{AVDD} + 0.3V)
Digital Output to DGND… .....-0.3V to (V_{DVDD} + 0.3V)
Analog Outputs to AGND.....-0.3V to (V_{AVDD} + 0.3V)
Continuous Current Into Any Pin.....50mA
Continuous Power Dissipation (T_A = +70°C)
40-Pin TQFN (derate 25.6mW/°C above +70°C) 2051.3mW
Operating Temperature Range
MAX11358_ _CTL+.....0°C to +70°C
MAX11358_ _ETL+ .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{DVDD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, CLK32K = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC DC ACCURACY						
Noise-Free Resolution		Data rate = 10sps, PGA gain = 2; data rate = 10sps to 60sps, PGA gain = 1; no missing codes, Table 1 (Note 2)	16			Bits
Conversion Rate		No missing codes, Table 1	10		512	sps
Output Noise		No missing codes		Table 1		μV_{RMS}
Integral Nonlinearity	INL	Unipolar mode, V_{AVDD} = 3V, PGA gain = 1, T_A = +25°C, data rate = 50sps		±0.004		%FSR
Unipolar Offset Error or Bipolar Zero Error (Note 3)		Uncalibrated		±1.0		%FSR
		PGA gain = 1, calibrated, T_A = +25°C, data rate = 50sps			±0.003	
Unipolar Offset-Error or Bipolar Zero-Error Temperature Drift (Note 4)		Bipolar		±2.0		µV/°C
		Unipolar		±10		
Gain Error (Notes 3, 5)		Uncalibrated		±0.6		%FSR
		PGA = 1, calibrated, data rate = 50sps		±0.003		
Gain-Error Temperature Coefficient		(Notes 4, 6)		±1.0		ppm/°C
DC Positive Power-Supply Rejection Ratio	PSRR	PGA gain = 1, unipolar mode, measured by full-scale error with V_{AVDD} = 1.8V to 3.6V		73		dB
ADC ANALOG INPUTS (AIN1, AIN2)						
DC Input Common-Mode Rejection Ratio	CMRR	PGA gain = 1, unipolar mode		85		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, CLK32K = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Normal-Mode 60Hz Rejection Ratio		PGA gain = 1, unipolar mode, data rate = 50sps (Note 2)	100			dB
Normal-Mode 50Hz Rejection Ratio		Data rate = 10sps or 50sps, PGA gain = 1, unipolar mode (Note 2)	100			dB
Absolute Input Range		Internal temperature sensor disabled (Figure 26)	V_{AGND}		V_{AVDD}	V
Differential Input Range		Unipolar mode	-0.05/ Gain		V_{REF}/ Gain	V
		Bipolar mode	-V_{REF}/ Gain		V_{REF}/ Gain	
DC Input Current (Note 7)		ADC not in measurement mode, mux enabled, $T_A \le +55°C$, inputs = +0.1V to (V_{AVDD} - 0.1V)			±1	nA
		T_A = +85°C			±5	
Input Sampling Capacitance	C_{IN}			5		pF
Input Sampling Rate	f_{SAMPLE}			21.84		kHz
External Source Impedance at Input		(Table 3)		Table 3		kΩ
FORCE-SENSE DAC (R_L = 10kΩ and C_L = 200pF, FBA = OUTA, unless otherwise noted)						
Resolution		Guaranteed monotonic	10			Bits
Differential Nonlinearity	DNL	Code 3Dhex to 3FF hex			±1	LSB
Integral Nonlinearity	INL	Code 3Dhex to 3FF hex			±4	LSB
Offset Error		Reference to code 52 hex			±20	mV
Offset-Error Tempco				±4.4		µV/°C
Gain Error		Excludes offset and voltage reference error			±5	LSB
Gain-Error Tempco		Excludes offset and reference drift		±1		ppm/°C
Input Leakage Current at SWA/B		SWA switches open (Notes 7, 8)			±1	nA
Input Leakage Current at FBA/B		V_{FBA} = +0.3V to (V_{AVDD} - 0.3V) (Note 7), T_A = -40°C to +85°C			±1	nA
		V_{FBA} = +0.3V to (V_{AVDD} - 0.3V) (Note 7), T_A = 0°C to +70°C			±600	pA
		V_{FBA} = +0.3V to (V_{AVDD} - 0.3V) (Note 7), T_A = 0°C to +50°C			±400	
DAC Output Buffer Leakage Current		DAC buffer disabled (Note 7)			±75	nA
Input Common-Mode Voltage		At FBA	0		V_{AVDD} - 0.35	V
Line Regulation		V_{AVDD} = +1.8V to +3.6V, T_A = +25°C		40	175	µV/V
Load Regulation		I_{OUT} = ±2mA, C_L = 1000pF (Note 2)			0.5	µV/µA
Output Voltage Range			V_{AGND}		V_{AVDD}	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, CLK32K = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Slew Rate		52 hex to 3FF hex code swing rising or falling, R_L = 10kΩ, C_L = 100pF			40		V/ms
Output-Voltage Settling Time		10% to 90% rising or falling to ±0.5 LSB			65		µs
Input Voltage Noise		Referred to FBA, excludes reference noise	f = 0.1Hz to 10Hz		80		$µV_{P-P}$
			f = 10Hz to 10kHz		200		
Output Short-Circuit Current		OUTA shorted to AGND			20		mA
		OUTA shorted to AVDD			15		
Input-Output SWA/SWB Switch Resistance		Between SWA and OUTA, HFCK enabled				150	Ω
SWA/SWB Switch Turn-On/Off Time		HFCK enabled			100		ns
Power-On Time		Excluding reference			18		µs
EXTERNAL REFERENCE (REF)							
Input Voltage Range				V_{AGND}		V_{AVDD}	V
Input Resistance		DAC on, internal REF and ADC off			2.5		MΩ
DC Input Leakage Current		Internal REF, DAC, and ADC off (Note 7)				100	nA
INTERNAL VOLTAGE REFERENCE (C_{REF} = 4.7µF)							
Reference Output Voltage	V_{REF}	V_{AVDD} ≥ +1.8V, T_A = +25°C		1.238	1.251	1.264	V
		V_{AVDD} ≥ +2.2V, T_A = +25°C		1.976	1.996	2.016	
		V_{AVDD} ≥ +2.7V, T_A = +25°C		2.349	2.422	2.495	
Output-Voltage Temperature Coefficient (Note 7)	TC	V_{REF} = 1.251V			15	50	ppm/°C
		V_{REF} = 1.996V, 2.422V				65	
Output Short-Circuit Current	I_{RSC}	REF shorted to AGND			18		mA
		REF shorted to AVDD			90		µA
Line Regulation		T_A = +25°C				100	µV/V
Load Regulation		T_A = +25°C, V_{REF} = 1.25V	I_{SOURCE} = 0 to 500µA			1.2	µV/µA
			I_{SINK} = 0 to 50µA		1.7		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, CLK32K = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Long-Term Stability		(Note 9)			35		ppm/ 1000hrs
Output Noise Voltage		f = 0.1Hz to 10Hz, V_{AVDD} = 3V			50		μV_{P-P}
		f = 10Hz to 10kHz, V_{AVDD} = 3V			400		
Turn-On Settling Time		Buffer only, settle to 0.1% of final value			100		µs
TEMPERATURE SENSOR							
Temperature Measurement Resolution		ADC resolution is 16-bit, 10sps			0.11		°C/LSB
Internal Temperature-Sensor Measurement Error		Internal voltage reference, four-current calibration, and stored calibration coefficients	T_A = 0°C to +50°C		±0.5		°C
			T_A = -40°C to +85°C		±1		
External Temperature-Sensor Measurement Error (Note 10)		T_A = +25°C			±0.50		°C
		T_A = 0°C to +50°C			±0.5		
		T_A = -40°C to +85°C			±1.0		
Temperature Measurement Noise					0.18		$°C_{RMS}$
Temperature Measurement Power-Supply Rejection Ratio					0.2		°C/V
OP AMP (R_L = 10kΩ connected to V_{AVDD}/2)							
Input Offset Voltage	V_{OS}	V_{CM} = 0.5V				±15	mV
Offset-Error Tempco					3		µV/°C
Input Bias Current (Note 7)	I_{BIAS}	IN1+, IN2+, IN3+	T_A = -40°C to +85°C		0.006	±1	nA
			T_A = 0°C to +70°C		4	±300	pA
			T_A = 0°C to +50°C		2	±200	
		IN1-, IN2-, IN3-	T_A = -40°C to +85°C		0.025	±1	nA
			T_A = 0°C to +70°C		20	±600	pA
			T_A = 0°C to +50°C			±400	
Input Offset Current	I_{OS}	$V_{IN1_}$, $V_{IN2_}$ = +0.3V to (V_{AVDD} - 0.3V) (Note				±1	nA
Input Common-Mode Voltage Range	CMVR			0		V_{AVDD} - 0.35	V
Common-Mode Rejection Ratio	CMRR	0 ≤ V_{CM} ≤ 75mV			60		dB
		75mV < V_{CM} ≤ V_{AVDD} - 0.35V, T_A = +25°C		60	75		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, CLK32K = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = +1.8V to +3.6V, T_A = +25°C		76.5	100		dB
Large-Signal Voltage Gain	A_{VOL}	100mV ≤ $V_{OUT_}$ ≤ V_{AVDD} - 100mV (Note 11)		90	116		dB
Maximum Current Drive	ΔV_{OUT}	Sourcing	I_{SOURCE} = 10µA			0.005	V
			I_{SOURCE} = 50µA			0.025	
			I_{SOURCE} = 100µA			0.05	
			I_{SOURCE} = 500µA			0.25	
			I_{SOURCE} = 2mA			0.5	
		Sinking	I_{SINK} = 10µA			0.005	
			I_{SINK} = 50µA			0.025	
			I_{SINK} = 100µA			0.05	
			I_{SINK} = 500µA			0.25	
			I_{SINK} = 2mA			0.5	
Gain Bandwidth Product	GBW	Unity-gain configuration, C_L = 1nF			80		kHz
Phase Margin		Unity-gain configuration, C_L = 1nF (Note 11)			60		Degrees
Output Slew Rate	SR	C_L = 200pF			0.04		V/µs
Input Voltage Noise		Unity-gain configuration	f = 0.1Hz to 10Hz		80		μV_{P-P}
			f = 10Hz to 10kHz		200		
Output Short-Circuit Current		$V_{OUT_}$ shorted to AGND			20		mA
		$V_{OUT_}$ shorted to AVDD			15		
Power-On Time					15		µs
SPDT SWITCHES (SNO_, SNC_, SCM_, HFCK enabled)							
On-Resistance	R_{ON}	$V_{SCM_}$ = 0V	T_A = 0°C to +50°C			45	Ω
		$V_{SCM_}$ = 0.5V	T_A = 0°C to +50°C			50	
		$V_{SCM_}$ = 0.5V to V_{AVDD}				150	
SNO_, SNC_ Off-Leakage Current	$I_{SNO_(OFF)}$ $I_{SNC_(OFF)}$	$V_{SNO_}$, $V_{SNC_}$ = +0.5V, +1.5V; $V_{SCM_}$ = +1.5V, +0.5V (Note 7)	T_A = -40°C to +85°C			±1	nA
			T_A = 0°C to +70°C			±600	pA
			T_A = 0°C to +50°C			±400	
SCM_ Off-Leakage Current	$I_{SCM_(OFF)}$	$V_{SNO_}$, $V_{SNC_}$ = +0.5V, +1.5V; $V_{SCM_}$ = +1.5V, +0.5V (Note 7)	T_A = -40°C to +85°C			±2	nA
			T_A = 0°C to +70°C			±1.2	
			T_A = 0°C to +50°C			±0.8	
SCM_ On-Leakage Current	$I_{SCM_(ON)}$	$V_{SNO_}$, $V_{SNC_}$ = +0.5V, +1.5V, or unconnected; $V_{SCM_}$ = +1.5V, +0.5V (Note 7)	T_A = -40°C to +85°C			±2	nA
			T_A = 0°C to +70°C			±1.2	
			T_A = 0°C to +50°C			±0.8	
Input Voltage Range				V_{AGND}		V_{AVDD}	V
Turn-On/Off Time	t_{ON}/t_{OFF}	Break-before-make			100		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, CLK32K = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance		SNO_, SNC_, or SCM_ = AVDD or AGND; switch connected to enabled mux input		5		pF
CHARGE PUMP (10µF at REG and 10µF external capacitor between CF+ and CF-)						
Maximum Output Current	I_{OUT}		10			mA
Output Voltage		No load	3.2	3.3	3.6	V
		I_{OUT} = 10mA	3.0			
Output Voltage Ripple		10µF external capacitor between CPOUT and DGND, I_{OUT} = 10mA, excluding ESR of external capacitor			50	mV
Load Regulation		I_{OUT} = 10mA, excluding ESR of external capacitor		15	20	mV/mA
REG Input Voltage Range		Internal linear regulator disabled	1.6		1.8	V
REG Input Current		Linear regulator off, charge pump off		3		nA
CPOUT Input Voltage Range		Charge pump disabled	1.8		3.6	V
CPOUT Input Leakage Current		Charge pump disabled		2		nA
SIGNAL-DETECT COMPARATOR						
Differential Input-Detection Threshold Voltage		TSEL[2:0] = 0 hex		0		mV
		TSEL[2:0] = 4 hex		50		
		TSEL[2:0] = 5 hex		100		
		TSEL[2:0] = 6 hex		150		
		TSEL[2:0] = 7 hex		200		
Differential Input-Detection Threshold Error				±10		mV
Common-Mode Input Voltage Range			V_{AGND}		V_{AVDD}	V
Turn-On Time				50		µs
VOLTAGE MONITORS						
DVDD Monitor Supply Voltage Range		For valid reset	1.0		3.6	V
Trip Threshold (V_{DVDD} Falling)			1.80	1.85	1.90	V
DVDD Monitor Timeout Reset Period				1.5		s
DVDD Monitor Hysteresis		HYSE bit set to logic 1		200		mV
		HYSE bit set to logic 0		35		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, CLK32K = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DVDD Monitor Turn-On Time				5		ms
CPOUT Monitor Supply Voltage Range			1.0		3.6	V
CPOUT Monitor Trip Threshold			2.7	2.8	2.9	V
CPOUT Monitor Hysteresis				35		mV
CPOUT Monitor Turn-On Time				5		ms
Internal Power-On Reset Voltage					1.7	V
32kHz Oscillator (32KIN, 32KOUT)						
Clock Frequency		V_{DVDD} = 2.7V		32.768		kHz
Stability		V_{DVDD} = 1.8V to 3.6V, excluding crystal		25		ppm
Oscillator Startup Time				1500		ms
Crystal Load Capacitance				6		pF
LOW-FREQUENCY CLOCK INPUT/OUTPUT (CLK32K)						
Output Clock Frequency				32.768		kHz
Absolute Input to Output Clock Jitter		Cycle to cycle		5		ns
Input to Output Rise/Fall Time		10% to 90%, 30pF load		5		ns
Input Duty Cycle			40		60	%
Output Duty Cycle				43		%
HIGH-FREQUENCY CLOCK OUTPUT (CLK)						
FLL Output Clock Frequency		f_{OUT} = f_{FLL}	4.8660	4.9152	4.9644	MHz
		f_{OUT} = f_{FLL}/2, power-up default	2.4330	2.4576	2.4822	MHz
		f_{OUT} = f_{FLL}/4	1.2165	1.2288	1.2411	MHz
		f_{OUT} = f_{FLL}/8	608.25	614.4	620.54	kHz
Absolute Clock Jitter		Cycle to cycle, FLL off		0.15		ns
		Cycle to cycle, FLL on		1		ns
Rise and Fall Time	t_R/t_F	10% to 90%, 30pF load			10	ns
Duty Cycle		f_{OUT} = 4.9152MHz	40		60	%
		f_{OUT} = 2.4576MHz, 1.2288MHz, 614.4kHz	45		55	%
Uncalibrated CLK Frequency Error		FLL calibration not performed			±35	%
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, UPIO_, CLK32K)						
Input High Voltage	V_{IH}		0.7 x V_{DVDD}			V
Input Low Voltage	V_{IL}				0.3 x V_{DVDD}	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, CLK32K = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UPIO_ Input High Voltage		DVDD supply voltage	0.7 x V_{DVDD}			V
		CPOUT supply voltage	0.7 x V_{CPOUT}			
UPIO_ Input Low Voltage		DVDD supply voltage			0.3 x V_{DVDD}	V
		CPOUT supply voltage			0.3 x V_{CPOUT}	
Input Hysteresis	V_{HYS}	V_{DVDD} = 3.0V		200		mV
Input Current	I_{IN}	V_{IN} = V_{DGND} or DVDD (Note 7)		±0.01	±100	nA
Input Capacitance		V_{IN} = V_{DGND} or DVDD		10		pF
UPIO_ Input Current		V_{IN} = DVDD or V_{CPOUT}, pullup enabled		±0.01	1	µA
		V_{IN} = DVDD or V_{CPOUT} or 0V, pullup disabled			1	
UPIO_ Pullup Current		V_{IN} = 0, pullup enabled, unconnected UPIO inputs are pulled up to DVDD or CPOUT with pullup enabled	0.5	2	5	µA
DIGITAL OUTPUTS (DOUT, $\overline{RESET}$, UPIO_, CLK32K, INT, CLK)						
Output Low Voltage	V_{OL}	I_{SINK} = 1mA			0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = 500µA	0.8 x V_{DVDD}			V
DOUT Three-State Leakage Current	I_L			±0.01	±1	µA
DOUT Three-State Output Capacitance	C_{OUT}			15		pF
$\overline{RESET}$ Output Low Voltage	V_{OL}	I_{SINK} = 1mA			0.4	V
$\overline{RESET}$ Output Leakage Current		Open-drain output, $\overline{RESET}$ deasserted			0.1	µA
UPIO_ Output Low Voltage	V_{OL}	I_{SINK} = 1mA, UPIO_ referenced to DVDD			0.4	V
		I_{SINK} = 4mA, UPIO_ referenced to CPOUT			0.4	
UPIO_ Output High Voltage	V_{OH}	I_{SOURCE} = 500µA, UPIO_ referenced to DVDD	0.8 x V_{DVDD}			V
		I_{SOURCE} = 4mA, UPIO_ referenced to CPOUT	V_{CPOUT} - 0.4			
POWER REQUIREMENT						
Analog Supply Voltage Range	AVDD		1.8		3.6	V
Digital Supply Voltage Range	DVDD		1.8		3.6	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, CLK32K = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Total Supply Current	I_{MAX}	Everything on, charge pump unloaded, no digital pins, sinking/sourcing current, e.g., $\overline{RST}$, UPIO, and CLK32K, max internal temp-sensor current, clock output buffers unloaded, ADC at 512sps	V_{AVDD} = V_{DVDD} = 3.6V		1.36	2.0	mA
			V_{AVDD} = V_{DVDD} = 3.3V		1.15	1.7	
	I_{NORMAL}	All on except charge pump and temp sensor, ADC at 512sps, CLK output buffer enabled, clock output buffers unloaded			1.17	1.3	
Sleep-Mode Supply Current	I_{SLEEP}	T_A = -45°C to +85°C	V_{AVDD} = V_{DVDD} = 3.0V			6.5	µA
			V_{AVDD} = V_{DVDD} =			9	
		T_A = +25°C	V_{AVDD} = V_{DVDD} = 3.0V		4.42		
			V_{AVDD} = V_{DVDD} = 3.6V		5.56		
Shutdown Supply Current	I_{SHDN}	All off	T_A = -40°C to +85°C			4	µA
			T_A = +25°C		1.6		

Note 1: Devices are production tested at T_A = +25°C and T_A = +85°C. Specifications to T_A = -40°C are guaranteed by design.

Note 2: Guaranteed by design or characterization.

Note 3: The offset and gain errors are corrected by self-calibration or system calibration. For accurate calibrations, perform calibration at the lowest rate. The calibration error is therefore in the order of peak-to-peak noise for the selected rate.

Note 4: Eliminate drift errors by recalibration at the new temperature.

Note 5: The gain error excludes reference error, offset error (unipolar), and zero error (bipolar).

Note 6: Gain-error drift does not include unipolar offset drift or bipolar zero-error drift. It is effectively the drift of the part if zero-scale error is removed.

Note 7: These specifications are obtained from characterization during design or from initial product evaluation. Not production tested or guaranteed.

Note 8: V_{OUTA} = +0.5V or +1.5V, V_{SWA} = +1.5V or +0.5V, T_A = 0°C to +50°C.

Note 9: Long-term stability is characterized using five to six parts. The bandgaps are turned on for 1000hrs at room temperature with the parts running continuously. Daily measurements are taken and any obvious outlying data points are discarded.

Note 10: All of the stated temperature accuracies assume that 1) the external diode characteristic is precisely known (i.e., ideal) and 2) the ADC reference voltage is exactly equal to 1.25V. Any variations to this known reference characteristic and voltage caused by temperature, loading, or power supply results in errors in the temperature measurement. The actual temperature calculation is performed externally by the microcontroller (µC).

Note 11: Values based on simulation results and are not production tested or guaranteed.

Table 1. Output Noise (Notes 12, 13, and 14)

RATE (sps)	OUTPUT NOISE (μV_{RMS})			
	GAIN = 1	GAIN = 2	GAIN = 4	GAIN = 8
10	1.684	1.684	1.684	1.684
40	3.178	3.178	3.178	3.178
50	3.234	3.234	3.234	3.234
60	3.307	3.307	3.307	3.307
200	55.336	55.336	55.336	55.336
240	104.596	104.596	104.596	104.596
400	587.138	587.138	587.138	587.138
512	983.979	983.979	983.979	983.979

Note 12: V_{REF} = ±1.25V, bipolar mode, V_{IN} = 1.24912V, PGA gain = 1, T_A = +85°C.

Note 13: C_{IN} = 5pF, op-amp noise is considered to be the same as the switching noise. The increase in the op amp's noise contribution is due to a large input swing (0 to 3.6V).

Note 14: Assume ±3 sigma peak-to-peak variation; noise-free resolution means no code flicker at given bits' LSB.

Table 2. Peak-to-Peak Resolution

RATE (sps)	PEAK-TO-PEAK RESOLUTION (Bits)			
	GAIN = 1	GAIN = 2	GAIN = 4	GAIN = 8
10	17.49	17.49	17.49	17.49
40	16.57	16.57	16.57	16.57
50	16.55	16.55	16.55	16.55
60	16.51	16.51	16.51	16.51
200	12.45	12.45	12.45	12.45
240	11.53	11.53	11.53	11.53
400	9.04	9.04	9.04	9.04
512	8.30	8.30	8.30	8.30

Table 3. Maximum External Source Impedance Without 16-Bit Gain Error

PARAMETER	EXTERNAL CAPACITANCE (pF)					
	0 (Note 15)	50	100	500	1000	5000
Resistance (kΩ)	350	60	30	10	4	1

Note 15: 2pF parasitic capacitance is assumed, which represents pad and any other parasitic capacitance.

TIMING CHARACTERISTICS (Figures 1 and 20)

(V_{AVDD} = V_{AVDD} = +1.8V to +3.6V, external V_{REF} = +1.25V, CLK32K = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Operating Frequency	f_{SCLK}		0		10	MHz
SCLK Cycle Time	t_{CYC}		100			ns
SCLK Pulse-Width High	t_{CH}		40			ns
SCLK Pulse-Width Low	t_{CL}		40			ns
DIN to SCLK Setup	t_{DS}		30			ns
DIN to SCLK Hold	t_{DH}		0			ns
SCLK Fall to DOUT Valid	t_{DO}	C_L = 50pF, Figure 2			40	ns
$\overline{CS}$ Fall to Output Enable	t_{DV}	C_L = 50pF, Figure 2			48	ns
$\overline{CS}$ Rise to DOUT Disable	t_{TR}	C_L = 50pF, Figure 2			48	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}		20			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}		0			ns
DVDD Monitor Timeout Period	t_{DSLP}	(Note 16)		1.5		s
Wake-Up (WU) Pulse Width	t_{WU}	Minimum pulse width required to detect a wake-up event		1		µs
Shutdown Delay	t_{DPU}	The delay for $\overline{SHDN}$ to go high after a valid wake-up event		1		µs
HFCK Turn-On Time	t_{DFON}	The turn-on time for the high-frequency clock and FLL (FLLE = 1) (Note 17)			10	ms
		If FLLE = 0, the turn-on time for the high-frequency clock (Note 18)			10	µs
CRDY to $\overline{INT}$ Delay	t_{DFI}	The delay for CRDY to go low after the HFCK clock output has been enabled (Note 19)		7.82		ms
HFCK Disable Delay	t_{DFOF}	The delay after a shutdown command has asserted and before HFCK is disabled (Note 20)		1.95		ms
$\overline{SHDN}$ Assertion Delay	t_{DPD}	(Note 21)		2.93		ms

Note 16: The delay for the sleep voltage monitor output, $\overline{RESET}$, to go high after V_{DD} rises above the reset threshold. This is largely driven by the startup of the 32kHz oscillator.

Note 17: It is gated by an AND function with three inputs—the external $\overline{RESET}$ signal, the internal DV_{DD} monitor output, and the external $\overline{SHDN}$ signal. The time delay is timed from the internal LOV_{DD} going high or the external $\overline{RESET}$ going high, whichever happens later. HFCK always starts in the low state.

Note 18: If FLLE = 0, the internal signal CRDY is not generated by the FLL block and $\overline{INT}$ or INT are deasserted.

Note 19: CRDY is used as an interrupt signal to inform the µC that the high-frequency clock has started. Only valid if FLLE = 1.

Note 20: t_{DFOF} gives the µC time to clean up and go into sleep-override mode properly.

Note 21: t_{DPD} is greater than the HFCK delay for the MAX11358B/MAX11359A to clean up before losing power.

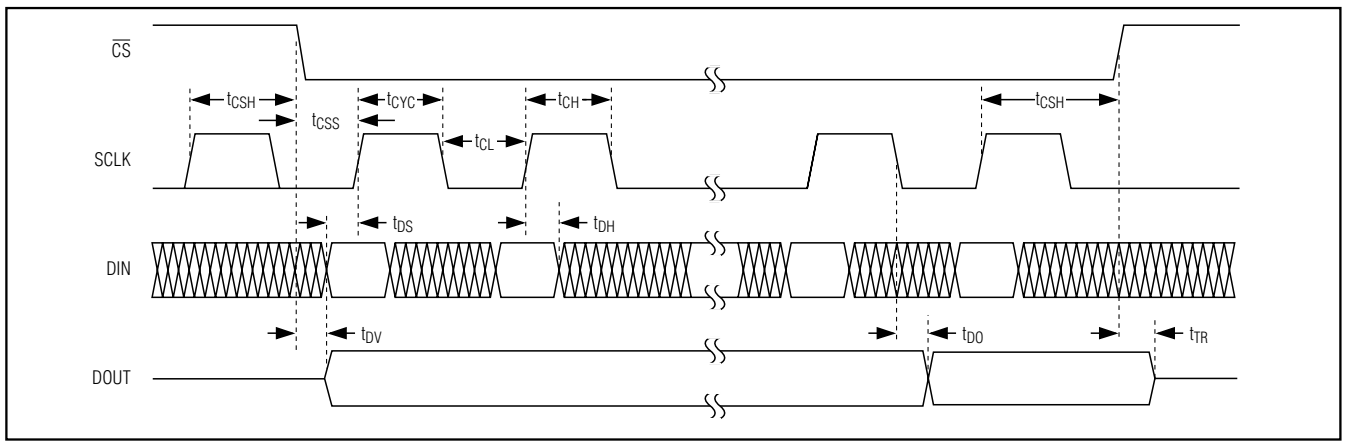


Figure 1. Detailed Serial-Interface Timing

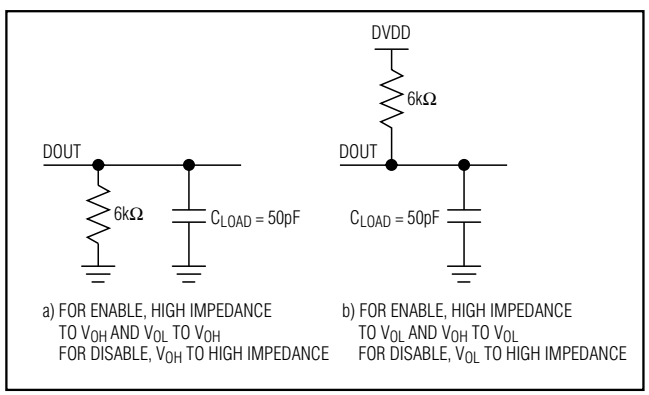
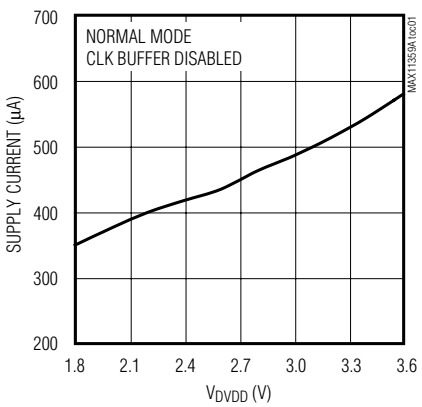


Figure 2. DOUT Enable and Disable Time Load Circuits

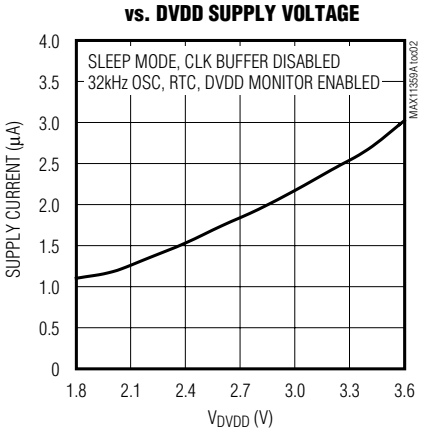
Typical Operating Characteristics

(V_{DVDD} = V_{AVDD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

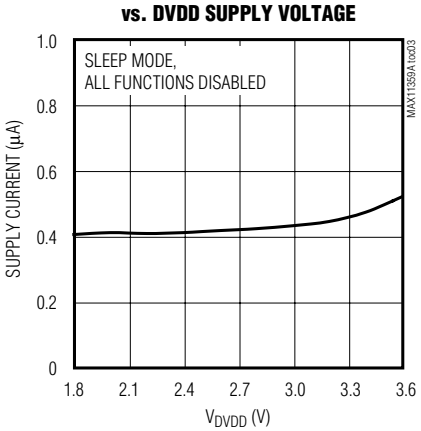
DVDD SUPPLY CURRENT vs. DVDD SUPPLY VOLTAGE



DVDD SUPPLY CURRENT vs. DVDD SUPPLY VOLTAGE



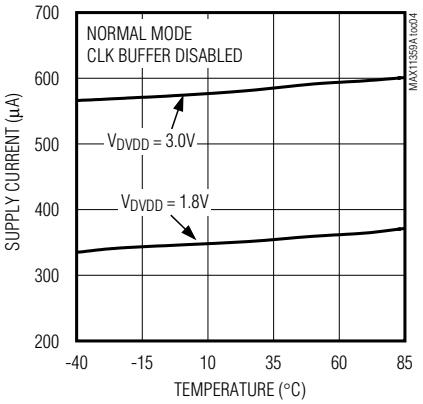
DVDD SUPPLY CURRENT vs. DVDD SUPPLY VOLTAGE



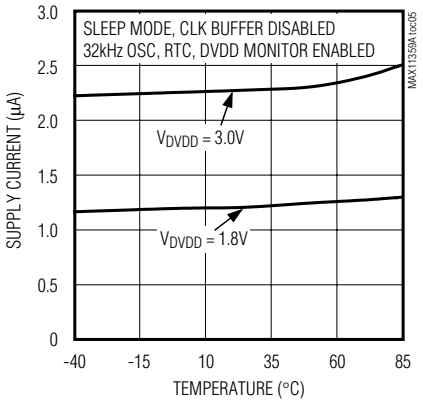
Typical Operating Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

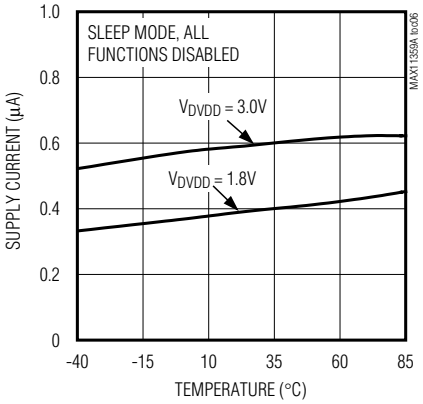
DVDD SUPPLY CURRENT vs. TEMPERATURE



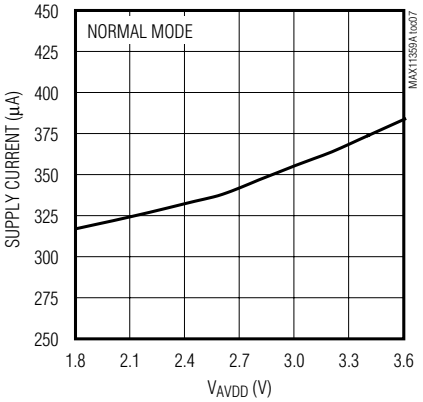
DVDD SUPPLY CURRENT vs. TEMPERATURE



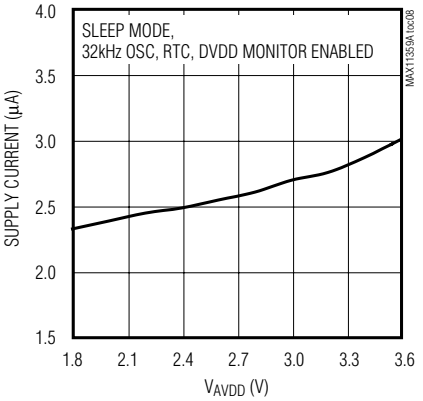
DVDD SUPPLY CURRENT vs. TEMPERATURE



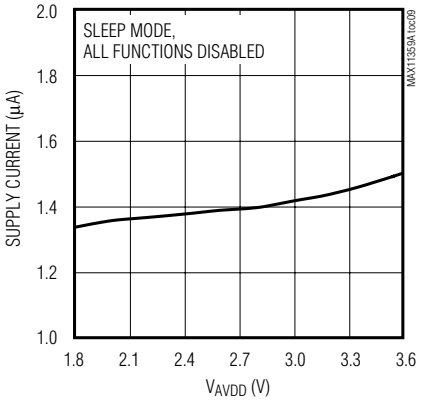
AVDD SUPPLY CURRENT vs. AVDD SUPPLY VOLTAGE



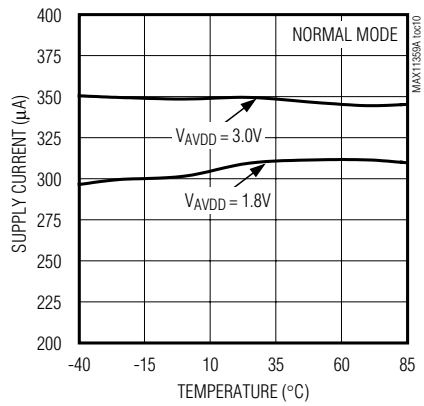
AVDD SUPPLY CURRENT vs. AVDD SUPPLY VOLTAGE



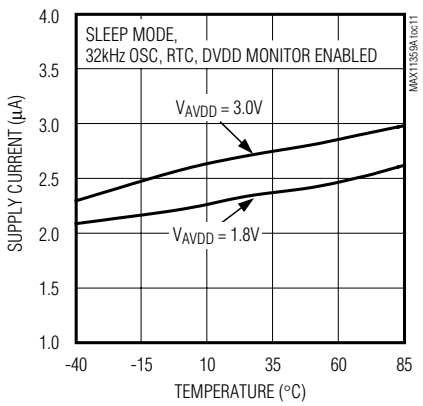
AVDD SUPPLY CURRENT vs. AVDD SUPPLY VOLTAGE



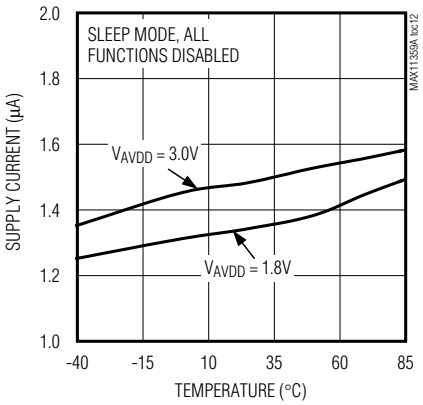
AVDD SUPPLY CURRENT vs. TEMPERATURE



AVDD SUPPLY CURRENT vs. TEMPERATURE



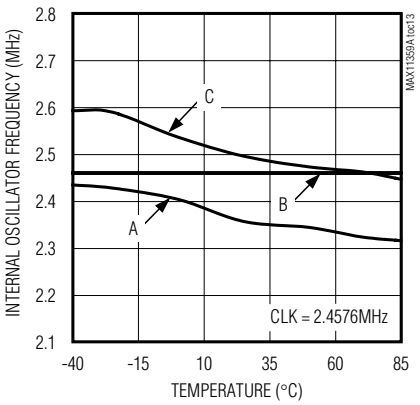
AVDD SUPPLY CURRENT vs. TEMPERATURE



Typical Operating Characteristics (continued)

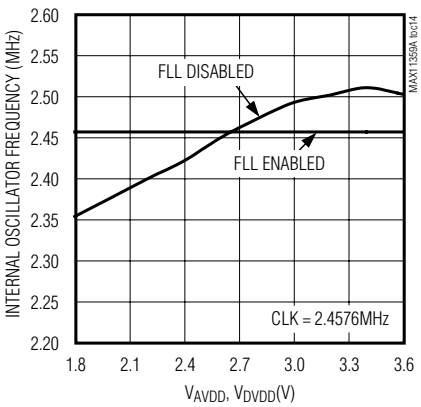
(V_{DVDD} = V_{AVDD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

INTERNAL OSCILLATOR FREQUENCY vs. TEMPERATURE

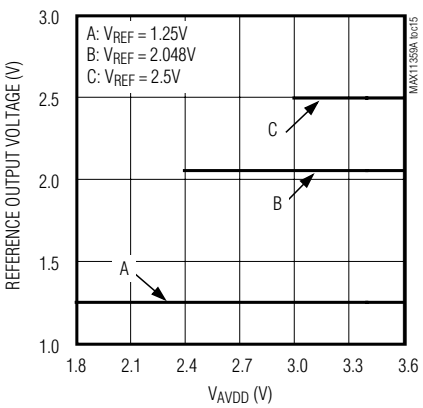


A: FLL DISABLED; V_{AVDD}, V_{DVDD} = 1.8V
B: FLL ENABLED
C: FLL DISABLED; V_{AVDD}, V_{AVDD} = 3.0V

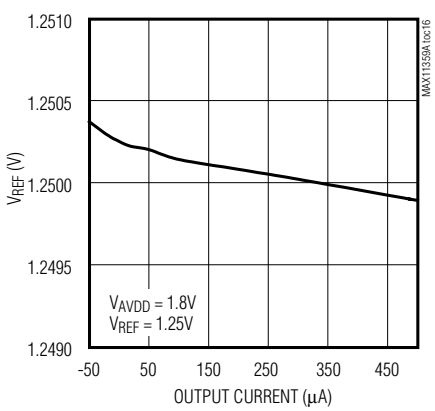
INTERNAL OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



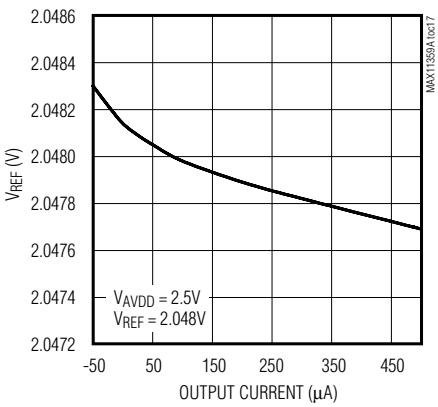
REFERENCE OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



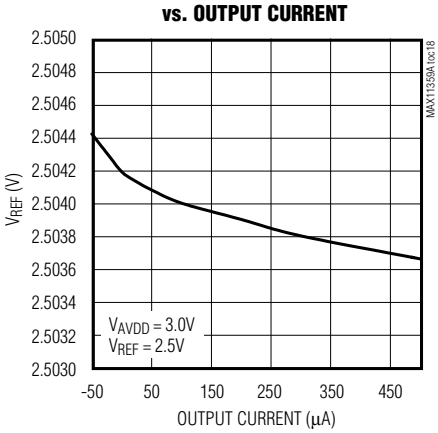
REFERENCE OUTPUT VOLTAGE vs. OUTPUT CURRENT



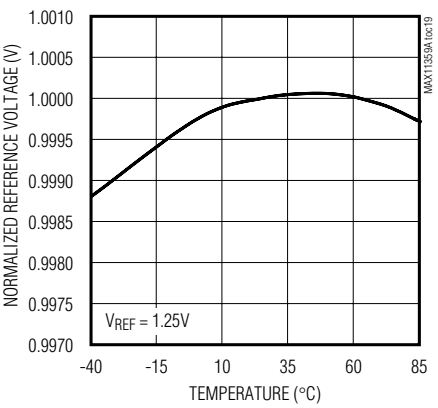
REFERENCE OUTPUT VOLTAGE vs. OUTPUT CURRENT



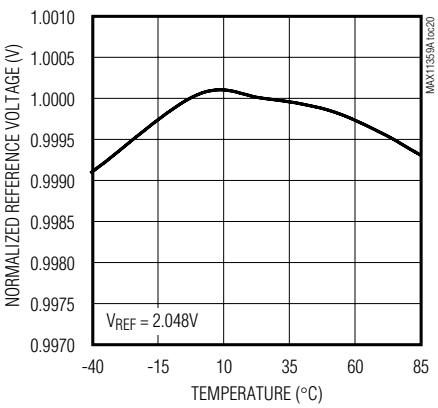
REFERENCE OUTPUT VOLTAGE vs. OUTPUT CURRENT



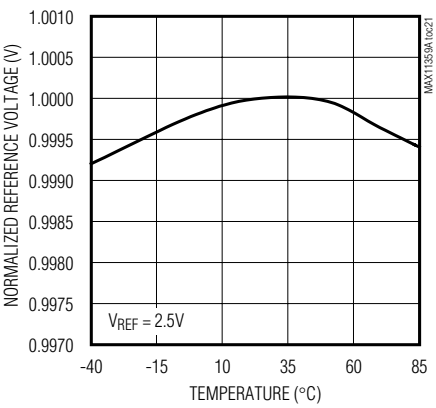
NORMALIZED REFERENCE OUTPUT VOLTAGE vs. TEMPERATURE



NORMALIZED REFERENCE OUTPUT VOLTAGE vs. TEMPERATURE



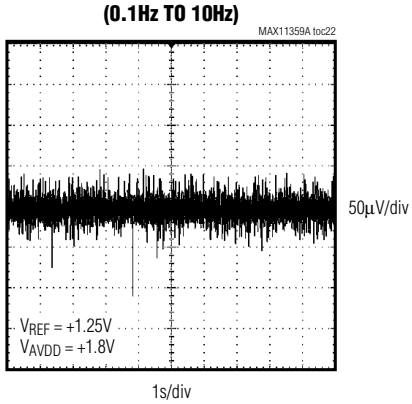
NORMALIZED REFERENCE OUTPUT VOLTAGE vs. TEMPERATURE



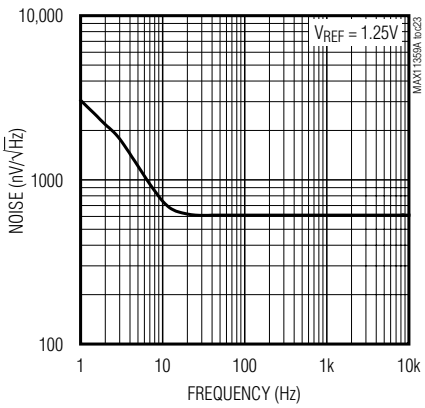
Typical Operating Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

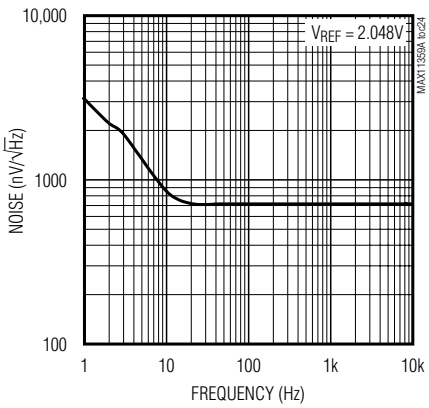
REFERENCE VOLTAGE OUTPUT NOISE (0.1Hz TO 10Hz)



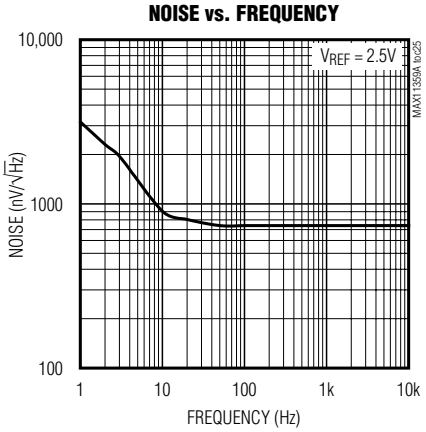
REFERENCE VOLTAGE OUTPUT NOISE vs. FREQUENCY



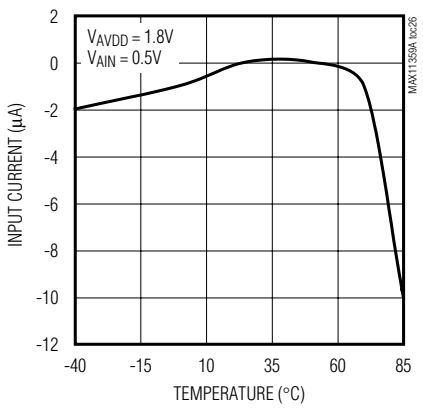
REFERENCE VOLTAGE OUTPUT NOISE vs. FREQUENCY



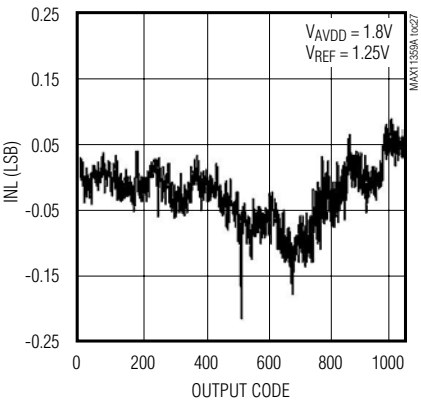
REFERENCE VOLTAGE OUTPUT NOISE vs. FREQUENCY



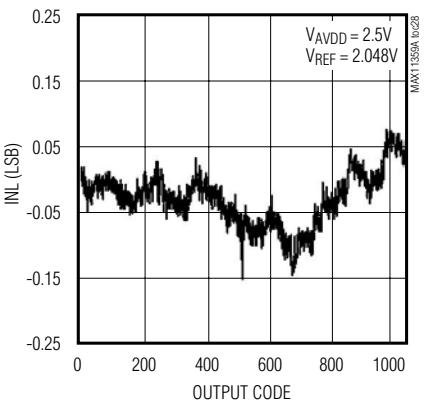
ADC MUX INPUT DC CURRENT vs. TEMPERATURE



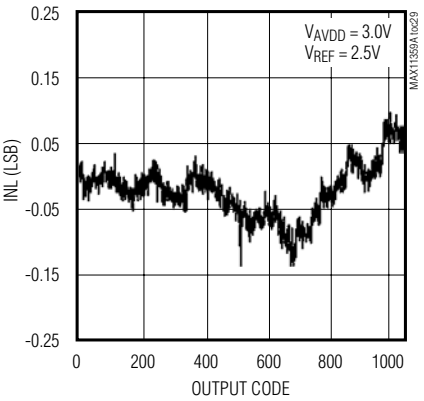
DAC INL vs. OUTPUT CODE



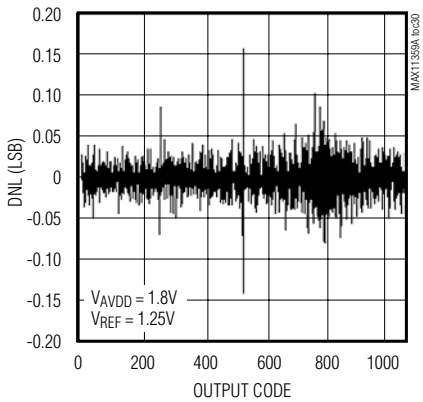
DAC INL vs. OUTPUT CODE



DAC INL vs. OUTPUT CODE



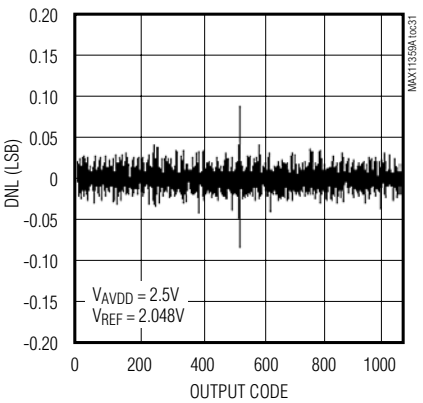
DAC DNL vs. OUTPUT CODE



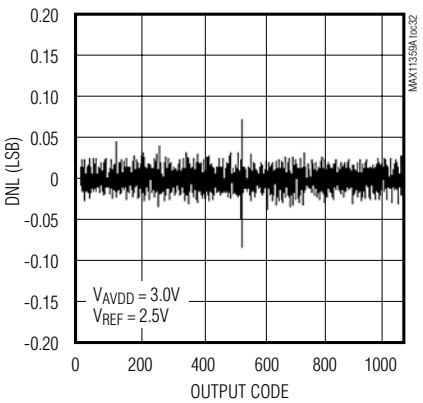
Typical Operating Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

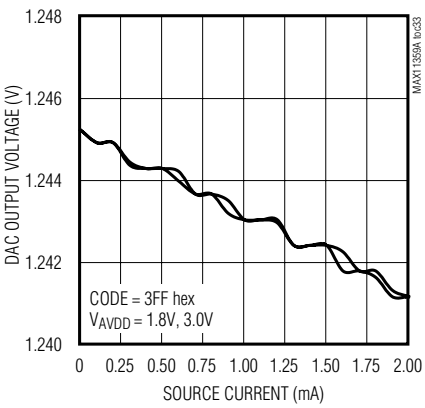
DAC DNL vs. OUTPUT CODE



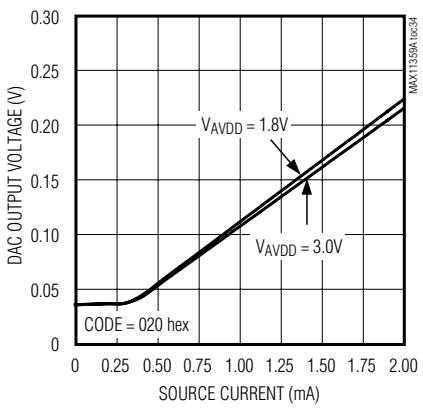
DAC DNL vs. OUTPUT CODE



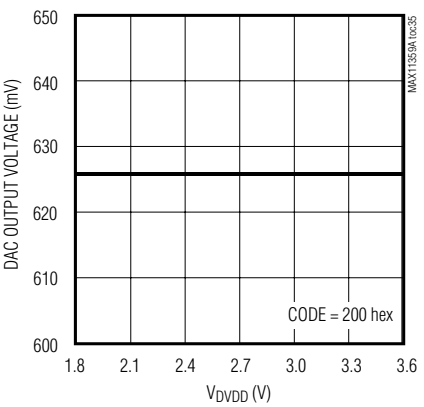
DAC OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT



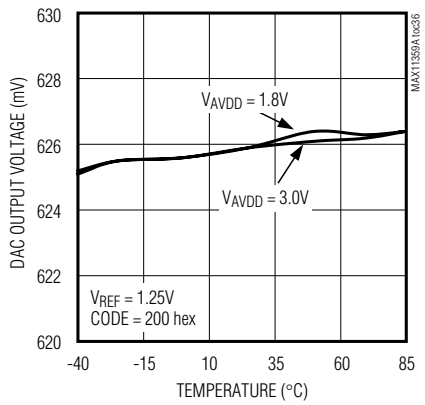
DAC OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT



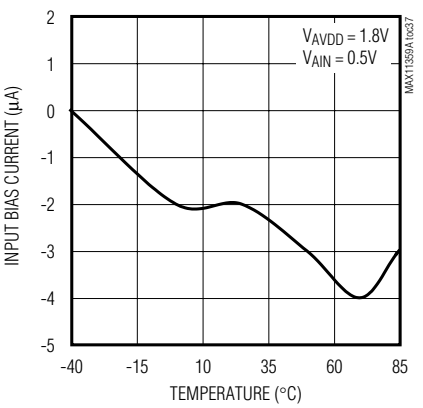
DAC OUTPUT VOLTAGE vs. ANALOG SUPPLY VOLTAGE



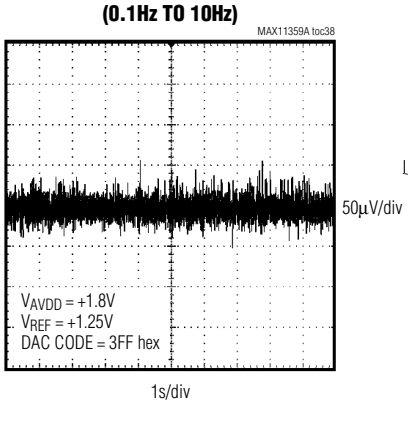
DAC OUTPUT VOLTAGE vs. TEMPERATURE



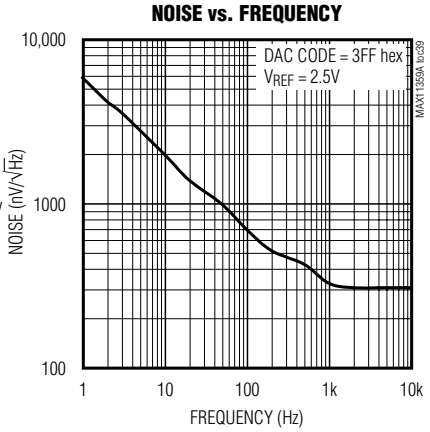
DAC FBA/B INPUT BIAS CURRENT vs. TEMPERATURE



DAC OUTPUT NOISE (0.1Hz TO 10Hz)



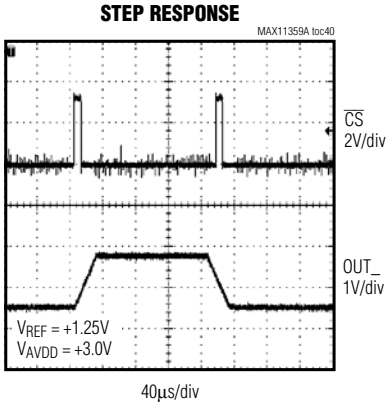
DAC OUTPUT NOISE vs. FREQUENCY



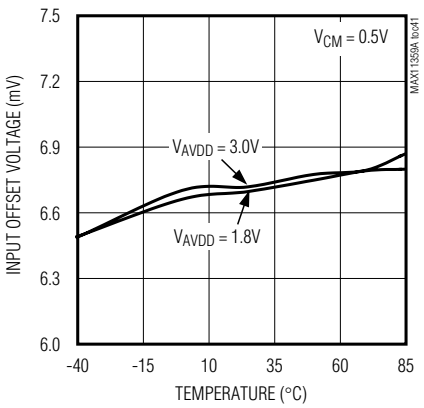
Typical Operating Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

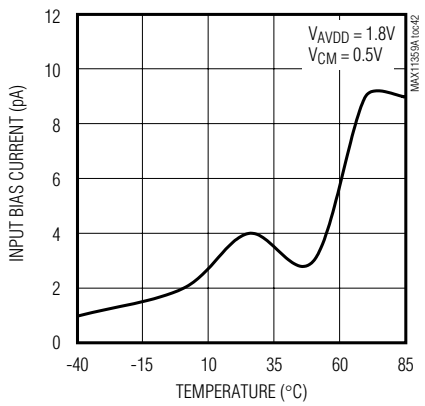
DAC LARGE-SIGNAL OUTPUT STEP RESPONSE



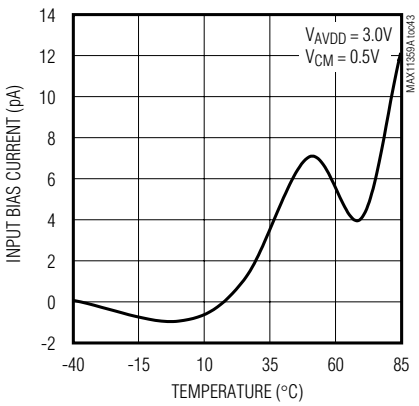
OP-AMP INPUT OFFSET VOLTAGE vs. TEMPERATURE



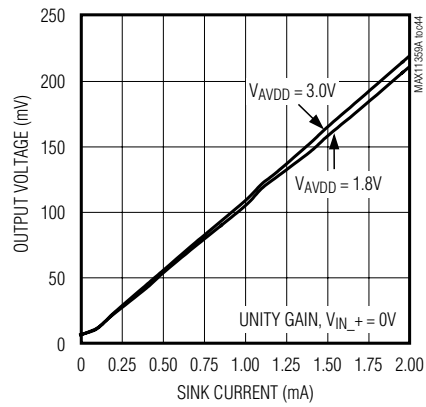
OP-AMP INPUT BIAS CURRENT vs. TEMPERATURE



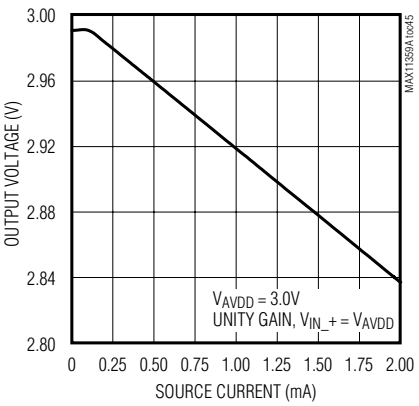
OP-AMP INPUT BIAS CURRENT vs. TEMPERATURE



OP-AMP OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT



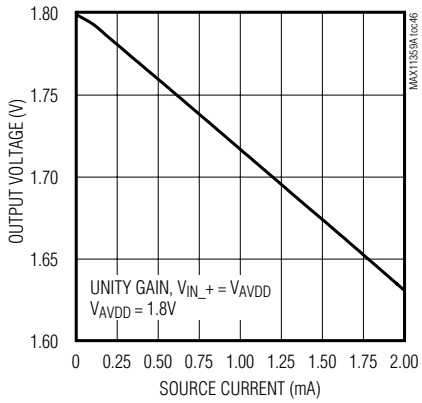
OP-AMP OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT



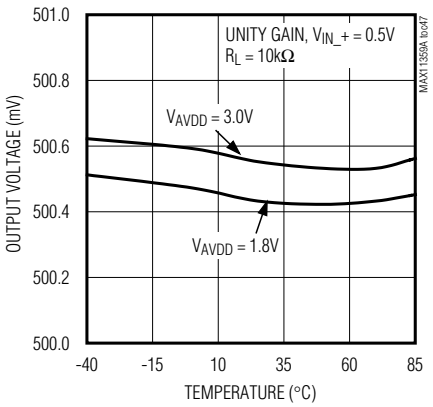
Typical Operating Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

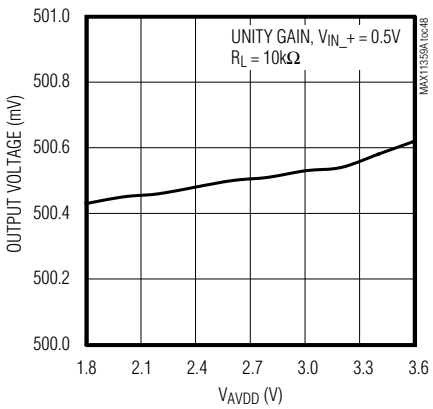
OP-AMP OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT



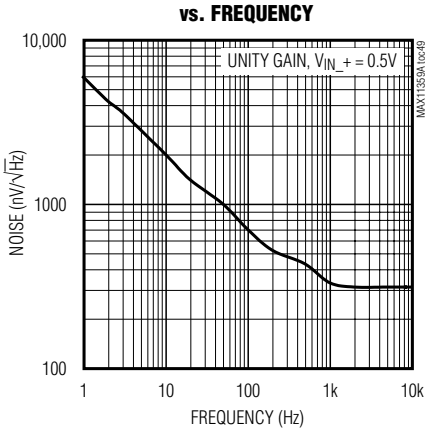
OP-AMP OUTPUT VOLTAGE vs. TEMPERATURE



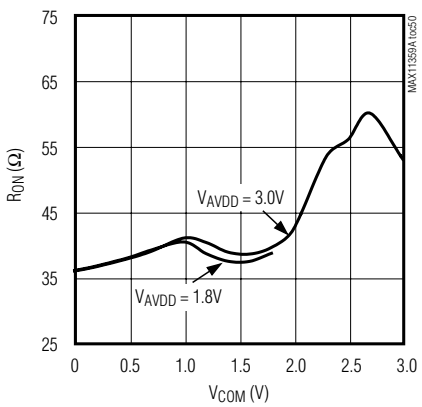
OP-AMP OUTPUT VOLTAGE vs. AV_{DD} SUPPLY VOLTAGE



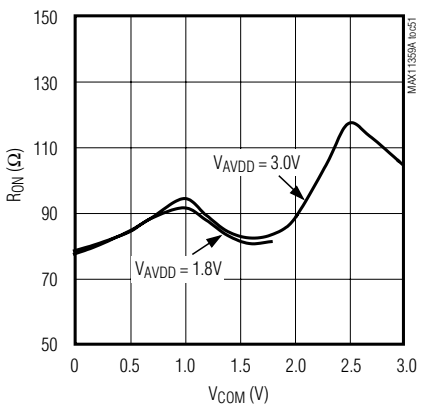
OP-AMP OUTPUT NOISE vs. FREQUENCY



SPDT ON-RESISTANCE vs. V_{COM} VOLTAGE



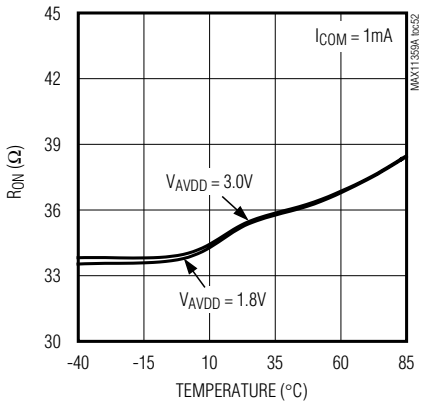
SPST ON-RESISTANCE vs. V_{COM} VOLTAGE



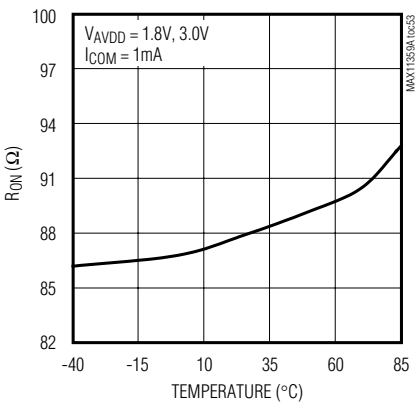
Typical Operating Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

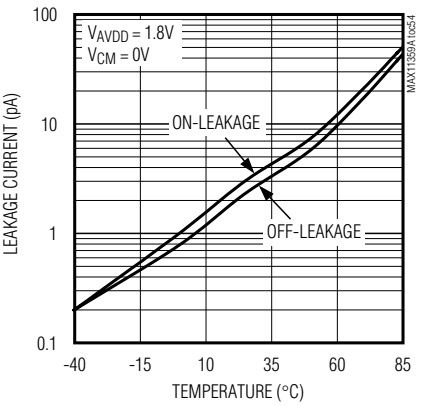
SPDT ON-RESISTANCE vs. TEMPERATURE



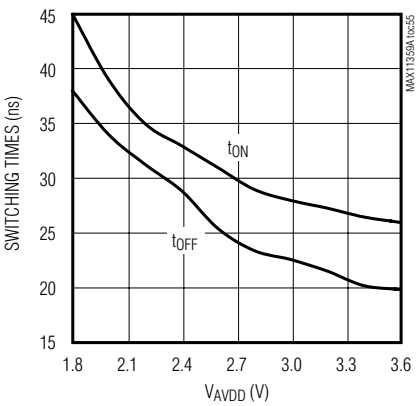
SPST ON-RESISTANCE vs. TEMPERATURE



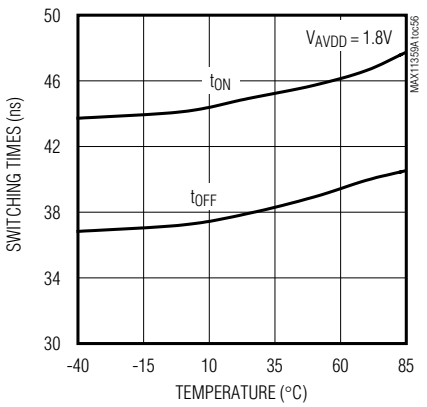
SPDT/SPST ON-/OFF-LEAKAGE CURRENT vs. TEMPERATURE



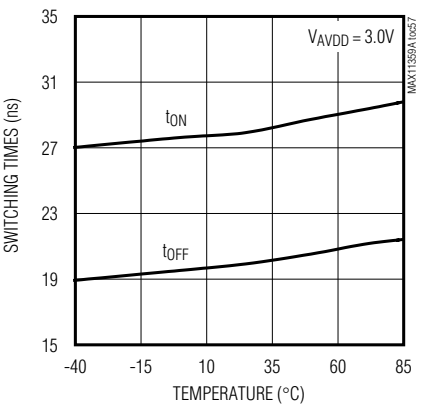
SPDT/SPST SWITCHING TIME vs. AVDD SUPPLY VOLTAGE



SPDT/SPST SWITCHING TIME vs. TEMPERATURE



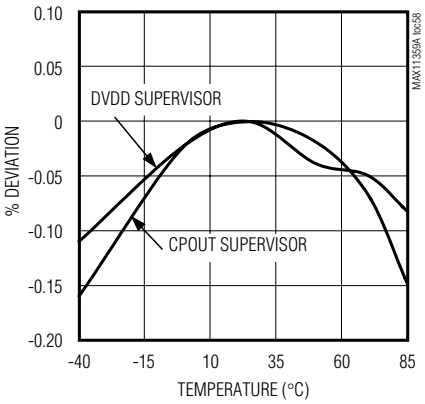
SPDT/SPST SWITCHING TIME vs. TEMPERATURE



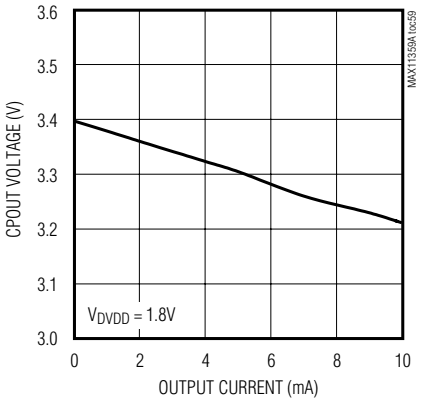
Typical Operating Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

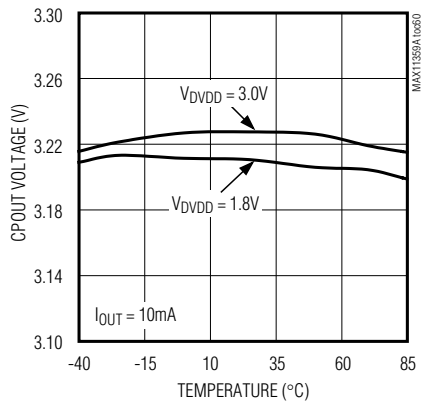
VOLTAGE SUPERVISOR THRESHOLD vs. TEMPERATURE



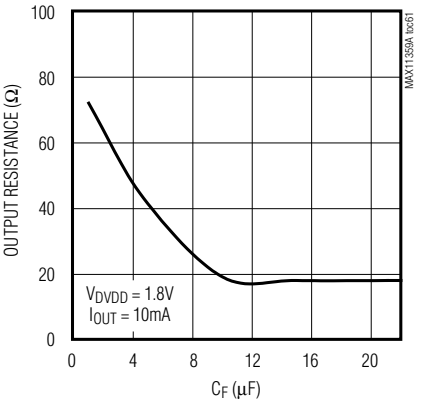
CHARGE-PUMP OUTPUT VOLTAGE vs. OUTPUT CURRENT



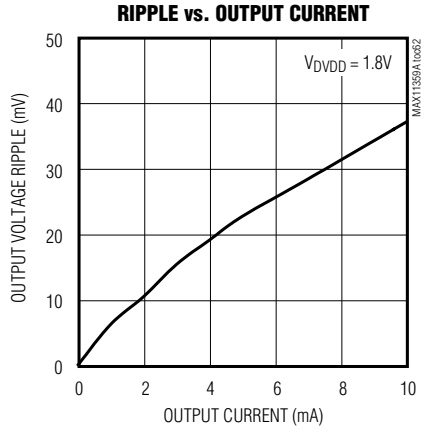
CHARGE-PUMP OUTPUT VOLTAGE vs. TEMPERATURE



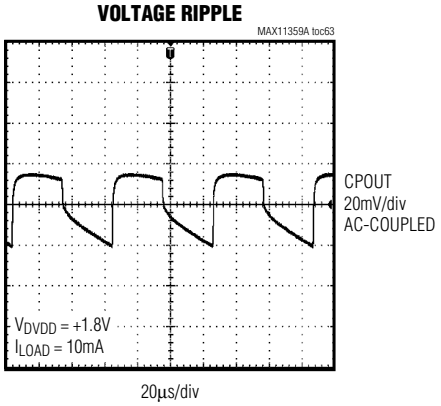
CHARGE-PUMP OUTPUT RESISTANCE vs. CAPACITANCE



CHARGE-PUMP OUTPUT VOLTAGE RIPPLE vs. OUTPUT CURRENT



CHARGE-PUMP OUTPUT VOLTAGE RIPPLE



Pin Description

PIN	NAME	FUNCTION
1	CLK	Clock Output. Default is 2.457MHz output clock for µC.
2	UPIO2	User-Programmable Input/Output 2. See the *UPIO2_CTRL Register* section for functionality.
3	UPIO3	User-Programmable Input/Output 3. See the *UPIO3_CTRL Register* section for functionality.
4	UPIO4	User-Programmable Input/Output 4. See the *UPIO4_CTRL Register* section for functionality.
5	DOUT	Serial-Data Output. Data is clocked out on SCLK's falling edge. High impedance when $\overline{CS}$ is high. When UPIO/SPI passthrough mode is enabled, DOUT mirrors the state of UPIO1.
6	SCLK	Serial-Clock Input. Clocks data in and out of the serial interface.
7	DIN	Serial-Data Input. Data is clocked in on SCLK's rising edge.
8	$\overline{CS}$	Active-Low Chip-Select Input. Data is not clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance. High impedance when $\overline{CS}$ is high. When UPIO/SPI passthrough mode is enabled, DOUT mirrors the state of UPIO1.
9	INT	Programmable Active-High/Low Interrupt Output. ADC, UPIO wake-up, alarm, and voltage-monitor events.
10	CLK32K	32kHz Clock Input/Output. Outputs 32kHz clock for µC. Can be programmed as an input by enabling the IO32E bit to accept an external 32kHz input clock. The RTC, PWM, and watchdog timer always use the internal 32kHz clock derived from the 32kHz crystal.
11	$\overline{RESET}$	Active-Low Open-Drain Reset Output. Remains low while DVDD is below the 1.8V voltage threshold, and stays low for a timeout period (t_{DSLP}) after DVDD rises above the 1.8V threshold. $\overline{RESET}$ also pulses low when the watchdog timer times out and holds low during POR until the 32kHz oscillator stabilizes.
12	32KOUT	32kHz Crystal Output. Connect external 32kHz watch crystal between 32KIN and 32KOUT.
13	32KIN	32kHz Crystal Input. Connect external 32kHz watch crystal between 32KIN and 32KOUT or drive with CMOS level as shown in Figure 25.
14	SNO1	Analog Switch 1 Normally Open Terminal. Analog input to mux.
15	SCM1	Analog Switch 1 Common Terminal. Analog input to mux.
16	SNC1	Analog Switch 1 Normally Closed Terminal. Analog input to mux (open on POR).
17	SNO2	Analog Switch 2 Normally Open Terminal. Analog input to mux.
18	SCM2	Analog Switch 2 Common Terminal. Analog input to mux (open on POR).
19	SNC2	Analog Switch 2 Normally Closed Terminal. Analog input to mux.
20	OUT1	Amplifier 1 Output. Analog input to mux.
21	IN1-	Amplifier 1 Inverting Input. Analog input to mux.
22	IN1+	Amplifier 1 Noninverting Input
23	SWA	DACA SPST Shunt Switch Input. Connects to OUTA through a SPST switch.
24	FBA	DACA Force-Sense Feedback Input. Analog input to mux.

Pin Description (continued)

PIN	NAME	FUNCTION
25	OUTA	DACA Force-Sense Output. Analog input to mux.
26	AGND	Analog Ground
27	AVDD	Analog Supply Voltage. Also ADC reference voltage during AVDD measurement. Bypass to AGND with 10µF and 0.1µF capacitors in parallel as close to the pin as possible.
28	IN2+	Amplifier 2 Noninverting Input
29	IN2-	Amplifier 2 Inverting Input. Analog input to mux.
30	OUT2	Amplifier 2 Output. Analog input to mux.
31	AIN2	Analog Input 2. Analog input to mux. Inputs have internal programmable current source for external temperature measurement.
32	AIN1	Analog Input 1. Analog input to mux. Inputs have internal programmable current source for external temperature measurement.
33	REF	Reference Input/Output. Output of the reference buffer amplifier or external reference input. Disabled at power-up to allow external reference. Reference voltage for ADC and DAC.
34	REG	Linear Voltage-Regulator Output. Charge-pump-doubler input voltage. Bypass REG with a 10µF capacitor to DGND for charge-pump regulation.
35	CF-	Charge-Pump Flying Capacitor Terminals. Connect an external 10µF (typ) capacitor between CF+ and CF-.
36	CF+	
37	CPOUT	Charge-Pump Output. Connect an external 10µF (typ) reservoir capacitor between CPOUT and DGND. There is a low threshold diode between DVDD and CPOUT. When the charge pump is disabled, CPOUT is pulled up within 300mV (typ) of DVDD.
38	DVDD	Digital Supply Voltage. Bypass to DGND with 10µF and 0.1µF capacitors in parallel as close to the pin as possible.
39	DGND	Digital Ground. Also ground for cascaded linear voltage regulator and charge-pump doubler.
40	UPIO1	User-Programmable Input/Output 1. See the *UPIO1_CTRL Register* for functionality.
—	EP	Exposed Pad. Leave unconnected or connect to AGND.

Detailed Description

The MAX11359A DAS features a multiplexed differential 16-bit ADC, 10-bit force-sense DACs, an RTC with an alarm, a selectable bandgap voltage reference, a signal-detect comparator, 1.8V and 2.7V voltage monitors, and wake-up control circuitry, all controlled by a 4-wire serial interface (See Figure 3 for the functional diagram).

The DAS directly interfaces to various sensor outputs and, once configured, provides the stimulus, signal conditioning, and data conversion, as well as µP support. See the *Applications* section for sample MAX11359A applications.

The 16-bit ADC features programmable continuous conversion rates as shown in Table 4, and gains of 1, 2, 4, and 8 (Table 5) to suit applications with different power

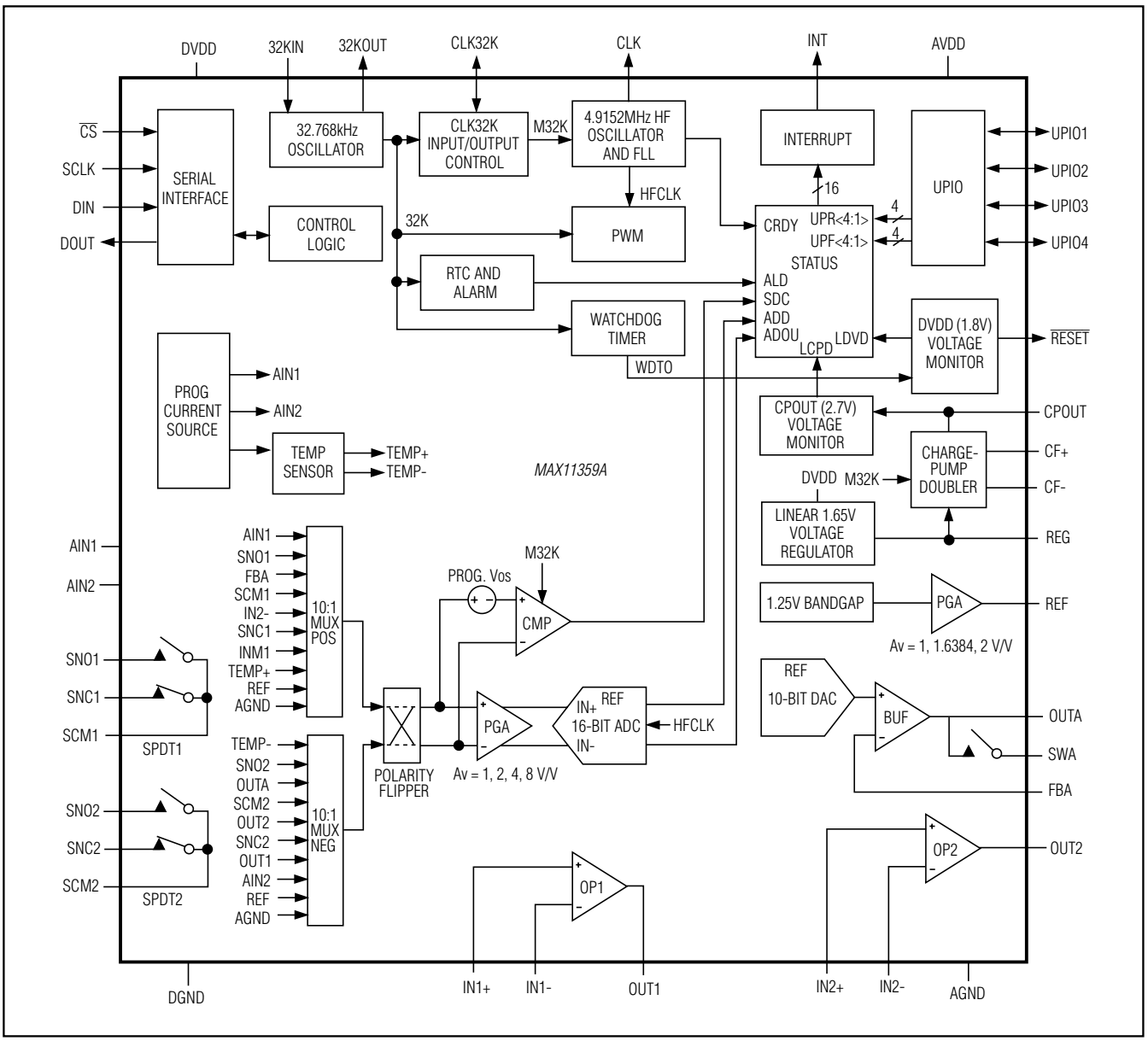


Figure 3. MAX11358B Functional Diagram

and dynamic range constraints. The force-sense DAC provides 10-bit resolution for precise sensor applications. The ADC and DACs both utilize a low-drift 1.25V internal bandgap reference for conversions and full-scale range setting. The RTC has a 138-year range and provides an alarm function that can be used to wake up the system or cause an interrupt at a predefined time. The power-supply voltage monitor detects when DVDD falls below a trip threshold voltage of +1.8V and asserts $\overline{\text{RESET}}$. The MAX11359A uses a 4-wire serial interface to communicate directly between SPI, QSPI, or MICROWIRE devices for system configuration and readback functions.

Analog-to-Digital Converter (ADC)

The MAX11359A includes a sigma-delta ADC with programmable conversion rate, a PGA, and a dual 10:1 input mux. When performing continuous conversions at 10sps or single conversions at the 40sps setting (effectively 10sps due to four sample sigma-delta settling), the ADC has 16-bit noise-free resolution. The noise-free resolution drops to 10 bits at the maximum sampling rate of 512sps. Differential inputs support unipolar (between 0 and V_{REF}) and bipolar (between $\pm V_{REF}$) modes of operation. **Note:** Avoid combinations of input signal and PGA gains that exceed the reference range at the ADC input. The ADOU bit in the status register indicates if the ADC has overranged or underranged.

Zero-scale and full-scale calibrations remove offset and gain errors. Direct access to gain and zero-scale calibration registers allows system-level offset and gain calibration. The zero-scale adjustment register allows intentional positive offset skewing to preserve unipolar-mode resolution for signals that have a slight negative offset (i.e., unipolar clipping near zero can be removed). Perform ADC calibration whenever the ADC configuration, temperature, or AVDD changes. The ADC-done status can be programmed to provide an interrupt on INT or on any UPIO_.

PGA Gain

An integrated PGA provides four selectable gains: +1V/V, +2V/V, +4V/V, and +8V/V to maximize the dynamic range of the ADC. Bits GAIN1 and GAIN0 set the gain (see the *ADC Register* for more information). The PGA gain is implemented in the digital filter of the ADC.

ADC Modulator

The MAX11359A performs analog-to-digital conversions using a single-bit, 3rd-order, switched-capacitor sigma-delta modulator. The sigma-delta modulation converts the input signal into a digital pulse train whose average duty cycle represents the digitized signal information. The pulse train is then processed by a digital decimation filter. The modulator provides 2nd-order frequency shaping of the quantization noise resulting from the single-bit quantizer. The modulator is fully differential for maximum signal-to-noise ratio and minimum susceptibility to power-supply noise.

Signal-Detect Comparator

INT asserts (and remains asserted) within 30µs when the differential voltage on the selected analog inputs exceeds the signal-detect comparator trip threshold. The signal-detect comparator's differential input trip threshold (i.e., offset) is user selectable and can be programmed to the following values: 0mV, 50mV, 100mV, 150mV, or 200mV.

Analog Inputs

The ADC provides two external analog inputs: AIN1 and AIN2. The rail-to-rail inputs accept differential or single-ended voltages, or external temperature-sensing diodes. The unused op amps, switches, or DAC inputs and output pins can also be used as rail-to-rail analog inputs if the associated function is disabled.

Analog Input Protection

Internal protection diodes clamp the analog inputs to AVDD and AGND, and allow the channel input to swing from (V_{AVDD} - 0.3V) to (V_{AVDD} + 0.3V). For accurate conversions near full scale, the inputs must not exceed AV_{DD} by more than 50mV or be lower than AGND by 50mV. If the inputs exceed (V_{AGND} - 0.3V) to (V_{AVDD} + 0.3V), limit the current to 50mA.

Analog Mux

The MAX11359A includes a dual 10:1 mux for the positive and negative inputs of the ADC. Figure 3 illustrates which signals are present at the inputs of each mux for the MAX11359A. The MUXP[3:0] and MUXN[3:0] bits of the mux register select the input to the ADC and the signal-detect comparator (Tables 8 and 9). See the mux register description in the *Register Definitions* section for multiplexer functionality. The POL bit of the ADC register swaps the polarity of mux output signals to the ADC.

Digital Filtering

The MAX11359A contains an on-chip digital lowpass filter that processes the data stream from the modulator using a SINC4 (sinx/x)4 response. The SINC4 filter has a settling time of four output data periods (4 x 200ms).

The MAX11359A has 25% overrange capability built into the modulator and digital filter:

$$H(f) = \left[\frac{1}{N}\frac{SIN\left(N\pi\frac{f}{f_m}\right)}{SIN\left(\pi\frac{f}{f_m}\right)}\right]^4$$

Figure 4 shows the filter frequency response. The SINC4 characteristic -3dB cutoff frequency is 0.228 times the first notch frequency.

The output data rate for the digital filter corresponds with the positioning of the first notch of the filter's frequency response. The notches of the SINC4 filter are repeated at multiples of the first notch frequency. The SINC4 filter provides an attenuation of better than 100dB at these notches. For example, 50Hz is equal to five times the first notch frequency and 60Hz is equal to six times the first notch frequency.

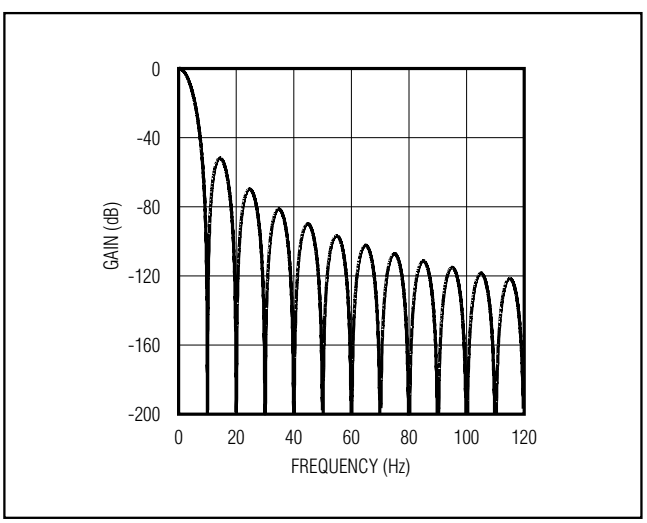


Figure 4. Filter Frequency Response

Force-Sense DAC

The MAX11359A incorporates a 10-bit force-sensing DAC. The DACs reference voltage sets the full-scale range. Program the DACA_OP register using the serial interface to set the output voltages of the DAC at OUTA. Connecting resistors in a voltage-divider configuration between OUTA, FBA, and GND sets a different closed-loop gain for the output amplifier (see the *Applications Information* section).

The DAC output amplifier typically settles to ±0.5 LSB from a full-scale transition within 50µs (unity gain and loaded with 10kΩ in parallel with 200pF). Loads of less than 1kΩ may degrade performance. See the *Typical Operating Characteristics* for the source-and-sink capability of the DAC output.

The MAX11359A features a software-programmable shutdown mode for the DAC. Power down DACA by clearing the DAE bits (see the *DACA_OP Register* section). DAC output OUTA goes high impedance when powered down. The DAC is normally powered down at power-on reset.

Charge Pump

The charge pump provides > 3V at CPOUT with a maximum 10mA load. Enable the charge pump through the PS_VMONS register. The charge pump is powered from DVDD. See Figures 5 and 6 for block diagrams of the charge pump and linear regulator. The charge pump is disabled at power-on reset.

An internal clock drives the charge-pump clock and ADC clock. The charge pump delivers a maximum 10mA of current to external devices. The droop and the ripple depend on the clock frequency (f_{CLK} = 32.768kHz/2), switch resistances (R_{SWITCH} = 5Ω), and the external capacitors (10µF) along with their respective ESRs, as shown below.

$$V_{DROOP} = I_{OUT}R_{OUT}$$

$$R_{OUT} = \frac{1}{f_{CLK}C_F} + 2R_{SWITCH} + 4ESR_{C_F} + ESR_{C_{CPOUT}}$$

$$V_{RIPPLE} = \frac{I_{OUT}}{f_{CLK}C_{CPOUT}} + 2I_{OUT}ESR_{C_{CPOUT}}$$

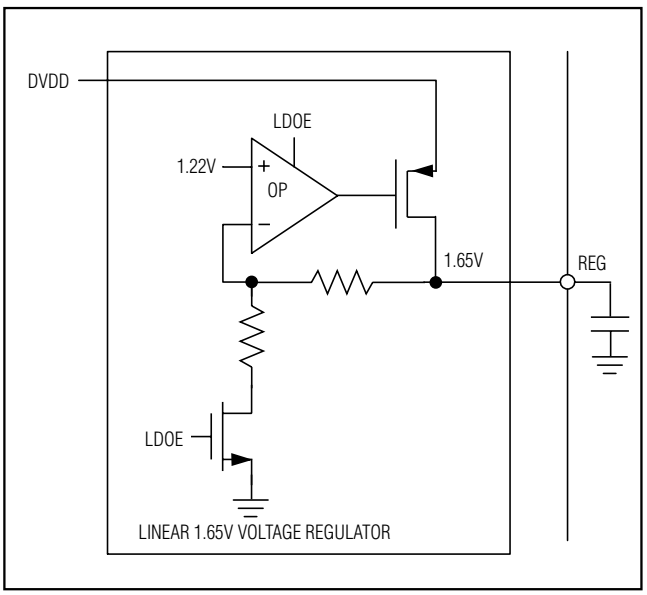


Figure 5. Linear-Regulator Block Diagram

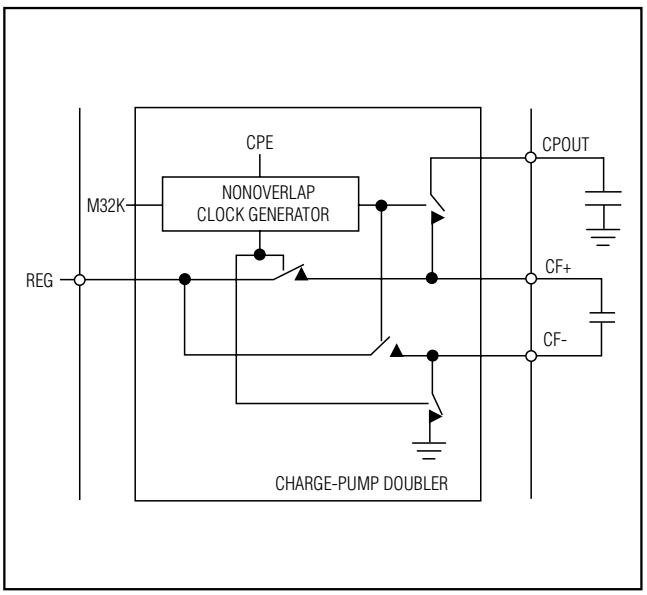


Figure 6. Charge-Pump Block Diagram

Voltage Supervisors

The MAX11359A provides voltage supervisors to monitor DVDD and CPOUT. The first supervisor monitors the DVDD supply voltage. $\overline{\text{RESET}}$ asserts and sets the corresponding LDVD status bit when DVDD falls below the 1.8V threshold voltage. When the DVDD supply voltage rises above the threshold during power-up, $\overline{\text{RESET}}$ deasserts after a nominal 1.5s timeout period to give the crystal oscillator time to stabilize. Set the threshold hysteresis using the HYSE bit of the PS_VMONS register. See the *PS_VMONS Register* section for configuring hysteresis. There is no separate voltage monitor for AVDD, but the analog supply is covered by the DVDD monitor in many applications where DVDD and AVDD are externally connected together. Multiple supply applications where AVDD and DVDD are not connected together require a separate external voltage monitor for AVDD. See Figure 7 for a block diagram of the DVDD voltage supervisor.

The second voltage monitor tracks the charge-pump output voltage, CPOUT. If CPOUT falls below the 2.7V threshold, a corresponding register status bit (LCPD) is set to flag the condition. The CPOUT monitor output can also be mapped to the interrupt generator and output on INT. The CPOUT monitor can be used as a 3V AVDD monitor in applications where the charge pump is disabled and CPOUT is connected to AVDD. AVDD must be greater or equal to DVDD when CPOUT is used to monitor AVDD. See Figure 8 for a block diagram of the CPOUT voltage supervisor.

Interrupt Generator (INT)

The interrupt generator provides an interrupt to an external µC. The source of the interrupt is generated by the status register and can be masked and unmasked through the IMSK register. CRDY is unmasked by default, and INT is active-high at power-on reset. INT is programmable as active-high and active-low. Possible sources include a rising or falling edge of UPIO_, an RTC alarm, an ADC conversion completion, or the voltage-supervisor outputs. The interrupt causes INT to assert when configured as an interrupt output.

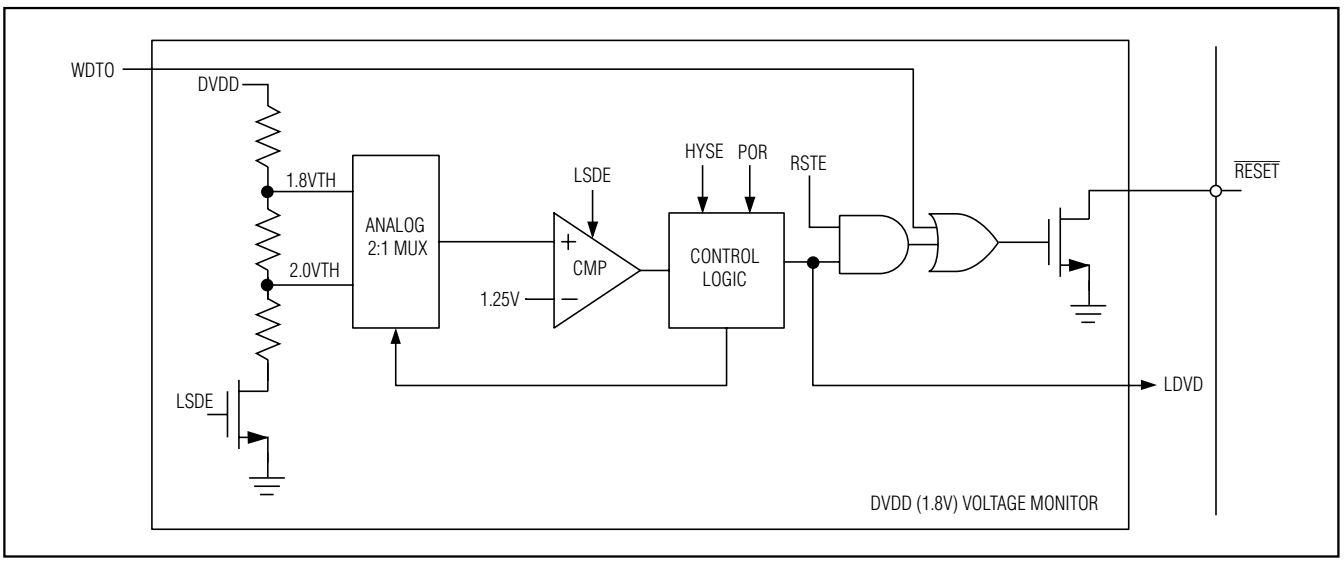


Figure 7. DVDD Voltage-Supervisor Block Diagram

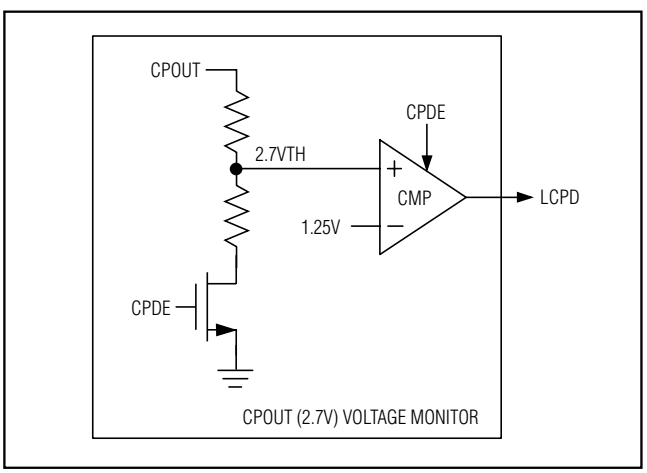


Figure 8. CPOUT Voltage-Supervisor Block Diagram

Crystal Oscillator

The on-chip oscillator requires an external crystal (or resonator) connected between 32KIN and 32KOUT with a 32.768kHz operating frequency. This oscillator is used for the RTC, alarm, PWM, watchdog, charge pump, and FLL. In any crystal-based oscillator circuit, the oscillator frequency is sensitive to the capacitive load (C_L). C_L is the capacitance that the crystal needs from the oscillator circuit and not the capacitance of the crystal. The input capacitance across 32KIN and 32KOUT is 6pF. Choose a crystal with a 32.768kHz oscillation frequency and a 6pF capacitive load such as the C-002RX32-E from Epson Crystal. Using a crystal with a C_L that is larger than the load capacitance of the oscillator circuit causes the oscillator to run faster than the specified nominal frequency of the crystal or to not start up. See Figures 9 and 10 for block diagrams of the crystal oscillator and the CLK32K I/O.

Real-Time Clock (RTC)

The integrated RTC provides the current time information from a 32-bit counter and subsecond counts from an 8-bit ripple counter. An internally generated reference clock of 256Hz (derived from the 32.768kHz crystal) drives the 8-bit subsecond counter. An overflow of the 8-bit subsecond counter inputs a 1Hz clock to increment the 32-bit second counter. The RTC 32-bit second counter is translatable to calendar format with firmware. All 40 bits (32-bit second counter and 8-bit subsecond counter) must be clocked in or out for valid data. The RTC and the 32.768kHz crystal oscillator consume less than 1µA when the rest of the device is powered down.

Time-of-Day Alarm

Program the AL_DAY register with a 20-bit value, which corresponds to a time 1s to 12 days later than the current time with a 1s resolution. The alarm status bit, ALD, asserts when the 20 bits of the AL_DAY register matches the 20 LSBs of the 32-bit second counter. The ADE bit automatically clears when the time-of-day alarm trips. The time-of-day alarm causes the device to exit sleep mode.

Watchdog

Enable the watchdog timer by writing a 1 to the WDE bit in the CLK_CTRL register. After enabling the watchdog timer, the device asserts $\overline{RESET}$ for 250ms, if the watchdog address register is not written every 500ms. Due to the asynchronous nature of the watchdog timer, the watchdog timeout period varies between 500ms and 750ms. Write a 0 to the WDE bit to disable the watchdog timer. See Figure 11 for a block diagram of the watchdog timer.

High-Frequency Clock

An internal oscillator and a frequency-locked loop (FLL) are used to generate a 4.9152MHz ±1% high-frequency clock. This clock and derivatives are used internally by the ADC, analog switches, and PWM. This clock signal outputs to CLK. When the FLL is enabled, the high-frequency clock is locked to the 32.768kHz reference. If the FLL is disabled, the high-frequency clock is free-running. At power-up, the CLK pin defaults to a 2.4576MHz clock output, which is compatible with most µCs. See Figure 12 for a block diagram of the high-frequency clock.

User-Programmable I/Os

The MAX11359A provides four digital programmable I/Os (UPIO1–UPIO4). Configure UPIOs as logic inputs or outputs using the UPIO control register. Configure the internal pullups using the UPIO setup register, if required. At power-up, the UPIOs are internally pulled up to DVDD. UPIO_ outputs can be referenced to DVDD or CPOUT. See the *UPIO__CTRL Register* and *UPIO_SPI Register* sections for more details on configuring the UPIO_ pins.

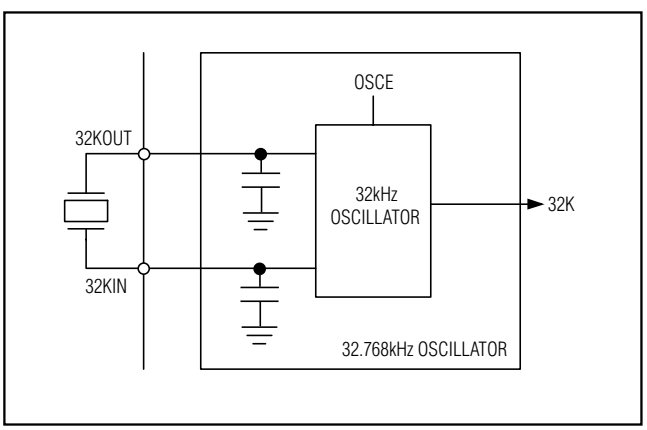


Figure 9. 32kHz Crystal-Oscillator Block Diagram

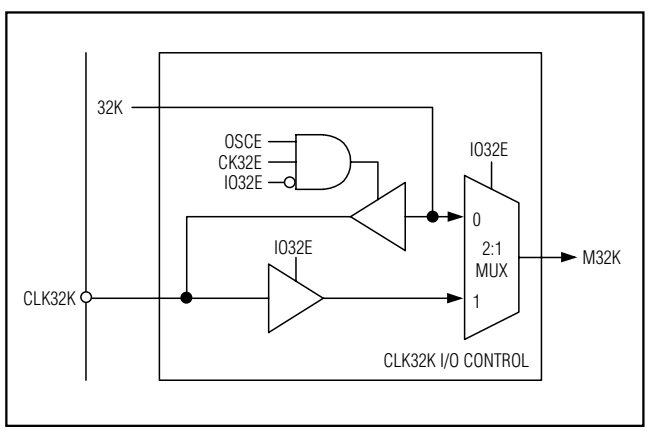


Figure 10. CLK32K I/O Block Diagram

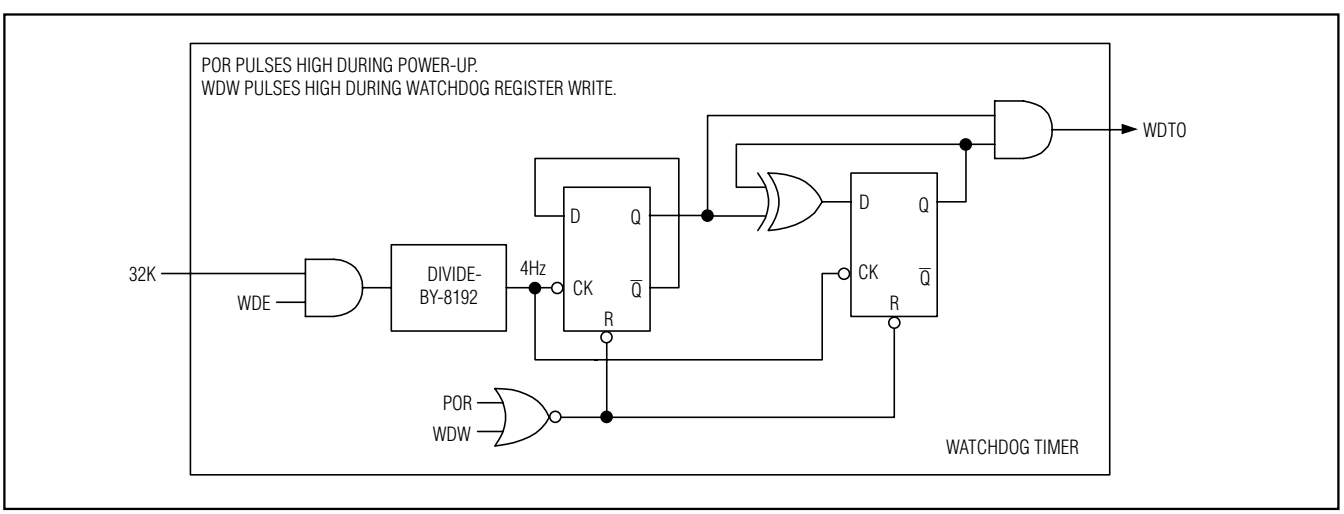


Figure 11. Watchdog Timer Block Diagram

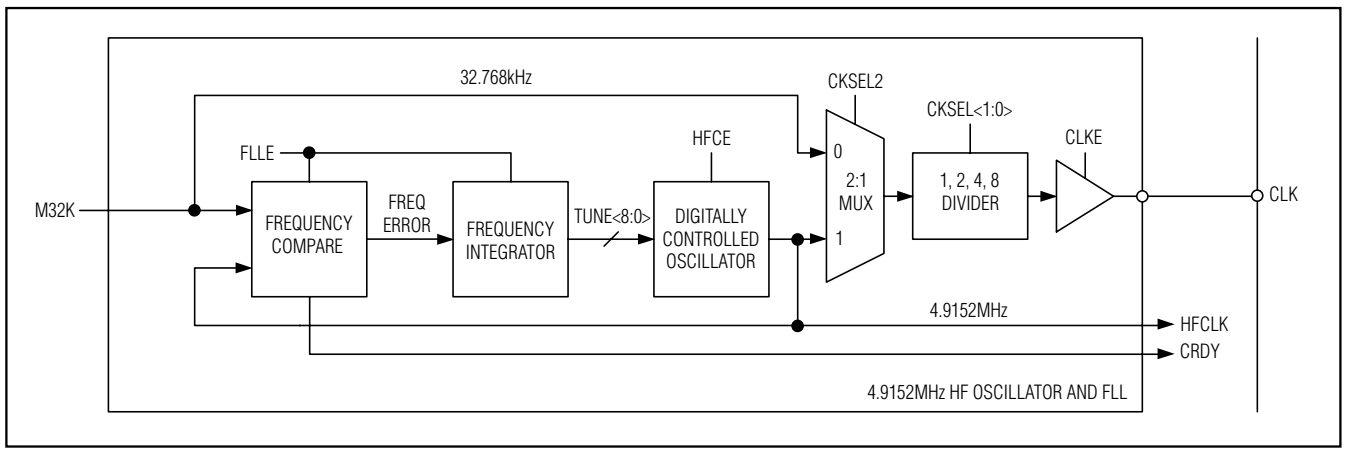


Figure 12. High-Frequency Clock and FLL Block Diagram

Program each UPIO1–UPIO4 as one of the following:

- General-purpose input
- Power-mode control
- Analog switch (SPST) and SPDT control input
- ADC data-ready output
- General-purpose output
- PWM output
- Alarm output
- SPI passthrough

Temperature Sensors

The internal temperature sensor measures die temperature, and the external temperature sensor measures remote temperatures. Use the internal temperature sensor or external temperature sensor (remote transistor/diode) with the ADC and internal current sources to measure the temperature. For either method, two to four currents are passed through a p-n junction and sense resistor, and its temperature is calculated by a µC using the diode equation and the forward-biased junction voltage drops measured by the ADC. The temperature offset between the internal p-n junction and ambient is negligible. For the four and eight measurement methods, the ratio of currents used in the diode calculations is precisely known since the ADC measures the resulting voltage across the same sense resistor. See Figure 13 for a block diagram of the temperature sensor.

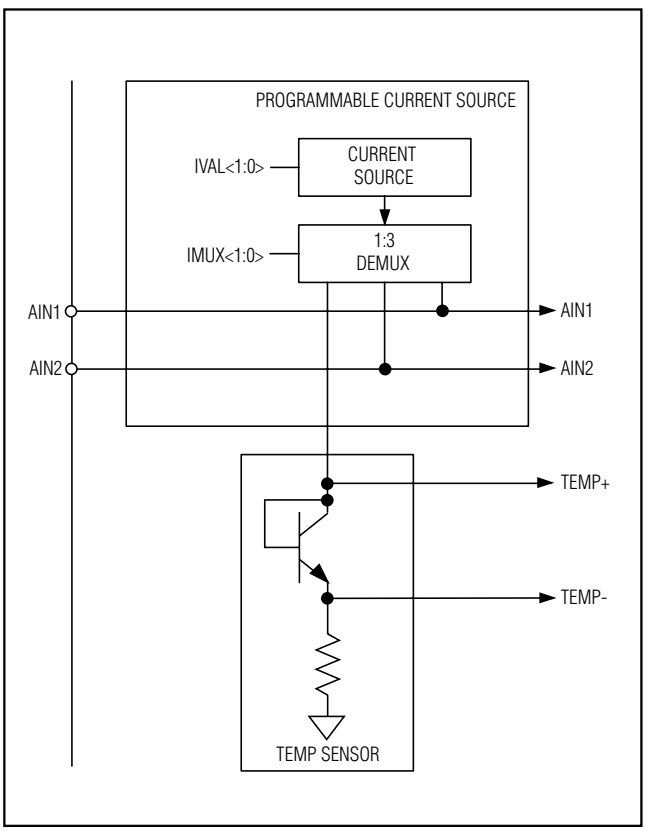


Figure 13. Temperature-Sensor Measurement Block Diagram

Two-Current Method

For the two-current method, currents I_1 and I_2 are passed through a p-n junction. This requires two V_{BE} measurements. Temperature measurements can be performed using I_1 and I_2.

$$T_{MEAS} = \frac{q(V_{BE2} - V_{BE1})}{nk\ ln\left(\frac{I_2}{I_1}\right)}$$

where k is Boltzman's constant and q is the absolute value of the charge on electron. A four-measurement procedure is adopted to improve accuracy by precisely measuring the ratio of I_1 and I_2:

1) Current I_1 is driven through the diode and the series resistor R, and the voltage across the diode is measured as V_{BE1}.
2) For the same current, the voltage across the diode and R is measured as V_1.
3) Repeat steps 1 and 2 with I_2. I_1 is typically 4µA and I_2 is typically 60µA (see Table 21).

Since only four integer numbers are accessible from the ADC conversions at a certain voltage reference, the previous equation can be represented in the following manner:

$$T_{MEAS} = \frac{q(N_{VBE2} - N_{VBE1})}{nk\ ln\left(\frac{N_{V2} - N_{VBE2}}{N_{V1} - N_{VBE1}}\right)} \times \frac{V_{REF}}{2^{16}}$$

where N_{V1}, N_{V2}, N_{VBE1}, and N_{VBE2} are the measurement results in integer format and V_{REF} is the reference voltage used in the ADC measurements.

Four-Current Method

The four-current method is used to account for the diode series resistance and trace resistance. The four currents are defined as follows; I_1, I_2, M_1I_1, and M_2I_2. If the currents are selected so $(M_1 - 1)I_1 = (M_2 - 1)I_2$, the effect of the series resistance is eliminated from the temperature measurements. For the currents I_1 = 4µA and I_2 = 60µA, the factors are selected as M_1 = 16 and M_2 = 2. This results in the currents $I_3 = M_1I_1$ = 64µA and $I_4 = M_2I_2$ = 120µA (typ). As in the case of the two-current method, two measurements per current are used to improve accuracy by precisely measuring the values of the currents.

1) Current I_1 is driven through the diode and the series resistor R, and the voltage is measured across the diode using the ADC as NVBE1.
2) For the same current, the voltage across the diode and the series resistor is measured by the ADC as NV1.
3) Repeat steps 1 and 2 with I_2, I_3, and I_4.

The measured temperature is defined as follows:

$$T_{MEAS} = \frac{q(N_{VBE3} - N_{VBE1}) - q(N_{VBE4} - N_{VBE2})}{nk\ ln\left(\frac{M_1}{M_2}\right)} \times \frac{V_{REF}}{2^{16}}$$

where V_{REF} is the reference voltage used and:

$$\frac{M_1}{M_2} = \left(\frac{N_{V3} - N_{VBE3}}{N_{V1} - N_{VBE1}}\right)\left(\frac{N_{V2} - N_{VBE2}}{N_{V4} - N_{VBE4}}\right)$$

External Temperature Sensor

For an external temperature sensor, either the two-current or four-current method can be used. Connect an external diode (such as 2N3904 or 2N3906) between pins AIN1 and AGND (or AIN2 and AGND). Connect a sense resistor R between AIN1 and AIN2. Maximize R so the IR drop plus V_{BE} of the p-n junction [(R x I_{MAX})+V_{BE}] is the smaller of the ADC reference voltage or (AVDD - 400mV). The same procedure as the internal temperature sensor can be used for the external temperature sensor, by routing the currents to AIN1 (or AIN2) (see Table 20).

For the two-current method, if the external diode's series resistance (R_S) is known, then the temperature measurement can be corrected as shown below:

$$T_{ACTUAL} = T_{MEAS} - \left(\frac{q(N_{V2} - N_{VBE2}) - q(N_{V1} - N_{VBE1})}{nk\ ln\left(\frac{N_{V2} - N_{VBE2}}{N_{V1} - N_{VBE1}}\right)} \times \frac{V_{REF}}{2^{16}} \times \frac{R_S}{R}\right)$$

Temperature-Sensor Calibration

To account for various error sources during the temperature measurement, the internal temperature sensor is calibrated at the factory. The calibrated temperature equation is:

$$T_A = g \times T_{MEAS} + b$$

where g and b are the gain and offset calibration values, respectively. These calibration values are available for reading from the TEMP_CAL register.

Voltage Reference and Buffer

An internal 1.25V bandgap reference has a buffer with a selectable 1.0V/V, 1.638V/V, or 2.0V/V gain, resulting in nominally 1.25V, 2.048V, or 2.5V reference voltage at REF. The ADC and DAC use this reference voltage. The state of the internal voltage reference output buffer at POR is disabled so it can be driven, at REF, with an external reference between AGND and AVDD. The MAX11359A reference has an initial tolerance of ±1%. Program the reference buffer through the serial interface. Bypass REF with a 4.7µF capacitor to AGND.

Operational Amplifiers (Op Amps)

The MAX11359A includes two op amps. These op amps feature rail-to-rail outputs, near rail-to-rail inputs, and have an 80kHz (1nF load) input bandwidth. The DACA_OP (DACB_OP) register controls the power state of the op amps. When powered down, the outputs of the op amps are high impedance.

Single-Pole/Double-Throw (SPDT) Switches

The MAX11359A provides two uncommitted SPDT switches. Each switch has a typical on-resistance of 35Ω. Control the switches through the SW_CTRL register, the PWM output, and/or a UPIO port configured to control the switches (UPIO1–UPIO4_CTRL register).

Pulse-Width Modulator (PWM)

A single 8-bit PWM is available for various system tasks such as LCD bias control, sensor bias voltage trim, buzzer drive, and duty-cycled sleep-mode power-control schemes. PWM input clock sources include the 4.9512MHz FLL output, the 32kHz clock, and frequency-divided versions of each. Although most µCs have built-in PWM functions, the MAX11359A PWM is more flexible by allowing the UPIO outputs to be driven to DVDD or regulated CPOUT logic-high voltage levels. For duty-cycled power-control schemes, use the 32kHz-derived input clock. The PWM output is available independent of µC power state. The FLL is typically disabled in sleep-override mode.

Serial Interface

The MAX11359A features a 4-wire serial interface consisting of a chip select ($\overline{CS}$), serial clock (SCLK), data in (DIN), and data out (DOUT). $\overline{CS}$ must be low to allow data to be clocked into or out of the device. DOUT is high impedance while $\overline{CS}$ is high. The data is clocked in at DIN on the rising edge of SCLK. Data is clocked out at DOUT on the falling edge of SCLK. The serial interface is compatible with SPI modes CPOL = 0, CPHA = 0 and CPOL = 1, CPHA = 1. A write operation to the MAX11359A takes effect on the last rising edge of SCLK. If $\overline{CS}$ goes high before the complete transfer, the write is ignored. Every data transfer is initiated by the command byte. The command byte consists of a start bit (MSB), R/$\overline{W}$ bit, and 6 address bits. The start bit must be 1 to perform data transfers to the device. Zeros clocked in are ignored. For SPI passthrough mode, see the *UPIO_SPI Register* section. An address byte identifies each register. Table 4 shows the complete register address map for this family of DAS. Figures 14, 15, and 16 provide timing diagrams for read and write commands.

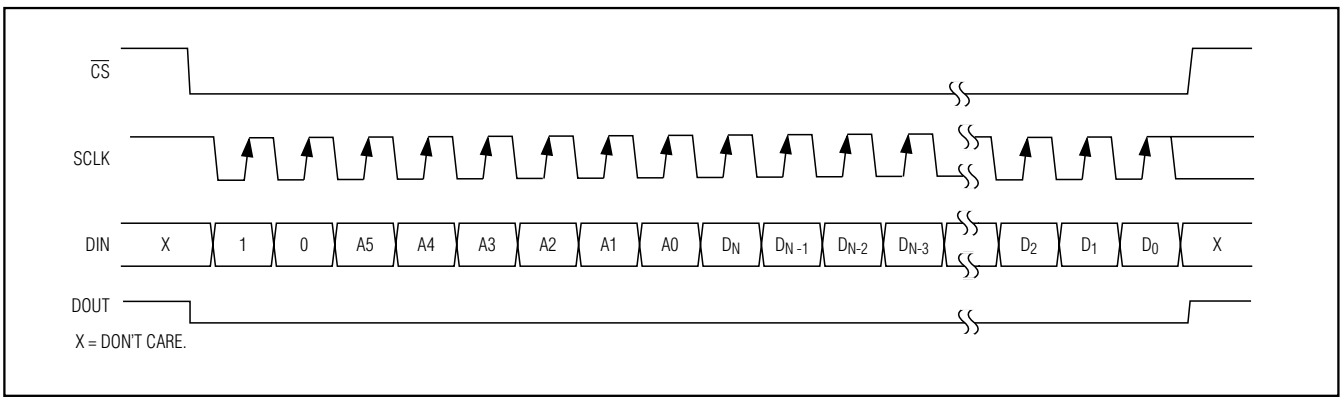


Figure 14. Serial-Interface Register Write with 8-Bit Control Word, Followed by a Variable Length Data Write

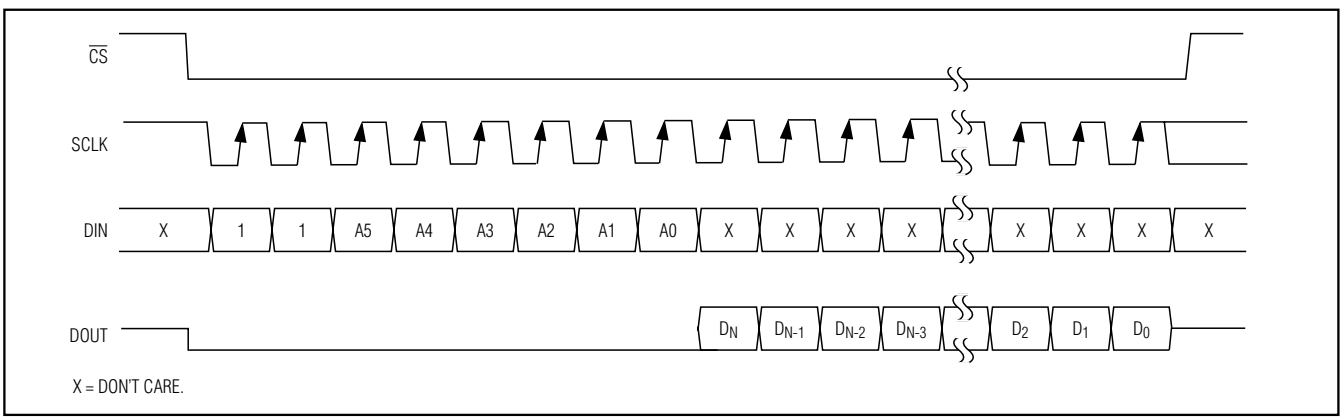


Figure 15. Serial-Interface Register Read with 8-Bit Control Word Followed by a Variable Length Data Read

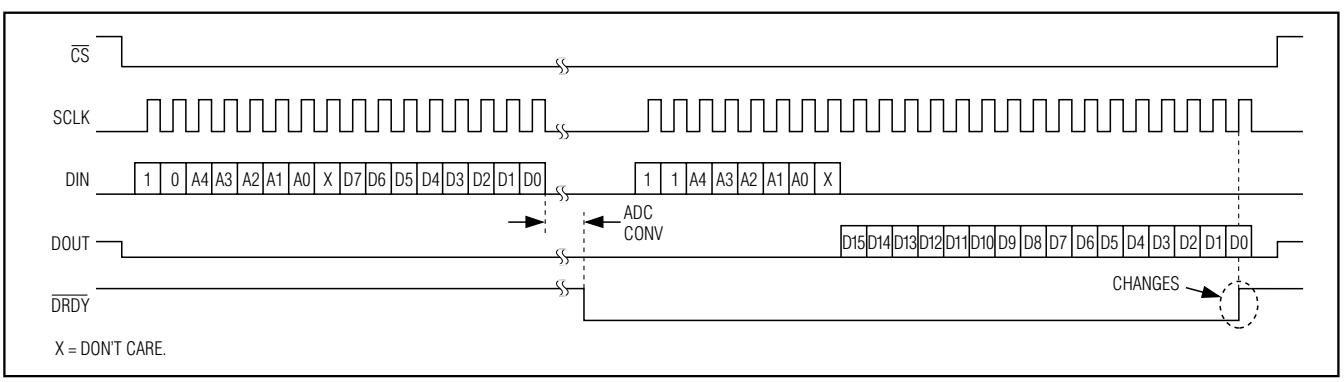


Figure 16. Performing an ADC Conversion ($\overline{DRDY}$ Function can be Accessed at UPIO Pins)

Register Definitions

Table 4. Register Address Map

REGISTER NAME	START	CTL (R/W)	ADR<5:0> (ADDRESS)						D<39:0>, D<23:0>, D<15:0> OR D<7:0> (DATA)							
ADC	1	R/W	0	0	0	0	0	X	ADCE	STRT	BIP	POL	CONT	ADCREF	GAIN<1:0>	
									RATE<2:0>			MODE<2:0>			X	X
MUX	1	R/W	0	0	0	0	1	S	MUXP<3:0>				MUXN<3:0>			
DATA	1	R	0	0	0	1	0	X	ADC<15:0>							
OFFSET CAL	1	R/W	0	0	0	1	1	X	Offset<23:0>							
GAIN CAL	1	R/W	0	0	1	0	0	X	Gain<23:0>							
RESERVED	1	R/W	0	0	1	0	1	X	Reserved. Do not use.							
DACA_OP	1	R/W	0	0	1	1	0	X	DAE/ OP3E	DBE/ OP2E	OP1E	X	X	X	DACA<9:8>	
									DACA<7:0>							
DACB_OP	1	R/W	0	0	1	1	1	X	DAE/ OP3E	DBE/ OP2E	OP1E	X	X	X	DACB<9:8>	
									DACB<7:0>							
REF_SDC	1	R/W	0	1	0	0	0	X	REFV<1:0>		AOFF	AON	SDCE	TSEL<2:0>		
AL_DAY	1	R/W	0	1	0	0	1	X	ASEC<19:4>							
									ASEC<3:0>				X	X	X	X
AL_SYS	1	R/W	0	1	0	1	0	X	ASUB<7:0>							
CLK_CTRL	1	R/W	0	1	0	1	1	X	AWE	ADE	ASE	RWE	RTCE	OSCE	FLLE	HFCE
									CKSEL<2:0>			IO32E	CK32E	CLKE	INTP	WDE
RTC	1	R/W	0	1	1	0	0	X	SEC<31:0>							
									SUB<7:0>							
PWM_CTRL	1	R/W	0	1	1	0	1	X	PWME	FSEL<2:0>			SWAH	SWAL	SWBH	SWBL
									SPD1	SPD2	X	X	X	X	X	X
PWM_THTP	1	R/W	0	1	1	1	0	X	PWMTH<7:0>							
									PWMTP<7:0>							
WATCHDOG	1	W	0	1	1	1	1	X	X	X	X	X	X	X	X	X
ON MODE	1	W	1	0	0	0	0	X	X	X	X	X	X	X	X	X
SLEEP_OVRR	1	W	1	0	0	0	1	X	X	X	X	X	X	X	X	X
SLEEP_CFG	1	R/W	1	0	0	1	0	SLP	SOSCE	SCK32E	SPWME	SHDN	X	X	X	X
UPIO4_CTRL	1	R/W	1	0	0	1	1	X	UP4MD<3:0>				PUP4	SV4	ALH4	LL4
UPIO3_CTRL	1	R/W	1	0	1	0	0	X	UP3MD<3:0>				PUP3	SV3	ALH3	LL3
UPIO2_CTRL	1	R/W	1	0	1	0	1	X	UP2MD<3:0>				PUP2	SV2	ALH2	LL2
UPIO1_CTRL	1	R/W	1	0	1	1	0	X	UP1MD<3:0>				PUP1	SV1	ALH1	LL1
UPIO_SPI	1	R/W	1	0	1	1	1	X	UP4S	UP3S	UP2S	UP1S	X	X	X	X
SW_CTRL	1	R/W	1	1	0	0	0	X	SWA	SWB	SPDT1<1:0>		SPDT2<1:0>		X	X
TEMP_CTRL	1	R/W	1	1	0	0	1	X	IMUX<1:0>		IVAL<1:0>		X	X	X	X
TEMP_CAL	1	R	1	1	0	1	0	X	TGAIN<7:0> TOFFS<7:0>							
IMSK	1	R/W	1	1	0	1	1	X	MLDVD	MLCP	MADO	MSDC	MCRD	MADD	MALD	MALS
									MUPR<4:1>				MUPF<4:1>			
RESERVED	1	R/W	1	1	1	0	0	X	Reserved. Do not use.							
PS_VMONS	1	R/W	1	1	1	0	1	X	LDOE	CPE	LSDE	CPDE	HYSE	RSTE	X	X
STATUS	1	R	1	1	1	1	1	X	LDVD	LCPD	ADOU	SDC	CRDY	ADD	ALD	ALS
									UPR<4:1>				UPF<4:1>			

X = Don't care.

Register Bit Descriptions

ADC Register (Power-On State: 0000 0000 0000 00XX)

MSB						LSB	
ADCE	STRT	BIP	POL	CONT	ADCREF	GAIN<1:0>	
RATE<2:0>			MODE<2:0>			X	X

The ADC register configures the ADC and starts a conversion.

ADCE: ADC power-enable bit. ADCE = 1 powers up the ADC, and ADCE = 0 powers down the ADC.

STRT: ADC start bit. STRT = 1 resets the registers inside the ADC filter and initiates a conversion or calibration. The conversion begins immediately after the 16th ADC control bit is clocked by the rising edge of SCLK. The initial conversion requires four conversion cycles for valid output data. If CONT = 0 when STRT is asserted, the ADC stops after a single conversion and holds the result in the DATA register. If CONT = 1 when STRT is asserted, the ADC performs continuous conversions at the rate specified by the RATE<2:0> bits until CONT is deasserted or ADCE is deasserted, powering down the ADC. The STRT bit is automatically deasserted after the initial conversion is complete (four conversion cycles; the ADC status bit ADD in the STATUS register asserts.) The current ADC configurations are not affected if the ADC register is written with STRT = 0. This allows the ADC and mux configurations to be updated simultaneously with the S bit in the MUX register.

BIP: Unipolar/bipolar bit. Set BIP = 0 for unipolar mode and BIP = 1 for bipolar mode. Unipolar-mode data is unsigned binary format and bipolar is two's complement. See the *ADC Transfer Functions* section for more details.

POL: Polarity flipper bit. POL = 1 flips the polarity of the differential signal to the ADC and the input to the signal-detect comparator (SDC). POL = 0 sets the positive mux output to the positive ADC and SDC inputs, and the negative mux output to the negative ADC and SDC inputs. POL = 1 sets the positive mux output to the negative ADC and SDC inputs, and the negative mux output to the positive ADC and SDC inputs.

CONT: Continuous conversion bit. CONT = 1 enables continuous conversions following completion of the first conversion or calibration(s) initiated by the STRT or S bit. Set CONT = 0 while asserting the STRT bit, or prior to asserting the S bit to perform a single conversion or to prevent conversions following a calibration. Set CONT = 0 to abort continuous conversions already in progress. When the ADC is stopped in this way, the last complete conversion result remains in the DATA register and the internal ADC state information is lost. Asserting the CONT bit does not restart the ADC, but results in continuous conversions once the ADC is restarted with the STRT or S bit.

ADCREF: ADC reference source bit. Set ADCREF = 0 to select REF as the ADC reference. Set ADCREF = 1 to select AVDD as the ADC reference. To measure the AVDD voltage without having to attenuate the supply voltage, select REF and AGND as the differential inputs to the ADC, with POL = 0 and while ADCREF = 1.

GAIN<1:0>: ADC gain-setting bits. These two bits select the gain of the ADC as shown in Table 5.

Table 5. Setting the Gain of the ADC

GAIN SETTING (V/V)	GAIN1	GAIN0
1	0	0
2	0	1
4	1	0
8	1	1

Table 6a. Setting the ADC Conversion Rate*

CONTINUOUS CONVERSION RATE (sps)	SINGLE CONVERSION RATE (sps)	RATE2	RATE1	RATE0
10	2.5	0	0	0
40	10	0	0	1
50	12.5	0	1	0
60	15	0	1	1
200	50	1	0	0
240	60	1	0	1
400	100	1	1	0
512	128	1	1	1

Table 6b. Actual ADC Conversion Rates

NOMINAL CONTINUOUS CONVERSION RATE (sps)	DECIMATION RATIO	ACTUAL CONTINUOUS CONVERSION RATE (sps)
10	1096	10.01042142
40	274	40.04168568
50	220	49.87009943
60	183	59.953125
200	55	199.4803977
240	46	238.5091712
400	27	406.3489583
512	23	477.0183424

*Calculate the ADC sampling rate using the following equation:

$$f_S = \frac{f_{HFCLK}}{448 \times \text{decimation ratio}}$$

where f_{HFCLK} = 4.9152MHz nominally.

RATE<2:0>: ADC conversion-rate-setting bits. These three bits set the conversion rate of the ADC as shown in Table 6. The initial conversion requires four conversion cycles for valid data, and subsequent conversions require only one cycle (if CONT = 1). A full-scale input change can require up to five cycles for valid data if the digital filter is not reset with the STRT or S bit.

MODE<2:0>: Conversion-mode bits. These three bits determine the type of conversion for the ADC as shown in Table 7. When the ADC finishes an offset calibration and/or gain calibration, the MODE<2:0> bits clear to 0 hex, the ADD bit in the STATUS register asserts, and an interrupt asserts on INT (or UPIO_ if programmed as DRDY) if MADD is unmasked. Perform a gain calibration after achieving the desired offset (calibrated or not). If an offset and gain calibration are performed together (MODE<2:0> = 7 hex), the offset calibration is performed first followed by the gain calibration, and the µC is interrupted by INT (or UPIO_ if programmed as DRDY) if MADD is unmasked only upon completion of both offset and gain calibration. After power-on or calibration, the ADC does not begin conversions until initiated by the user (see the ADCE and STRT bit descriptions in this section and see the S bit descriptions in the *MUX Register* section). See the *GAIN CAL Register* and *OFFSET CAL Register* sections for details on system calibration.

Table 7. Setting the ADC Conversion Mode

CONVERSION MODE	MODE2	MODE1	MODE0
Normal	0	0	0
System Offset Calibration	0	0	1
System Gain Calibration	0	1	0
Normal	0	1	1
Normal	1	0	0
Self Offset Calibration	1	0	1
Self Gain Calibration	1	1	0
Self Offset and Gain Calibration	1	1	1

MUX Register (Power-On State: 0000 0000)

MSB								LSB
S (ADR0)	MUXP3	MUXP2	MUXP1	MUXP0	MUXN3	MUXN2	MUXN1	MUXN0

The MUX register configures the positive and negative mux inputs and can start an ADC conversion.

S (ADR0): Conversion start bit. The S bit is the LSB of the MUX register address byte. S = 1 resets the registers inside the ADC filter and initiates a conversion or calibration. The conversion begins immediately after the eighth MUX register data bit, when S = 1 and when writing to the MUX register. This allows the new MUX and ADC register settings to take effect simultaneously for a new conversion, if STRT = 0 during the last write to the ADC register. If the S bit is asserted and the command is a read from the MUX register, the conversion starts immediately after the S bit (ADR0) is clocked in by the rising edge of SCLK.

Read the MUX register with S = 1 for the fastest method of initiating a conversion because only 8 bits are required. The subsequent MUX register read is valid, but can be aborted by raising $\overline{CS}$ with no harmful side effects. The initial conversion requires four conversion cycles for valid output data. If CONT = 0 and S = 1, the ADC stops after a single conversion and holds the result in the DATA register. If CONT = 1 and S = 1, the ADC performs continuous conversions at the rate specified by the RATE<2:0> bits until CONT deasserts or ADCE deasserts, powering down the ADC. When a conversion initiates using the S bit, the STRT bit asserts and deasserts automatically after the initial conversion completes. Writing to the MUX register with S = 0 causes the MUX settings to change immediately and the ADC continues in its prior state with its settings unaffected. When the ADC is powered down, MUX inputs are open.

MUXP<3:0>: MUX positive input bits. These four bits select one of ten inputs from the positive MUX to go to the positive output of the MUX as shown in Table 8. Any writes to the MUX register take effect immediately once the LSB (MUXN0) is clocked by the rising edge of SCLK.

MUXN<3:0> MUX negative input bits. These four bits select one of ten inputs from the negative MUX to go to the negative output of the MUX as shown in Table 9. Any writes to the MUX register take effect immediately once the LSB (MUXN0) is clocked by the rising edge of SCLK.

The DATA register contains the data from the most recently completed conversion.

The OFFSET CAL register contains the 24-bit data of the most recently completed offset calibration.

Table 8. Selecting the Positive MUX Inputs

POSITIVE MUX INPUT	MUXP3	MUXP2	MUXP1	MUXP0
AIN1	0	0	0	0
SNO1	0	0	0	1
FBA	0	0	1	0
SCM1	0	0	1	1
IN2-	0	1	0	0
SNC1	0	1	0	1
IN1-	0	1	1	0
TEMP+	0	1	1	1
REF	1	0	0	0
AGND	1	0	0	1
Open	1	0	1	X
	1	1	X	X

X = Don't care.

Table 9. Selecting the Negative MUX Inputs

NEGATIVE MUX INPUT	MUXN3	MUXN2	MUXN1	MUXN0
TEMP-	0	0	0	0
SNO2	0	0	0	1
OUTA	0	0	1	0
SCM2	0	0	1	1
OUT2	0	1	0	0
SNC2	0	1	0	1
OUT1	0	1	1	0
AIN2	0	1	1	1
REF	1	0	0	0
AGND	1	0	0	1
Open	1	0	1	X
	1	1	X	X

X = Don't care.

DATA Register (Power-On State: 0000 0000 0000 0000)

MSB							
ADC15	ADC14	ADC13	ADC12	ADC11	ADC10	ADC9	ADC8
						LSB	
ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0

ADC<15:0> Analog-to-digital conversion data bits. These 16 bits are the results from the most recently completed conversion. The data format is unsigned; binary for unipolar mode, and two's complement for bipolar mode.

OFFSET CAL Register (Power-On State: 0000 0000 0000 0000 0000 0000)

MSB							
OFFSET23	OFFSET22	OFFSET21	OFFSET20	OFFSET19	OFFSET18	OFFSET17	OFFSET16
OFFSET15	OFFSET14	OFFSET13	OFFSET12	OFFSET11	OFFSET10	OFFSET9	OFFSET8
							LSB
OFFSET7	OFFSET6	OFFSET5	OFFSET4	OFFSET3	OFFSET2	OFFSET1	OFFSET0

OFFSET<23:0>: Offset-calibration bits. The data format is two's complement and is subtracted from the ADC output before being written to the DATA register. The offset calibration allows input offset errors between V_{REF} ±50% to be corrected in unipolar or bipolar mode. The MAX11359A can perform system offset calibration or self offset calibration. Self-calibration performs a calibration for the entire signal path. See the *ADC Calibration* section for more details.

The ADC input voltage range specifications must always be obeyed, and the OFFSET CAL register effectively offsets the ADC digital scale to a "zero" value determined by the calibration.

GAIN CAL Register (Power-On State: 1000 0000 0000 0000 0000 0000)

MSB							
GAIN23	GAIN22	GAIN21	GAIN20	GAIN19	GAIN18	GAIN17	GAIN16
GAIN15	GAIN14	GAIN13	GAIN12	GAIN11	GAIN10	GAIN9	GAIN8
							LSB
GAIN7	GAIN6	GAIN5	GAIN4	GAIN3	GAIN2	GAIN1	GAIN0

GAIN<23:0>: Gain-calibration bits. The data format is unsigned binary with 23 bits to the right of the decimal point and scales the ADC output before being written to the DATA register. The gain calibration allows full-scale errors between $-V_{REF}/2$ and $+V_{REF}/2$ to be corrected in unipolar mode, and full-scale errors between (+50% x V_{REF}) and (+200% x V_{REF}) in unipolar or bipolar mode. The MAX11359A can perform system gain calibration or self gain calibration. Self-calibration performs a calibration for offsets in the ADC, and system calibration performs a calibration for the entire signal path. See the *ADC Calibration* section for more details.

The ADC input voltage range specifications must always be obeyed, and the GAIN CAL register effectively scales the ADC digital output to a full-scale value determined by the calibration. The usable gain-calibration range is limited to less than the full GAIN CAL register digital-scaling range by the internal noise of the ADC.

DACA_OP Register (Power-On State: 000X XX00 0000 0000)

MSB							
DAE	DBE	OP1E	X	X	X	DACA9	DACA8
							LSB
DACA7	DACA6	DACA5	DACA4	DACA3	DACA2	DACA1	DACA0

DACA_OP Register

Writing to the DACA_OP output register updates DACA on the rising SCLK edge of the LSB data bit. The output voltage can be calculated as follows:

$$V_{OUTA} = V_{REF} \times N/2^{10}$$

where:

V_{REF} is the reference voltage for the DAC.

N is the integer value of the DACA<9:0> output register. The output buffer is in unity gain.

The DACA data is 10 bits long and right justified.

DAE: DACA enable bit. Set DAE = 1 to power up the DACA and the DACA output buffer in the MAX11359A.

OP2E: OP2 power-enable bit. Set OP2E = 1 to power up OP2 in the MAX11359A.

OP1E: OP1 power-enable bit. Set OP1E = 1 to power up OP1 in the MAX11359A. This bit is mirrored in the DACB_OP register.

DACA<9:0>: DACA data bits.

REF_SDC Register (Power-On State: 0000 0000)

MSB							LSB
REFV1	REFV0	AOFF	AON	SDCE	TSEL2	TSEL1	TSEL0

The REF_SDC register contains bits to control the reference voltage and signal-detect comparator.

REFV<1:0>: Reference buffer voltage gain and enable bits. Enables the output buffer, sets the gain and the voltage at the REF pin as shown in Table 10. Power-on state is off to enable an external reference to drive the REF pin without contention.

AOFF: ADC and DAC/op-amp power-off bit. This bit provides a method for turning off several analog functions with a single write. Setting AOFF = 1 deasserts the ADCE in the ADC register and DAE/OP3E, OP2E, and OP1E bits in the DACA_OP registers, powering down these analog blocks. Setting AOFF = 0 has no effect. The AON bit has priority when both AON and AOFF bits are asserted.

Most of the analog functions can be disabled with a single write to the REF_SDC register by using AOFF, REFV<1:0>, and SDCE.

Table 10. Setting the Reference Output Voltage

REFERENCE BUFFER GAIN (V/V)	REF OUTPUT VOLTAGE (V)	REFV1	REFV0
Disabled	Off (High Impedance at REF)	0	0
1.0	1.251	0	1
1.638	1.996	1	0
2.0	2.422	1	1

AON: ADC and DAC/op-amp power-on bit. This bit provides a method of turning on several analog functions with a single write. Setting AON = 1 asserts the ADCE bit in the ADC register and DAE/OP3E, OP2E, and OP1E bits in the DACA_OP register, powering up these blocks. Setting AON = 0 has no effect. The AON bit has priority when both AON and AOFF bits are asserted.

Most of the analog functions can be enabled with a single write to the REF_SDC register using AON, REFV<1:0>, and SDCE.

SDCE: Signal-detect comparator power-enable bit. Set SDCE = 1 to power up the signal-detect comparator, and set SDCE = 0 to power down the signal-detect comparator. The ADCE bit in the ADC register must be set to 1 to use the signal-detect comparator.

TSEL<2:0>: Threshold-select bits. These bits select the threshold for the signal-detect comparator as shown in Table 11.

Table 11. Setting the Signal-Detect Comparator Threshold

NOMINAL THRESHOLD (mV)	TSEL2	TSEL1	TSEL0
0	0	X	X
50	1	0	0
100	1	0	1
150	1	1	0
200	1	1	1

X = Don't care.

AL_DAY Register (Power-On State: 0000 0000 0000 0000 0000 XXXX)

MSB							
ASEC19	ASEC18	ASEC17	ASEC16	ASEC15	ASEC14	ASEC13	ASEC12
ASEC11	ASEC10	ASEC9	ASEC8	ASEC7	ASEC6	ASEC5	ASEC4
							LSB
ASEC3	ASEC2	ASEC1	ASEC0	X	X	X	X

The AL_DAY register stores the second information of the time-of-day alarm.

ASEC<19:0>: Alarm-second bits. These 20 bits store the time-of-day alarm, which corresponds to the lower 20 bits of the RTC second counter or SEC<19:0>. Program the time-of-day alarm trigger between 1s to just over 12 days beyond the current RTC second counter value in increments of 1s.

Assert the AWE bit in the CLK_CTRL register (see the *CLK_CTRL Register* section) to enable writing to the AL_DAY register. Enabling the time-of-day alarm requires two writes to the CLK_CTRL register. Write the 20 alarm-second bits in 3 bytes, MSB first. If $\overline{CS}$ is raised before the LSB is written, the alarm write is aborted, and the existing value remains. When the lower 20 bits in the RTC second counter match the contents of this register, the alarm triggers and asserts ALD in the STATUS register. It also asserts an interrupt on the INT pin unless masked by the MALD bit in the IMSK register. The part enters normal mode if an alarm triggers while in sleep mode. The time-of-day alarm is intended to trigger single events. Therefore, once it triggers, in the CLK_CTRL register, the ADE bit is automatically cleared, disabling the time-of-day alarm. Implement a recurring alarm with repeated software writes over the serial interface each time the time-of-day alarm triggers. The time-of-day alarm can also be programmed to output at the UPIO pins.

When configured this way the MALD bit does not mask the UPIO alarm output.

CLK_CTRL Register (Power-On State: 00X0 1111 0010 1110)

MSB							
AWE	ADE	X	RWE	RTCE	OSCE	FLLE	HFCE
							LSB
CKSEL2	CKSEL1	CKSEL0	IO32E	CK32E	CLKE	INTP	WDE

The CLK_CTR register contains the control bits for the RTC alarms and clocks.

AWE: Alarm write-enable bit. Set AWE = 1 to write data to the AL_DAY register as well as the ADE bit in this register. When AWE = 0, all writes are prevented to the AL_DAY register and the ADE bit in this register. A second write to this register is required to change the value of the ADE bit. The power-on default state is 0.

ADE: Alarm (time-of-day) enable bit. Set ADE = 1 to enable the time-of-day alarm, and set ADE = 0 to disable the time-of-day alarm. When enabled, the ALD bit in the STATUS register asserts when the RTC second counter time matches AL_DAY register. The device wakes up from sleep to normal mode if not already awake. The ADE bit can only be written if the AWE = 1 from a previous write. The power-on default state is 0.

RWE: RTC write-enable bit. Set RWE = 1 prior to writing to the RTC register and the RTCE bit in this register. If RWE = 0, all writes are prevented to the RTC register as well as the RTCE bit in this register. The RWE signal takes effect after the rising edge of the 16th clock; therefore, a second write to this register is required to change the value of the RTCE bit. The power-on default state is 0.

RTCE: Real-time-clock enable bit. Set RTCE = 1 to enable the RTC, and set RTCE = 0 to disable the RTC. The RTC has a 32-bit second and an 8-bit subsecond counter. The power-on default state is 1.

OSCE: 32kHz crystal-oscillator enable bit. Set OSCE = 1 to power up the 32kHz oscillator, and set OSCE = 0 to power down the oscillator. The power-on default state is 1.

FLLE: Frequency-locked-loop enable bit. Set FLLE = 1 to enable the FLL, and set FLLE = 0 to disable the FLL. If HFCE = 1 and FLLE = 0, the internal high-frequency oscillator is enabled, but it is not frequency-locked to the 32kHz clock. When FLLE is asserted, it typically takes 3.5ms for the high-frequency clock to settle to within 1% of the 32kHz reference clock frequency. Switching the FLL on or off with this bit does not cause high-frequency clock glitching. The power-on default state is 1.

HFCE: High-frequency-clock enable bit. Set HFCE = 1 to enable the internal high-frequency clock source, and set HFCE = 0 to disable the high-frequency clock source.

If HFCE = 1 and CLKE = 1, the internal high-frequency oscillator is enabled and is present at CLK. The power-on default state is 1.

CKSEL<2:0>: Clock selection bits. These bits select the FLL-based output clock frequency at the high-frequency CLK pin as shown in Table 12. The power-on default state is 001.

IO32E: Input/output 32kHz clock select bit. Set IO32E = 0 to configure the CLK32K pin as an output, and set IO32E = 1 to configure the CLK32K pin as an input, regardless of the signal on the 32KIN pin as shown in Table 13.

External clock frequencies applied to CLK32K are clock sources to the FLL, charge pump, and the signal-detect comparator. The default power-on state is 0.

CK32E: CLK32K output-buffer enable bit. Set CK32E = 1 to enable the CLK32K output buffer as long as OSCE = 1 and IO32E = 0; otherwise the CK32E bit will not be asserted. Set CK32E = 0 to disable the CLK32K output buffer. The power-on default state is 1.

CLKE: CLK output-buffer enable bit. Set CLKE = 1 to enable the CLK output buffer. Set CLKE = 0 to disable the buffer. Disabling the buffer is useful for saving power in cases where the high-frequency clock is used internally but is not needed externally. If HFCE = 0, or if CLKE = 0, CLK remains low. The power-on default state is 1.

INTP: Interrupt pin polarity bit. Set INTP = 1 to make INT an active-high output when asserted, and set INTP = 0 to make INT an active-low output when asserted. The power-on default state is 1.

WDE: Watchdog-enable bit. Set WDE = 1 to enable the watchdog timer, which asserts $\overline{\text{RESET}}$ low within 500ms if the WATCHDOG register is not written. Set WDE = 0 to disable the watchdog timer. The power-on default state is 0.

Table 12. Setting the CLK Frequency

CLOCK FREQUENCY (kHz)	CKSEL2	CKSEL1	CKSEL0
4915.2	0	0	0
2457.6	0	0	1
1228.8	0	1	0
614.4	0	1	1
32.768	1	0	0
16.384	1	0	1
8.192	1	1	0
4.096	1	1	1

Table 13. Configuring the CLK32K as an Input or Output

CLK32K	CLK32K	IO32E	32KIN, 32KOUT	RTC, PWM, WDT CLOCK SOURCE	FLL, C/P, SDC INPUT SOURCE	ADC CLOCK SOURCE
Output	1	0	XTAL attached	XTAL	XTAL	FLL/HFCLK
Input	0	1	XTAL attached	XTAL	CLK32K	FLL/HFCLK

RTC Register (Power-On State: 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000)

MSB							
SEC31	SEC30	SEC29	SEC28	SEC27	SEC26	SEC25	SEC24
SEC23	SEC22	SEC21	SEC20	SEC19	SEC18	SEC17	SEC16
SEC15	SEC14	SEC13	SEC12	SEC11	SEC10	SEC9	SEC8
SEC7	SEC6	SEC5	SEC4	SEC3	SEC2	SEC1	SEC0
							LSB
SUB7	SUB6	SUB5	SUB4	SUB3	SUB2	SUB1	SUB0

The RTC register stores the 40-bit second and subsecond count of the respective time-of-day and system clocks.

SEC<31:0>: The second bits store the time-of-day clock settings. It is a 32-bit binary counter with 1s resolution that can keep time for a span of over 136 years. Firmware in the µC can translate this time count to units that are meaningful to the system (i.e., translate to calendar time or as an elapsed time from some predefined time = 0, such as January 1, 2000). The RTC runs continuously as long as RTCE = 1 (see the *CLK_CNTL Register* section) and does not stop for reads or writes. The counter increments when the subsecond counter overflows. Set RWE = 1 to enable writing to the RTC register. After writing to RWE, perform another write and set RTCE = 1 to enable the RTC. A 40-bit burst write operation, starting with SEC31 and finishing with SUB0 is required to set the RTC second and subsecond bits. If $\overline{CS}$ is brought high before the 40th rising SCLK edge, the write is aborted and the RTC contents are unchanged. The RTC register is loaded on the rising SCLK edge of the 40th bit (SUB0). A 40-bit burst read operation, starting with SEC31 and finishing with SUB0, is required to retrieve the current RTC second and subsecond counts. The read command can be aborted prior to receiving the 40th bit (SUB0) by raising $\overline{CS}$ and any RTC data read to that point is valid. When the read command is received, a snapshot of a valid RTC second count is latched to avoid reading an erroneous, transitioning RTC value. Due to the asynchronous nature of RTC reads, it is possible to have a maximum 1s error between the actual and reported times from the time-of-day clock. To prevent the data from changing during a read operation, complete reads of the RTC register in less than 1ms. The power-on default state is 0000 0000 hex.

SUB<7:0>: The subsecond bits store the system clock. This 8-bit binary counter has 3.9ms resolution (1/256Hz) and a span of 1s. The subsecond counter increments in single counts from 00 hex to FF hex before rolling over again to 00 hex, at which time the RTC second counter (SEC<31:0>) increments. The RTC runs continuously (as long as RTCE = 1) and does not stop for reads or writes. A 256Hz clock, derived from the 32kHz crystal, increments this counter. Set the RWE = 1 bit to enable writing to the RTC register. After writing to RWE, perform another write, setting RTCE = 1, to enable the RTC. A 40-bit burst write operation, starting with SEC31 and finishing with SUB0, is required to set the RTC second and subsecond bits. If $\overline{CS}$ is brought high before the 40th rising SCLK edge, the write is aborted and the RTC contents are unchanged. The RTC register is loaded on the rising SCLK edge of the 40th bit (SUB0). A 40-bit burst read operation, starting with SEC31 and finishing with SUB0, is required to retrieve the current RTC second and subsecond counts. The read command can be aborted prior to receiving the 40th bit (SUB0) by raising $\overline{CS}$, and any RTC data read to that point is valid. When the read command is received, a snapshot of a valid RTC second count is latched to avoid reading an erroneous, transitioning RTC value. Due to the asynchronous nature of RTC reads, it is possible to have a maximum 1s error between the actual and reported times from the time-of-day clock. To prevent the data from changing during a read operation, complete reads of the RTC registers occur in less than 1ms. The power-on default state is 00 hex.

PWM_CTRL Register (Power-On State: 0000 0000 00XX XXXX)

MSB							
PWME	FSEL2	FSEL1	FSEL0	SWAH	SWAL	X	X
							LSB
SPD1	SPD2	X	X	X	X	X	X

The PWM_CTRL register contains control bits for the 8-bit PWM.

PWME: PWM-enable bit. Set PWME = 1 to enable the internal PWM, and set PWME = 0 to disable the internal PWM. Enable the high-frequency clock before enabling the PWM when using input clock frequencies above 32.768kHz. The power-on default state is 0.

FSEL<2:0>: Frequency selection bits. Selects the PWM input clock frequency as shown in Table 14. The power-on default is 000.

Table 14. Setting the PWM Frequency

PWM INPUT FREQUENCY* (kHz)	FSEL2	FSEL1	FSEL0
4915.2**	0	0	0
2457.6**	0	0	1
1228.8**	0	1	0
32.768	0	1	1
8.192	1	0	0
1.024	1	0	1
0.256	1	1	0
0.032	1	1	1

**The lower PWM frequencies are useful for power-supply duty cycling to conserve battery life and enable a single-battery cell-powered system. The higher frequencies allow reasonably small, external components for RC filtering when used as a DAC for bias adjustments.*

***When the part is in sleep mode, the HFCK is shut down. In this case, PWM frequencies above 32kHz are not available (see SPWME in the SLEEP_CFG Register section).*

SWAH: SWA-switch PWM-high control bit. Set SWAH = 1 to enable the PWM output to directly control the SWA switch. When SWAH = SWAL, the PWM output is disabled from controlling the SWA switch. When SWAH = 1, a PWM high output closes the SWA switch and a PWM low output opens the SWA switch. The PWM high output refers to the beginning of the period when the output is logic-high. See Table 17 for more details. The power-on default is 0.

SWAL: SWA-switch PWM-low control bit. Set SWAL = 1 to enable the inverted PWM output to directly control the SWA switch. When SWAH = SWAL, the PWM output is disabled from controlling the SWA switch. When SWAL = 1, a PWM low output closes the SWA switch and a PWM high output opens the SWA switch. The PWM low output refers to the end of the period when the output is logic-low. See Table 17 for more details. The power-on default is 0.

SPD1: SPDT1-switch PWM drive control bit. Set SPD1 = 1 to enable the PWM output to directly control the SPDT1 switch, and set SPD1 = 0 to disable the PWM output controlling the SPDT1 switch. The SPDT1<1:0> bits, the UPIO pins (if programmed), and the PWM output (if enabled), determine the SPDT1-switch state. See Table 18 for more details. The power-on default is 0.

SPD2: SPDT2-switch PWM drive control bit. Set SPD2 = 1 to enable the PWM output to directly control the SPDT2 switch, and set SPD2 = 0 to disable the PWM output controlling the SPDT2 switch. The SPDT2<1:0> bits, the UPIO pins (if programmed), and the PWM output (if enabled), determine the SPDT2-switch state. See Table 19 for more details. The power-on default is 0.

PWM_THTP Register (Power-On State: 0000 0000 0000 0000)

MSB							
PWMTH7	PWMTH6	PWMTH5	PWMTH4	PWMTH3	PWMTH2	PWMTH1	PWMTH0
							LSB
PWMTP7	PWMTP6	PWMTP5	PWMTP4	PWMTP3	PWMTP2	PWMTP1	PWMTP0

The PWM_THTP register contains the bits that set the PWM on-time and period.

PWMTH<7:0>: PWM time high bits. These bits define the PWM on (or high) time and when combined with the PWMTP<7:0> bits, they determine the duty cycle and period. The on-time duty cycle is defined as:

(PWMTH<7:0> + 1)/(PWMTP<7:0> + 1)

To get 50% duty cycle, set PWMTH<7:0> to 127 decimal and PWMTP<7:0> to 255 decimal. A 100% duty cycle (i.e., always on) is possible with a value of PWMTH<7:0> ≥ PWMTP<7:0> > 0. A 0% duty cycle is possible by setting PWMTH<7:0> = 0 or PWME = 0 in the PWM_CTRL register. If the PWM is selected to drive the UPIO_ pin(s), the ALH_ bit(s) (UPIO_CTRL register) determine the on-time polarity at the beginning of the PWM cycle. If ALH_ = 1, the on-time at the start of the PWM period causes a logic-high level (DVDD or CPOUT) at the UPIO_ pin. When ALH_ = 0, it causes a logic-low level (DGND) during the on-time. When the PWM output drives the SWA/B switches, the SWA(B)H or SWA(B)L bits in the PWM_CTRL register determine which PWM phase closes these switches. The SPDT1 and SPDT2 switches do not have PWM polarity inversion bits (see the SPDT1<1:0> and SPDT2<1:0> bit descriptions in the *SW_CTRL Register* section), but their effective polarity is set by how the switches are connected externally. The power-on default is 00 hex.

PWMTP<7:0>: PWM time period bits. These bits control the PWM output period defined. The PWM output period is defined as:

(PWMTP<7:0> + 1)/(PWM input frequency)

Set the PWM input frequency by selecting the FSEL<2:0> bits as described in Table 14. The power-on default is 00 hex.

WATCHDOG Register (Power-On State: N/A)

Writing to the WATCHDOG register address sets the watchdog timer to 0ms. If the watchdog is enabled (WDE = 1) and the WATCHDOG register is not written to before the 750ms expiration, $\overline{\text{RESET}}$ asserts low for 250ms and the watchdog timer restarts at 0ms when the watchdog timer is enabled. There are no data bits for this register, and the watchdog timer is reset on the rising edge of SCLK during the ADR0 bit in the WATCHDOG register address control byte. Figure 17 shows an example of watchdog timing.

NORM_MD Register (Power-On State: N/A)

Exit sleep mode and enter normal mode by writing to the NORM_MD register. The specific normal-mode state of all circuit blocks is set by the user, who must configure the individual power-enable bits before entering sleep mode (Table 15). There are no data bits for this register, and normal mode begins on the rising edge of SCLK during the ADR0 bit in the NORM_MD register address control byte.

SLEEP Register (Power-On State: N/A)

Enter sleep mode by writing to the SLEEP register. This low-power state overrides most of the normal power-control bits. Table 15 shows which functions are off, which functions are unaffected (ADE, RTCE, LSDE, and HYSE), and which functions are controlled by special sleep-mode bits (SOSCE, SCK32E, and SPWME) while in sleep mode. There are no data bits for this register, and sleep mode begins on the rising edge of SCLK during the ADR0 bit in the SLEEP register address control byte.

Table 15. Normal-Mode and Sleep-Register Summary

REGISTER NAME	CIRCUIT BLOCK DESCRIPTION	POR DEFAULT	NORMAL MODE	SLEEP
ADC	ADC	ADCE = 0	ADCE	Off
DACA_OP	DACA/OP3	DAE/OP3E = 0	DAE/OP3E	Off
	OP1	OP1E = 0	OP1E	Off
REF_SDC	Reference Buffer Gain and Enable	REFV<1:0> = 00	REFV<1:0>	Off
	Signal-Detect Comparator	SDCE = 0	SDCE	Off
CLK_CTRL	Time-of-Day Alarm Enable	ADE = 0	ADE	ADE
	RTC	RTCE = 1	RTCE	RTCE
	CK32 Xtal Oscillator	OSCE = 1	OSCE	SOSCE
	CK32 Output Buffer	CK32E = 1	CK32E	SCK32E
	High-Frequency Clock	HFCE = 1	HFCE	Off
	High-Frequency Clock Output Buffer	CLKE = 1	CLKE	Off
	FLL Enable	FLLE = 1	FLLE	Off
	Watchdog Timer	WDE = 0	WDE	Off
PWM_CTRL	PWM	PWME = 0	PWME	SPWME
PS_VMONS	Linear Regulator	LDOE = 0	LDOE	Off
	Charge-Pump Doubler	CPE = 0	CPE	Off
	CPOUT Voltage Monitor	CPDE = 0	CPDE	Off
	1.8V DVDD Monitor	LSDE = 1	LSDE	LSDE
	1.8V Monitor Hysteresis	HYSE = 0	HYSE	HYSE
TEMP_CTRL	Temperature Sense Source	IMUX<1:0> = 00	IMUX<1:0>	Off
UPIO_CTRL	UPIO_ Function	UP_MD<3:0> = 0 hex	UP_MD<3:0>	UP_MD<3:0>
	UPIO_ Pullup	PUP_ = 1	PUP_	PUP_
	UPIO_ Supply Voltage	SV_ = 0	SV_	SV_
	UPIO_ Assertion Level	ALH_ = 0	ALH_	ALH_

SLEEP_CFG Register (Power-On State: 1100 XXXX)

MSB								LSB
SLP (ADR0)	SOSCE	SCK32E	SPWME	SHDN	X	X	X	X

The SLEEP_CFG register allows users to program specific behavior for the 32kHz oscillator, buffer, and PWM in sleep mode. It also contains a sleep-control bit (SLP) to enable sleep mode.

SLP (ADR0): Sleep bit. The SLP bit is the LSB in the SLEEP_CFG address control byte. Set SLP = 1 to assert the SHDN bit and enter sleep mode. Writing the register with SLP = 0 or reading with SLP = 0 or SLP = 1 has no effect on the SHDN bit.

SOSCE: Sleep-mode 32kHz crystal oscillator enable bit. SOSCE = 1 enables the 32kHz oscillator in sleep mode, and SOSCE = 0 disables it in sleep mode, regardless of the state of the OSCE bit. The power-on default is 1.

SCK32E: Sleep-mode CK32K-pin output-buffer enable bit. SCK32E = 1 enables the 32kHz output buffer in sleep mode, and SCK32E = 0 disables it in sleep mode, regardless of the state of the CK32E bit. The power-on default is 1.

SPWME: Sleep-mode PWM enable bit. SPWME = 1 enables the internal PWM in sleep mode, and SPWME = 0 disables it in sleep mode, regardless of the state of the PWME bit.

Input frequencies are limited to 32.768kHz or lower since the high-frequency clock is disabled in sleep mode. SOSCE must be asserted to have 32kHz available as an input to the PWM. The power-on default is 0.

SHDN: Shutdown bit. This bit is read only. SHDN is asserted by writing to the SLEEP register address or by writing to the SLEEP_CFG register with SLP = 1. When SHDN is asserted, the device is in sleep mode even if the SLEEP or $\overline{SLEEP}$ function on the UPIO is deasserted. The SHDN bit is deasserted by writing to the NORM_MD register or by other defined events. Events that cause SHDN to be deasserted are a day alarm or an edge on the UPIO wake-up pin causing wake-up to be asserted. The power-on default is 0.

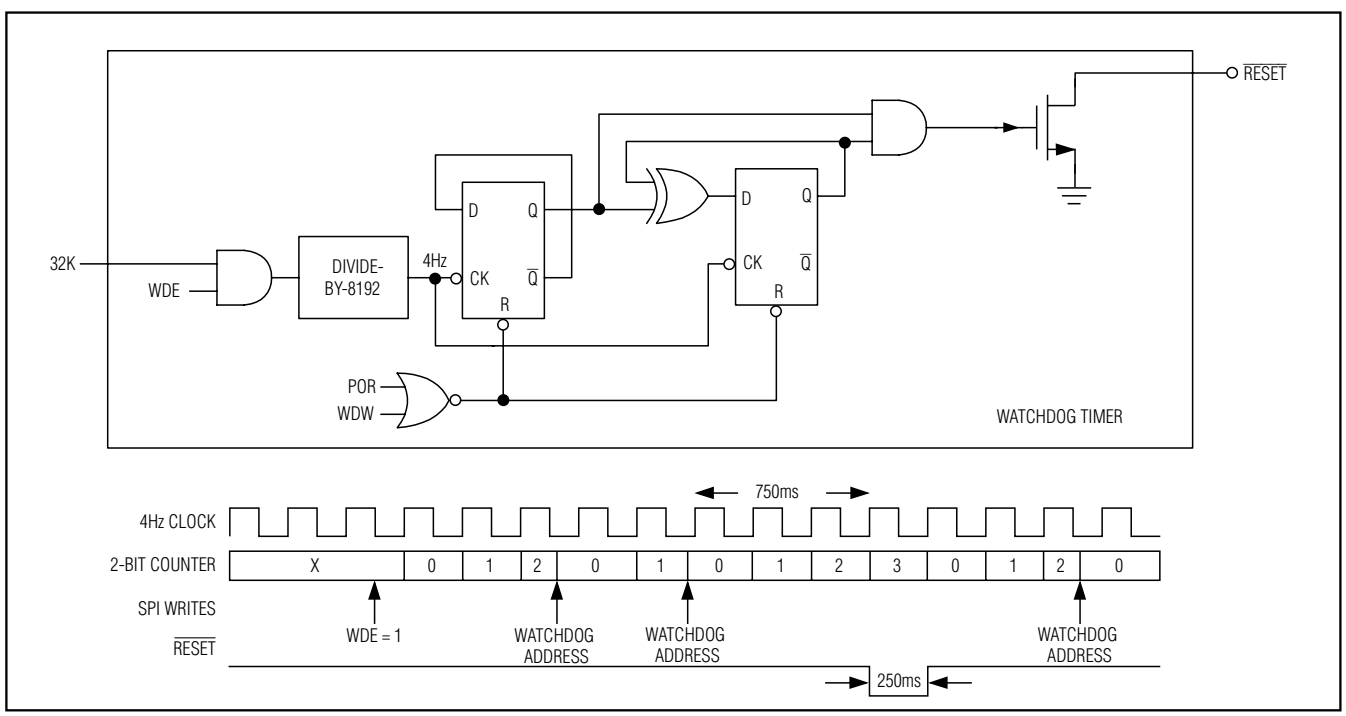


Figure 17. Watchdog Timer Architecture

UPIO4_CTRL Register (Power-On State: 0000 1000)

MSB							LSB
UP4MD3	UP4MD2	UP4MD1	UP4MD0	PUP4	SV4	ALH4	LL4

UPIO4_CTRL register. This register configures the UPIO4 pin functionality.

UP4MD<3:0>: UPIO4-mode selection bits. These bits configure the mode for the UPIO4 pin. See Table 16 for a detailed description. The power-on default is 0 hex.

PUP4: Pullup UPIO4 control bit. Set PUP4 = 1 to enable a weak pullup resistor on the UPIO4 pin, and set PUP4 = 0 to disable it. The pullup resistor is connected to either DVDD or CPOUT as programmed by the SV4 bit. The pullup is enabled only when UPIO4 is configured as an input. Open-drain behavior can be simulated at UPIO4 by setting the mode to GPO with LL4 = 0 and by changing the mode to GPI with PUP4 = 0, allowing external high pullup. The power-on default is 1.

SV4: Supply-voltage UPIO4 selection bit. Set SV4 = 0 to select DVDD as the supply voltage for the UPIO4 pin, and set SV4 = 1 to select CPOUT as the supply voltage. The selected supply voltage applies to all modes for the UPIO4 pin. The power-on default is 0.

ALH4: Active logic-level assertion high UPIO4 bit. Set ALH4 = 0 to define the input or output assertion level for UPIO4 as low except when in GPI and GPO modes. Set ALH4 = 1 to define the input or output assertion level as high. For example, asserting ALH4 defines the UPIO4 output signal as ALARM, while deasserting ALH4 defines it as $\overline{\text{ALARM}}$. Similarly, asserting ALH4 defines the UPIO4 input signal as WU, while deasserting ALH4 defines it as $\overline{\text{WU}}$. The power-on default is 0.

LL4: Logic-level UPIO4 bit. When UPIO4 is configured as GPO, LL4 = 0 sets the output to a logic-low and LL4 = 1 sets the output to a logic-high. A read of LL4 returns the voltage level at the UPIO4 pin at the time of the read, regardless of how it is programmed. The power-on default is 0.

UPIO3_CTRL Register (Power-On State: 0000 1000)

MSB							LSB
UP3MD3	UP3MD2	UP3MD1	UP3MD0	PUP3	SV3	ALH3	LL3

UPIO3_CTRL register. This register configures the UPIO3 pin functionality.

UP3MD<3:0>: UPIO3-mode selection bits. These bits configure the mode for the UPIO3 pin. See Table 16 for a detailed description. The power-on default is 0 hex.

PUP3: Pullup UPIO3 control bit. Set PUP3 = 1 to enable a weak pullup resistor on the UPIO3 pin, and set PUP3 = 0 to disable it. The pullup resistor is connected to either DVDD or CPOUT as programmed by the SV3 bit. The pullup is enabled only when UPIO3 is configured as an input. Open-drain behavior can be simulated at UPIO3 by setting the mode to GPO with LL3 = 0 and by changing the mode to GPI with PUP3 = 0, allowing external high pullup. The power-on default is 1.

SV3: Supply-voltage UPIO3 selection bit. Set SV3 = 0 to select DV_{DD} as the supply voltage for the UPIO3 pin, and set SV3 = 1 to select CPOUT as the supply voltage. The selected supply voltage applies to all modes for the UPIO3 pin. The power-on default is 0.

ALH3: Active logic-level assertion high UPIO3 bit. Set ALH3 = 0 to define the input or output assertion level for UPIO3 as low except when in GPI and GPO modes. Set ALH3 = 1 to define the input or output assertion level as high. For example, asserting ALH3 defines the UPIO3 output signal as ALARM, while deasserting ALH3 defines it as $\overline{\text{ALARM}}$. Similarly, asserting ALH3 defines the UPIO3 input signal as WU, while deasserting ALH3 defines it as $\overline{\text{WU}}$. The power-on default is 0.

LL3: Logic-level UPIO3 bit. When UPIO3 is configured as GPO, LL3 = 0 sets the output to a logic-low and LL3 = 1 sets the output to a logic-high. A read of LL3 returns the voltage level at the UPIO3 pin at the time of the read, regardless of how it is programmed. The power-on default is 0.

UPIO2_CTRL Register (Power-On State: 0000 1000)

MSB							LSB
UP2MD3	UP2MD2	UP2MD1	UP2MD0	PUP2	SV2	ALH2	LL2

UPIO2_CTRL register. This register configures the UPIO2 pin functionality.

UP2MD<3:0>: UPIO2-mode selection bits. These bits configure the mode for the UPIO2 pin. See Table 16 for a detailed description. The power-on default is 0 hex.

PUP2: Pullup UPIO2 control bit. Set PUP2 = 1 to enable a weak pullup resistor on the UPIO2 pin, and set PUP2 = 0 to disable it. The pullup resistor is connected to either DVDD or CPOUT as programmed by the SV2 bit. The pullup is enabled only when UPIO2 is configured as an input. Open-drain behavior can be simulated at UPIO2 by setting the mode to GPO with LL2 = 0 and by changing the mode to GPI with PUP2 = 0, allowing external high pullup. The power-on default is 1.

SV2: Supply-voltage UPIO2 selection bit. Set SV2 = 0 to select DVDD as the supply voltage for the UPIO2 pin, and set SV2 = 1 to select CPOUT as the supply voltage. The selected supply voltage applies to all modes for the UPIO2 pin. The power-on default is 0.

ALH2: Active logic-level assertion high UPIO2 bit. Set ALH2 = 0 to define the input or output assertion level for UPIO2 as low except when in GPI and GPO modes. Set ALH2 = 1 to define the input or output assertion level as high. For example, asserting ALH2 defines the UPIO2 output signal as $\overline{\text{ALARM}}$, while deasserting ALH2 defines it as $\overline{\text{ALARM}}$. Similarly, asserting ALH2 defines the UPIO2 input signal as $\overline{\text{WU}}$, while deasserting ALH2 defines it as $\overline{\text{WU}}$. The power-on default is 0.

LL2: Logic-level UPIO2 bit. When UPIO2 is configured as GPO, LL2 = 0 sets the output to a logic-low and LL2 = 1 sets the output to a logic-high. A read of LL2 returns the voltage level at the UPIO2 pin at the time of the read, regardless of how it is programmed. The power-on default is 0.

UPIO1_CTRL Register (Power-On State: 0000 1000)

MSB							LSB
UP1MD3	UP1MD2	UP1MD1	UP1MD0	PUP1	SV1	ALH1	LL1

UPIO1_CTRL register. This register configures the UPIO1 pin functionality.

UP1MD<3:0>: UPIO1-mode selection bits. These bits configure the mode for the UPIO1 pin. See Table 16 for a detailed description. The power-on default is 0 hex.

PUP1: Pullup UPIO1 control bit. Set PUP1 = 1 to enable a weak pullup resistor on the UPIO1 pin, and set PUP1 = 0 to disable it. The pullup resistor is connected to either DVDD or CPOUT as programmed by the SV1 bit. The pullup is enabled only when UPIO1 is configured as an input. Open-drain behavior can be simulated at UPIO1 by setting the mode to GPO with LL1 = 0 and by changing the mode to GPI with PUP1 = 0, allowing external high pullup. The power-on default is 1.

SV1: Supply-voltage UPIO1 selection bit. Set SV1 = 0 to select DVDD as the supply voltage for the UPIO1 pin, and set SV1 = 1 to select CPOUT as the supply voltage. The selected supply voltage applies to all modes for the UPIO1 pin. The power-on default is 0.

ALH1: Active logic-level assertion high UPIO1 bit. Set ALH1 = 0 to define the input or output assertion level for UPIO1 as low except when in GPI and GPO modes. Set ALH1 = 1 to define the input or output assertion level as high. For example, asserting ALH1 defines the UPIO1 output signal as $\overline{\text{ALARM}}$, while deasserting ALH1 defines it as $\overline{\text{ALARM}}$. Similarly, asserting ALH1 defines the UPIO1 input signal as WU, while deasserting ALH1 defines it as $\overline{\text{WU}}$. The power-on default is 0.

LL1: Logic-level UPIO1 bit. When UPIO1 is configured as GPO, LL1 = 0 sets the output to a logic-low and LL1 = 1 sets the output to a logic-high. A read of LL1 returns the voltage level at the UPIO1 pin at the time of the read, regardless of how it is programmed. The power-on default is 0.

Table 16. UPIO Mode Configuration

UP4MD<3:0>, UP3MD<3:0>, UP2MD<3:0>, UP1MD<3:0>				MODE	DESCRIPTION
				MAX11359A	
0	0	0	0	GPI	General-purpose digital input. Active edges detected by UPR_ or UPF_ status register bits. ALH_ has no effect with this setting.
0	0	0	1	GPO	General-purpose digital output. Logic level set by LL_ bit. ALH_ has no effect with this setting.
0	0	1	0	SWA or $\overline{SWA}$	Digital input. DAC A buffer switch control. See the SWA bit description in the *SW_CTRL Register* section.
0	0	1	1	Reserved	Reserved. Do not use these settings.
0	1	0	0	SPDT1 or $\overline{SPDT1}$	Digital input. SPDT1 switch control. See the SPDT1<1:0> bit description in the *SW_CTRL Register* section.
0	1	0	1	SPDT2 or $\overline{SPDT2}$	Digital input. SPDT2 switch control. See the SPDT2<1:0> bit description in the *SW_CTRL Register* section.
0	1	1	0	SLEEP or $\overline{SLEEP}$	Sleep-mode digital input. Overrides power-control register and puts the part into sleep mode when asserted. When deasserted, power mode is determined by the SHDN bit.
0	1	1	1	WU or $\overline{WU}$	Wake-up digital input. Asserted edge clears SHDN bit.
1	0	0	0	Reserved	Reserved. Do not use these settings.
1	0	0	1		
1	0	1	0		
1	0	1	1	PWM or $\overline{PWM}$	PWM digital output. Signal defined by the PWM_CTRL register. PWM on (or high or “1”); assertion level defined by the ALH_ bit. When PWM is disabled (PWME = 0), the UPIO pin idles high (DVDD or CPOUT) if ALH = 1, and low (DGND) if ALH = 0.
1	1	0	0	SHDN or $\overline{SHDN}$	Power-supply shutdown digital output. Equivalent to SHDN bit. Power-on default of GPI with pullup ensures initial power-supply turn-on when UPIO is connected to a power supply with a $\overline{SHDN}$ input.
1	1	0	1	AL_DAY or $\overline{AL_DAY}$	RTC alarm digital output. Asserts for time-of-day alarm events; equivalent to ALD in STATUS register.
1	1	1	0	Reserved	Reserved. Do not use these settings.
1	1	1	1	DRDY or $\overline{DRDY}$	ADC data-ready digital output. Asserts when analog-to-digital conversion or calibration completes. Not masked by MADD bit.

Note: *When multiple UPIO inputs are configured for the same input function, the inputs are OR’ed together.*

UPIO_SPI Register (Power-On State: 0000 XXXX)

MSB							LSB
UP4S	UP3S	UP2S	UP1S	X	X	X	X

UPIO_SPI pass-through control register. These bits map the serial interface signals to the UPIO pins, allowing the DAS to drive other devices at CPOUT or DVDD voltage levels, depending on the SV_ bit setting found in the UPIO_CTRL register. Individual bits are provided to set only the desired UPIO inputs to the SPI pass-through mode. This mode becomes active when $\overline{CS}$ is driven high to complete the write to this register, and remains active as long as $\overline{CS}$ stays high (i.e., multiple pass-through writes are possible). The SPI pass-through mode is deactivated immediately when $\overline{CS}$ is pulled low for the next DAS write.

The UPIO_ state (both before and after the SPI pass-through mode) is set by the UP_MD<3:0> and LL_ bits. When a UPIO is configured for SPI pass-through mode and the $\overline{CS}$ is high, UPR_, UPF_, and LL_ continue to detect UPIO_ edges, which can still generate interrupts. See Figure 19 for an SPI pass-through timing diagram.

UP4S: UPIO4 SPI pass-through-mode enable bit. A logic 1 maps the inverted $\overline{CS}$ signal to the UPIO4 pin. Therefore, UPIO4 is low (near DGND) when SPI pass-through mode is active, and is high (near DVDD or CPOUT) when the mode is inactive. A logic 0 disables the UPIO4 SPI pass-through mode. The power-on default is 0.

UP3S: UPIO3 SPI pass-through-mode enable bit. A logic 1 maps the SCLK signal to UPIO3 (directly with no inversion), while a logic 0 disables the UPIO3 SPI pass-through mode. The power-on default is 0.

UP2S: UPIO2 SPI pass-through-mode enable bit. A logic 1 maps the DIN signal to UPIO2 (directly with no inversion), while a logic 0 disables the UPIO2 SPI pass-through mode. The power-on default is 0.

UP1S: UPIO1 SPI pass-through-mode enable bit. A logic 1 maps the UPIO1 input signal to DOUT (directly with no inversion), while a logic 0 disables the UPIO1 SPI pass-through mode. The power-on default is 0.

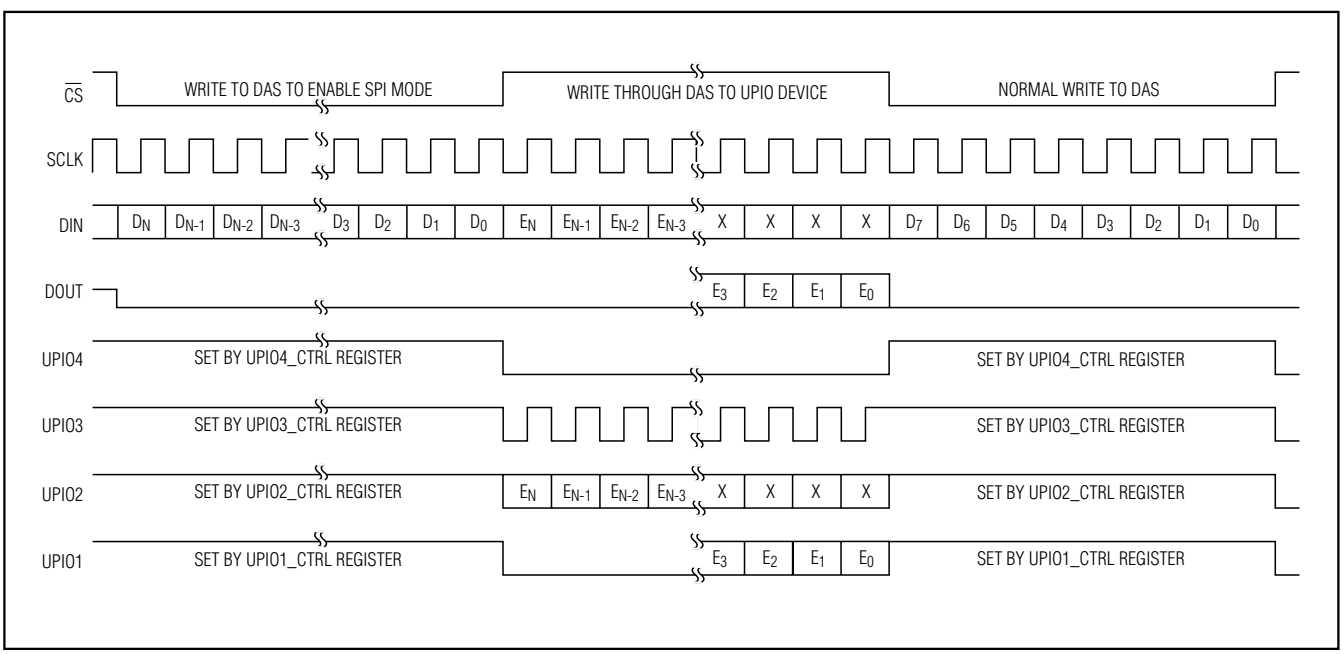


Figure 18. SPI Pass-Through Timing Diagram

SW_CTRL Register (Power-On State: 0000 00XX)

MSB							LSB
SWA	X	SPDT11	SPDT10	SPDT21	SPDT20	X	X

The switch-control register controls the two SPDT switches (SPDT1 and SPDT2) and the DACA output buffer SPST switch (SWA). Control this switch by the serial bits in this register, by any of the UPIO pins that are enabled for that function, or by the PWM.

SWA: DACA output buffer SPST-switch A control bit. The SWA bit, the UPIO inputs (if configured), and the PWM (if configured) control the state of the SWA switch as shown in Table 17. The UPIO_ states of 0 and 1 in the table correspond to respective deasserted and asserted logic states as defined by the ALH_ bit of the UPIO_CTRL register. If a UPIO is not configured for this mode, its value applied to the table is 0. The PWM states of 0 and 1 in the table correspond to the respective PWM off (or low) and on (or high) states defined by the SWAH and SWAL bits (see the *PWM_CTRL Register* section). If the PWM is not configured for this mode, its value applied to the table is 0. The power-on default is 0.

SPDT1<1:0>: Single-pole double-throw switch 1 control bits. The SPDT1<1:0> bits, the UPIO pins (if configured), and the PWM (if configured) control the state of the switch as shown in Table 18. The UPIO_ states of 0 and 1 in the table correspond to respective deasserted and asserted logic states as defined by the ALH_ bit of the UPIO_CTRL register. If a UPIO is not configured for this mode, its value applied to Table 18 is 0. The PWM states of 0 and 1 in Table 18 correspond to the respective PWM off (low) and on (high) states defined by the SPD1 bit in the PWM_CTRL register. If the PWM is not configured for this mode, its value applied to Table 18 is 0. The power-on default is 00.

SPDT2<1:0>: Single-pole double-throw switch 2 control bits. The SPDT2<1:0> bits, the UPIO pins (if configured), and the PWM (if configured) control the state of the switch as shown in Table 19. The UPIO_ states of 0 and 1 in the table correspond to respective deasserted and asserted logic states as defined by the ALH_ bit in the UPIO_CTRL register. If a UPIO is not configured for this mode, its value applied to Table 19 is 0. The PWM states of 0 and 1 in Table 19 correspond to the respective PWM off (low) and on (high) states defined by the SPD2 bit in the PWM_CTRL register. If the PWM is not configured for this mode, its value applied to Table 19 is 0. The power-on default is 00.

Table 17. SWA States

SWA BIT*	UPIO_*	PWM*	SWA SWITCH STATE
0	0	0	Switch open
X	X	1	Switch closed
X	1	X	Switch closed
1	X	X	Switch closed

X = Don't care.

**Switch SW_ control is effectively an OR of the SW_ bit, UPIO pins, and PWM.*

Table 18. SPDT Switch 1 States

SPDT1<1:0>		UPIO_*	PWM*	SPDT1 SWITCH STATE
0	0	0	0	SNO1 open, SNC1 open
0	X	X	1	SNO1 closed, SNC1 closed
0	X	1	X	SNO1 closed, SNC1 closed
0	1	X	X	SNO1 closed, SNC1 closed
1	0	0	0	SNC1 closed, SNO1 open
1	X	X	1	SNC1 open, SNO1 closed
1	X	1	X	SNC1 open, SNO1 closed
1	1	X	X	SNC1 open, SNO1 closed

X = Don't care.

**Switch SPDT1 control is effectively an OR of the SPDT10 bit, the UPIO pins, and the PWM output. The SPDT11 bit determines if the switches open and close together or if they toggle.*

Table 19. SPDT Switch 2 States

SPDT2<1:0>		UPIO_*	PWM*	SPDT2 SWITCH STATE
0	0	0	0	SNO2 open, SNC2 open
0	X	X	1	SNO2 closed, SNC2 closed
0	X	1	X	SNO2 closed, SNC2 closed
0	1	X	X	SNO2 closed, SNC2 closed
1	0	0	0	SNC2 closed, SNO2 open
1	X	X	1	SNC2 open, SNO2 closed
1	X	1	X	SNC2 open, SNO2 closed
1	1	X	X	SNC2 open, SNO2 closed

X = Don't care.

**Switch SPDT2 control is effectively an OR of the SPDT20 bit, the UPIO pins, and the PWM output. The SPDT21 bit determines if the switches open and close together or if they toggle.*

TEMP_CTRL Register (Power-On State: 0000 XXXX)

MSB							LSB
IMUX1	IMUX0	IVAL1	IVAL0	X	X	X	X

The temperature-sensor control register controls the internal and external temperature measurement.

IMUX<1:0>: Internal current-source MUX bits. Selects the pin to be driven by the internal current sources as shown in Table 20. The power-on default is 00.

IVAL<1:0>: Internal current-source value bits. Selects the value of the internal current source as shown in Table 21. The power-on default is 00.

Table 20. Selecting Internal Current Source

CURRENT SOURCE	IMUX1	IMUX0
Disabled	0	0
Internal temperature sensor	0	1
AIN1	1	0
AIN2	1	1

Table 21. Setting the Current Level

CURRENT	TYPICAL CURRENT (µA)	IVAL1	IVAL0
I_1	4	0	0
I_2	60	0	1
I_3	64	1	0
I_4	120	1	1

TEMP_CAL Register (Power-On State: Varies By Factory Calibration)

MSB							
TGAIN7	TGAIN6	TGAIN5	TGAIN4	TGAIN3	TGAIN2	TGAIN1	TGAIN0
							LSB
TOFFS5	TOFFS4	TOFFS3	TOFFS2	TOFFS1	TOFFS0	X	X

This register is the internal temperature sensor calibration register.

TGAIN<7:0>: Factory-preset temperature gain correction coefficient bits. This is the linear scaling factor used to derive absolute temperature values from temperature values measured with the internal temperature sensor ($T_{ACTUAL} = T_{MEAS} \times T_{GAIN} + T_{OFFS}$). The coefficients are optimized for an internal voltage reference of 1.25V using the four-current method. The power-on default varies.

TOFFS<5:0>: Factory-preset temperature offset correction coefficient bits. This is the linear offset factor used to derive absolute temperature values from temperature values measured with the internal temperature sensor ($T_{ACTUAL} = T_{MEAS} \times T_{GAIN} + T_{OFFS}$). The coefficients are optimized for an internal voltage reference of 1.25V using the four-current method. The power-on default varies.

IMSK Register (Power-On State: 1111 011X 1111 1111)

MSB							
MLDVD	MLCPD	MADO	MSDC	MCRDY	MADD	MALD	X
							LSB
MUPR4	MUPR3	MUPR2	MUPR1	MUPF4	MUPF3	MUPF2	MUPF1

The IMSK register determines which bits of the STATUS register generate an interrupt on INT. The bits in this register do not mask output signals routed to UPIO since the output signals are masked by disabling that UPIO function.

MLDVD: LDVD status bit mask. Set MLDVD = 0 to enable the LDVD status bit interrupt to INT, and set MLDVD = 1 to mask the LDVD status bit interrupt. The power-on default value is 1.

MLCPD: LCP status bit mask. Set MLCPD = 0 to enable the LCP status bit interrupt to INT, and set MLCPD = 1 to mask the LCP status bit interrupt. The power-on default value is 1.

MADO: ADO status bit mask. Set MADO = 0 to enable the ADO status bit interrupt to INT, and set MADO = 1 to mask the ADO status bit interrupt. The power-on default value is 1.

MSDC: SDC status bit mask. Set MSDC = 0 to enable the SDC status bit interrupt to INT, and set MSDC = 1 to mask the SDC status bit interrupt. The power-on default value is 1.

MCRDY: CRD status bit mask. Set MCRDY = 0 to enable the CRDY status bit interrupt to INT, and set MCRDY = 1 to mask the CRDY status bit interrupt. The power-on default value is 0.

MADD: ADD status bit mask. Set MADD = 0 to enable the ADD status bit interrupt to INT, and set MADD = 1 to mask the ADD status bit interrupt. The power-on default value is 1.

MALD: ALD status bit mask. Set MALD = 0 to enable the ALD status bit interrupt to INT, and set MALD = 1 to mask the ALD status bit interrupt. The power-on default value is 1.

MUPR<4:1>: UPR<4:1> status bits mask. Set MUPR_ = 0 to enable the UPR_ status bit interrupt to INT, and set MUPR_ = 1 to mask the UPR_ status bit interrupt. (_ = 1, 2, 3, or 4 and corresponds to the UPIO1, UPIO2, UPIO3, or UPIO4 pins, respectively.) The power-on default value is F hex.

MUPF<4:1>: UPF<4:1> status bits mask. Set MUPF_ = 0 to enable the UPF_ status bit interrupt to INT, and set MUPF_ = 1 to mask the UPF_ status bit interrupt. (_ = 1, 2, 3, or 4 and corresponds to the UPIO1, UPIO2, UPIO3, or UPIO4 pins, respectively.) The power-on default value is F hex.

PS_VMONS Register (Power-On State: 0010 01XX)

MSB							LSB
LDOE	CPE	LSDE	CPDE	HYSE	RSTE	X	X

This register is the power-supply and voltage monitors control register.

LDOE: Low-dropout linear-regulator enable bit. Set LDOE = 1 to enable the low-dropout linear regulator to provide the internal source voltage for the charge pump. Set LDOE = 0 to disable the LDO, allowing an external drive to the charge-pump input through REG. The power-on default value is 0.

CPE: Charge-pump enable bit. Set CPE = 1 to enable the charge-pump doubler, and set CPE = 0 to disable the charge-pump doubler. The power-on default value is 0.

LSDE: DVDD low-supply voltage-detector power-enable bit. Set LSDE = 1 to enable the +1.8V (DVDD) low-supply-voltage detector, and set LSDE = 0 to disable the DVDD low-supply-voltage detector. The power-on default value is 1.

CPDE: CPOUT low-supply voltage-detector power-enable bit. Set CPDE = 1 to enable the +2.7V CPOUT low-supply voltage-detector comparator, and set CPDE = 0 to disable the CPOUT low-supply voltage-detector comparator. The power-on default value is 0.

HYSE: DVDD low-supply voltage-detector hysteresis-enable bit. Set HYSE = 1 to set the hysteresis for the +1.8V (DVDD) low-supply-voltage detector to +200mV, and set HYSE = 0 to set the hysteresis to +20mV. On initial power-up, the hysteresis is +20mV and can be programmed to 200mV once $\overline{\text{RESET}}$ goes high. Once programmed to +200mV, the DVDD falling threshold is +1.8V nominally and the rising threshold is +2.0V nominally. The

hysteresis helps eliminate chatter when running directly off unregulated batteries. If DVDD falls below +1.3V (typ), the power-on reset circuitry is enabled and the HYSE bit is deasserted setting the hysteresis back to +20mV. The power-on default is 0.

RSTE: $\overline{\text{RESET}}$ output enable bit. Set RSTE = 1 to enable $\overline{\text{RESET}}$ to be controlled by the +1.8V DVDD low-supply-voltage detector, and set RSTE = 0 to disable this control. The power-on default is 1.

STATUS Register (Power-On State: 0000 000X 0000 0000)

MSB							
LDVD	LCPD	ADOU	SDC	CRDY	ADD	ALD	X
							LSB
UPR4	UPR3	UPR2	UPR1	UPF4	UPF3	UPF2	UPF1

The STATUS register contains the status bits of events in various system blocks. Any status bits not masked in the IMSK register cause an interrupt on INT. Some of the status bit setting events (GPI, WAKEUP, ALARM, DRDY) can be directed to UPIO_ to provide multiple µC interrupt inputs. There are no specific mask bits for the UPIO interrupt signals since the bits are effectively masked by selecting a different function for UPIO. The STATUS bits always record the triggering event(s), even for masked bits, which do not generate an interrupt on INT. It is possible to set multiple STATUS bits during a single INT interrupt event. Clear all STATUS bits except for ADD and ADOU by reading the STATUS register. During a STATUS register read, INT deasserts when the first STATUS data bit (LDVD) reads out (9th rising SCLK) and remains deasserted until shortly after the last STATUS data bit (~15ns). At this point, INT reasserts if any STATUS bit is set during the STATUS register read. If the STATUS register is partially read (i.e., the read is aborted midway), none of the STATUS bits are cleared. New events occurring during a STATUS register read, or events that persist after reading the STATUS bits result in another interrupt immediately after the STATUS register read finishes. This is a read-only register.

LDVD: Low DVDD voltage-detector status bit. LDVD = 1 indicates DVDD is below the +1.8V threshold; otherwise LDVD = 0. LDVD clears during the STATUS register read as long as the condition does not persist. Otherwise, the LDVD bit reasserts immediately. If the DVDD low voltage detector is disabled, LDVD = 0. The power-on default is 0.

LCPD: Low CPOUT voltage-detector status bit. LCPD = 1 indicates CPOUT is below the +2.7V threshold; otherwise LCPD = 0. LCPD clears during the STATUS register read as long as the condition does not persist. Otherwise the LCPD bit reasserts immediately. LCPD = 0 when the CPOUT low voltage detector is disabled. The power-on default is 0.

ADOU: ADC overflow/underflow status bit. ADOU = 1 indicates an ADC underflow or overflow condition in the current ADC result. New conversions that are valid clear the ADOU bit. ADOU = 0 when the ADC data is valid or the ADC is disabled (ADCE = 0). An underflow condition occurs when the ADC data is theoretically less than 0000 hex in unipolar mode and less than 8000 hex in bipolar mode. An overflow condition occurs when the ADC data is theoretically greater than FFFF hex in unipolar mode and greater than 7FFF hex in bipolar mode. Use this bit to determine the validity of an ADC result at the maximum or minimum code values (i.e., 0000 hex or FFFF hex for unipolar mode and 8000 hex and 7FFF hex for bipolar mode). The power-on default is 0. Reading the STATUS register does not clear the ADOU bit.

SDC: Signal-detect comparator status bit. When SDC = 1, the positive input to the signal-detect comparator exceeds the negative input plus the programmed threshold voltage. The SDC bit clears during the STATUS register read unless the condition remains true. The SDC bit also deasserts when the signal-detect comparator powers down (SDCE = 0). The power-on default is 0.

CRDY: High-frequency-clock ready status bit. CRDY = 1 indicates a locked high-frequency clock to the 32kHz reference frequency by the FLL. The CRDY bit clears during the STATUS register read. This bit only asserts after power-up or after enabling the FLL using the FLLE bit. The power-on default is 0.

ADD: ADC-done status bit. ADD = 1 indicates a completed ADC conversion or calibration. Clear the ADD bit by reading the appropriate ADC data, offset, or gain-calibration registers. The ADC status bit also clears when a new ADC result updates to the data or calibration registers (i.e., it follows the assertion level of the UPIO = $\overline{\text{DRDY}}$ signal). Reading the STATUS register does not clear this bit. This bit is equivalent to the DRDY signal available through UPIO_. The power-on default is 0.

ALD: Alarm (day) status bit. ALD = 1 when the value programmed in ASEC<19:0> in the AL_DAY register matches SEC<19:0> in the RTC register. Clear the ALD bit by reading the STATUS register or by disabling the day alarm (ADE = 0). The power-on default is 0.

UPR<4:1>: User-programmable I/O rising-edge status bits. UPR_ = 1 indicates a rising edge on the respective UPIO_ pin has occurred. Clear UPR_ by reading the STATUS register. Rising edges are detected independent of UPIO_ configuration, providing the ability to capture and record rising input (e.g., WU) or output (e.g., PWM) edge events on the UPIO_. Set the appropriate mask to determine if the edge will generate an interrupt on INT. If the UPIO_ is configured as an output, INT provides confirmation that an intended rising edge output occurred and has reached the desired DVDD or CPOUT level (i.e., was not loaded down externally). The power-on default is 0.

UPF<4:1>: User-programmable I/O falling-edge status bit. UPF_ = 1 indicates a falling edge on the respective UPIO_ has occurred. Clear UPF_ by reading the STATUS register. Falling edges are detected independent of UPIO_ configuration, providing the ability to capture and record falling input (e.g., WU) or output (e.g., PWM) edge events on the UPIO_. Set the appropriate mask to determine if that edge should generate an interrupt on the INT pin. If the UPIO is configured as an output, INT provides confirmation that an intended falling edge output occurred at the pin and it reached the desired DGND level. The power-on default is 0.

Applications Information

Analog Filtering

The internal digital filter does not provide rejection close to the harmonics of the modulator sample frequency. However, due to high oversampling ratios in the MAX11359A, these bands typically occupy a small fraction of the spectrum and most broadband noise is filtered. Therefore, the analog filtering requirements in front of the MAX11359A are considerably reduced compared to a conventional converter with no on-chip filtering. In addition, because the device's common-mode rejection (60dB) extends out to several kHz, the common-mode noise susceptibility in this frequency range is substantially reduced.

Depending on the application, provide filtering prior to the MAX11359A to eliminate unwanted frequencies the digital filter does not reject. Providing additional filtering in some applications ensures that differential noise signals outside the frequency band of interest do not saturate the analog modulator.

When placing passive components in front of the MAX11359A, ensure a low enough source impedance to prevent introducing gain errors to the system. This configuration significantly limits the amount of passive anti-aliasing filtering that can be applied in front of the MAX11359A. See Table 3 for acceptable source impedances.

Power-On Reset or Power-Up

After a power-on reset, the DVDD voltage supervisor is enabled and all UPIOs are configured as inputs with pullups enabled. The internal oscillators are enabled and are output at CLK and CLK32K once the DVDD voltage supervisor is cleared and the subsequent timeout period has expired. All interrupts are masked except CRDY. Figure 19 illustrates the timing of various signals during initial power-up, sleep mode, and wake-up events. The ADC, charge pump, internal reference, op amp(s), DAC, and switches are disabled after power-up.

Power Modes

Two power modes are available for the MAX11359A: sleep and normal mode. In sleep mode, all functional blocks are powered down except the serial interface, data registers, internal bandgap, wake-up circuitry (if enabled), DVDD voltage supervisor (if enabled), and the 32kHz oscillator (if enabled), which remain active. See Table 15 for details of the sleep-mode and normal-mode power states of the various internal blocks.

Each analog block can be shut down individually through its respective control register with the exception of the bandgap reference.

Sleep Mode

Sleep mode is entered one of three ways:

- Writing to the SLEEP register address. The result is the SHDN bit is set to 1.
- Asserting the SLEEP or $\overline{\text{SLEEP}}$ function on a UPIO (SLEEP takes precedence over software writes or wake-up events). The SHDN bit is unaffected.
- Asserting the SHDN bit by writing SLP = 1 in the SLEEP_CFG register.

Entering sleep mode is an OR function of the UPIO or SHDN bit. Before entering sleep mode, configure the normal mode conditions.

Exit sleep mode and enter normal mode by one of the following methods:

- With the SHDN bit = 0, deassert the SLEEP or $\overline{\text{SLEEP}}$ function on UPIO, only if SLEEP or $\overline{\text{SLEEP}}$ function is used for entering sleep mode.

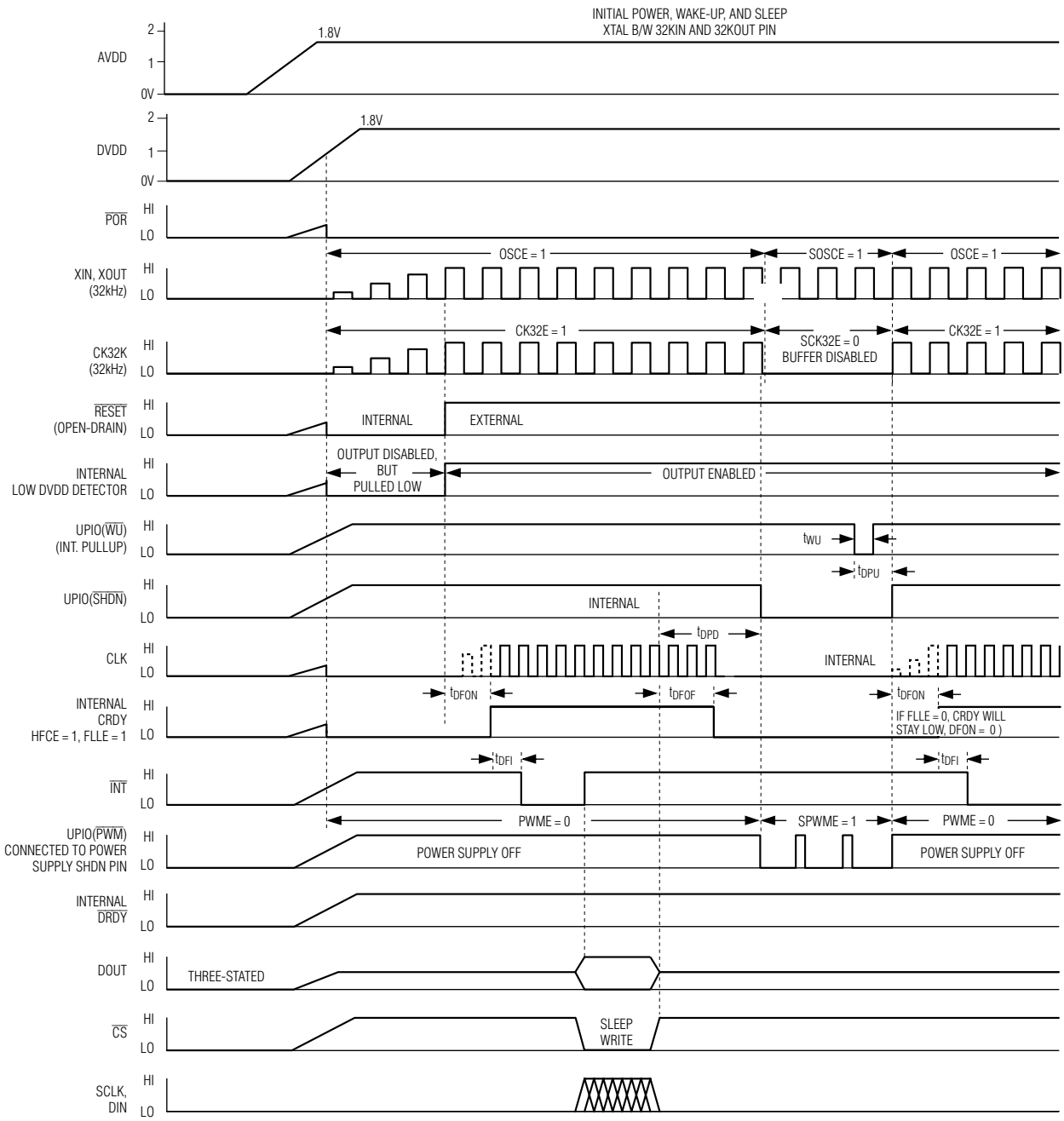


Figure 19. Initial Power-Up, Sleep Mode, and Wake-Up Timing Diagram with V_{AVDD} > 1.8V

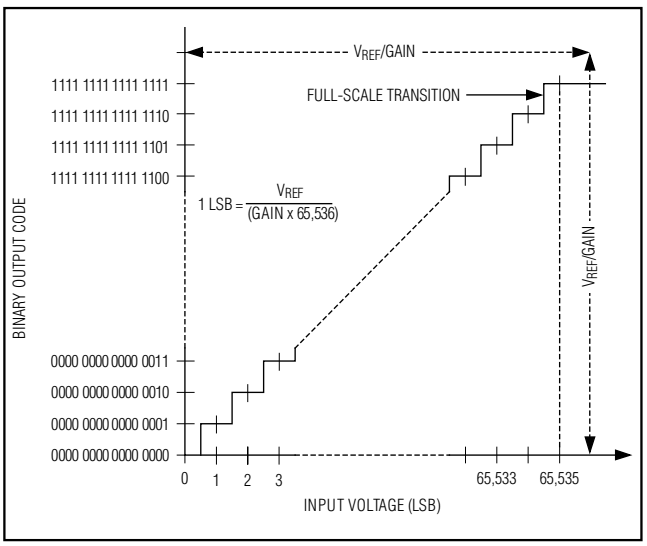


Figure 20. ADC Unipolar Transfer Function

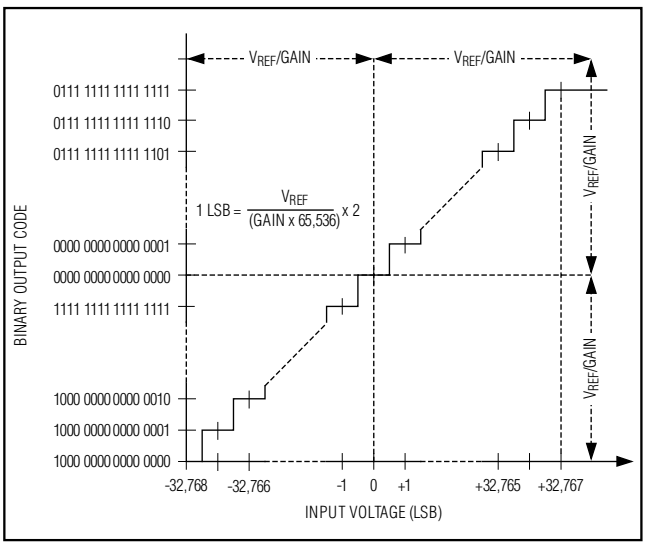


Figure 21. ADC Bipolar Transfer Function

- With the SLEEP or $\overline{\text{SLEEP}}$ function deasserted on UPIO, clear the SHDN bit by writing to the normal-mode register address control byte.
- With the SLEEP or $\overline{\text{SLEEP}}$ function deasserted, assert WU or $\overline{\text{WU}}$ (wake-up) function on UPIO.
- With the SLEEP or $\overline{\text{SLEEP}}$ function deasserted, the day alarm triggers.

Wake-Up

A wake-up event, such as an assertion of a UPIO configured as WU or a time-of-day alarm causes the MAX11359A to exit sleep mode, if in sleep mode. A wake-up event in normal mode results only in a wake-up event being recorded in the STATUS register.

$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ output pulls low for any one of the following cases: power-on reset, DVDD monitor trips and RSTE = 0, watchdog timer expires, crystal oscillator is attached, and 32kHz clock not ready.

The $\overline{\text{RESET}}$ output can be turned off through the RSTE bit in the PS_VMONS register, causing DVDD low supply voltage events to issue an interrupt or poll through the LDVD status bit. This allows brownout detection µCs that operate with V_{DVDD} < 1.8V.

Driving UPIO Outputs to AVDD Levels

UPIO outputs can be driven to AVDD levels in systems with separate AVDD and DVDD supplies. Disable the charge-pump doubler by setting CPE = 0 in the PS_VMONS register, and connect the system's analog supply to AVDD and CPOUT. Setting UPIO outputs to drive to CPOUT results in AVDD-referenced logic levels.

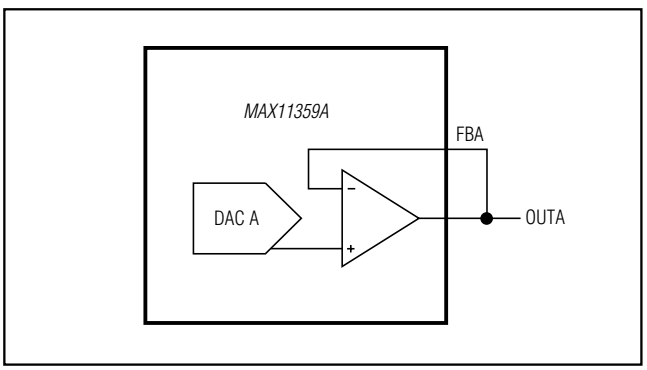


Figure 22. DAC Unipolar Output Circuit

Supply Voltage Measurement

The AVDD supply voltage can be measured with the ADC by reversing the normal input and reference signal s. The REF voltage is applied to one multiplexer input, and AGND is selected in the other. The AVDD signal is then switched in as the ADC reference voltage and a conversion is performed. The AVDD value can then be calculated directly as:

$$V_{AVDD} = (V_{REF} \times Gain \times 65536)/N$$

where V_{REF} is the reference voltage for the ADC, Gain is the PGA gain before the ADC, and N is the ADC result. Note the AVDD voltage must be greater than the gained-up REF voltage ($V_{AVDD} > V_{REF} \times Gain$). This measurement must be done in unipolar mode.

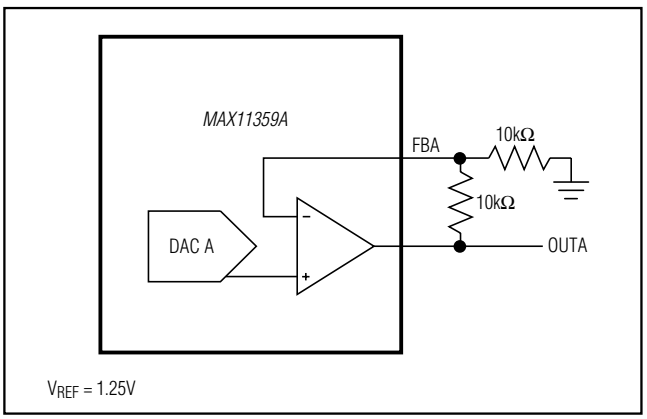


Figure 23. DAC Unipolar Rail-to-Rail Output Circuit

Power Supplies

AVDD and DVDD provide power to the MAX11359A. The AV_{DD} powers up the analog section, while the DVDD powers up the digital section. The power supply for both AVDD and DVDD ranges from +1.8V to +3.6V. Both AVDD and DVDD must be greater than +1.8V for device operation. AVDD and DVDD can connect to the same power supply. Bypass AVDD to AGND with a 10µF electrolytic capacitor in parallel with a 0.1µF ceramic capacitor, and bypass DVDD to DGND with a 10µF electrolytic capacitor in parallel with a 0.1µF ceramic capacitor. For improved performance, place the bypass capacitors as close to the device as possible.

ADC Transfer Functions

Figures 20 and 21 provide the ADC transfer functions for unipolar and bipolar mode. The digital output code format is binary for unipolar mode and two's complement for bipolar mode. Calculate 1 LSB using the following equations:

1 LSB (Unipolar Mode) = V_{REF}/(Gain x 65,536)

1 LSB (Bipolar Mode) = ±2V_{REF}/(Gain x 65,536)

where V_{REF} equals the reference voltage at REF and Gain equals the PGA gain.

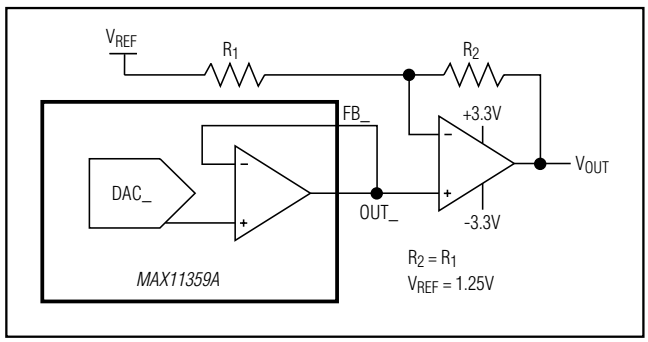


Figure 24. DAC Bipolar Output Circuit

In unipolar mode, the output code ranges from 0 to 65,535 for inputs from zero to full-scale. In bipolar mode, the output code ranges from -32,768 to +32,767 for inputs from negative full-scale to positive full-scale.

DAC Unipolar Output

For a unipolar output, the output voltages and the reference have the same polarity. Figure 22 shows the unipolar output circuit of the MAX11359A, which is also the typical operating circuit for the DAC. Table 22 lists some unipolar input codes and their corresponding output voltages.

For larger output swing, see Figure 23. This circuit shows the output amplifiers configured with a closed-loop gain of +2V/V to provide 0 to 2.5V full-scale range with the 1.25V reference.

DAC Bipolar Output

The MAX11359A DAC output can be configured for bipolar operation using the application circuit in Figure 24:

$$V_{OUT} = V_{REF}\left[\left(\frac{2N}{1024}\right) - 1\right]$$

where N is the decimal value of the DAC's binary input code.

Table 23 shows digital codes (offset binary) and corresponding output voltages for Figure 24 assuming $R_1 = R_2$.

Table 22. Unipolar Code

DAC CONTENTS MSB LSB	ANALOG OUTPUT
1111 1111 11	+V_{REF} (1023/1024)
1000 0000 01	+V_{REF} (513/1024)
1000 0000 00	+V_{REF} (512/1024) = +V_{REF}/2
0111 1111 11	+V_{REF} (511/1024)
0000 0000 01	+V_{REF} (1/1024)
0000 0000 00	0

Table 23. Bipolar Code

DAC CONTENTS MSB LSB	ANALOG OUTPUT
1111 1111 11	+V_{REF} (511/512)
1000 0000 01	+V_{REF} (1/512)
1000 0000 00	0
0111 1111 11	-V_{REF} (1/512)
0000 0000 01	-V_{REF} (511/512)
0000 0000 00	-V_{REF} (512/512) = -V_{REF}

Clocking with a CMOS Signal

A CMOS signal can be used to drive 32KIN if it is divided down. Figure 25 is an example circuit, which works well.

Input Multiplexer

The mux inputs can range between AGND to AVDD. However, when the internal temperature sensor is enabled, AIN1 and AIN2 cannot exceed 0.7V. This necessitates additional circuitry to divide down the input signal. See Figure 26 for an example circuit that divides down backlight V_{DD} to work properly with the AIN1 pin.

Optical Reflectometry Application with Dual LED and Single Photodiode

Figure 27 illustrates the MAX11359A in a complete optical reflectometry application with two transmitting LEDs and one receiving photodiode. The LEDs transmit light at a specific wavelength onto the sample strip, and the photodiode receives the reflections from the strip. Set the DAC to provide appropriate bias currents for the LEDs. Always keep the photodiodes reverse-biased or zero-biased. SPDT1 and SPDT2 switch between the two LEDs.

Electrochemical Sensor Operation

The MAX11359A family interfaces with electrochemical sensors. The 10-bit DAC with the force-sense buffers have the flexibility to connect to many different types of sensors. An external precision resistor completes the transimpedance amplifier configuration to convert the current generated by the sensor to a voltage measurement using the ADC. The induced error from this source is negligible due to FBA's extremely low input bias current. Internally, the ADC can differentially measure directly across the external transimpedance resistor, RF, eliminating any errors due to voltages drifting over time, temperature, or supply voltage.

Temperature Measurement with Two Remote Sensors

Use two diode-connected 2N3904 transistors for external temperature sensing in Figure 28. Select AIN1 and AIN2 through the positive and negative mux, respectively. For internal temperature sensor measurements, set MUXP<3:0> to 0111, and set MUXN<3:0> to 0000. The analog input signals feed through a PGA to the ADC for conversion.

Programmable-Gain Instrumentation Amplifier

Use two op amps and two SPDT switches to implement a programmable-gain instrumentation amplifier as shown in Figure 29.

PWM Applications

The MAX11359A integrated PWM is available for LCD bias control, sensor-bias voltage trimming, buzzer drive, and duty-cycled sleep-mode power-control schemes. Figure 30 shows the MAX11359A performing LCD bias control. A sensor-bias voltage trimming application is shown in Figure 31. Figures 33 and 34 show the PWM circuitry being used in a single-ended and differential piezoelectric buzzer-driving application.

ADC Calibration

Internal to the MAX11359A, the ADC is 24 bits and is always in bipolar mode. The OFFSET CAL and GAIN CAL data are also 24 bits. The conversion to unipolar and the gain are performed digitally. The default values for the OFFSET CAL and GAIN CAL registers in the MAX11359A are 00 0000h and 80 0000h, respectively.

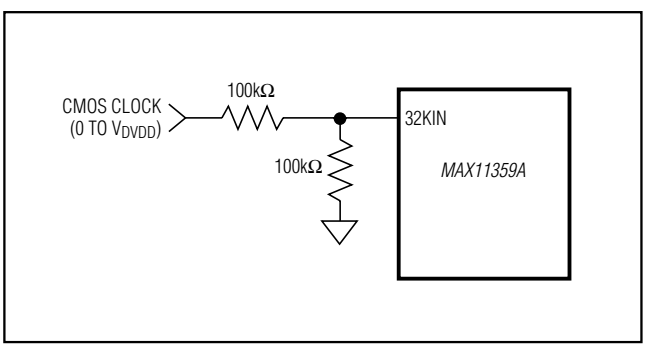


Figure 25. Clocking with a CMOS Signal

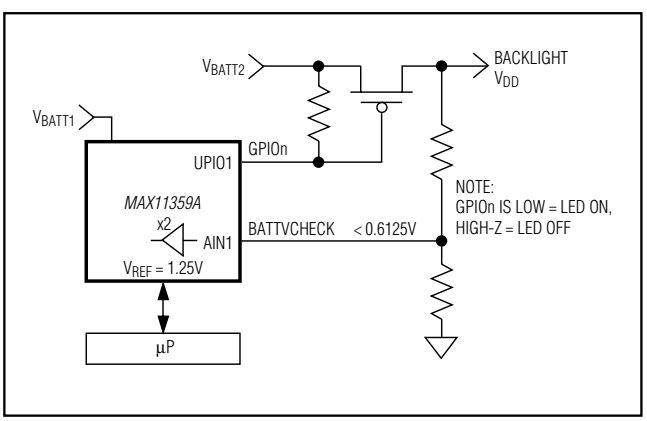


Figure 26. Input Multiplexer

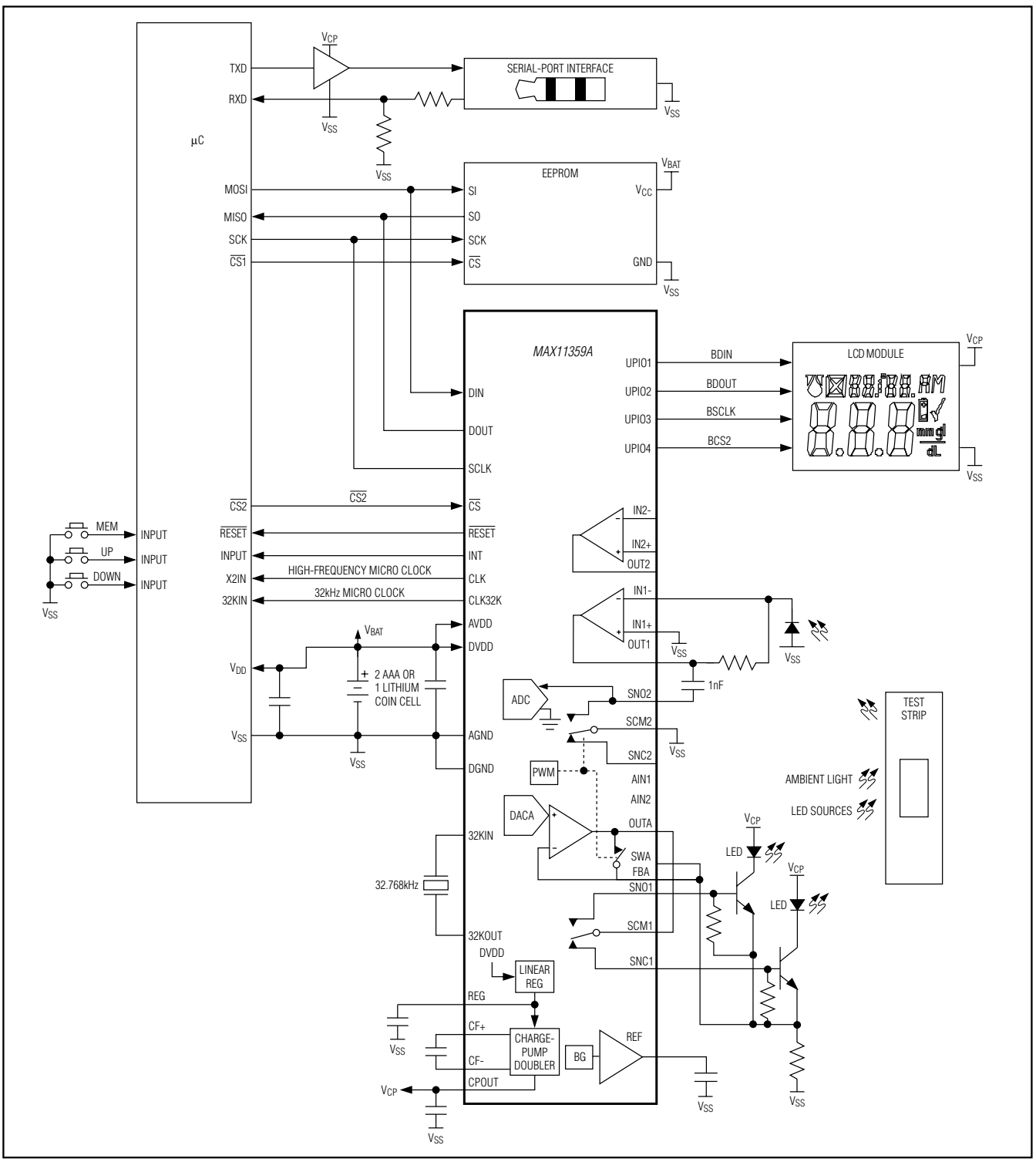


Figure 27. Optical Reflectometry Application with Dual LED and Single Photodiode

The calibration works as follows:

ADC = (RAW - OFFSET) x Gain x PGA

where ADC is the conversion result in the DATA register, RAW is the output of the decimation filter internal to the MAX11359A, OFFSET is the value stored in the OFFSET CAL register, Gain is the value stored in the GAIN CAL register, and PGA is the selected PGA gain found in the ADC register as GAIN<1:0>. In unipolar mode, all negative values return a zero result and an additional gain of 2 is added.

For self-calibration, the offset value is the RAW result when the inputs are shorted internally and the gain value is 1/(RAW - OFFSET) with the reference connected to the input. This is done automatically when these modes are selected. The self offset and gain calibration corrects for errors internal to the ADC and the results are stored and used automatically in the OFFSET CAL and GAIN CAL registers. For best results, use the ADC in the same configuration as the calibration. This pertains to conversion rate only because the PGA gain and unipolar/bipolar modes are performed digitally.

For system calibration, the offset and gain values correct for errors in the whole signal path including the internal ADC and any external circuits in the signal path. For the system calibration, a user-provided zero-input condition is required for the offset calibration and a user-provided full-scale input is required for the gain calibration. These values are automatically written to the OFFSET CAL and GAIN CAL registers. The order of the calibrations should be offset followed by gain.

The offset correction value is in two's complement. The default value is 000000h, 00...00b, or 0 decimal.

The gain correction value is an unsigned binary number with 23 bits to the right of the decimal point. The largest number is therefore 1.1111...1b = $2 - 2^{-23}$ and the smallest is 0.000...0b = 0, although it does not make sense to use a number smaller than 0.1000...0b = 0.5. The default value is 800000h, 1.000...0b or 1 decimal.

Changing the offset or gain calibration values does not affect the value in the DATA register until a new conversion has completed. This applies to all the mode bits for PGA gain, unipolar/bipolar, etc.

Grounding and Layout

For best performance, use PCB with separate analog and digital ground planes.

Design the PCB so that the analog and digital sections are separated and confined to different areas of the board. Join the digital and analog ground planes at one point. If the DAS is the only device requiring an AGND-to-DGND connection, connect planes to the AGND pin of the DAS. In systems where multiple devices require AGND-to-DGND connections, the connection should still be made at only one point. Make the star ground as close as possible to the MAX11359A.

Avoid running digital lines under the device because these may couple noise onto the device. Run the analog ground plane under the MAX11359A to minimize coupling of digital noise. Make the power-supply lines to the MAX11359A as wide as possible to provide low-impedance paths and reduce the effects of glitches on the power-supply line.

Shield fast-switching signals such as clocks with digital ground to avoid radiating noise to other sections of the board. Avoid running clock signals near the analog inputs. Avoid crossover of digital and analog signals.

Good decoupling is important when using high-resolution ADCs. Decouple all analog supplies with 10µF capacitors in parallel with 0.1µF HF ceramic capacitors to AGND. Place these components as close to the device as possible to achieve the best decoupling.

Crystal Layout

Follow basic layout guidelines when placing a crystal on a PCB with a DAS to avoid coupled noise:

1) Place the crystal as close as possible to 32KIN and 32KOUT. Keeping the trace lengths between the crystal and inputs as short as possible reduces the probability of noise coupling by reducing the length of the "antennae". Keep the 32KIN and 32KOUT lines close to each other to minimize the loop area of the clock lines. Keeping the trace lengths short also decreases the amount of stray capacitance.
2) Keep the crystal solder pads and trace width to 32KIN and 32KOUT as small as possible. The larger these bond pads and traces are, the more likely it is that noise will couple from adjacent signals.
3) Place a guard ring (connect to ground) around the crystal to isolate the crystal from noise coupled from adjacent signals.
4) Ensure that no signals on other PCB layers run directly below the crystal or below the traces to 32KIN and 32KOUT. The more the crystal is isolated from other signals on the board, the less likely it is that noise will be coupled into the crystal. Maintain a minimum distance of 5mm between any digital signal and any trace connected to 32KIN or 32KOUT.

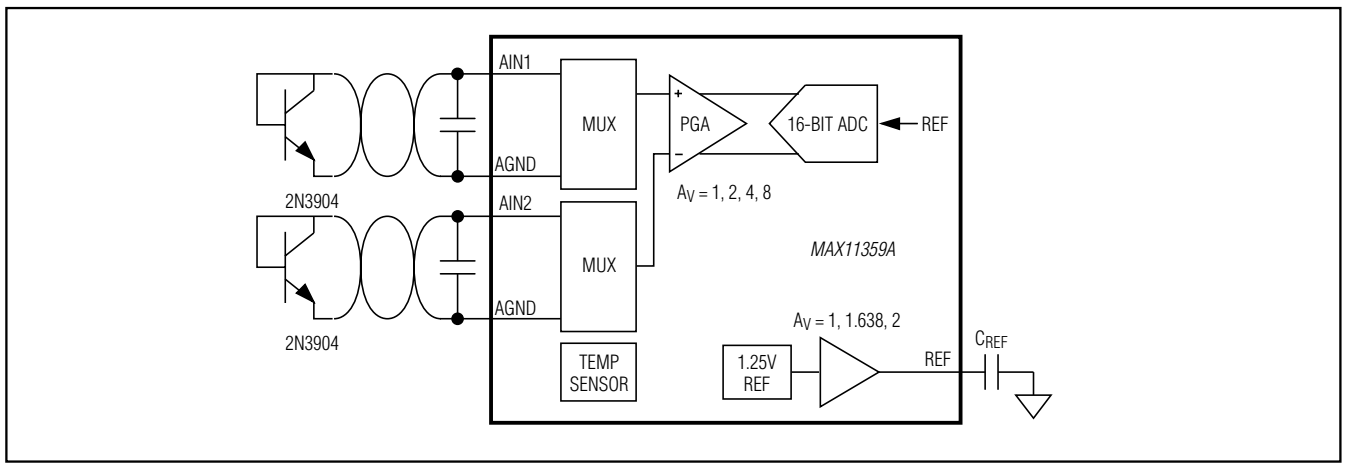


Figure 28. Temperature Measurement with Two Remote Sensors

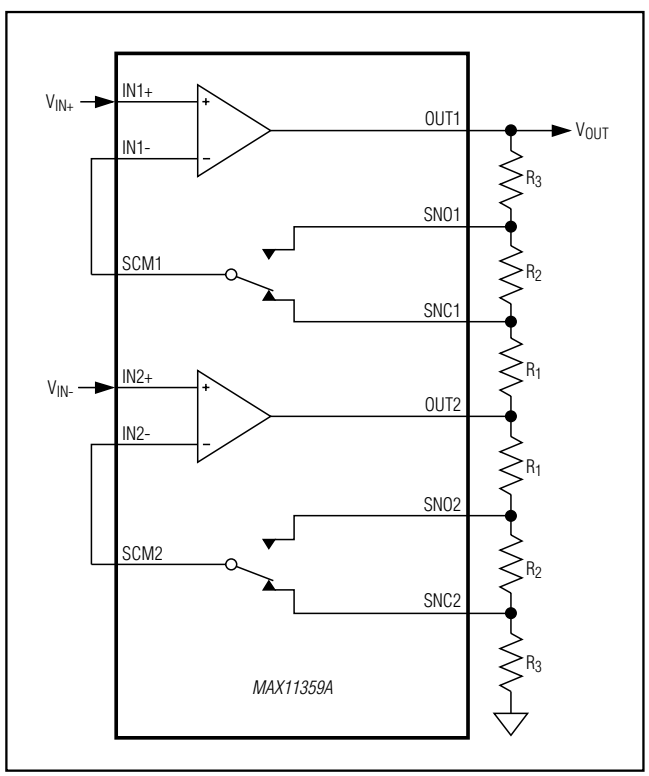


Figure 29. Programmable-Gain Instrumentation Amplifier

5) Place a local ground plane on the PCB layer immediately below the crystal guard ring. This helps to isolate the crystal from noise coupling from signals on other PCB layers.

   Note: The ground plane must be in the vicinity of the crystal only and not on the entire board.

Parameter Definitions

INL

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line is either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nulled. INL for the MAX11359A is measured using the end-point method.

DNL

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of greater than -1 LSB guarantees no missing codes and a monotonic transfer function.

Gain Error

Gain error is the amount of deviation between the measured full-scale transition point and the ideal full-scale transition point.

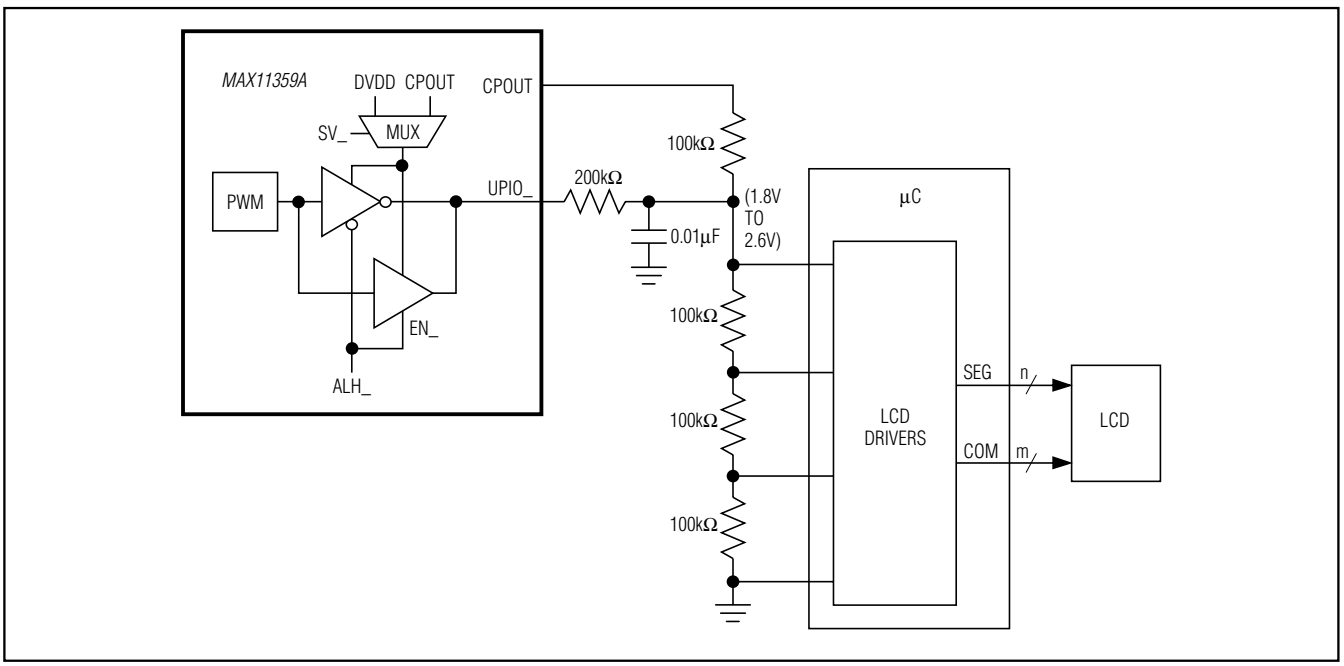


Figure 30. LCD Contrast-Adjustment Application

Common-Mode Rejection

Common-mode rejection (CMR) is the ability of a device to reject a signal that is common to both input terminals. The common-mode signal can be either an AC or a DC signal or a combination of the two. CMR is often expressed in decibels.

Power-Supply Rejection Ratio (PSRR)

Power-supply rejection ratio (PSRR) is the ratio of the input supply change (in volts) to the change in the converter output (in volts). It is typically measured in decibels.

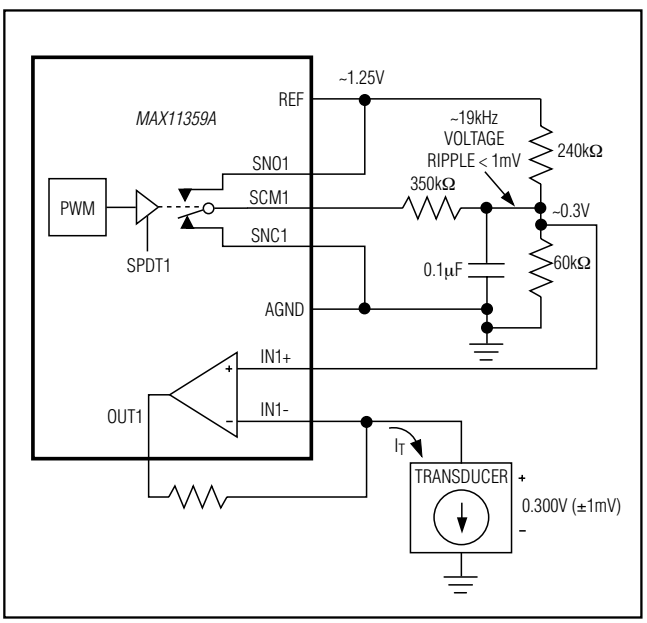


Figure 31. Sensor-Bias Voltage Trim Application

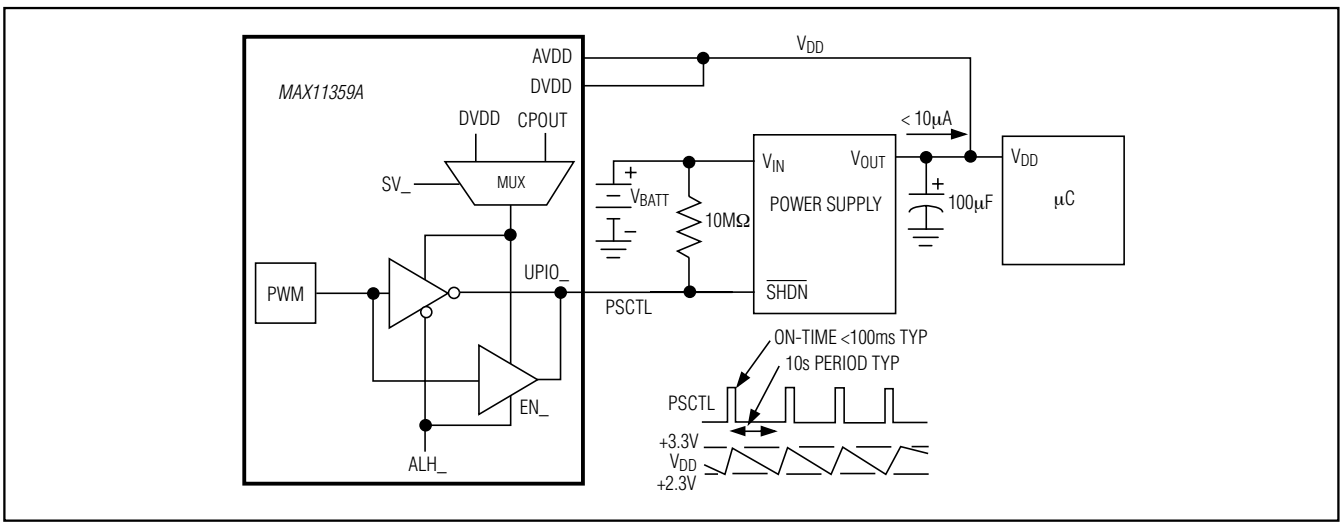


Figure 32. Power-Supply Sleep-Mode Duty-Cycle Control

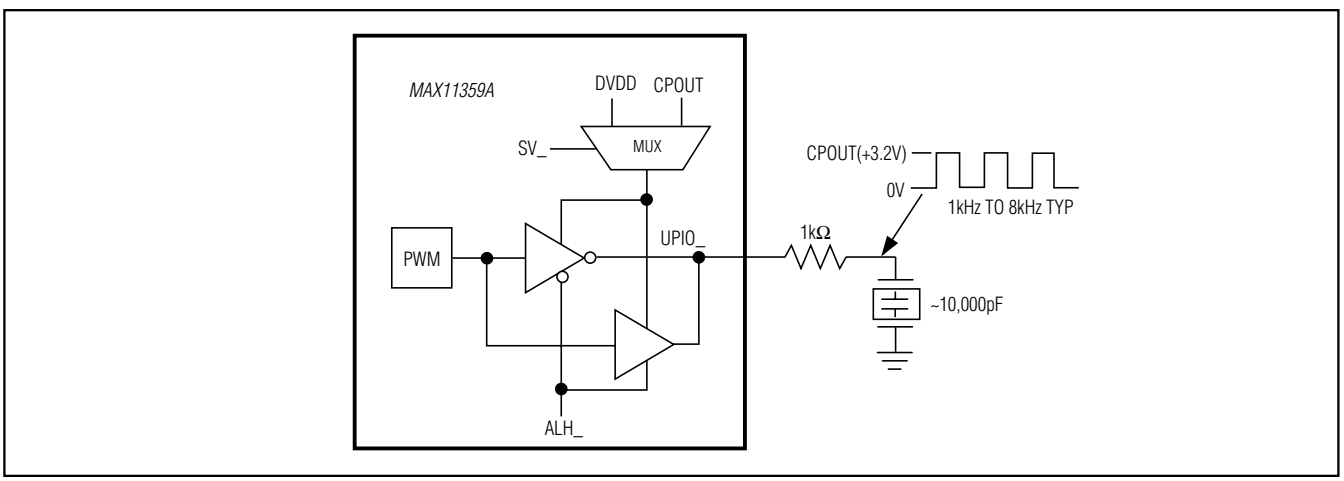


Figure 33. Single-Ended Piezoelectric Buzzer Drive

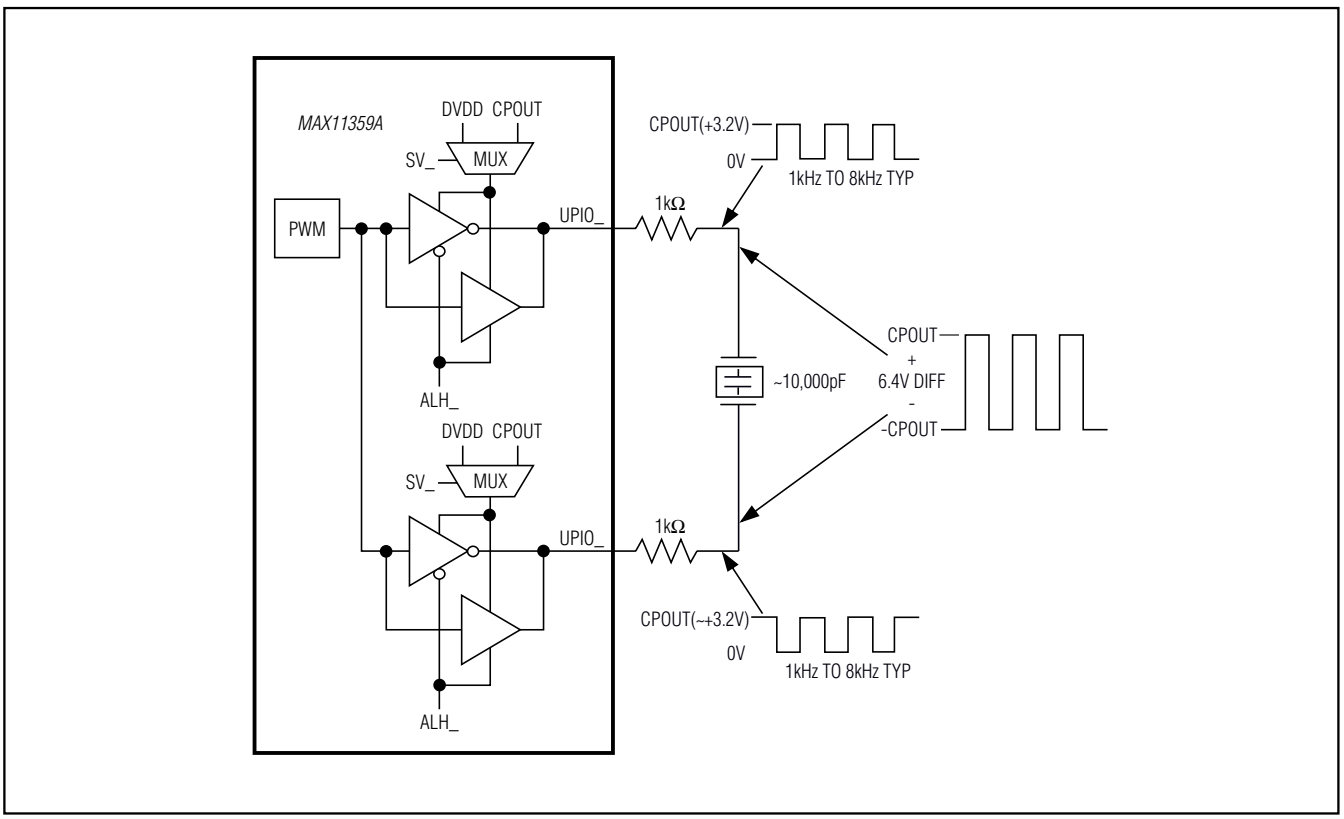


Figure 34. Differential Piezoelectric Buzzer Drive

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
40 TQFN-EP	T4066+5	21-0141	90-0055

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/09	Initial release	—
1	1/12	Updated package information and style updates.	1–10, 12–29, 31, 32, 35, 45, 46, 48–51, 54-61, 64–66

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