THE DATASHEET OF

MAX1204BEAP+

maxim integrated™

MAX1204

5V, 8-Channel, Serial, 10-Bit ADC with 3V Digital Interface

General Description

The MAX1204 is a 10-bit data-acquisition system specifically designed for use in applications with mixed +5V (analog) and +3V (digital) supply voltages. It operates with a single +5V analog supply or dual ±5V analog supplies, and combines an 8-channel multiplexer, internal track/hold, and serial interface with high conversion speed and low power consumption.

A 4-wire serial interface connects directly to SPI/MICROWIRE® devices without external logic, and a serial strobe output allows direct connection to TMS320-family digital signal processors. The MAX1204 uses either the internal clock or an external serial-interface clock to perform successive-approximation analog-to-digital conversions. The serial interface operates at up to 2MHz.

The MAX1204 features an internal 4.096V reference and a reference-buffer amplifier that simplifies gain trim. It also has a V_L pin that supplies power to the digital outputs. Output logic levels (3V, 3.3V, or 5V) are determined by the value of the voltage applied to this pin.

A hard-wired $\overline{SHDN}$ pin and two software-selectable power-down modes are provided. Accessing the serial interface automatically powers up the device. A quick turn-on time allows the MAX1204 to be shut down between conversions, enabling the user to optimize supply currents. By customizing power-down between conversions, supply current can drop below 10µA at reduced sampling rates.

The MAX1204 is available in 20-pin SSOP and PDIP packages, and is specified for the commercial and extended temperature ranges.

Applications

5V/3V Mixed-Supply Systems

Data Acquisition

Process Control

Battery-Powered Instruments

Medical Instruments

Typical Operating Circuit appears on last page.

MICROWIRE is a registered trademark of National Semiconductor Corp.

Features

- **8-Channel Single-Ended or 4-Channel Differential Inputs**
- **Operates from +5V Single or ±5V Dual Supplies**
- **User-Adjustable Output Logic Levels (2.7V to 5.25V)**
- **Low Power: 1.5mA (Operating Mode)**
  2µA (Power-Down Mode)
- **Internal Track/Hold, 133kHz Sampling Rate**
- **Internal 4.096V Reference**
- **SPI/MICROWIRE/TMS320-Compatible 4-Wire Serial Interface**
- **Software-Configurable Unipolar/Bipolar Inputs**
- **20-Pin PDIP/SSOP**
- **Pin-Compatible 12-Bit Upgrade: MAX1202**

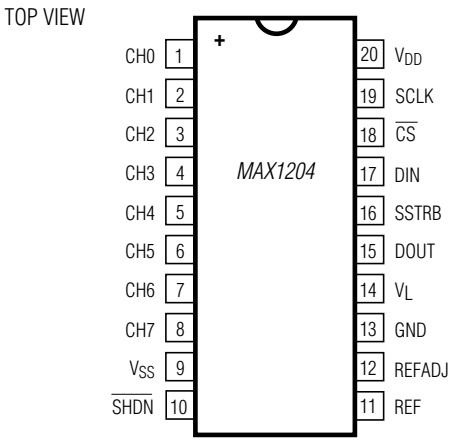
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX1204ACPP+	0°C to +70°C	20 PDIP	±1/2
MAX1204BCPP+	0°C to +70°C	20 PDIP	±1
MAX1204ACAP+	0°C to +70°C	20 SSOP	±1/2
MAX1204BCAP+	0°C to +70°C	20 SSOP	±1

Ordering Information continued at end of data sheet.

+Denotes a lead(Pb)-free/RoHS-compliant package.

Pin Configuration



PDIP/SSOP

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-1179; Rev 1; 1/12

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
V_L .....-0.3V to (V_{DD} + 0.3V)
V_{SS} to GND .....+0.3V to -6V
V_{DD} to V_{SS} .....-0.3V to +12V
CH0–CH7 to GND .....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
CH0–CH7 Total Input Current .....±20mA
REF to GND .....-0.3V to (V_{DD} + 0.3V)
REFADJ to GND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to GND .....-0.3V to (V_{DD} + 0.3V)
Digital Outputs to GND .....-0.3V to (V_L + 0.3V)
Digital Output Sink Current 25mA
Continuous Power Dissipation (T_A = +70°C)
PDIP (derate 11.11mW/°C above +70°C) 889mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
Operating Temperature Ranges
MAX1204_C_P .....0°C to +70°C
MAX1204_E_P .....-40°C to +85°C
Storage Temperature Range .....-60°C to +150°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, V_L = 2.7V to 3.6V; V_{SS} = 0V or -5V ±5%; f_{SCLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); 4.7µF capacitor at REF; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution			10			Bits
Relative Accuracy (Note 2)	INL	MAX1204A			±0.5	LSB
		MAX1204B			±1.0	
Differential Nonlinearity	DNL	No missing codes over temperature			±1.0	LSB
Offset Error		MAX1204A			±1.0	LSB
		MAX1204B			±2.0	
Gain Error (Note 3)		MAX1204A			±1.0	LSB
		MAX1204B			±2.0	
Gain Temperature Coefficient		External reference, 4.096V		±0.8		ppm/°C
Channel-to-Channel Offset Matching				±0.1		LSB
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, 4.096V_{P-P}, 133ksps, 2.0MHz external clock, bipolar input mode)						
Signal-to-Noise + Distortion Ratio	SINAD			66		dB
Total Harmonic Distortion (up to the 5th harmonic)	THD			-70		dB
Spurious-Free Dynamic Range	SFDR			70		dB
Channel-to-Channel Crosstalk		V_{IN} = 4.096V_{P-P}, 65kHz (Note 4)		-75		dB
Small-Signal Bandwidth		-3dB rolloff		4.5		MHz
Full-Power Bandwidth				800		kHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, V_L = 2.7V to 3.6V; V_{SS} = 0V or -5V ±5%; f_{SCLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); 4.7µF capacitor at REF; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONVERSION RATE						
Conversion Time (Note 5)	t_{CONV}	Internal clock	5.5		10	µs
		External clock, 2MHz, 12 clocks/conversion	6			
Track/Hold Acquisition Time	t_{ACQ}		1.5			µs
Aperture Delay				10		ns
Aperture Jitter				<50		ps
Internal Clock Frequency				1.7		MHz
External Clock-Frequency Range		External compensation mode, 4.7µF	0.1		2.0	MHz
		Internal compensation mode (Note 6)	0.1		0.4	
		Used for data transfer only	0		2.0	
ANALOG INPUT						
Input Voltage Range, Single-Ended and Differential (Note 7)		Unipolar, V_{SS} = 0V			V_{REF}	V
		Bipolar, V_{SS} = -5V			$\pm V_{REF} / 2$	
Multiplexer Leakage Current		On/off leakage current, $V_{CH\_}$ = ±5V		±0.01	±1	µA
Input Capacitance		(Note 6)		16		pF
INTERNAL REFERENCE						
REF Output Voltage		T_A = +25°C	4.076	4.096	4.116	V
REF Short-Circuit Current					30	mA
V_{REF} Temperature Coefficient		MAX1204AC		±30	±50	ppm/°C
		MAX1204AE		±30	±60	
		MAX1204B		±30		
Load Regulation (Note 8)		0mA to 0.5mA output load		2.5		mV
Capacitive Bypass at REF		Internal compensation mode	0			µF
		External compensation mode	4.7			
Capacitive Bypass at REFADJ			0.01			µF
REFADJ Adjustment Range				±1.5		%
EXTERNAL REFERENCE AT REF (Buffer disabled, V_{REF} = 4.096V)						
Input Voltage Range			2.50		V_{DD} + 50mV	V
Input Current				200	350	µA
Input Resistance			12	20		kΩ
REF Input Current in Shutdown		$V_{\overline{SHDN}}$ = 0V		1.5	10	µA
REFADJ Buffer Disable Threshold			V_{DD} - 50mV			V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, V_L = 2.7V to 3.6V; V_{SS} = 0V or -5V ±5%; f_{SCLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); 4.7µF capacitor at REF; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXTERNAL REFERENCE AT REFADJ						
Capacitive Bypass at REF		Internal compensation mode	0			µF
		External compensation mode	4.7			
Reference-Buffer Gain				1.68		V/V
REFADJ Input Current					±50	µA
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}			5 ±5%		V
Negative Supply Voltage	V_{SS}			0 or -5 ±5%		V
Positive Supply Current	I_{DD}	Operating mode		1.5	2.5	mA
		Fast power-down (Note 9)		30	70	µA
		Full power-down (Note 9)		2	10	
Negative Supply Current	I_{SS}	Operating mode and fast power-down			50	µA
		Full power-down			10	
Logic Supply Voltage	V_L		2.70		5.25	V
Logic Supply Current (Notes 6, 10)	I_{VL}	V_L = V_{DD} = 5V			10	µA
Positive Supply Rejection (Note 11)	PSR	V_{DD} = 5V ±5%; external reference, 4.096V; full-scale input		±0.06	±0.5	mV
Negative Supply Rejection (Note 11)	PSR	V_{SS} = -5V ±5%; external reference, 4.096V; full-scale input		±0.01	±0.5	mV
Logic Supply Rejection (Note 12)	PSR	External reference, 4.096V; full-scale input		±0.06	±0.5	mV

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, V_L = 2.7V to 5.25V; V_{SS} = 0V or -5V ±5%; f_{SCLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); 4.7µF capacitor at REF; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS: DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$						
DIN, SCLK, $\overline{CS}$ Input High Voltage	V_{IH}		2.0			V
DIN, SCLK, $\overline{CS}$ Input Low Voltage	V_{IL}				0.8	V
DIN, SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}			0.15		V
DIN, SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}			±1	µA
DIN, SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 6)			15	pF
$\overline{SHDN}$ Input High Voltage	V_{SH}		V_{DD} - 0.5			V
$\overline{SHDN}$ Input Mid-Voltage	V_{SM}		1.5		V_{DD} - 1.5	V
$\overline{SHDN}$ Voltage, Open	V_{FLT}	$\overline{SHDN}$ = open		2.75		V
$\overline{SHDN}$ Input Low Voltage	V_{SL}				0.5	V
$\overline{SHDN}$ Input Current, High	I_{SH}	$\overline{SHDN}$ = V_{DD}			4.0	µA
$\overline{SHDN}$ Input Current, Low	I_{SL}	$V_{\overline{SHDN}}$ = 0V	-4.0			µA
$\overline{SHDN}$ Maximum Allowed Leakage, Mid-Input		$\overline{SHDN}$ = open	-100		100	nA
DIGITAL OUTPUTS: DOUT, SSTRB (V_L = 2.7V to 3.6V)						
Output Voltage Low	V_{OL}	I_{SINK} = 3mA			0.4	V
		I_{SINK} = 6mA		0.3		
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA	V_L - 0.5			V
Three-State Leakage Current	I_L	$\overline{CS}$ = V_L			±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = V_L (Note 6)			15	pF
DIGITAL OUTPUTS: DOUT, SSTRB (V_L = 4.75V to 5.25V)						
Output Voltage Low	V_{OL}	I_{SINK} = 5mA			0.4	V
		I_{SINK} = 8mA		0.3		
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA	4			V
Three-State Leakage Current	I_L	$V_{\overline{CS}}$ = 5V			±10	µA
Three-State Output Capacitance	C_{OUT}	$V_{\overline{CS}}$ = 5V (Note 6)			15	pF

TIMING CHARACTERISTICS

(V_{DD} = +5V ±5%, V_L = 2.7V to 3.6V, V_{SS} = 0V or -5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Acquisition Time	t_{ACQ}		1.5			µs
DIN to SCLK Setup	t_{DS}		100			ns
DIN to SCLK Hold	t_{DH}				0	ns
SCLK Fall to Output Data Valid	t_{DO}	C_{LOAD} = 100pF	20		240	ns
$\overline{CS}$ Fall to Output Enable	t_{DV}	C_{LOAD} = 100pF			240	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	C_{LOAD} = 100pF			240	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}		100			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}		0			ns
SCLK Pulse Width High	t_{CH}		200			ns
SCLK Pulse Width Low	t_{CL}		200			ns
SCLK Fall to SSTRB	t_{SSTRB}	C_{LOAD} = 100pF			240	ns
$\overline{CS}$ Fall to SSTRB Output Enable (Note 6)	t_{SDV}	External clock mode only, C_{LOAD} = 100pF			240	ns
$\overline{CS}$ Rise to SSTRB Output Disable (Note 6)	t_{STR}	External clock mode only, C_{LOAD} = 100pF			240	ns
SSTRB Rise to SCLK Rise (Note 6)	t_{SCK}	Internal clock mode only	0			ns

Note 1: Tested at V_{DD} = 5.0V; V_{SS} = 0V; unipolar input mode.

Note 2: Relative accuracy is the analog value's deviation (at any code) from its theoretical value after the full-scale range is calibrated.

Note 3: Internal reference, offset nulled.

Note 4: On-channel grounded; sine-wave applied to all off-channels.

Note 5: Conversion time is defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.

Note 6: Guaranteed by design. Not subject to production testing.

Note 7: Common-mode range for analog inputs is from V_{SS} to V_{DD}.

Note 8: External load should not change during the conversion for specified accuracy.

Note 9: Shutdown supply current is measured with V_L at 3.3V, and with all digital inputs tied to either V_L or GND (Figure 12c); REFADJ = GND.

Note 10: Logic supply current is measured with the digital outputs (DOUT and SSTRB) disabled ($\overline{CS}$ high). When the outputs are active ($\overline{CS}$ low), the logic supply current depends on f_{SCLK}, and on the static and capacitive load at DOUT and SSTRB.

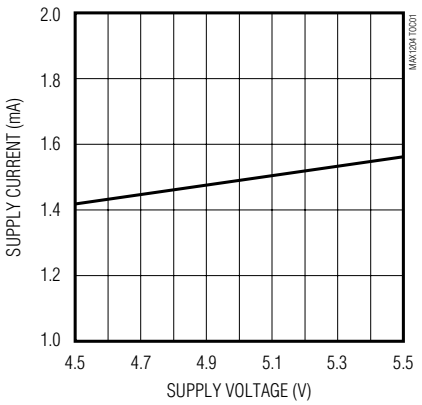
Note 11: Measured at V_{SUPPLY} +5% and V_{SUPPLY} -5% only.

Note 12: Measured at V_L = 2.7V and V_L = 3.6V.

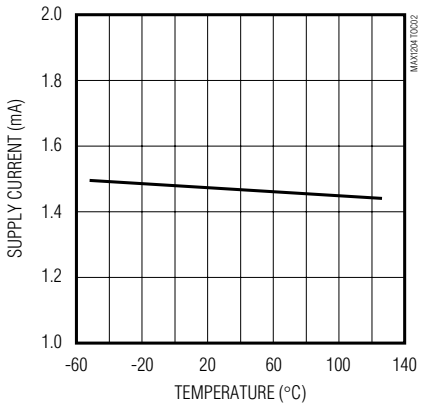
Typical Operating Characteristics

(V_{DD} = 5V ±5%; V_L = 2.7V to 3.6V; f_{SCLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); 4.7µF capacitor at REF; T_A = +25°C; unless otherwise noted.)

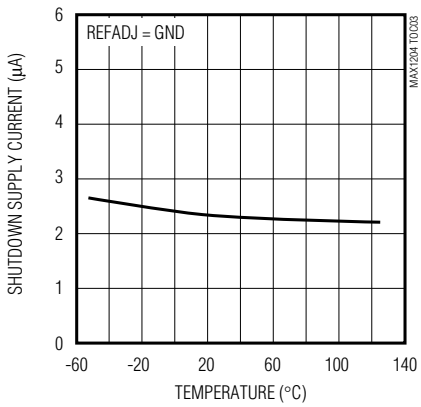
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1–8	CH0–CH7	Sampling Analog Inputs
9	V_{SS}	Negative Supply Voltage. Tie V_{SS} to -5V ±5% or GND.
10	$\overline{SHDN}$	Three-Level Shutdown Input. Pulling $\overline{SHDN}$ low shuts the MAX1204 down to 10µA (max) supply current; otherwise, the MAX1204 is fully operational. Pulling $\overline{SHDN}$ to V_{DD} puts the reference-buffer amplifier in internal compensation mode. Letting $\overline{SHDN}$ float puts the reference-buffer amplifier in external compensation mode.
11	REF	Reference Buffer Output/ADC Reference Input. In internal reference mode, the reference buffer provides a 4.096V nominal output, externally adjustable at REFADJ. In external reference mode, disable the internal buffer by pulling REFADJ to V_{DD}.
12	REFADJ	Input to the Reference-Buffer Amplifier. Tie REFADJ to V_{DD} to disable the reference-buffer amplifier.
13	GND	Ground; IN- Input for Single-Ended Conversions
14	V_L	Supply Voltage for Digital Output Pins. Voltage applied to V_L determines the positive output swing of the Digital Outputs (DOUT, SSTRB).
15	DOUT	Serial-Data Output. Data is clocked out at SCLK's falling edge. High impedance when $\overline{CS}$ is high.
16	SSTRB	Serial-Strobe Output. In internal clock mode, SSTRB goes low when the MAX1204 begins the analog-to-digital conversion and goes high when the conversion is finished. In external clock mode, SSTRB pulses high for one clock period before the MSB decision. High impedance when $\overline{CS}$ is high (external clock mode).
17	DIN	Serial-Data Input. Data is clocked in at SCLK's rising edge.
18	$\overline{CS}$	Active-Low Chip Select. Data is not clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance.
19	SCLK	Serial-Clock Input. SCLK clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed. (Duty cycle must be 40% to 60% in external clock mode.)
20	V_{DD}	Positive Supply Voltage, +5V ±5%

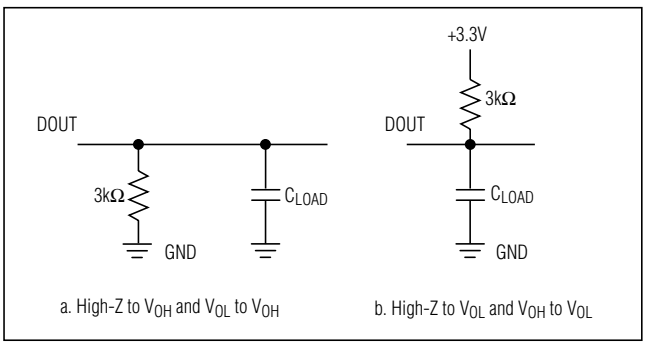


Figure 1. Load Circuits for Enable Time

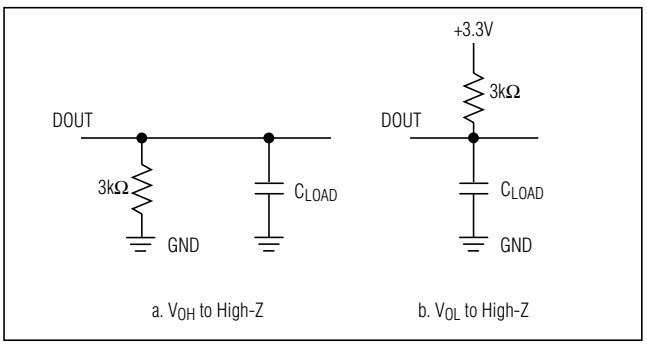


Figure 2. Load Circuits for Disable Time

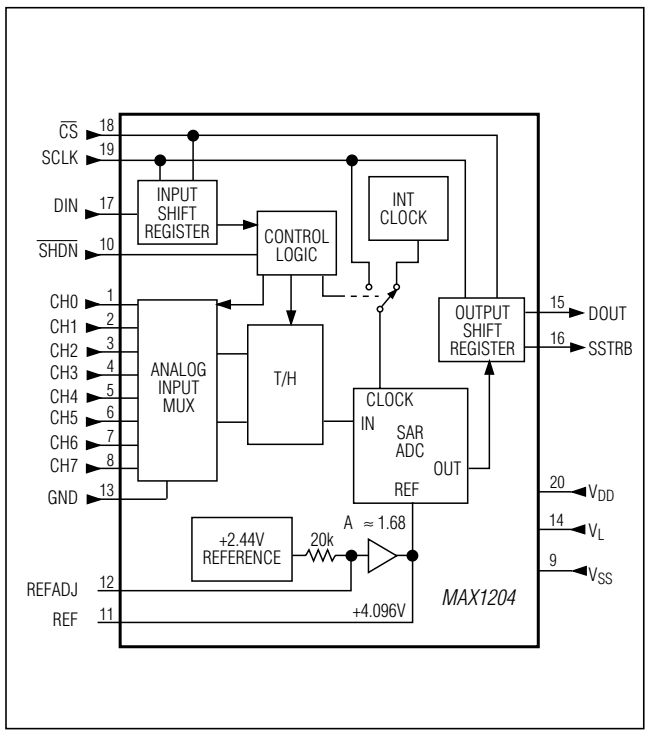


Figure 3. Block Diagram

Detailed Description

The MAX1204 uses a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to a 10-bit digital output. A flexible serial interface provides easy interface to 3V microprocessors (µPs). Figure 3 is the MAX1204 block diagram.

Pseudo-Differential Input

Figure 4 shows the analog-to-digital converter's (ADC's) analog comparator's sampling architecture. In single-ended mode, IN+ is internally switched to CH0–CH7 and IN- is switched to GND. In differential mode, IN+ and IN- are selected from pairs of CH0/CH1, CH2/CH3, CH4/CH5, and CH6/CH7. Configure the channels using Tables 3 and 4.

In differential mode, IN- and IN+ are internally switched to either of the analog inputs. This configuration is pseudo-differential such that only the signal at IN+ is sampled. The return side (IN-) must remain stable within ±0.5 LSB (±0.1 LSB for best results) with respect to GND during a conversion. To do this, connect a 0.1µF capacitor from IN- (of the selected analog input) to GND.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor C_{HOLD}. The acquisition interval spans three SCLK cycles and ends on the falling SCLK edge after the input control word's last bit is entered. The T/H switch opens at the end of the acquisition interval, retaining charge on C_{HOLD} as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching C_{HOLD} from the positive input (IN+) to the negative input (IN-). In single-ended mode, IN- is simply GND. This unbalances node ZERO at the comparator's input. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 10-bit resolution. This action is equivalent to transferring a charge of 16pF x $[(V_{IN}+) - (V_{IN}-)]$ from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

Track/Hold

The T/H enters tracking mode on the falling clock edge after the fifth bit of the 8-bit control word is shifted in. The T/H enters hold mode on the falling clock edge after the eighth bit of the control word is shifted in. IN- is connected to GND if the converter is set up for single-ended inputs, and the converter samples the "+" input. IN- connects to the "-" input if the converter is set up for differential inputs, and the difference of |IN+ - IN-| is sampled. The positive input connects back to IN+ at the end of the conversion, and C_{HOLD} charges to the input signal.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, acquisition time increases and more time must be allowed between conversions. The acquisition time, t_{ACQ}, is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired. It is calculated by the following:

$$t_{ACQ} = 7 \times (R_S + R_{IN}) \times 16pF$$

where R_{IN} = 9kΩ, R_S = the source impedance of the input signal, and t_{ACQ} is never less than 1.5µs. Note that source impedances below 4kΩ do not significantly affect the ADC's AC performance. Higher source impedances can be used if an input capacitor is connected to the analog inputs, as shown in Figure 5. Note that the input capacitor forms an RC filter with the input source impedance, limiting the ADC's signal bandwidth.

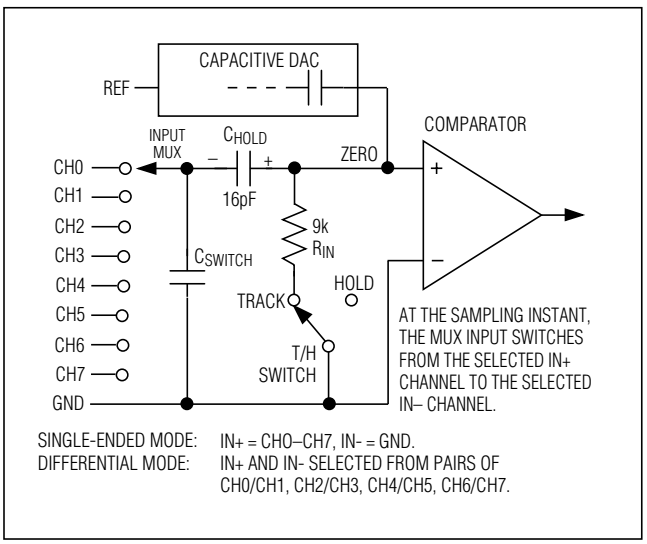


Figure 4. Equivalent Input Circuit

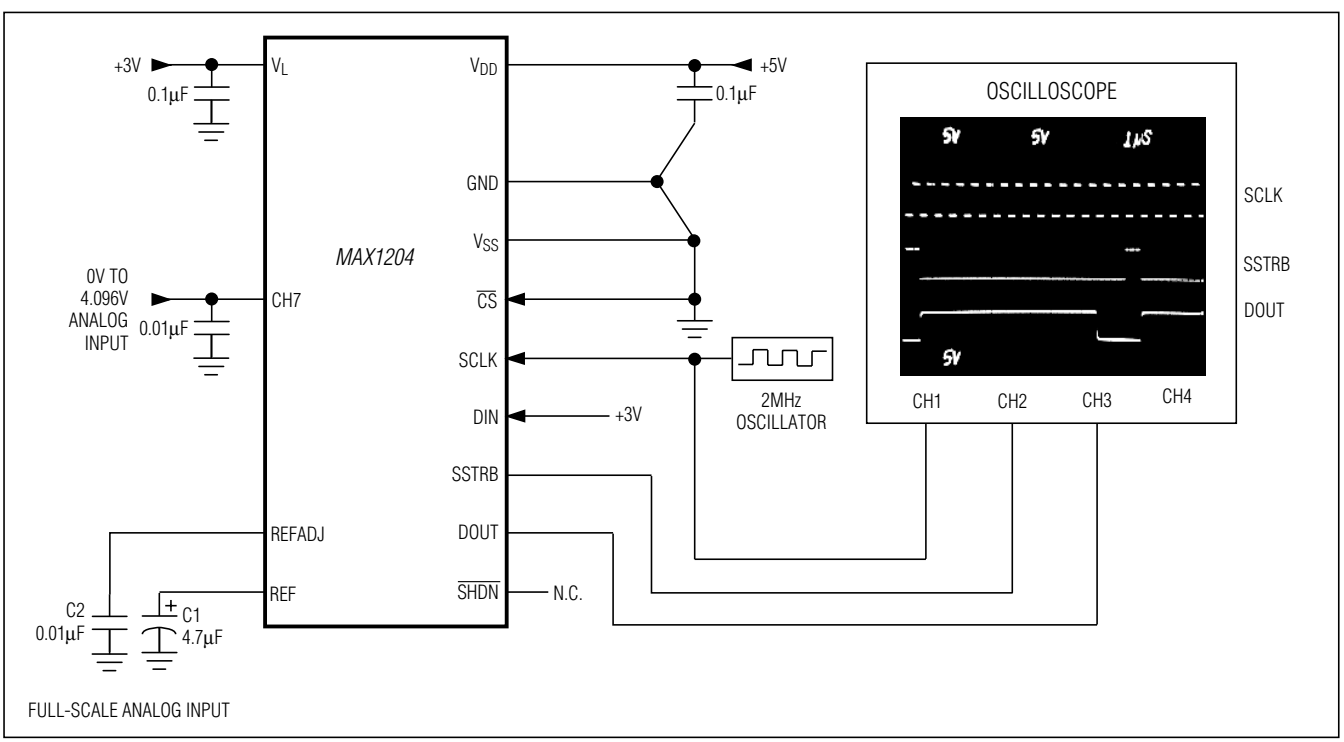


Figure 5. Quick-Look Circuit

Table 1a. Unipolar Full Scale and Zero Scale

REFERENCE		ZERO SCALE	FULL SCALE
Internal		0V	+4.096V
External	at REFADJ	0V	V_{REFADJ} x 1.68
	at REF	0V	V_{REF}

Table 1b. Bipolar Full Scale, Zero Scale, and Negative Full Scale

REFERENCE		NEGATIVE FULL SCALE	ZERO SCALE	FULL SCALE
Internal		-4.096V/2	0V	+4.096V / 2
External	at REFADJ	-1/2 V_{REFADJ} x 1.68	0V	+1/2 V_{REFADJ} x 1.68
	at REF	-1/2 V_{REF}	0V	+1/2 V_{REF}

Input Bandwidth

The ADC's input tracking circuitry has a 4.5MHz small-signal bandwidth. Therefore, it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Range and Input Protection

Internal protection diodes, which clamp the analog inputs to V_{DD} and V_{SS}, allow the analog input pins to swing from (V_{SS} - 0.3V) to (V_{DD} + 0.3V) without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV, or be lower than V_{SS} by 50mV.

If the analog input exceeds 50mV beyond the supplies, do not forward bias the protection diodes of off-channels over 2mA, as excessive current degrades on-channel conversion accuracy.

The full-scale input voltage depends on the voltage at REF (Tables 1a and 1b).

Quick Look

Use the circuit of Figure 5 to quickly evaluate the MAX1204's analog performance. The MAX1204 requires that a control byte be written to DIN before each conversion. Tying DIN to +3V feeds in control byte $FF hex, which triggers single-ended unipolar conversions on CH7 in external clock mode without powering down between conversions. In external clock mode, the SSTRB output pulses high for one clock period before the most significant bit of the conversion result shifts out of DOUT. Varying the analog input to CH7 alters the sequence of bits from DOUT. A total of 15 clock cycles per conversion is required. All SSTRB and DOUT output transitions occur on SCLK's falling edge.

How to Start a Conversion

Clocking a control byte into DIN starts conversion on the MAX1204. With $\overline{CS}$ low, each rising edge on SCLK clocks a bit from DIN into the MAX1204's internal shift register. After $\overline{CS}$ falls, the first logic "1" bit defines the control byte's MSB. Until this first "start" bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 2 shows the control-byte format.

The MAX1204 is fully compatible with MICROWIRE and SPI devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. MICROWIRE and SPI both transmit a byte and receive a byte at the same time. Using the *Typical Operating Circuit*, the simplest software interface requires only three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the conversion result).

Table 2. Control-Byte Format

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
START	SEL 2	SEL 1	SEL 0	UNI/$\overline{BIP}$	SGL/$\overline{DIF}$	PD1	PD0

Bit	Name	Description
7 (MSB)	START	The first logic **1** bit after $\overline{CS}$ goes low defines the beginning of the control byte.
6 5 4	SEL2 SEL1 SEL0	These three bits select which of the eight channels is used for the conversion (Tables 3 and 4).
3	UNI/$\overline{BIP}$	**1** = unipolar, **0** = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, an analog input signal from 0V to V_{REF} can be converted; in bipolar mode, the signal can range from $-V_{REF}$ / 2 to $+V_{REF}$ / 2.
2	SGL/$\overline{DIF}$	**1** = single ended, **0** = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to GND. In differential mode, the voltage difference between two channels is measured. (Tables 3 and 4.)
1 0 (LSB)	PD1 PD0	Selects clock and power-down modes. PD1 PD0 Mode **0** **0** Full power-down (I_{DD} = 2µA, internal reference) **0** **1** Fast power-down (I_{DD} = 30µA, internal reference) **1** **0** Internal clock mode **1** **1** External clock mode

Table 3. Channel Selection in Single-Ended Mode (SGL/$\overline{DIF}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	GND
0	0	0	+								–
1	0	0		+							–
0	0	1			+						–
1	0	1				+					–
0	1	0					+				–
1	1	0						+			–
0	1	1							+		–
1	1	1								+	–

Table 4. Channel Selection in Differential Mode (SGL/$\overline{DIF}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	+	–						
0	0	1			+	–				
0	1	0					+	–		
0	1	1							+	–
1	0	0	–	+						
1	0	1			–	+				
1	1	0					–	+		
1	1	1							–	+

Simple Software Interface

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 100kHz to 2MHz.

1) Set up the control byte for external clock mode and call it TB1. TB1's format should be: 1XXXXX11 binary, where the Xs denote the particular channel and conversion mode selected.
2) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ on the MAX1204 low.
3) Transmit TB1 and simultaneously receive a byte and call it RB1. Ignore RB1.
4) Transmit a byte of all zeros ($00 hex) and simultaneously receive byte RB2.
5) Transmit a byte of all zeros ($00 hex) and simultaneously receive byte RB3.
6) Pull $\overline{CS}$ on the MAX1204 high.

Figure 6 shows the timing for this sequence. Bytes RB2 and RB3 contain the result of the conversion padded with one leading zero, two trailing sub-bits (S1 and S0), and three trailing zeros. Total conversion time is a function of the serial clock frequency and the amount of idle time between 8-bit transfers. To avoid excessive T/H droop, make sure that the total conversion time does not exceed 120µs.

Digital Output

In unipolar input mode, the output is straight binary (Figure 15); for bipolar inputs, the output is two's-complement (Figure 16). Data is clocked out at SCLK's falling edge in MSB-first format. The digital output logic level is adjusted with the V_L pin. This allows DOUT and SSTRB to interface with 3V logic without the risk of overdrive. The MAX1204's digital inputs are designed to be compatible with 3V CMOS logic as well as 5V logic.

Internal and External Clock Modes

The MAX1204 can use either an external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the MAX1204. The T/H acquires the input signal as the last three bits of the control byte are clocked into DIN. Bits PD1 and PD0 of the control byte program the clock mode. Figures 7–10 show the timing characteristics common to both modes.

External Clock

In external clock mode, the external clock not only shifts data in and out, but it also drives the A/D conversion steps. SSTRB pulses high for one clock period after the last bit of the control byte. Successive-approximation bit decisions are made and appear at DOUT on each of the next 12 SCLK falling edges (Figure 6). SSTRB and DOUT go into a high-impedance state when $\overline{CS}$ goes high; after the next $\overline{CS}$ falling edge, SSTRB outputs a logic low. Figure 8 shows the SSTRB timing in external clock mode.

The conversion must complete in some minimum time or droop on the sample-and-hold can degrade conversion results. Use internal clock mode if the clock period exceeds 10µs or if serial-clock interruptions could cause the conversion interval to exceed 120µs.

Internal Clock

In internal clock mode, the MAX1204 generates its own conversion clock. This frees the µP from running the SAR conversion clock, and allows the conversion results to be read back at the processor's convenience, at any clock rate from zero to 2MHz. SSTRB goes low at the start of the conversion, then goes high when the conversion is complete. SSTRB is low for a maximum of 10µs, during which time SCLK should remain low for best noise performance. An internal register stores data while the conversion is in progress. SCLK clocks the data out at this register at any time after the conversion is complete. After SSTRB goes high, the next falling clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (Figure 9). $\overline{CS}$ does not need to be held low once a conversion is started. Pulling $\overline{CS}$ high prevents data from being clocked into the MAX1204 and three-states DOUT, but it does not adversely affect an internal clock-mode conversion already in progress. When internal clock mode is selected, SSTRB does not go high impedance when $\overline{CS}$ goes high.

Figure 10 shows the SSTRB timing in internal clock mode. Data can be shifted in and out of the MAX1204 at clock rates up to 2.0MHz if the acquisition time, t_{ACQ}, is kept above 1.5µs.

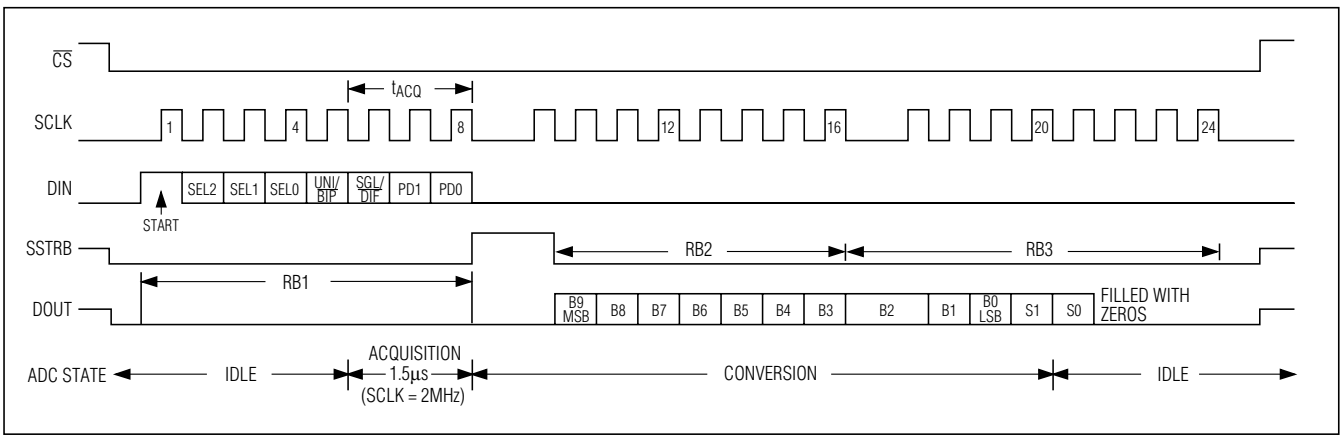


Figure 6. 24-Bit External-Clock-Mode Conversion Timing (Microwire/SPI Compatible)

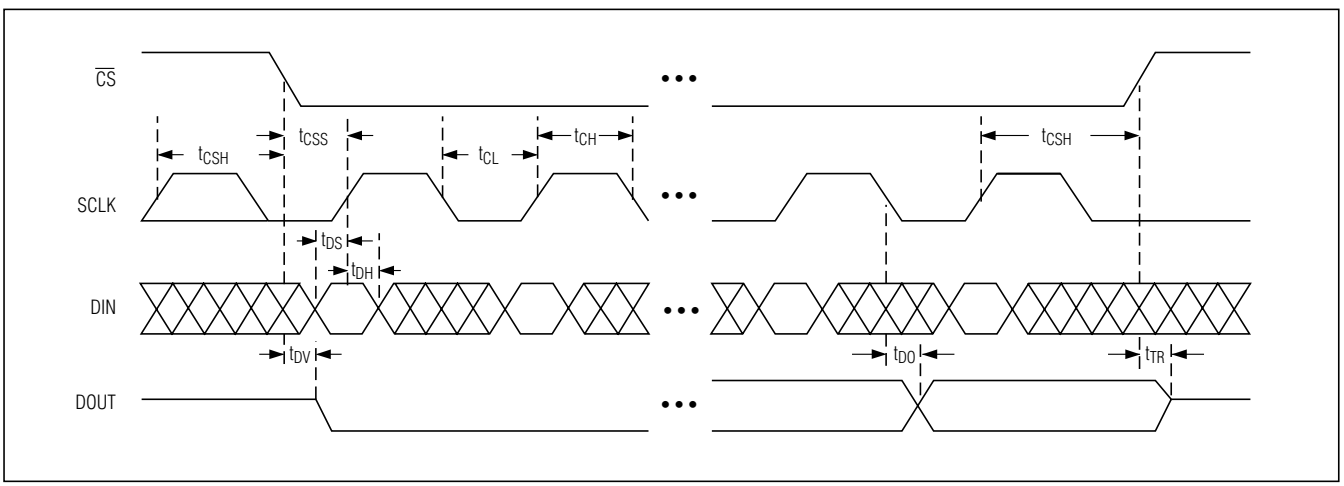


Figure 7. Detailed Serial-Interface Timing

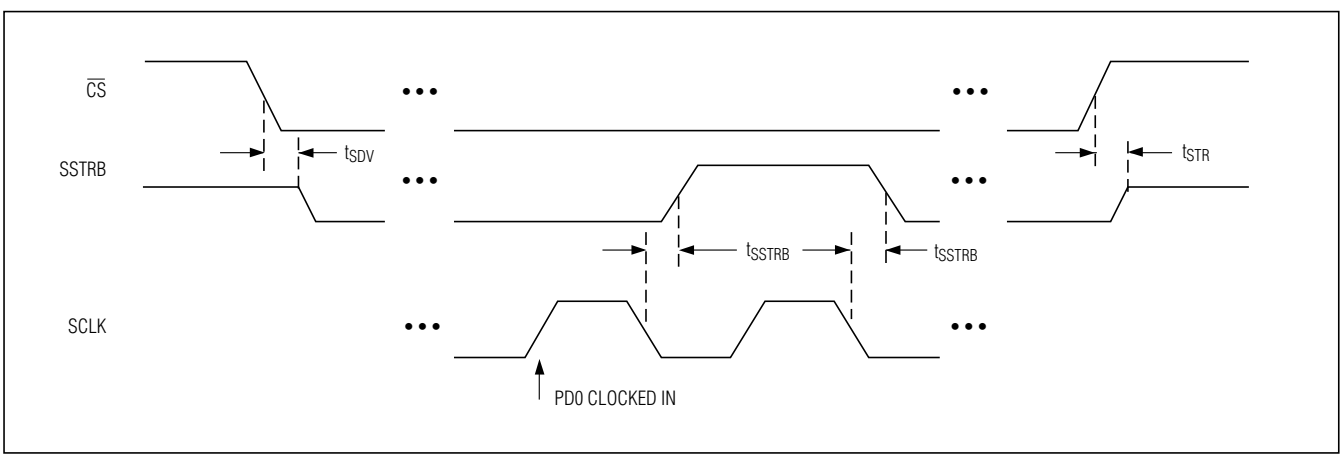


Figure 8. External Clock-Mode SSTRB Detailed Timing

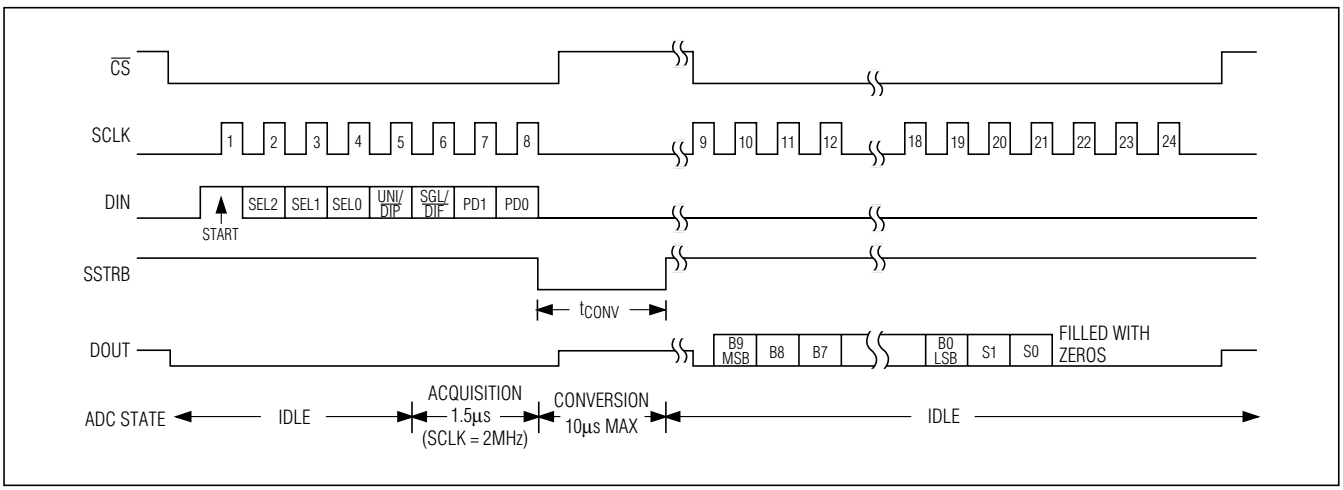


Figure 9. Internal Clock Mode Timing

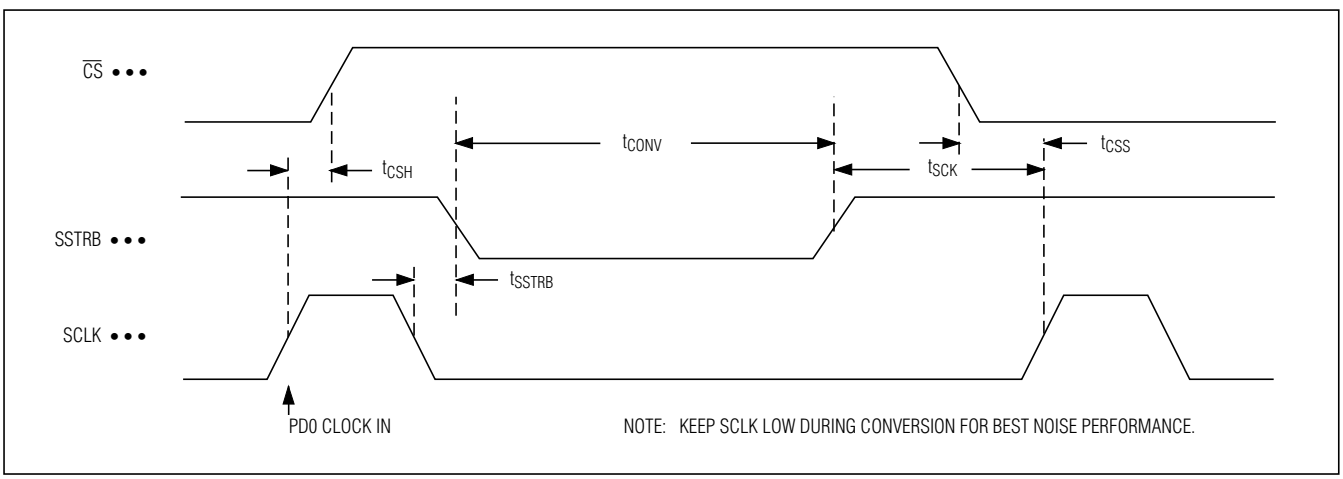


Figure 10. Internal Clock Mode SSTRB Detailed Timing

Data Framing

$\overline{CS}$'s falling edge does **not** start a conversion on the MAX1204. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on SCLK's falling edge after the eighth bit of the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as:

The first high bit clocked into DIN with $\overline{CS}$ low anytime the converter is idle; (e.g., after V_{DD} is applied).

or

The first high bit clocked into DIN after bit 3 (B3) of a conversion in progress appears at DOUT.

If a falling edge on $\overline{CS}$ forces a start bit before B3 becomes available, the current conversion is terminated and a new one started. Thus, the fastest the MAX1204 can run is 15 clocks/conversion. Figure 11a shows the serial-interface timing necessary to perform a conversion every 15 SCLK cycles in external clock mode. If $\overline{CS}$ is low and SCLK is continuous, guarantee a start bit by first clocking in 16 zeros.

Most microcontrollers (µCs) require that conversions occur in multiples of eight SCLK clocks; 16 clocks per conversion is typically the fastest that a µC can drive the MAX1204. Figure 11b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

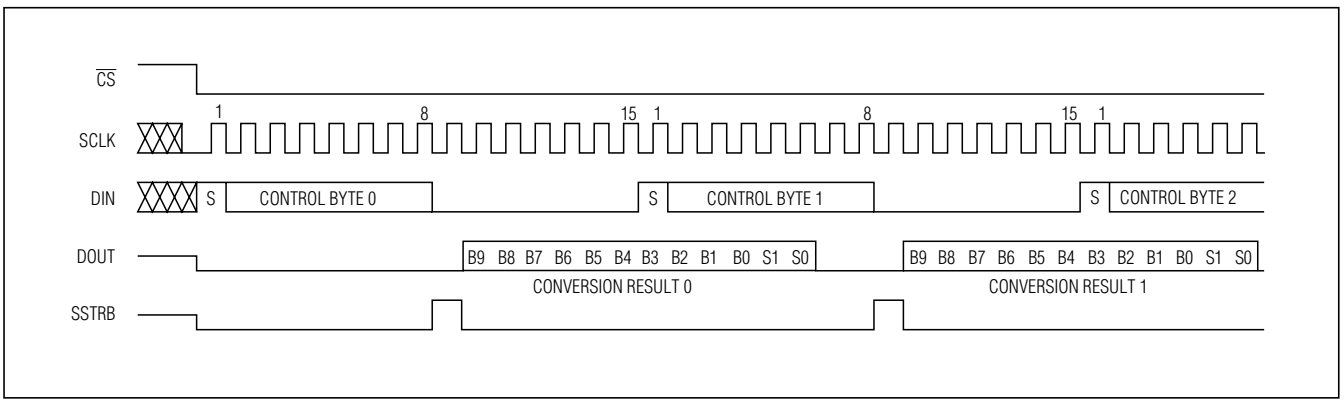


Figure 11a. External Clock Mode, 15 Clocks/Conversion Timing

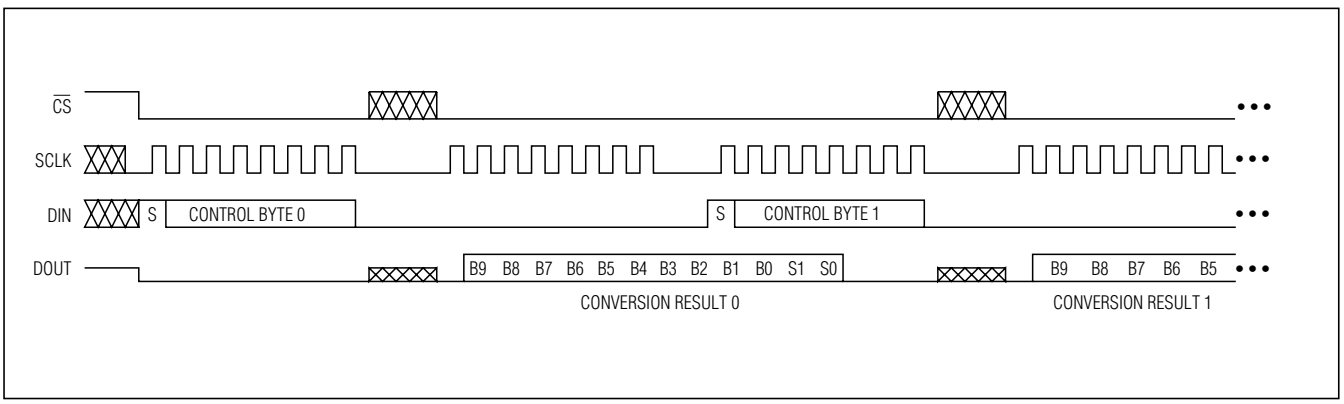


Figure 11b. External Clock Mode, 16 Clocks/Conversion Timing

Applications Information

Power-On Reset

When power is first applied and if $\overline{SHDN}$ is not pulled low, internal power-on reset circuitry activates the MAX1204 in internal clock mode, ready to convert with SSTRB = high. After the power supplies are stabilized, the internal reset time is 100µs. No conversions should be performed during this phase. SSTRB is high on power-up, and if $\overline{CS}$ is low, the first logical 1 on DIN is interpreted as a start bit. Until a conversion takes place, DOUT shifts out zeros.

Reference-Buffer Compensation

In addition to its shutdown function, $\overline{SHDN}$ also selects internal or external compensation. The compensation affects both power-up time and maximum conversion speed. Compensated or not, the minimum clock rate is 100kHz due to droop on the sample-and-hold.

Float $\overline{SHDN}$ to select external compensation. The *Typical Operating Circuit* uses a 4.7µF capacitor at REF. A value of 4.7µF or greater ensures stability and allows converter operation at the 2MHz full clock speed. External compensation increases power-up time (see the section *Choosing Power-Down Mode,* and Table 5).

Internal compensation requires no external capacitor at REF, and is selected by pulling $\overline{SHDN}$ high. Internal compensation allows for the shortest power-up times, but is only available using an external clock up to 400kHz.

Power-Down

Choosing Power-Down Mode

You can save power by placing the converter in a low-current shutdown state between conversions. Select full power-down or fast power-down mode via bits 1 and 0 of the DIN control byte with $\overline{SHDN}$ high or open (Tables 2 and 6). Pull $\overline{SHDN}$ low at any time to shut down the converter completely. $\overline{SHDN}$ overrides bits 1 and 0 of the control byte.

Full power-down mode turns off all chip functions that draw quiescent current, reducing I_{DD} and I_{SS} typically to 2µA.

Fast power-down mode turns off all circuitry except the bandgap reference. With fast power-down mode, the supply current is 30µA. Power-up time can be shortened to 5µs in internal compensation mode.

The I_{DD} shutdown current can increase if any digital input (DIN, SCLK, $\overline{CS}$) is held high in either power-down mode. The actual shutdown current depends on the state of the digital inputs, the voltage applied to the digital inputs (V_{IH}), the supply voltage (V_{DD}), and the operating temperature. Figure 12c shows the maximum I_{DD} increase for each digital input held high in power-down mode for different operating conditions. This current is cumulative, so if all three digital inputs are held high, the additional shutdown current is three times the value shown in Figure 12c.

In both software power-down modes, the serial interface remains operational, but the ADC does not convert. Table 5 shows how the choice of reference-buffer compensation and power-down mode affects both power-up delay and maximum sample rate.

In external compensation mode, power-up time is 20ms with a 4.7µF compensation capacitor (200ms with a 33µF capacitor) when the capacitor is initially fully discharged.

From fast power-down, start-up time can be eliminated by using low-leakage capacitors that do not discharge more than 1/2 LSB while shut down. In power-down, the capacitor has to supply the current into the reference (typically 1.5µA) and the transient currents at power-up.

Figures 12a and 12b show the various power-down sequences in both external and internal clock modes.

Software Power-Down

Software power-down is activated using bits PD1 and PD0 of the control byte. As shown in Table 6, PD1 and PD0 also specify clock mode. When software power-down is asserted, the ADC continues to operate in the last specified clock mode until the conversion is complete. The ADC then powers down into a low quiescent-current state. In internal clock mode, the interface remains active and conversion results can be clocked out even though the MAX1204 has already entered a software power-down.

The first logical 1 on DIN is interpreted as a start bit and powers up the MAX1204. Following the start bit, the control byte also determines clock and power-down modes. For example, if the control byte contains PD1 = 1, the chip remains powered up. If PD1 = 0, power-down resumes after one conversion.

Table 5. Typical Power-Up Delay Times

REFERENCE BUFFER	REFERENCE-BUFFER COMPENSATION MODE	REFERENCE CAPACITOR (µF)	POWER-DOWN MODE	POWER-UP DELAY (µs)	MAXIMUM SAMPLING RATE (ksps)
Enabled	Internal	—	Fast	5	26
Enabled	Internal	—	Full	300	26
Enabled	External	4.7	Fast/Full	See Figure 14c	133
Disabled	—	—	Fast	2	133
Disabled	—	—	Full	2	133

Table 6. Software Shutdown and Clock Mode

PD1	PD0	DEVICE MODE
1	1	External clock mode
1	0	Internal clock mode
0	1	Fast power-down mode
0	0	Full power-down mode

Table 7. Hard-Wired Shutdown and Compensation Mode

$\overline{SHDN}$ STATE	DEVICE MODE	REFERENCE-BUFFER COMPENSATION
V_{DD}	Enabled	Internal compensation
Open	Enabled	External compensation
GND	Full Power-Down	N/A

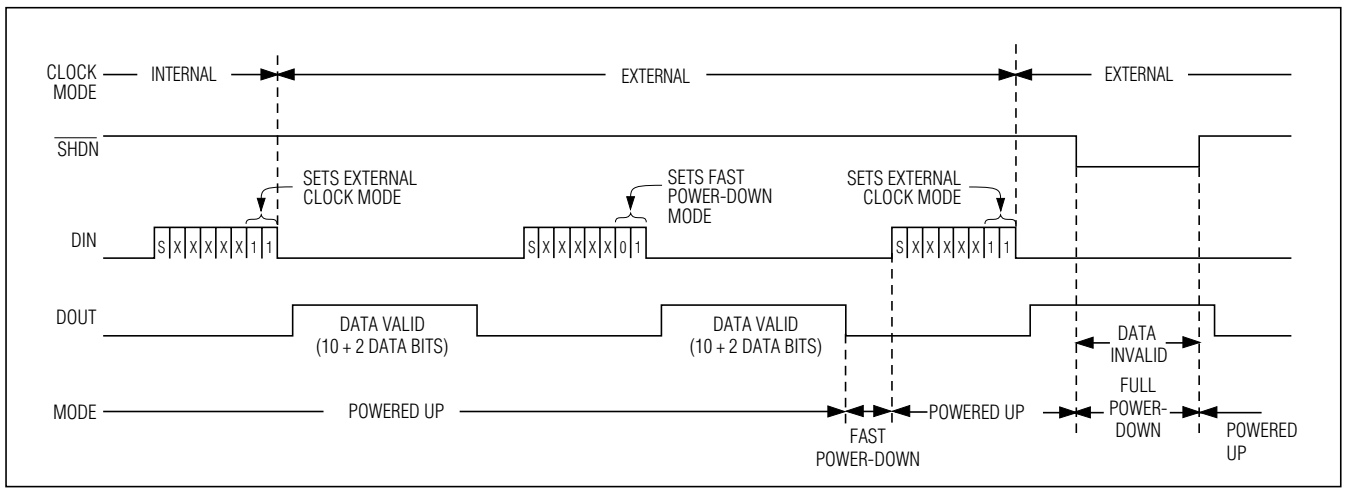


Figure 12a. Timing Diagram for Power-Down Modes (External Clock)

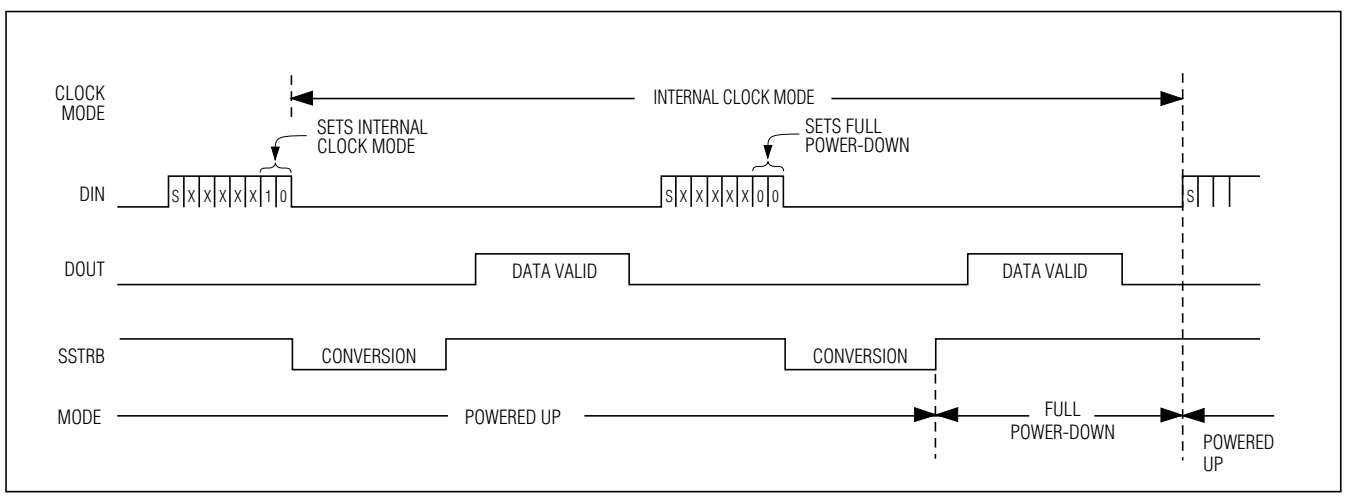


Figure 12b. Timing Diagram for Power-Down Modes (Internal Clock)

Hardware Power-Down

The $\overline{SHDN}$ pin places the converter into full power-down mode. Unlike the software power-down modes, conversion is not completed; it stops coincidentally with $\overline{SHDN}$ being brought low. There is no power-up delay if an external reference, which is not shut down, is used. $\overline{SHDN}$ also selects internal or external reference compensation (Table 7).

Power-Down Sequencing

The MAX1204's automatic power-down modes can save considerable power when operating at less than maximum sample rates. The following sections discuss the various power-down sequences.

Lowest Power at up to 500 Conversions per Channel per Second

Figure 14a depicts MAX1204's power consumption for one or eight channel conversions using full power-down mode and internal reference compensation. A 0.01µF bypass capacitor at REFADJ forms an RC filter with the internal 20kΩ reference resistor, with a 0.2ms time constant. To achieve full 10-bit accuracy, 10 time constants (or 2ms in this example) are required for the reference buffer to settle. When exiting FULLPD, waiting this 2ms in FASTPD mode (instead of just exiting FULLPD mode and returning to normal operating mode) reduces power consumption by a factor of 10 or more (Figure 13).

Lowest Power at Higher Throughputs

Figure 14b shows power consumption with external-reference compensation in fast power-down, with one and eight channels converted. The external 4.7µF compensation requires a 50µs wait after power-up. This circuit combines fast multichannel conversion with the lowest power consumption possible. Full power-down mode can increase power savings in applications where the MAX1204 is inactive for long periods of time, but where intermittent bursts of high-speed conversions are required.

External and Internal References

The MAX1204 can be used with an internal or external reference. An external reference can be connected directly at the REF terminal or at the REFADJ pin.

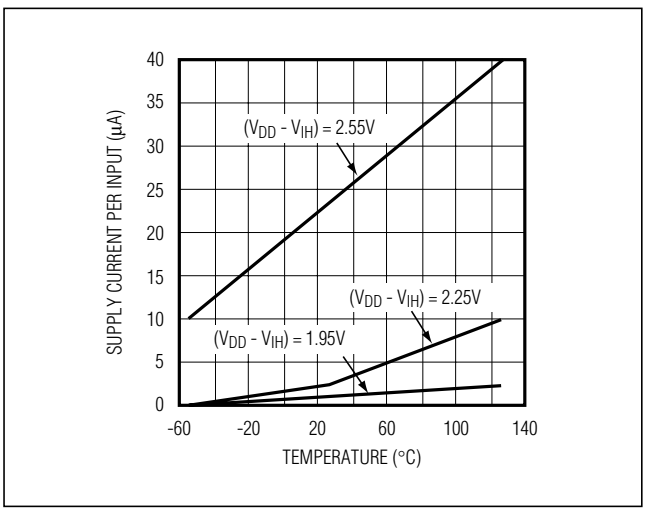


Figure 12c. Additional I_{DD} Shutdown Supply Current vs. V_{IH} for Each Digital Input at a Logic 1

An internal buffer is designed to provide 4.096V at REF for the MAX1204. Its internally trimmed 2.44V reference is buffered with a 1.68 nominal gain.

Internal Reference

The MAX1204's full-scale range with internal reference is 4.096V with unipolar inputs and ±2.048V with bipolar inputs. The internal reference voltage is adjustable to ±1.5% with the circuit of Figure 17.

External Reference

An external reference can be placed at either the input (REFADJ) or the output (REF) of the MAX1204's internal buffer amplifier. The REFADJ input impedance is typically 20kΩ. At REF, the input impedance is a minimum of 12kΩ for DC currents. During conversion, an external reference at REF must deliver up to 350µA DC load current and have an output impedance of 10Ω or less. If the reference has higher output impedance or is noisy, bypass it close to the REF pin with a 4.7µF capacitor.

Using the buffered REFADJ input makes buffering of the external reference unnecessary. To use the direct REF input, disable the internal buffer by tying REFADJ to V_{DD}. In power-down, the input bias current to REFADJ can be as much as 25µA with REFADJ tied to V_{DD}. Pull REFADJ to GND to minimize the input bias current in power-down.

Transfer Function and Gain Adjust

Figure 15 depicts the nominal, unipolar input/output (I/O) transfer function, and Figure 16 shows the bipolar I/O transfer function. Code transitions occur halfway between successive integer LSB values. Output coding is binary with 1 LSB = 4mV (4.096V/1024) for unipolar operation and 1 LSB = 4mV [(4.096V/2 - -4.096V/2)/1024] for bipolar operation.

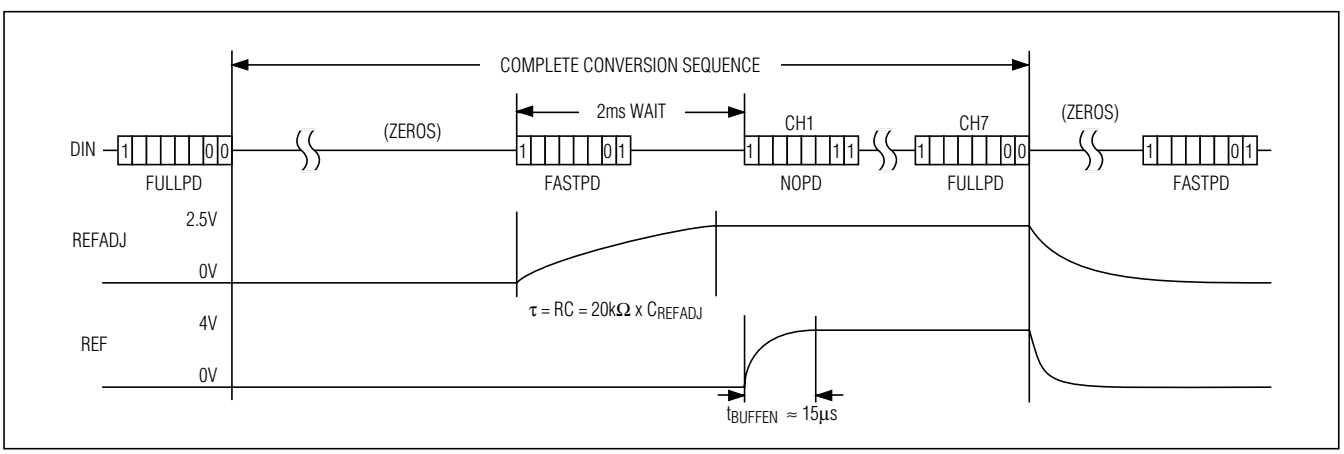


Figure 13. MAX1204 FULLPD/FASTPD Power-Up Sequence

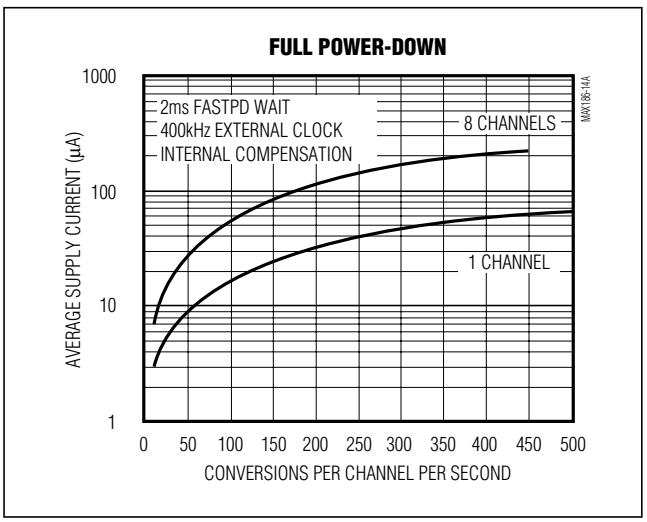


Figure 14a. MAX1204 Supply Current vs. Sample Rate/Second, FULLPD, 400kHz Clock

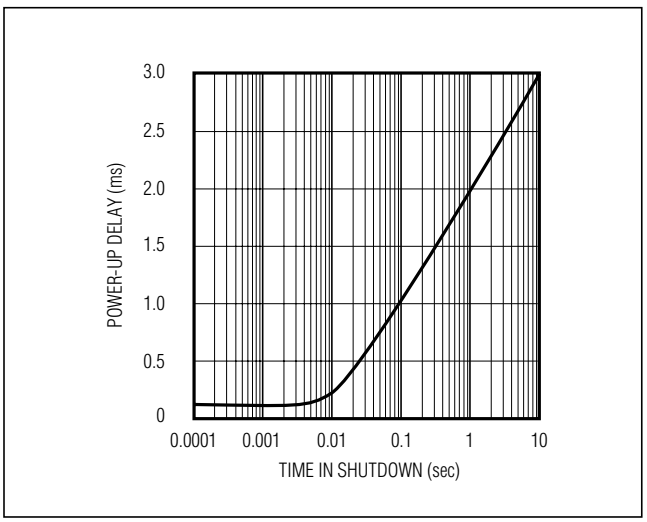


Figure 14c. Typical Power-Up Delay vs. Time in Shutdown

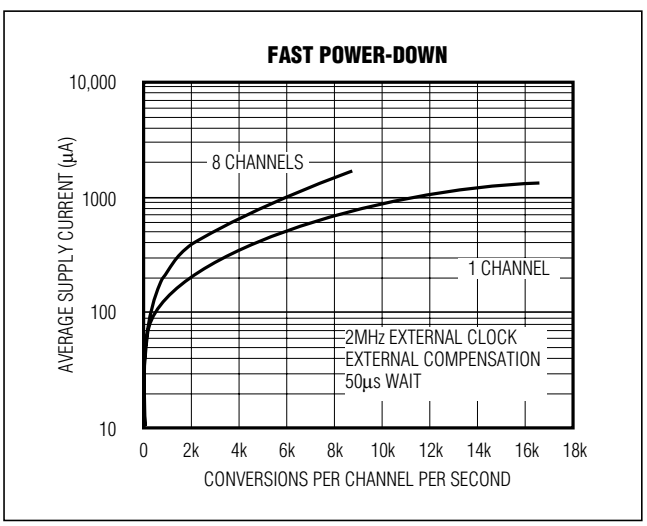


Figure 14b. MAX1204 Supply Current vs. Sample Rate/Second, FASTPD, 2MHz Clock

Figure 17, the Reference-Adjust Circuit, shows how to adjust ADC gain in applications that use the internal reference. The circuit provides ±1.5% (±16 LSBs) of gain-adjustment range.

Layout, Grounding, Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 18 shows the recommended system-ground connections. Establish a single-point analog ground (star ground point) at GND. Connect all other analog grounds to this ground. No other digital system ground should be connected to this single-point analog ground. The ground return to the power supply should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply may affect the high-speed comparator in the ADC. Bypass these supplies to the single-point analog ground with 0.1µF and 4.7µF bypass capacitors close to the MAX1204. Minimize capacitor lead lengths for best supply-noise rejection. If the +5V power supply is very noisy, a 10Ω resistor can be connected as a lowpass filter, as shown in Figure 18.

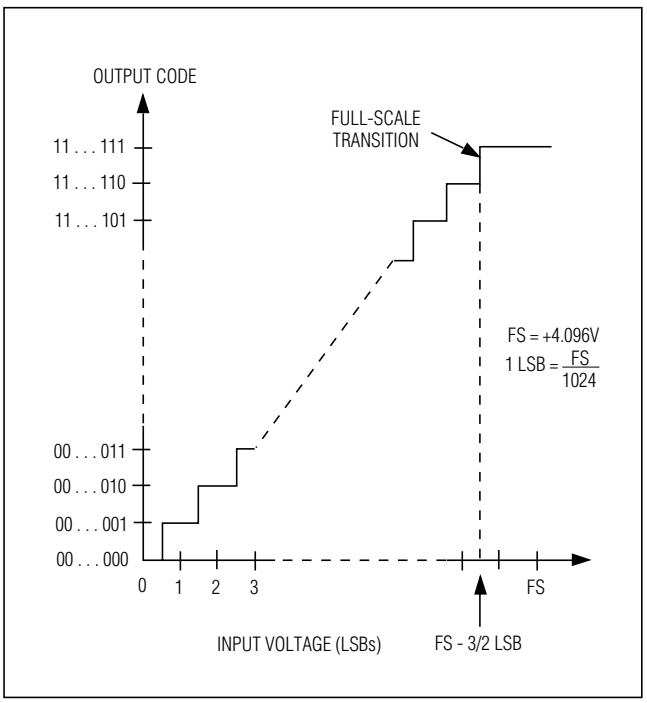


Figure 15. Unipolar Transfer Function, 4.096V = Full Scale

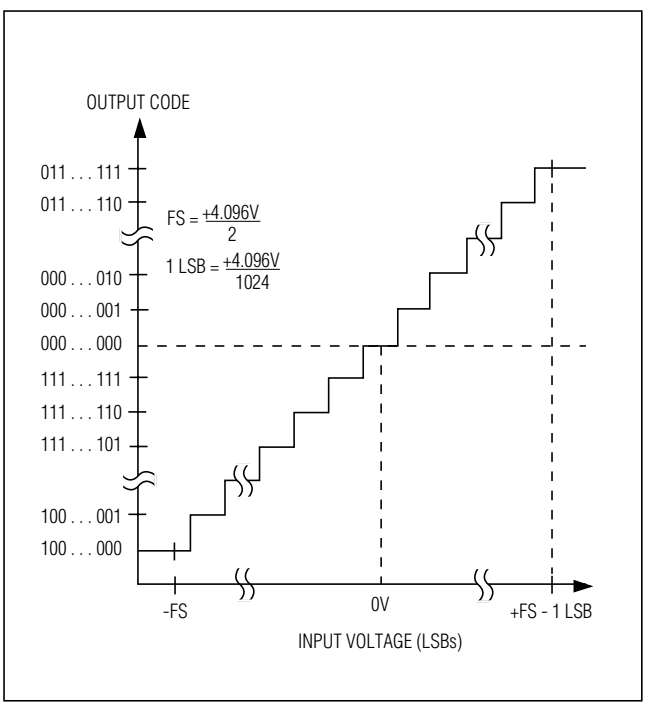


Figure 16. Bipolar Transfer Function, ±4.096V/2 = Full Scale

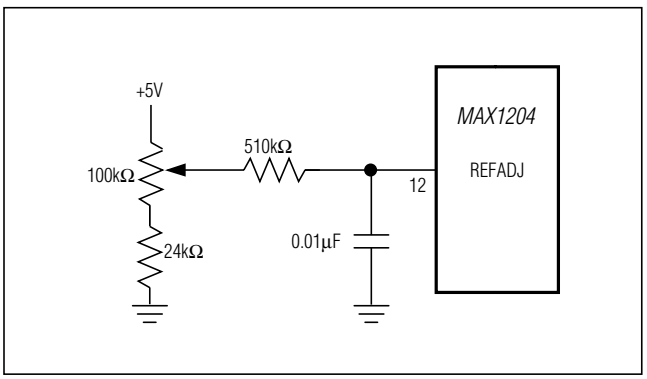


Figure 17. Reference-Adjust Circuit

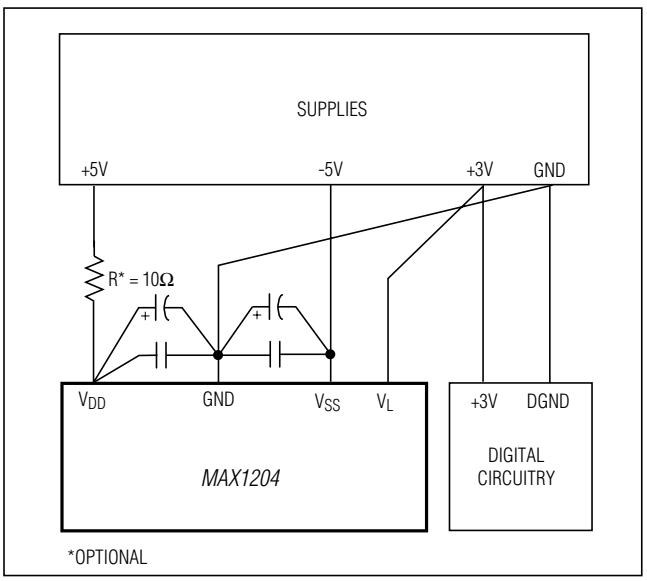


Figure 18. Power-Supply Grounding Connection

TMS320CL3x to MAX1204 Interface

Figure 19 shows an application circuit to interface the MAX1204 to the TMS320 in external clock mode. Figure 20 is the timing diagram for this interface circuit.

Use the following steps to initiate a conversion in the MAX1204 and to read the results.

1) The TMS320 should be configured with CLKX (transmit clock) as an active-high output clock and CLKR (TMS320 receive clock) as an active-high input clock. The TMS320's CLKX and CLKR are tied together with the MAX1204's SCLK input.
2) The MAX1204's $\overline{CS}$ is driven low by the TMS320's XF_ I/O port to enable data to be clocked into the MAX1204's DIN.
3) Write an 8-bit word (1XXXXX11) to the MAX1204 to initiate a conversion and place the device into external clock mode. Refer to Table 2 to select the proper XXXXX bit values for your specific application.
4) The MAX1204's SSTRB output is monitored via the TMS320's FSR input. A falling edge on the SSTRB output indicates that the conversion is in progress and data is ready to be received from the MAX1204.
5) The TMS320 reads in one data bit on each of the next 16 rising edges of SCLK. These data bits represent the 10-bit conversion result followed by two sub-bits and four trailing bits, which should be ignored.
6) Pull $\overline{CS}$ high to disable the MAX1204 until the next conversion is initiated.

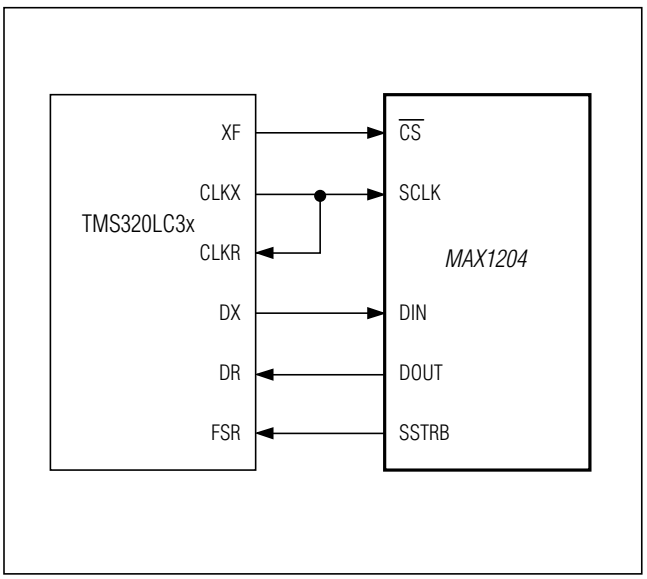


Figure 19. MAX1204 to TMS320 Serial Interface

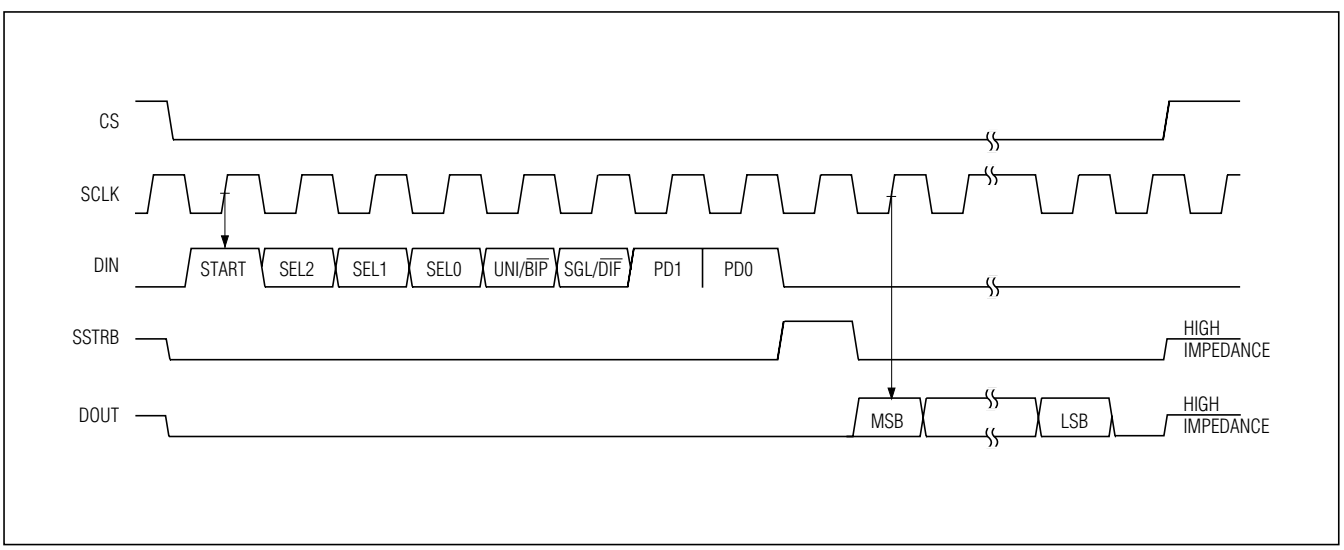


Figure 20. TMS320 Serial-Interface Timing Diagram

_Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX1204AEPP+	-40°C to +85°C	20 PDIP	±1/2
MAX1204BEPP+	-40°C to +85°C	20 PDIP	±1
MAX1204AEAP+	-40°C to +85°C	20 SSOP	±1/2
MAX1204BEAP+	-40°C to +85°C	20 SSOP	±1

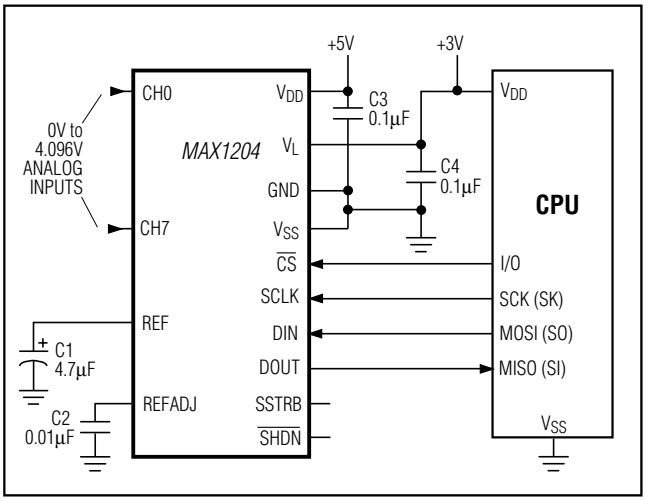
+Denotes a lead(Pb)-free/RoHS-compliant package.

_____Chip Information

SUBSTRATE CONNECTED TO V_{SS}

PROCESS: BiCMOS

_____Typical Operating Circuit



_____Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 PDIP	P20+3	21-0043	—
20 SSOP	A20+2	21-0056	90-0094

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/97	Initial release	—
1	1/12	Remove military grade packages.	22

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