THE DATASHEET OF

MAX153EWP+

MAX153

1Msps, µP-Compatible, 8-Bit ADC with 1µA Power-Down

General Description

The MAX153 high-speed, microprocessor (µP)-compatible, 8-bit analog-to-digital converter (ADC) uses a half-flash technique to achieve a 660ns conversion time, and digitizes at a rate of 1M samples per second (Msps). It operates with single +5V or dual ±5V supplies and accepts either unipolar or bipolar inputs. A $\overline{\text{POWERDN}}$ (power-down) pin reduces current consumption to a typical value of 1µA (with 5V supply). The part returns from power-down to normal operating mode in less than 200ns, providing large reductions in supply current in applications with burst-mode input signals.

The MAX153 is DC and dynamically tested. Its µP interface appears as a memory location or input/output port that requires no external interface logic. The data outputs use latched, three-state buffered circuitry for direct connection to a µP data bus or system input port. The ADC's input/reference arrangement enables ratiometric operation.

Applications

- Cellular Telephones
- Portable Radios
- Battery-Powered Systems
- Burst-Mode Data Acquisition
- Digital-Signal Processing
- Telecommunications
- High-Speed Servo Loops

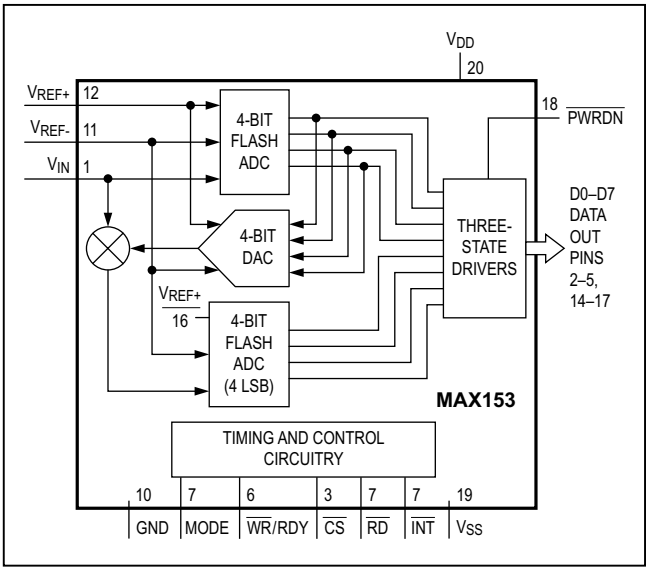
***Ordering Information* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX153.related.

Features

- 660ns Conversion Time
- Power-Up/Power-Down in 200ns
- Internal Track/Hold
- 1Msps Throughput
- Low Power
  40mW (Operating Mode)
  5µW (Power-Down Mode)
- 1MHz Full-Power Bandwidth
- 20-Pin Narrow DIP, SO, and SSOP Packages
- No External Clock Required
- Unipolar/Bipolar Inputs
- Single +5V or Dual ±5V Supplies
- Ratiometric Reference Inputs

Functional Diagram



maxim integrated™

Absolute Maximum Ratings

(All voltages referenced to GND.)
V_{DD}.....-0.3V to +7V
V_{SS}.....+0.3V to -7V
Digital Input Voltage ..... +0.3V to (V_{DD} + 0.3V)
Digital Output Voltage..... -0.3V to (V_{DD} + 0.3V)
V_{REF+}, V_{REF+}, V_{IN}.....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
PDIP (derate 11.11mW/°C above + 70°C). 889mW
SO(W) (derate 10.00mW/°C above +70°C.....800mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
Operating Temperature Ranges
MAX153C .....0 to +70°C
MAX153E ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{DD} = +5V ±5%, V_{GND} = 0V; Unipolar Input Range: V_{SS} = GND, V_{REF+} = 5V, V_{REF-} = GND; Bipolar Input Range: V_{SS} = -5V ±5%, V_{REF+} = 2.5V, V_{REF-} = -2.5V; 100% production tested, specifications are given for RD Mode (MODE = GND), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY						
Resolution	N		8			Bits
Total Unadjusted Error	TUE	Unipolar range			±1	LSB
Differential Nonlinearity	DNL	No missing codes guaranteed			±1	LSB
Zero-Code Error		Bipolar input range			±1	LSB
Full-Scale Error		Bipolar input range			±1	LSB
DYNAMIC SPECIFICATIONS (Note 1)						
Signal-to-Noise Plus Distortion Noise	SINAD	f_{SAMPLE} = 1MHz, f_{IN} = 195.8kHz	45			dB
Total Harmonic Distortion	THD	f_{SAMPLE} = 1MHz, f_{IN} = 195.8kHz			-50	dB
Peak Harmonic or Spurious Noise		f_{SAMPLE} = 1MHz, f_{IN} = 195.8kHz			-50	dB
Conversion Time (WR-RD Mode) (Note 2)	t_{CWR}	T_A = +25°C, t_{RD} < t_{INTL}, C_L = 20pF			660	ns
Conversion Time (RD Mode)	t_{CRD}	T_A = +25°C			700	ns
		T_A = T_{MIN} to T_{MAX}			875	
Full-Power Bandwidth		V_{IN} = $5V_{P-P}$		1		MHz
Input Slew Rate			3.14	15		V/µs
ANALOG INPUT						
Input Voltage Range	V_{IN}		V_{REF-}		V_{REF+}	V
Input Leakage Current	I_{IN}	-5V ≤ V_{IN} ≤ +5V			±3	µA
Input Capacitance	C_{IN}			22		pF
REFERENCE INPUT						
Reference Resistance	R_{REF}		1	2	4	kΩ
V_{REF+} Input Voltage Range			V_{REF-}		V_{DD}	V
V_{REF-} Input Voltage Range			V_{SS}		V_{REF+}	V

Electrical Characteristics (continued)

(V_{DD} = +5V ±5%, V_{GND} = 0V; Unipolar Input Range: V_{SS} = GND, V_{REF+} = 5V, V_{REF-} = GND; Bipolar Input Range: V_{SS} = -5V ±5%, V_{REF+} = 2.5V, V_{REF-} = -2.5V; 100% production tested, specifications are given for RD Mode (MODE = GND), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC INPUTS							
Input High Voltage	V_{INH}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$		2.4			V
		MODE		3.5			
Input Low Voltage	V_{INL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$				0.8	V
		MODE				1.5	
Input High Current	I_{INH}	$\overline{CS}$, $\overline{RD}$, $\overline{PWRDN}$				1	µA
		$\overline{WR}$				3	
		MODE			50	200	
Input Low Current	I_{INL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$				±1	µA
Input Capacitance (Note 3)	C_{IN}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$, MODE			5	8	pF
LOGIC OUTPUTS							
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA, $\overline{INT}$, D0–D7				0.4	V
		RDY, I_{SINK} = 2.6mA				0.4	
Output High Voltage	V_{OH}	I_{SOURCE} = 360µA, $\overline{INT}$, D0–D7		4			V
Floating State Current	I_{LKG}	D0–D7, RDY				±3	µA
Floating Capacitance (Note 3)	C_{OUT}	D7–D0, RDY			5	8	pF
POWER REQUIREMENTS							
Positive Supply Voltage	V_{DD}	±5% for specified accuracy			5		V
Negative Supply Voltage (Unipolar Operation)	V_{SS}				GND		V
Negative Supply Voltage (Bipolar Operation)	V_{SS}	±5% for specified accuracy			-5		V
V_{DD} Supply Current	I_{DD}	$V_{\overline{CS}}$ = $V_{\overline{RD}}$ = 0V, $V_{\overline{PWRDN}}$ = 5V	MAX153C		8	15	mA
			MAX153E		8	20	
Power-Down VDD Current		$V_{\overline{CS}}$ = $V_{\overline{RD}}$ = 5V, $V_{\overline{PWRDN}}$ = 0V (Note 4)			1	100	µA
V_{SS} Supply Current	I_{SS}	$V_{\overline{CS}}$ = $V_{\overline{RD}}$ = 0V, $V_{\overline{PWRDN}}$ = 5V			25	100	µA
Power-Down V_{SS} Current		$V_{\overline{CS}}$ = $V_{\overline{RD}}$ = 5V, $V_{\overline{PWRDN}}$ = 0V			12	100	µA
Power-Supply Rejection	PSR	V_{DD} = 4.75V to 5.25V, V_{REF}+ = 4.75V (max), unipolar mode			±1/16	±1/4	LSB

Note 1: Bipolar input range, V_{IN} = ±2.5V_{P-P}. WR-RD mode.
Note 2: See Figure 1 for load circuit. Parameter defined as the time required for the output to cross +0.8V or +2.4V.
Note 3: Guaranteed by design.
Note 4: Tested with $\overline{CS}$, $\overline{RD}$, $\overline{PWRDN}$ at CMOS logic levels. Power-down current increases to several hundred) µA at TTL levels.

TIMING CHARACTERISTICS (Note 5)

(V_{DD} = +5V ±5%, V_{SS} = 0V for Unipolar Input Range, V_{SS} = -5V ±5% for Bipolar Input Range, 100% production tested, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ TO $\overline{RD}$/$\overline{WR}$ Setup Time	t_{CSS}		0			ns
$\overline{CS}$ to $\overline{RD}$/$\overline{WR}$ Hold Time	t_{CSH}		0			ns
$\overline{CS}$ to $\overline{RDY}$ Delay (Note 6)	t_{RDY}	C_L = 50pF			70	ns
		T_A = T_{MIN} to T_{MAX}, C_L = 50pF			85	
Data-Access Time (RD Mode) (Note 2)	t_{ACC0}	C_L = 20pF			t_{CRD} + 25	ns
		T_A = T_{MIN} to T_{MAX}, C_L = 20pF			t_{CRD} + 30	
		C_L = 100pF			t_{CRD} + 50	
		T_A = T_{MIN} to T_{MAX}, C_L = 100pF			t_{CRD} + 65	
$\overline{RD}$ to $\overline{INT}$ Delay (RD Mode)	t_{INTH}	C_L = 50pF		50	80	ns
		T_A = T_{MIN} to T_{MAX}, C_L = 50pF			85	
Data-Hold Time (Note 7)	t_{DH}				60	ns
		T_A = T_{MIN} to T_{MAX}			70	
Delay Time Between Conversions (Acquisition Time)	t_P		160			ns
		T_A = T_{MIN} to T_{MAX}	185			
Write Pulse Width	t_{WR}		0.250		10	µs
		T_A = T_{MIN} to T_{MAX}	0.280		10	
Delay Time Between $\overline{WR}$ and $\overline{RD}$ Pulses	t_{RD}		250			ns
		T_A = T_{MIN} to T_{MAX}	350			
RD Pulse Width ($\overline{WR}$-$\overline{RD}$ Mode) Determined by t_{ACC1}	t_{READ1}	Figure 6	160			ns
		T_A = T_{MIN} to T_{MAX}, Figure 6	205			
Data-Access Time ($\overline{WR}$-$\overline{RD}$ Mode (Note 2) t_{RD} < t_{INL}	t_{ACC1}	C_L = 20pF, Figure 6			160	ns
		T_A = T_{MIN} to T_{MAX}, C_L = 20pF, Figure 6			205	
		C_L = 100pF, Figure 6			185	
		T_A = T_{MIN} to T_{MAX}, C_L = 100pF, Figure 6			235	
$\overline{RD}$ to $\overline{INT}$ Delay	t_{RI}				150	ns
		T_A = T_{MIN} to T_{MAX}			185	
$\overline{WR}$ to $\overline{INT}$ Delay	t_{INTL}	C_L = 50pF		380	500	ns
		T_A = T_{MIN} to T_{MAX}, C_L = 50pF			610	
$\overline{RD}$ Pulse Width (WR-RD Mode) Determinted by t_{ACC2} t_{RD} > t_{INTL}	t_{READ2}	Figure 5	65			ns
		T_A = T_{MIN} to T_{MAX}, Figure 5	75			
Data-Access Time (WR-RD Mode) (Note 2) t_{RD} > t_{INTL}	t_{ACC2}	C_L = 20pF, Figure 5			65	ns
		T_A = T_{MIN} to T_{MAX}, C_L = 20pF, Figure 5			75	
		C_L = 100pF, Figure 5			90	
		T_A = T_{MIN} to T_{MAX}, C_L = 100pF, Figure 5			110	

TIMING CHARACTERISTICS (Note 5) (continued)

(V_{DD} = +5V ±5%, V_{SS} = 0V for Unipolar Input Range, V_{SS} = -5V ±5% for Bipolar Input Range, 100% production tested, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{WR}$ to $\overline{INT}$ Delay (Pipelined Mode)	t_{IHWR}	C_L = 50pF			80	ns
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 50pF			100	
Data-Access Time After $\overline{INT}$ (Note 2)	t_{ID}	C_L = 20pF			30	ns
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 20pF			35	
		C_L = 100pF			45	
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 100pF			60	

Note 5: Input control signals are specified with $t_r = t_t$ = 5ns, 10% to 90% of +5V and timed from a 1.6V voltage level.
Note 6: R_L = 5.1kΩ pullup resistor.
Note 7: See Figure 2 for load circuit. Parameter defined as the time required for data lines to change 0.5V.

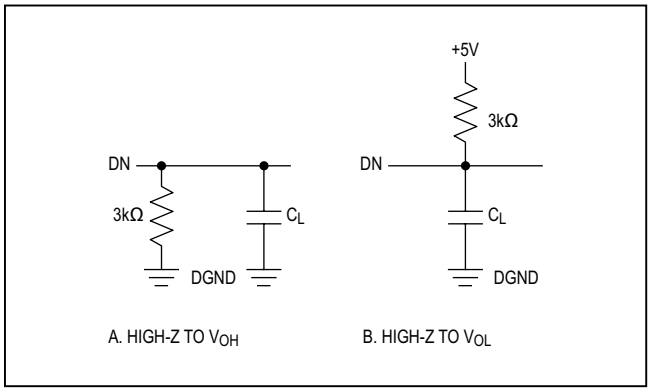


Figure 1. Load Circuits for Data-Access Time Test

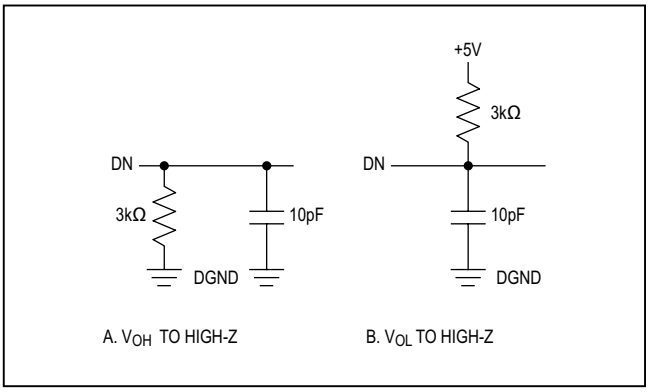
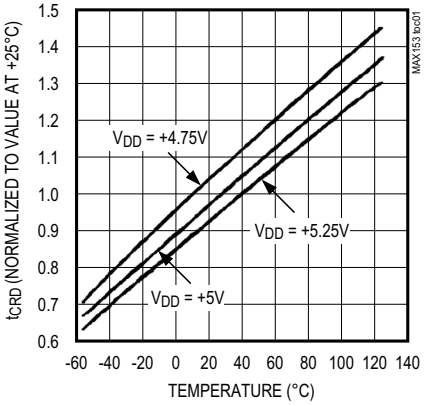


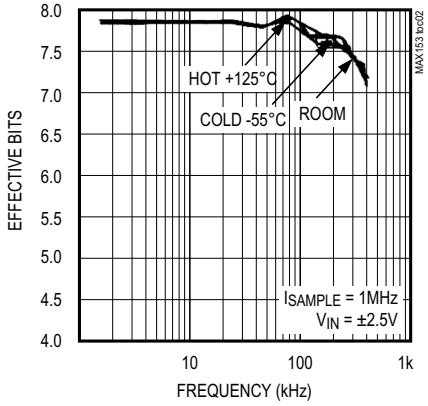
Figure 2. Load Circuits for Data-Hold Time Test

Typical Operating Characteristics

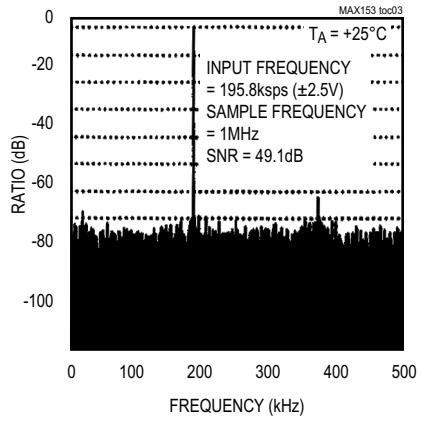
CONVERSION TIME vs. AMBIENT TEMPERATURE



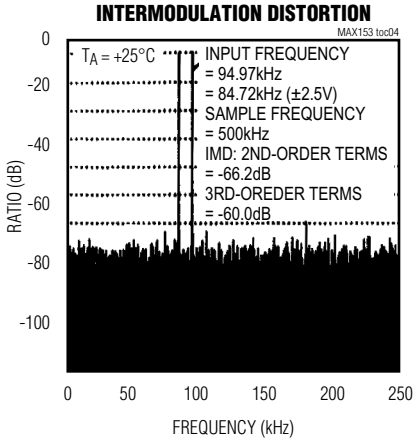
EFFECTIVE BITS vs. INPUT FREQUENCY, WR-RD MODE



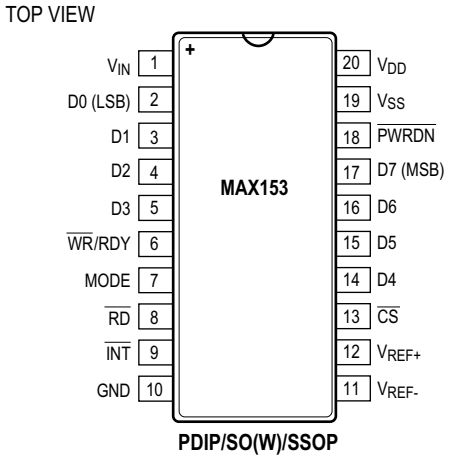
SIGNAL-TO-NOISE RATIO



INTERMODULATION DISTORTION



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	V_{IN}	Analog Input. Range is $V_{REF-} > V_{IN} < V_{REF+}$.
2	D0	Three-State Data Output (LSB)
3–5	D1–D3	Three-State Data Outputs
6	$\overline{WR}$/RDY	$\overline{WRITE}$ Control Input/READY Status Output*
7	MODE	MODE Selection Input. Internally pulled low with a 50µA current source. MODE = 0 activates read mode. MODE = 1 actives write-read mode*
8	$\overline{RD}$	$\overline{READ}$ Input. Must be low to access data*.
9	$\overline{INT}$	$\overline{INTERRUPT}$ Output goes low to indicate end of conversion*.
10	GND	Ground
11	V_{REF-}	Lower Limit of Reference Span. Sets the zero-code voltage. Range is $V_{SS} < V_{REF-} < V_{REF+}$.
12	V_{REF+}	Upper Limit to Reference Span. Sets the full-scale input voltage. Range is $V_{REF-} < V_{REF+} < V_{DD}$.
13	$\overline{CS}$	$\overline{CHIP\ SELECT}$ Input. Must be low for the device to recognize $\overline{WR}$ or $\overline{RD}$ inputs.
14–16	D4–D6	Three-State Data Outputs
17	D7	Three-State Data Output (MSB)
18	$\overline{PWRDN}$	$\overline{POWERDOWN}$ Input. Reduces supply current when low. $\overline{CS}$ must be high during power-down.
19	V_{SS}	Negative Supply. Unipolar: V_{SS} = 0V, Bipolar: V_{SS} = -5V.
20	V_{DD}	Positive Supply, +5V

**See the Digital Interface section.*

Detailed Description

Converter Operation

The MAX153 uses a half-flash conversion technique (see the *Functional Diagram*) in which two 4-bit flash ADC sections achieve an 8-bit result. Using 15 comparators, the flash ADC compares the unknown input voltage to the reference ladder and provides the upper 4 data bits.

An internal digital-to-analog converter (DAC) uses the 4 most significant bits (MSBs) to generate the analog result from the first flash conversion and a residue voltage that is the difference between the unknown input and the DAC voltage. The residue is then compared again with the flash comparators to obtain the lower 4 data bits (LSBs).

Power-Down Mode

In burst-mode or low sample-rate applications, the MAX153 can be shut down between conversions, reducing supply current to microamp levels. A TTL/CMOS logic-low on the $\overline{PWRDN}$ pin shuts the device down, reducing supply current to typically 1µA when powered from a single 5V supply. $\overline{CS}$ must be high when power-down is used. A logic-high on $\overline{PWRDN}$ wakes up the MAX153. A new conversion can be started ($\overline{WR}$ asserted low) within 360ns of the $\overline{PWRDN}$ pin being driven high 200ns to power up plus 160ns for track/hold acquisition). If power-down mode is not required, connect $\overline{PWRDN}$ to V_{DD}.

Once the MAX153 is in power-down mode, lowest supply current is drawn with MODE low (RD mode) due to an internal 50µA pulldown resistor at this pin. $\overline{CS}$ must remain high during shutdown because the MAX153 may attempt to start a conversion that it cannot complete. In addition, for minimum current consumption, other digital inputs should remain stable in power-down. RDY, an open-drain output (in RD mode), will then fall and remain low throughout. Power-down, sinking additional supply current unless $\overline{CS}$ remains high. See the *Reference* section for information on reducing reference current during power-down.

Digital Interface

The MAX153 has two basic interface modes set by the status of the MODE input pin. When MODE is low, the converter is in the RD mode; when MODE is high, the converter is set up for the WR-RD mode.

Read Mode (MODE = 0)

In RD mode, conversion control and data access are controlled by the $\overline{RD}$ input (Figure 3). The comparator inputs track the analog input voltage for the duration of t_P. A minimum of 160ns is required for the input to be acquired. A conversion is initiated by driving $\overline{RD}$ low. With µPs that can be forced into a wait state, hold $\overline{RD}$ low until output data appears. The µP starts the conversion, waits, and then reads data with a single read instruction.

$\overline{WR}$/RDY is configured as a status output (RDY) in RD mode, where it can drive the ready or wait input of a µP. RDY is an open-collector output (with no internal pullup) that goes low after the falling edge of $\overline{CS}$ and goes high at the end of the conversion. If not used, the $\overline{WR}$/RDY pin can be left unconnected. The $\overline{INT}$ output goes low at the end of the conversion and returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

Write-Read Mode (MODE = 1)

Figures 4 and 5 show the operating sequence for the write-read (WR-RD) mode. The comparator inputs track the analog input voltage for the duration of t_P. A minimum of 160ns is required for the input voltage to be acquired. The conversion is initiated by a falling edge of $\overline{WR}$. When WR returns high, the 4 MSBs flash result is latched into the output buffers and the 4 LSBs conversion begins. INT goes low about 380ns later, indicating conversion end, and the lower 4 data bits are latched into the output buffers. The data is then accessible 65ns to 130ns after RD goes low (see the *Timing Characteristics*).

If an externally controlled conversion time is required, drive $\overline{RD}$ low 250ns after $\overline{WR}$ goes high. This latches the lower 4 data bits and outputs the conversion result on D0–07. A minimum 160ns delay is required from $\overline{INT}$ going low to the start of another conversion ($\overline{WR}$ going low).

Options for reading data from the converter include the following:

Using Internal Delay

The µP waits for the $\overline{INT}$ output to go low before reading the data (Figure 4). $\overline{INT}$ typically goes low 380ns after the rising edge of $\overline{WR}$, indicating the conversion is complete, and the result is available in the output latch. With $\overline{CS}$ low, data outputs D0–D7 can be accessed by pulling $\overline{RD}$ low. $\overline{INT}$ is then reset by the rising edge of $\overline{CS}$ or $\overline{RD}$.

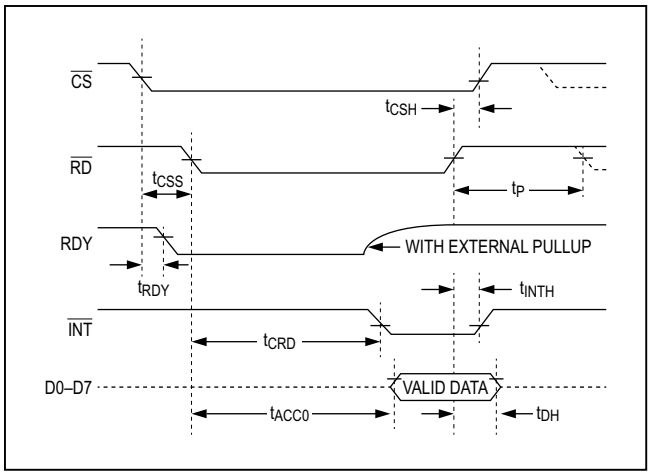


Figure 3. RD Mode Timing (MODE = 0)

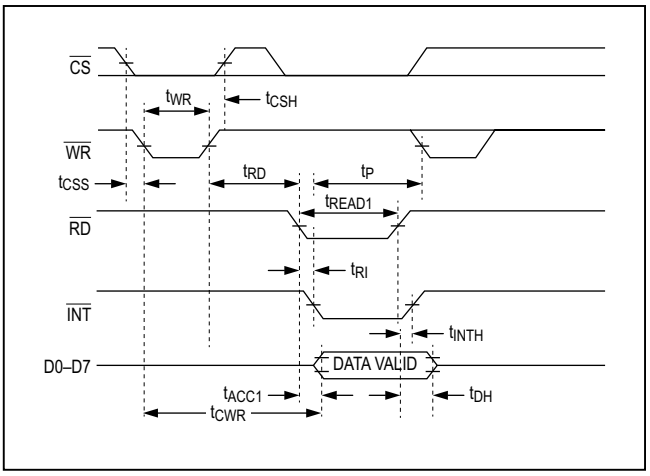


Figure 5. WR-RD Mode Timing (t_{RD} > t_{INTL}), Fastest Operating Mode (MODE = 1)

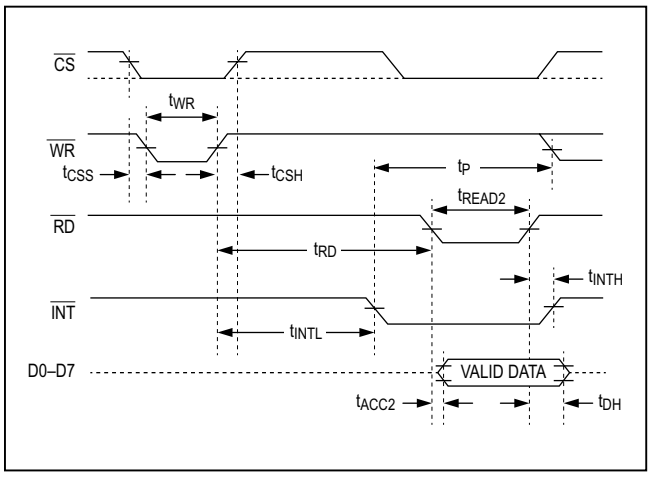


Figure 4. WR-RD Mode Timing (t_{RD} > t_{INTL}) (MODE = 1)

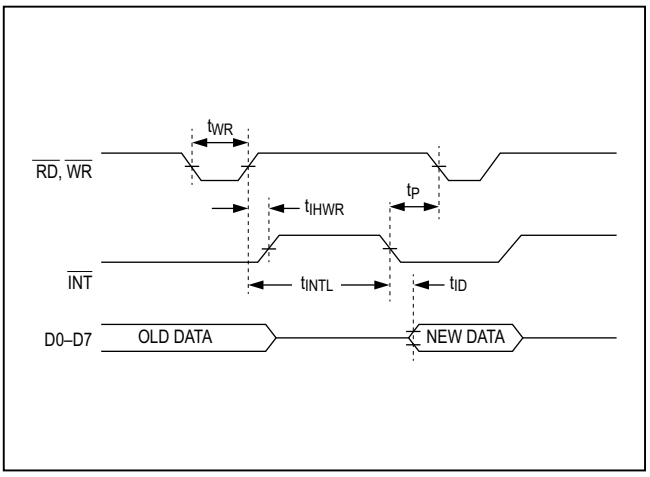


Figure 6. Pipelined Mode Timing ($\overline{WR}$ = $\overline{RD}$) (MODE = 1)

Fastest Conversion: Reading Before Delay

An external method of controlling the conversion time is shown in Figure 5. The internally generated delay t_{INTL} varies slightly with temperature and supply voltage, and can be overridden with $\overline{RD}$ to achieve the fastest conversion time. $\overline{INT}$ is ignored, and $\overline{RD}$ is brought low typically 250ns after the rising edge of $\overline{WR}$. This completes the conversion and enables the output buffers (D0–D7) that contain the conversion result. $\overline{INT}$ also goes low after the falling edge of $\overline{RD}$ and is reset on the rising edge of $\overline{RD}$ or $\overline{CS}$. The total conversion time is therefore:

$$t_{CWR} = t_{WR} (250ns) + t_{CSH} (0ns) \text{ to } t_{RD} (250ns) + t_{ACC1} (160ns) = 660ns.$$

Pipelined Operation

Besides the two standard WR-RD mode options, pipelined operation can be achieved by connecting $\overline{WR}$ and $\overline{RD}$ together (Figure 6). With $\overline{CS}$ low, driving $\overline{WR}$ and $\overline{RD}$ low initiates a conversion and reads the result of the previous conversion concurrently.

Analog Considerations

Reference

Figures 7a–7c show some reference connections. V_{REF+} and V_{REF-} inputs set the full-scale and zero-input voltages of the ADC. The voltage at V_{REF-} defines the input that produces an output code of all zeros, and the voltage at V_{REF+} defines the input that produces an output code of all ones.

The internal resistances from V_{REF+} and V_{REF-} may be as low as 1kΩ. Since current is still drawn by the reference inputs during power-down, reference supply current can be reduced during shutdown by using the circuit shown in Figure 7d. A logic-level n-channel MOSFET, connected between V_{REF-} and ground, disconnects the reference load when the ADC enters power-down. ($\overline{PWRDN}$ = low). The FET should have no more than 0.5Ω of on-resistance to maintain accuracy.

Bypassing

A 4.7µF electrolytic in parallel with a 0.1µF ceramic capacitor should be used to bypass V_{DD} to GND. These capacitors should have minimal lead length.

The reference inputs should be bypassed with 0.1µF capacitors, as shown in Figures 7a–7c.

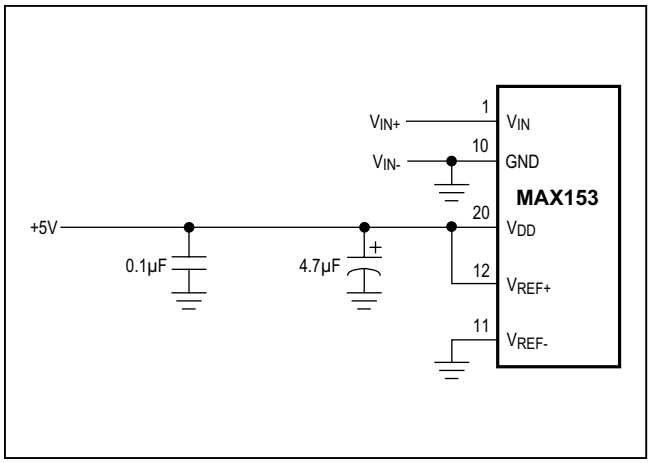


Figure 7a. Power Supply as Reference

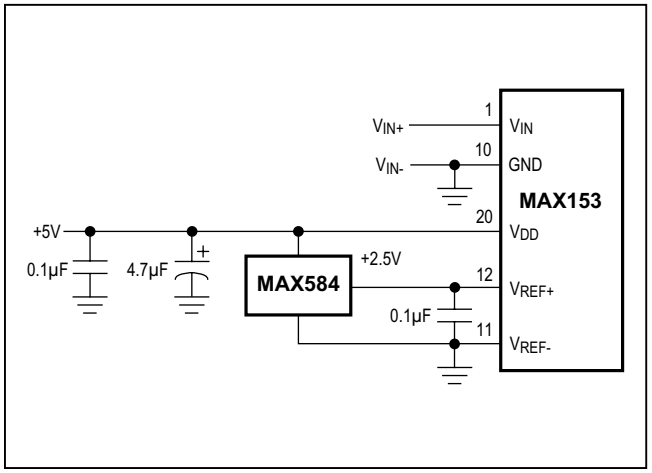


Figure 7b. External Reference, +2.5V Full Scale

Input Current

Figure 8 shows the equivalent circuit of the converter input. When the conversion starts and $\overline{WR}$ is low, V_{IN} is connected to 16 0.6pF capacitors. During this acquisition phase, the input capacitors charge to the input voltage through the resistance of the internal analog switches (about 2kΩ). In addition, about 12pF of stray capacitance must be charged. The input can be modeled as an equivalent RC network (Figure 9). As source impedance increases, the capacitors take longer to charge.

The typical 22pF input capacitance allows source resistance as high as 2.2kΩ without setup problems. For larger resistances, the acquisition time (t_P) must be increased

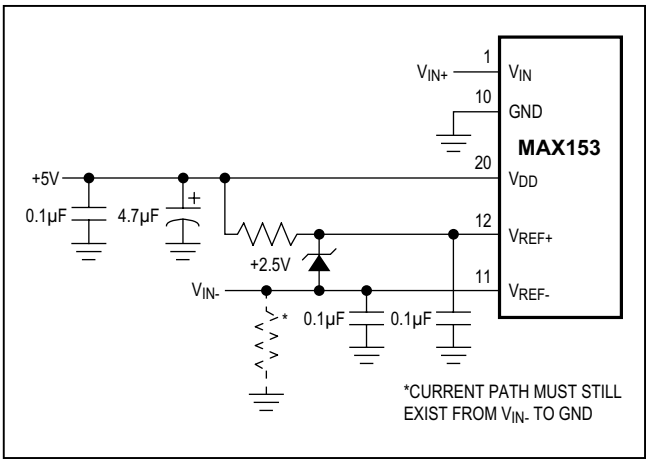


Figure 7c. Input Not Referenced to GND

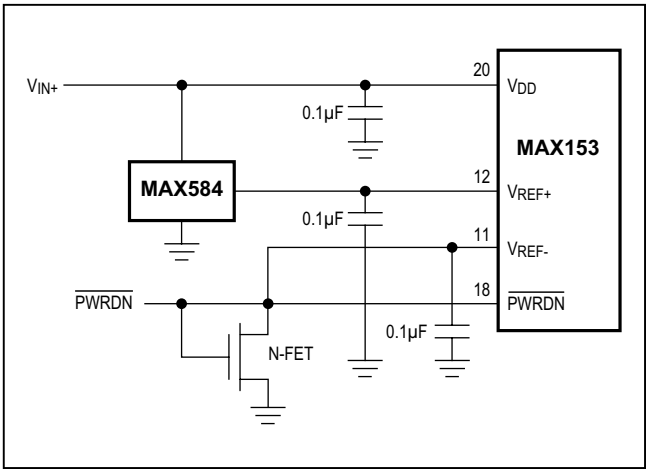


Figure 7d. An n-Channel MOSFET Switches Off the Reference Load During Power-Down

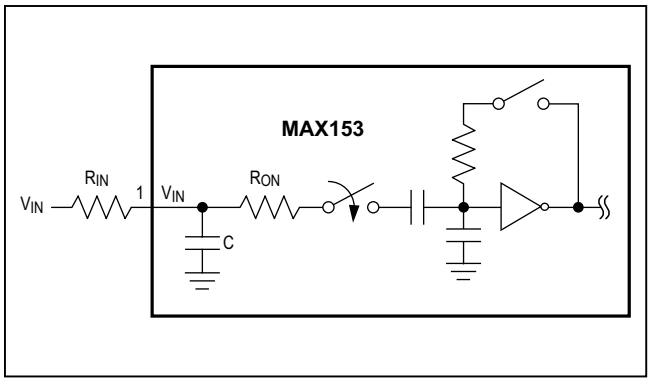


Figure 8. Equivalent Input Circuit

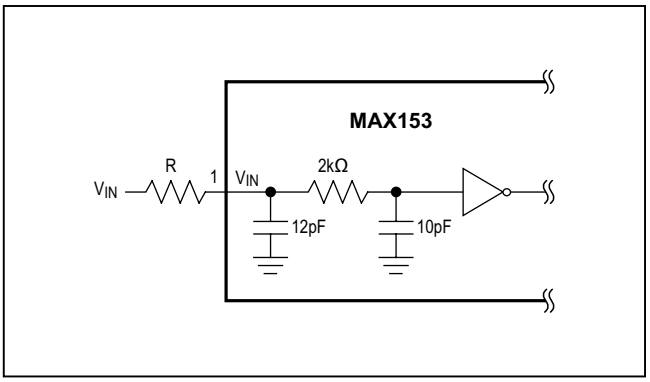


Figure 9. RC Network Equivalent Input Model

Conversion Rate

The maximum sampling rate (f_{MAX}) for the MAX153 is achieved in the WR-RD mode ($t_{RD} < t_{INTL}$) and is calculated as follows:

$$f_{MAX} = \frac{1}{t_{WR} + t_{RD} + t_{RI} + t_P}$$

$$f_{MAX} = \frac{1}{250ns + 250ns + 150ns + 165ns}$$

$$f_{MAX} = 1.23MHz$$

where t_{WR} = Write pulse width

t_{RD} = Delay between $\overline{WR}$ and $\overline{RD}$ pulses

t_{RI} = $\overline{RD}$ to $\overline{INT}$ delay

t_P = Delay time between conversions

Signal-to-Noise Ratio and Effective Number of Bits

Signal-to-noise ratio (SNR) is the ratio of the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other analog-to-digital output values. The output band is limited to one-half the A/D sample (conversion) rate. This ratio usually includes distortion as well as noise components. For this reason, the ratio is sometimes referred to as signal-to-noise plus distortion.

The theoretical minimum A/D noise is caused by quantization error and results directly from the ADC's resolution: SNR = (6.02N + 1.76)dB, where N is the number of bits of resolution. Therefore, a perfect 8-bit ADC can do no better than 50dB.

The FFT plot (*Typical Operating Characteristics*) shows the result of sampling a pure 200kHz sinusoid at a 1MHz rate. This FFT plot of the output shows the output level in various spectral bands.

The effective resolution, or effective number of bits, the ADC provides can be measured by transposing the equation that converts resolution to SNR: N = (SNR - 1.76)/6.02.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal (in the frequency band above DC and below one-half the sample rate) to the fundamental itself. This is expressed as:

$$THD = 20\log\left[\frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + ... + V_N^2)}}{V_1}\right]$$

where V_1 is the fundamental RMS amplitude, and V_2 to V_N are the amplitudes of the 2nd through Nth harmonics.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is the ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one-half the sample rate). Usually this peak occurs at some harmonic of the input frequency, but if the ADC is exceptionally linear, it may occur only at a random peak in the ADC's noise floor.

Intermodulation Distortion

An FFT plot of intermodulation distortion (IMD) is generated by sampling an analog input applied to the ADC. This input consists of very low distortion sine waves at two frequencies. A 2048 point plot for IMD of the MAX153 is shown in the *Typical Operating Characteristics*.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX153CAP+	0°C to +70°C	20 SSOP**
MAX153CPP+	0°C to +70°C	20 PDIP
MAX153CWP+	0°C to +70°C	20 SO(W)
MAX153C/D	0°C to +70°C	Dice*
MAX153EAP+	-40°C to +85°C	20 SSOP**
MAX153EPP+	-40°C to +85°C	20 PDIP
MAX153EWP+	-40°C to +85°C	20 Wide SO

+Denotes a lead(Pb)-free/RoHS-compliant package.

**Contact factory for dice specifications.*

***Contact factory for availability of SSOP packages*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 PDIP	P20+3	21-0043	—
20 SO(W)	W20+2	21-0042	90-0108
20 SSOP	A20+1	21-0056	90-0094

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/92	Initial release	—
1	10/93	Corrected die topography	11
2	1/12	Removed military packages	1–5

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