THE DATASHEET OF

MAX1637EEE+T

19-1321; Rev 2; 8/05

EVALUATION KIT AVAILABLE

Miniature, Low-Voltage, Precision Step-Down Controller

General Description

The MAX1637 synchronous, buck, switch-mode power-supply controller generates the CPU supply voltage in battery-powered systems. The MAX1637 is a stripped-down version of the MAX1636 in a smaller 16-pin QSOP package. The MAX1637 is intended to be powered separately from the battery by an external bias supply (typically the +5V system supply) in applications where the battery exceeds 5.5V. The MAX1637 achieves excellent DC and AC output voltage accuracy. This device can operate from a low input voltage (3.15V) and delivers the excellent load-transient response needed by upcoming generations of dynamic-clock CPUs.

Using synchronous rectification, the MAX1637 achieves up to 95% efficiency. Efficiency is greater than 80% over a 1000:1 load-current range, which extends battery life in system-suspend or standby mode. Excellent dynamic response corrects output load transients caused by the latest dynamic-clock CPUs within five 300kHz clock cycles. Powerful 1A on-board gate driv-ers ensure fast external N-channel MOSFET switching.

The MAX1637 features a logic-controlled and synchronizable, fixed-frequency, pulse-width-modulation (PWM) operating mode. This reduces noise and RF interference in sensitive mobile-communications and pen-entry applications. Asserting the $\overline{SKIP}$ pin enables fixed-frequency mode, for lowest noise under all load conditions. For a stand-alone device that includes a +5V VL linear regulator and low-dropout capabilities, refer to the MAX1636 data sheet.

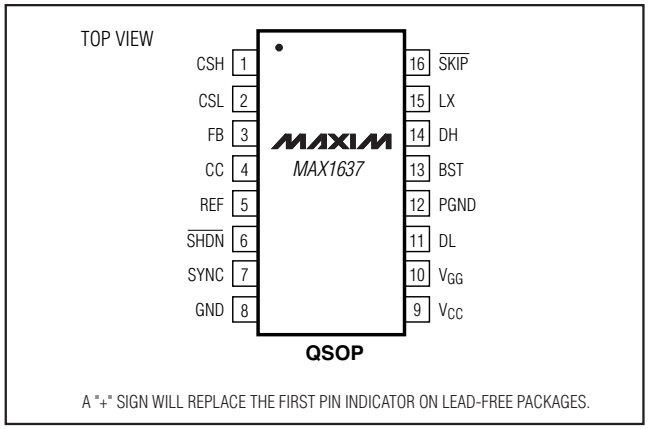
Applications

Notebook Computers

Subnotebook Computers

Handy-Terminals, PDAs

Pin Configuration



Idle Mode is a trademark of Maxim Integrated Products.

Features

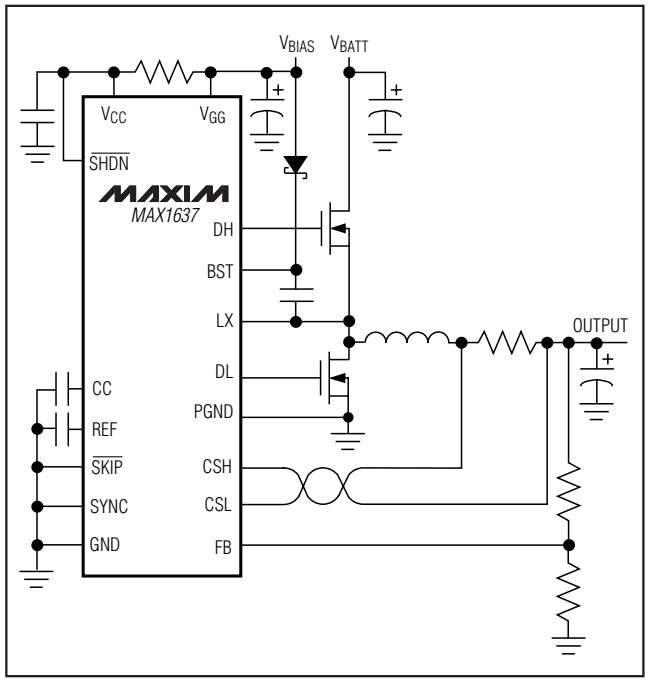
- ♦ **±2% DC Accuracy**
- ♦ **0.1% (typ) DC Load Regulation**
- ♦ **Adjustable Switching Frequency to 350kHz**
- ♦ **Idle Mode™ Pulse-Skipping Operation**
- ♦ **1.10V to 5.5V Adjustable Output Voltage**
- ♦ **3.15V Minimum IC Supply Voltage (at V_{CC} pin)**
- ♦ **Internal Digital Soft-Start**
- ♦ **1.1V ±2% Reference Output**
- ♦ **1µA Total Shutdown Current**
- ♦ **Output Overvoltage Crowbar Protection**
- ♦ **Output Undervoltage Shutdown (foldback)**
- ♦ **Tiny 16-Pin QSOP Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1637EEE	40°C to +85°C	16 QSOP
MAX1637EEE+	40°C to +85°C	16 QSOP

+Denotes lead-free package.

Typical Operating Circuit



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ABSOLUTE MAXIMUM RATINGS

GND to PGND .....+2V to -2V
LX, BST to GND.....-0.3V to +36V
BST, DH to LX.....-0.3V to +6V
V_{CC}, V_{GG}, CSL, CSH, $\overline{SHDN}$ to GND.....-0.3V to +6V
DL to GND.....-0.3V to (V_{GG} + 0.3V)
REF, $\overline{SKIP}$, SYNC, CC to GND .....-0.3V to (V_{CC} + 0.3V)
REF Output Current.....20mA
REF Short-Circuit to GND .....Indefinite
Operating Temperature Range .....-40°C to +85°C
Continuous Power Dissipation (T_A = +70°C)
QSOP (derate 8.3mW/°C above +70°C).....667mW
Storage Temperature Range .....-65°C to +160°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{CC} = V_{GG} = 5V, SYNC = V_{CC}, I_{REF} = 0mA, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SMPS CONTROLLER						
Input Voltage Range	V_{CC}, V_{GG}		3.15		5.5	V
Output Voltage	FB tied to V_{OUT}, 0mV < (CSH - CSL) < 80mV, includes line and load regulation		1.080	1.100	1.120	V
Output Adjustment Range	V_{CC} = 5V		V_{REF}		5.5	V
	V_{CC} = 3.3V		V_{REF}		3.6	
Current-Limit Threshold	CSH > CSL		80	100	120	mV
	CSH < CSL		-145	-100	-55	
Power Consumption	Output not switching	V_{CC} = V_{GG} = 5V		1.5	2.5	mW
		V_{CC} = V_{GG} = 3.3V		1	1.75	
Shutdown Supply Current	$\overline{SHDN}$ = GND, V_{CC} = V_{GG}			0.5	3	µA
FB Input Current	V_{FB} = V_{REF}		-50		50	nA
Soft-Start Ramp Time	$\overline{SHDN}$ to full current limit, four levels			512		clocks
Idle-Mode Switchover Threshold	CSH - CSL		20	30	40	mV
AC Load Regulation	CSH - CSL = 0mV to CSH - CSL = 100mV			2		%
INTERNAL REFERENCE						
V_{CC} Undervoltage Lockout Threshold	Rising edge, hysteresis = 15mV		2.80		3.05	V
V_{GG} Undervoltage Lockout Threshold	Rising edge, hysteresis = 15mV		2.80		3.05	V
REF Output Voltage	REF load = 0µA		1.080	1.100	1.120	V
REF Load Regulation	REF load = 0µA to 50µA				10	mV
REF Line Regulation	V_{CC} = 3.15V to 5.5V				3	mV
OSCILLATOR						
Oscillator Frequency	SYNC = V_{CC}		270	300	330	kHz
	SYNC = GND		170	200	230	
Maximum Duty Factor	SYNC = V_{CC}		89	92		%
	SYNC = GND		93	96		
SYNC Input Pulse Width High			200			ns
SYNC Input Pulse Width Low			200			ns
SYNC Input Rise/Fall Time	(Note 1)				200	ns
SYNC Input Frequency Range			240		340	kHz

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{CC} = V_{GG} = 5V, SYNC = V_{CC}, I_{REF} = 0mA, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OVERVOLTAGE PROTECTION					
Overvoltage Trip Threshold	FB, with respect to regulation point	4	7	10	%
Overvoltage Fault Propagation Delay	FB to DL delay, 22mV overdrive, C_{GATE} = 2000pF		1.25		µs
Output Undervoltage Lockout Threshold	% of nominal output	60	70	80	%
Output Undervoltage Lockout Delay	From shutdown or power-on-reset state		6144		clocks
INPUTS AND OUTPUTS					
Logic Input Voltage High	$\overline{SHDN}$, $\overline{SKIP}$, SYNC	2.4			V
Logic Input Voltage Low	$\overline{SHDN}$, $\overline{SKIP}$, SYNC			0.8	V
Logic Input Bias Current	Pin at GND or V_{CC}	-1		1	µA
Current-Sense Input Leakage Current	CSH = CSL = 5V, V_{CC} = V_{GG} = GND, either CSH or CSL input			10	µA
Gate Driver Sink/Source Current	DH or DL forced to 2V		1		A
Gate Driver On-Resistance	High or low, DH or DL			7	Ω

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{CC} = V_{GG} = 5V, SYNC = V_{CC}, I_{REF} = 0mA, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SMPS CONTROLLER					
Input Voltage Range	V_{CC}, V_{GG}	3.15		5.5	V
Output Voltage	FB tied to V_{OUT}, 0mV < (CSH - CSL) < 80mV, includes line and load regulation	1.080		1.120	V
Output Adjustment Range	V_{CC} = 5V	V_{REF}		5.5	V
	V_{CC} = 3.3V	V_{REF}		3.6	
Current-Limit Threshold	CSH > CSL	70		130	mV
Power Consumption	V_{CC} = V_{GG} = 5V, output not switching			2.5	mW
	V_{CC} = V_{GG} = 3.3V, output not switching			1.75	mW
INTERNAL REFERENCE					
V_{CC} Undervoltage Lockout Threshold	Rising edge, hysteresis = 15mV	2.80		3.05	V
V_{GG} Undervoltage Lockout Threshold	Rising edge, hysteresis = 15mV	2.80		3.05	V
OSCILLATOR					
Oscillator Frequency	SYNC = V_{CC}	262		338	kHz
	SYNC = GND	170		230	
SYNC Input Pulse Width High		200			ns
SYNC Input Pulse Width Low		200			ns
SYNC Input Rise/Fall Time				200	ns
SYNC Input Frequency Range		240		340	kHz

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{CC} = V_{GG} = 5V, SYNC = V_{CC}, I_{REF} = 0mA, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

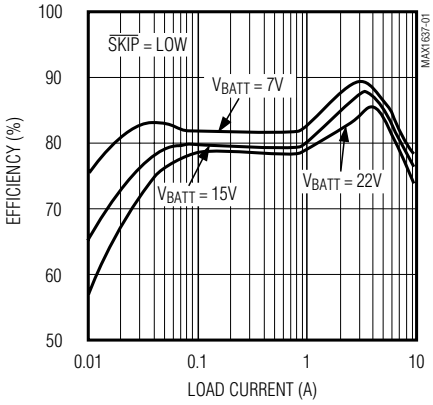
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OVERVOLTAGE PROTECTION					
Overvoltage Trip Threshold	FB, with respect to regulation point	4.0		10	%
Output Undervoltage Lockout Threshold	% of nominal output	60		80	%
INPUTS AND OUTPUTS					
Logic Input Voltage High	$\overline{SHDN}$, $\overline{SKIP}$, SYNC	2.4			V
Logic Input Voltage Low	$\overline{SHDN}$, $\overline{SKIP}$, SYNC			0.8	V

Note 1: Guaranteed by design, not production tested.
Note 2: Specifications from -40°C to 0°C are guaranteed by design and not production tested.

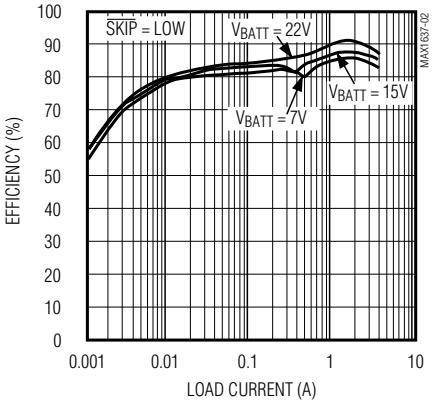
Typical Operating Characteristics

(V_{OUT} = 3.3V, T_A = +25°C, unless otherwise noted.)

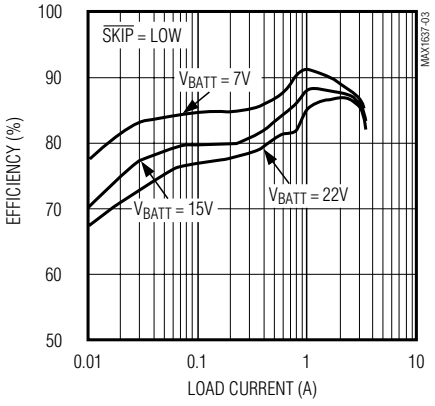
EFFICIENCY vs. LOAD CURRENT (1.7V/7A CIRCUIT)



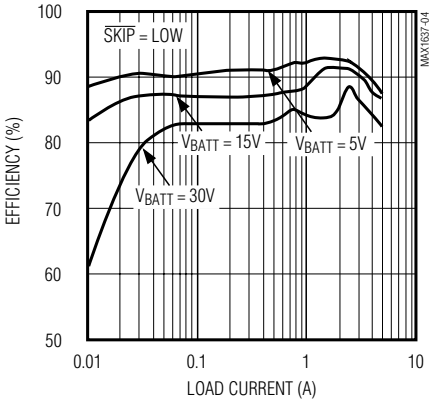
EFFICIENCY vs. LOAD CURRENT (2.5V/3A CIRCUIT)



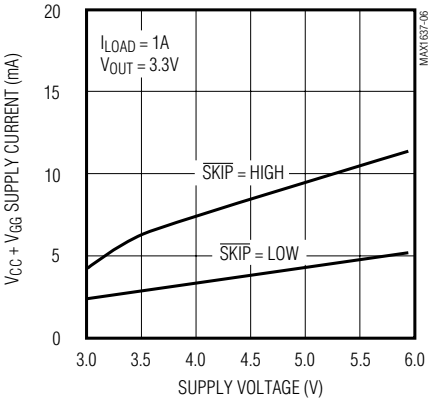
EFFICIENCY vs. LOAD CURRENT (2.5V/2A CIRCUIT)



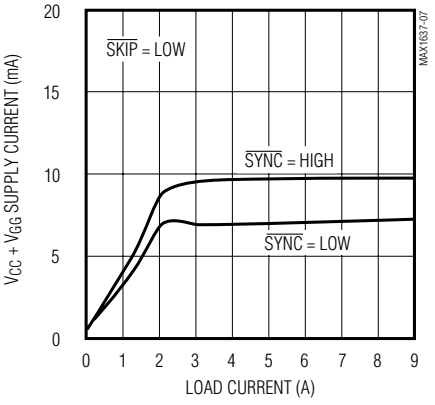
EFFICIENCY vs. LOAD CURRENT (3.3V/3A CIRCUIT)



SUPPLY CURRENT vs. SUPPLY VOLTAGE



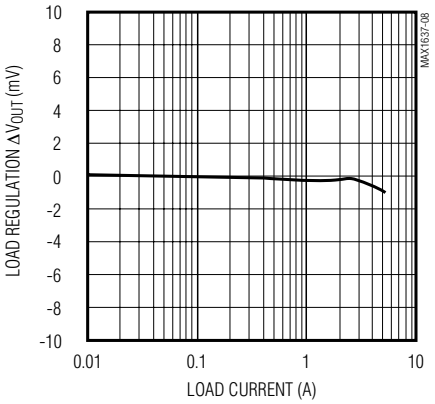
SUPPLY CURRENT vs. LOAD CURRENT



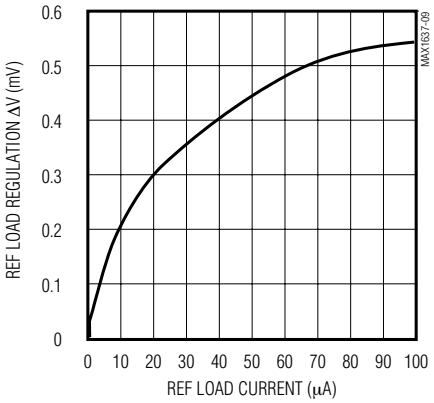
Typical Operating Characteristics (continued)

(V_{OUT} = 3.3V, T_A = +25°C, unless otherwise noted.)

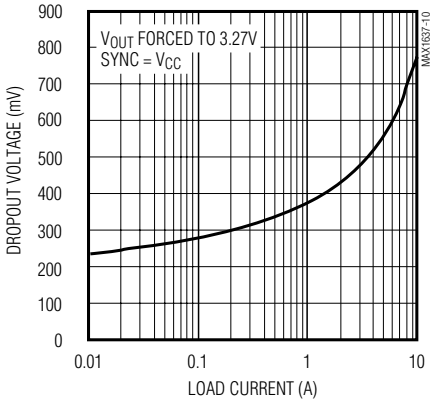
LOAD REGULATION vs. LOAD CURRENT



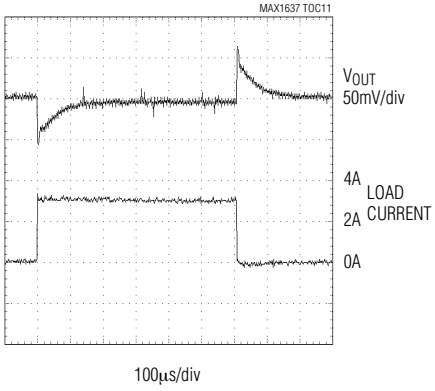
REF LOAD-REGULATION ERROR vs. REF LOAD CURRENT



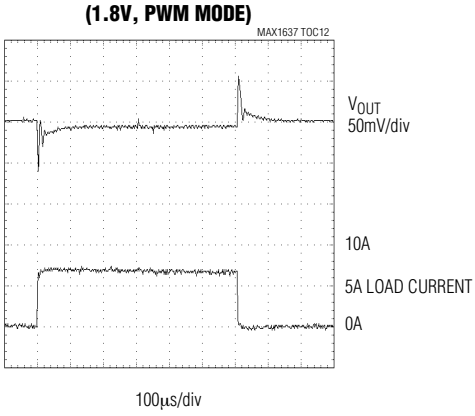
DROPOUT VOLTAGE vs. LOAD CURRENT



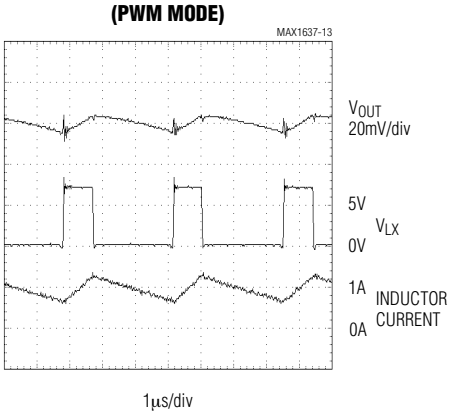
LOAD-TRANSIENT RESPONSE (3.3V/3A, PWM MODE)



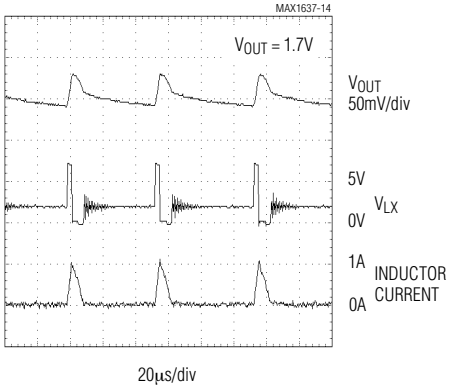
LOAD-TRANSIENT RESPONSE (1.8V, PWM MODE)



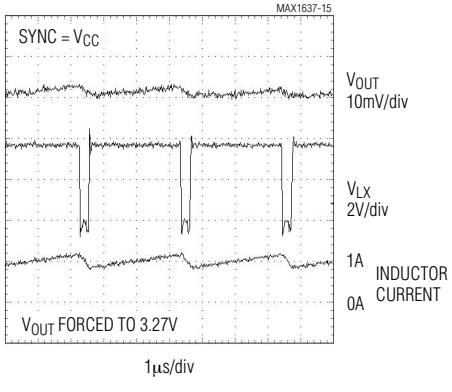
SWITCHING WAVEFORMS (PWM MODE)



SWITCHING WAVEFORMS (PFM MODE)



SWITCHING WAVEFORMS DROPOUT OPERATION

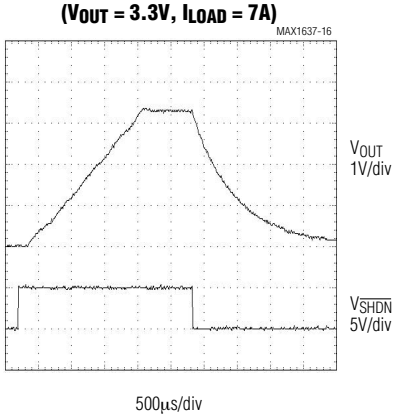


Miniature, Low-Voltage, Precision Step-Down Controller

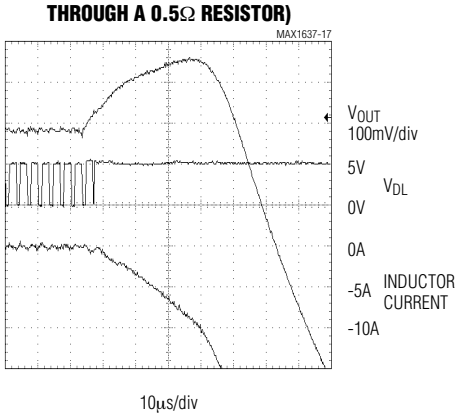
Typical Operating Characteristics (continued)

(V_{OUT} = 3.3V, T_A = +25°C, unless otherwise noted.)

TIME EXITING SHUTDOWN (V_{OUT} = 3.3V, I_{LOAD} = 7A)



OVERVOLTAGE-PROTECTION WAVEFORMS (V_{IN} SHORTED TO V_{OUT} THROUGH A 0.5Ω RESISTOR)



Pin Description

PIN	NAME	FUNCTION
1	CSH	High-Side Current-Sense Input
2	CSL	Low-Side Current-Sense Input
3	FB	Feedback Input. Connect to center of resistor divider.
4	CC	Compensation Pin. Connect a small capacitor to GND to set the integration time constant.
5	REF	1.100V Reference Output. Capable of sourcing 50µA for external loads. Bypass with 0.22µF minimum.
6	$\overline{SHDN}$	Shutdown Control Input. Turns off entire IC. When low, reduces supply current below 0.5µA (typ). Drive with logic input or connect to RC network between GND and V_{CC} for automatic start-up.
7	SYNC	Oscillator Frequency Select and Synchronization Input. Tie to V_{CC} for 300kHz operation; tie to GND for 200kHz operation.
8	GND	Analog Ground
9	V_{CC}	Main Analog Supply-Voltage Input to the Chip. V_{CC} powers the PWM controller, logic, and reference. Input range is 3.15V to 5.5V. Bypass to GND with a 0.1µF capacitor close to the pin.
10	V_{GG}	Gate-Drive and Boost-Circuit Power Supply. Can be driven from a supply other than V_{CC}. If the same supply is used by both V_{CC} and V_{GG}, isolate V_{CC} from V_{GG} with a 20Ω resistor. Bypass to PGND with a 4.7µF capacitor. V_{GG} current = (Q_{G1} + Q_{G2}) x f, where Q_G is the MOSFET gate charge at V_{GS} = V_{GG}.
11	DL	Low-Side Gate-Driver Output
12	PGND	Power Ground
13	BST	Boost Capacitor Connection
14	DH	High-Side Gate-Driver Output
15	LX	Inductor Connection
16	$\overline{SKIP}$	Low-Noise Mode Control. Forces fixed-frequency PWM operation when high.

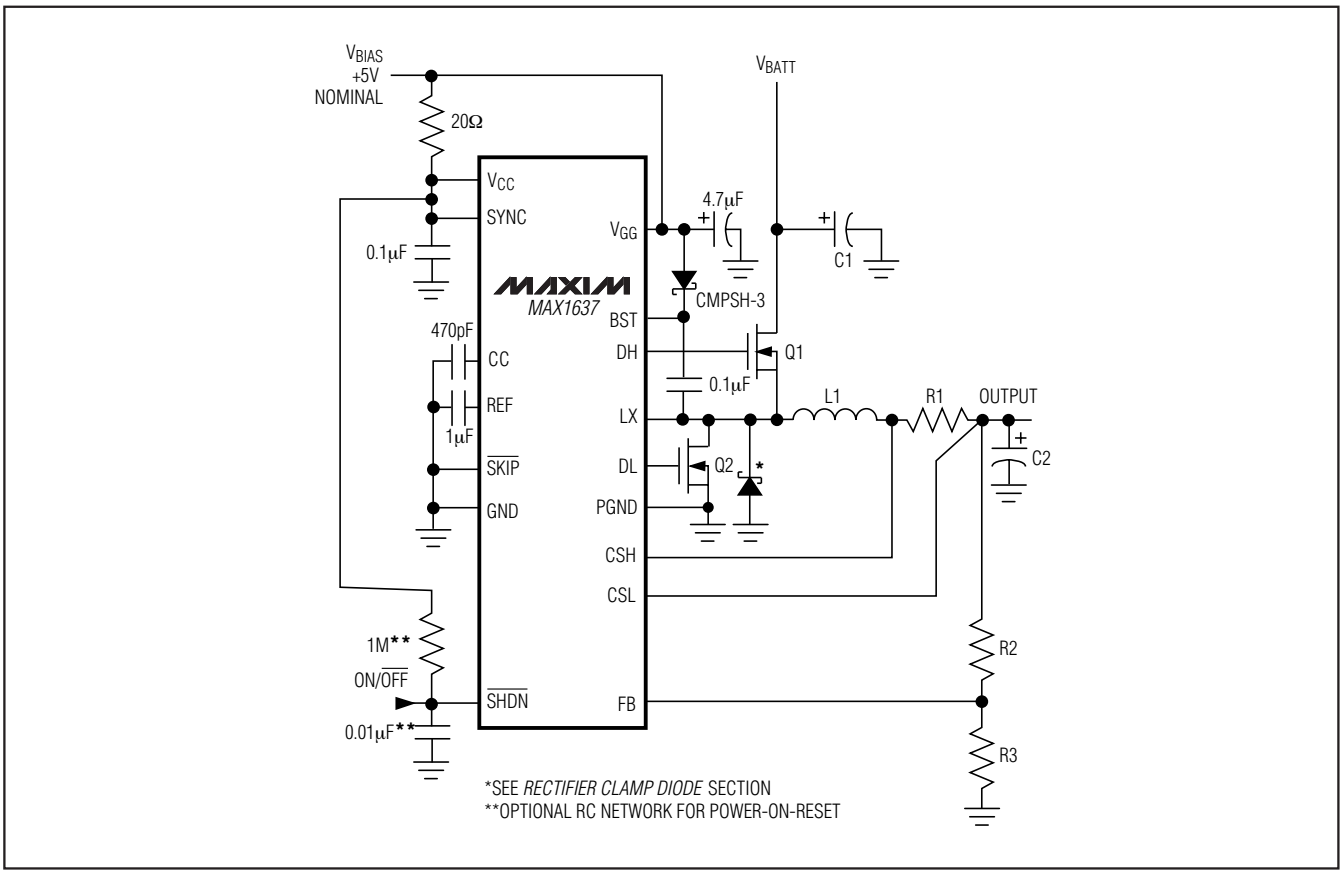


Figure 1. Standard Application Circuit

Standard Application Circuit

The basic MAX1637 buck converter (Figure 1) is easily adapted to meet a wide range of applications where a 5V or lower supply is available. The components listed in Table 1 represent a good set of trade-offs among cost, size, and efficiency, while staying within the worst-case specification limits for stress-related parameters such as capacitor ripple current. Do not change the circuit's switching frequency without first recalculating component values (particularly inductance value at maximum battery voltage).

The power Schottky diode across the synchronous rectifier is optional because the MOSFETs chosen incorporate a high-speed silicon diode. However, installing the Schottky will generally improve efficiency by about 1%. If used, the Schottky diode DC current must be rated to at least one-third of the maximum load current.

Detailed Description

The MAX1637 is a BiCMOS, switch-mode power-supply (SMPS) controller designed primarily for buck-topology regulators in battery-powered applications where high efficiency and low quiescent supply current are critical. Light-load efficiency is enhanced by automatic idle-mode operation—a variable-frequency, pulse-skipping mode that reduces transition and gate-charge losses. The step-down, power-switching circuit consists of two N-channel MOSFETs, a rectifier, and an LC output filter. Output voltage for this device is the average AC voltage at the switching node, which is regulated by changing the duty cycle of the MOSFET switches. The gate-drive signal to the high-side N-channel MOSFET, which must exceed the battery voltage, is provided by a flying-capacitor boost circuit that uses a 100nF capacitor between BST and LX. Figure 2 shows the major circuit blocks.

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Table 1. Component Selection for Standard Applications

COMPONENT	LOAD CURRENT			
	2A	3A (EV KIT)	7A (EV KIT)	3A
Input Voltage Range	7V to 22V	7V to 22V	7V to 22V	4.75V to 30V
Output Voltage Range	2.5V	2.5V	1.7V	3.3V
Application	Chipset Supply	Chipset Supply	CPU Core	General Purpose
Frequency	300kHz	300kHz	300kHz	300kHz
Q1 High-Side MOSFET	1/2 Si4902DY or 1/2 MMDF3NO3HD	International Rectifier IRF7403 or Siliconix Si4412	Fairchild FDS9412 or International Rectifier IRF7403	International Rectifier IRF7403 or Siliconix Si4412
Q2 Low-Side MOSFET	1/2 Si4902DY or 1/2 MMDF3NO3HD	International Rectifier IRF7413 or Siliconix Si4410DY	Fairchild FDS6680 or Siliconix Si4420DY	International Rectifier IRF7413 or Siliconix Si4410DY
C1 Input Capacitor	10µF, 25V ceramic Tokin C34Y5U1E106Z or Marcon/United Chemicon THCR40E1E106ZT	10µF, 25V ceramic Tokin C34Y5U1E106Z or Marcon/United Chemicon THCR40E1E106ZT	4 x 10µF, 25V ceramic Tokin C34Y5U1E106Z or Marcon/United Chemicon THCR40E1E106ZT	10µF, 30V Sanyo OS-CON
C2 Output Capacitor	220µF, 6.3V tantalum Sprague 595D227X96R3C2	470µF, 6.3V tantalum Kemet T510X477(1)006AS or 470µF, 4V tantalum Sprague 594D477X0004R2T	3 x 470µF, 6.3V tantalum Kemet T510X477(1)006AS or 470µF, 4V tantalum Sprague 594D477X0004R2T	470µF, 6.3V tantalum Kemet T510X477(1)006AS or 470µF, 4V tantalum Sprague 594D477X0004R2T
R1 Resistor	0.033Ω, 1% (2010) Dale WSL-2010-R033F	0.020Ω, 1% (2010) Dale WSL-2010-R020F	0.010Ω, 1% (2512) Dale WSL-2512-R010F	0.020Ω, 1% (2010) Dale WSL-2010-R020F
L1 Inductor	10µH Coilcraft DO3316P-103 or Coiltronics UP2-100	10µH Sumida CDRH125-100	2.2µH Panasonic P1F2R0HL or Coiltronics UP4-2R2 or Coilcraft DO5022P-222HC	10µH Sumida CDRH125-100

Table 2. Component Suppliers

COMPANY	FACTORY FAX (COUNTRY CODE)	USA PHONE
AVX	(1) 803-626-3123	(803) 946-0690
Central Semiconductor	(1) 516-435-1824	(516) 435-1110
Coilcraft	(1) 847-639-1469	(847) 639-6400
Coiltronics	(1) 561-241-9339	(561) 241-7876
Dale	(1) 605-665-1627	(605) 668-4131
Fairchild	(1) 408-721-1635	(408) 721-2181
International Rectifier (IR)	(1) 310-322-3332	(310) 322-3331
IRC	(1) 512-992-3377	(512) 992-7900

COMPANY	FACTORY FAX (COUNTRY CODE)	USA PHONE
Marcon/United Chemi-Con	(1) 847-696-9278	(847) 696-2000
Matsuo	(1) 714-960-6492	(714) 969-2491
Motorola	(1) 602-994-6430	(602) 303-5454
Panasonic	(1) 714-373-7183	(714) 373-7939
Sanyo	(81) 7-2070-1174	(619) 661-6835
Siliconix	(1) 408-970-3950	(408) 988-8000
Sprague	(1) 603-224-1430	(603) 224-1961
Sumida	(81) 3-3607-5144	(847) 956-0666
TDK	(1) 847-390-4428	(847) 390-4373
Tokin	(1) 408-434-0375	(408) 432-8020

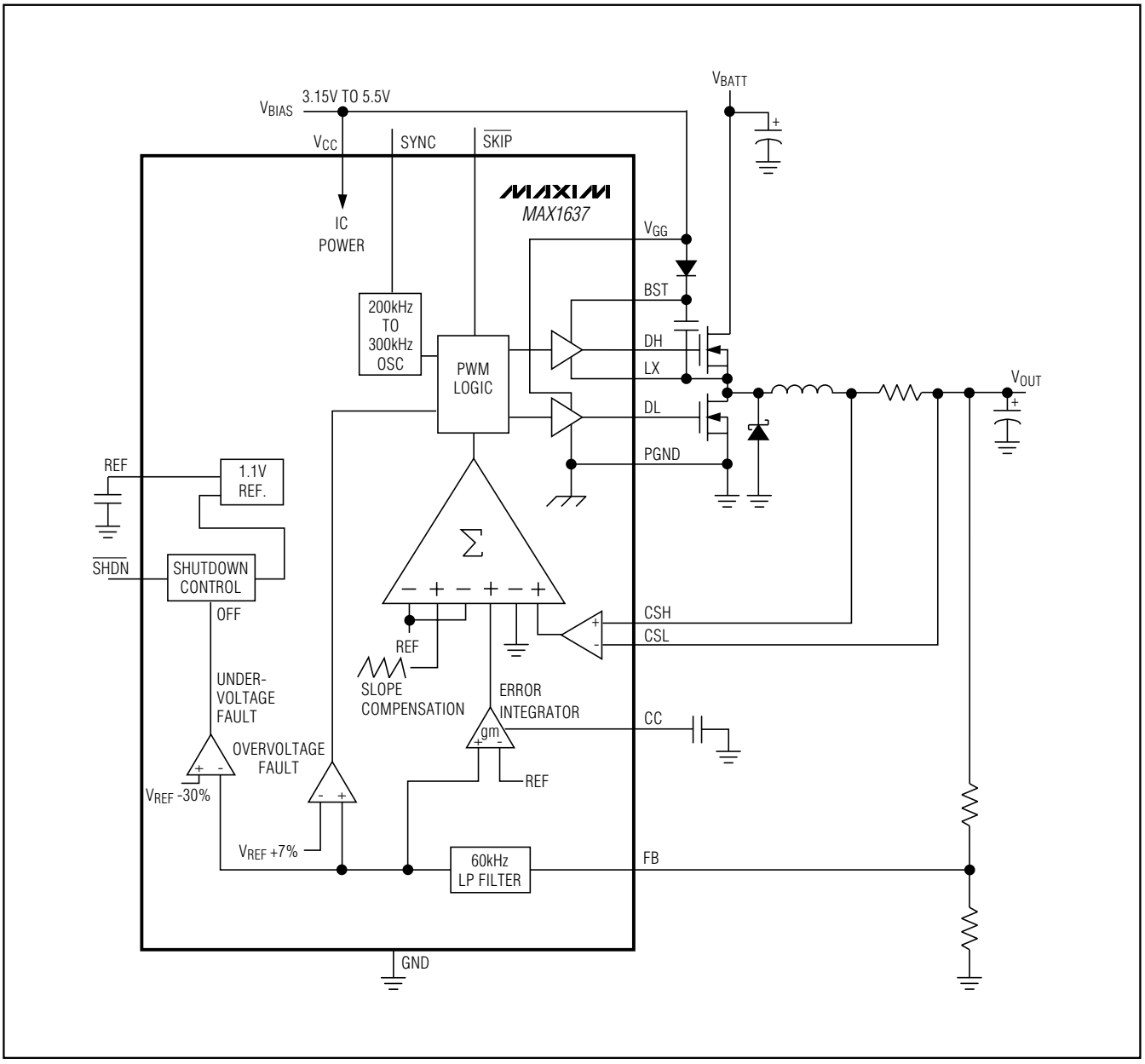

Figure 2. Functional Diagram

The pulse-width-modulation (PWM) controller consists of a multi-input PWM comparator, high-side and low-side gate drivers, and logic. It uses a 200kHz/300kHz synchronizable oscillator. The MAX1637 contains fault-protection circuits that monitor the PWM output for undervoltage and overvoltage. It includes a 1.100V precision reference. The circuit blocks are powered from an internal IC power rail that receives power from V_{CC}. V_{GG} provides direct power to the synchronous-switch gate driver, but provides indirect power to the high-side-switch gate driver via an external diode-capacitor boost circuit.

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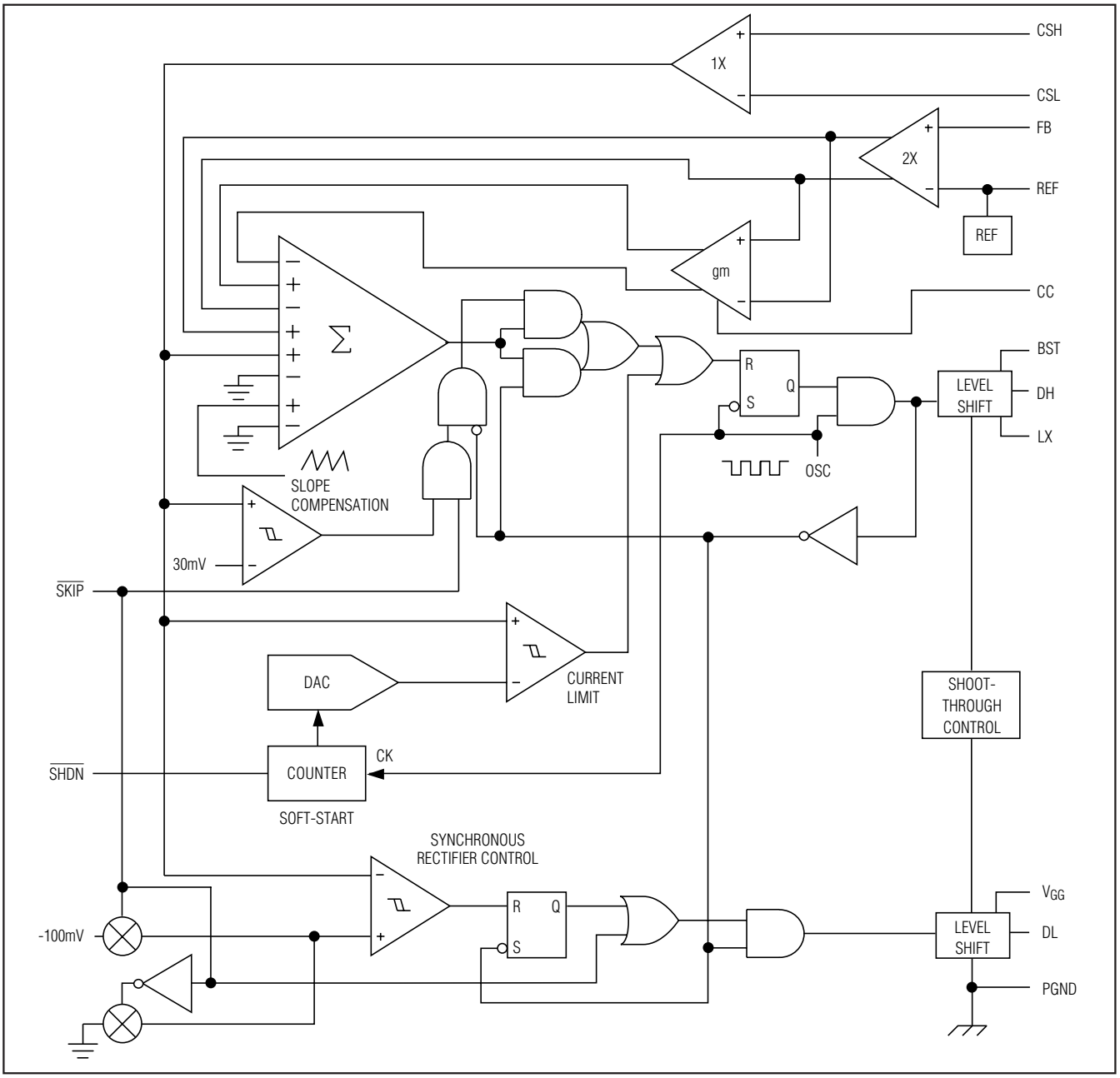

Figure 3. PWM Controller Functional Diagram

PWM Controller Block

The heart of the current-mode PWM controller is a multi-input, open-loop comparator that sums four signals: the output voltage error signal with respect to the reference voltage, the current-sense signal, the integrated voltage-feedback signal, and the slope-compensation ramp (Figure 3). The PWM controller is a direct-summing type, lacking a traditional error amplifier and the phase shift associated with it. This direct-summing configuration approaches ideal cycle-by-cycle control over the output voltage.

Idle Mode

When $\overline{SKIP}$ is low, idle-mode circuitry automatically optimizes efficiency throughout the load-current range. Idle mode dramatically improves light-load efficiency by reducing the effective frequency, subsequently reducing switching losses. It forces the peak inductor current to ramp to 30% of the full current limit, delivering extra energy to the output and allowing subsequent cycles to be skipped. Idle mode transitions seamlessly to fixed-frequency PWM operation as load current increases (Table 3).

Fixed-Frequency Mode

When $\overline{SKIP}$ is high, the controller always operates in fixed-frequency PWM mode for lowest noise. Each pulse from the oscillator sets the main PWM latch that turns on the high-side switch for a period determined by the duty factor (approximately V_{OUT} / V_{IN}). As the high-side switch turns off, the synchronous rectifier latch is set; 60ns later, the low-side switch turns on. The low-side switch stays on until the beginning of the next clock cycle.

In PWM mode, the controller operates as a fixed-frequency, current-mode controller in which the duty factor is set by the input/output voltage ratio. PWM mode ($\overline{SKIP}$ = high) forces two changes on the PWM controller. First, it disables the minimum-current comparator, ensuring fixed-frequency operation. Second, it changes the detection threshold for reverse-current limit from 0mV to -100mV, allowing the inductor current to reverse at light loads. This results in fixed-frequency operation and continuous inductor-current flow. PWM mode eliminates discontinuous-mode inductor ringing and improves cross-regulation of transformer-coupled, multiple-output supplies.

Table 3. $\overline{SKIP}$ PWM Table

$\overline{SKIP}$	LOAD CURRENT	MODE	DESCRIPTION
Low	Light	Idle	Pulse-skipping, discontinuous inductor current
Low	Heavy	PWM	Constant frequency PWM, continuous inductor current
High	Light	PWM	Constant frequency PWM, continuous inductor current
High	Heavy	PWM	Constant frequency PWM, continuous inductor current

The current-mode feedback system regulates the peak inductor-current value as a function of the output voltage error signal. In continuous-conduction mode, the average inductor current is nearly the same as the peak current, so the circuit acts as a switch-mode transconductance amplifier. This pushes the second output LC filter pole, normally found in a duty-factor-controlled (voltage-mode) PWM, to a higher frequency. To preserve inner-loop stability and eliminate regenerative inductor-current "staircasing," a slope-compensation ramp is summed into the main PWM comparator to make the apparent duty factor less than 50%.

The relative gains of the voltage-sense and current-sense inputs are weighted by the values of the current sources that bias four differential input stages in the main PWM comparator (Figure 4). The voltage sense into the PWM has been conditioned by an integrated component of the feedback voltage, yielding excellent DC output voltage accuracy. See the *Output Voltage Accuracy* section for details.

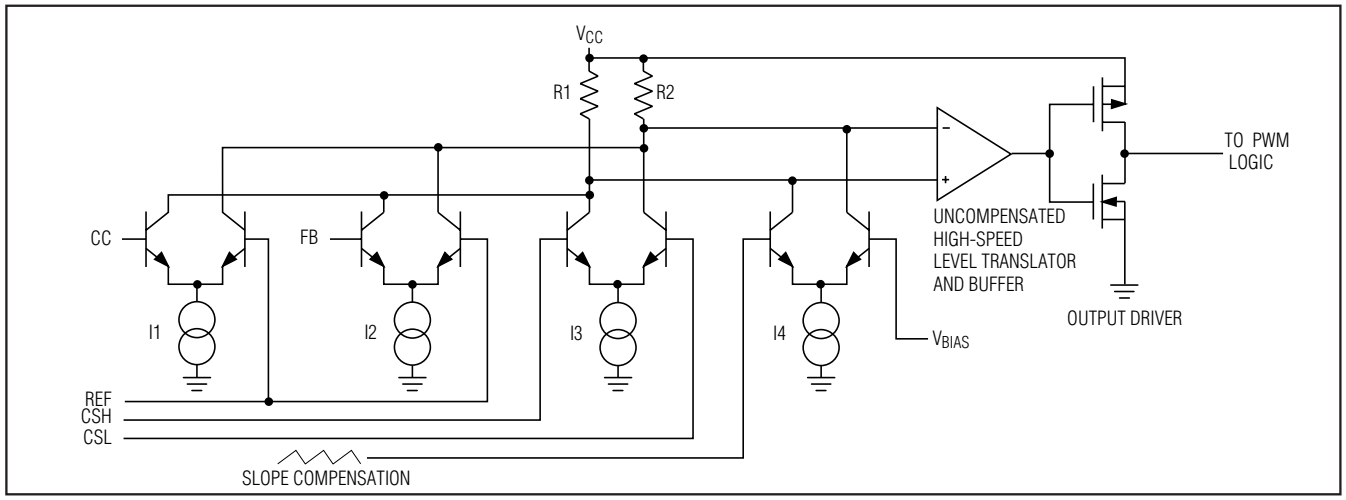

Figure 4. Main PWM Comparator Functional Diagram

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REF, V_{CC}, and V_{GG} Supplies

The 1.100V reference (REF) is accurate to ±2% over temperature, making REF useful as a precision system reference. Bypass REF to GND with a 0.22µF (min) capacitor. REF can supply up to 50µA for external loads. Loading REF reduces the main output voltage slightly because of the reference load-regulation error.

The MAX1637 has two independent supply pins, V_{CC} and V_{GG}. V_{CC} powers the sensitive analog circuitry of the SMPS, while V_{GG} powers the high-current MOSFET drivers. No protection diodes or sequencing requirements exist between the two supplies. Isolate V_{GG} from V_{CC} with a 20Ω resistor if they are powered from the same supply. Bypass V_{CC} to GND with a 0.1µF capacitor located directly adjacent to the pin. Use only small-signal diodes for the boost circuit (10mA to 100mA Schottky or 1N4148 diodes are preferred), and bypass V_{GG} to PGND with a 4.7µF capacitor directly at the package pins. The V_{CC} and V_{GG} input range is 3.15V to 5.5V.

High-Side Boost Gate Drive (BST)

Gate-drive voltage for the high-side N-channel switch is generated by a flying-capacitor boost circuit (Figure 2). The capacitor between BST and LX is alternately charged from the V_{GG} supply and placed parallel to the high-side MOSFET's gate-source terminals.

On start-up, the synchronous rectifier (low-side MOSFET) forces LX to 0V and charges the boost capacitor to V_{GG}. On the second half-cycle, the SMPS turns on the high-side MOSFET by closing an internal switch between BST and DH. This provides the necessary enhancement voltage to turn on the high-side switch, an action that boosts the gate-drive signal above the battery voltage.

Ringing at the high-side MOSFET gate (DH) in discontinuous-conduction mode (light loads) is a natural operating condition. It is caused by residual energy in the tank circuit, formed by the inductor and stray capacitance at the switching node, LX. The gate-drive negative rail is referred to LX, so any ringing there is directly coupled to the gate-drive output.

Synchronous-Rectifier Driver (DL)

Synchronous rectification reduces conduction losses in the rectifier by shunting the normal Schottky catch diode with a low-resistance MOSFET switch. Also, the synchronous rectifier ensures proper start-up of the boost gate-driver circuit. If the synchronous power MOSFET is omitted for cost or other reasons, replace it with a small-signal MOSFET, such as a 2N7002.

If the circuit is operating in continuous-conduction mode, the DL drive waveform is simply the complement of the DH high-side-drive waveform (with controlled dead time to prevent cross-conduction or "shoot-through"). In discontinuous (light-load) mode, the synchronous switch is turned off as the inductor current falls through zero.

Shutdown Mode and Power-On Reset

$\overline{SHDN}$ is a logic input with a threshold of about 1.5V that, when held low, places the IC in its 0.5µA shutdown mode. The MAX1637 has no power-on-reset circuitry, and the state of the device is not known on initial power-up. In applications that use logic to drive $\overline{SHDN}$, it may be necessary to toggle $\overline{SHDN}$ to initialize the part once V_{CC} is stable. In applications that require automatic start-up, drive $\overline{SHDN}$ through an external RC network (Figure 5). The network will hold $\overline{SHDN}$ low until V_{CC} stabilizes. Typical values for R and C are 1MΩ and 0.01µF. For slow-rising V_{CC}, use a larger capacitor. When cycling V_{CC}, V_{CC} must stay low long enough to discharge the 0.01µF capacitor, otherwise the circuit may not start. A diode may be added in parallel with the resistor to speed up the discharge.

Current-Limiting and Current-Sense Inputs (CSH and CSL)

The current-limit circuit resets the main PWM latch and turns off the high-side MOSFET switch whenever the voltage difference between CSH and CSL exceeds 100mV. This limiting is effective for both current flow directions, putting the threshold limit at ±100mV. The tolerance on the positive current limit is ±20%, so the external low-value sense resistor (R1) must be sized for 80mV / I_{PEAK}, where I_{PEAK} is the peak inductor current required to support the full load current. Components must be designed to withstand continuous current stresses of 120mV / R1.

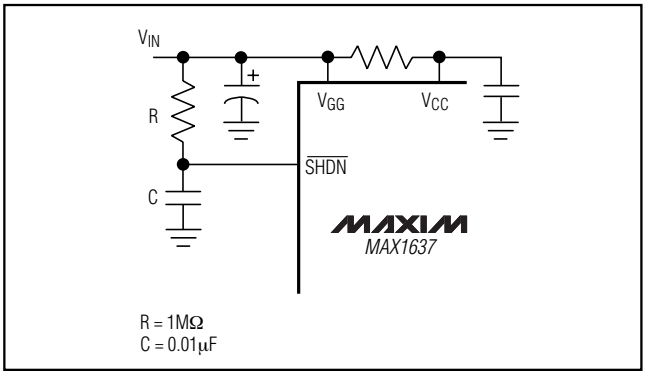

Figure 5. Power-On Reset RC Network for Automatic Start-Up

For prototyping or for very high-current applications, it may be useful to wire the current-sense inputs with a twisted pair rather than PC traces (two pieces of wrapped wire twisted together are sufficient). This reduces the noise picked up at CSH and CSL, which can cause unstable switching and reduced output current.

Oscillator Frequency and Synchronization (SYNC)

The SYNC input controls the oscillator frequency as follows: low selects 200kHz, high selects 300kHz. SYNC can also be used to synchronize with an external 5V CMOS or TTL clock generator. It has a guaranteed 240kHz to 340kHz capture range. A high-to-low transition on SYNC initiates a new cycle.

Operation at 300kHz optimizes the application circuit for component size and cost. Operation at 200kHz increases efficiency, reduces dropout, and improves load-transient response at low input-output voltage differences (see the *Low-Voltage Operation* section).

Output Voltage Accuracy (CC)

Output voltage error is guaranteed to be within ±2% over all conditions of line, load, and temperature. The MAX1637's DC load regulation is typically better than 0.1%, due to its integrator amplifier. The device optimizes transient response by providing a feedback signal with a direct path from the output to the main summing PWM comparator. The integrated feedback signal from the CC transconductance amplifier is also summed into the PWM comparator, with the gain weighted so that the signal has only enough gain to correct the DC inaccuracies. The integrator's response time is determined by the time constant set by the capacitor placed on the CC pin. The time constant should neither be so fast that the integrator responds to the normal V_{OUT} ripple, nor too slow to negate the integrator's effect. A 470pF to 1500pF CC capacitor is sufficient for 200kHz to 300kHz frequencies.

Figure 6 shows the output voltage response to a 0A to 3A load transient with and without the integrator. With the integrator, the output voltage returns to within 0.1% of its no-load value with only a small AC excursion. Without the integrator, load regulation is degraded (Figure 6b). Asymmetrical clamping at the integrator output prevents worsening of load transients during pulse-skipping mode.

Output Undervoltage Lockout

The output undervoltage-lockout circuit protects against heavy overloads and short-circuits at the main SMPS output. This scheme employs a timer rather than a foldback current limit. The SMPS has an undervoltage-protection circuit, which is activated 6144 clock cycles after the SMPS is enabled. If the SMPS output is under 70% of the nominal value, it is latched off and does not restart until $\overline{SHDN}$ is toggled. Applications that use the recommended RC power-on-reset circuit will also clear the fault condition when V_{CC} falls below 0.5V (typical). Note that undervoltage protection can

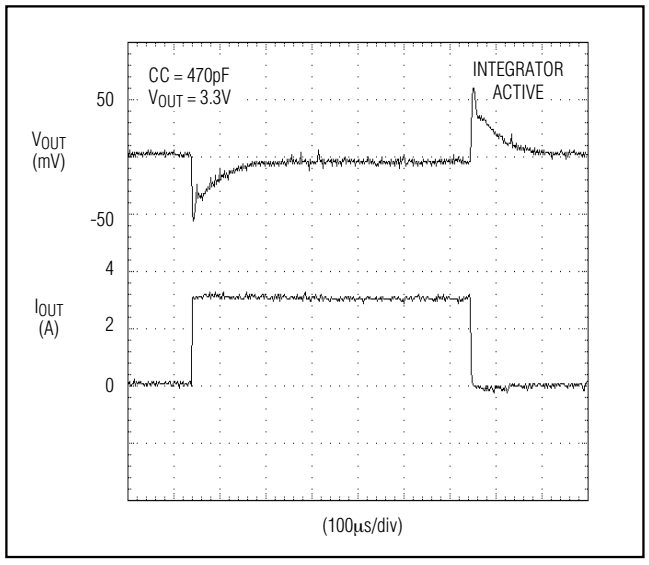

Figure 6a. Load-Transient Response with Integrator Active

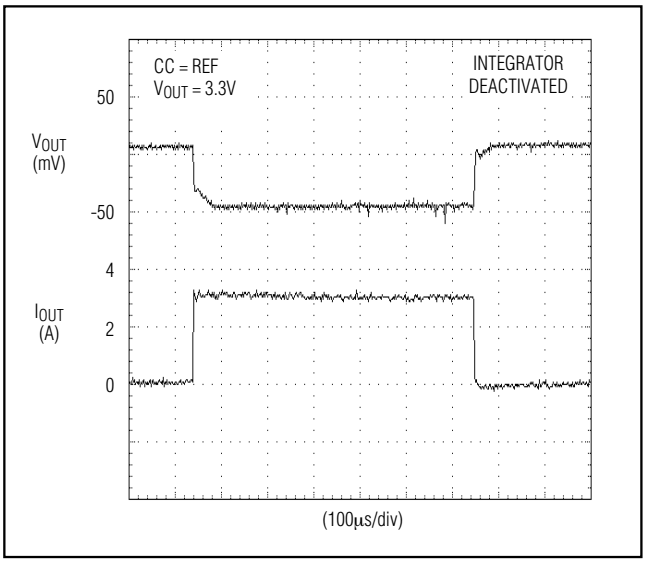

Figure 6b. Load-Transient Response with Integrator Deactivated

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make prototype troubleshooting difficult since only 20ms or 30ms elapse before the SMPS is latched off. The overvoltage crowbar protection is disabled in output undervoltage mode.

Output Overvoltage Protection

The overvoltage crowbar-protection circuit is intended to blow a fuse in series with the battery if the main SMPS output rises significantly higher than its standard level (Table 4). In normal operation, the output is compared to the internal precision reference voltage. If the output goes 7% above nominal, the synchronous-rectifier MOSFET turns on 100% (the high-side MOSFET is simultaneously forced off) in order to draw massive amounts of battery current to blow the fuse. This safety feature does not protect the system against a failure of the controller IC itself, but is intended primarily to guard against a short across the high-side MOSFET. A crowbar event is latched and can only be reset by a rising edge on $\overline{SHDN}$ (or by removal of the V_{CC} supply voltage). The overvoltage-detection decision is made relative to the regulation point.

Internal Digital Soft-Start Circuit

Soft-start allows a gradual increase of the internal current-limit level at start-up to reduce input surge currents. The SMPS contains an internal digital soft-start circuit controlled by a counter, a digital-to-analog converter (DAC), and a current-limit comparator. In shutdown, the soft-start counter is reset to zero. When the SMPS is enabled, its counter starts counting oscillator pulses, and the DAC begins incrementing the comparison voltage applied to the current-limit comparator. The DAC output increases from 0mV to 100mV in five equal steps as the count increases to 512 clocks. As a result, the main output capacitor charges up relatively slowly. The exact time of the output rise depends on output capacitance and load current, but it is typically 1ms with a 300kHz oscillator.

Setting the Output Voltage

The output voltage is set via a resistor divider connected to FB (Figure 1). Calculate the output voltage with the following formula:

$$V_{OUT} = V_{REF} (1 + R2 / R3)$$

where V_{REF} = 1.1V nominal.

Recommended normal values for R3 range from 5kΩ to 100kΩ. To achieve a 1.1V nominal output, connect FB directly to CSL. Remote output voltage sensing is possible by using the top of the external resistor divider as the remote sense point.

Design Procedure

The standard application circuit (Figure 1) contains a ready-to-use solution for common application needs. Use the following design procedure to optimize the basic schematic for different voltage or current requirements. But before beginning a design, firmly establish the following:

- Maximum input (battery) voltage, $V_{IN(MAX)}$. This value should include the worst-case conditions, such as no-load operation when a battery charger or AC adapter is connected but no battery is installed. $V_{IN(MAX)}$ must not exceed 30V.
- Minimum input (battery) voltage, $V_{IN(MIN)}$. This value should be taken at full load under the lowest battery conditions. If the minimum input-output difference is less than 1.5V, the filter capacitance required to maintain good AC load regulation increases (see *Low-Voltage Operation* section).

Table 4. Operating Modes

MODE	$\overline{SHDN}$	CONDITIONS	STATUS	NOTES
Run	High	V_{OUT} in regulation	All circuit blocks active	Normal operation
Shutdown	Low	—	All circuit blocks off	Lowest current consumption
Overvoltage (Crowbar)	High	V_{OUT} greater than 7% above regulation point	REF = off, DL = high	Rising edge on $\overline{SHDN}$ exits crowbar
Output Undervoltage Lockout	High	V_{OUT} below 70% of nominal after 20ms to 30ms timeout expires	REF = off, DL = low	Rising edge on $\overline{SHDN}$ exits UVLO

Inductor Value

The exact inductor value is not critical and can be freely adjusted to allow trade-offs among size, cost, and efficiency. Lower inductor values minimize size and cost, but reduce efficiency due to higher peak-current levels. The smallest inductor value is obtained by lowering the inductance until the circuit operates at the border between continuous and discontinuous mode. Further reducing the inductor value below this crossover point results in discontinuous-conduction operation, even at full load. This helps lower output filter capacitance requirements, but efficiency suffers under these conditions, due to high I^2R losses. On the other hand, higher inductor values produce greater efficiency, but also result in resistive losses due to extra wire turns—a consequence that eventually overshadows the benefits gained from lower peak current levels. High inductor values can also affect load-transient response (see the V_{SAG} equation in the *Low-Voltage Operation* section). The equations in this section are for continuous-conduction operation.

Three key inductor parameters must be specified: inductance value (L), peak current (I_{PEAK}), and DC resistance (R_{DC}). The following equation includes a constant, LIR, which is the ratio of inductor peak-to-peak AC current to DC load current. A higher LIR value allows lower inductance, but results in higher losses and ripple. A good compromise is a 30% ripple-current to load-current ratio (LIR = 0.3), which corresponds to a peak inductor current 1.15 times higher than the DC load current.

$$L = V_{OUT}(V_{IN(MAX)} - V_{OUT}) / (V_{IN(MIN)} \times f \times I_{OUT} \times LIR)$$

where f = switching frequency (normally 200kHz or 300kHz), and I_{OUT} = maximum DC load current.

The peak current can be calculated as follows:

$$I_{PEAK} = I_{LOAD} + [V_{OUT}(V_{IN(MAX)} - V_{OUT}) / (2 \times f \times L \times V_{IN(MAX)})]$$

The inductor's DC resistance should be low enough that $R_{DC} \times I_{PEAK} < 100mV$, as it is a key parameter for efficiency performance. If a standard, off-the-shelf inductor is not available, choose a core with an LI^2 rating greater than $L \times IPEAK^2$ and wind it with the largest diameter wire that fits the winding area. For 300kHz applications, ferrite-core material is strongly preferred; for 200kHz applications, Kool-Mu® (aluminum alloy) or even powdered iron is acceptable. If light-load efficiency is unimportant (in desktop PC applications, for example), then low-permeability iron-powder cores can be acceptable, even at 300kHz. For high-current applications, shielded-core geometries (such as toroidal or pot core) help keep noise, EMI, and switching-waveform jitter low.

Current-Sense Resistor Value

The current-sense resistor value is calculated according to the worst-case, low-current limit threshold voltage (from the *Electrical Characteristics*) and the peak inductor current:

$$R_{SENSE} = 80mV / I_{PEAK}$$

Use I_{PEAK} from the second equation in the *Inductor Value* section. Use the calculated value of R_{SENSE} to size the MOSFET switches and specify inductor saturation-current ratings according to the worst-case high-current-limit threshold voltage:

$$I_{PEAK} = 120mV / R_{SENSE}$$

Low-inductance resistors, such as surface-mount metal film, are recommended.

Input Capacitor Value

Connect low-ESR bulk capacitors directly to the drain on the high-side MOSFET. The bulk input filter capacitor is usually selected according to input ripple current requirements and voltage rating, rather than capacitor value. Electrolytic capacitors with low enough equivalent series resistance (ESR) to meet the ripple-current requirement invariably have sufficient capacitance values. Aluminum electrolytic capacitors, such as Sanyo OS-CON or Nichicon PL, are superior to tantalum types, which risk power-up surge-current failure, especially when connecting to robust AC adapters or low-impedance batteries. RMS input ripple current (I_{RMS}) is determined by the input voltage and load current, with the worst case occurring at $V_{IN} = 2 \times V_{OUT}$. Therefore, when V_{IN} is $2 \times V_{OUT}$:

$$I_{RMS} = I_{LOAD} / 2$$

V_{CC} and V_{GG} should be isolated from each other with a 20Ω resistor and bypassed to ground independently. Place a 0.1µF capacitor between V_{CC} and GND, as close to the supply pin as possible. A 4.7µF capacitor is recommended between V_{GG} and PGND.

Output Filter Capacitor Value

The output filter capacitor values are generally determined by the ESR and voltage-rating requirements, rather than by actual capacitance requirements for loop stability. In other words, the low-ESR electrolytic capacitor that meets the ESR requirement usually has more output capacitance than is required for AC stability.

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Miniature, Low-Voltage, Precision Step-Down Controller

Use only specialized low-ESR capacitors intended for switching-regulator applications, such as AVX TPS, Sprague 595D, Sanyo OS-CON, or Nichicon PL series. To ensure stability, the capacitor must meet both minimum capacitance and maximum ESR values as given in the following equations:

$$C_{OUT} > V_{REF}(1 + V_{OUT} / V_{IN(MIN)}) / V_{OUT} \times R_{SENSE} \times f$$

$$R_{ESR} < R_{SENSE} \times V_{OUT} / V_{REF}$$

where R_{ESR} can be multiplied by 1.5, as discussed below.

These equations are worst case, with 45 degrees of phase margin to ensure jitter-free, fixed-frequency operation, and provide a nicely damped output response for zero to full-load step changes. Some cost-conscious designers may wish to bend these rules with less-expensive capacitors, particularly if the load lacks large step changes. This practice is tolerable if some bench testing over temperature is done to verify acceptable noise and transient response.

No well-defined boundary exists between stable and unstable operation. As phase margin is reduced, the first symptom is timing jitter, which shows up as blurred edges in the switching waveforms where the scope does not quite sync up. Technically speaking, this jitter (usually harmless) is unstable operation since the duty factor varies slightly. As capacitors with higher ESRs are used, the jitter becomes more pronounced, and the load-transient output voltage waveform starts looking ragged at the edges. Eventually, the load-transient waveform has enough ringing on it that the peak noise levels exceed the allowable output voltage tolerance. Note that even with zero phase margin and gross instability, the output voltage seldom declines beyond $I_{PEAK} \times R_{ESR}$ (under constant loads).

Designers of RF communicators or other noise-sensitive analog equipment should be conservative and stay within the guidelines. Designers of notebook computers and similar commercial-temperature-range digital systems can multiply the R_{ESR} value by a factor of 1.5 without affecting stability or transient response.

The output voltage ripple, which is usually dominated by the filter capacitor's ESR, can be approximated as $I_{RIPPLE} \times R_{ESR}$. There is also a capacitive term, so the full equation for ripple in continuous-conduction mode is $V_{RIPPLE(p-p)} = I_{RIPPLE} \times [R_{ESR} + 1 / (2\pi f \times C_{OUT})]$. In idle mode, the inductor current becomes discontinuous, with high peaks and widely spaced pulses, so the noise can actually be higher at light load (compared to full load). In idle mode, calculate the output ripple as follows:

$$V_{RIPPLE(p-p)} = (0.02 \times R_{ESR} / R_{SENSE}) + [0.0003 \times L \times (1 / V_{OUT} + 1 / (V_{IN} - V_{OUT})) / R_{SENSE}^2 \times C_F]$$

Selecting Other Components

MOSFET Switches

The high-current N-channel MOSFETs must be logic-level types with guaranteed on-resistance specifications at V_{GS} = 4.5V. Lower gate-threshold specifications are better (i.e., 2V max rather than 3V max). Drain-source breakdown voltage ratings must at least equal the maximum input voltage, preferably with a 20% margin. The best MOSFETs have the lowest on-resistance per nanocoulomb of gate charge. Multiplying $R_{DS(ON)}$ by Qg provides a good figure of merit for comparing various MOSFETs. Newer MOSFET process technologies with dense cell structures generally perform best. The internal gate drivers tolerate >100nC total gate charge, but 70nC is a more practical upper limit to maintain best switching times.

In high-current applications, MOSFET package power dissipation often becomes a dominant design factor. I^2R power losses are the greatest heat contributor for both high-side and low-side MOSFETs. I^2R losses are distributed between Q1 and Q2 according to duty factor, as shown in the following equations. Generally, switching losses affect only the upper MOSFET since the Schottky rectifier usually clamps the switching node before the synchronous rectifier turns on. Gate-charge losses are dissipated by the driver and do not heat the MOSFET. Calculate the temperature rise according to package thermal-resistance specifications to ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature. The worst-case dissipation for the high-side MOSFET occurs at both extremes of input voltage, and the worst-case dissipation for the low-side MOSFET occurs at maximum input voltage.

$$Duty = (V_{OUT} + V_{Q2}) / (V_{IN} - V_{Q1})$$

$$P_{D\ (UPPER\ FET)} = I_{LOAD}^2 \times R_{DS(ON)} \times duty + V_{IN} \times I_{LOAD} \times f \times [(V_{IN} \times C_{RSS}) / I_{GATE} + 20ns]$$

$$P_{D\ (LOWER\ FET)} = I_{LOAD}^2 \times R_{DS(ON)} \times (1 - duty)$$

where V_Q = the on-state voltage drop ($I_{LOAD} \times R_{DS(ON)}$), C_{RSS} = the MOSFET reverse transfer capacitance, I_{GATE} = the DH driver peak output current capability (1A typ), and the DH driver inherent rise/fall time is 20ns. The MAX1637's output undervoltage shutdown function protects the synchronous rectifier under output short-circuit conditions. To reduce EMI, add a 0.1µF ceramic capacitor from the high-side switch drain to the low-side switch source.

Rectifier Clamp Diode

The rectifier is a clamp across the low-side MOSFET that catches the negative inductor swing during the 60ns dead time between turning one MOSFET off and turning each low-side MOSFET on. The latest generations of MOSFETs incorporate a high-speed silicon body diode, which serves as an adequate clamp diode if efficiency is not of primary importance. A Schottky diode can be placed in parallel with the body diode to reduce the forward voltage drop, typically improving efficiency 1% to 2%. Use a diode with a DC current rating equal to one-third of the load current; for example, use an MBR0530 (500mA-rated) type for loads up to 1.5A, a 1N5819 type for loads up to 3A, or a 1N5822 type for loads up to 10A. The rectifier's rated reverse-breakdown voltage must be at least equal to the maximum input voltage, preferably with a 20% margin.

Boost-Supply Diode D2

A signal diode such as a 1N4148 works well in most applications. Do not use large power diodes, such as 1N5817 or 1N4001.

Low-Voltage Operation

Low input voltages and low input-output differential voltages each require extra care in their design. Low V_{IN}-V_{OUT} differentials can cause the output voltage to sag when the load current changes abruptly. The sag's amplitude is a function of inductor value and maximum duty factor (D_{MAX}, an *Electrical Characteristics* parameter, 93% guaranteed over temperature at f = 200kHz) as follows:

$$V_{SAG} = [(I_{STEP})^2 \times L] / [2C_F \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})]$$

Table 5 is a low-voltage troubleshooting guide. The cure for low-voltage sag is to increase the output capacitor's value. For example, at V_{IN} = 5.5V, V_{OUT} = 5V, L = 10µH, f = 200kHz, and I_{STEP} = 3A, a total capacitance of 660µF keeps the sag below 200mV. Note that only the capacitance requirement increases; the ESR requirements do not change. Therefore, the added capacitance can be supplied by a low-cost bulk capacitor in parallel with the normal low-ESR capacitor.

Applications Information

Heavy-Load Efficiency Considerations

The major efficiency-loss mechanisms under loads are as follows, in the usual order of importance:

- $P(I^2R) = I^2R$ losses
- P(tran) = transition losses
- P(gate) = gate-charge losses
- P(diode) = diode-conduction losses
- P(cap) = capacitor ESR losses
- P(IC) = losses due to the IC's operating supply current

Inductor core losses are fairly low at heavy loads because the inductor's AC current component is small. Therefore, these losses are not considered in this analysis. Ferrite cores are preferred, especially at 300kHz, but powdered cores, such as Kool-Mu, can also work well.

$$\text{Efficiency} = P_{OUT} / P_{IN} \times 100\%$$

$$= P_{OUT} / (P_{OUT} + P_{TOTAL}) \times 100\%$$

$$P_{TOTAL} = P(I^2R) + P(\text{tran}) + P(\text{gate}) + P(\text{diode}) + P(\text{cap}) + P(\text{IC})$$

$$P = (I^2R) = I_{LOAD}^2 \times (R_{DC} + R_{DS(ON)} + R_{SENSE})$$

where R_{DC} is the DC resistance of the coil, $R_{DS(ON)}$ is the MOSFET on-resistance, and R_{SENSE} is the current-sense resistor value. The $R_{DS(ON)}$ term assumes identical MOSFETs for the high-side and low-side switches because they time-share the inductor current. If the MOSFETs are not identical, their losses can be estimated by averaging the losses according to duty factor.

$$PD(\text{tran}) = \text{transition loss} = V_{IN} \times I_{LOAD} \times f \times [(V_{IN} C_{RSS} / I_{GATE}) + 20\text{ns}]$$

where C_{RSS} is the reverse transfer capacitance of the high-side MOSFET (a data sheet parameter), I_{GATE} is the DH gate-driver peak output current (1.5A typ), and the rise/fall time of the DH driver is typically 20ns.

Table 5. Low-Voltage Troubleshooting Guide

SYMPTOM	CONDITION	ROOT CAUSE	SOLUTION
Sag or droop in V_{OUT} under step-load change	Low V_{IN}-V_{OUT} differential, under 1.5V	Limited inductor-current slew rate per cycle	Increase bulk output capacitance per formula (see *Low-Voltage Operation* section). Reduce inductor value.
Dropout voltage is too high	Low V_{IN}-V_{OUT} differential, under 1V	Maximum duty-cycle limits exceeded	Reduce operation to 200kHz. Reduce MOSFET on-resistance and coil DC resistance.

Miniature, Low-Voltage, Precision Step-Down Controller

$$P(gate) = Q_g \times f \times V_{GG}$$

where Q_g is the sum of the gate-charge values for low-side and high-side switches. For matched MOSFETs, Q_g is twice the data-sheet value of an individual MOSFET. Efficiency can usually be optimized by connecting V_{GG} to the most efficient 5V source, such as the system +5V supply.

$$P(diode) = \text{diode conduction losses} = I_{LOAD} \times V_{FWD} \times t_D \times f$$

where t_D is the diode conduction time (120ns typ), and V_{FWD} is the diode forward voltage. This power is dissipated in the MOSFET body diode if no external Schottky diode is used.

$$P(cap) = \text{input capacitor ESR loss} = I_{RMS}^2 \times R_{ESR}$$

where I_{RMS} is the input ripple current as calculated in the *Input Capacitor Value* section.

Light-Load Efficiency Considerations

Under light loads, the PWM operates in discontinuous mode. The inductor current discharges to zero at some point during the charging cycle. This makes the inductor current's AC component high compared to the load current, which increases core losses and I^2R losses in the input-output filter capacitors. For best light-load efficiency, use MOSFETs with moderate gate-charge levels and use ferrite MPP or other low-loss core material. Avoid powdered-iron cores; even Kool-Mu (aluminum alloy) is not as desirable as ferrite.

Low-Noise Operation

Noise-sensitive applications such as hi-fidelity multimedia-equipped systems, cellular phones, RF communicating computers, and electromagnetic pen-entry systems should operate the controller in PWM mode ($\overline{SKIP}$ = high). This mode forces a constant switching frequency, reducing interference due to switching noise by concentrating the radiated EM fields at a known frequency outside the system audio or IF bands. Choose an oscillator frequency for which switching-frequency harmonics do not overlap a sensitive frequency band. If necessary, synchronize the oscillator to a tight-tolerance external clock generator.

Powering From a Single Low-Voltage Supply

The circuit of Figure 7 is powered from a single 3.3V to 5.5V source and delivers 4A at 2.5V. At input voltages of 3.15V, this circuit typically achieves efficiencies of 90% at 3.5A load currents. When using a single supply to power both V_{BATT} and V_{BIAS}, be sure that it does not exceed the 5.5V rating (6V absolute maximum) for V_{GG} and V_{CC}. Also, heavy current surges from the input may cause transient dips on V_{CC}. To prevent this, the decoupling capacitor on V_{CC} may need to be increased to 2µF or greater. This circuit uses low-threshold (specified at V_{GS} = 2.7V) IRF7401 MOSFETs which allow a typical startup of 3.15V at above 4A. Low input voltages demand the use of larger input capacitors. Sanyo OS-CONs are recommended for their high capacity and low ESR.

PC Board Layout Considerations

Good PC board layout is required to achieve specified noise, efficiency, and stable performance. The PC board layout artist must be given explicit instructions, preferably a pencil sketch showing the placement of power-switching components and high-current routing. See the PC board layout in the MAX1637 evaluation kit manual for examples. A ground plane is essential for optimum performance. In most applications, the circuit will be located on a multi-layer board, and full use of the four or more copper layers is recommended. Use the top layer for high-current connections, the bottom layer for quiet connections (REF, CC, GND), and the inner layers for an uninterrupted ground plane. Use the following step-by-step guide:

1) Place the high-power components (C1, C2, Q1, Q2, D1, L1, and R1) first, with their grounds adjacent.
   - *Minimize current-sense resistor trace lengths* and ensure accurate current sensing with Kelvin connections (Figure 8).
   - *Minimize ground trace lengths* in the high-current paths.
   - *Minimize other trace lengths* in the high-current paths.
     - — Use >5mm-wide traces.
     - — CIN to high-side MOSFET drain: 10mm max length
     - — Rectifier diode cathode to low side
     - — MOSFET: 5mm max length
     - — LX node (MOSFETs, rectifier cathode, inductor): 15mm max length

Ideally, surface-mount power components are butted up to one another with their ground terminals almost touching. These high-current grounds are then connected to each other with a wide, filled zone of top-layer copper so they do not go through vias. The resulting top-layer subground plane is connected to the normal inner-layer ground plane at the output ground terminals, which ensures that the IC's analog ground is

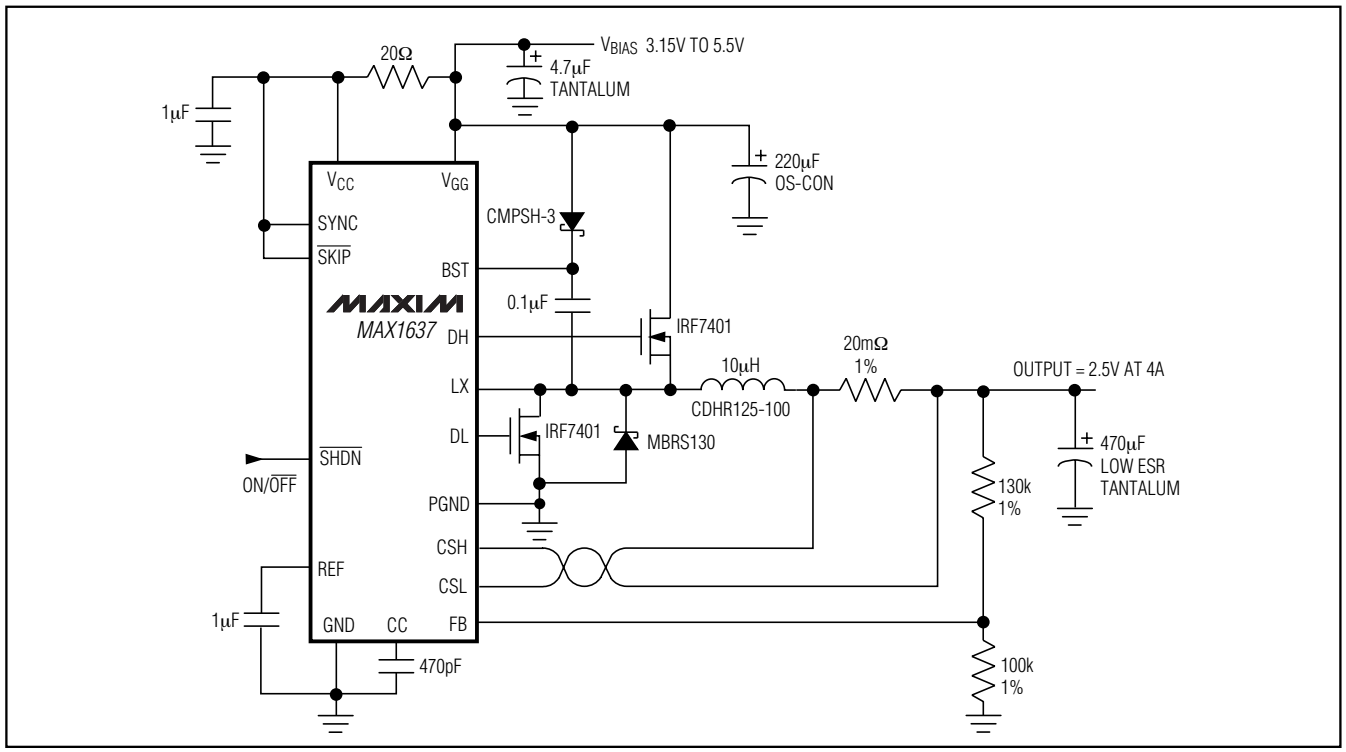


Figure 7. 3.15V to 5.5V Single-Supply Application Circuit

sensing at the supply's output terminals without interference from IR drops and ground noise. Other high-current paths should also be minimized, but focusing primarily on short ground and current-sense connections eliminates about 90% of all PC board layout problems (see the PC board layouts in the MAX1637 evaluation kit manual for examples).

2) Place the IC and signal components. Keep the main switching nodes (LX nodes) away from sensitive analog components (current-sense traces and REF capacitor). Place the IC and analog components on the opposite side of the board from the power-switching node. **Important**: The IC must be no further than 10mm from the current-sense resistors. Keep the gate-drive traces (DH, DL, and BST) shorter than 20mm and route them away from CSH, CSL, and REF. Place ceramic bypass capacitors close to the IC. The bulk capacitors can be placed further away.

3) Use a single-point star ground where the input ground trace, power ground (subground plane), and normal ground plane meet at the supply's output ground terminal. Connect both IC ground pins and all IC bypass capacitors to the normal ground plane.

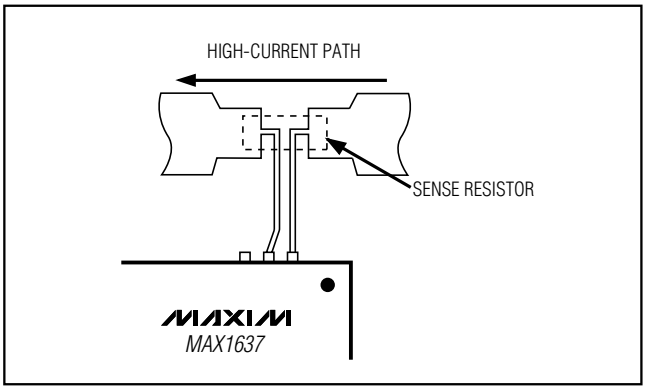


Figure 8. Kelvin Connections for the Current-Sense Resistors

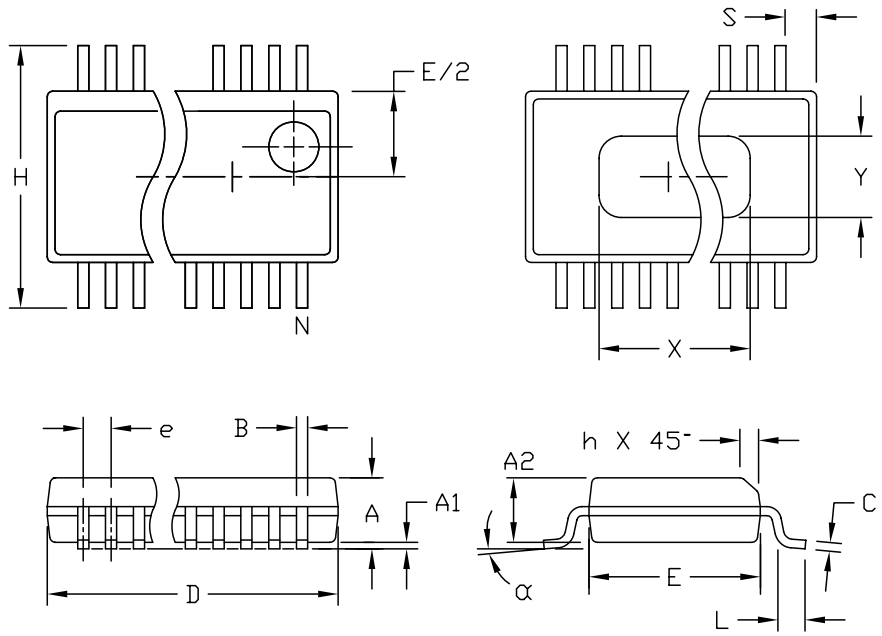
Chip Information

TRANSISTOR COUNT: 2164

Miniature, Low-Voltage, Precision Step-Down Controller

Package Information

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.
5. MEETS JEDEC MO137.

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	C	1/1

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