THE DATASHEET OF

MAX1714BEEE-T

19-1536; Rev 2; 8/05

EVALUATION KIT AVAILABLE

High-Speed Step-Down Controller for Notebook Computers

General Description

The MAX1714 pulse-width modulation (PWM) controller provides the high efficiency, excellent transient response, and high DC output accuracy needed for stepping down high-voltage batteries to generate low-voltage CPU core or chip-set/RAM supplies in notebook computers.

Maxim's proprietary Quick-PWM™ quick-response, constant-on-time PWM control scheme handles wide input/output voltage ratios with ease and provides 100ns "instant-on" response to load transients while maintaining a relatively constant switching frequency.

The MAX1714 achieves high efficiency at a reduced cost by eliminating the current-sense resistor found in traditional current-mode PWMs. Efficiency is further enhanced by an ability to drive very large synchronous-rectifier MOSFETs.

Single-stage buck conversion allows these devices to directly step down high-voltage batteries for the highest possible efficiency. Alternatively, two-stage conversion (stepping down the +5V system supply instead of the battery) at a higher switching frequency allows the minimum possible physical size.

The MAX1714 is intended for CPU core, chipset, DRAM, or other low-voltage supplies as low as 1V. The MAX1714A is available in a 20-pin QSOP package and includes overvoltage protection. The MAX1714B is available in a 16-pin QSOP package with no overvoltage protection. For applications requiring VID compliance or DAC control of output voltage, refer to the MAX1710/MAX1711 data sheet. For a dual output version, refer to the MAX1715† data sheet.

Applications

Notebook Computers

CPU Core Supply

Chipset/RAM Supply as Low as 1V

1.8V and 2.5V I/O Supply

Quick-PWM is a trademark of Maxim Integrated Products.

† Future product—contact factory for availability.

Pin Configurations appear at end of data sheet.

Features

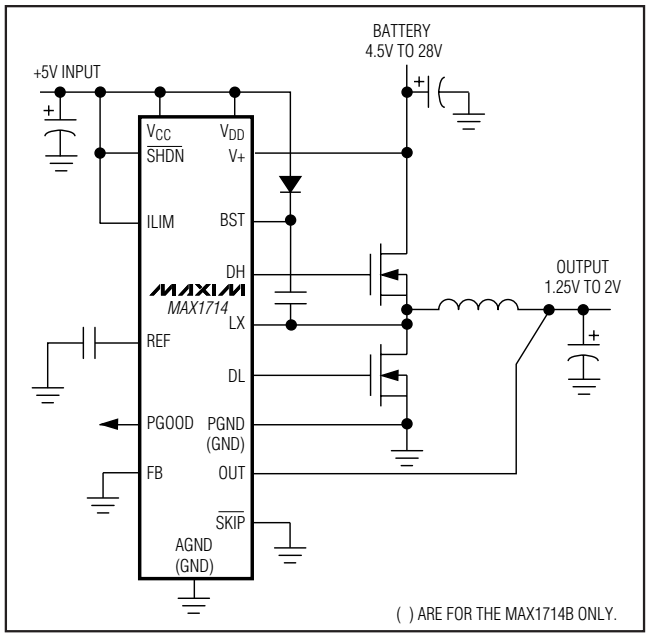
- **Ultra-High Efficiency**
- **No Current-Sense Resistor (Lossless I_{LIMIT})**
- **Quick-PWM with 100ns Load-Step Response**
- **1% V_{OUT} Accuracy Over Line and Load**
- **2.5V/3.3V Fixed or 1V to 5.5V Adjustable Output Range**
- **2V to 28V Battery Input Range**
- **200/300/450/600kHz Switching Frequency**
- **Overvoltage Protection (MAX1714A)**
- **Undervoltage Protection**
- **1.7ms Digital Soft-Start**
- **Drives Large Synchronous-Rectifier FETs**
- **2V ±1% Reference Output**
- **Power-Good Indicator**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1714AEEP	-40°C to +85°C	20 QSOP
MAX1714AEEP+	-40°C to +85°C	20 QSOP
MAX1714BEEE	-40°C to +85°C	16 QSOP
MAX1714BEEE+	-40°C to +85°C	16 QSOP

+Denotes lead-free package.

Minimal Operating Circuit



High-Speed Step-Down Controller for Notebook Computers

ABSOLUTE MAXIMUM RATINGS

V+ to AGND (Note 1).....-0.3V to +30V
V_{DD}, V_{CC} to AGND (Note 1).....-0.3V to +6V
PGND to AGND (Note 1) ..... ±0.3V
$\overline{SHDN}$, PGOOD, OUT to AGND (Note 1).....-0.3V to +6V
ILIM, FB, REF, $\overline{SKIP}$,
TON to AGND (Notes 1, 2).....-0.3V to (V_{CC} + 0.3V)
DL to PGND (Note 1).....-0.3V to (V_{DD} + 0.3V)
BST to AGND (Note 1) .....-0.3V to +36V
DH to LX.....-0.3V to (BST + 0.3V)
LX to BST.....-6V to +0.3V
REF Short Circuit to AGND.....Continuous
Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.3mW/°C above +70°C).....667mW
20-Pin QSOP (derate 9.1mW/°C above +70°C).....727mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: For the MAX1714B, AGND and PGND refer to a single pin designated GND.

Note 2: $\overline{SKIP}$ may be forced below -0.3V, temporarily exceeding the absolute maximum rating, disabling over/undervoltage fault detection for the purpose of debugging prototypes (Figure 6). Limit the current drawn to 5mA maximum.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, 4A components from Table 1, V+ = +15V, V_{CC} = V_{DD} = +5V, $\overline{SKIP}$ = AGND, **T_A = 0°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	Battery voltage, V+		2		28	V
	V_{CC}, V_{DD}		4.5		5.5	
Error Comparator Threshold (DC Output Voltage Accuracy) (Note 3)	V+ = 4.5V to 28V, $\overline{SKIP}$ = V_{CC}	FB = OUT	0.99	1.0	1.01	V
		FB = AGND	2.475	2.5	2.525	
		FB = V_{CC}	3.267	3.3	3.333	
Load Regulation Error	I_{LOAD} = 0 to 3A, $\overline{SKIP}$ = V_{CC}			9		mV
Line Regulation Error	V_{CC} = 4.5V to 5.5V, V+ = 4.5V to 28V			5		mV
FB Input Bias Current			-0.1		0.1	µA
OUT Input Resistance	FB = AGND		100	190	300	kΩ
Soft-Start Ramp Time	Rising edge of $\overline{SHDN}$ to full I_{LIM}			1.7		ms
On-Time	V+ = 24V, V_{OUT} = 2V (Note 4)	TON = AGND (600kHz)	140	160	180	ns
		TON = REF (450kHz)	175	200	225	
		TON = unconnected (300kHz)	260	290	320	
		TON = V_{CC} (200kHz)	380	425	470	
Minimum Off-Time	(Note 4)			400	500	ns
Quiescent Supply Current (V_{CC})	FB forced above the regulation point			550	750	µA
Quiescent Supply Current (V_{DD})	FB forced above the regulation point			<1	5	µA
Quiescent Supply Current (V+)				25	40	µA
Shutdown Supply Current (V_{CC})	V $\overline{SHDN}$ = 0			<1	5	µA
Shutdown Supply Current (V_{DD})	V $\overline{SHDN}$ = 0			<1	5	µA
Shutdown Supply Current (V+)	V $\overline{SHDN}$ = 0 , V+ = 28V, V_{CC} = V_{DD} = 0 or 5V			<1	5	µA
Reference Voltage	V_{CC} = 4.5V to 5.5V, no external REF load		1.98	2	2.02	V
Reference Load Regulation	I_{REF} = 0 to 50µA				0.01	V
REF Sink Current	REF in regulation		10			µA
REF Fault Lockout Voltage	Falling edge, hysteresis = 40mV			1.6		V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, 4A components from Table 1, V+ = +15V, V_{CC} = V_{DD} = +5V, $\overline{SKIP}$ = AGND, **T_A = 0°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Overvoltage Trip Threshold	With respect to error comparator threshold (MAX1714A only)		10.5	12.5	14.5	%
Overvoltage Fault Propagation Delay	FB forced 2% above trip threshold (MAX1714A only)			1.5		µs
Output Undervoltage Protection Threshold	With respect to error comparator threshold		65	70	75	%
Output Undervoltage Protection Blanking Time	From $\overline{SHDN}$ signal going high		10		30	ms
Current-Limit Threshold (Positive Direction, Fixed)	PGND - LX, I_{LIM} = V_{CC}		90	100	110	mV
Current-Limit Threshold (Positive Direction, Adjustable)	PGND - LX	V_{ILIM} = 0.5V	40	50	60	mV
		V_{ILIM} = 2.0V	170	200	230	
Current-Limit Threshold (Negative Direction)	PGND - LX, $\overline{SKIP}$ = V_{CC}, T_A = +25°C, with respect to positive current-limit threshold		-90	-120	-140	%
Current-Limit Threshold (Zero Crossing)	PGND - LX, $\overline{SKIP}$ = AGND			3		mV
PGOOD Propagation Delay	FB forced 2% below PGOOD trip threshold, falling edge			1.5		µs
PGOOD Output Low Voltage	I_{SINK} = 1mA				0.4	V
PGOOD Leakage Current	High state, forced to 5.5V				1	µA
Thermal Shutdown Threshold	Hysteresis = 10°C			150		°C
V_{CC} Undervoltage Lockout Threshold	Rising edge, hysteresis = 20mV, PWM disabled below this level		4.1		4.4	V
DH Gate-Driver On-Resistance	BST - LX forced to 5V			1.5	5	Ω
DL Gate-Driver On-Resistance (Pull-Up)	DL, high state			1.5	5	Ω
DL Gate-Driver On-Resistance (Pull-Down)	DL, low state			0.5	1.7	Ω
DH Gate-Driver Source/Sink Current	DH forced to 2.5V, BST - LX forced to 5V			1		A
DL Gate-Driver Source Current	DL forced to 2.5V			1		A
DL Gate-Driver Sink Current	DL forced to 2.5V			3		A
Dead Time	DL rising			35		ns
	DH rising			26		
$\overline{SKIP}$ Input Current Logic Threshold	To disable overvoltage and undervoltage fault detection, T_A = +25°C		-1.5		-0.1	mA
PGOOD Trip Threshold	Measured at FB with respect to error comparator threshold, falling edge		-8	-6	-4	%
Logic Input High Voltage	$\overline{SHDN}$, $\overline{SKIP}$		2.4			V
Logic Input Low Voltage	$\overline{SHDN}$, $\overline{SKIP}$				0.8	V
Logic Input Current	$\overline{SHDN}$, $\overline{SKIP}$		-1		1	µA
ILIM Input Current	$\overline{SHDN}$, $\overline{SKIP}$			±10		nA

High-Speed Step-Down Controller for Notebook Computers

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, 4A components from Table 1, V+ = +15V, V_{CC} = V_{DD} = +5V, $\overline{SKIP}$ = AGND, **T_A = 0°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TON V_{CC} Level		V_{CC} - 0.4			V
TON Float Voltage		3.15		3.85	V
TON Reference Level		1.65		2.35	V
TON AGND Level				0.5	V
TON Input Current	Forced to AGND or V_{CC}	-3		3	µA

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, 4A components from Table 1, V+ = 15V, V_{CC} = V_{DD} = +5V, $\overline{SKIP}$ = AGND, **T_A = -40°C to +85°C**, unless otherwise noted.) (Notes 1, 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	Battery voltage, V+		2		28	V
	V_{CC}, V_{DD}		4.5		5.5	
Error Comparator Threshold (DC Output Voltage Accuracy) (Note 3)	V+ = 4.5V to 28V, $\overline{SKIP}$ = V_{CC}	FB = OUT	0.985		1.015	V
		FB = AGND	2.462		2.538	
		FB = V_{DD}	3.25		3.35	
On-Time	V+ = 24V, V_{OUT} = 2V (Note 4)	TON = AGND (600kHz)	140		180	ns
		TON = REF (450kHz)	175		225	
		TON = unconnected (300kHz)	260		320	
		TON = V_{CC} (200kHz)	380		470	
Minimum Off-Time	(Note 4)				500	ns
Quiescent Supply Current (V_{CC})	FB forced above the regulation point				750	µA
Reference Voltage	V_{CC} = 4.5V to 5.5V, no external REF load		1.98		2.02	V
Overvoltage Trip Threshold	With respect to error comparator threshold (MAX1714A only)		10		15	%
Output Undervoltage Protection Threshold	With respect to error comparator threshold		65		75	%
Current-Limit Threshold (Positive Direction, Fixed)	PGND - LX, ILIM = V_{CC}		85		115	mV
Current-Limit Threshold (Positive Direction, Adjustable)	PGND - LX	V_{ILIM} = 0.5V	35		65	mV
		V_{ILIM} = 2.0V	160		240	
V_{CC} Undervoltage Lockout Threshold	Rising edge, hysteresis = 20mV, PWM disabled below this level		4.1		4.4	V
Logic Input High Voltage	$\overline{SHDN}$, $\overline{SKIP}$		2.4			V
Logic Input Low Voltage	$\overline{SHDN}$, $\overline{SKIP}$				0.8	V
Logic Input Current	$\overline{SHDN}$, $\overline{SKIP}$		-1		1	µA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, 4A components from Table 1, V+ = +15V, V_{CC} = V_{DD} = +5V, $\overline{SKIP}$ = AGND, **T_A = -40°C to +85°C**, unless otherwise noted.) (Notes 1, 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
PGOOD Trip Threshold	Measured at FB with respect to error comparator threshold, falling edge	-8		-4	%
PGOOD Output Low Voltage	I_{SINK} = 1mA			0.4	V
PGOOD Leakage Current	High state, forced to 5.5V			1	µA

Note 1: For the MAX1714B, AGND and PGND refer to a single pin designated GND.

Note 2: $\overline{SKIP}$ may be forced below -0.3V, temporarily exceeding the absolute maximum rating, disabling over/undervoltage fault detection for the purpose of debugging prototypes (Figure 6). Limit the current drawn to 5mA maximum.

Note 3: When the inductor is in continuous conduction, the output voltage will have a DC regulation level higher than the error-comparator threshold by 50% of the ripple. In discontinuous conduction ($\overline{SKIP}$ = AGND, light-loaded), the output voltage will have a DC regulation level higher than the trip level by approximately 1.5% due to slope compensation.

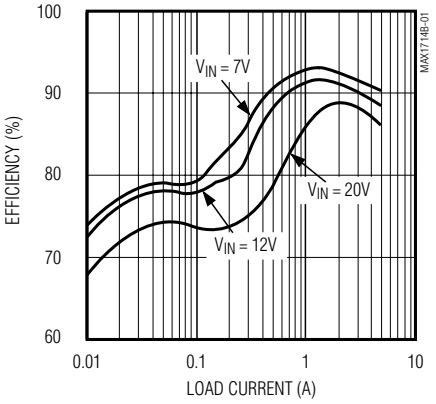
Note 4: On-time and off-time specifications are measured from 50% point to 50% point at the DH pin with LX = PGND, V_{BST} = 5V, and a 250pF capacitor connected from DH to LX. Actual in-circuit times may differ due to MOSFET switching speeds.

Note 5: Specifications to -40°C are guaranteed by design, not production tested.

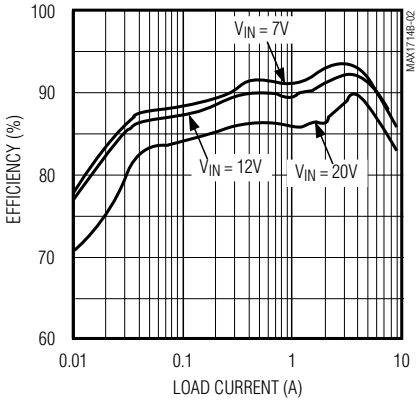
Typical Operating Characteristics

(Circuit of Figure 1, components from Table 1, V_{IN} = +15V, $\overline{SKIP}$ = AGND, TON = unconnected, T_A = +25°C, unless otherwise noted.)

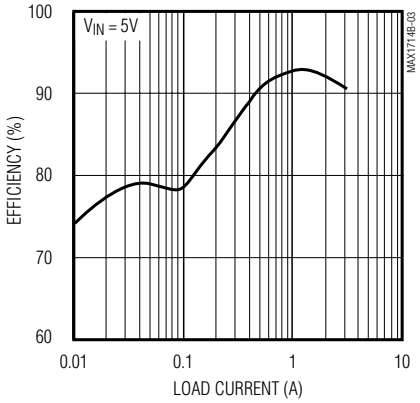
EFFICIENCY vs. LOAD CURRENT (4A COMPONENTS, V_{OUT} = 2.5V, 300kHz)



EFFICIENCY vs. LOAD CURRENT (8A COMPONENTS, V_{OUT} = 1.6V, 300kHz)



EFFICIENCY vs. LOAD CURRENT (1.5A COMPONENTS, V_{OUT} = 2.5V, TON = GND, 600kHz)

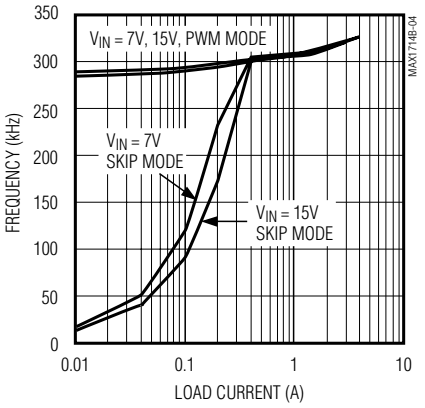


High-Speed Step-Down Controller for Notebook Computers

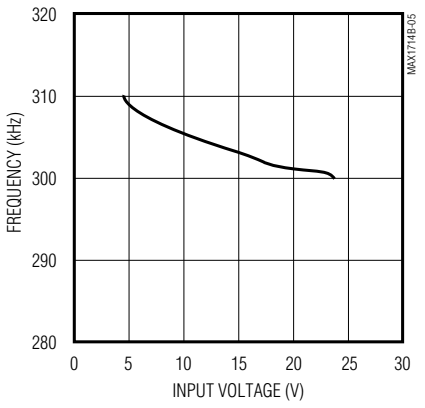
Typical Operating Characteristics (continued)

(Circuit of Figure 1, components from Table 1, V_{IN} = +15V, $\overline{SKIP}$ = AGND, TON = unconnected, T_A = +25°C, unless otherwise noted.)

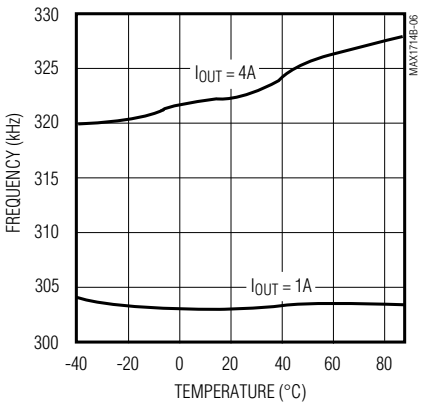
FREQUENCY vs. LOAD CURRENT (4A COMPONENTS, V_{OUT} = 2.5V)



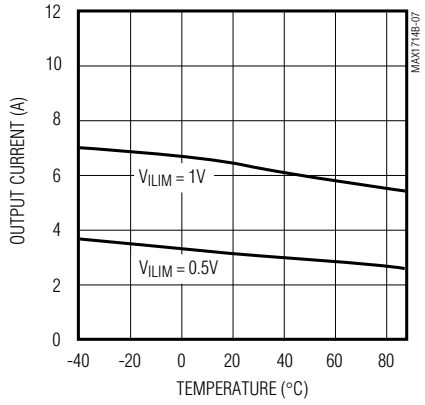
FREQUENCY vs. INPUT VOLTAGE (4A COMPONENTS, V_{OUT} = 2.5V, I_{OUT} = 1A)



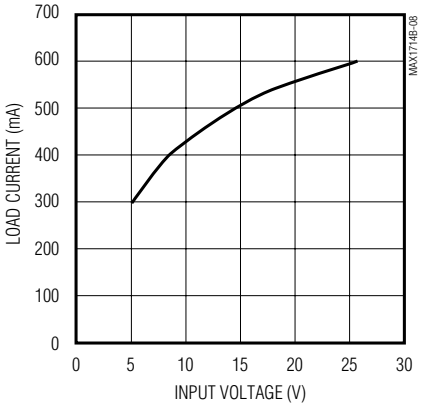
FREQUENCY vs. TEMPERATURE (4A COMPONENTS, V_{OUT} = 2.5V)



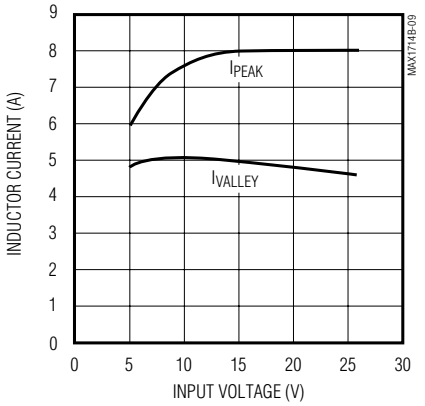
I_{OUT} AT CURRENT LIMIT vs. TEMPERATURE (4A COMPONENTS, V_{OUT} = 2.5V)



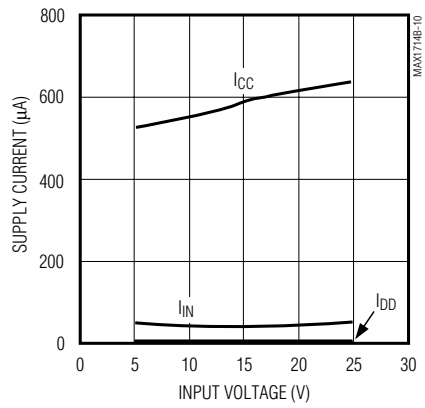
CONTINUOUS TO DISCONTINUOUS INDUCTOR CURRENT POINT vs. INPUT VOLTAGE (4A COMPONENTS, V_{OUT} = 2.5V)



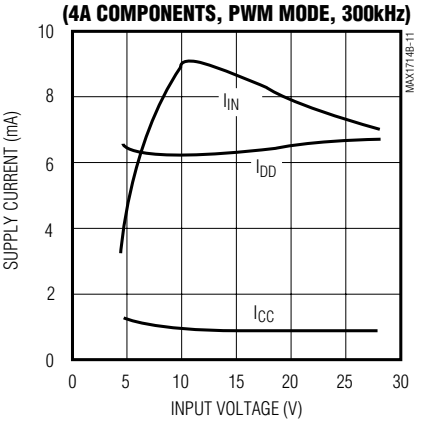
INDUCTOR CURRENT PEAKS AND VALLEYS vs. INPUT VOLTAGE (4A COMPONENTS, AT CURRENT-LIMIT TRIP POINT)



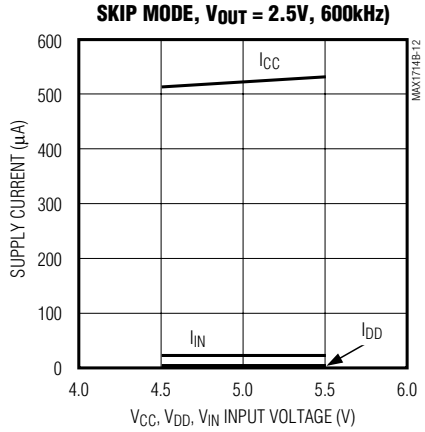
NO-LOAD SUPPLY CURRENT (4A COMPONENTS, SKIP MODE, 300kHz)



NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (4A COMPONENTS, PWM MODE, 300kHz)



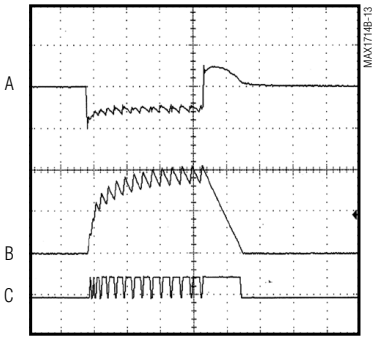
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (1.5A COMPONENTS, SKIP MODE, V_{OUT} = 2.5V, 600kHz)



Typical Operating Characteristics (continued)

(Circuit of Figure 1, components from Table 1, V_{IN} = +15V, $\overline{SKIP}$ = AGND, TON = unconnected, T_A = +25°C, unless otherwise noted.)

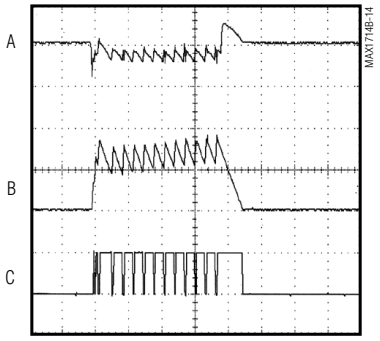
LOAD-TRANSIENT RESPONSE (4A COMPONENTS, V_{OUT} = 2.5V, 300kHz)



10µs/div

A = V_{OUT}, AC-COUPLED, 100mV/div
B = INDUCTOR CURRENT, 2A/div
C = DL, 10V/div

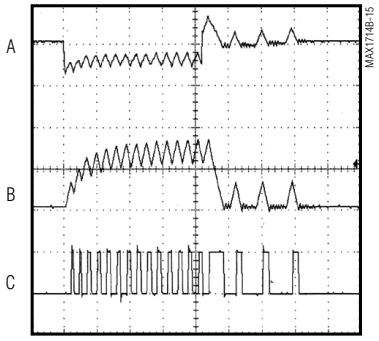
LOAD-TRANSIENT RESPONSE (8A COMPONENTS, V_{OUT} = 1.6V, 300kHz)



10µs/div

A = V_{OUT}, AC-COUPLED, 100mV/div
B = INDUCTOR CURRENT, 5A/div
C = DL, 5V/div

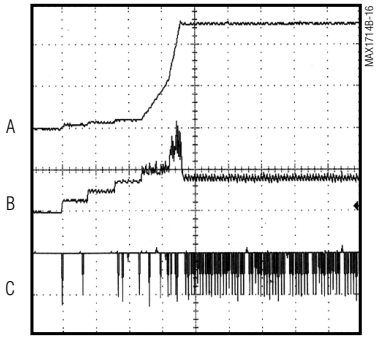
LOAD-TRANSIENT RESPONSE (1.5A COMPONENTS, V_{IN} = 5V, V_{OUT} = 2.5V, 600kHz)



5µs/div

A = V_{OUT}, AC-COUPLED, 100mV/div
B = INDUCTOR CURRENT, 1A/div
C = DL, 5V/div

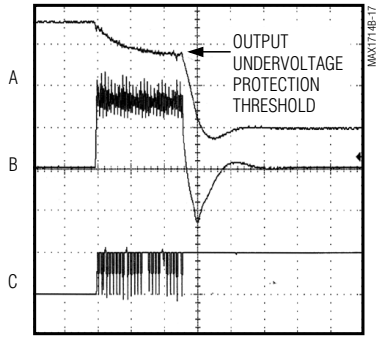
START-UP WAVEFORM (4A COMPONENTS, I_{OUT} = 4A, ACTIVE LOAD, V_{OUT} = 2.5V, 300kHz)



500µs/div

A = V_{OUT}, 1V/div
B = INDUCTOR CURRENT, 5A/div
C = DL, 5V/div

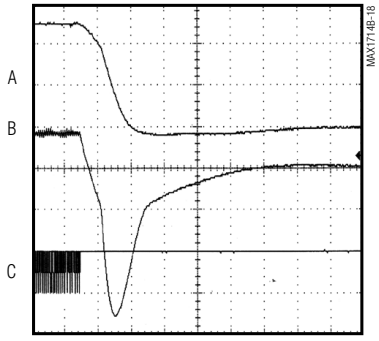
OUTPUT OVERLOAD WAVEFORM (4A COMPONENTS, V_{OUT} = 2.5V, 300kHz)



200µs/div

A = V_{OUT}, 1V/div
B = INDUCTOR CURRENT, 5A/div
C = DL, 5V/div

SHUTDOWN WAVEFORM (4A COMPONENTS, V_{OUT} = 2.5V, 300kHz)



50µs/div

A = V_{OUT}, 1V/div
B = INDUCTOR CURRENT, 5A/div
C = DL, 5V/div

High-Speed Step-Down Controller for Notebook Computers

Pin Description

PIN		NAME	FUNCTION
MAX1714A	MAX1714B		
1	1	DH	High-Side Gate Driver Output. Swings from LX to BST.
2, 9, 11	–	N.C.	No Connection. These pins are not connected to any internal circuitry. Connect N.C. pins to the ground plane to enhance thermal conductivity.
3	2	$\overline{SHDN}$	Shutdown Control Input. Drive $\overline{SHDN}$ to AGND to force the MAX1714 into shutdown. Drive or connect to V_{CC} for normal operation. A rising edge on $\overline{SHDN}$ clears the fault latch.
4	3	FB	Feedback Input. Connect to AGND for a +2.5V fixed output or to V_{CC} for a +3.3V fixed output, or connect FB to a resistor divider from OUT for an adjustable output.
5	4	OUT	Output Voltage Connection. Connect directly to the junction of the external and output filter capacitors. OUT senses the output voltage to determine the on-time and also serves as the feedback input in fixed-output modes.
6	5	ILIM	Current-Limit Threshold Adjustment. Connect ILIM to V_{CC} for 100mV current-limit threshold. For an adjustable threshold, connect an external voltage source to ILIM, or use a two-resistor divider from REF to AGND. The external adjustment range of 0.5V to 2.0V corresponds to a current-limit threshold of 50mV to 200mV.
7	6	REF	+2.0V Reference Voltage Output. Bypass to AGND with 0.22µF (minimum) capacitor. Can supply 50µA for external loads.
8	–	AGND	Analog Ground.
10	7	PGOOD	Power-Good Open-Drain Output. PGOOD is low when the output voltage is more than 6% below the normal regulation point or during soft-start. PGOOD is high impedance when the output is in regulation and the soft-start circuit has terminated.
–	8	GND	Analog and Power Ground. AGND and PGND connect together internally.
12	–	PGND	Power Ground. Connect directly to the low-side MOSFET's source. Serves as the negative input of the current-limit comparator.
13	9	DL	Low-Side Gate-Driver Output. Swings from PGND to V_{DD}.
14	10	V_{DD}	Supply Input for the DL Gate Drive. Connect to the system supply voltage, +4.5V to +5.5V. Bypass to PGND with a 1µF (min) ceramic capacitor.
15	11	V_{CC}	Analog-Supply Input. Connect to the system supply voltage, +4.5V to +5.5V, with a series 20Ω resistor. Bypass to AGND with a 1µF (min) ceramic capacitor.
16	12	TON	On-Time Selection-Control Input. This is a four-level input used to determine DH on-time. Connect to AGND, REF, or V_{CC}, or leave TON unconnected to set the following switching frequencies: AGND = 600kHz, REF = 450kHz, floating = 300kHz, and V_{CC} = 200kHz.
17	13	V+	Battery Voltage Sense Connection. Connect to input power source. V+ is used only to set the PWM one-shot timing.
18	14	$\overline{SKIP}$	Pulse-Skipping Control Input. Connect to V_{CC} for low-noise forced-PWM mode. Connect to AGND to enable pulse-skipping operation.
19	15	BST	Boost Flying-Capacitor Connection. Connect to an external capacitor and diode according to the Standard Application Circuit (Figure 1). See *MOSFET Gate Drivers (DH, DL)* section.
20	16	LX	External Inductor Connection. Connect LX to the switched side of the inductor. LX serves as the lower supply rail for the DH high-side gate driver. LX is also the positive input to the current-limit comparator.

Standard Application Circuit

The standard application circuit (Figure 1) generates a low-voltage rail for general-purpose use in a notebook computer (I/O supply, fixed CPU core supply, DRAM supply). This DC-DC converter steps down a battery or AC adapter voltage to voltages from 1.0V to 5.5V with high efficiency and accuracy.

See Table 1 for a list of component selections for common applications. Table 2 lists component manufacturers.

Detailed Description

The MAX1714 buck controller is targeted for low-voltage power supplies for notebook computers. Maxim's proprietary Quick-PWM pulse-width modulator in the MAX1714 is specifically designed for handling fast load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The Quick-PWM architecture circumvents the poor load-transient timing problems of fixed-frequency current-mode PWMs while also avoiding the problems caused by widely varying switching frequencies in conventional constant-on-time and constant-off-time PWM schemes.

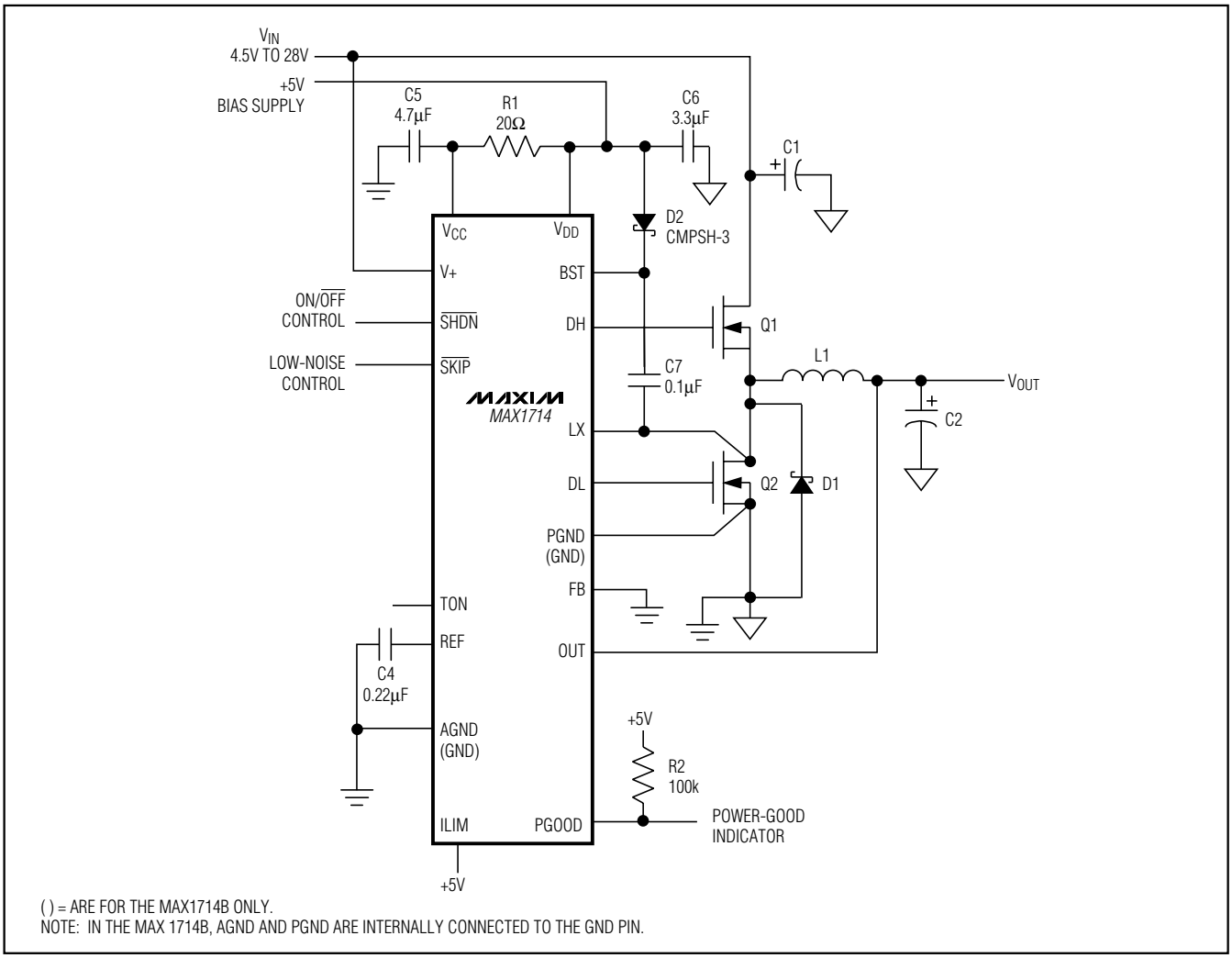


Figure 1. Standard Application Circuit

High-Speed Step-Down Controller for Notebook Computers

Table 1. Component Selection for Standard Applications

COMPONENT	2.5V AT 4A	1.6V AT 8A	2.5V AT 1.5A
Input Range	7V to 20V	7V to 20V	4.5V to 5.5V
Frequency	300kHz	300kHz	600kHz
Q1 High-Side MOSFET	Fairchild Semiconductor 1/2 FDS6982A	International Rectifier IRF7811	International Rectifier 1/2 IRF7301
Q2 Low-Side MOSFET	Fairchild Semiconductor 1/2 FDS6982A	Fairchild Semiconductor FDS6670A	International Rectifier 1/2 IRF7301
D2 Rectifier	Nihon EP10QY03	Motorola MBRS340T3	Motorola MBR0520LT1
L1 Inductor	6.8µH Coilcraft DO3316P-682	1.5µH Sumida CEP1251R5MC	3.3µH Coiltronics UP1B-3R3
C1 Input Capacitor	10µF, 25V Taiyo Yuden TMK432BJ106KM	(2) 10µF, 25V Taiyo Yuden TMK432BJ106KM	100µF, 10V Sanyo POSCAP 10TPA100M
C2 Output Capacitor	470µF, 6V Kemet T510X477108M006AS	(2) 470µF 6V Kemet T510X477108M006AS	100µF, 10V Sanyo POSCAP 10TPA100M

Table 2. Component Suppliers

MANUFACTURER	USA PHONE	FACTORY FAX [Country Code]
AVX	803-946-0690	[1] 803-626-3123
Central Semiconductor	516-435-1110	[1] 516-435-1824
Coilcraft	847-639-6400	[1] 847-639-1469
Coiltronics	561-241-7876	[1] 561-241-9339
Fairchild	408-822-2181	[1] 408-721-1635
International Rectifier	310-322-3331	[1] 310-322-3332
Kemet	408-986-0424	[1] 408-986-1442
Matsuo	714-969-2491	[1] 714-960-6492
Motorola	602-303-5454	[1] 602-994-6430
Murata	814-237-1431 800-831-9172	[1] 814-238-0490
NIEC (Nihon)	805-867-2555*	[81] 3-3494-7414
Sanyo	619-661-6835	[81] 7-2070-1174
Siliconix	408-988-8000 800-554-5565	[1] 408-970-3950
Sprague	603-224-1961	[1] 603-224-1430
Sumida	847-956-0666	[81] 3-3607-5144
Taiyo Yuden	408-573-4150	[1] 408-573-4159
TDK	847-390-4461	[1] 847-390-4405

**Distributor*

+5V Bias Supply (V_{CC} and V_{DD})

The MAX1714 requires an external +5V bias supply in addition to the battery. Typically, this +5V bias supply is the notebook's 95% efficient +5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the +5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If stand-alone capability is needed, the +5V supply can be generated with an external linear regulator such as the MAX1615.

The battery and +5V bias inputs can be tied together if the input source is a fixed +4.5V to +5.5V supply. If the +5V bias supply is powered up prior to the battery supply, the enable signal ($\overline{SHDN}$) must be delayed until the battery voltage is present in order to ensure startup. The +5V bias supply must provide V_{CC} and gate-drive power, so the maximum current drawn is:

$$I_{BIAS} = I_{CC} + f (Q_{G1} + Q_{G2}) = 5mA \text{ to } 30mA \text{ (typ)}$$

where I_{CC} is 600µA typical, f is the switching frequency, and Q_{G1} and Q_{G2} are the MOSFET data sheet total gate-charge specification limits at V_{GS} = 5V.

Free-Running, Constant-On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant-on-time current-mode type with voltage feed-forward (Figure 2). This architecture relies on the output filter capacitor's ESR to act as the current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose period is inversely proportional to input voltage and directly proportional to output voltage. Another one-shot sets a minimum off-time (400ns typical). The on-time one-shot is triggered if the error comparator is low, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

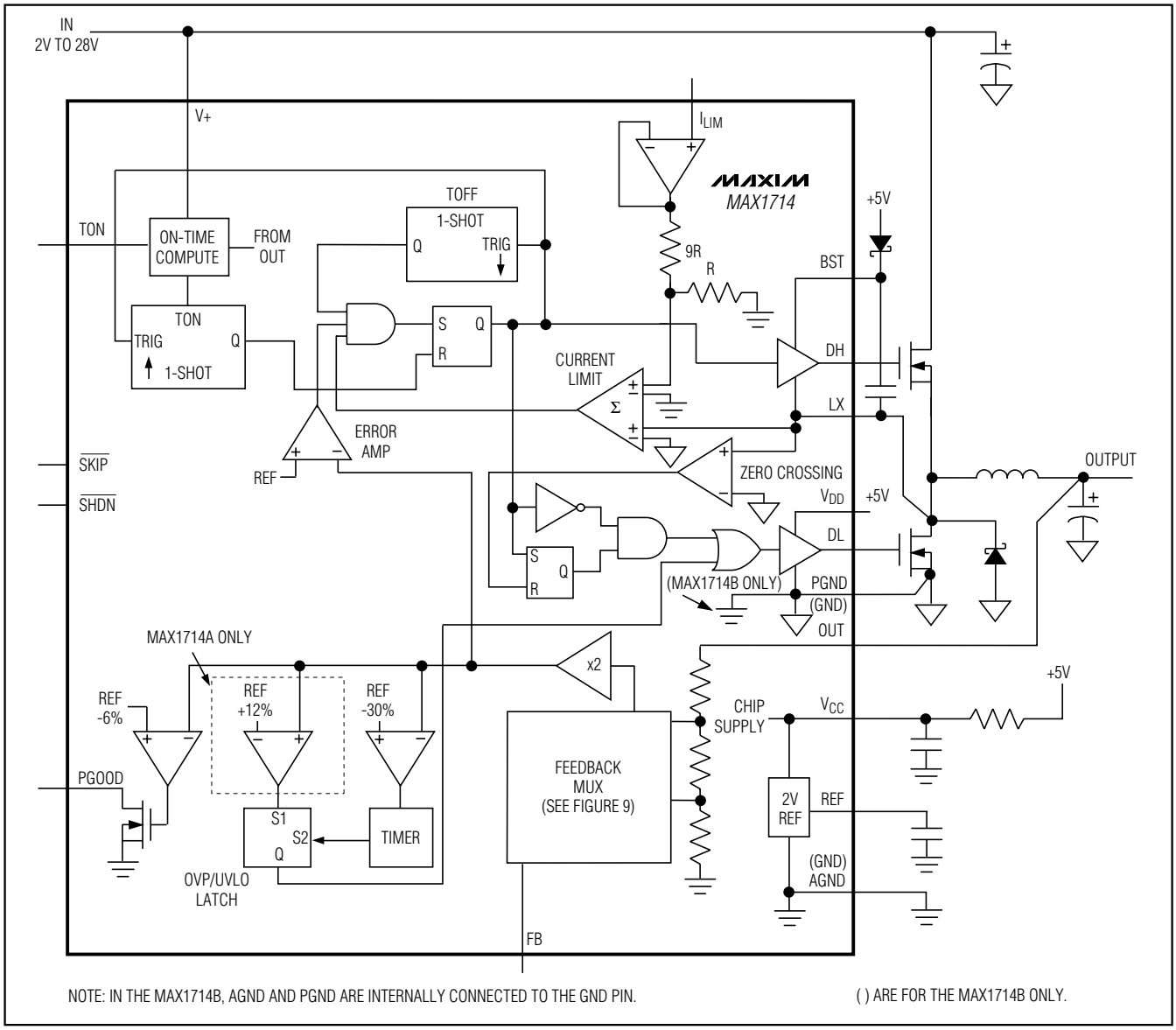


Figure 2. MAX1714 Functional Diagram

On-Time One-Shot (TON)

The heart of the PWM core is the one-shot that sets the high-side switch on-time. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to battery and output voltage. The high-side switch on-time is inversely proportional to the battery voltage as measured by the V+ input, and proportional to the output voltage. This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator. The benefits of a constant switching frequency are twofold: first, the frequency can be selected to avoid noise-sensitive regions such as the 455kHz IF band; second, the inductor ripple-current operating point remains relatively constant, resulting in easy design methodology and predictable output voltage ripple.

$$\text{On-Time} = K (V_{OUT} + 0.075V) / V_{IN}$$

High-Speed Step-Down Controller for Notebook Computers

where K is set by the TON pin-strap connection and 0.075V is an approximation to accommodate for the expected drop across the low-side MOSFET switch. One-shot timing error increases for the shorter on-time settings due to fixed propagation delays; it is approximately ±12.5% at 600kHz and 450kHz, and ±10% at the two slower settings. This translates to reduced switching-frequency accuracy at higher frequencies (Table 5). Switching frequency increases as a function of load current due to the increasing drop across the low-side MOSFET, which causes a faster inductor-current discharge ramp. The on-times guaranteed in the *Electrical Characteristics* are influenced by switching delays in the external high-side power MOSFET.

Two external factors that influence switching-frequency accuracy are resistive drops in the two conduction loops (including inductor and PC board resistance) and the dead-time effect. These effects are the largest contributors to the change of frequency with changing load current. The dead-time effect increases the effective on-time, reducing the switching frequency as one or both dead times are added to the effective on-time. It occurs only in PWM mode ($\overline{SKIP}$ = high) when the inductor current reverses at light or negative load currents. With reversed inductor current, the inductor's EMF causes LX to go high earlier than normal, extending the on-time by a period equal to the low-to-high dead time.

For loads above the critical conduction point, the actual switching frequency is:

$$f = \frac{V_{OUT} + V_{DROP1}}{t_{ON}(V_{IN} + V_{DROP2})}$$

where V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PC board resistances; V_{DROP2} is the sum of the resistances in the charging path, and t_{ON} is the on-time calculated by the MAX1714.

Automatic Pulse-Skipping Switchover

In skip mode ($\overline{SKIP}$ low), an inherent automatic switchover to PFM takes place at light loads. This switchover is effected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the "critical conduction" point; see the Continuous to Discontinuous Inductor Current Point vs. Input Voltage graph in the *Typical Operating Characteristics*). In low-duty-cycle applications, this threshold is relatively constant, with only a minor dependence on battery voltage.

$$I_{LOAD(SKIP)} \approx \frac{KV_{OUT}}{2L} \cdot \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

where K is the on-time scale factor (Table 5). The load-current level at which PFM/PWM crossover occurs, $I_{LOAD(\overline{SKIP})}$, is equal to 1/2 the peak-to-peak ripple current, which is a function of the inductor value (Figure 3). For example, in the standard application circuit with K = 3.3µs (Table 5), V_{OUT} = 2.5V, V_{IN} = 15V, and L = 6.8µH, switchover to pulse-skipping operation occurs at I_{LOAD} = 0.51A or about 1/8 full load. The crossover point occurs at an even lower value if a swinging (soft-saturation) inductor is used.

The switching waveforms may appear noisy and asynchronous when light loading causes pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in PFM noise vs. light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response (especially at low input voltage levels).

DC output accuracy specifications refer to the error-comparator threshold of the error comparator. When the inductor is in continuous conduction, the output voltage will have a DC regulation level higher than the trip level by 50% of the ripple. In discontinuous conduction ($\overline{SKIP}$ = AGND, light-loaded), the output voltage will have a DC regulation level higher than the error-comparator threshold by approximately 1.5% due to slope compensation.

Forced-PWM Mode ($\overline{SKIP}$ = High)

The low-noise forced-PWM mode ($\overline{SKIP}$ = high) disables the zero-crossing comparator, which controls the low-side switch on-time. This causes the low-side gate-drive waveform to become the complement of the high-side gate-drive waveform. This in turn causes the inductor current to reverse at light loads while DH maintains a duty factor of V_{OUT}/V_{IN}. The benefit of forced-PWM mode is to keep the switching frequency fairly constant, but it comes at a cost: the no-load battery current can be 10mA to 40mA, depending on the external MOSFETs.

Forced-PWM mode is most useful for reducing audio-frequency noise, improving load-transient response, providing sink-current capability for dynamic output voltage adjustment, and improving the cross-regulation of

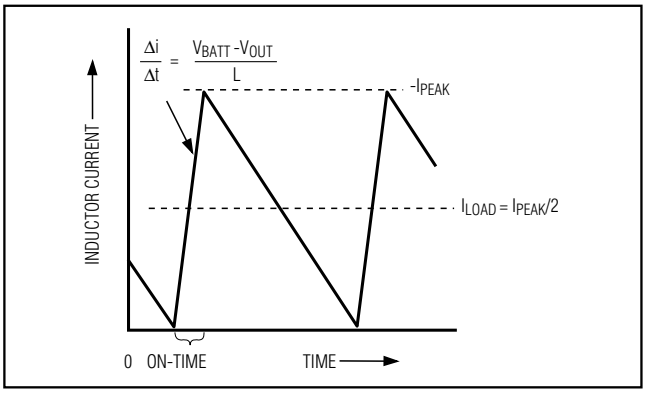


Figure 3. Pulse-Skipping/Discontinuous Crossover Point

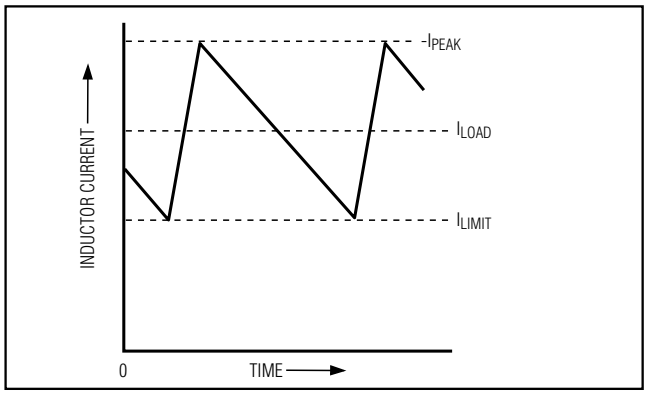


Figure 4. "Valley" Current-Limit Threshold Point

multiple-output applications that use a flyback transformer or coupled inductor.

Current-Limit Circuit (ILIM)

The current-limit circuit employs a unique "valley" current-sensing algorithm that uses the on-state resistance of the low-side MOSFET as a current-sensing element (Figure 4). If the current-sense voltage (PGND - LX) is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the MOSFET on-resistance, inductor value, and battery voltage. The reward for this uncertainty is robust, lossless overcurrent sensing. When combined with the UVP protection circuit, this current-limit method is effective in almost every circumstance.

There is also a negative current limit that prevents excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is set to approximately 120% of the positive current limit, and therefore tracks the positive current limit when ILIM is adjusted.

The current-limit threshold is adjusted with an external resistor-divider at ILIM. A 1µA min divider current is recommended. The current-limit threshold adjustment range is from 50mV to 200mV. In the adjustable mode, the current-limit threshold voltage is precisely 1/10 the voltage seen at ILIM. The threshold defaults to 100mV when ILIM is connected to V_{CC}. The logic threshold for switchover to the 100mV default value is approximately V_{CC} - 1V.

The adjustable current limit accommodates MOSFETs with a wide range of on-resistance characteristics (see *Design Procedure*).

Carefully observe the PC board layout guidelines to ensure that noise and DC errors don't corrupt the current-sense signals seen by LX and PGND. Mount or place the IC close to the low-side MOSFET with short, direct traces, making a Kelvin sense connection to the source and drain terminals.

MOSFET Gate Drivers (DH, DL)

The DH and DL drivers are optimized for driving moderate-sized high-side, and larger low-side power MOSFETs. This is consistent with the low duty factor seen in the notebook environment, where a large V_{BATT} - V_{OUT} differential exists. An adaptive dead-time circuit monitors the DL output and prevents the high-side FET from turning on until DL is fully off. There must be a low-resistance, low-inductance path from the DL driver to the MOSFET gate for the adaptive dead-time circuit to work properly; otherwise, the sense circuitry in the MAX1714 will interpret the MOSFET gate as "off" while there is actually still charge left on the gate. Use very short, wide traces measuring no more than 20 squares (50 to 100 mils wide if the MOSFET is 1 inch from the MAX1714).

The dead time at the other edge (DH turning off) is determined by a fixed 35ns (typical) internal delay.

The internal pull-down transistor that drives DL low is robust, with a 0.5Ω typical on-resistance. This helps prevent DL from being pulled up during the fast rise-time of the inductor node, due to capacitive coupling from the drain to the gate of the low-side synchronous-rectifier MOSFET. However, for high-current applications, you might still encounter some combinations of high- and low-side FETs that will cause excessive gate-drain coupling, which can lead to efficiency-killing, EMI-producing shoot-through currents. This is often remedied by adding a resistor in series with BST, which increases the turn-on time of the high-side FET without degrading the turn-off time (Figure 5).

High-Speed Step-Down Controller for Notebook Computers

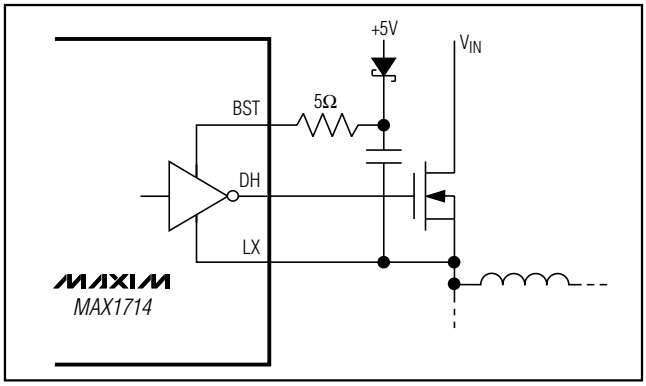


Figure 5. Reducing the Switching-Node Rise Time

POR, UVLO, and Soft-Start

Power-on reset (POR) occurs when V_{CC} rises above approximately 2V, resetting the fault latch and soft-start counter, and preparing the PWM for operation. V_{CC} undervoltage lockout (UVLO) circuitry inhibits switching and forces the DL gate driver high (to enforce output overvoltage protection) until V_{CC} rises above 4.2V, whereupon an internal digital soft-start timer begins to ramp up the maximum allowed current limit. The ramp occurs in five steps: 20%, 40%, 60%, 80%, and 100%; 100% current is available after 1.7ms ±50%.

A continuously adjustable analog soft-start function can be realized by adding a capacitor in parallel with the ILIM resistor. This soft-start method requires a minimum interval between power-down and power-up to discharge the capacitor.

Power-Good Output (PGOOD)

The output voltage is continuously monitored for undervoltage by the PGOOD comparator. In shutdown, standby, and soft-start, PGOOD is actively held low. After digital soft-start has terminated, PGOOD is released if the digital output is within 6% of the error-comparator threshold. The PGOOD output is a true open-drain type with no parasitic ESD diodes. Note that the PGOOD undervoltage detector is completely independent of the output UVP fault detector.

Output Overvoltage Protection

The overvoltage protection (OVP) circuit is available in the MAX1714A only, and is designed to protect against a shorted high-side MOSFET by drawing high current and blowing the battery fuse. The output voltage is continuously monitored for overvoltage. If the output is more than 12.5% above the trip level of the error amplifier, overvoltage protection (OVP) is triggered and the circuit shuts down. The DL low-side gate-driver output is then latched high until $\overline{SHDN}$ is toggled or V_{CC} power is cycled below 1V. This action turns on the synchronous-rectifier MOSFET with 100% duty and, in turn, rapidly discharges the output filter capacitor and forces the output to ground. If the condition that caused the overvoltage (such as a shorted high-side MOSFET) persists, the battery fuse will blow. DL is also kept high continuously when V_{CC} UVLO is active, as well as in shutdown mode (Table 3).

Note that DL latching high causes the output voltage to go slightly negative, due to energy stored in the output LC tank circuit when OVP activates. If the load can't tolerate being forced to a negative voltage, it may be desirable to place a power Schottky diode across the output to act as a reverse-polarity clamp.

Overvoltage protection can be defeated using the no-fault test mode (see *No-Fault Test Mode* section).

Output Undervoltage Protection

The output undervoltage protection (OVP) function is similar to foldback current limiting, but employs a timer rather than a variable current limit. If the MAX1714 output voltage is under 70% of the nominal value 20ms after coming out of shutdown, the PWM is latched off and won't restart until V_{CC} power is cycled or $\overline{SHDN}$ is toggled. Under- voltage protection can be defeated using the no-fault test mode.

No-Fault Test Mode

The over/undervoltage protection features can complicate the process of debugging prototype breadboards, since there are (at most) a few milliseconds in which to determine what went wrong. Therefore, a test mode is provided to totally disable the OVP, UVP, and thermal shutdown features, and clear the fault latch if it has been set. The PWM operates as if $\overline{SKIP}$ were grounded (PFM/PWM mode).

The no-fault test mode is entered by sinking 1.5mA from $\overline{SKIP}$ through an external negative voltage source in series with a resistor (Figure 6). $\overline{SKIP}$ is clamped to AGND with a silicon diode, so choose a resistor value of approximately (V_{FORCE} - 0.65V) / 1.5mA.

Design Procedure

Component selection for the MAX1714 is primarily dictated by the following four criteria:

1) **Input voltage range**. The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case high AC adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest battery voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.

Table 3. Operating Mode Truth Table

$\overline{SHDN}$	$\overline{SKIP}$	DL	MODE	COMMENTS
0	X	High	Shutdown	Low-power shutdown state. DL is forced to V_{DD}, enforcing OVP. I_{CC} < 1µA typ.
1	Below AGND	Switching	No Fault	Test mode with OVP, UVP, and thermal faults disabled and latches cleared. Otherwise normal operation, with automatic PWM/PFM switchover for pulse skipping at light loads (Figure 6).
1	V_{CC}	Switching	Run (PWM), Low Noise	Low-noise operation with no automatic switchover. Fixed-frequency PWM action is forced regardless of load. Inductor current reverses at light load levels. Low noise, high I_Q.
1	AGND	Switching	Run (PFM/PWM)	Normal operation with automatic PWM/PFM switchover for pulse skipping at light loads. Best light-load efficiency.
1	X	High	Fault	Fault latch has been set by OVP, output UVLO, or thermal shutdown. Device will remain in FAULT mode until V_{CC} power is cycled, $\overline{SKIP}$ is forced below ground (Figure 6), or $\overline{SHDN}$ is toggled.

2) **Maximum load current**. There are two values to consider. The *peak load current* ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements, and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The *continuous load current* (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components. Modern notebook CPUs generally exhibit:

$$I_{LOAD} = I_{LOAD(MAX)} \cdot 80\%$$

3) **Switching frequency**. This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses that are proportional to frequency and V_{IN}^2. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical (Table 4).

4) **Inductor operating point**. This choice provides trade-offs between size vs. efficiency. Low inductor values cause large ripple currents, resulting in the smallest size, but poor efficiency and high output ripple. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit.

   The MAX1714's pulse-skipping algorithm initiates skip mode at the critical conduction point. So, the inductor operating point also determines the load-current value at which PFM/PWM switchover occurs.

These four factors impact the component selection process. Selecting components and calculating their effect on the MAX1714's operation is best done with a spreadsheet. Using the formulas provided, calculate the LIR (the ratio of the inductor ripple current to the designed maximum load current) for both the minimum and maximum input voltages. Maintaining an LIR within a 20% to 50% range is prudent. The use of a spreadsheet allows quick evaluation of component selection.

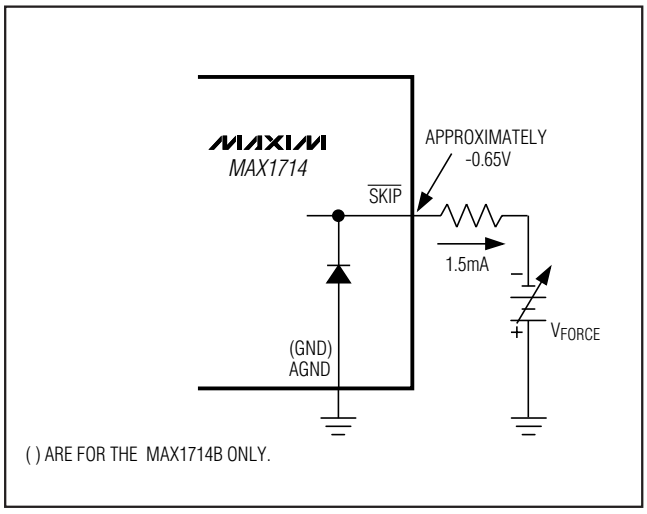


Figure 6. Disabling Over/Undervoltage Protection (No-Fault Test Mode)

High-Speed Step-Down Controller for Notebook Computers

Inductor Selection

The switching frequency and inductor operating point determine the inductor value as follows:

$$L = \frac{V_{OUT}\,(V_{IN} - V_{OUT})}{V_{IN} \cdot f \cdot LIR \cdot I_{LOAD(MAX)}}$$

Example: $I_{LOAD(MAX)}$ = 8A, V_{IN} = 7V, V_{OUT} = 1.5V, f = 300kHz, 33% ripple current or LIR = 0.33.

$$L = \frac{1.5V\,(7V - 1.5V)}{7V \cdot 300kHz \cdot 0.33 \cdot 8A} = 1.49\mu H$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}).

$$I_{PEAK} = I_{LOAD(MAX)} + [(LIR / 2) \cdot I_{LOAD(MAX)}]$$

Most inductor manufacturers provide inductors in standard values, such as 1.0µH, 1.5µH, 2.2µH, 3.3µH, etc. Also look for nonstandard values, which can provide a better compromise in LIR across the input voltage range. For example, Sumida offers 3.1µH and 4.4µH in their CDRH125 series. If using a swinging inductor (where the no-load inductance decreases linearly with increasing current), evaluate the LIR with properly scaled inductance values.

Transient Response

The inductor ripple current also impacts transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step.

Table 4. Frequency Selection Guidelines

FREQUENCY (kHz)	TYPICAL APPLICATION	COMMENTS
200 TON = V_{CC}	4-cell Li+ notebook	Use for absolute best efficiency.
300 TON = Float	4-cell Li+ notebook	Considered mainstream by current standards.
450 TON = REF	3-cell Li+ notebook	Useful in 3-cell systems for lighter loads than the CPU core or where size is key.
600 TON = AGND	+5V input	Good operating point for compound buck designs or desktop circuits.

The amount of output sag is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time:

$$V_{SAG} = \frac{(\Delta I_{LOAD(MAX)})^2 \cdot L}{2 \cdot C_F \cdot DUTY\,(V_{IN(MIN)} - V_{OUT})}$$

where

$$DUTY = \frac{K\,(V_{OUT} + 0.075V)\,V_{IN}}{K\,(V_{OUT} + 0.075V)\,V_{OUT} + \text{min off-time}}$$

and minimum off-time = 400ns typ (see Table 5 for K values).

The amount of overshoot during a full-load to no-load transient due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{L \cdot I_{PEAK}^2}{2C_{OUT}V_{OUT}}$$

where I_{PEAK} is the peak inductor current.

Setting the Current Limit

The minimum current-limit threshold must be high enough to support the maximum load current. The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half of the ripple current (Figure 4); therefore:

$$I_{LIMIT(LOW)} > I_{LOAD(MAX)} - (LIR / 2)\,I_{LOAD(MAX)}$$

where $I_{LIMIT(LOW)}$ equals minimum current-limit threshold voltage divided by the $R_{DS(ON)}$ of Q2. For the MAX1714, the minimum current-limit threshold using the 100mV default setting is 90mV. Use the worst-case maximum value for $R_{DS(ON)}$ from the MOSFET Q2 data sheet, and add some margin for the rise in $R_{DS(ON)}$ with temperature. A good general rule is to allow 0.5% additional resistance for each °C of temperature rise.

Examining the 8A circuit example with a maximum $R_{DS(ON)}$ = 12mΩ at high temperature reveals the following:

$$I_{LIMIT(LOW)} = 90mV / 12m\Omega = 7.5A$$

This 7.5A is greater than the valley current of 6.7A, so the circuit can easily deliver the full rated 8A using the default 100mV nominal ILIM threshold.

For an adjustable threshold, connect a two-resistor divider from REF to AGND, with ILIM connected at the center tap. The external adjustment range of 0.5V to 2.0V corresponds to a current-limit threshold of 50mV to 200mV. When adjusting the current limit, use 1% tolerance resistors to prevent a significant increase of errors in

the current-limit tolerance. A 1µA minimum divider current is recommended.

Output Capacitor Selection

The output filter capacitor must have low enough effective series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. Also, the capacitance value must be high enough to absorb the inductor energy going from a full-load to no-load condition without tripping the overvoltage protection circuit.

In CPU V_{CORE} converters and other applications where the output is subject to violent load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} \le \frac{V_{DIP}}{I_{LOAD(MAX)}}$$

In non-CPU applications, the output capacitor's size depends on how much ESR is needed to maintain an acceptable level of output voltage ripple:

$$R_{ESR} \le \frac{Vp\text{-}p}{LIR \cdot I_{LOAD(MAX)}}$$

The actual microfarad capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalums, OS-CONs, and other electrolytics).

When using low-capacity filter capacitors such as ceramic or polymer types, capacitor size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (also, see the V_{SAG} and V_{SOAR} equation in the *Transient Response* section).

Output Capacitor Stability Considerations

Stability is determined by the value of the ESR zero relative to the switching frequency. The point of instability is given by the following equation:

$$f_{ESR} = \frac{f}{\pi}$$

$$\text{where } f_{ESR} = \frac{1}{2 \cdot \pi \cdot R_{ESR} \cdot C_F}$$

For a typical 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz.

Tantalum and OS-CON capacitors in widespread use at the time of publication have typical ESR zero frequencies of 25kHz. In the design example used for inductor selection, the ESR needed to support 50mVp-p ripple is 60mV/2.7A = 22mΩ. Two 470µF/4V Kemet T510 low-ESR tantalum capacitors in parallel provide 22mΩ max ESR. Their typical combined ESR results in a zero at 27kHz, well within the bounds of stability.

Don't put high-value ceramic capacitors directly across the feedback sense point without taking precautions to ensure stability. Large ceramic capacitors can have a high ESR zero frequency and cause erratic, unstable operation. However, it's easy to add enough series resistance by placing the capacitors a couple of inches downstream from the feedback sense point, which should be as close as possible to the inductor (see the *All-Ceramic-Capacitor Application* section).

Unstable operation manifests itself in two related but distinctly different ways: double-pulsing and fast-feedback loop instability.

Double-pulsing occurs due to noise on the output or because the ESR is so low that there isn't enough voltage ramp in the output voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the 400ns minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability, which is caused by insufficient ESR.

Loop instability can result in oscillations at the output after line or load perturbations that can trip the overvoltage protection latch or cause the output voltage to fall below the tolerance limit.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output voltage ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Don't allow more than one cycle of ringing after the initial step-response under- or overshoot.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. Nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to power-up surge currents.

$$I_{RMS} = I_{LOAD}\left(\frac{\sqrt{V_{OUT}\left(V_{IN} - V_{OUT}\right)}}{V_{IN}}\right)$$

High-Speed Step-Down Controller for Notebook Computers

For optimal circuit reliability, choose a capacitor that has less than 10°C temperature rise at the peak ripple current.

Power MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability (>5A) when using high-voltage (>20V) AC adapters. Low-current applications usually require less attention.

For maximum efficiency, choose a high-side MOSFET (Q1) that has conduction losses equal to the switching losses at the optimum battery voltage (15V). Check to ensure that the conduction losses at **minimum** input voltage don't exceed the package thermal limits or violate the overall thermal budget. Check to ensure that conduction losses plus switching losses at the **maximum** input voltage don't exceed the package ratings or violate the overall thermal budget.

Choose a low-side MOSFET (Q2) that has the lowest possible $R_{DS(ON)}$, comes in a moderate to small package (i.e., SO-8), and is reasonably priced. Ensure that the MAX1714 DL gate driver can drive Q2; in other words, check that the gate isn't pulled up by the high-side switch turn on, due to parasitic drain-to-gate capacitance, causing cross-conduction problems. Switching losses aren't an issue for the low-side MOSFET, since it's a zero-voltage switched device when used in the buck topology.

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET, the worst-case power dissipation due to resistance occurs at minimum battery voltage:

$$PD(Q1\ Resistive) = (V_{OUT} / V_{IN(MIN)}) \cdot I_{LOAD}^2 \cdot R_{DS(ON)}$$

Generally, a small high-side MOSFET is desired to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power-dissipation limits often limits how small the MOSFET can be. Again, the optimum occurs when the switching (AC) losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses don't usually become an issue until the input is greater than approximately 15V.

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied, due to the squared term in the CV^2F switching loss equation. If the high-side MOSFET you've chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when subjected to $V_{IN(MAX)}$, you must reconsider your choice of MOSFET.

Calculating the power dissipation in Q1 due to switching losses is difficult, since it must allow for difficult-to-quantify factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PC board layout characteristics. The following switching loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including a sanity check using a thermocouple mounted on Q1.

$$PD(Q1\ switching) = \frac{C_{RSS} \cdot V_{IN(MAX)}^2 \cdot f \cdot I_{LOAD}}{I_{GATE}}$$

where C_{RSS} is the reverse transfer capacitance of Q1 and I_{GATE} is the peak gate-drive source/sink current (1A typical).

For the low-side MOSFET, Q2, the worst-case power dissipation always occurs at maximum battery voltage:

$$PD(Q2) = (1 - V_{OUT} / V_{IN(MAX)}) \cdot I_{LOAD}^2 \cdot R_{DS(ON)}$$

The absolute worst case for MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD(MAX)}$ but are not quite high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, you must "overdesign" the circuit to tolerate $I_{LOAD} = I_{LIMIT(HIGH)} + [(LIR / 2) \cdot I_{LOAD(MAX)}]$, where $I_{LIMIT(HIGH)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and on-resistance variation. This means that the MOSFETs must be very well heatsinked. If short-circuit protection without overload protection is enough, a normal I_{LOAD} value can be used for calculating component stresses.

Choose a Schottky diode D1 having a forward voltage low enough to prevent the Q2 MOSFET body diode from turning on during the dead time. As a general rule, a diode having a DC current rating equal to 1/3 of the load current is sufficient. This diode is optional, and if efficiency isn't critical it can be removed.

Application Issues

Dropout Performance

The output voltage adjust range for continuous-conduction operation is restricted by the nonadjustable 500ns (max) minimum off-time one-shot. For best dropout performance, use the slowest (200kHz) on-time setting. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on- and off-times. Manufacturing tolerances and internal propagation delays introduce an error to the TON K-factor. This error is greater at higher frequencies (Table 5). Also, keep in mind that transient response performance of buck regulators operated close to dropout is poor,

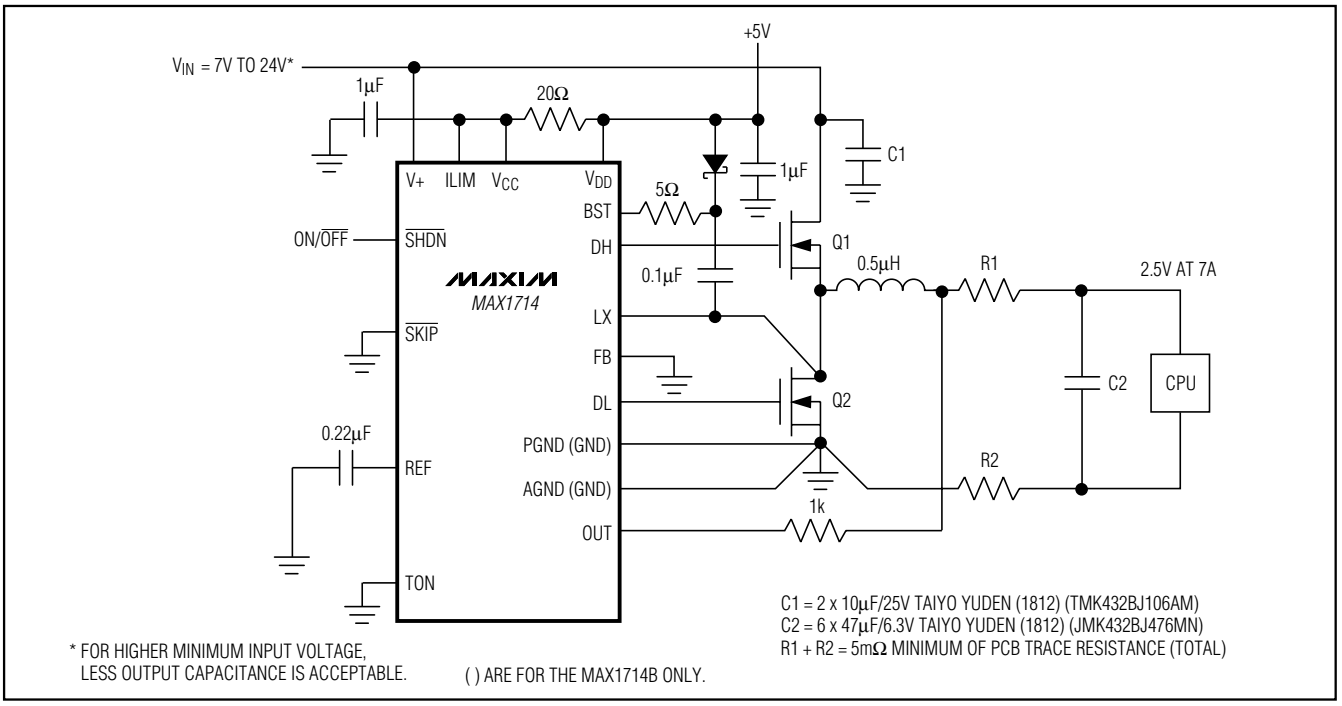


Figure 7. All-Ceramic-Capacitor Application

Table 5. Approximate K-Factor Errors

TON SETTING (kHz)	K FACTOR (µs)	APPROXIMATE K-FACTOR ERROR (%)	MIN V_{IN} AT V_{OUT} = 2V (V)
200	5	±10	2.6
300	3.3	±10	2.9
450	2.2	±12.5	3.2
600	1.7	±12.5	3.6

and bulk output capacitance must often be added (see the V_{SAG} equation in *Transient Response* section).

Dropout Design Example: V_{IN} = 3V min, V_{OUT} = 2V, f = 300kHz. The required duty is (V_{OUT} + V_{SW}) / (V_{IN} - V_{SW}) = (2V + 0.1V) / (3.0V - 0.1V) = 72.4%. The worst-case on-time is (V_{OUT} + 0.075) / V_{IN} • K = 2.075V / 3V • 3.35µs-V • 90% = 2.08µs. The IC duty-factor limitation is:

$$DUTY = \frac{t_{ON(MIN)}}{t_{ON(MIN)} + t_{OFF(MAX)}} = \frac{2.08\mu s}{2.08\mu s + 500ns} = 80.6\%,$$

which meets the required duty.

Remember to include inductor resistance and MOSFET on-state voltage drops (V_{SW}) when doing worst-case dropout duty-factor calculations.

All-Ceramic-Capacitor Application

Ceramic capacitors have advantages and disadvantages. They have ultra-low ESR, are noncombustible, are relatively small, and are nonpolarized. On the other hand, they're expensive and brittle, and their ultra-low ESR characteristic can result in excessively high ESR zero frequencies (affecting stability). In addition, their relatively low capacitance value can cause output overshoot when going abruptly from full-load to no-load conditions, unless there are some bulk tantalum or electrolytic capacitors in parallel to absorb the stored energy in the inductor. In some cases, there may be no room for electrolytics, creating a need for a DC-DC design that uses nothing but ceramics.

The all-ceramic-capacitor application of Figure 7 replaces the standard, typical tantalum output capacitors with ceramics in a 7A circuit. This design relies on having a minimum of 5mΩ parasitic PC board trace resistance in series with the capacitor in order to reduce the ESR zero frequency. This small amount of resistance is easily obtained by locating the MAX1714 circuit 2 or 3 inches away from the CPU, and placing all the ceramic

High-Speed Step-Down Controller for Notebook Computers

capacitors close to the CPU. Resistance values higher than 5mΩ just improve the stability (which can be observed by examining the load-transient response characteristic as shown in the *Typical Operating Characteristics*). Avoid adding excess PC board trace resistance, as there's an efficiency penalty; 5mΩ is sufficient for a 7A circuit.

$$R_{ESR} \geq \frac{1}{2FC_{OUT}}$$

V_{SOAR} determines the minimum output capacitance requirement. In this example, the switching frequency has been increased to 600kHz and the inductor value has been reduced to 0.5µH (compared to 300kHz and 1.5µH for the standard 8A circuit) in order to minimize the energy transferred from inductor to capacitor during load-step recovery. The overshoot must be calculated to avoid tripping the OVP latch. The efficiency penalty for operating at 600kHz is about 2% to 3%, depending on the input voltage.

An optional 1kΩ resistor is placed in series with OUT. This resistor attenuates high-frequency noise in some boards, which can cause double pulsing.

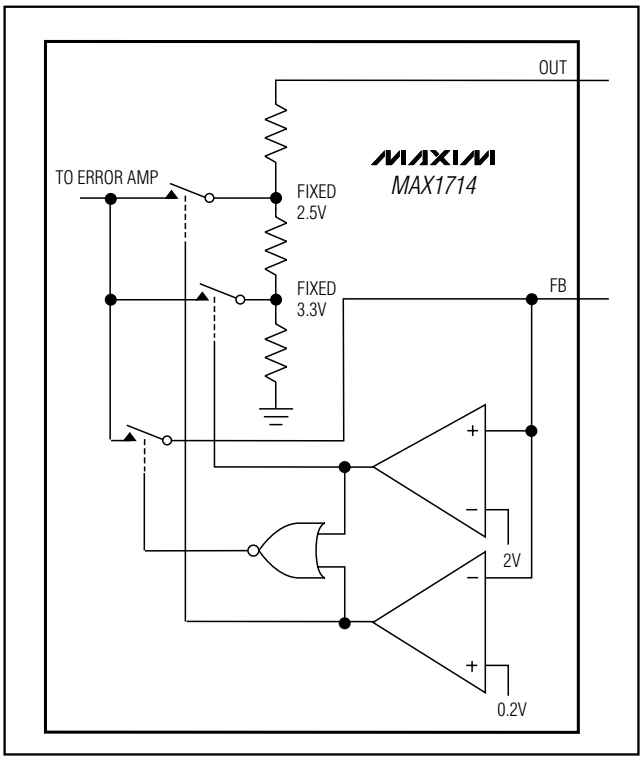


Figure 8. Feedback Mux

Fixed Output Voltages

The MAX1714's Dual Mode™ operation allows the selection of common voltages without requiring external components (Figure 8). Connect FB to AGND for a fixed +2.5V output or to V_{CC} for a +3.3V output, or connect FB directly to OUT for a fixed +1.0V output.

Setting V_{OUT} with a Resistor-Divider

The output voltage can be adjusted with a resistor-divider if desired (Figure 9). The equation for adjusting the output voltage is:

$$V_{OUT} = V_{FB}\left(1 + \frac{R1}{R2}\right)$$

where V_{FB} is 1.0V.

2-Stage (5V Powered) Notebook CPU Buck Regulator

The most efficient and overall cost-effective solution for stepping down a high-voltage battery to a very low output voltage is to use a single-stage buck regulator that's powered directly from the battery. However, there may be situations where the battery bus can't be routed near the CPU, or where space constraints dictate the smallest possible local DC-DC converter. In such cases, the 5V powered circuit of Figure 10 may be appropriate. The reduced input voltage allows a higher switching frequency and a much smaller inductor value.

PC Board Layout Guidelines

Careful PC board layout is critical to achieving low switching losses and clean, stable operation. The switching power stage requires particular attention (Figure 11). If possible, mount all of the power components on the top side of the board with their ground terminals flush against one another. Follow these guidelines for good PC board layout:

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Connect AGND and PGND together close to the IC. For the MAX1714B, these grounds are connected internally to the GND pin. Carefully follow the grounding instructions under step 4 of the *Layout Procedure*.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PC boards (2 oz vs. 1 oz) can enhance full-load efficiency by 1% or more. Correctly routing PC board traces is a difficult task that must be approached in terms of fractions of centimeters,

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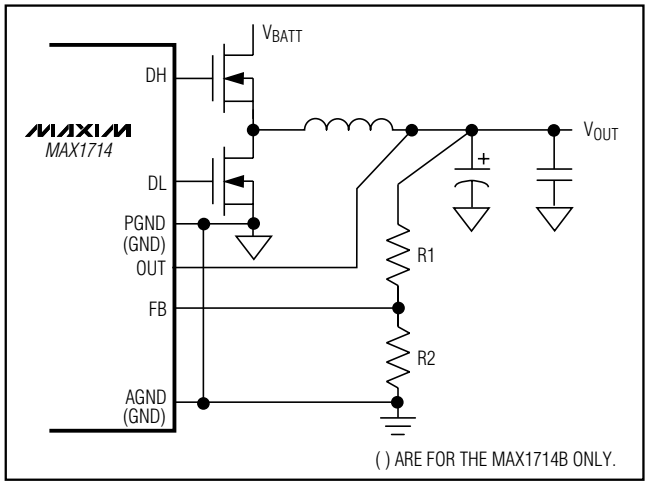

Figure 9. Setting V_{OUT} with a Resistor-Divider

where a single milliohm of excess trace resistance causes a measurable efficiency penalty.

- LX and PGND connections to Q2 for current limiting must be made using Kelvin sense connections to guarantee the current-limit accuracy. With SO-8 MOSFETs, this is best done by routing power to the MOSFETs from outside using the top copper layer, while tying in PGND and LX *inside* (underneath) the SO-8 package.
- When trade-offs in trace lengths must be made, it's preferable to allow the inductor charging path to be made longer than the discharge path. For example, it's better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
- Ensure that the OUT connection to C_{OUT} is short and direct. However, in some cases it may be desirable to deliberately introduce some trace length between the OUT inductor node and the output filter capacitor (see the *All-Ceramic-Capacitor Application* section).
- Route high-speed switching nodes (BST, LX, DH, and DL) away from sensitive analog areas (REF, FB).
- Make all pin-strap control input connections ($\overline{SKIP}$, ILIM, etc.) to AGND or V_{CC} rather than PGND or V_{DD}.

Layout Procedure

1) Place the power components first, with ground terminals adjacent (Q2 source, CIN-, COUT-, D1 anode). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Mount the controller IC adjacent to MOSFET Q2, preferably on the back side opposite Q2 in order to keep LX, PGND, and the DL gate-drive lines short and wide. The DL gate trace must be short and wide, measuring 10 to 20 squares (50 to 100 mils wide if the MOSFET is 1 inch from the controller IC).
3) Group the gate-drive components (BST diode and capacitor, V_{DD} bypass capacitor) together near the controller IC.
4) Make the DC-DC controller ground connections as shown in Figure 11. This diagram can be viewed as having three separate ground planes: output ground, where all the high-power components go; the PGND plane, where the PGND pin and V_{DD} bypass capacitor go; and an analog AGND plane, where sensitive analog components go. The analog ground plane and PGND plane must meet only at a single point directly beneath the IC. For the MAX1714B, this point should be the GND pin. These two planes are then connected to the high-power output ground with a short connection from V_{DD} cap/PGND to the source of the low-side MOSFET, Q2 (the middle of the star ground). This point must also be very close to the output capacitor ground terminal.
5) Connect the output power planes (V_{CORE} and system ground planes) directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the CPU as is practical.

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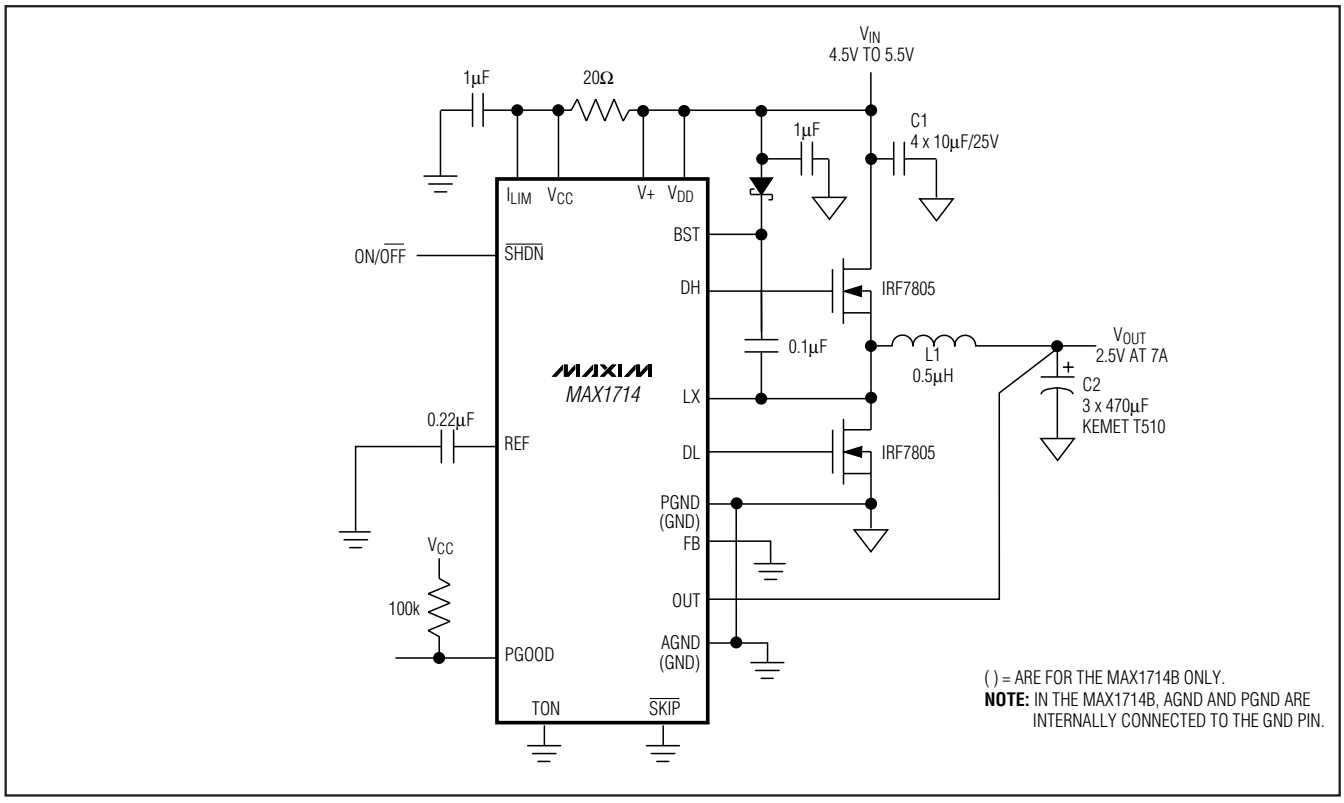
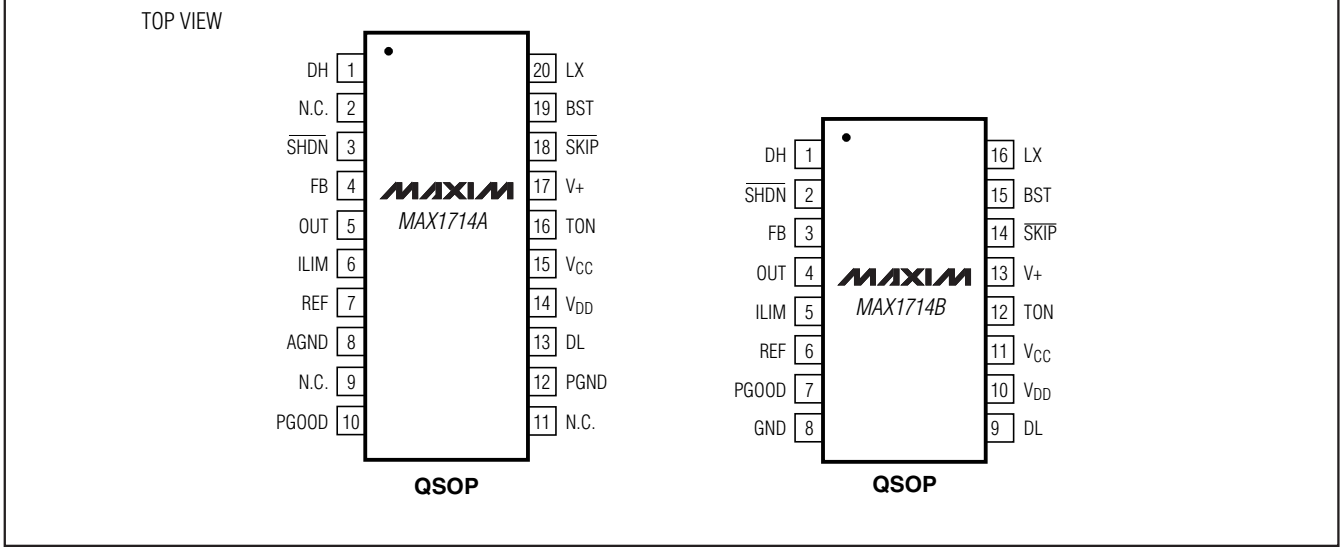


Figure 10. 5V Powered, 7A CPU Buck Regulator

Pin Configurations



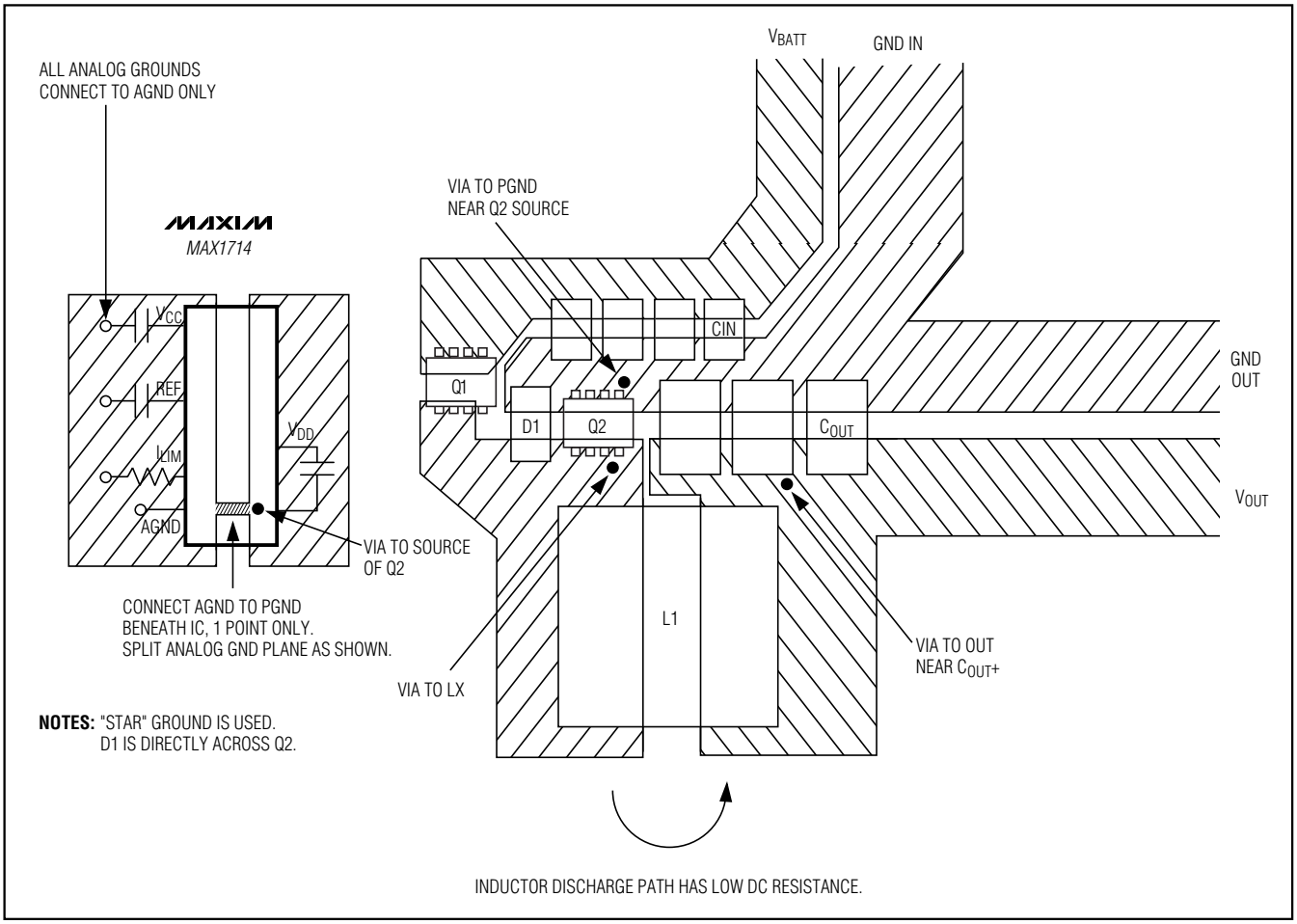


Figure 11. Power-Stage PC Board Layout Example

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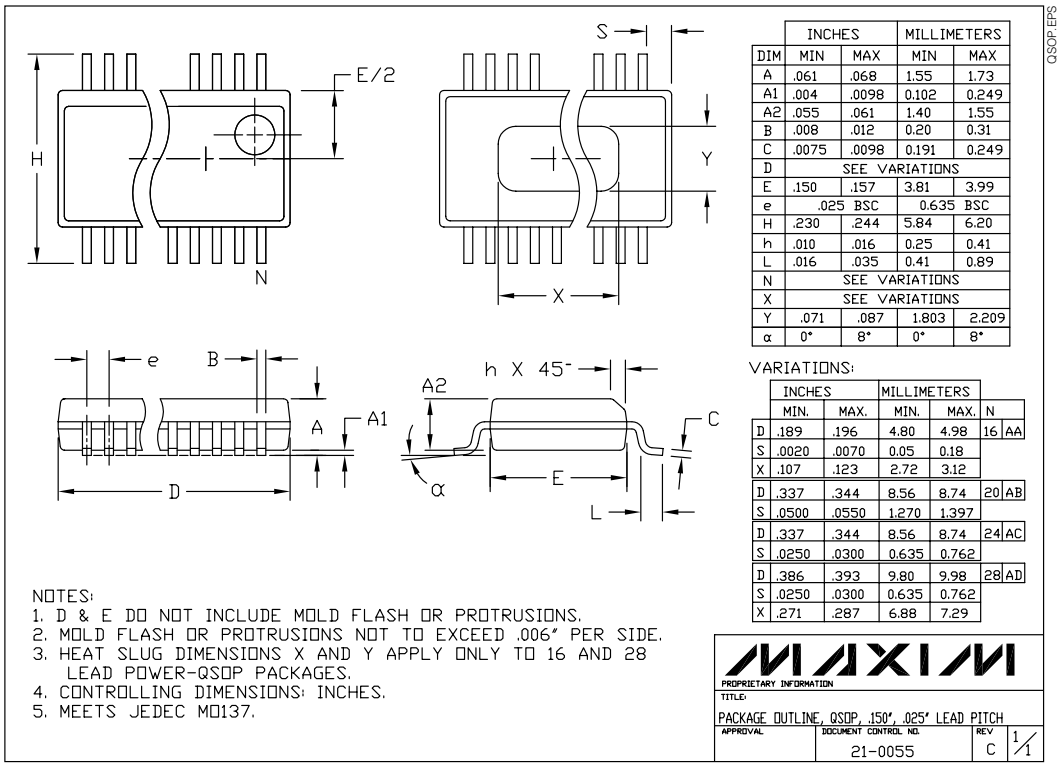
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.
5. MEETS JEDEC MO137.

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH
APPROVAL | DOCUMENT CONTROL NO. 21-0055 | REV C | 1/1

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