THE DATASHEET OF

MAX17511GTL+T

www.win-source.net 0086-755-83957316

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EVALUATION KIT AVAILABLE

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

General Description

The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T are dual-output, step-down, constant on-time Quick-PWM™ controllers for VR12/IMVP-7 CPU core supplies. The controllers consist of two high-current switching power supplies for CPU and GFX cores. The CPU regulator (regulator A) is a three-phase constant on-time architecture. The GFX regulator (regulator B) is also constant on-time architecture. The MAX17411 supports 2-phase operation and the MAX17511/MAX17511C/MAX17511N/MAX17511T support 1-phase operation. The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T include two internal drivers on regulator A and one internal driver on regulator B. External drivers such as the MAX17491 enable the additional phases.

Both regulator A and regulator B include output voltage sensing and accurate load-line gain. Switching frequencies are programmable from 200kHz to 600kHz per phase. Output overvoltage protection (OVP, MAX17411/MAX17511/MAX17511C/MAX17511N), undervoltage protection (UVP), and thermal protection ensure effective and reliable operation. When any of these protection features detect a fault, the controller shuts down both outputs.

The multiphase regulators include transient-phase overlap and active overshoot suppression, which speed up the response time and reduce the total output capacitance. The CPU and GFX outputs are controlled independently by writing the appropriate data into a function-mapped register file. VID code transitions and soft-start are enabled with a precision slew-rate control circuit. The SVID interface also allows each regulator to be individually set into a low-power, single-phase, pulse-skipping state to optimize efficiency. The MAX17411 is available in a 48-pin, 6mm x 6mm, TQFN package. The MAX17511/MAX17511C/MAX17511N/MAX17511T are available in a 40-pin, 5mm x 5mm, TQFN lead-free package.

Applications

VR12/IMVP-7 CPU Core Power Supplies

Notebooks/Desktops/Servers

Features

- **Intel VR12/IMVP-7-Compliant Serial Interface**
- **3-/2-/1-Phase Quick-PWM CPU Core Regulator**
  - **Two Internal Drivers and One External Driver**
  - **Transient-Phase Overlap Mode**
  - **Dynamic Phase Selection**
- **2-/1-Phase Quick-PWM GFX Regulator**
  - **One Internal and One External Driver**
- **Active Overshoot Suppression**
- **8-Bit VR12/IMVP-7 DAC**
- **±0.5% V_{OUT} Accuracy Over Line, Load, and Temperature**
- **Active Voltage Positioning with Programmable Gain**
- **Accurate Lossless Current Balance**
- **Accurate Droop and Current Limit**
- **Remote Output and Ground Sense**
- **Power-Good Window Comparators (POKA and POKB)**
- **4.5V to 24V Battery-Input Voltage Range**
- **Programmable 200kHz to 600kHz Switching Frequency**
- **External Thermal-Fault Detection Output (VR_HOT#)**
- **Overvoltage (MAX17411/MAX17511/MAX17511C/MAX17511N), Undervoltage, and Thermal-Fault Protection**
- **Slew-Rate Controlled Soft-Start**
- **Passive Soft-Shutdown (20Ω Discharge Switches)**
- **Integrated Boost Switches**
- **Low-Profile, 48-Lead/40-Lead TQFN Packages**

Quick PWM is a trademark of Maxim Integrated Products, Inc.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	FEATURE
MAX17411GTM+	-40°C to +105°C	48 TQFN-EP*	3-/2-/1-Phase + 2-/1-Phase
MAX17511GTL+	-40°C to +105°C	40 TQFN-EP*	3-/2-/1-Phase + 1-Phase

Ordering Information continued on last page.

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

For information on other Maxim products, visit Maxim's website at www.maxim-ic.com.

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

ABSOLUTE MAXIMUM RATINGS

V_{CC}, V_{DDA}, V_{DDB} to GND (AGND) ..... -0.3V to +6V
VDIO, CLK, ALERT# to GND (AGND) ..... -0.3V to +6V
CSPAAVE, CSPBAVE, CSP_,
CSN_ to GND (AGND) ..... -0.3V to +6V
FBA, FBB to GND (AGND) ..... -0.3V to (V_{CC} + 0.3V)
SR, IMAX_ to GND (AGND) ..... -0.3V to (V_{CC} + 0.3V)
POKA, POKB, EN to GND (AGND) ..... -0.3V to +6V
VR_HOT# to GND (AGND) ..... -0.3V to +6V
THERMA, THERMB to GND (AGND) ..... -0.3V to (V_{CC} + 0.3V)
GNDSA, GNDSB to GND (AGND) ..... -0.3V to +0.3V
TON to GND ..... -0.3V to +26V
DRVPWMA to GND (AGND) ..... -0.3V to (V_{DDA} + 0.3V)
DRVPWMB to GND (AGND) ..... -0.3V to (V_{DDB} + 0.3V)
DLA_ to GND (PGND) ..... -0.3V to (V_{DDA} + 0.3V)
DLB to GND (PGND) ..... -0.3V to (V_{DDB} + 0.3V)
BSTA_ to V_{DDA} ..... -0.3V to +26V
BSTB to V_{DDB} ..... -0.3V to +26V
LXA_ to BSTA_ ..... -6V to +0.3V
LXB to BSTB ..... -6V to +0.3V
LX_ to GND (AGND) ..... -6V to +26V
DHA_ to LXA_ ..... -0.3V to ($V_{BSTA_}$ + 0.3V)
DHB to LXB ..... -0.3V to (V_{BSTB} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
40-Pin TQFN (derate 35.7mW/°C above +70°C) ... 2857.1mW
48-Pin TQFN (derate 37mW/°C above +70°C) 2963mW
Operating Temperature Range ..... -40°C to +105°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +165°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

PACKAGE THERMAL CHARACTERISTICS (Note 1)

40 TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 28°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 1.6°C/W

48 TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 27°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 1.3°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS_}$ = 0V, $V_{FB_}$ = V_{CSP_AVE} = $V_{CSP_}$ = $V_{CSN_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C. All devices 100% tested at T_A = +25°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range		V_{CC}, V_{DDA}, V_{DDB}		4.5		5.5	V
DC Output Voltage Accuracy		Measured at FB_ with respect to GNDS_; includes load regulation error (Note 2)	DAC codes from 1.000V to 1.520V	-0.5		+0.5	%
			DAC codes from 0.800V to 0.995V	-5		+5	mV
			DAC codes from 0.250V to 0.795V	-8		+8	
Line Regulation Error		V_{CC} = 4.5V to 5.5V, V_{IN} = 4.5V to 24V			0.1		mV
$V_{SETTLED}$ Bit Accuracy		Upward transitions		-15	-10	-5	mV
		Downward transitions		5	10	15	
GNDS_ Input Range				-200		+200	mV
GNDS_ Gain	A_{GNDS}	$\Delta V_{OUT}/\Delta V_{GNDS_}$		0.97	1.00	1.03	V/V
GNDS_ Input Bias Current		T_A = +25°C		-0.5		+0.5	µA
TON Shutdown Current		EN = GND, V_{IN} = 24V, V_{CC} = 0V, T_A = +25°C			0.01	0.1	µA
Boot Voltage	V_{BOOT}	MAX17511N only, Reg A and Reg B		1.094	1.100	1.106	V
		MAX17511C only, Reg B only		0.895	0.900	0.905	

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS_}$ = 0V, $V_{FB_}$ = V_{CSP_AVE} = $V_{CSP_}$ = $V_{CSN_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C. All devices 100% tested at T_A = +25°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DHA_ On-Time (Note 3)	t_{ONA}	Measured at DHA_ (600kHz - 10%), R_{TON} = 96.7kΩ (MAX17411 only), R_{TON} = 48.35kΩ (MAX17511/MAX17511C/MAX17511N/MAX17511T)	157	185	213	ns
		Measured at DHA_, V_{IN} = 12V (300kHz - 10%), R_{TON} = 200kΩ (MAX17411 only), R_{TON} = 100kΩ (MAX17511/MAX17511C/MAX17511N/MAX17511T)	276	307	338	
		Measured at DHA_ (200kHz - 10%), R_{TON} = 303.3kΩ (MAX17411 only), R_{TON} = 151.65kΩ (MAX17511/MAX17511C/MAX17511N/MAX17511T)	470	554	638	
DHB On-Time (Note 3)	t_{ONB}	Measured at DHB (600kHz + 10%), R_{TON} = 96.7kΩ (MAX17411 only), R_{TON} = 48.35kΩ (MAX17511/MAX17511C/MAX17511N/MAX17511T)	128	151	174	ns
		Measured at DHB, V_{IN} = 12V (300kHz + 10%), R_{TON} = 200kΩ (MAX17411 only), R_{TON} = 100kΩ (MAX17511/MAX17511C/MAX17511N/MAX17511T)	226	251	277	
		Measured at DHB (200kHz + 10%), R_{TON} = 303.3kΩ (MAX17411 only), R_{TON} = 151.65kΩ (MAX17511/MAX17511C/MAX17511N/MAX17511T)	385	453	521	
Minimum Off-Time (Note 3)	$t_{OFF(MIN)}$	Measured at DH_	150	200	250	ns
Minimum DRVPWM_ Pulse Width				40		ns
BIAS CURRENTS						
Quiescent Supply Current (V_{CC})	I_{BIAS}	Measured at V_{CC}, SKIP mode, FB_ forced above the regulation point		5	10	mA
Quiescent Supply Current ($V_{DD_}$)	I_{DRV}	T_A = +25°C, measured at $V_{DD_}$, FPWM mode, FB_ forced above the regulation point		0.02	1	µA
Shutdown Supply Current (V_{CC})		Measured at V_{CC}, EN = GND		16	30	µA
Shutdown Supply Current ($V_{DD_}$)		T_A = +25°C, measured at V_{DD}, EN = GND		0.01	1	µA
SLEW-RATE CONTROL						
Slew-Rate Accuracy		V_{SR} = 0V or V_{SR} = 5V; SetVID - fast slew rate = 10mV/µs (min)	10			mV/µs
		V_{SR} = 0V or V_{SR} = 5V; SetVID - slow slew rate = 2.5mV/µs (min)	2.5			
		V_{SR} = 3V or V_{SR} = 1.5V; SetVID - fast slew rate = 20mV/µs (min)	20			
		V_{SR} = 3V or V_{SR} = 1.5V; SetVID - slow slew rate = 5mV/µs (min)	5			

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS_}$ = 0V, $V_{FB_}$ = V_{CSP_AVE} = $V_{CSP_}$ = $V_{CSN_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C. All devices 100% tested at T_A = +25°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Soft-Start Slew Rate		Non-zero V_{BOOT}	2.5			mV/µs
Discharge Switch Resistance		CSNA, CSNB		20		Ω
SR Four-Level Logic Thresholds		Low			0.4	V
		Mid-low	1.2		1.8	
		Mid-high	2.2		V_{CC} - 1.2V	
		High	V_{CC} - 0.4V			
FAULT PROTECTION						
Upper POK_ (MAX17411/ MAX17511/MAX17511C/ MAX17511N/MAX17511T) and Output Overvoltage Protection Trip Threshold(MAX17411/ MAX17511/MAX17511C/ MAX17511N)	V_{OVP}	SKIP mode after output reaches the regulation voltage or PWM mode; measured at FB_ with respect to the voltage target set by the VID code (see Table 3)	200	250	300	mV
		Soft-start, SKIP mode, and output has not reached the regulation voltage; measured at FB_	1.72	1.77	1.82	V
		Minimum OVP threshold, measured at FB_		0.8		
Upper POK_ and Output Overvoltage Propagation Delay	t_{OVP}	FB_ forced 25mV above trip threshold (MAX17411/MAX17511/MAX17511C/MAX17511N)		5		µs
Lower POK_ and Output Undervoltage Protection Trip Threshold	V_{UVP}	Measured at FB_ with respect to unloaded output voltage	-300	-250	-200	mV
Lower POK_ Propagation Delay		FB_ forced 25mV below trip threshold		5		µs
Output Undervoltage Propagation Delay	t_{UVP}	FB_ forced 25mV below trip threshold	100	200	350	µs
POK_ Output Low Voltage		I_{SINK} = 4mA			0.3	V
POK_ Leakage Current		High state, POK_ forced to 5V, T_A = +25°C			1	µA
POK_ Startup Delay and Transitions Blanking Time	$t_{POK_}$	Measured from the time when FB_ reaches the target voltage		20		µs
V_{CC} Undervoltage-Lockout Threshold	V_{UVLO}	Rising edge, 50mV typical hysteresis, controller disabled below this level	4.05	4.25	4.45	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS_}$ = 0V, $V_{FB_}$ = V_{CSP_AVE} = $V_{CSP_}$ = $V_{CSN_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C. All devices 100% tested at T_A = +25°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
THERMAL PROTECTION							
VR_HOT# Trip Threshold		Measured at THERM_ with respect to V_{CC} falling edge; specify as % error for all TEMP MAX DAC code settings, typical hysteresis = 100mV		49.5		50.5	%
Thermal Zone Registers Trip Points		Thermal zone comparator trip points, measured with respect to V_{CC}; voltage threshold corresponding to TMAX x (1 - N%), N = 0, 3, 6, 9, 12, 15, 18, 25		49 + 24 x N/31	50 + 24 x N/31	51 + 24 x N/31	%
THERM_ Input Leakage	I_{THRM}	$V_{THERM_}$ = 2.5V, T_A = +25°C		-100		+100	nA
VR_HOT# Leakage Current		High-Z state (THERM_ > 0.505 x V_{CC}), VR_HOT# forced to 5V, T_A = +25°C				1	µA
Internal Thermal Fault Shutdown Threshold	T_{TSHDN}	Typical hysteresis = 15°C			160		°C
VALLEY CURRENT LIMIT AND DROOP							
Valley Current-Limit Threshold Voltage (Positive)	V_{ILIMA}	$V_{CSP_}$ - $V_{CSN_}$, V_{SR} = 0V, V_{SR} = 1.5V, or one-phase operation	R_{SENSE} = 0.65mΩ, I_{MAXA} = 39A	22.5	25.5	28.5	mV
			R_{SENSE} = 0.65mΩ, I_{MAXA} = 36A	21.5	24.5	27.5	
			R_{SENSE} = 0.65mΩ, I_{MAXA} = 30A	17.0	20.0	23.0	
			R_{SENSE} = 0.65mΩ, I_{MAXA} = 26A	15.0	18.0	21.0	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 39A	27.0	30.0	33.0	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 36A	25.0	28.0	31.0	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 30A	20.0	23.0	26.0	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 26A	17.0	20.0	23.0	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 39A	30.0	33.0	36.0	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 36A	28.0	31.0	34.0	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 30A	22.5	25.5	28.5	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 26A	20.0	23.0	26.0	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 39A	33.5	36.5	39.5	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 36A	31.0	34.0	37.0	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 30A	25.0	28.0	31.0	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 26A	21.5	24.5	27.5	

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS_}$ = 0V, $V_{FB_}$ = V_{CSP_AVE} = $V_{CSP_}$ = $V_{CSN_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C. All devices 100% tested at T_A = +25°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Valley Current-Limit Threshold Voltage (Positive)	V_{ILIMA}	$V_{CSP_}$ - $V_{CSN_}$, V_{SR} = 3V or V_{SR} = 5V, exclude one-phase operaton	R_{SENSE} = 0.65mΩ, I_{MAXA} = 39A	29.0	33.0	37.0	mV
			R_{SENSE} = 0.65mΩ, I_{MAXA} = 36A	28.0	32.0	36.0	
			R_{SENSE} = 0.65mΩ, I_{MAXA} = 30A	22.0	26.0	30.0	
			R_{SENSE} = 0.65mΩ, I_{MAXA} = 26A	19.5	23.5	27.5	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 39A	35.0	39.0	43.0	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 36A	32.5	36.5	40.5	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 30A	26.0	29.9	33.8	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 26A	22.0	26.0	30.0	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 39A	39.0	43.0	47.0	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 36A	36.5	40.5	44.5	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 30A	29.0	33.0	37.0	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 26A	26.0	30.0	34.0	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 39A	43.5	47.5	51.5	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 36A	40.0	44.0	48.0	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 30A	32.5	36.5	40.5	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 26A	28.0	32.0	36.0	
Valley Current-Limit Threshold Voltage (Positive)	V_{ILIMB}	$V_{CSP_}$ - $V_{CSN_}$, V_{SR} = 0V, V_{SR} = 1.5V, or one-phase operation	R_{SENSE} = 0.65mΩ, I_{MAXB} = 39A	22.5	25.5	28.5	mV
			R_{SENSE} = 0.65mΩ, I_{MAXB} = 36A	21.5	24.5	27.5	
			R_{SENSE} = 0.65mΩ, I_{MAXB} = 23A	13.0	16.0	19.0	
			R_{SENSE} = 0.65mΩ, I_{MAXB} = 20A	11.0	14.0	17.0	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 39A	27.0	30.0	33.0	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 36A	25.0	28.0	31.0	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 23A	15.0	18.0	21.0	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 20A	13.0	16.0	19.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 39A	30.0	33.0	36.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 36A	28.0	31.0	34.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 23A	17.0	20.0	23.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 20A	15.0	18.0	21.0	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 39A	33.5	36.5	39.5	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 36A	31.0	34.0	37.0	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 23A	20.0	23.0	26.0	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 20A	17.0	20.0	23.0	

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS_}$ = 0V, $V_{FB_}$ = V_{CSP_AVE} = $V_{CSP_}$ = $V_{CSN_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C. All devices 100% tested at T_A = +25°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Valley Current-Limit Threshold Voltage (Positive)	V_{ILIMB}	$V_{CSP_}$ - $V_{CSN_}$, V_{SR} = 3V or V_{SR} = 5V, exclude one-phase operaton	R_{SENSE} = 0.65mΩ, I_{MAXB} = 39A	29.0	33.0	37.0	mV
			R_{SENSE} = 0.65mΩ, I_{MAXB} = 36A	28.0	32.0	36.0	
			R_{SENSE} = 0.65mΩ, I_{MAXB} = 23A	17.0	21.0	25.0	
			R_{SENSE} = 0.65mΩ, I_{MAXB} = 20A	14.0	18.0	22.0	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 39A	35.0	39.0	43.0	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 36A	32.5	36.5	40.5	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 23A	19.5	23.5	27.5	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 20A	17.0	21.0	25.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 39A	39.0	43.0	47.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 36A	36.5	40.5	44.5	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 23A	22.0	26.0	30.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 20A	19.5	23.5	27.5	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 39A	43.5	47.5	51.5	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 36A	40.0	44.0	48.0	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 23A	26.0	30.0	34.0	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 20A	22.0	26.0	30.0	
Current-Limit Threshold Voltage (Zero Crossing)	V_{ZERO}	V_{GND} - $V_{LX_}$			1		mV
Current-Balance Offset Voltage				-1.5		+1.5	mV
CSPAAVE, CSPBAVE, CSP_, Input Current		T_A = +25°C		-0.12		+0.12	µA
CSN_ Pulldown Current				7		14	µA
Phase Disable Threshold		CSPB2, CSPB1, CSPA3, CSPA2, CSPA1		3	V_{CC} - 1	V_{CC} - 0.4	V
FB_ Droop Amplifier (GMD) Offset		(V_{CSP_AVE} - $V_{CSN_}$) at $I_{FB_}$ = 0mA		-1.0		+1.0	mV
FB_ Droop Amplifier (GMD) Transconductance		$\Delta I_{FB_}/\Delta(V_{CSP_AVE} - V_{CSN_})$, V_{CSP_AVE} - $V_{CSN_}$ = -15mV to +15mV		591	600	609	µS

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS_}$ = 0V, $V_{FB_}$ = V_{CSP_AVE} = $V_{CSP_}$ = $V_{CSN_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C. All devices 100% tested at T_A = +25°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IMAX_ LOGIC						
IMAX_ Detection Thresholds		Threshold 0, fault			13.65 x V_{CC}/50	V
		Threshold 1, R_{SENSE} = 0.65mΩ, I_{MAX} = 39A	14.20 x V_{CC}/50		14.65 x V_{CC}/50	
		Threshold 2, R_{SENSE} = 0.65mΩ, I_{MAX} = 36A	15.20 x V_{CC}/50		15.65 x V_{CC}/50	
		Threshold 3, R_{SENSE} = 0.65mΩ, $I_{MAXA/B}$ = 30A/23A	16.20 x V_{CC}/50		16.65 x V_{CC}/50	
		Threshold 4, R_{SENSE} = 0.65mΩ, $I_{MAXA/B}$ = 26A/20A	17.20 x V_{CC}/50		17.65 x V_{CC}/50	
		Threshold 5, R_{SENSE} = 0.75mΩ, I_{MAX} = 39A	18.20 x V_{CC}/50		18.65 x V_{CC}/50	
		Threshold 6, R_{SENSE} = 0.75mΩ, I_{MAX} = 36A	19.20 x V_{CC}/50		19.65 x V_{CC}/50	
		Threshold 7, R_{SENSE} = 0.75mΩ, I_{MAX} = 30A/23A	20.20 x V_{CC}/50		20.65 x V_{CC}/50	
		Threshold 8, R_{SENSE} = 0.75mΩ, I_{MAX} = 26A/20A	21.20 x V_{CC}/50		21.65 x V_{CC}/50	
		Threshold 9, R_{SENSE} = 0.85mΩ, I_{MAX} = 39A	22.20 x V_{CC}/50		22.65 x V_{CC}/50	
		Threshold 10, R_{SENSE} = 0.85mΩ, I_{MAX} = 36A	23.20 x V_{CC}/50		23.65 x V_{CC}/50	
		Threshold 11, R_{SENSE} = 0.85mΩ, $I_{MAXA/B}$ = 30A/23A	24.20 x V_{CC}/50		24.65 x V_{CC}/50	
		Threshold 12, R_{SENSE} = 0.85mΩ, $I_{MAXA/B}$ = 26A/20A	25.20 x V_{CC}/50		25.65 x V_{CC}/50	
		Threshold 13, R_{SENSE} = 0.95mΩ, I_{MAX} = 39A	26.20 x V_{CC}/50		26.65 x V_{CC}/50	
		Threshold 14, R_{SENSE} = 0.95mΩ, I_{MAX} = 36A	27.20 x V_{CC}/50		27.65 x V_{CC}/50	
		Threshold 15, R_{SENSE} = 0.95mΩ, $I_{MAXA/B}$ = 30A/23A	28.20 x V_{CC}/50		28.65 x V_{CC}/50	
		Threshold 16, R_{SENSE} = 0.95mΩ, $I_{MAXA/B}$ = 26A/20A	29.20 x V_{CC}/50		29.65 x V_{CC}/50	
		Threshold 17, fault	30.20 x V_{CC}/50			

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS_}$ = 0V, $V_{FB_}$ = V_{CSP_AVE} = $V_{CSP_}$ = $V_{CSN_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C. All devices 100% tested at T_A = +25°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	$R_{ON(DH)}$	BST_ - LX_ forced to 5V	High state (pullup)		0.9	2.5	Ω
			Low state (pulldown)		0.7	2.0	
DL_ Gate-Driver On-Resistance	$R_{ON(DL)}$	High state (pullup)			0.7	2.0	Ω
		Low state (pulldown)			0.25	0.7	
Internal BST_ Switch On-Resistance	R_{BST}	BSTA1 to V_{DDA}, BSTA2 to V_{DDA}, BSTB to V_{DDB}, $V_{DD_}$ = 5V			10	20	Ω
DH_ Gate-Driver Source Current	$I_{DH(SRC)}$	DH_ forced to 2.5V, BST_ - LX_ forced to 5V			2.2		A
DH_ Gate-Driver Sink Current	$I_{DH(SINK)}$	DH_ forced to 2.5V, BST_ - LX_ forced to 5V			2.7		A
DL_ Gate-Driver Source Current	$I_{DL(SRC)}$	DL_ forced to 2.5V			2.7		A
DL_ Gate-Driver Sink Current	$I_{DL(SINK)}$	DL_ forced to 2.5V			8		A
Driver Propagation Delay		DH_ low to DL_ high			30		ns
		DL_ low to DH_ high			30		
DL_ Transition Time		DL_ falling, C_{DL} = 3nF			20		ns
		DL_ rising, C_{DL} = 3nF			20		
DH_ Transition Time		DH_ falling, C_{DH} = 3nF			20		ns
		DH_ rising, C_{DH} = 3nF			20		
DRVPWMA, DRVPWMB Logic-High Voltage		I_{SOURCE} = 3mA		$V_{DD_}$ - 0.4			V
DRVPWMA, DRVPWMB Logic-Low Voltage		I_{SINK} = 3mA				0.4	V
LOGIC AND I/O							
Enable Input High Voltage	V_{EN_IH}			0.67			V
Enable Input Low Voltage	V_{EN_IL}					0.33	V
Enable Input Current		T_A = +25°C		-1		+1	µA
SERIALVID INTERFACE (per Intel SerialVID Specification—see the *Detailed Description*)							
SerialVID Input Low Voltage (CLK, VDIO)	V_{IL}			-0.1		+0.45	V
SerialVID Input High Voltage (CLK, VDIO)	V_{IH}			0.65		V_{TT} + 1V	V
SerialVID Output High Voltage (VDIO, ALERT#)	V_{OH}	Open-drain pullup to V_{TT}			V_{TT}		V
SerialVID Output Low Level (VDIO, ALERT#)	V_{OL}	Open-drain pullup to V_{TT}, R_{PU} = 50Ω				0.36	V

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS_}$ = 0V, $V_{FB_}$ = V_{CSP_AVE} = $V_{CSP_}$ = $V_{CSN_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C. All devices 100% tested at T_A = +25°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SerialVID Open-Drain Output On-Resistance (VDIO, ALERT#, VRHOT#)	R_{ON}	I_{SINK} = 30mA	4		13	Ω
SerialVID Logic-Input Leakage Current (CLK, VDIO)		T_A = +25°C	-1		+1	µA
ALERT# Deasserted Leakage Current		T_A = +25°C, $V_{ALERT\#}$ = 3.3V			1	µA
SerialVID Logic Slew Rate (CLK, VDIO, ALERT#)			0.5		2.0	V/ns
SerialVID Input Capacitance	C_{PAD}				4	pF
CLK Frequency	f_{CLK}		13	25	33.3	MHz
CLK Absolute Min/Max Period		Specified as a percentage of f_{CLK}	-5		+5	%
CLK High Time	t_{HIGH}	Specified as a percentage of t_{CLK} period	45			%
CLK Low Time	t_{LOW}	Specified as a percentage of t_{CLK} period	45			%
Rise Time	t_{RISE}		0.25		2.5	ns
Fall Time	t_{FALL}		0.25		2.5	ns
Duty Cycle			45		55	%
SerialVID Inactivity Timeout	t_{RSTNA}		0.14		0.40	µs

ELECTRICAL CHARACTERISTICS

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS_}$ = 0V, $V_{FB_}$ = V_{CSP_AVE} = $V_{CSP_}$ = $V_{CSN_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = -40°C to +105°C**, unless otherwise noted. Specifications to -40°C and +105°C are guaranteed by design, not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range		V_{CC}, V_{DDA}, V_{DDB}		4.5		5.5	V
DC Output Voltage Accuracy		Measured at FB_ with respect to GNDS_; includes load regulation error (Note 2)	DAC codes from 1.000V to 1.520V	-0.8		+0.8	%
			DAC codes from 0.800V to 0.995V	-8		+8	mV
			DAC codes from 0.250 to 0.795V	-8		+8	
$V_{SETTLED}$ BIT Accuracy		Upward transitions		-15		-5	mV
		Downward transitions		5		15	
GNDS_ Input Range				-200		+200	mV
GNDS_ Gain	A_{GNDS}	$\Delta V_{OUT}/\Delta V_{GNDS_}$		0.97		1.03	V/V
Boot Voltage	V_{BOOT}	MAX17511N only, Reg A and Reg B		1.091		1.109	V
		MAX17511C only, Reg B only		0.892		0.908	

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS_}$ = 0V, $V_{FB_}$ = V_{CSP_AVE} = $V_{CSP_}$ = $V_{CSN_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = -40°C to +105°C**, unless otherwise noted. Specifications to -40°C and +105°C are guaranteed by design, not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DHA_ On-Time (Note 3)	t_{ONA}	Measured at DHA_ (600kHz - 10%), R_{TON} = 96.7kΩ (MAX17411 only), R_{TON} = 48.35K (MAX17511/MAX17511C/MAX17511N/MAX17511T)	157		213	ns
		Measured at DHA_, V_{IN} = 12V (300kHz - 10%), R_{TON} = 200kΩ (MAX17411 only), R_{TON} = 100kΩ (MAX17511/MAX17511C/MAX17511N/MAX17511T)	276		338	
		Measured at DHA_ (200kHz - 10%), R_{TON} = 303.3kΩ (MAX17411 only), R_{TON} = 151.65kΩ (MAX17511/MAX17511C/MAX17511N/MAX17511T)	470		638	
DHB On-Time (Note 3)	t_{ONB}	Measured at DHB (600kHz + 10%), R_{TON} = 96.7kΩ (MAX17411 only), R_{TON} = 48.35kΩ (MAX17511/MAX17511C/MAX17511N/MAX17511T)	128		174	ns
		Measured at DHB, V_{IN} = 12V (300kHz + 10%), R_{TON} = 200kΩ (MAX17411 only), R_{TON} = 100kΩ (MAX17511/MAX17511C/MAX17511N/MAX17511T)	226		277	
		Measured at DHB (200kHz + 10%), R_{TON} = 303.3kΩ (MAX17411 only), R_{TON} = 151.65kΩ (MAX17511/MAX17511C/MAX17511N/MAX17511T)	385		521	
Minimum Off-Time (Note 3)	$t_{OFF(MIN)}$	Measured at DH_	150		250	ns
BIAS CURRENTS						
Quiescent Supply Current (V_{CC})	I_{BIAS}	Measured at V_{CC}, SKIP mode, FB_ forced above the regulation point			10	mA
Shutdown Supply Current (V_{CC})		Measured at V_{CC}, EN = GND			30	µA
SLEW-RATE CONTROL						
Slew-Rate Accuracy		V_{SR} = 0V or V_{SR} = 5V; SetVID - fast slew rate = 10mV/µs (min)	10			mV/µs
		V_{SR} = 0V or V_{SR} = 5V; SetVID - slow slew rate = 2.5mV/µs (min)	2.5			
		V_{SR} = 3V or V_{SR} = 1.5V; SetVID - fast slew rate = 20mV/µs (min)	20			
		V_{SR} = 3V or V_{SR} = 1.5V; SetVID - slow slew rate = 5mV/µs (min)	5			
Soft-Start Slew Rate		Non-zero V_{BOOT}	2.5			mV/µs
SR Four-Level Logic Thresholds		Low			0.4	V
		Mid-low	1.2		1.8	
		Mid-high	2.2		V_{CC} - 1.2V	
		High	V_{CC} - 0.4V			

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS_}$ = 0V, $V_{FB_}$ = V_{CSP_AVE} = $V_{CSP_}$ = $V_{CSN_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = -40°C to +105°C**, unless otherwise noted. Specifications to -40°C and +105°C are guaranteed by design, not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FAULT PROTECTION							
Upper POK_ (MAX17411/ MAX17511/MAX17511N/ MAX17511T) and Output Overvoltage Protection Trip Threshold (MAX17411/ MAX17511/MAX17511C/ MAX17511N)	V_{OVP}	SKIP mode after output reaches the regulation voltage or PWM mode; measured at FB_ with respect to the voltage target set by the VID code (see Table 3)		200		300	mV
		Soft-start, SKIP mode, and output has not reached the regulation voltage, measured at FB_		1.72		1.82	V
Lower POK_ and Output Undervoltage Protection Trip Threshold	V_{UVP}	Measured at FB_ with respect to unloaded output voltage		-300		-200	mV
Output Undervoltage Propagation Delay	t_{UVP}	FB_ forced 25mV below trip threshold		100		350	µs
POK_ Output Low Voltage		I_{SINK} = 4mA				0.3	V
V_{CC} Undervoltage Lockout Threshold	V_{UVLO}	Rising edge, 50mV typical hysteresis, controller disabled below this level		4.05		4.45	V
THERMAL PROTECTION							
VR_HOT# Trip Threshold		Measured at THERM_ with respect to V_{CC} falling edge; specify as % error for all TEMP MAX DAC code settings; typical hysteresis = 100mV		49.5		50.5	%
Thermal Zone Registers Trip Points		Thermal zone comparator trip points, measured with respect to V_{CC}, voltage threshold corresponding to TMAX x (1 - N%), N = 0, 3, 6, 9, 12, 15, 18, 25		49 + 24 x N/31		51 + 24 x N/31	%
VALLEY CURRENT LIMIT AND DROOP							
Valley Current-Limit Threshold Voltage (Positive)	V_{ILIMA}	$V_{CSP_}$ - $V_{CSN_}$, V_{SR} = 0V, V_{SR} = 1.5V, or one-phase operation	R_{SENSE} = 0.65mΩ, I_{MAXA} = 39A	22.5		28.5	mV
			R_{SENSE} = 0.65mΩ, I_{MAXA} = 36A	21.5		27.5	
			R_{SENSE} = 0.65mΩ, I_{MAXA} = 30A	17.0		23.0	
			R_{SENSE} = 0.65mΩ, I_{MAXA} = 26A	15.0		21.0	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 39A	27.0		33.0	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 36A	25.0		31.0	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 30A	20.0		26.0	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 26A	17.0		23.0	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 39A	30.0		36.0	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 36A	28.0		34.0	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 30A	22.5		28.5	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 26A	20.0		26.0	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 39A	33.5		39.5	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 36A	31.0		37.0	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 30A	25.0		31.0	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 26A	21.5		27.5	

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS_}$ = 0V, $V_{FB_}$ = V_{CSP_AVE} = $V_{CSP_}$ = $V_{CSN_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = -40°C to +105°C**, unless otherwise noted. Specifications to -40°C and +105°C are guaranteed by design, not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Valley Current-Limit Threshold Voltage (Positive)	V_{ILIMA}	$V_{CSP_}$ - $V_{CSN_}$, V_{SR} = 3V or V_{SR} = 5V, exclude one-phase operation	R_{SENSE} = 0.65mΩ, I_{MAXA} = 39A	29.0		37.0	mV
			R_{SENSE} = 0.65mΩ, I_{MAXA} = 36A	28.0		36.0	
			R_{SENSE} = 0.65mΩ, I_{MAXA} = 30A	22.0		30.0	
			R_{SENSE} = 0.65mΩ, I_{MAXA} = 26A	19.5		27.5	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 39A	35.0		43.0	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 36A	32.5		40.5	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 30A	26.0		33.8	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 26A	22.0		30.0	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 39A	39.0		47.0	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 36A	36.5		44.5	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 30A	29.0		37.0	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 26A	26.0		34.0	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 39A	43.5		51.5	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 36A	40.0		48.0	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 30A	32.5		40.5	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 26A	28.0		36.0	
Valley Current-Limit Threshold Voltage (Positive)	V_{ILIMB}	$V_{CSP_}$ - $V_{CSN_}$, V_{SR} = 0V, V_{SR} = 1.5V, or one-phase operation	R_{SENSE} = 0.65mΩ, I_{MAXB} = 39A	22.5		28.5	mV
			R_{SENSE} = 0.65mΩ, I_{MAXB} = 36A	21.5		27.5	
			R_{SENSE} = 0.65mΩ, I_{MAXB} = 23A	13.0		19.0	
			R_{SENSE} = 0.65mΩ, I_{MAXB} = 20A	11.0		17.0	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 39A	27.0		33.0	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 36A	25.0		31.0	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 23A	15.0		21.0	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 20A	13.0		19.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 39A	30.0		36.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 36A	28.0		34.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 23A	17.0		23.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 20A	15.0		21.0	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 39A	33.5		39.5	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 36A	31.0		37.0	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 23A	20.0		26.0	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 20A	17.0		23.0	

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS_}$ = 0V, $V_{FB_}$ = V_{CSP_AVE} = $V_{CSP_}$ = $V_{CSN_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = -40°C to +105°C**, unless otherwise noted. Specifications to -40°C and +105°C are guaranteed by design, not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Valley Current-Limit Threshold Voltage (Positive)	V_{ILIMB}	$V_{CSP_}$ - $V_{CSN_}$, V_{SR} = 3V or V_{SR} = 5V, exclude one-phase operation	R_{SENSE} = 0.65mΩ, I_{MAXB} = 39A	29.0		37.0	mV
			R_{SENSE} = 0.65mΩ, I_{MAXB} = 36A	28.0		36.0	
			R_{SENSE} = 0.65mΩ, I_{MAXB} = 23A	17.0		25.0	
			R_{SENSE} = 0.65mΩ, I_{MAXB} = 20A	14.0		22.0	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 39A	35.0		43.0	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 36A	32.5		40.5	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 23A	19.5		27.5	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 20A	17.0		25.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 39A	39.0		47.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 36A	36.5		44.5	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 23A	22.0		30.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 20A	19.5		27.5	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 39A	43.5		51.5	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 36A	40.0		48.0	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 23A	26.0		34.0	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 20A	22.0		30.0	
Current-Balance Offset Voltage				-1.5		+1.5	mV
Phase Disable Threshold		CSPB2, CSPB1, CSPA3, CSPA2, CSPA1		3		V_{CC} - 0.4	V
FB_ Droop Amplifier (G_{MD}) Offset		V_{CSP_AVE} - $V_{CSN_}$ at $I_{FB_}$ = 0mA		-1.0		+1.0	mV
FB_ Droop Amplifier (G_{MD}) Transconductance		$\Delta I_{FB_}/\Delta(V_{CSP_AVE} - V_{CSN_})$, V_{CSP_AVE} - $V_{CSN_}$ = -15mV to +15mV		588		612	µS

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS_}$ = 0V, $V_{FB_}$ = V_{CSP_AVE} = $V_{CSP_}$ = $V_{CSN_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = -40°C to +105°C**, unless otherwise noted. Specifications to -40°C and +105°C are guaranteed by design, not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IMAX_ LOGIC							
IMAX_ Detection Thresholds		Threshold 0, fault				13.65 x V_{CC}/50	V
		Threshold 1, R_{SENSE} = 0.65mΩ, I_{MAX} = 39A		14.20 x V_{CC}/50		14.65 x V_{CC}/50	
		Threshold 2, R_{SENSE} = 0.65mΩ, I_{MAX} = 36A		15.20 x V_{CC}/50		15.65 x V_{CC}/50	
		Threshold 3, R_{SENSE} = 0.65mΩ, $I_{MAXA/B}$ = 30A/23A		16.20 x V_{CC}/50		16.65 x V_{CC}/50	
		Threshold 4, R_{SENSE} = 0.65mΩ, $I_{MAXA/B}$ = 26A/20A		17.20 x V_{CC}/50		17.65 x V_{CC}/50	
		Threshold 5, R_{SENSE} = 0.75mΩ, I_{MAX} = 39A		18.20 x V_{CC}/50		18.65 x V_{CC}/50	
		Threshold 6, R_{SENSE} = 0.75mΩ, I_{MAX} = 36A		19.20 x V_{CC}/50		19.65 x V_{CC}/50	
		Threshold 7, R_{SENSE} = 0.75mΩ, I_{MAX} = 30A/23A		20.20 x V_{CC}/50		20.65 x V_{CC}/50	
		Threshold 8, R_{SENSE} = 0.75mΩ, I_{MAX} = 26A/20A		21.20 x V_{CC}/50		21.65 x V_{CC}/50	
		Threshold 9, R_{SENSE} = 0.85mΩ, I_{MAX} = 39A		22.20 x V_{CC}/50		22.65 x V_{CC}/50	
		Threshold 10, R_{SENSE} = 0.85mΩ, I_{MAX} = 36A		23.20 x V_{CC}/50		23.65 x V_{CC}/50	
		Threshold 11, R_{SENSE} = 0.85mΩ, $I_{MAXA/B}$ = 30A/23A		24.20 x V_{CC}/50		24.65 x V_{CC}/50	
		Threshold 12, R_{SENSE} = 0.85mΩ, $I_{MAXA/B}$ = 26A/20A		25.20 x V_{CC}/50		25.65 x V_{CC}/50	
		Threshold 13, R_{SENSE} = 0.95mΩ, I_{MAX} = 39A		26.20 x V_{CC}/50		26.65 x V_{CC}/50	
		Threshold 14, R_{SENSE} = 0.95mΩ, I_{MAX} = 36A		27.20 x V_{CC}/50		27.65 x V_{CC}/50	
		Threshold 15, R_{SENSE} = 0.95mΩ, $I_{MAXA/B}$ = 30A/23A		28.20 x V_{CC}/50		28.65 x V_{CC}/50	
		Threshold 16, R_{SENSE} = 0.95mΩ, $I_{MAXA/B}$ = 26A/20A		29.20 x V_{CC}/50		29.65 x V_{CC}/50	
		Threshold 17, fault		30.20 x V_{CC}/50			
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	$R_{ON(DH)}$	BST_ - LX_ forced to 5V	High state (pullup)			2.5	Ω
			Low state (pulldown)			2.0	
DL_ Gate-Driver On-Resistance	$R_{ON(DL)}$	High state (pullup)				2.0	Ω
		Low state (pulldown)				0.7	

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS_}$ = 0V, $V_{FB_}$ = V_{CSP_AVE} = $V_{CSP_}$ = $V_{CSN_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = -40°C to +105°C**, unless otherwise noted. Specifications to -40°C and +105°C are guaranteed by design, not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Internal BST_ Switch On-Resistance	R_{BST}	BSTA1 to V_{DDA}, BSTA2 to V_{DDA}, BSTB to V_{DDB} $V_{DD_}$ = 5V			20	Ω
DRVPWMA, DRVPWMB Logic-High Voltage		I_{SOURCE} = 3mA	$V_{DD_}$ - 0.4			V
DRVPWMA, DRVPWMB Logic-Low Voltage		I_{SINK} = 3mA			0.4	V
LOGIC AND I/O						
Enable Input High Voltage	V_{EN_IH}		0.67			V
Enable Input Low Voltage	V_{EN_IL}				0.33	V
SERIALVID INTERFACE (per Intel SerialVID specification—see the *Detailed Description*)						
SerialVID Input Low Voltage (CLK, VDIO)	V_{IL}		-0.1		+0.45	V
SerialVID Input High Voltage (CLK, VDIO)	V_{IH}		0.65		V_{TT} + 1V	V
SerialVID Output Low Level (VDIO, ALERT#)	V_{OL}	Open-drain pullup to V_{TT}, R_{PU} = 50Ω			0.36	V
SerialVID Open-Drain Output On-Resistance (VDIO, ALERT#, VRHOT#)	R_{ON}	I_{SINK} = 30mA, T_A = 0°C to +105°C	4		13	Ω
SerialVID Logic Slew Rate (CLK, VDIO, ALERT#)			0.5		2.0	V/ns
SerialVID Input Capacitance	C_{PAD}				4	pF
CLK Frequency	f_{CLK}		13		33.3	MHz
CLK Absolute Min/Max Period		Specified as a percentage of f_{CLK}	-5		+5	%
CLK High Time	t_{HIGH}	Specified as a percentage of t_{CLK} period	45			%
CLK Low Time	t_{LOW}	Specified as a percentage of t_{CLK} period	45			%
Rise Time	t_{RISE}		0.25		2.5	ns
Fall Time	t_{FALL}		0.25		2.5	ns
Duty Cycle			45		55	%
SerialVID Inactivity Timeout	t_{RSTNA}		0.14		0.40	µs

Note 2: The equation for the target voltage V_{TARGET} is:

V_{TARGET} = the slew-rate-controlled version of either V_{DAC}

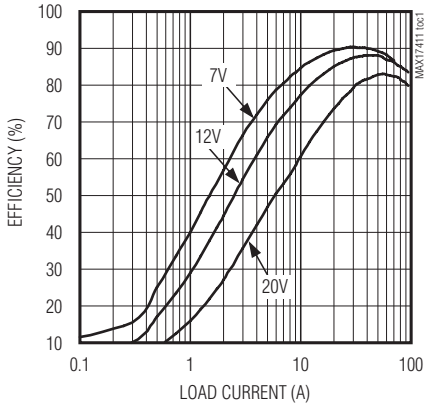
where V_{DAC} = 0V for shutdown, V_{DAC} = V_{BOOT} during startup, otherwise V_{DAC} = V_{ID} (the V_{ID} voltages for all possible VID codes are given in Table 3 and V_{OFFSET} = the negative or positive offset to the output voltage based on the voltage set from the offset register and the mode of operation (startup, shutdown, deeper sleep, or normal operation), as defined elsewhere in this document.

Note 3: On-time and minimum off-time specifications are measured from 50% to 50% at the DH_ pin, with LX_ forced to 0V, BST_ forced to 5V, and a 500pF capacitor from DH_ to LX_ to simulate external MOSFET gate capacitance. Actual in-circuit times may be different due to MOSFET switching speeds.

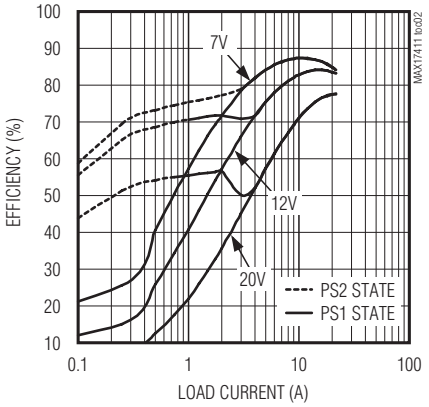
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

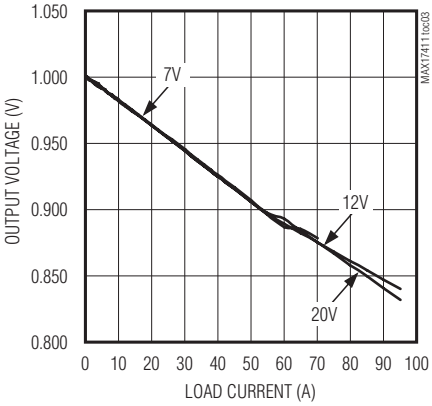
REG A EFFICIENCY vs. LOAD CURRENT IN PS0 STATE (SVID = 1V)



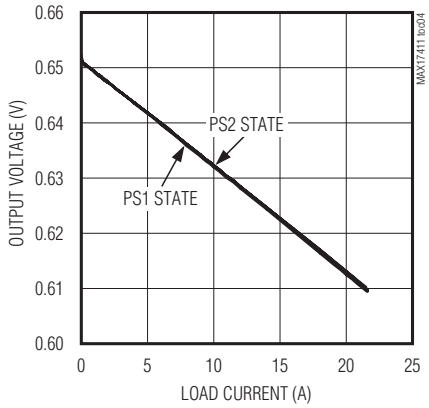
REG A EFFICIENCY vs. LOAD CURRENT IN PS1 AND PS2 STATES (SVID = 0.65V)



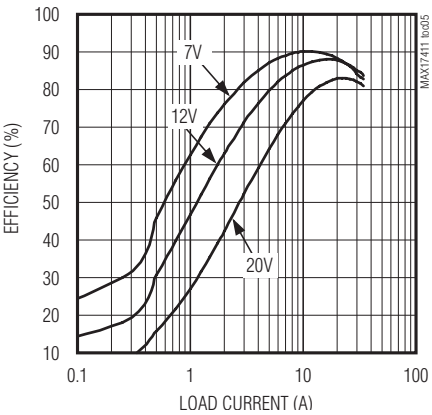
REG A OUTPUT VOLTAGE vs. LOAD CURRENT IN PS0 STATE (SVID = 1V)



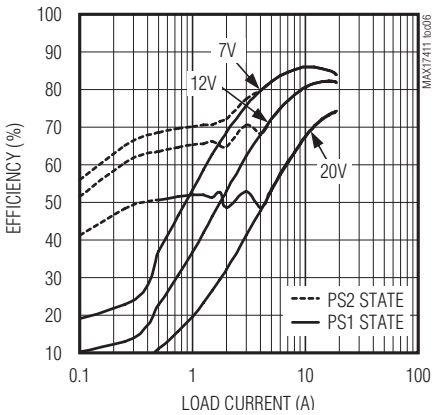
REG A OUTPUT VOLTAGE vs. LOAD CURRENT IN PS1 AND PS2 STATES (SVID = 0.65V)



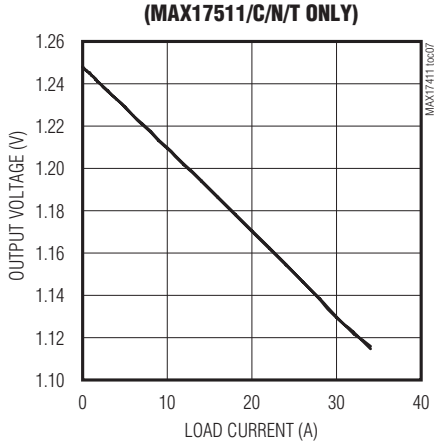
REG B EFFICIENCY vs. LOAD CURRENT IN PS0 STATE (SVID = 1.25V) (MAX17511/C/N/T ONLY)



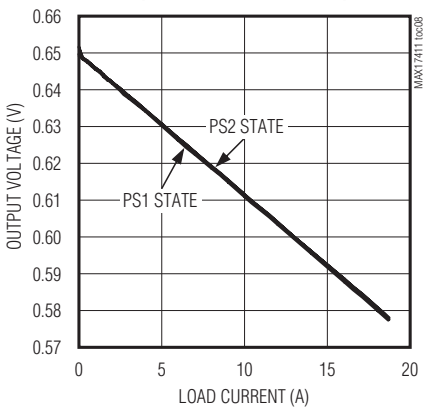
REG B EFFICIENCY vs. LOAD CURRENT IN PS1 AND PS2 STATES (SVID = 0.65V) (MAX17511/C/N/T ONLY)



REG B OUTPUT VOLTAGE vs. LOAD CURRENT IN PS0 STATE (SVID = 1.25V) (MAX17511/C/N/T ONLY)



REG B OUTPUT VOLTAGE vs. LOAD CURRENT IN PS1 AND PS2 STATES (SVID = 0.65V) (MAX17511/C/N/T ONLY)

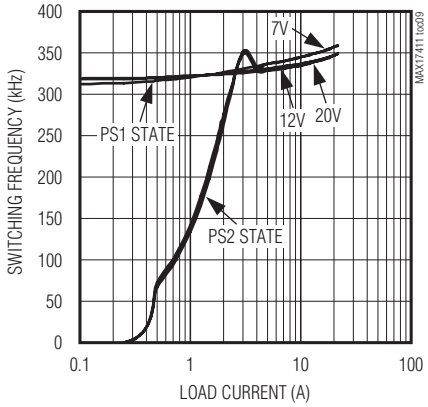


Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

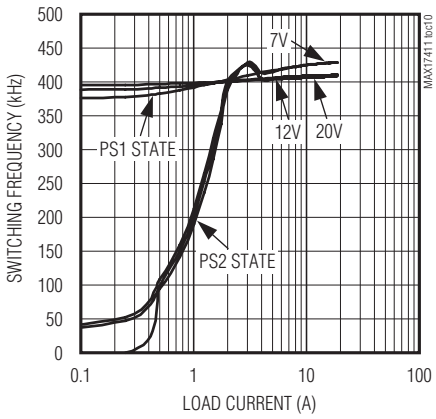
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

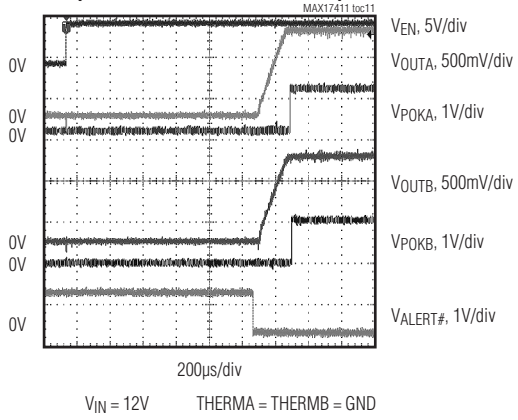
REG A SWITCHING FREQUENCY vs. LOAD CURRENT (SVID = 0.65V)



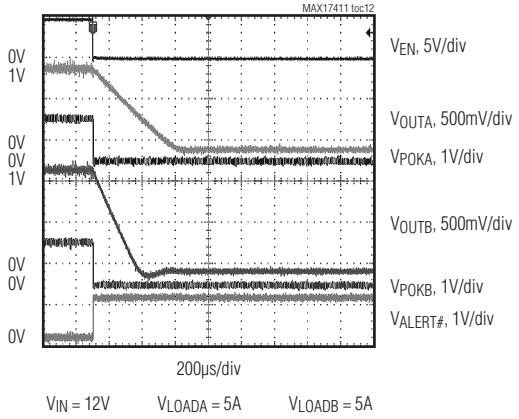
REG B SWITCHING FREQUENCY vs. LOAD CURRENT (SVID = 0.65V) (MAX17511/C/N/T ONLY)



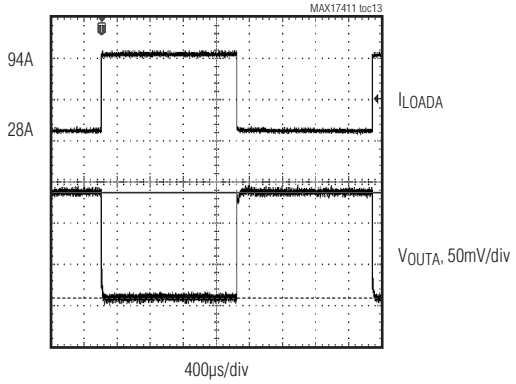
NON-ZERO V_{BOOT} STARTUP WAVEFORMS (V_{BOOT}, 1.05V) (MAX17511/MAX17511T ONLY)



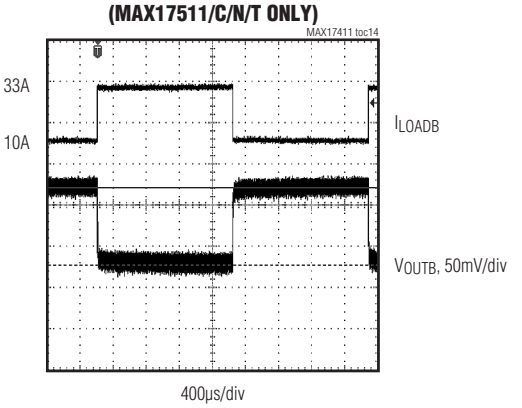
SHUTDOWN WAVEFORMS



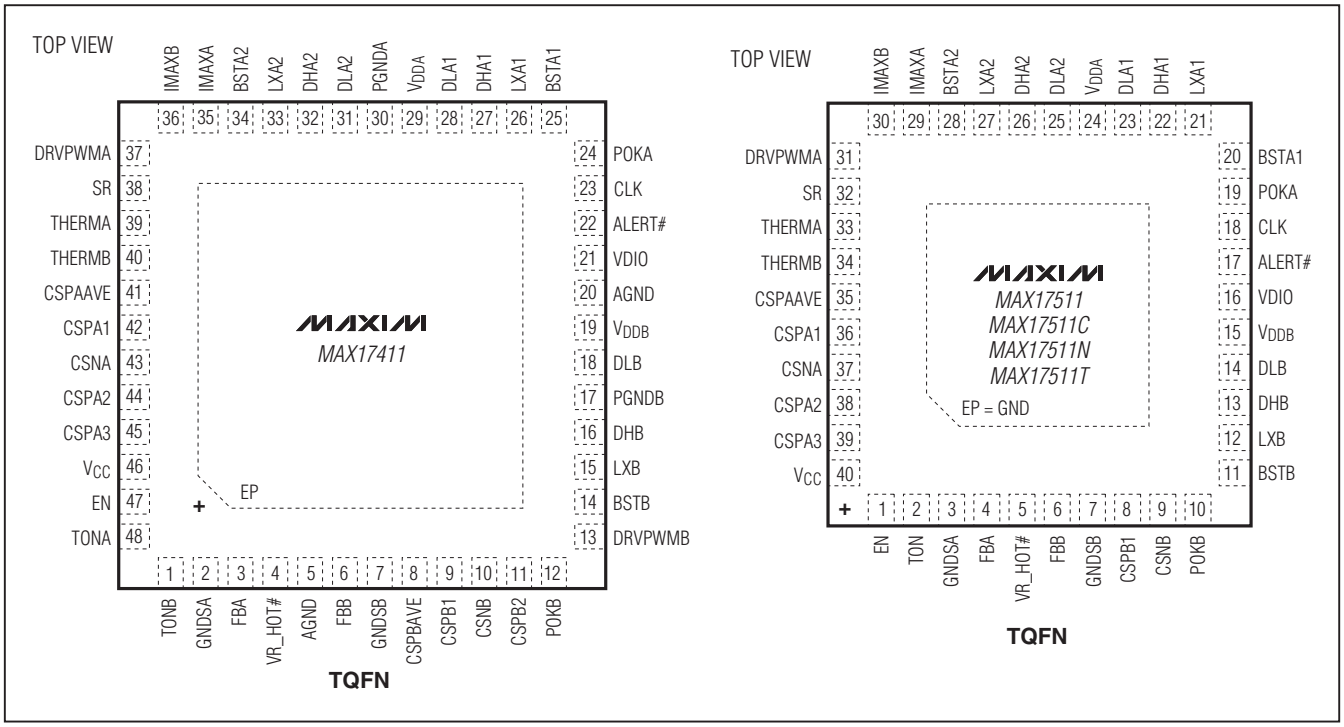
REG A LOAD-TRANSIENT RESPONSE



REG B LOAD-TRANSIENT RESPONSE (MAX17511/C/N/T ONLY)



Pin Configurations



Pin Description

PIN		NAME	FUNCTION
MAX17411	MAX17511/ MAX17511C/ MAX17511N/ MAX17511T		
1	—	TONB	Switching Frequency Adjustment Input for Regulator B. An external resistor between the input power source and TONB sets the switching period (per phase) for regulator B according to the following equation: $t_{SWB} = (R_{TONB} + 6.5k\Omega) \times 14.6pF$ where $f_{SWB} = 1/t_{SWB}$ is the nominal switching frequency. TONB is high-impedance in shutdown. If REG B is disabled, connect TONB to GND or V_{CC}.
—	2	TON	Switching Frequency Adjustment Input for Both Regulators. An external resistor between the input power source and TON sets the switching period (per phase) according to the following equations: $t_{SWA} = (2 \times R_{TON} + 6.5k\Omega) \times 17.9pF$ $t_{SWB} = (2 \times R_{TON} + 6.5k\Omega) \times 14.6pF$ where $f_{SW} = 1/t_{SW}$ is the nominal switching frequency. If REG B is disabled: $t_{SWA} = (R_{TON} + 6.5k\Omega) \times 17.9pF$ TON is high-impedance in shutdown.

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

Pin Description (continued)

PIN		NAME	FUNCTION
MAX17411	MAX17511/ MAX17511C/ MAX17511N/ MAX17511T		
2	3	GNDSA	Ground Remote-Sense Input for Regulator A. Connect GNDSA to the ground-sense pin of the CPU located directly at the point of load. GNDSA internally connects to an internal transconductance amplifier that adjusts the output voltage to compensate for voltage drops between the controller analog ground and the load ground.
3	4	FBA	Feedback Remote-Sense Input and Voltage Positioning Transconductance (VPS) Amplifier Output for Regulator A. Connect a resistor (R_{FBA}) between FBA and the positive side of the feedback remote sense (the CPU output remote sense (V_{CC_SENSE})) to set the DC steady-state droop based on the voltage-positioning gain requirement. $$R_{FBA} = (N_{PH} \times R_{DROOP})/(R_{SENSEA} \times G_{MD})$$ where R_{DROOP} is the desired voltage-positioning slope, G_{MD} = 600µS (typ), and R_{SENSEA} is the current-sense resistance with respect to the CSPAAVE to CSNA current-sense inputs. See the *CSP_AVE - CSN_ Inputs* section. FBA is internally connected to the input of an error comparator and an integrator that corrects for output ripple, error comparator offsets, and the ground-sense offset of regulator A as shown in Figure 5. Shorting FBA directly to the output disables voltage positioning, but impacts the stability requirements. Designs that disable voltage positioning require a higher minimum output capacitance ESR to maintain stability (see the *Output Capacitor Selection* section). FBA enters a high-impedance state in shutdown.
4	5	VR_HOT#	Open-Drain Output of the Thermal Comparators that monitor THERMA and THERMB. These comparators are wire-ORed with output at VR_HOT#. This output is required as backup to the temperature zone register in the event of an SVID bus failure. The comparator responds to the temperature threshold voltage of 2.5V at THERMA OR THERMB. This threshold is equivalent to the 100% threshold defined in the Temperature-Zone register (12h).
5, 20	—	AGND	Analog Ground

Pin Description (continued)

PIN		NAME	FUNCTION
MAX17411	MAX17511/ MAX17511C/ MAX17511N/ MAX17511T		
6	6	FBB	Feedback Remote-Sense Input and Voltage Positioning Transconductance (VPS) Amplifier Output for Regulator B. Connect a resistor (R_{FBB}) between FBB and the positive side of the feedback remote sense to set the DC steady-state droop based on the voltage-positioning gain requirement. $$R_{FBB} = (N_{PH} \times R_{DROOP})/(R_{SENSEB} \times G_{MD})$$ where R_{DROOP} is the desired voltage-positioning slope, G_{MD} = 600µS (typ), and R_{SENSEB} is the current-sense resistance with respect to the CSPBAVE to CSNB (MAX17411) or CSPB1 - CSNB (MAX17511/MAX17511C/MAX17511N/MAX17511T) current-sense inputs. See the *CSP_AVE – CSN_ Inputs* section. FBB is internally connected to the input of an error comparator and an integrator that corrects for output ripple, error comparator offsets, and the ground-sense offset of regulator B as shown in Figures 6 and 7. Shorting FBB directly to the output disables voltage positioning, but impacts the stability requirements. Designs that disable voltage positioning require a higher minimum output capacitance ESR to maintain stability (see the *Output Capacitor Selection* section). FBB enters a high-impedance state in shutdown.
7	7	GNDSB	Ground Remote-Sense Input for Regulator B. Connect GNDSB to the ground-sense pin of the GFX located directly at the point of load. GNDSB internally connects to an internal transconductance amplifier that adjusts the output voltage to compensate for voltage drops between the controller analog ground and the load ground.
8	—	CSPBAVE	Positive Current-Sense Average Input for Regulator B. Connect CSPBAVE to the positive side of the differential output of external current-sense averaging network. The averaging is achieved by using a resistive summation and current-sense resistors, or by using a parallel DCR sense network with a single NTC thermistor for thermal compensation (see Figure 9). The average current-sense input is used for the load-line and current monitor.
9	8	CSPB1	Positive Current-Sense Input for Regulator B. Connect CSPB1 to the positive side of the current-sense resistor or the DCR sense filter capacitor of regulator B as shown in Figure 8. To *completely* disable Regulator B, Connect CSPB1 and CSPB2 to V_{CC}. Also leave BSTB, DHB, LXB, DLB, CSPBAVE, and CSNB unconnected. Address 1 is disabled from the SVID bus.
10	9	CSNB	Negative Current-Sense Input of Regulator B. Connect CSNB to the negative side of the current-sense element as shown in Figure 8. An internal 20Ω discharge MOSFET between CSNB and ground is enabled under an input UVLO or shutdown condition. A bypass capacitor between CSNB and GND in the range of 1nF to 0.1µF is recommended.

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

Pin Description (continued)

PIN		NAME	FUNCTION
MAX17411	MAX17511/ MAX17511C/ MAX17511N/ MAX17511T		
11	—	CSPB2	Positive Current-Sense Input for Second Phase of Regulator B. Connect CSPB2 to the positive side of the current-sense element of the second phase of regulator B as shown in Figure 8.Connect CSPB2 to V_{CC} and leave DRVPWMB unconnected to disable the second phase of Regulator B.
12	10	POKB	Open-Drain Power-Good Output for Regulator B. During soft-start and shutdown, POKB stays low. At the end of soft-start, approximately 20µs (typ) after FBB reaches the output voltage set by the VID code, POKB becomes high-impedance and remains high-impedance as long as FBB is in regulation. POKB is blanked high-impedance when the slew-rate controller for regulator B is active (VID transition occurs). In pulse-skipping mode, the upper POKB threshold is blanked during downward transitions until the output voltage reaches its regulation value.POKB is forced low in shutdown (EN = GND) and after any fault condition is detected on either regulator.To obtain a logic signal, pull up POKB with an external resistor connected to a positive logic supply of +5V and lower.
13	—	DRVPWMB	Direct-Drive PWM Output for Controlling the External Second Phase Driver for Regulator B. DRVPWMB is three-stated in shutdown when the controller detects an output overvoltage fault condition on regulator B.
14	11	BSTB	Boost Flying Capacitor Connection for High-Side Gate Voltage for the First Phase of Regulator B. Connect a ceramic capacitor between BSTB and LXB. See the *Boost Capacitors* section.
15	12	LXB	Inductor Connection for the First Phase of Regulator B. LXB serves as the lower supply rail for the DHB high-side gate driver. LXB is also used as an input to the zero-crossing comparator for regulator B.
16	13	DHB	High-Side Gate-Driver Output for Regulator B. DHB output voltage swings from V_{BSTB} to V_{LXB}. DHB is pulled low in shutdown.
17	—	PGNDB	Power Ground of the Low-Side Driver of Regulator B
18	14	DLB	Low-Side Gate-Driver Output for the First Phase of Regulator B. DLB output voltage swings from V_{DDB} to GND. DLB is forced high when the controller detects an output overvoltage fault condition on regulator B. DLB is forced low in shutdown and in pulse-skipping mode when an inductor current zero crossing (LXB - GND) is detected.
19	15	V_{DDB}	Driver-Supply Voltage Input for Regulator B. V_{DDB} provides power for the low-side driver of regulator B and is used to recharge the BSTB flying capacitor during the on-time of DLB. Connect V_{DDB} to the 4.5V to 5.5V system supply voltage. Bypass V_{DDB} to power ground with a 1µF or greater ceramic capacitor.
21	16	VDIO	Serial VID Input/Output
22	17	ALERT#	Serial VID Alert Output. ALERT# is in the high state in shutdown.
23	18	CLK	Serial VID Clock Input

Pin Description (continued)

PIN		NAME	FUNCTION
MAX17411	MAX17511/ MAX17511C/ MAX17511N/ MAX17511T		
24	19	POKA	Open-Drain Power-Good Output for Regulator A. During soft-start and shutdown, POKA stays low. At the end of soft-start, approximately 20µs (typ) after FBA reaches the output voltage set by the VID code, POKA becomes high-impedance and remains high-impedance as long as FBA is in regulation. POKA is blanked high-impedance when the slew-rate controller for regulator A is active (VID transition occurs). In pulse-skipping mode, the upper POKA threshold is blanked during downward transitions until the output voltage reaches its regulation value. POKA is forced low in shutdown (EN = GND) and after any fault condition is detected on either regulator. To obtain a logic signal, pull up POKA with an external resistor connected to a positive logic supply of +5V and lower.
25	20	BSTA1	Boost Flying Capacitor Connection for High-Side Gate Voltage for the First Phase of Regulator A. Connect a ceramic capacitor between BSTA1 and LXA1. See the *Boost Capacitors* section.
26	21	LXA1	Inductor Connection for the First Phase of Regulator A. LXA1 serves as the lower supply rail for the DHA1 high-side gate driver. LXA1 is also used as an input to the zero-crossing comparator for regulator A.
27	22	DHA1	High-Side Gate-Driver Output for the First Phase of Regulator A. DHA1 output voltage swings from V_{BSTA1} to V_{LXA1}. DHA1 is pulled low in shutdown.
28	23	DLA1	Low-Side Gate-Driver Output for the First Phase of Regulator A. DLA1 output voltage swings from V_{DDA} to V_{GND}. DLA1 is forced high when the controller detects an output overvoltage fault condition on regulator A. DLA1 is forced low in shutdown and in pulse-skipping mode when an inductor current zero crossing (LXA1 - GND) is detected.
29	24	V_{DDA}	Driver Supply Voltage Input for Regulator A. V_{DDA} is the driver supply voltage used for the DLA_ low-side drivers, and to recharge the BSTA_ flying capacitors when the corresponding DLA_s are high. Connect V_{DDA} to the 4.5V to 5.5V system supply voltage. Bypass V_{DDA} to power ground with a 1µF or greater ceramic capacitor.
30	—	PGNDA	Power Ground of the Low-Side Drivers of Regulator A.
31	25	DLA2	Low-Side Gate-Driver Output for the Second Phase of Regulator A. DLA2 Output Voltage swings from V_{DDA} to V_{GND}. DLA2 is forced high when the controller detects an output overvoltage fault condition on regulator A. DLA2 is forced low in shutdown and in pulse-skipping mode when an inductor current zero crossing (LXA2 - GND) is detected.
32	26	DHA2	High-Side Gate-Driver Output for the Second Phase of Regulator A. DHA2 Output Voltage swings from V_{BSTA2} to V_{LXA2}. DHA2 is pulled low in shutdown.
33	27	LXA2	Inductor Connection for the Second Phase of Regulator A. LXA2 serves as the lower supply rail for the DHA2 high-side gate driver. LXA2 is also used as an input to the zero crossing comparator for Regulator A.

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

Pin Description (continued)

PIN		NAME	FUNCTION
MAX17411	MAX17511/ MAX17511C/ MAX17511N/ MAX17511T		
34	28	BSTA2	Boost Flying Capacitor Connection for High-Side Gate Voltage for the Second Phase of Regulator A. Connect a ceramic capacitor between BSTA2 and LXA2. See the *Boost Capacitors* section.
35	29	IMAXA	Maximum Current Threshold for Regulator A. This multivalued logic input sets the valley current limit and compensates for inductor DCR. The maximum output current value in register 21h is determined by the number of phases times the maximum output current per phase set by IMAXA. If the voltage applied to IMAXA is not within the defined threshold, the MAX17411/MAX17511/MAX17511C/ MAX17511N/MAX17511T detect a fault and latch off. See Table 6 for more details.
36	30	IMAXB	Maximum Current Threshold for Regulator B. This multivalued logic input sets the valley current limit and compensates for inductor DCR. The maximum output current value in register 21h is determined by the number of phases times the maximum output current per phase set by IMAXB. If the voltage applied to IMAXB is not within the defined threshold, the MAX17411/MAX17511/MAX17511C/ MAX17511N/MAX17511T detect a fault and latch off. See Table 6 for more details.
37	31	DRVPWMA	Direct-Drive PWM Output for Controlling the External Third Phase Driver for Regulator A. DRVPWMA is three-stated in shutdown when the controller detects an output overvoltage fault condition on regulator A.
38	32	SR	Fast Slew-Rate Adjustment for Both Regulators. The SR setting determines the value stored in the Slew Rate Fast (24h) and Slew Rate Slow (25h) registers. The input uses a four-level voltage sense to determine the slew rate setting upon power-up and if NTC are used for the CSP_ signals. The SR values in the registers (24h and 25h) change accordingly.

SR THRESHOLD (V)	SR (min) (mV/µs)	NTC
0	10	Yes
1.5	20	Yes
3	20	No
V_{CC}	10	No

39	33	THERMA	Thermal-Sense Input for Regulator A. Connect THERMA to a resistor/thermistor-divider network between V_{CC} and THERMA to analog ground. The VR_HOT# is pulled low when the voltage at THERMA or THERMB drops below 0.5 x V_{CC}. If THERMA is held low at startup, REG A is forced in to non-zero V_{BOOT} mode with an output voltage of 1.05V (MAX17411/MAX17511/MAX17511T).
40	34	THERMB	Thermal-Sense Input for Regulator B. Connect THERMB to a resistor/thermistor-divider network between V_{CC} and THERMB to analog ground. The VR_HOT# is pulled low when the voltage at THERMA or THERMB drops below 0.5 x V_{CC}. If THERMB is held low at startup, REG B is forced in to non-zero V_{BOOT} mode with a output voltage of 1.05V (MAX17411/MAX17511/MAX17511T).
41	35	CSPAAVE	Positive Current-Sense Average Input for Regulator A. Connect CSPAAVE to the positive side of the differential output of external current-sense averaging network. The averaging is achieved by using a resistive summation and current-sense resistors, or by using a parallel DCR sense network with a single NTC thermistor for thermal compensation (see Figures 1, 2, and 3). The average current-sense input is used for the load-line and current monitor.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX17411	MAX17511/ MAX17511C/ MAX17511N/ MAX17511T		
42	36	CSPA1	Positive Current-Sense Input for the First Phase of Regulator A. Connect CSPA1 to the positive side of the current-sense resistor or the DCR sense filter capacitor of regulator A as shown in Figure 8. To *completely* disable Regulator A, connect CSPA1, CSPA2, and CSPA3 to V_{CC} and leave BSTA1, DHA1, LXA1, DLA1, CSPAAVE, and CSNA unconnected. Address 0 is also disabled from the SVID bus.
43	37	CSNA	Negative Current-Sense Input of Regulator A. Connect CSNA to the negative side of the current-sense element as shown in Figure 8. An internal 20Ω discharge MOSFET between CSNA and ground is enabled under an input UVLO or shutdown condition. A bypass capacitor between CSNA and GND in the range of 1nF to 0.1µF is recommended.
44	38	CSPA2	Positive Current-Sense Input for the Second Phase of Regulator A. Connect CSPA2 to the positive side of the current-sense resistor or the DCR sense filter capacitor of regulator A as shown in Figure 8. To *completely* disable Regulator A, connect CSPA1, CSPA2, and CSPA3 to V_{CC}. Address 0 is also disabled from the SVID bus. When Phase 2 is disabled, leave BSTA2, DHA2, LXA2, and DLA2 unconnected. If phase 2 is disabled, phase 3 must be disabled as well.
45	39	CSPA3	Positive Current-Sense Input for Third Phase of Regulator A. Connect CSPA3 to the positive side of the current-sense element of the third phase of regulator A as shown in Figure 8. Connect CSPA3 to V_{CC} and leave DRVPWMA unconnected to disable the third phase of Regulator A.
46	40	V_{CC}	Analog Supply Voltage. Connect to a filtered 4.5V to 5.5V source. Bypass V_{CC} to AGND with a 1µF or greater ceramic capacitor.
47	1	EN	Controller Enable Input. Pull EN high or connect EN to V_{CC} for normal operation. Connect to ground to put the controller into its 30µA (max) shutdown state. During soft-start, the controller slowly ramps the output voltage up to the boot voltage with a 2.5mV/µs (min) slew rate. During the transition from normal operation to shutdown, the output is discharged through a 20Ω internal CSN_ FET. Toggling EN resets the fault latches. EN cannot withstand the battery voltage.
48	—	TONA	Switching Frequency Adjustment Input for Regulator A. An external resistor between the input power source and TONA sets the switching period (per phase) for regulator A according to the following equation: $t_{SWA} = (R_{TONA} + 6.5k\Omega) \times 17.9pF$ where $f_{SWA} = 1/t_{SWA}$ is the nominal switching frequency. TONA is high-impedance in shutdown. If REG A is disabled, connect TONA to GND.
EP	—	PAD (AGND)	Exposed Pad. Connect EP to the ground plane with thermally enhanced vias.
—	EP	PAD (GND)	Exposed Pad. Connect EP to the ground plane with thermally enhanced vias. Power ground pads and analog ground pads are all internally connected to the exposed pad.

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

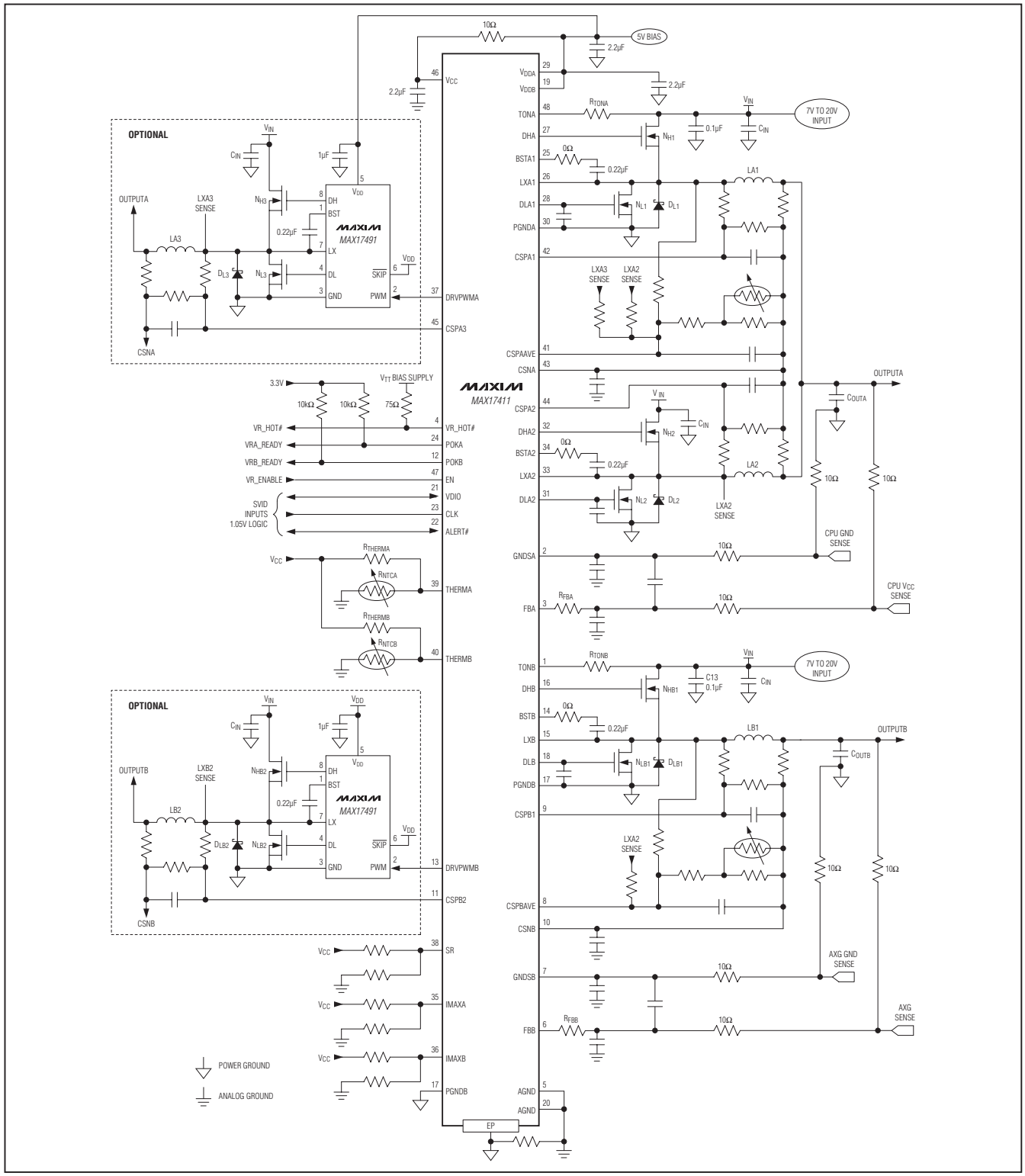


Figure 1. MAX17411 Typical CPU Core Application Circuit

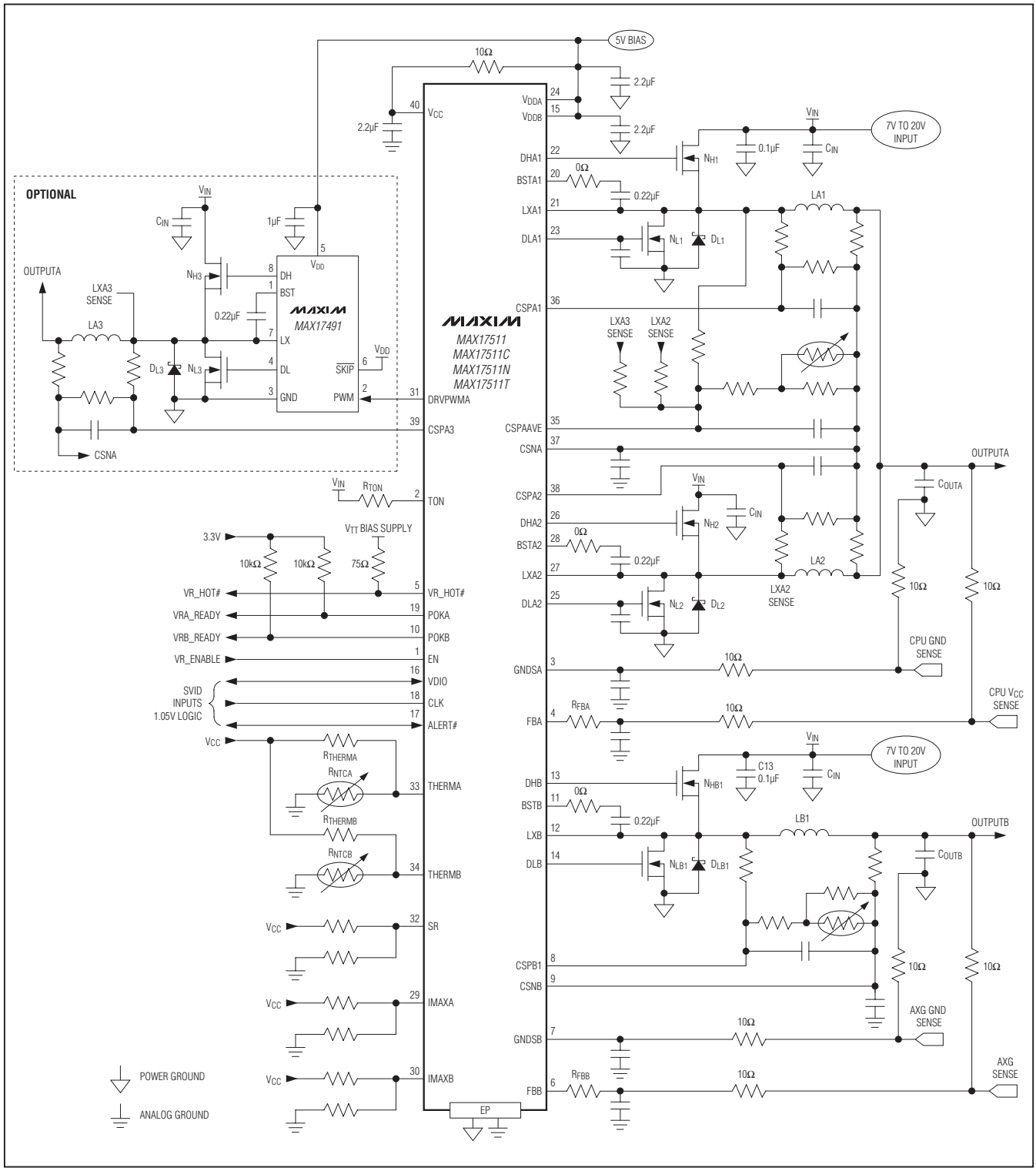


Figure 2. MAX17511 Typical Application Circuit (3-Phase + 1-Phase)

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

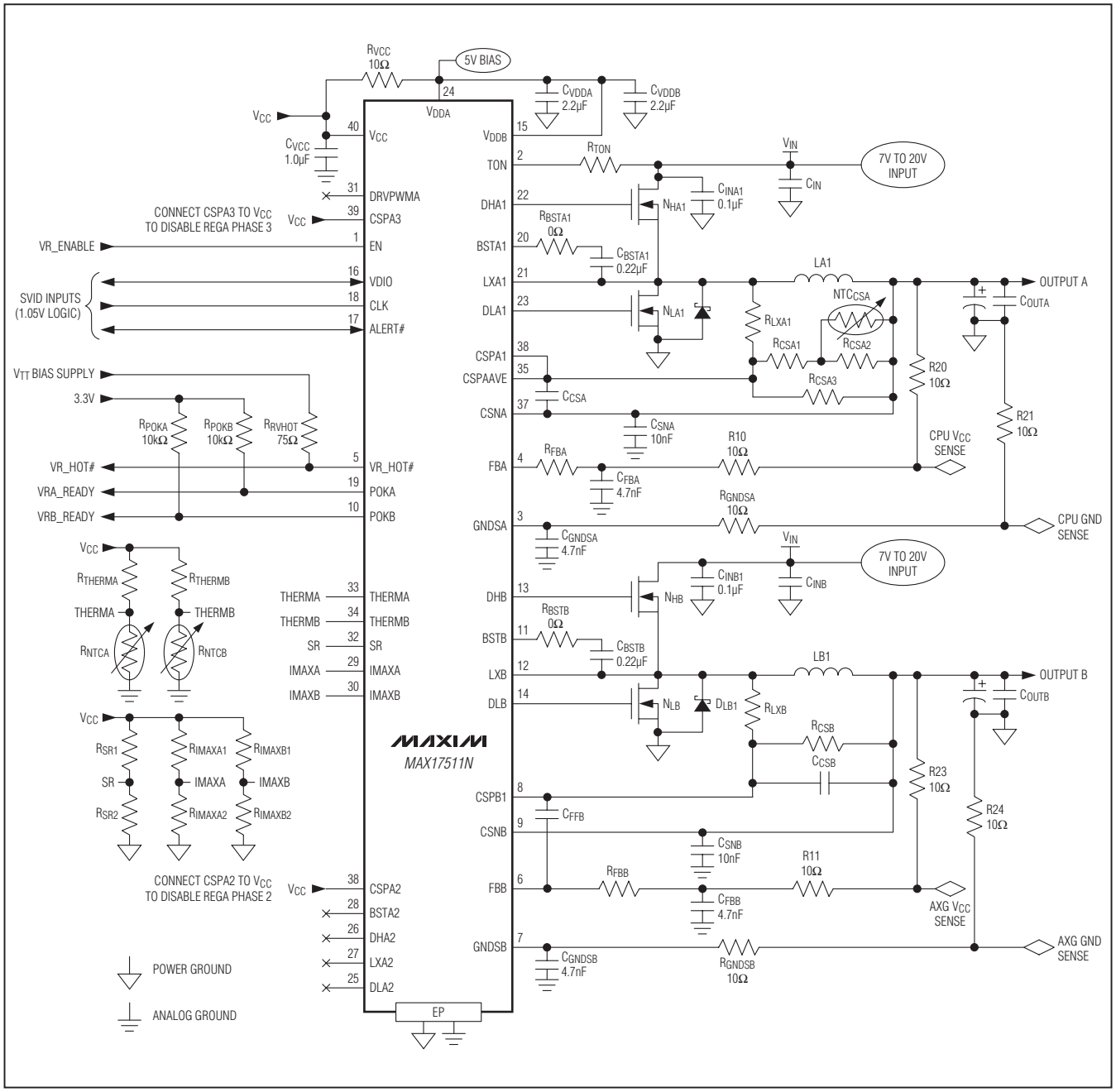


Figure 3. MAX17511N Typical Application Circuit (1-Phase + 1-Phase)

Table 1. Regulator A Typical Component Values (refer to the MAX17411/MAX17511 Evaluation Kit)

COMPONENT	REF	QTY	VR12/IMVP-7 ATOM CPU, TDC = 3.3A/ I_{CCMAX} = 6A 410kHz OPERATION (Figure 3)	VR12/IMVP-7 SV CPU TDC = 36A/ I_{CCMAX} = 53A 325kHz OPERATION (Figures 1 and 2)	VR12/IMVP-7 XE CPU TDC = 52A/ I_{CCMAX} = 94A 325kHz OPERATION (Figures 1 and 2)
Conditions	—	—	V_{IN} = 7V to 20V, SVID = 1.1V	V_{IN} = 7V to 20V, SVID = 1.05V	V_{IN} = 7V to 20V, SVID = 0.9V
Phases	—	—	1	2	3
High-Side FET	$N_{H_}$	1 per phase	Fairchild FDMS7602S	Fairchild FDMS7680 Vishay (Siliconix) SiR462DP	Fairchild FDMS7680 Vishay (Siliconix) SiR462DP
Low-Side FET	$N_{L_}$	2 per phase	Fairchild FDMS76702S 1 per phase	Fairchild FDMS7670AS Vishay (Siliconix) Sir158DP	Fairchild FDMS7670AS Vishay (Siliconix) Sir158DP
Schottky Diode	$D_{L_}$	None; most applications do not use Schottkys	None	None	None
Sense Resistor	$R_{SENSE_}$	None; most applications use DCR sensing	0.75mΩ, 1%, 1W Cyntec Co. RL1632L4-0R75m-FNH	0.75mΩ, 1%, 1W Cyntec Co. RL1632L4-0R75m-FNH	0.75mΩ, 1%, 1W Cyntec Co. RL1632L4-0R75m-FNH
Inductor	$L_$	1 per phase	1.5µH, 8A, 4.5mΩ power inductor TOKO FDVE0630-1R5M	0.36µH, 36A, 0.82mΩ power inductor Panasonic ETQP4LR36AFC	0.36µH, 36A, 0.82mΩ power inductor Panasonic ETQP4LR36AFC
Output Capacitors	$C_{OUT_}$	Total	1x 470µF, 2V, 4.5mΩ low-ESR Panasonic EEFSX0D471E4	4x 470µF, 2V, 4.5mΩ low-ESR polymer capacitor (D case) Panasonic EEFSX0D471E4 or Sanyo 2TPW470M4R +18 x 22µF + 10 x 10µF ceramic	4x 470µF, 2V, 4.5mΩ low-ESR polymer capacitor (D case) Panasonic EEFSX0D471E4 or Sanyo 2TPW470M4R +18 x 22µF + 10 x 10µF ceramic
Input Capacitors	$C_{IN_}$	Total	10µF, 25V, X5R ceramic capacitor	10µF, 25V, X5R ceramic capacitors 3 per phase	10µF, 25V, X5R ceramic capacitors 3 per phase
Switching Frequency	R_{TON}	1	64.9kΩ, 1% (410kHz) for the (MAX17511/ MAX17511C/ MAX17511N/MAX17511T)	180kΩ, 1% (300kHz) for the MAX17411, 82.5kΩ, 1% (325kHz) for the (MAX17511/MAX17511C/ MAX17511N/MAX17511T)	180kΩ, 1% (300kHz) for the MAX17411, 82.5kΩ, 1% (325kHz) for the (MAX17511/MAX17511C/ MAX17511N/MAX17511T)
Slew Rate	—	—	V_{SR} = 5V 10mV/µs	V_{SR} = 5V 10mV/µs	V_{SR} = 5V 10mV/µs
FB_ Droop Setting	R_{FBA}	1	2.15kΩ, 1% (droop = -5.9mV/A)	8.66kΩ, 1% (droop = -1.9mV/A)	13kΩ, 1% (droop = -1.9mV/A)

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

Table 1. Regulator A Typical Component Values (refer to the MAX17411/MAX17511 Evaluation Kit) (continued)

COMPONENT	REF	QTY	VR12/IMVP-7 ATOM CPU, TDC = 3.3A/ I_{CCMAX} = 6A 410kHz OPERATION (Figure 3)	VR12/IMVP-7 SV CPU TDC = 36A/ I_{CCMAX} = 53A 325kHz OPERATION (Figures 1 and 2)	VR12/IMVP-7 XE CPU TDC = 52A/ I_{CCMAX} = 94A 325kHz OPERATION (Figures 1 and 2)
THERMA Setting	R_{THERMA}, R_{NTC}	—	5.62kΩ, 1% + 100kΩ, 5% NTC thermistor B = 4250 (0603) Murata NCP18WF104J03RB TDK NTCG163JF104J (0402) or Panasonic ERT-J1VR104J	5.62kΩ, 1% +100kΩ, 5% NTC thermistor B = 4250 (0603), Murata NCP18WF104J03RB, TDK NTCG163JF104J (0402) or Panasonic ERT-J1VR104J	5.62kΩ, 1% + 100kΩ, 5% NTC thermistor B = 4250 (0603) Murata NCP18WF104J03RB TDK NTCG163JF104J (0402) or Panasonic ERT-J1VR104J

Table 2. Regulator B Typical Component Values (refer to the MAX17411/MAX17511 Evaluation Kit)

COMPONENT	REF	QTY	VR12/IMVP-7 GT; TDC = 1.4A/ I_{CCMAX} = 2.5A; 500kHz OPERATION (MAX17511/MAX17511C/ MAX17511N/MAX17511T) (Figure 3)	VR12/IMVP-7 GT; TDC = 21.5A/; I_{CCMAX} = 33A; 400kHz OPERATION (MAX17511/MAX17511C/ MAX17511N/MAX17511T) (Figure 2)	VR12/IMVP-7 GT; TDC = 40A/; I_{CCMAX} = 66A; 370kHz OPERATION (MAX17411) (Figure 1)
Conditions	—	—	V_{IN} = 7V to 20V SVID = 1.23V	V_{IN} = 7V to 20V SVID = 1.23V	V_{IN} = 7V to 20V SVID = 1.23V
Phases	—	—	1	1	2
High-Side FET	$N_{H_}$	1 per phase	Fairchild FDMC8200	Fairchild FDMS7680 Vishay (Siliconix) SiR462DP	Fairchild FDMS7680 Vishay (Siliconix) SiR462DP
Low-Side FET	$N_{L_}$	—	Fairchild FDMC8200 1 per phase	Fairchild FDMS7670AS Vishay (Siliconix) Sir158DP 2 per phase	Fairchild FDMS7670AS Vishay (Siliconix) Sir158DP 2 per phase
Schottky Diode	$D_{L_}$	None; most applications do not use Schottkys	3A, 40V Schottky diode Diodes Inc B340LB-13-F	3A, 40V Schottky diode Diodes Inc. B340LB-13-F	3A, 40V Schottky diode Diodes Inc B340LB-13-F
Sense Resistor	$R_{SENSE_}$	None; most applications use DCR sensing	0.75mΩ, 1%, 1W Cyntec Co. RL1632L4-0R75m-FNH	0.75mΩ, 1%, 1W Cyntec Co. RL1632L4-0R75m-FNH	0.75mΩ, 1%, 1W Cyntec Co. RL1632L4-0R75m-FNH
Inductor	$L_$	1 per phase	3.3µH, 5.5A, 29.6mΩ TOKO: FDV0530-3R3M	0.36µH, 36A, 0.82mΩ power inductor Panasonic ETQP4LR36AFC	0.36µH, 36A, 0.82mΩ power inductor Panasonic ETQP4LR36AFC

Table 2. Regulator B Typical Component Values (refer to the MAX17411/MAX17511 Evaluation Kit) (continued)

COMPONENT	REF	QTY	VR12/IMVP-7 GT; TDC = 1.4A/I_{CCMAX} = 2.5A; 500kHz OPERATION (MAX17511/MAX17511C/ MAX17511N/MAX17511T) (Figure 3)	VR12/IMVP-7 GT; TDC = 21.5A; I_{CCMAX} = 33A; 400kHz OPERATION (MAX17511/MAX17511C/ MAX17511N/MAX17511T) (Figure 2)	VR12/IMVP-7 GT TDC = 40A/I_{CCMAX} = 66A 370kHz OPERATION (MAX17411) (Figure 1)
Output Capacitors	$C_{OUT_}$	Total	1 x 100µF + 47µF ceramic	2 x 470µF, 2V, 4.5mΩ low-ESR polymer capacitor (D case) Panasonic EEFSX0D471E4 or NEC/ TOKIN PSGV0E477M4.5 +14 x 22µF ceramic	3 x 470µF, 2V, 4.5mΩ low-ESR polymer capacitor (D case) Panasonic EEFSX0D471E4 or NEC/TOKIN PSGV0E477M4.5 +14 x 22µF ceramic
Input Capacitors	$C_{IN_}$	Total	10µF, 25V, X5R ceramic	4 x 10µF, 25V, X5R ceramic capacitors	3 x 10µF, 25V, X5R ceramic capacitors per phase
Switching Frequency	R_{TON}	1	64.9kΩ, 1% (500kHz)	82.5kΩ, 1% (400kHz)	180kΩ, 1% (370kHz)
Slew Rate	—	—	V_{SR} = 5V, 10mV/µs	V_{SR} = 5V, 10mV/µs	V_{SR} = 5V, 10mV/µs
FB_ Droop Setting	R_{FBB}	1	100Ω, C_{FFB} = 0.1µF (no DC droop, AC couple signal)	8.66kΩ, 1% (droop = -3.9mV/A)	17.4kΩ, 1% (droop = 3.9mV/A)
THERMB Setting	R_{THERMB}, R_{NTC}	—	5.62kΩ, 1% + 100kΩ, 5% NTC thermistor B = 4250 (0603) Murata NCP18WF104J03RB TDK NTCG163JF104J (0402) or Panasonic ERT-J1VR104J	5.62kΩ, 1% +100kΩ, 5% NTC thermistor B = 4250 (0603) Murata NCP18WF104J03RB TDK NTCG163JF104J (0402) or Panasonic ERT-J1VR104J	5.62kΩ, 1% + 100kΩ, 5% NTC thermistor B = 4250 (0603) Murata NCP18WF104J03RB TDK NTCG163JF104J (0402) or Panasonic ERT-J1VR104J

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

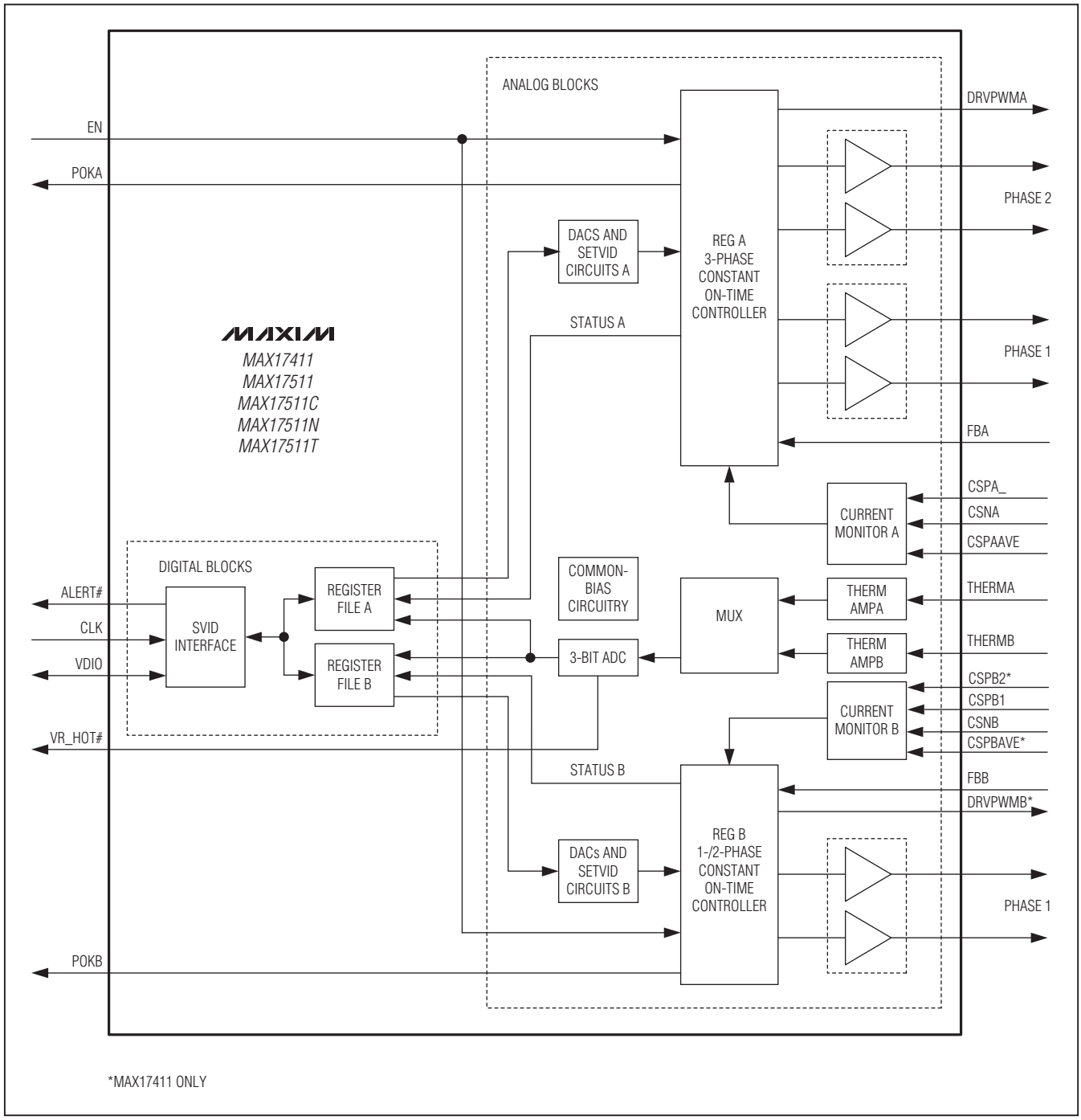
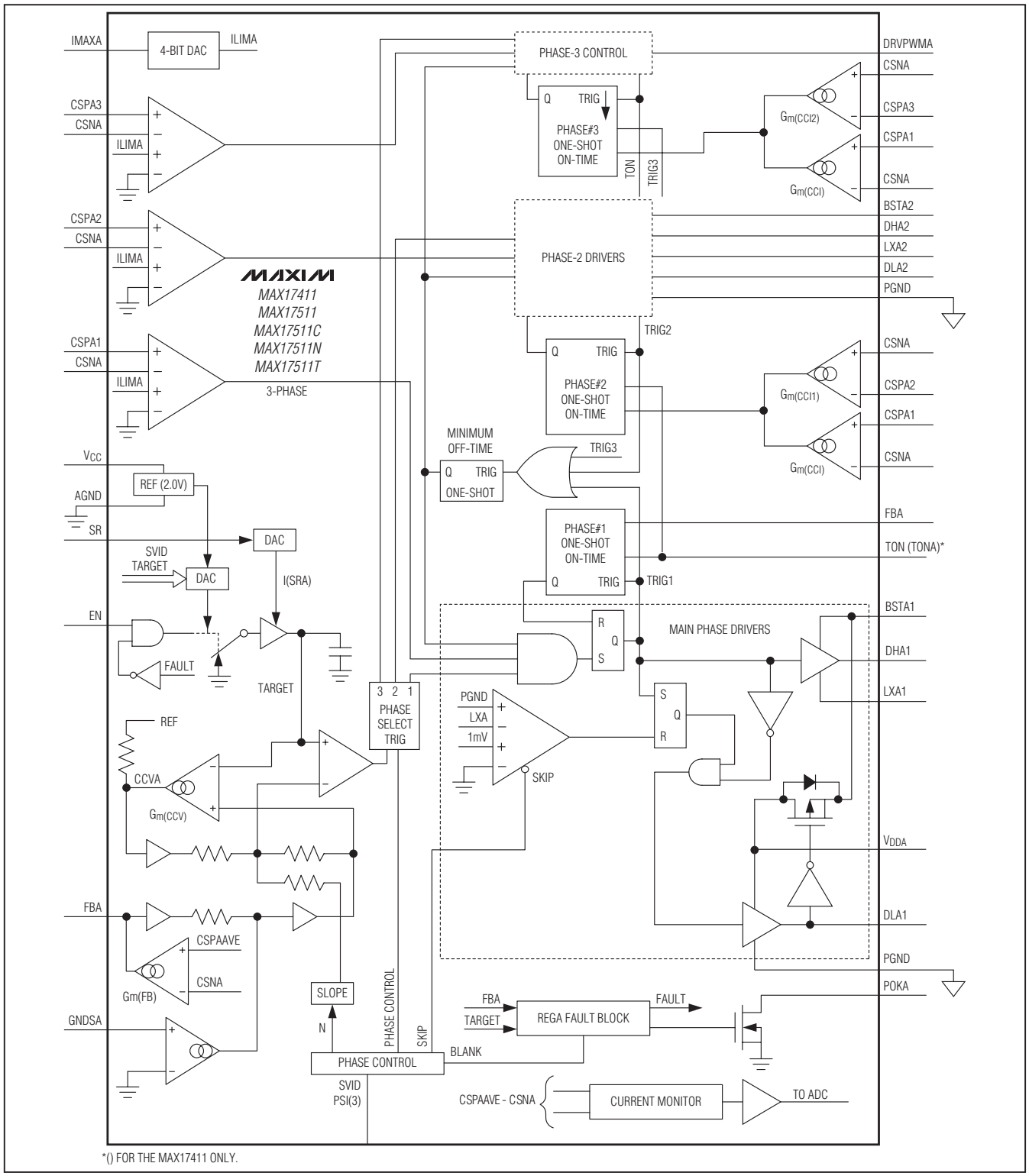


Figure 4. MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T High-Level Block Diagram



*() FOR THE MAX17411 ONLY.

Figure 5. Regulator A Block Diagram with SVID Functions

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

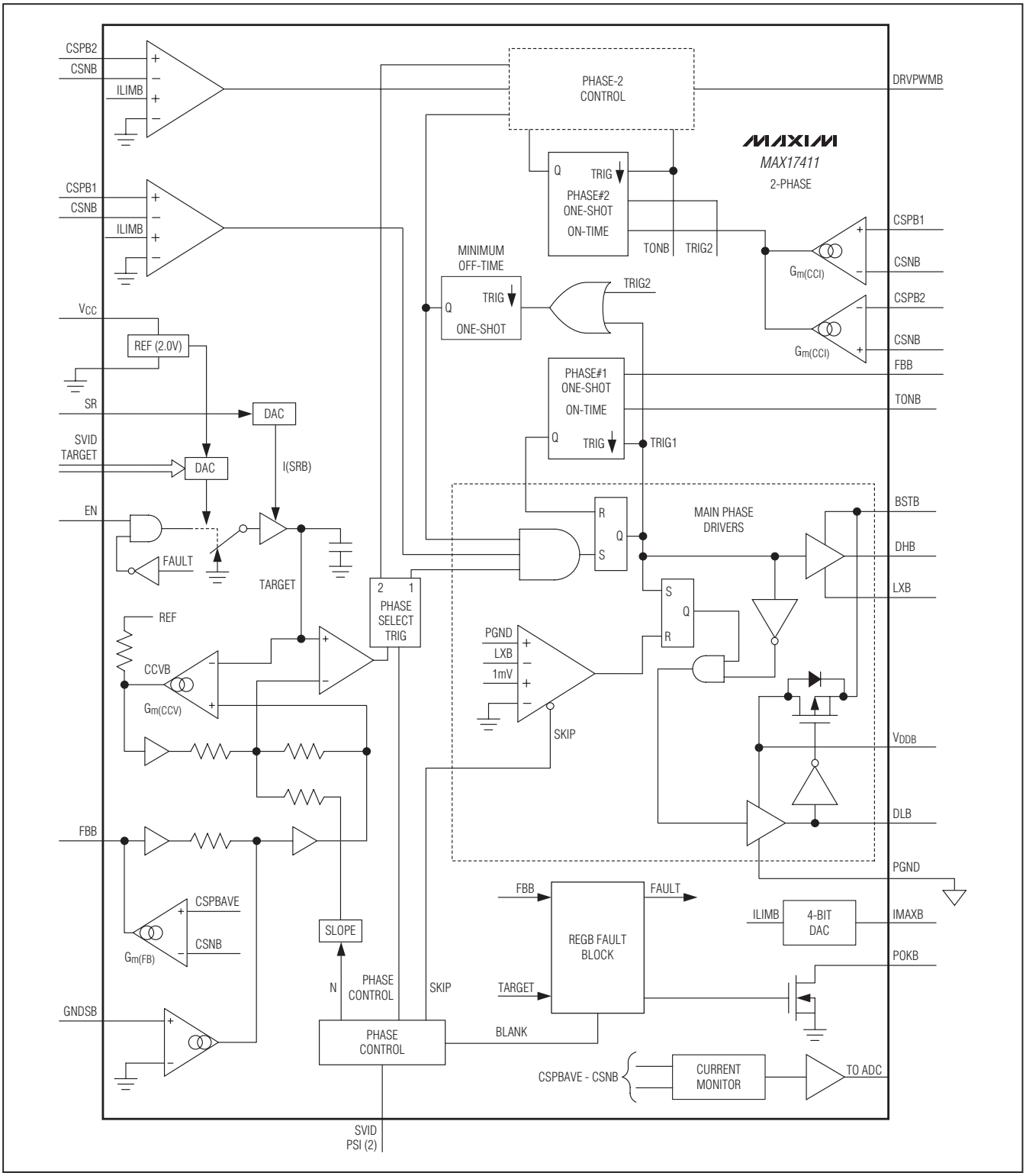


Figure 6. MAX17411 Regulator B Block Diagram with SVID Function

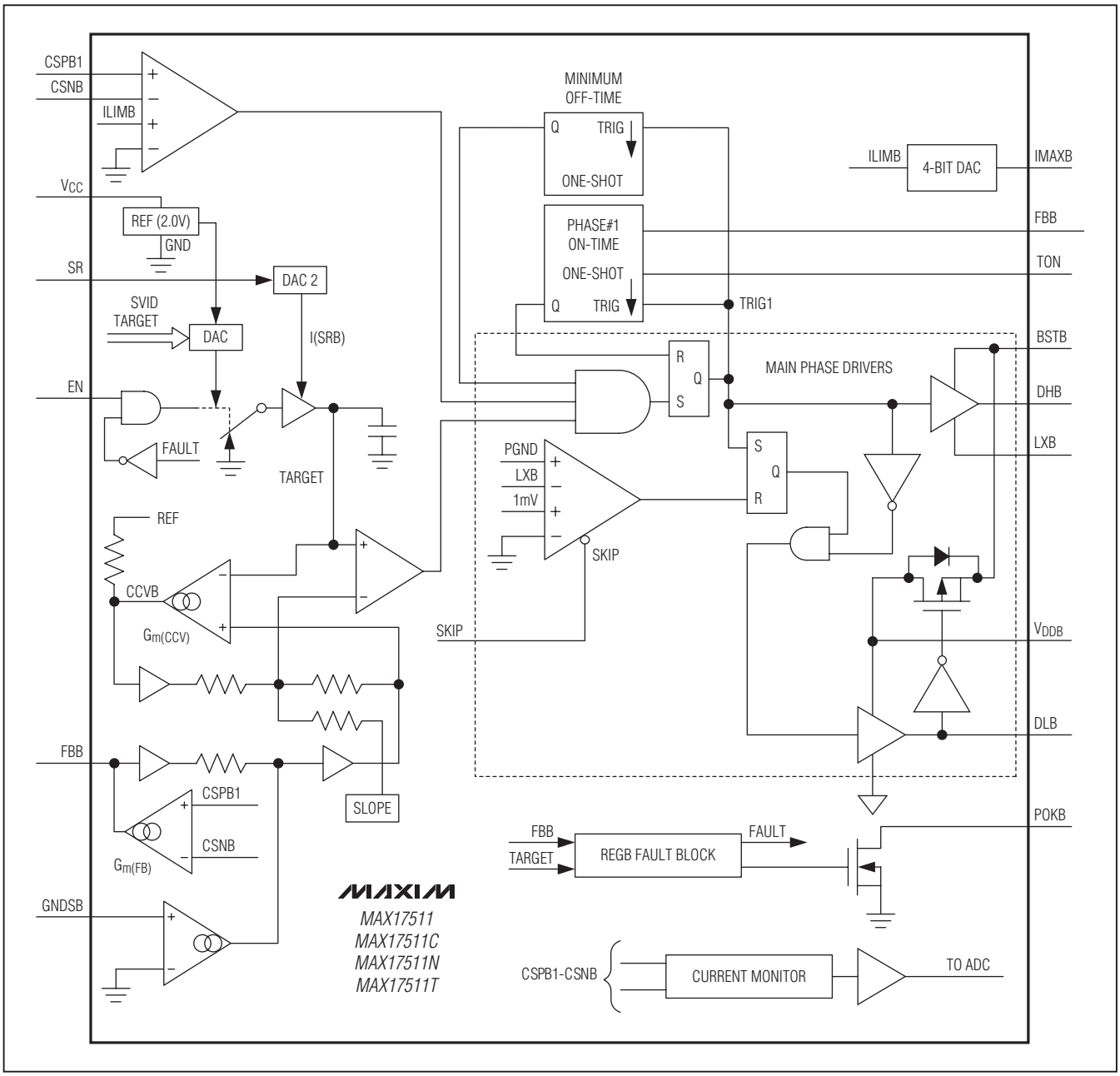


Figure 7. MAX17511/MAX17511C/MAX17511N/MAX17511T Regulator B Block Diagram with SVID Function

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

Detailed Description

The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T are dual-output, step-down, constant on-time controllers for VR12/IMVP-7 CPU core supplies. The controllers consist of two high-current SMPSs for the CPU and GFX cores. The CPU regulator (regulator A, ADDR0) is a three-phase constant on-time architecture. The optional third phase is configured with an external MAX17491 driver. The second GFX regulator (regulator B, ADDR1) is a single-phase (MAX17511/MAX17511C/MAX17511N/MAX17511T) or two-phase (MAX17411) constant on-time architecture. The three-phase CPU core regulator runs 120° out-of-phase for true interleaved operation, minimizing input capacitance. Figure 4 is the high-level block diagram. Table 1 lists typical component values for regulator A, and Table 2 lists typical component values for regulator B.

CPU and GFX outputs are controlled independently by writing the appropriate data into a function-mapped register file. Output voltages are dynamically changed through a 3-wire serial VID interface (3-wire SVID: clock, data, ALERT#), allowing the switching regulators to be individually programmed to different voltages. The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T generate well-controlled technologies between VID codes and automatically soft-start for non-zero V_{BOOT} operation. The SVID interface also allows each regulator to be individually set into a low-power pulse-skipping state. Individual phases can be shut down based on the processors' operating conditions (1- or 3-phase operation is possible under software control). Transient-phase overlap mode improves the current delivery response time of regulator A, which reduces the total output capacitance. Both regulators include active overshoot suppression to reduce the required output decoupling capacitance.

The devices include output overvoltage (MAX17411/MAX17511/MAX17511C/MAX17511N), output undervoltage, and thermal protections. When any of these protection features detects a fault, the controller shuts down both channels. True differential current sensing improves load-line and current-limit accuracy. Both regulators A and B feature programmable switching frequency, allowing 200kHz to 600kHz per phase operation. VR12/IMVP-7 requires temperature measurements for the individual outputs. For this reason, an ADC with MUX is included to digitize the analog variables of interest. A thermistor-based temperature sensor provides a programmable thermal-fault output (VR_HOT#).

Free-Running Constant On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a pseudo-fixed frequency, constant on-time, current-mode regulator with voltage feed-forward (Figures 5, 6, and 7). The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose period is inversely proportional to input voltage, and directly proportional to output voltage or the difference between the main and secondary inductor currents (see the *On-Time One-Shot* section). Another one-shot sets a minimum off-time. The on-time one-shot triggers when the error comparator goes low, the inductor current of the selected phase is below the valley current-limit threshold, and the minimum off-time one-shot times out. Regulator A maintains 120° out-of-phase operation by alternately triggering the three phases after the error comparator drops below the output voltage set point. Two-phase controller (regulator B, MAX17411) maintains 180° out-of-phase operation by alternately triggering the two phases after the error comparator drops below the output-voltage set point.

Triple 120° Out-Of-Phase Operation

The three phases in the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T operate 120° out-of-phase to minimize input and output filtering requirements, reduce electromagnetic interference (EMI), and improve efficiency. This effectively lowers component count—reducing cost, board space, and component power requirements—making these devices ideal for high-power, cost-sensitive applications. The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T share the current between three phases that operate 120° out-of-phase, so the high-side MOSFETs never turn on simultaneously during normal operation. The instantaneous input current of each phase is effectively reduced, resulting in reduced input voltage ripple, ESR power loss, and RMS ripple current (see the *Input Capacitor Selection* section). Therefore, the same performance can be achieved with fewer or less-expensive input capacitors.

Dual 180° Out-Of-Phase Operation (MAX17411 Only)

The two phases in the MAX17411 operate 180° out-of-phase to minimize input and output filtering requirements, reduce EMI, and improve efficiency. This effectively lowers component count—reducing cost, board space, and component power requirements—making this device ideal for high-power, cost-sensitive applications. The MAX17411 shares the current between two phases that operate 180°

out-of-phase, so the high-side MOSFETs never turn on simultaneously during normal operation. The instantaneous input current of each phase is effectively reduced, resulting in reduced input-voltage ripple, ESR power loss, and RMS ripple current (see the *Input Capacitor Selection* section). Therefore, the same performance can be achieved with fewer or less-expensive input capacitors.

+5V Bias Supply (V_{CC}, V_{DDA}, and V_{DDB})

The Quick-PWM controllers require an external 5V bias supply in addition to the battery. Typically, this +5V bias supply is the notebook's 95% efficient 5V system supply. The +5V bias supply must provide V_{CC} (PWM controller) and V_{DDA} and V_{DDB} (gate-drive power). V_{DDA} and V_{DDB} can be shorted together on the PCB. The maximum current drawn from the 5V bias supply is:

$$I_{BIAS} = I_{CC} + f_{SW}(Q_{G(LOW)} + Q_{G(HIGH)})\ I_{REGA} + f_{SW}(Q_{G(LOW)} + Q_{G(HIGH)})\ I_{REGB}$$

where I_{CC} is provided in the *Electrical Characteristics* table, f_{SW} is the switching frequency, and $Q_{G(LOW)}$ and $Q_{G(HIGH)}$ are the MOSFET data sheet's total gate-charge specification limits at V_{GS} = 5V. V_{CC}, V_{DDA}, and V_{DDB} can be connected together if the input power source is a fixed 4.5V to 5.5V supply. If the 5V bias supply is powered up prior to the battery supply, the enable signal (EN going from low to high) must be delayed until the battery voltage is present to ensure startup.

Switching Frequency (TON)

For the MAX17411, connect two resistors (R_{TONA} and R_{TONB}) between TONA and V_{IN} and TONB and V_{IN} to set the switching period $t_{SW_}$ = 1/f_{SW}, per phase:

$$t_{SW_} = C_{TON_} \times (R_{TON_} + 6.5k\Omega)$$

where $C_{TON_}$ = 17.9pF for regulator A and $C_{TON_}$ = 14.6pF for regulator B.

For the MAX17511/MAX17511C/MAX17511N/MAX17511T, connect a resistor (R_{TON}) between TON and V_{IN} to set the switching period t_{SW} = 1/f_{SW}, per phase for both regulator A and regulator B:

$$t_{SWA} = (2 \times R_{TON} + 6.5k\Omega) \times 17.9pF$$

$$t_{SWB} = (2 \times R_{TON} + 6.5k\Omega) \times 14.6pF$$

If the MAX17511 regulator B is disabled, then

$$t_{SWA} = (R_{TON} + 6.5k\Omega) \times 17.9pF$$

High-frequency (600kHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. Low-frequency (200kHz) operation offers the best overall efficiency at the expense of component size and board space.

TON Open-Circuit Protection

The TON inputs include open-circuit protection to avoid long, uncontrolled on-times that could result in an overvoltage condition on the output. The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T detect an open-circuit fault if the TON current drops below 10µA for any reason—the TON resistor (R_{TON}) is unpopulated, a high resistance value is used, the input voltage is low, etc. Under these conditions, the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T stop switching (DH_ and DL_ pulled low) and immediately set the fault latch for both regulator A and regulator B. Toggle EN or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller.

On-Time One-Shot

Regulator A and regulator B contain fast, low-jitter, adjustable one-shots that set the respective high-side MOSFETs on-time. The one-shot timing is shared among the operating phases. The one-shot for the main phase varies the on-time in response to the input and feedback voltages. The main high-side switch on-time is inversely proportional to the input voltage as measured by the V_{IN}, and proportional to the feedback voltage ($V_{FB_}$):

$$t_{ON} = \frac{t_{SW}(V_{FB_} + 0.075V)}{V_{IN}}$$

The one-shot for the second phase and third phase varies the on-time in response to the input voltage and the difference between the main and the other inductor currents. Two identical transconductance amplifiers integrate the difference between the master and each slave's current-sense signals. The respective error signals are used to correct the t_{ON} of the high-side MOSFETs for the 2nd and 3rd phase.

During phase overlap, t_{ON} is calculated based on the on-time requirements of the first phase, but reduced by 33% when operating with three phases. For a three-phase regulator, the third phase cannot be enabled until the other two phases have completed their on-time and the minimum off-times have expired. As such, the minimum period is limited by 3 x (t_{ON} + $t_{OFF(MIN)}$). The maximum t_{ON} is dependent on the minimum input and maximum output voltage:

$$t_{SW(MIN)} = N_{PH} \times (t_{ON(MAX)} + t_{OFF(MIN)})$$

where:

$$t_{ON(MAX)} = \frac{V_{FB_(MAX)}}{V_{IN(MIN)}} \times t_{SW(MIN)}$$

and N_{PH} = total number of active phases.

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So:

$$t_{SW(MIN)} = \frac{t_{OFF(MIN)}}{1/N_{PH} - V_{FB_(MAX)}/V_{IN(MIN)}}$$

Hence, for a 7V input and 1.1V output, the maximum switching frequency is 700kHz. Running at this limit is not desirable since there is no room to allow the regulator to make adjustments without triggering phase overlap. For a three-phase, high-current application with minimum 8V input, the practical switching frequency is 300kHz. On-times translate only roughly to switching frequencies. The on-times guaranteed in the *Electrical Characteristics* table are influenced by parasitics in the conduction paths and propagation delays. For loads above the critical conduction point, where the dead-time effect (LX flying high and conducting through the high-side FET body diode) is no longer a factor, the actual switching frequency (per phase) is:

$$f_{SW} = \frac{(V_{OUT} + V_{DIS})}{t_{ON}(V_{IN} + V_{DIS} + V_{CHG})}$$

where V_{DIS} is the sum of the parasitic voltage drops in the inductor discharge and charge paths, including MOSFET, inductor, and PCB resistances; V_{CHG} is the sum of the parasitic voltage drops in the inductor charge path, including high-side switch, inductor, and PCB resistances, and t_{ON} is the on-time as determined above.

Current Sense

The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T sense the output current of each phase, allowing the use of current-sense resistors or inductor DCR as the current-sense element. Low-offset amplifiers are used for current balance, voltage-positioning gain, and current limit. Using the DC resistance (R_{DCR}) of the output inductor allows higher efficiency. The initial tolerance and temperature coefficient of the inductor's DCR must be accounted for in the output-voltage droop-error budget and current monitor. This current-sense method uses an RC filter network to extract the current information from the output inductor (see Figure 8).

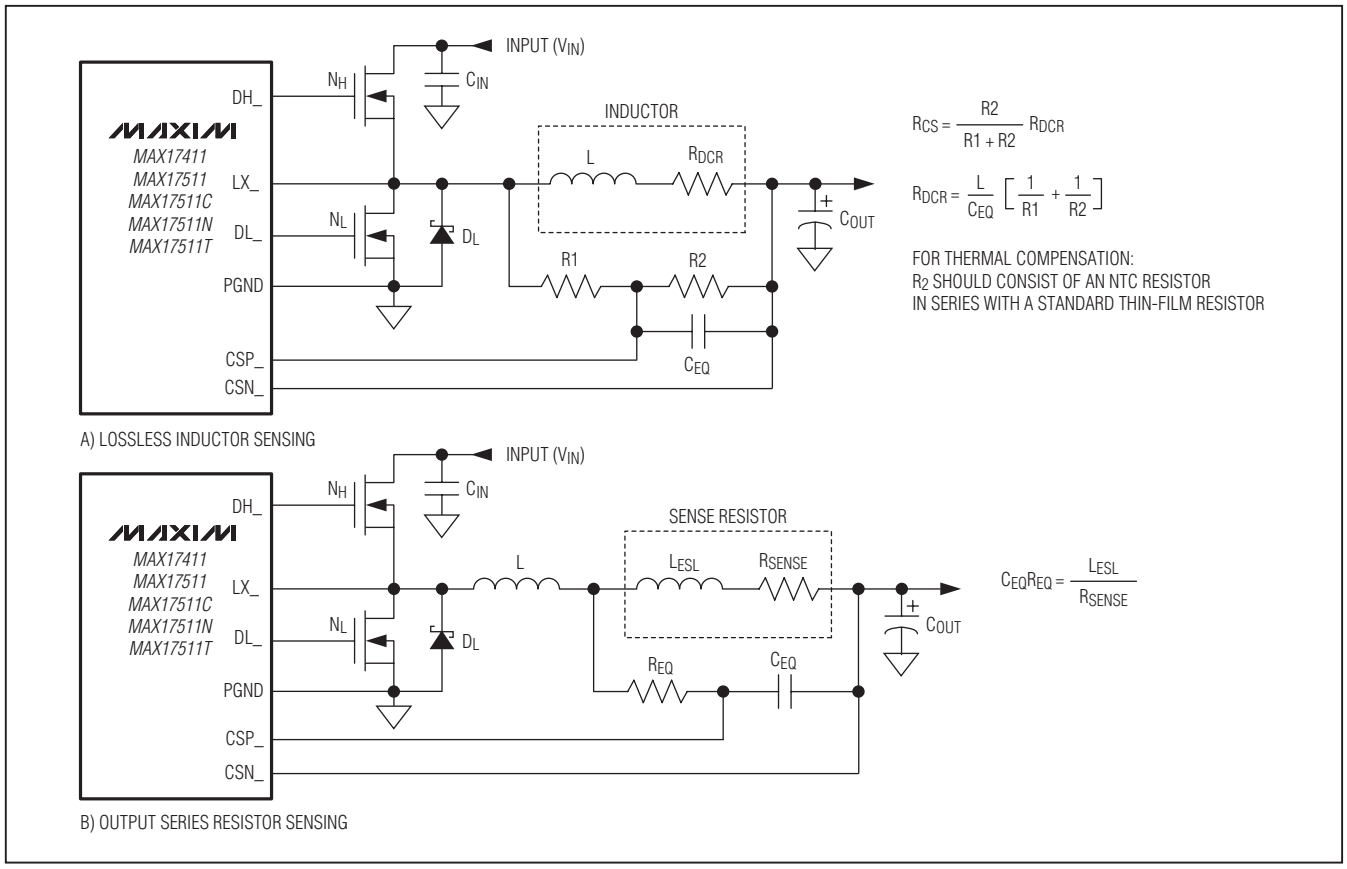

Figure 6. Current-Sense Methods

The RC network should match the time constant of the inductor (L/R_{DCR}):

$$R_{CS} = \left(\frac{R2}{R1+R2}\right) R_{DCR}$$

and:

$$R_{DCR} = \frac{L}{C_{EQ}}\left[\frac{1}{R1}+\frac{1}{R2}\right]$$

where R_{CS} is the required current-sense resistance, and R_{DCR} is the inductor's series DC resistance. Use the typical inductance and R_{DCR} values provided by the inductor manufacturer. To minimize the current-sense error due to the bias current of the current-sense inputs ($I_{CSP_}$ and $I_{CSN_}$), choose $R1 \mid\mid R2$ to be less than 2kΩ and use the above equation to determine the sense capacitance (C_{EQ}). Choose capacitors with 5% tolerance and resistors with 1% tolerance specifications. Temperature compensation is recommended for this current-sense method. See the *Voltage Positioning* section for detailed information.

When using a current-sense resistor for accurate output-voltage positioning, the circuit requires a differential RC filter to eliminate the AC voltage step caused by the equivalent series inductance (L_{ESL}) of the current-sense resistor (see Figure 8). The ESL-induced voltage step might affect the average current-sense voltage. The time constant of the RC filter should match the L_{ESL}/R_{SENSE} time constant formed by the parasitic inductance of the current-sense resistor:

$$\frac{L_{ESL}}{R_{SENSE}} = C_{EQ}R_{EQ}$$

where L_{ESL} is the equivalent series inductance of the current-sense resistor, R_{SENSE} is the current-sense resistance value, and C_{EQ} and R_{EQ} are the time-constant matching components.

Current Balance

Regulator A integrates the difference between the current-sense voltages and adjusts the on-time of the second and third phases to maintain current balance. The current balance relies on the accuracy of the current-sense signals across the current-sense resistor or inductor DCR. With active current balancing, the current mismatch is determined by the current-sense resistor or inductor DCR values and the offset voltage of the transconductance amplifiers:

$$I_{OS(IBAL)} = I_{LMAIN} - I_{LSEC} = \frac{V_{OS(IBAL)}}{R_{SENSE}}$$

where R_{SENSE} is the equivalent DCR sense resistance and $V_{OS(IBAL)}$ is the current-balance offset specification in the *Electrical Characteristics* table. The worst-case current mismatch occurs immediately after a load transient due to inductor value mismatches, resulting in different di/dt for the two phases. The time it takes for the current-balance loop to correct the transient imbalance depends on the mismatch between the inductor values and switching frequency.

Current Limit

The current-limit circuit employs a "valley" current-sensing algorithm that senses the voltage across the current-sense resistors or inductor DCR at the current-sense inputs (CSP_ to CSN_). If the current-sense signal of the selected phase is above the current-limit threshold, the PWM controller does not initiate a new cycle until the inductor current of the selected phase drops below the valley current-limit threshold. When any one phase exceeds the current limit, all phases are effectively current limited since the interleaved controller does not initiate a cycle with the next phase. Since only the valley current is actively limited, the actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are functions of the current-sense resistance, inductor value, and battery voltage. The positive valley current-limit threshold voltage at CSP_ to CSN_ is preset using the IMAX_ and SR multivalue logic inputs.

Carefully observe the PCB layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signals seen by the current-sense inputs (CSP_, CSN_).

Feedback Adjustment Amplifier

Voltage-Positioning Amplifier (Steady-State Droop)

Regulators A and B include transconductance amplifiers for adding gain to the voltage-positioning sense path. The input of the amplifier is generated by summing the current-sense voltage inputs, which differentially sense the voltage across either current-sense resistors or the inductor's DCR. The output of the droop amplifier, $G_{m(FB_)}$ connects directly to the voltage-positioned feedback input (FB_) of the regulator, so the resistance between FB_ and the output-voltage sense point determines the voltage-positioning gain:

$$V_{OUT} = V_{TARGET} - (R_{FB} \times I_{FB_})$$

where the target voltage (V_{TARGET}) is defined in the *Nominal Output Voltage Selection* section, and the

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$G_{m(FB_)}$ output current $I_{FB_}$. $I_{FB_}$ is determined by the sum of the current-sense voltages:

$$I_{FB_} = G_{m(FB)_} \times V_{CSX}$$

where $V_{CSX} = V_{CSP_AVE} - V_{CSN_}$ or $V_{CSX} = V_{CSPB1} - V_{CSNB}$ (for regulator B of the MAX17511/MAX17511C/MAX17511N/MAX17511T) is the differential current-sense voltage, and $G_{m(FB_)}$ is 600µs (typ) as defined in the *Electrical Characteristics* table. The controller uses the V_{CSP_AVG} or the V_{CSPB1} input to get the average inductor current from the positive current-sense averaging network. Since the feedback voltage (FB_) is regulated, the output voltage changes in response to the feedback current $I_{FB_}$ to create a load line with accuracy defined by the characteristics of $R_{FB_}$ and $G_{m(FB_)}$.

When the inductor's DCR is used as the current-sense element ($R_{SENSE} = R_{DCR}$), the current-sense inputs should include an NTC thermistor to minimize the temperature dependence of the voltage-positioning slope.

CSP_AVE - CSN_ Inputs

The current-sense information across all phases are averaged together at the CSP_AVE - CSN_ or the CSPB1 - CSNB (MAX17511/MAX17511C/MAX17511N/MAX17511T) inputs. This signal contains both the DC average current information and the AC ripple information. The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T use the DC information to generate the load line, and the AC information for stability.

CSPAAVE - CSNA Design Using Inductor DCR Sensing

When the inductor DCR is used as the current-sense element, a DCR circuit network shown in Figure 9 is used to generate the average current signal for the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T.

The DCR circuit network is the divider of the actual inductor DCR. Hence the effective resistance at CSPAAVE - CSNA will be lower than the DCR resistance.

Since there are more unknowns than the equations in the current-sense network, the component values must be calculated by iteration. A spreadsheet helps as the variation over temperature should also be checked. The following steps provide some initial values to work with.

1) Use typical L and DCR values in the calculations.
2) For inductors with low DCR less than 1mΩ, add about 0.015mΩ to the DCR value to compensate for parasitic resistances due to layout and assembly.
3) Choose $C_{CSPAAVE}$ first since capacitor choices are limited. A good value to start with is 0.22µF. It is good to add a small capacitor position in parallel to $C_{CSPAAVE}$ to fine tune the total capacitance.
4) Larger $C_{CSPAAVE}$ results in smaller $R_{LX_}$ values. Smaller $R_{LX_}$ values are required to reduce the error due to pin leakages. As a rule, the $R_{LX_}$ resistors in parallel should be about 2kΩ or less.
5) Select $R_{CSPAAVE2}$ start with a value between 1kΩ and 4kΩ.
6) Select $R_{CSPAAVE1}$. Large values like 20kΩ to 100kΩ are recommended. $R_{CSPAAVE1}$ may even not be populated. Generally, $R_{CSPAAVE1}$ helps to reduce the variation over temperature.
7) Use a 10kΩ NTC with a beta of 3435k. The beta of 3435k is easier to keep effective DCR flat over temperature.
8) Calculate $R_{LXA_}$ assuming just one phase is used. After this value is determined, scale the actual $R_{LXA_}$ by the number of active phases in the design.

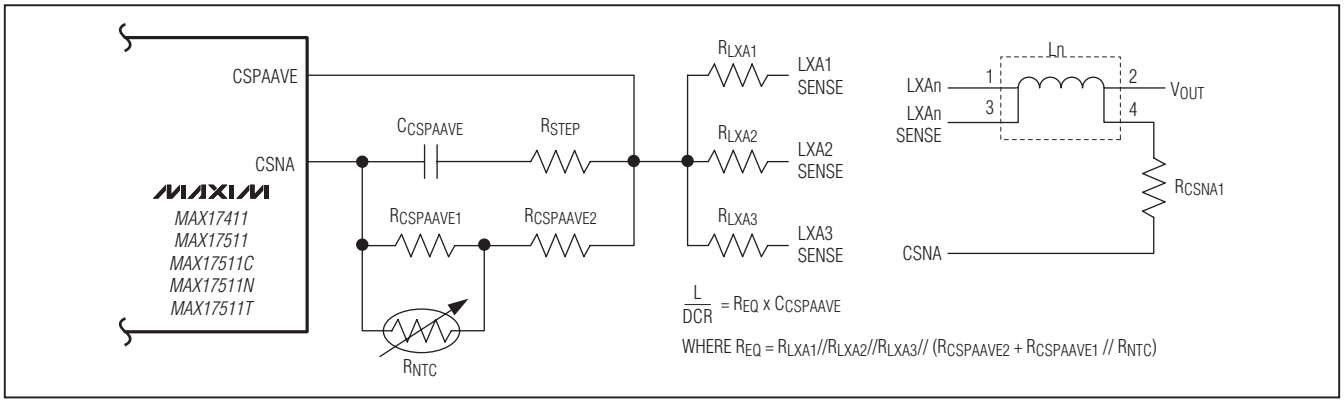

Figure 9. CSPAAVE - CSNA DCR Network

Differential Remote Sense

Both regulators A and B include differential, remote-sense inputs to eliminate the effects of voltage drops along the PCB traces and through the power pins of the processor. The feedback-sense node connects to the voltage-positioning resistor ($R_{FB_}$). The ground-sense (GNDS_) input connects to an amplifier that adds an offset directly to the target voltage, effectively adjusting the output voltage to counteract the voltage drop in the ground path. Connect the voltage-positioning resistor ($R_{FB_}$) and ground-sense (GNDS_) input directly to the remote-sense outputs of the processor as shown in Figure 1. The correction range is bounded to less than ±200mV. The remote-sense lines draw less than ±0.5µA to minimize offset errors.

Integrator Amplifier

Regulators A and B utilize internal integrator amplifiers that force the DC average of the FB_ voltage to equal the target voltage, allowing accurate DC output voltage regulation regardless of the output voltage. The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T disable the integrators by connecting the amplifier inputs together at the beginning of all VID transitions done in pulse-skipping mode (PS2, PS3). The integrators remain disabled until the transition is completed (the internal target settles) and the output is in regulation (edge detected on the error comparator).

Transient-Phase Overlap Operation

When a transient occurs, the response time of the controller depends on how quickly it can slew the inductor current. Multiphase controllers that remain 180° or 120° out-of-phase when a transient occurs actually respond slower than an equivalent single-phase controller. To provide fast transient response, regulator A and regulator B support phase-overlap mode, which allows the dual and triple regulators to operate in-phase when heavy load transients are detected, effectively reducing the response time. After any high-side MOSFET turns off, if the output voltage does not exceed the regulation voltage when the minimum off-time expires, the controller simultaneously turns on all high-side MOSFETs with the same on-time during the next on-time cycle. The phases remain overlapped until the output voltage exceeds the regulation voltage after the minimum off-time expires. The on-time for each phase is based on the input voltage to FB_ ratio (i.e., follows the master on-time), but reduced by 33% in a three-phase configuration, and not reduced in a two-phase configuration. This maximizes the total inductor current slew rate. After the phase-overlap mode ends, the controller automatically begins with the next phase. For example, if phase 2 provides the last on-time pulse before overlap operation begins, the controller starts switching with phase 3 when overlap operation ends.

Nominal Output Voltage Selection

The nominal no-load output voltage (V_{TARGET}) is defined by the selected voltage reference (SVID DAC), plus the remote ground-sense adjustment (V_{GNDS}) as defined in the following equation:

$$V_{TARGET} = V_{FB_} = V_{DAC} + V_{GNDS}$$

where V_{DAC} is the selected SVID voltage. On startup, the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T slew the target voltage from ground to the preset boot voltage. Table 3* lists the SVID code set for VR12/IMVP7.

***Table 3. VR12/IMVP-7 8-Bit DAC Code SVID[7:0]**

LINE	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX1	HEX0	DAC SET POINT	
											VOLTAGE (V)	ACCURACY
0	0	0	0	0	0	0	0	0	0	0	0	—
1	0	0	0	0	0	0	0	1	0	1	0.2500	±8mV
2	0	0	0	0	0	0	1	0	0	2	0.2550	±8mV
3	0	0	0	0	0	0	1	1	0	3	0.2600	±8mV
4	0	0	0	0	0	1	0	0	0	4	0.2650	±8mV
5	0	0	0	0	0	1	0	1	0	5	0.2700	±8mV
6	0	0	0	0	0	1	1	0	0	6	0.2750	±8mV
7	0	0	0	0	0	1	1	1	0	7	0.2800	±8mV
8	0	0	0	0	1	0	0	0	0	8	0.2850	±8mV
9	0	0	0	0	1	0	0	1	0	9	0.2900	±8mV
10	0	0	0	0	1	0	1	0	0	A	0.2950	±8mV

Table 3. VR12/IMVP-7 8-Bit DAC Code SVID[7:0] (continued)

LINE	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX1	HEX0	DAC SET POINT	
											VOLTAGE (V)	ACCURACY
11	0	0	0	0	1	0	1	1	0	B	0.3000	±8mV
12	0	0	0	0	1	1	0	0	0	C	0.3050	±8mV
13	0	0	0	0	1	1	0	1	0	D	0.3100	±8mV
14	0	0	0	0	1	1	1	0	0	E	0.3150	±8mV
15	0	0	0	0	1	1	1	1	0	F	0.3200	±8mV
16	0	0	0	1	0	0	0	0	1	0	0.3250	±8mV
17	0	0	0	1	0	0	0	1	1	1	0.3300	±8mV
18	0	0	0	1	0	0	1	0	1	2	0.3350	±8mV
19	0	0	0	1	0	0	1	1	1	3	0.3400	±8mV
20	0	0	0	1	0	1	0	0	1	4	0.3450	±8mV
21	0	0	0	1	0	1	0	1	1	5	0.3500	±8mV
22	0	0	0	1	0	1	1	0	1	6	0.3550	±8mV
23	0	0	0	1	0	1	1	1	1	7	0.3600	±8mV
24	0	0	0	1	1	0	0	0	1	8	0.3650	±8mV
25	0	0	0	1	1	0	0	1	1	9	0.3700	±8mV
26	0	0	0	1	1	0	1	0	1	A	0.3750	±8mV
27	0	0	0	1	1	0	1	1	1	B	0.3800	±8mV
28	0	0	0	1	1	1	0	0	1	C	0.3850	±8mV
29	0	0	0	1	1	1	0	1	1	D	0.3900	±8mV
30	0	0	0	1	1	1	1	0	1	E	0.3950	±8mV
31	0	0	0	1	1	1	1	1	1	F	0.4000	±8mV
32	0	0	1	0	0	0	0	0	2	0	0.4050	±8mV
33	0	0	1	0	0	0	0	1	2	1	0.4100	±8mV
34	0	0	1	0	0	0	1	0	2	2	0.4150	±8mV
35	0	0	1	0	0	0	1	1	2	3	0.4200	±8mV
36	0	0	1	0	0	1	0	0	2	4	0.4250	±8mV
37	0	0	1	0	0	1	0	1	2	5	0.4300	±8mV
38	0	0	1	0	0	1	1	0	2	6	0.4350	±8mV
39	0	0	1	0	0	1	1	1	2	7	0.4400	±8mV
40	0	0	1	0	1	0	0	0	2	8	0.4450	±8mV
41	0	0	1	0	1	0	0	1	2	9	0.4500	±8mV
42	0	0	1	0	1	0	1	0	2	A	0.4550	±8mV
43	0	0	1	0	1	0	1	1	2	B	0.4600	±8mV
44	0	0	1	0	1	1	0	0	2	C	0.4650	±8mV
45	0	0	1	0	1	1	0	1	2	D	0.4700	±8mV
46	0	0	1	0	1	1	1	0	2	E	0.4750	±8mV
47	0	0	1	0	1	1	1	1	2	F	0.4800	±8mV
48	0	0	1	1	0	0	0	0	3	0	0.4850	±8mV
49	0	0	1	1	0	0	0	1	3	1	0.4900	±8mV
50	0	0	1	1	0	0	1	0	3	2	0.4950	±8mV
51	0	0	1	1	0	0	1	1	3	3	0.5000	±8mV

Table 3. VR12/IMVP-7 8-Bit DAC Code SVID[7:0] (continued)

LINE	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX1	HEX0	DAC SET POINT	
											VOLTAGE (V)	ACCURACY
52	0	0	1	1	0	1	0	0	3	4	0.5050	±8mV
53	0	0	1	1	0	1	0	1	3	5	0.5100	±8mV
54	0	0	1	1	0	1	1	0	3	6	0.5150	±8mV
55	0	0	1	1	0	1	1	1	3	7	0.5200	±8mV
56	0	0	1	1	1	0	0	0	3	8	0.5250	±8mV
57	0	0	1	1	1	0	0	1	3	9	0.5300	±8mV
58	0	0	1	1	1	0	1	0	3	A	0.5350	±8mV
59	0	0	1	1	1	0	1	1	3	B	0.5400	±8mV
60	0	0	1	1	1	1	0	0	3	C	0.5450	±8mV
61	0	0	1	1	1	1	0	1	3	D	0.5500	±8mV
62	0	0	1	1	1	1	1	0	3	E	0.5550	±8mV
63	0	0	1	1	1	1	1	1	3	F	0.5600	±8mV
64	0	1	0	0	0	0	0	0	4	0	0.5650	±8mV
65	0	1	0	0	0	0	0	1	4	1	0.5700	±8mV
66	0	1	0	0	0	0	1	0	4	2	0.5750	±8mV
67	0	1	0	0	0	0	1	1	4	3	0.5800	±8mV
68	0	1	0	0	0	1	0	0	4	4	0.5850	±8mV
69	0	1	0	0	0	1	0	1	4	5	0.5900	±8mV
70	0	1	0	0	0	1	1	0	4	6	0.5950	±8mV
71	0	1	0	0	0	1	1	1	4	7	0.6000	±8mV
72	0	1	0	0	1	0	0	0	4	8	0.6050	±8mV
73	0	1	0	0	1	0	0	1	4	9	0.6100	±8mV
74	0	1	0	0	1	0	1	0	4	A	0.6150	±8mV
75	0	1	0	0	1	0	1	1	4	B	0.6200	±8mV
76	0	1	0	0	1	1	0	0	4	C	0.6250	±8mV
77	0	1	0	0	1	1	0	1	4	D	0.6300	±8mV
78	0	1	0	0	1	1	1	0	4	E	0.6350	±8mV
79	0	1	0	0	1	1	1	1	4	F	0.6400	±8mV
80	0	1	0	1	0	0	0	0	5	0	0.6450	±8mV
81	0	1	0	1	0	0	0	1	5	1	0.6500	±8mV
82	0	1	0	1	0	0	1	0	5	2	0.6550	±8mV
83	0	1	0	1	0	0	1	1	5	3	0.6600	±8mV
84	0	1	0	1	0	1	0	0	5	4	0.6650	±8mV
85	0	1	0	1	0	1	0	1	5	5	0.6700	±8mV
86	0	1	0	1	0	1	1	0	5	6	0.6750	±8mV
87	0	1	0	1	0	1	1	1	5	7	0.6800	±8mV
88	0	1	0	1	1	0	0	0	5	8	0.6850	±8mV
89	0	1	0	1	1	0	0	1	5	9	0.6900	±8mV
90	0	1	0	1	1	0	1	0	5	A	0.6950	±8mV
91	0	1	0	1	1	0	1	1	5	B	0.7000	±8mV
92	0	1	0	1	1	1	0	0	5	C	0.7050	±8mV

Table 3. VR12/IMVP-7 8-Bit DAC Code SVID[7:0] (continued)

LINE	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX1	HEX0	DAC SET POINT	
											VOLTAGE (V)	ACCURACY
93	0	1	0	1	1	1	0	1	5	D	0.7100	±8mV
94	0	1	0	1	1	1	1	0	5	E	0.7150	±8mV
95	0	1	0	1	1	1	1	1	5	F	0.7200	±8mV
96	0	1	1	0	0	0	0	0	6	0	0.7250	±8mV
97	0	1	1	0	0	0	0	1	6	1	0.7300	±8mV
98	0	1	1	0	0	0	1	0	6	2	0.7350	±8mV
99	0	1	1	0	0	0	1	1	6	3	0.7400	±8mV
100	0	1	1	0	0	1	0	0	6	4	0.7450	±8mV
101	0	1	1	0	0	1	0	1	6	5	0.7500	±8mV
102	0	1	1	0	0	1	1	0	6	6	0.7550	±8mV
103	0	1	1	0	0	1	1	1	6	7	0.7600	±8mV
104	0	1	1	0	1	0	0	0	6	8	0.7650	±8mV
105	0	1	1	0	1	0	0	1	6	9	0.7700	±8mV
106	0	1	1	0	1	0	1	0	6	A	0.7750	±8mV
107	0	1	1	0	1	0	1	1	6	B	0.7800	±8mV
108	0	1	1	0	1	1	0	0	6	C	0.7850	±8mV
109	0	1	1	0	1	1	0	1	6	D	0.7900	±8mV
110	0	1	1	0	1	1	1	0	6	E	0.7950	±8mV
111	0	1	1	0	1	1	1	1	6	F	0.8000	±5mV
112	0	1	1	1	0	0	0	0	7	0	0.8050	±5mV
113	0	1	1	1	0	0	0	1	7	1	0.8100	±5mV
114	0	1	1	1	0	0	1	0	7	2	0.8150	±5mV
115	0	1	1	1	0	0	1	1	7	3	0.8200	±5mV
116	0	1	1	1	0	1	0	0	7	4	0.8250	±5mV
117	0	1	1	1	0	1	0	1	7	5	0.8300	±5mV
118	0	1	1	1	0	1	1	0	7	6	0.8350	±5mV
119	0	1	1	1	0	1	1	1	7	7	0.8400	±5mV
120	0	1	1	1	1	0	0	0	7	8	0.8450	±5mV
121	0	1	1	1	1	0	0	1	7	9	0.8500	±5mV
122	0	1	1	1	1	0	1	0	7	A	0.8550	±5mV
123	0	1	1	1	1	0	1	1	7	B	0.8600	±5mV
124	0	1	1	1	1	1	0	0	7	C	0.8650	±5mV
125	0	1	1	1	1	1	0	1	7	D	0.8700	±5mV
126	0	1	1	1	1	1	1	0	7	E	0.8750	±5mV
127	0	1	1	1	1	1	1	1	7	F	0.8800	±5mV
128	1	0	0	0	0	0	0	0	8	0	0.8850	±5mV
129	1	0	0	0	0	0	0	1	8	1	0.8900	±5mV
130	1	0	0	0	0	0	1	0	8	2	0.8950	±5mV
131	1	0	0	0	0	0	1	1	8	3	0.9000	±5mV
132	1	0	0	0	0	1	0	0	8	4	0.9050	±5mV
133	1	0	0	0	0	1	0	1	8	5	0.9100	±5mV

Table 3. VR12/IMVP-7 8-Bit DAC Code SVID[7:0] (continued)

LINE	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX1	HEX0	DAC SET POINT	
											VOLTAGE (V)	ACCURACY
134	1	0	0	0	0	1	1	0	8	6	0.9150	±5mV
135	1	0	0	0	0	1	1	1	8	7	0.9200	±5mV
136	1	0	0	0	1	0	0	0	8	8	0.9250	±5mV
137	1	0	0	0	1	0	0	1	8	9	0.9300	±5mV
138	1	0	0	0	1	0	1	0	8	A	0.9350	±5mV
139	1	0	0	0	1	0	1	1	8	B	0.9400	±5mV
140	1	0	0	0	1	1	0	0	8	C	0.9450	±5mV
141	1	0	0	0	1	1	0	1	8	D	0.9500	±5mV
142	1	0	0	0	1	1	1	0	8	E	0.9550	±5mV
143	1	0	0	0	1	1	1	1	8	F	0.9600	±5mV
144	1	0	0	1	0	0	0	0	9	0	0.9650	±5mV
145	1	0	0	1	0	0	0	1	9	1	0.9700	±5mV
146	1	0	0	1	0	0	1	0	9	2	0.9750	±5mV
147	1	0	0	1	0	0	1	1	9	3	0.9800	±5mV
148	1	0	0	1	0	1	0	0	9	4	0.9850	±5mV
149	1	0	0	1	0	1	0	1	9	5	0.9900	±5mV
150	1	0	0	1	0	1	1	0	9	6	0.9950	±5mV
151	1	0	0	1	0	1	1	1	9	7	1.0000	±0.5%
152	1	0	0	1	1	0	0	0	9	8	1.0050	±0.5%
153	1	0	0	1	1	0	0	1	9	9	1.0100	±0.5%
154	1	0	0	1	1	0	1	0	9	A	1.0150	±0.5%
155	1	0	0	1	1	0	1	1	9	B	1.0200	±0.5%
156	1	0	0	1	1	1	0	0	9	C	1.0250	±0.5%
157	1	0	0	1	1	1	0	1	9	D	1.0300	±0.5%
158	1	0	0	1	1	1	1	0	9	E	1.0350	±0.5%
159	1	0	0	1	1	1	1	1	9	F	1.0400	±0.5%
160	1	0	1	0	0	0	0	0	A	0	1.0450	±0.5%
161	1	0	1	0	0	0	0	1	A	1	1.0500	±0.5%
162	1	0	1	0	0	0	1	0	A	2	1.0550	±0.5%
163	1	0	1	0	0	0	1	1	A	3	1.0600	±0.5%
164	1	0	1	0	0	1	0	0	A	4	1.0650	±0.5%
165	1	0	1	0	0	1	0	1	A	5	1.0700	±0.5%
166	1	0	1	0	0	1	1	0	A	6	1.0750	±0.5%
167	1	0	1	0	0	1	1	1	A	7	1.0800	±0.5%
168	1	0	1	0	1	0	0	0	A	8	1.0850	±0.5%
169	1	0	1	0	1	0	0	1	A	9	1.0900	±0.5%
170	1	0	1	0	1	0	1	0	A	A	1.0950	±0.5%
171	1	0	1	0	1	0	1	1	A	B	1.1000	±0.5%
172	1	0	1	0	1	1	0	0	A	C	1.1050	±0.5%
173	1	0	1	0	1	1	0	1	A	D	1.1100	±0.5%
174	1	0	1	0	1	1	1	0	A	E	1.1150	±0.5%

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

Table 3. VR12/IMVP-7 8-Bit DAC Code SVID[7:0] (continued)

LINE	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX1	HEX0	DAC SET POINT	
											VOLTAGE (V)	ACCURACY
175	1	0	1	0	1	1	1	1	A	F	1.1200	±0.5%
176	1	0	1	1	0	0	0	0	B	0	1.1250	±0.5%
177	1	0	1	1	0	0	0	1	B	1	1.1300	±0.5%
178	1	0	1	1	0	0	1	0	B	2	1.1350	±0.5%
179	1	0	1	1	0	0	1	1	B	3	1.1400	±0.5%
180	1	0	1	1	0	1	0	0	B	4	1.1450	±0.5%
181	1	0	1	1	0	1	0	1	B	5	1.1500	±0.5%
182	1	0	1	1	0	1	1	0	B	6	1.1550	±0.5%
183	1	0	1	1	0	1	1	1	B	7	1.1600	±0.5%
184	1	0	1	1	1	0	0	0	B	8	1.1650	±0.5%
185	1	0	1	1	1	0	0	1	B	9	1.1700	±0.5%
186	1	0	1	1	1	0	1	0	B	A	1.1750	±0.5%
187	1	0	1	1	1	0	1	1	B	B	1.1800	±0.5%
188	1	0	1	1	1	1	0	0	B	C	1.1850	±0.5%
189	1	0	1	1	1	1	0	1	B	D	1.1900	±0.5%
190	1	0	1	1	1	1	1	0	B	E	1.1950	±0.5%
191	1	0	1	1	1	1	1	1	B	F	1.2000	±0.5%
192	1	1	0	0	0	0	0	0	C	0	1.2050	±0.5%
193	1	1	0	0	0	0	0	1	C	1	1.2100	±0.5%
194	1	1	0	0	0	0	1	0	C	2	1.2150	±0.5%
195	1	1	0	0	0	0	1	1	C	3	1.2200	±0.5%
196	1	1	0	0	0	1	0	0	C	4	1.2250	±0.5%
197	1	1	0	0	0	1	0	1	C	5	1.2300	±0.5%
198	1	1	0	0	0	1	1	0	C	6	1.2350	±0.5%
199	1	1	0	0	0	1	1	1	C	7	1.2400	±0.5%
200	1	1	0	0	1	0	0	0	C	8	1.2450	±0.5%
201	1	1	0	0	1	0	0	1	C	9	1.2500	±0.5%
202	1	1	0	0	1	0	1	0	C	A	1.2550	±0.5%
203	1	1	0	0	1	0	1	1	C	B	1.2600	±0.5%
204	1	1	0	0	1	1	0	0	C	C	1.2650	±0.5%
205	1	1	0	0	1	1	0	1	C	D	1.2700	±0.5%
206	1	1	0	0	1	1	1	0	C	E	1.2750	±0.5%
207	1	1	0	0	1	1	1	1	C	F	1.2800	±0.5%
208	1	1	0	1	0	0	0	0	D	0	1.2850	±0.5%
209	1	1	0	1	0	0	0	1	D	1	1.2900	±0.5%
210	1	1	0	1	0	0	1	0	D	2	1.2950	±0.5%
211	1	1	0	1	0	0	1	1	D	3	1.3000	±0.5%
212	1	1	0	1	0	1	0	0	D	4	1.3050	±0.5%
213	1	1	0	1	0	1	0	1	D	5	1.3100	±0.5%
214	1	1	0	1	0	1	1	0	D	6	1.3150	±0.5%
215	1	1	0	1	0	1	1	1	D	7	1.3200	±0.5%

Table 3. VR12/IMVP-7 8-Bit DAC Code SVID[7:0] (continued)

LINE	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX1	HEX0	DAC SET POINT	
											VOLTAGE (V)	ACCURACY
216	1	1	0	1	1	0	0	0	D	8	1.3250	±0.5%
217	1	1	0	1	1	0	0	1	D	9	1.3300	±0.5%
218	1	1	0	1	1	0	1	0	D	A	1.3350	±0.5%
219	1	1	0	1	1	0	1	1	D	B	1.3400	±0.5%
220	1	1	0	1	1	1	0	0	D	C	1.3450	±0.5%
221	1	1	0	1	1	1	0	1	D	D	1.3500	±0.5%
222	1	1	0	1	1	1	1	0	D	E	1.3550	±0.5%
223	1	1	0	1	1	1	1	1	D	F	1.3600	±0.5%
224	1	1	1	0	0	0	0	0	E	0	1.3650	±0.5%
225	1	1	1	0	0	0	0	1	E	1	1.3700	±0.5%
226	1	1	1	0	0	0	1	0	E	2	1.3750	±0.5%
227	1	1	1	0	0	0	1	1	E	3	1.3800	±0.5%
228	1	1	1	0	0	1	0	0	E	4	1.3850	±0.5%
229	1	1	1	0	0	1	0	1	E	5	1.3900	±0.5%
230	1	1	1	0	0	1	1	0	E	6	1.3950	±0.5%
231	1	1	1	0	0	1	1	1	E	7	1.4000	±0.5%
232	1	1	1	0	1	0	0	0	E	8	1.4050	±0.5%
233	1	1	1	0	1	0	0	1	E	9	1.4100	±0.5%
234	1	1	1	0	1	0	1	0	E	A	1.4150	±0.5%
235	1	1	1	0	1	0	1	1	E	B	1.4200	±0.5%
236	1	1	1	0	1	1	0	0	E	C	1.4250	±0.5%
237	1	1	1	0	1	1	0	1	E	D	1.4300	±0.5%
238	1	1	1	0	1	1	1	0	E	E	1.4350	±0.5%
239	1	1	1	0	1	1	1	1	E	F	1.4400	±0.5%
240	1	1	1	1	0	0	0	0	F	0	1.4450	±0.5%
241	1	1	1	1	0	0	0	1	F	1	1.4500	±0.5%
242	1	1	1	1	0	0	1	0	F	2	1.4550	±0.5%
243	1	1	1	1	0	0	1	1	F	3	1.4600	±0.5%
244	1	1	1	1	0	1	0	0	F	4	1.4650	±0.5%
245	1	1	1	1	0	1	0	1	F	5	1.4700	±0.5%
246	1	1	1	1	0	1	1	0	F	6	1.4750	±0.5%
247	1	1	1	1	0	1	1	1	F	7	1.4800	±0.5%
248	1	1	1	1	1	0	0	0	F	8	1.4850	±0.5%
249	1	1	1	1	1	0	0	1	F	9	1.4900	±0.5%
250	1	1	1	1	1	0	1	0	F	A	1.4950	±0.5%
251	1	1	1	1	1	0	1	1	F	B	1.5000	±0.5%
252	1	1	1	1	1	1	0	0	F	C	1.5050	±0.5%
253	1	1	1	1	1	1	0	1	F	D	1.5100	±0.5%
254	1	1	1	1	1	1	1	0	F	E	1.5150	±0.5%
255	1	1	1	1	1	1	1	1	F	F	1.5200	±0.5%

**The output voltage accuracy in Table 3 is specified for T_A = 0°C to +85°C. See the* Electrical Characteristics *table for output voltage accuracy over T_A = -40°C to +105°C temperature range.*

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

Output Voltage Transient Timing

At the beginning of an output voltage transition, the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T blank both power-good thresholds, preventing the POK_ open-drain outputs from changing states during the transition. The controller enables the lower power-good threshold approximately 20µs after the slew-rate controller reaches the target output voltage, but the upper threshold is enabled only if the controller remains in forced-PWM operation. If the controller enters pulse-skipping operation, the upper threshold remains blanked until an LX pulse is required.

The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T automatically control the current to the minimum level required to complete the transition. The total transition time depends on the SR input setting, the particular SETVID command (fast, slow) and the voltage difference, and the accuracy of the slew-rate controller (see the *Slew-Rate Accuracy* in the *Electrical Characteristics* table). The slew rate is not dependent on the total output capacitance, as long as the surge current is less than the current limit. For dynamic SVID transitions, the transition time (t_{TRAN}) is given by:

$$t_{TRAN} = \frac{|V_{NEW} - V_{OLD}|}{(dV_{TARGET}/dt)}$$

where dV_{TARGET}/dt is the slew rate set with the SR input and the SetVID command, V_{OLD} is the original output voltage, and V_{NEW} is the new target voltage. The maximum programmable slew rate is 20mV/µs.

For non-zero V_{BOOT}, the soft-start slew rate is fixed at 2.5mV/µs (minimum). The average inductor current per phase required to make an output voltage transition is:

$$I_L = \frac{C_{OUT}}{N_{TOTAL}} \times (dV_{TARGET}/dt)$$

where dV_{TARGET}/dt is the required slew rate, C_{OUT} is the total output capacitance, and N_{TOTAL} is the number of active phases.

Forced-PWM Operation (PS0, PS1)

During startup and normal operation, when the CPU is actively running (PS0, PS1) the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T operate with the low-noise, forced-PWM control scheme. Forced-PWM operation disables the zero-crossing comparators of all active phases, forcing the low-side gate-drive waveforms to constantly be the complement of the high-side gate-drive waveforms. This keeps the switching frequency constant and allows the inductor current to reverse under light loads, providing fast, accurate negative output voltage transitions by quickly discharging the output capacitors. Forced-PWM operation comes at a cost: the no-load +5V bias supply current remains between 10mA to 50mA per phase, depending on the external MOSFETs and switching frequency. To maintain high efficiency under light-load conditions, the processor can switch the controller to a low-power pulse-skipping control scheme by entering PS2 or PS3.

Light-Load Pulse-Skipping Operation (PS2, PS3)

When the SVID bus master issues a SetPS command to PS2 or PS3, the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T immediately disable phases 2 and 3 (DH_2, DL_2 forced low, DRVPWM_ three-state), and enters pulse-skipping operation. The pulse-skipping mode enables the zero-crossing comparator of the driver, so the controller pulls DL_ low when its current-sense inputs detect “zero” inductor current. This keeps the inductor from discharging the output capacitors and forces the controller to skip pulses under light-load conditions to avoid overcharging the output. If the VIDs are set to a lower voltage setting, the output drops at a rate determined by the load and the output capacitance. The internal target still ramps as before, and POK_ remains blanked high impedance until 20µs after the output voltage reaches the internal target. Once this time expires, POK_ monitors only the lower threshold. Upon entering pulse-skipping operation, the MAX17411/MAX17511/MAX17511C/MAX17511N temporarily set the OVP threshold to 1.77V (typ), preventing false OVP faults when the transition to pulse-skipping operation coincides with an SVID code change. Once the VR_Settled comparator detects that the output voltage is in regulation, the OVP threshold tracks the selected SVID DAC code. The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T automatically use forced-PWM operation during soft-start, regardless of the SetPS command.

Automatic Pulse-Skipping Switchover

In SKIP mode (PS2, PS3), an inherent automatic switchover to PFM takes place at light loads (Figure 10). This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current’s zero crossing. The zero-crossing comparator senses the

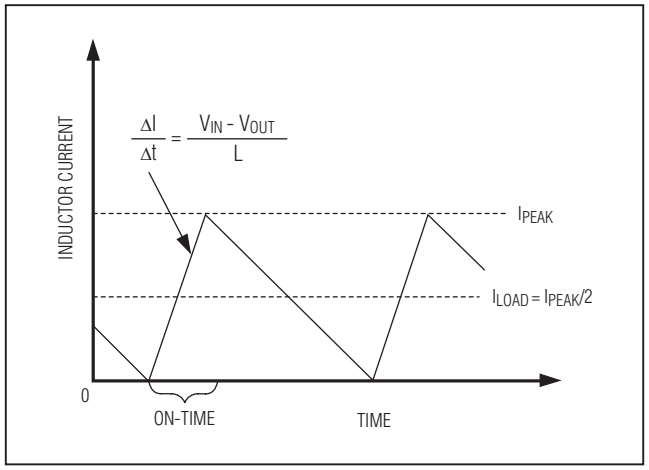

Figure 10. Pulse Skipping/Discontinuous Crossover Point

inductor current across the low-side MOSFETs. Once $V_{LX_}$ drops below the zero-crossing comparator threshold (see the *Electrical Characteristics* table), the comparator forces DL_ low. This mechanism causes the threshold between pulse-skipping PFM and non-skipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation. The PFM/PWM crossover occurs when the load current of each phase is equal to 1/2 the peak-to-peak ripple current, which is a function of the inductor value. For a battery input range of 7V to 20V, this threshold is relatively constant, with only a minor dependence on the input voltage due to the typically low duty cycles. The total load current at the PFM/PWM crossover threshold ($I_{LOAD(SKIP)}$) is approximately:

$$I_{LOAD(SKIP)} = \left(\frac{t_{SW} V_{OUT}}{2L}\right)\left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

Power-Up Sequence (POR, UVLO)

The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T are enabled when EN is driven high (Figures 11 and 12). The reference powers up first. Once the internal reference exceeds its UVLO threshold, the internal analog blocks are turned on and masked by a 50µs one-shot delay. The startup ADC then begins to detect the voltage applied to IMAX_ and SR inputs to set the current limits and slew rate as well as the contents of the ICC_MAX (21h), SR_Fast (24h), and SR_Slow (25h) registers. After this initialization, the PWM controller begins switching. Power-on reset (POR) occurs when V_{CC} rises above approximately 2V, resetting the fault latch and preparing the controller for operation. The V_{CC} UVLO circuitry inhibits switching until V_{CC} rises above 4.25V. The controller powers up the reference once the system enables the controller, V_{CC} is above 4.25V, and EN is driven high. With the reference in regulation, the controller ramps the output voltage to the programmed boot voltage at the command slew rate for zero V_{BOOT} or the slow slew rate for non-zero V_{BOOT}.

$$t_{TRAN(START)} = \frac{V_{BOOT}}{(dV_{TARGET}/dt)}$$

where dV_{TARGET}/dt is the slew rate.

The soft-start circuitry does not use a variable current limit, so full output current is available immediately.

Note the IMAX_ and SR multivalued logic inputs are sampled after POR and the data latched into the respective registers. These values cannot be changed without driving the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T through another POR cycle.

The startup sequence is as follows:

1) The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T have power and IC V_{CC} is > UVLO.
2) EN goes high.
3) The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T's SVID buses are active and idle.
4) If V_{BOOT} register = 00h, the MAX17411/MAX17511/MAX17511T wait at 0V, POK_ is deasserted and ALERT# remains deasserted and hold until the SVID command. If V_{BOOT} register is programmed to a VID setting other than zero (V_{BOOT} = 1.1V for the MAX17511N), the device ramps to the programmed voltage, asserts POK_ and ALERT#, and hold until the SVID command.
5) CPU initiates the SVID clock.
6) CPU sends out the SetVID_Slow command to program the initial output voltage.
7) The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T acknowledge and ramp to the voltage in the SetVID_Slow command at the slow slew rate, toggle status bit VR_Settled.
8) The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T assert POK_ for that rail.
9) Steps 4, 5, 6, 7, and 8 are repeated for regulator B. If V_{CC} drops below 4.25V after POR, the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T set the fault latch and turn off.

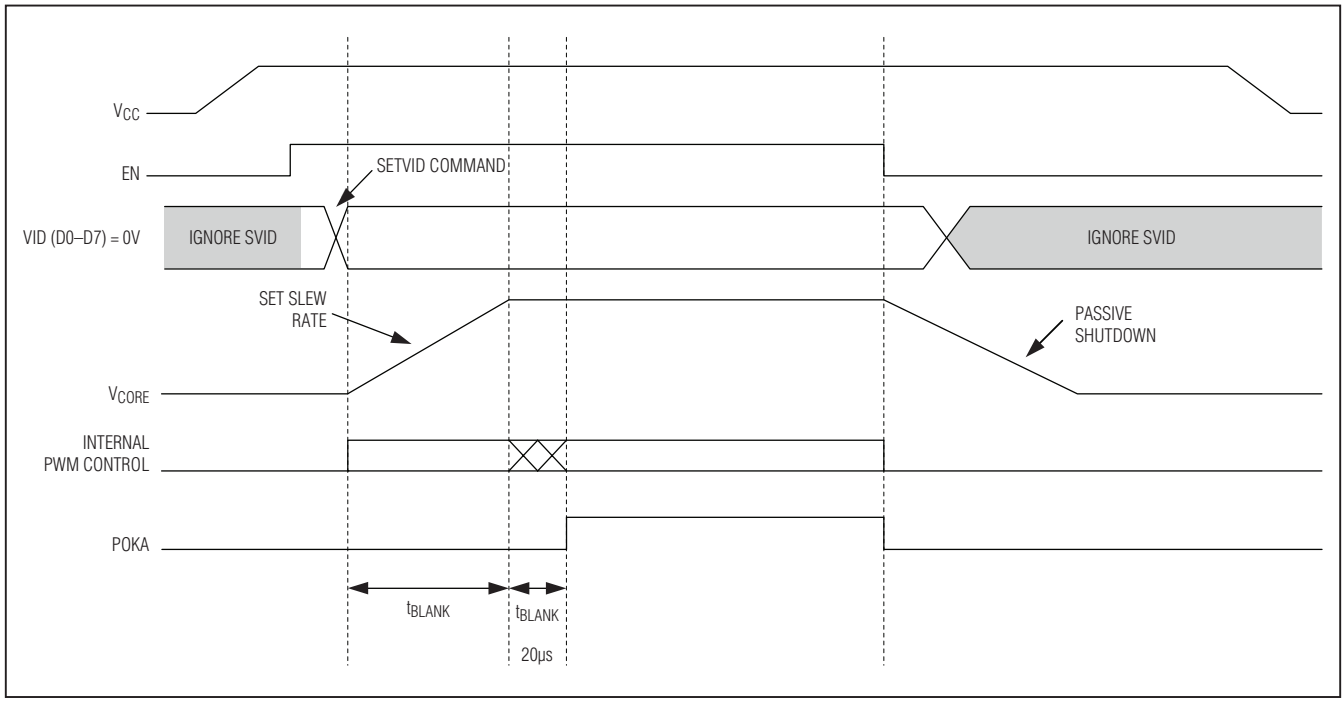

Figure 11. Startup Sequence for Zero V_{BOOT}

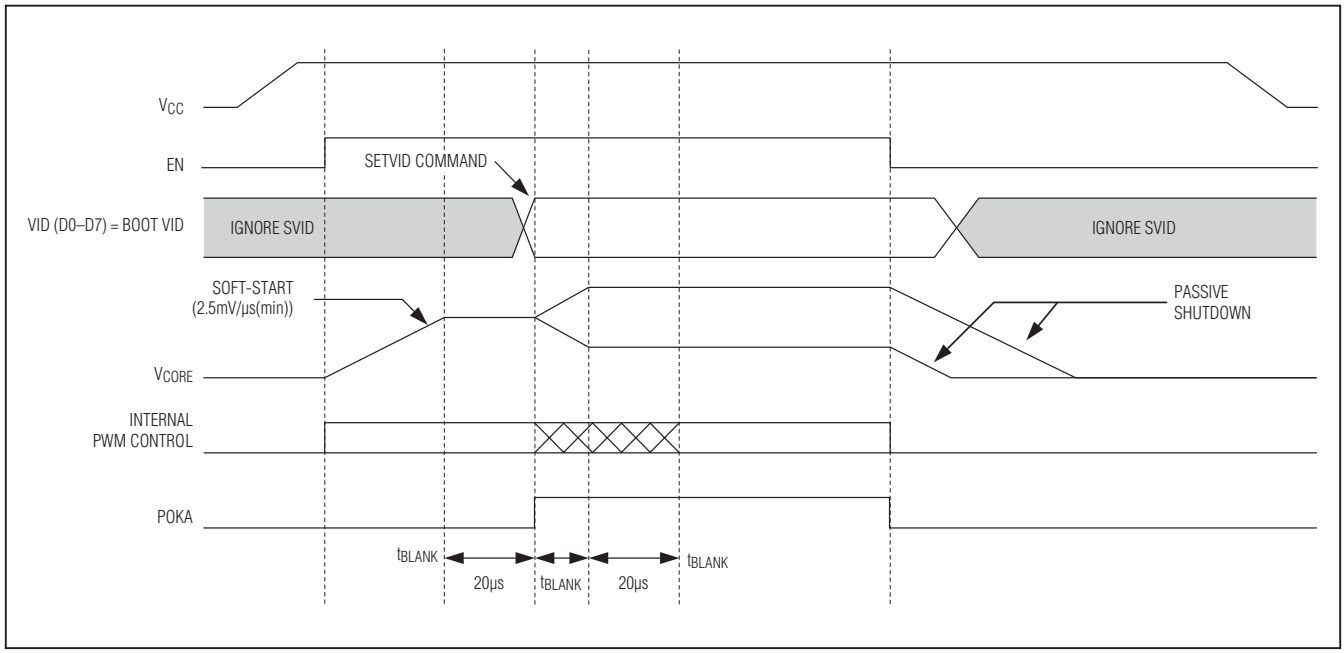

Figure 12. Startup Sequence for Non-Zero V_{BOOT}

Shutdown Control

When EN goes low, the MAX17411/MAX17511 MAX17511C/MAX17511N/MAX17511T enter low-power shutdown mode. POK_ is pulled low immediately, and the output voltage ramps down through an internal 20Ω discharge resistor.

After EN goes low, the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T shut down completely—the drivers are disabled (DL_ and DH_ driven low, and DRVPWM_ is three-state), the reference turns off, and the supply current drops below 30µA. When an undervoltage fault condition activates the shutdown sequence, the protection circuitry sets the fault latch to prevent the controller from restarting. To clear the fault latch and reactivate the controller, toggle EN or cycle V_{CC} power below 0.5V.

The EN input controls both regulator A and regulator B outputs. EN is active-high and is compatible with 1V logic. When EN is asserted, with V_{BOOT} = 0V, the SVID bus is active within 200µs and enters an idle state, waiting for first commands and initial voltage target. For non-zero V_{BOOT}, the SVID interface can accept commands after the output voltage reaches its target value.

Regulator A or regulator B can be independently placed in non-zero V_{BOOT} mode by connecting THERMA or THERMB to ground at startup (MAX17411/MAX17511/MAX17511T).

Power-Good (POKA, POKB)

Regulator A and regulator B have independent power-good signals (POKA, POKB). These active-high outputs indicate the startup sequence is complete and the respective output voltage has moved to the programmed SVID value. These signals are used for system sequencing for other voltage regulators, the clock, and microprocessor reset. POK_ remains asserted during normal DC-DC operation and deasserts under any fault or shutdown condition.

POKA and POKB continuously monitor the output voltage for undervoltage and overvoltage fault conditions. If the regulator enters current limit, the respective POK_ signal will not go low until the UVP threshold is reached. POK_ is actively held low in shutdown (EN = GND) and during soft-start and shutdown. Approximately 20µs (typ) after the soft-start terminates, POK_ becomes high impedance as long as the feedback voltage is above the UVP threshold (VID - 250mV) and below the OVP threshold (VID + 250mV). POK_ goes low if the feedback voltage drops -200mV (max) below the target voltage or rises 200mV (min) above the target voltage, or the SMPS controller shuts down. POK_ must use an external pullup resistor between POK_ and V_{CC} to deliver a valid logic-level output.

Temperature Comparator (VR_HOT#)

The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T feature two independent comparators with inputs at THERMA and THERMB. These comparators have accurate thresholds matching the appropriate thermal levels required for the Temperature Zone register (12h). Since these thresholds are nonlinear, it is essential to use the correct resistor and thermistor values specified in Figures 1 and 2. When the maximum temperature is exceeded at either THERMA or THERMB, VR_HOT# is pulled low. For each regulator, place the thermistor as close to the MOSFETs and inductors as possible. The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T EV kits provide good examples of thermistor placement.

Fault Protection (Latched)

Output Overvoltage Protection (OVP) (MAX17411/MAX17511/MAX17511C/MAX17511N Only)

The OVP circuit is designed to protect the load against a shorted high-side MOSFET by drawing high current and activating the adapter or battery protection circuits. The MAX17411/MAX17511/MAX17511C/MAX17511N continuously monitor each output for an overvoltage fault. An OVP fault is detected if the output voltage exceeds the SVID DAC voltage by more than 200mV (min), or the fixed 1.77V (typ) threshold during a downward VID transition in SKIP mode. During pulse-skipping operation (PS2, PS3), the OVP threshold tracks the SVID DAC voltage as soon as the output is in regulation; otherwise, the fixed 1.77V (typ) threshold is used. When the OVP circuit detects an overvoltage fault while in multiphase mode (PS0), the MAX17411/MAX17511/MAX17511C/MAX17511N immediately force DL_ high, three-state DRVPWM_, and pull DH_ low. This action turns on the synchronous-rectifier MOSFETs with 100% duty cycle and, in turn, rapidly discharges the output filter capacitor and forces the output low. If the condition that caused the overvoltage (such as a shorted high-side MOSFET) persists, the battery fuse blows or the high-current protection activates. Toggle EN or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller. When an overvoltage fault occurs, the MAX17411/MAX17511/MAX17511C/MAX17511N immediately force DL_high, pull DH_low and three-states DRVPWM_.

Output Undervoltage Protection (UVP)

If the output voltage on regulator A or B is 200mV (max) below the target voltage and stays below this level for 200µs (typ), the controller activates the shutdown sequence. The regulator turns on a 20Ω discharge resis-

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tor and sets the fault latch. DL_ and DH_ are forced low, and DRVPWM goes to the three-state output defined in the *Electrical Characteristics* table. Toggle EN or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller.

Thermal-Fault Protection

In addition to VR_HOT#, the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T feature internal thermal-fault-protection circuits for regulator A and regulator B. When the junction temperature rises above +160°C, a thermal sensor sets the fault latch and forces the DL_ and DH_ low, and three-states DRVPWM_. Toggle EN or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller after the junction temperature cools by 15°C (typ).

MOSFET Gate Drivers

The DH_ and DL_ drivers are optimized for driving moderate-sized high-side and larger low-side power MOSFETs. This is consistent with the low duty factor seen in notebook applications, where a large V_{IN} - V_{OUT} differential exists. The high-side gate drivers (DH_) source 2.2A and sink 2.7A, and the low-side gate drivers (DL_) source 2.7A and sink 8A. This ensures robust gate drive for high-current applications. The DH_ high-side MOSFET drivers are powered by internal boost switch charge pumps at BST_, while the DL_ synchronous-rectifier drivers are powered directly by the 5V bias supply ($V_{DD_}$). Adaptive dead-time circuits monitor the DL_ and DH_ drivers and prevent either MOSFET from turning on until the other is fully off. The adaptive driver dead-time allows operation without shoot-through with a wide range of MOSFETs, minimizing delays and maintaining efficiency. A low-resistance, low-inductance path from the DL_ and DH_ drivers to the MOSFET gates is required for the adaptive dead-time circuits to work properly; otherwise, the sense circuitry in the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T may interpret the MOSFET gates as "off" while significant charge is still present.

Use very short, wide traces (50mils to 100mils wide if the MOSFET is 1in from the driver). The DL_ low on-resistance of 0.25Ω (typ) helps prevent DL_ from being pulled up due to capacitive coupling from the drain to the gate of the low-side MOSFET when the inductor switching node (LX_) transitions from ground to V_{IN}. The capacitive coupling between LX_ and DL_ created by the MOSFET's gate-to-drain capacitance (C_{RSS}), gate-to-source capacitance (C_{ISS} - C_{RSS}), and additional board parasitics should not exceed the following minimum threshold to prevent shoot-through currents:

$$V_{GS(TH)} > V_{IN(MAX)}\left(\frac{C_{RSS}}{C_{ISS}}\right)$$

Adding a 4700pF between DL_ and power ground (C_{NL} in Figure 13), close to the low-side MOSFET greatly reduces coupling. Do not exceed 22nF of total gate capacitance to prevent excessive turn-off delays. Shoot-through currents can also be caused by a combination of fast high-side MOSFET and slow low-side MOSFET. If the turn-off delay time of the low-side MOSFET is too long, the high-side MOSFET can turn on before the low-side MOSFET has actually turned off. Adding a resistor less than 5Ω in series with BST_ slows down the high-side MOSFET turn-on time, eliminating the shoot-through currents without degrading the turn-off time (R_{BST} in Figure 13). Slowing down the high-side MOSFET also reduces the LX_ node rise time, thereby reducing EMI and high-frequency coupling responsible for switching noise.

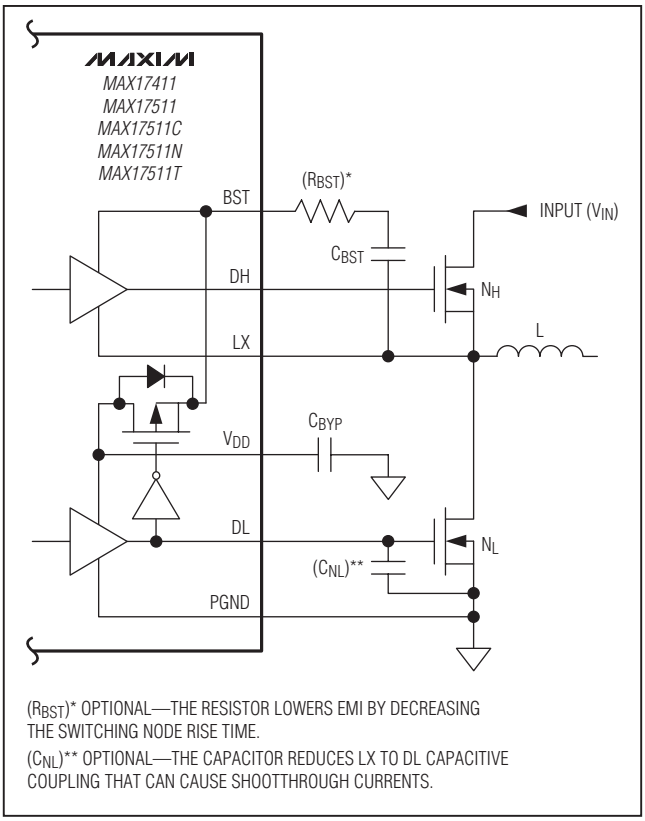

Figure 13. Gate-Drive Circuit

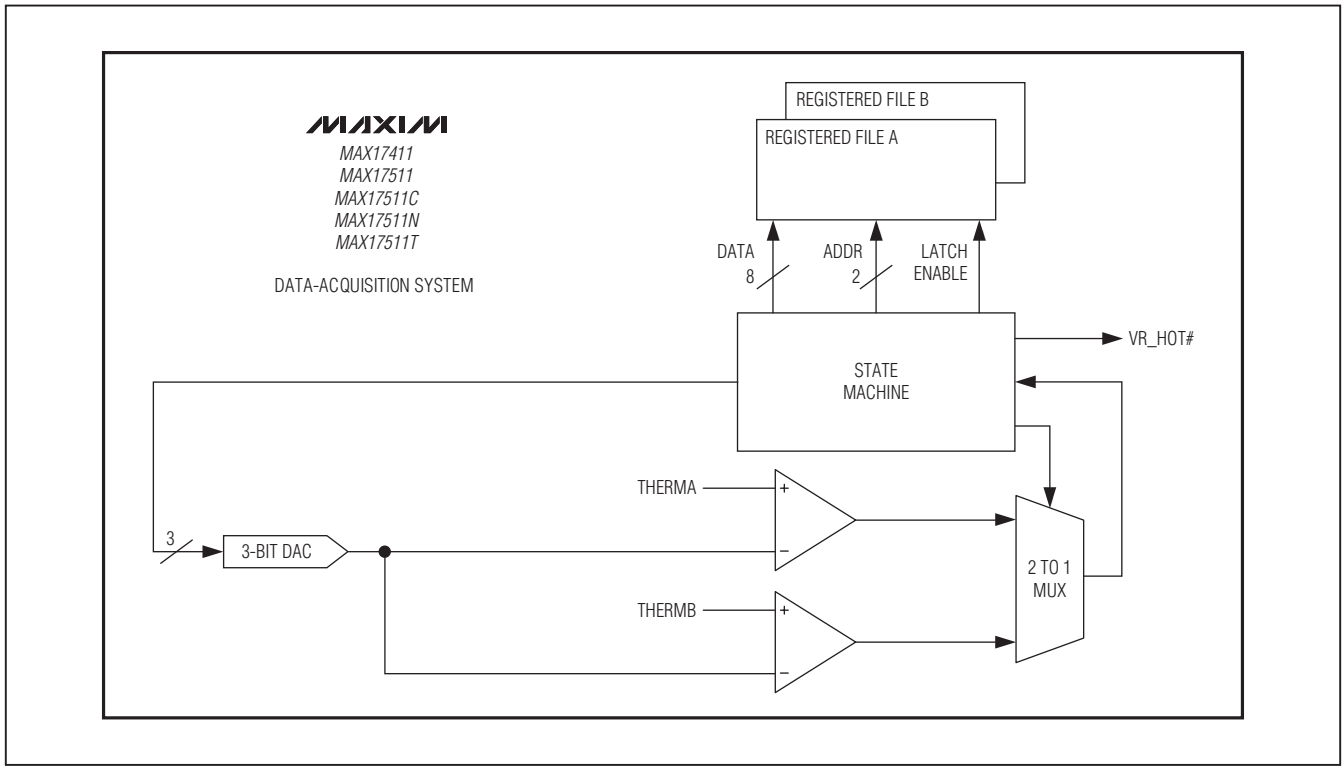

Figure 14. Data-Acquisition System Block Diagram

External Drivers and Disabling Phases

The MMAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T support an external driver, MAX17491, for three-phase operation in regulator A. The MAX17411 also supports an external driver for two-phase operation of regulator B. The DRVPWM_ output provides the signal to trigger the driver. Connecting CSPA3/CSPB2 to V_{CC} disables phase 3 of regulator A and phase 2 of regulator B, respectively. Similarly, phase 2 can be disabled for single-phase operation by connecting CSPA2 to V_{CC}.

Data-Acquisition System

The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T include current and thermal-monitoring functions. A simplified data-acquisition system is employed to convert the analog signals from the current-sense and THERM_ inputs to 8-bit and 3-bit values in the ICC_MAX and Temperature Zone registers, respectively (see Figure 14). An independent VR_HOT# output is available to make certain the system is alerted to an overtemperature fault in the event of SVID bus failure.

Serial VID Interface, Commands, Registers, and Digital Control

A simplified block diagram of the SVID interface for the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T is shown in Figure 15. The interface consists of a high-speed transceiver, control logic, and two independent, identically configured register files for regulators A and B. Refer to Intel's VR12/IMVP-7 SVID protocol documentation for complete details on the interface and the required configuration of SVID data packets.

Regulator Addressing

The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T do not feature programmable addressing. Regulator A is hard coded to be SVID bus address 0, and regulator B is hard coded to be SVID bus address 1.

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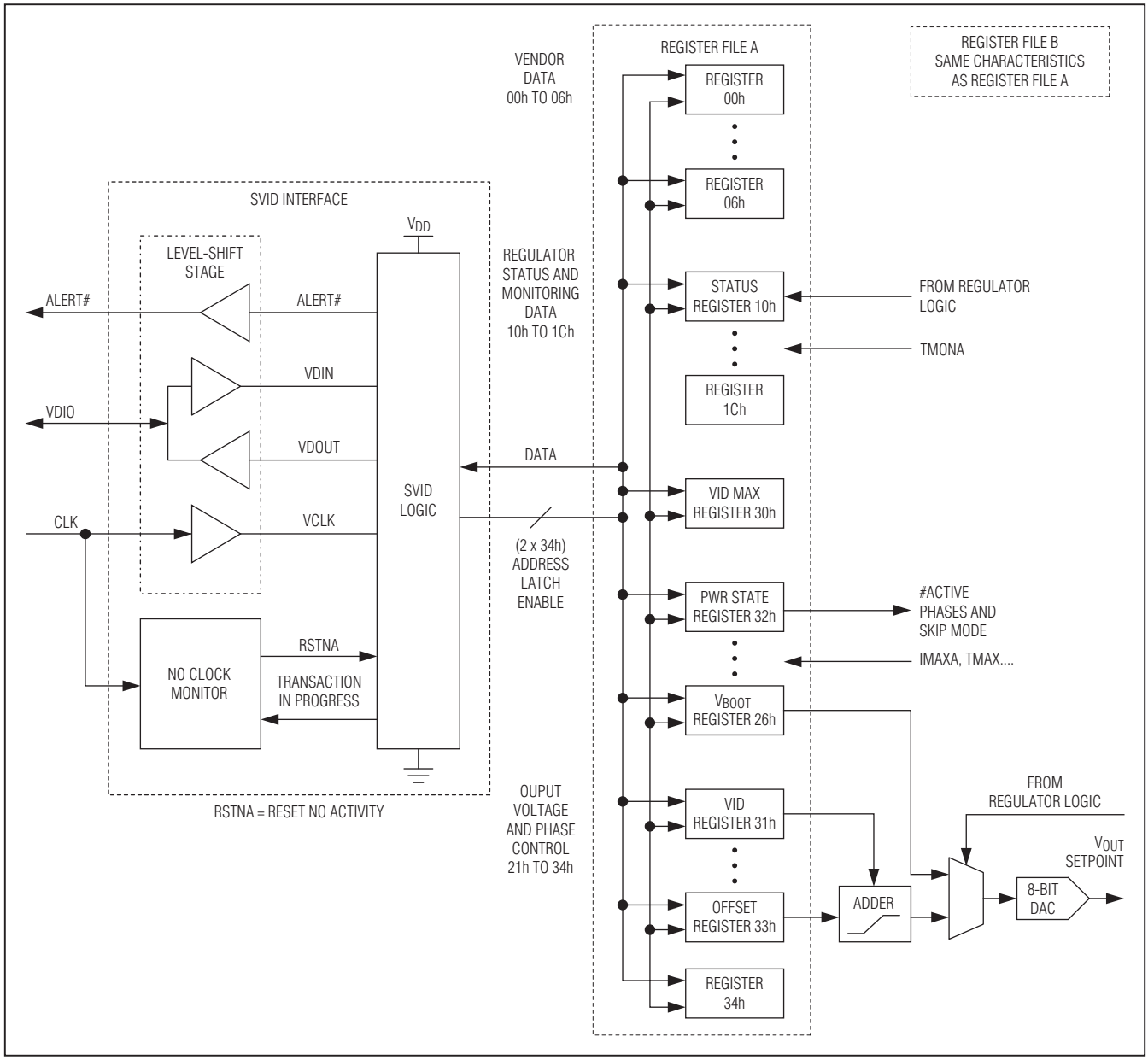

Figure 15. SVID Interface Block Diagram

Serial VID Commands

The MMAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T support the following commands (Table 4) and registers according to Intel's VR12/IMVP-7 protocol specification. Note the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T support ALL CALL commands according to Intel specification. For ALL CALL commands write 1111b or 1110b in the address command bit.

SetVID_Fast (01h)

The SetVID_Fast command contains the target SVID in the payload byte. The output voltage range is defined in Table 3. The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T drive the respective output voltages to the new VID setting with a fast slew rate as defined in the SR_Fast register (24h). This register is programmed with the SR pin. The default fast slew rate is 10mV/µs.

The SetVID_Fast command is preemptive. If the SVID bus master interrupts current transition and attempts to move the output to a new VID, the regulator responds immediately after registering the new command. With back-to-back SetVID commands, the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T reset the ALERT# line after the ACK and start moving the output voltage to the new target. For the case of back-to-back SetVID commands to the same voltage, the VR asserts ALERT# immediately since there is no settling time.

Table 4. Serial VID Commands

COMMAND		MASTER PAYLOAD	SLAVE PAYLOAD	DESCRIPTION
00h	Extended	Extended Command Index	—	Not supported
01h	SetVID-Fast	VID Code	N/A	Command sets the new SVID target (up or down) at the fast slew rate programmed by the SR input. When the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T receive an SVID code for an upward transition, they exit all low-power states to PS0 to ensure the fastest slew to the new voltage. When the output reaches the new VID target, the VR_Settled bit is set and ALERT# goes low.
02h	SetVID-Slow	VID Code	N/A	Command sets the new SVID target (up or down) at the slow slew rate equal to 1/4 the fast slew rate programmed by the SR input. When the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T receive an SVID code for an upward transition, it exits all low-power states to PS0 to ensure the fastest slew to the new voltage. When the output reaches the new VID target, the VR_Settled bit is set and ALERT# goes low.
03h	SetVID-Decay	VID Code	N/A	Command sets the new SVID target but **does not** control the slew rate. The output is allowed to decay at a rate defined by the load. This command is used for only high-to-low output transitions. When the output reaches the new VID target, The VR_Settled bit is set but ALERT# does not go low.
04h	SetPS	Byte Indicating Power Status of CPU	N/A	Command sets the power state PS_ of the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T so they can enable the correct number of phases and control SKIP mode for optimized operation. See the *Power States (PS)* section.
05h	SetRegADR	Address of the Index in the Register File, see Table 5	N/A	Command sets the address pointer in the data register table. Typically, the next command, SetRegDAT, is the payload that gets loaded into this address. However, for multiple writes to the same address, only one SetRegADR is needed.
06h	SetRegDAT	New Data Register Contents	N/A	Command writes the contents to the data register that was previously identified by the address pointer with SetRegADR.
07h	GetReg	Define Which Register	Specified Register Contents	Command returns the contents of the specified register as the payload. See the *Data and Configuration Registers* section for a description of supported registers.
08h	TestMode	—	—	—
09h–1Fh	Reserved	—	N/A	—

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SetVID_Slow (02h)

The SetVID_Slow command contains the target SVID in the payload byte. The output voltage range is defined in Table 3. The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T drive the respective output voltage to the new VID setting with a slow slew rate as defined in the SR_Slow register (25h). SetVID_Slow transitions occur at 1/4 the fast slew rate. The SetVID_Slow command is preemptive. If the SVID bus master interrupts current transition and attempts to move the output to a new VID, the regulator responds immediately after registering the new command. With back-to-back SetVID commands, the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T reset the ALERT# line after the ACK and start moving the output voltage to the new target. For the case of back-to-back SetVID commands to the same voltage, the VR asserts ALERT# immediately since there is no settling time.

SetVID_Decay (03h)

The SetVID_Decay command contains the target SVID in the payload byte. The range of voltage is defined in Table 3. It is used for VID down transitions. The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T do not control the slew rate, instead the output voltage decays at a rate defined by the output load current.

The SetVID_Decay command is preemptive for positive-going SetVID_Fast or SetVID_Slow commands. If the SVID bus master interrupts current transition and attempts to move the output to a new VID, the regulator responds immediately after registering the new command. The ALERT# line remains high during the SetVID_Decay transition. The SVID bus master normally does not issue a SetVID_Decay with target voltage higher than current setting. If this occurs, the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T reject the command (Acknowledge = 11b) and remain at the same voltage setting.

SetPS_ Set Power State (04h)

The SetPS command sends a byte that is encoded as to the power state of the CPU. Based on the power-state command, the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T can change their configuration to meet the processor's power needs with greater efficiency. See the *Power States (PS)* section. The format of the SetPS command payload is:

B7	B6	B5	B4	B3	B2	B1	B0
PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0

If the SVID bus master attempts to program a power state that is not supported, the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T acknowledge with NAK (01b) and enter the lowest power state that is supported. The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T enter the new power state after sending back the ACK of the SetPS command. If the devices are in low-power states and receive a SetVID_ command (either up or down), the target regulators exit the low-power state to normal mode (PS0) to move the voltage up at the requested slew rate and reset the power-state register to 00h when they acknowledge the SetVID (UP) command. The microprocessor must reissue a low-power state command if it is in a low-current condition at the new higher voltage.

The SetPS command is not preemptive; the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T wait until it has completed the previous command or the output has settled, then they change power state. If the VR receives a SetPS command while it is still slewing from the previous SetVID command, the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T reject (11b) the SetPS command, indicating they cannot carry out the command. These devices enter the new power state after they send back the ACK of the SetPS command.

If the VR receives a SetPS command while it is still slewing down from a SetVID_Decay command, then the VR enters the new power state, slewing down with the decay rate.

SetRegADR (05h), SetRegDAT (06h), and GetReg (07h)

Accessing the register files of the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T is accomplished with three commands: SetRegADR, SetRegDAT, and GetReg. SetRegADR sets the target register address, SetRegDAT writes data to the specified register, and GetReg retrieves data from the specified register. To program a register, two commands must be executed in order. SetRegADR chooses the address in Table 5 and then the next command is a SetRegDAT to write or set the data into the previously defined address. For multiple writes to the same address, only one SetRegADR command is sent, followed by multiple SetRegDAT commands.

All the telemetry data from the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T is accessed through the GetReg command. The payload byte in the command contains an index into the data register file. A slave device that receives the GetReg command must insert the contents of the indexed data register into the payload of the response.

If SVID bus master issues a SetRegADR or GetReg command that contains a nonsupported address, the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T respond with the REJECT (11b) acknowledge. If SVID bus master issues an ALL CALL SetRegADR, SetRegDAT, or GetReg, the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T respond with the not NAK (01b).

Data and Configuration Registers

The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T support the data and configuration registers listed in Table 5. The registers retain data as long as V_{CC} is powered up and in regulation. During hard reset (EN = low) or power cycle, all data is lost and registers return to default contents. Regulator A and regulator B include separate, independent register files.

Access definitions for these registers are as follows:

- RO = Read only.
- RW = Read write.
- R-M = Read by SVID bus master (CPU).
- W-PWM = Written by the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T only.
- HC = Hard coded into the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T.
- Platform = Programmed at PCB assembly using pin strapping—cannot be overwritten by master.
- Master = Programmed by the SVID bus master through the SVID bus with the SetRegADR, SetRegDAT.
- PWM = Programmed by the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T during operation for reporting information to the master.

Table 5. Data and Configuration Register File Definition

INDEX	REGISTER NAME	DESCRIPTION	ACCESS	DEFAULT
00h	Vendor ID	The vendor ID is unique to Maxim and is assigned by Intel	RO HC	17h
01h	Product ID	Uniquely identifies the MAX17411/MAX17511 products	RO HC	01h
02h	Product Revision	Uniquely identifies the revision or stepping of the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T	RO HC	01h
03h	Vendor Product Date Code (Year/Month)	Not supported	—	N/A
04h	Lot Code	Not supported	—	N/A
05h	Protocol ID	Identifies what version of SVID protocol is supported by the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T	RO HC	01h
06h	Capability	SVID capability register	RO HC	01h
07h–0Eh	Not Used	—	—	—
0Fh	Vendor Product Date Code (Day/Time)	Not supported	—	N/A
10h	Status1	Data register containing the Status1 data. This register is read after the ALERT# signal is asserted. It communicates the status of the MAX17411/MAX17511. Status1 is cleared after a GetReg(10h) command.	R-M W-PWM	00h
11h	Status2	Data register containing the Status2 data (SerialVID Errors). Status2 is cleared after a GetReg(11h) command.	R-M W-PWM	00h

Table 5. Data and Configuration Register File Definition (continued)

INDEX	REGISTER NAME	DESCRIPTION	ACCESS	DEFAULT
12h	Temperature Zone	Data register containing the measurement data from the THERM_ input.	R-M W-PWM	00h
13h	Current Zone	Not supported	—	N/A
14h	Reserved	—	—	—
15h	Output Current	Not supported	—	00h
16h	Output Voltage	Not supported	—	N/A
17h	Temperature	Not supported	—	N/A
18h	Output Power	Not supported	—	N/A
19h	Input Current	Not supported	—	N/A
1Ah	Input Voltage	Not supported	—	N/A
1Bh	Input Power	Not supported	—	N/A
1Ch	Status2_LastRead	This register contains a copy of the Status2 data that was last read with the GetReg(Status2) command. In the case of a communications error or parity error, when the MAX17411/MAX17511/MAX17511C/ MAX17511N/MAX17511T send the payload back to the SVID bus master, the master can read the Status2_ LastRead register so the alert data is not lost.	R-M W-PWM	00h
1Dh–20h	Not Used	—	—	—
21h	ICC_MAX (Maximum Output Current Capability)	Data register containing the maximum output current limit that the regulator supports. The register uses a binary format in amps, e.g., 64h = 100A.	RO Platform	Based on the IMAX_ logic voltage level input
22h	Temp MAX	Data register containing the temperature max the platform supports and the level VR_HOT# asserts. This register contains a fixed value of +100°C. Binary format in °C, e.g., 64h = +100°C.	RO HC	64h
23h	DC Load-Line	Not supported	—	N/A
24h	SR_Fast	Data register containing the fast slew-rate capability of the MAX17411/MAX17511/MAX17511C/MAX17511N/ MAX17511T programmed at the SR input. Register format is in mV/µs, e.g., 0Ah = 10mV/µs.	RO Platform	0Ah = (10mV/µs)
25h	SR_Slow	Data register containing the slow slew-rate capability of the MAX17411/MAX17511/MAX17511C/MAX17511N/ MAX17511T. This value is 1/4 the rate programmed at the SR input. Register format is in mV/µs, e.g., 02h = 2.5mV/µs.	RO Platform	02h = (2.5mV/µs)
26h	V_{BOOT}	Data register containing the boot voltage. The register uses SVID data format, e.g., 97h = 1.0V.	RO HC	83h (0.9V) for Reg B of MAX17511C. ABh (1.1V) for MAX17511N, 00h (0V) for other devices

Table 5. Data and Configuration Register File Definition (continued)

INDEX	REGISTER NAME	DESCRIPTION	ACCESS	DEFAULT
27h	VR tolerance	Not supported	—	N/A
28h	Current Offset	Not supported	—	N/A
29h	Temperature Offset	Not supported	—	N/A
2Ah–2Fh	Not Used	—	—	—
30h	V_{OUT}_MAX	This register is programmable by the master and sets the maximum VID the MAX17411/ MAX17511/ MAX17511C/ MAX17511N/MAX17511T support. If a higher VID code is received, the MAX17411/ MAX17511/MAX17511C/MAX17511N/MAX17511T respond with “not supported” acknowledge. The register uses SVID data format. This register must be programmed by MASTER during boot-up sequence.	RW Master	FBh (1.5V)
31h	VID Setting	Data register containing currently programmed VID voltage. The register uses SVID data format.	RW Master	00h
32h	Power State	Register containing the current programmed power state.	RW Master W-PWM	00h
33h	VID Offset (Voltage Margining)	This register contains an offset added to the programmed SVID data. Data format is the number of SVID steps. Negative offsets are in the two’s-complement format. See the *Offset Register (33h)* section.	RW Master	00h
34h	Multi-VR Configuration	This register contains the bit-mapped data for configuring multiple regulators that utilize the SVID bus.	RW Master	00h
35h	SerRegADR	This register is a scratchpad register for temporarily storing the SetRegADR payload. The data is the address pointer for subsequent SetRegDAT commands.	RW Master	00h
36h–6Fh	Not Used	—	—	—

Status1 Register (10h)

The data in the Status1 register answers the following questions: Is the output voltage in regulation? Is the regulator temperature approaching the thermal limit? Is the regulator's output current approaching current limit? Also, should the SVID bus master check the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T for SVID data errors in the Status2 register? When there are any bit changes in Status1, the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T assert the ALERT# to notify the SVID bus master to start the polling process of reading the status from each address on the bus.

Bit 0 in Status1 indicates that a SetVID command is completed and the output voltage has transitioned to within ±10mV (max) of the final target voltage. During VR slewing/transitioning, the VR_Settled bit is "0". Bit 1 indicates that the VR temperature (in Temperature Zone register value (12h)) has reached 97% of the maximum temperature set in the Temp MAX register (22h). Bit 2 indicates an overcurrent condition. The ICC MAX Alert bit (bit 2) is latched when it sets high. A GetReg (Status1) command updates this latched bit. Bit 7 indicates that a Status2 register change was recorded. When either bit 0, 1, 2, or 7 changes, the respective registers should be read to take further action. The format of the Status1 register is:

B7	B6	B5	B4	B3	B2	B1	B0
Read Status2	RSV 0b	RSV 0b	RSV 0b	RSV 0b	ICC MAX Alert (Latched)	Therm Alert	VR_Settled

The bit values in the Status1 register reflect the most current status and a GetReg (Status1) command does not clear them.

Status2 Register (11h)

Parity and data frame errors are recorded in the Status2 register. When the SVID bus master reads Status2, the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T copy the contents into Status2_LastRead register (1Ch), then clear the contents of the Status2 register. In the case of a parity error in the payload, the master can read the Status2_LastRead register to get the status prior to reset.

The format of Status2 register is:

B7	B6	B5	B4	B3	B2	B1	B0
RSV 0b	RSV 0b	RSV 0b	RSV 0b	RSV 0b	RSV 0b	SVID Data Frame Error	SVID Parity Error

Temperature Zone Register (12h)

The digitized measurements from the thermistor bridges at THERMA and THERMB are recorded in the Temperature Zone register. The required thresholds of the Temperature Zone register are nonlinear, but equate to increments listed below. It is essential to use the correct resistor and thermistor values specified in Figures 1, 2, and 3. When 97% TMAX (bit 6) for either is exceeded at either THERMA or THERMB, bit 1 of Status1 register (10h) is set and ALERT# asserts low. When 100% TMAX bit (bit 7) for either regulator is set, VR_HOT# is pulled low. For each regulator, place the thermistor as close to the MOSFETs and inductors as possible. The MAX17411/MAX17511 EV kits provide good examples of thermistor placement.

The Temperature Zone register and VR_HOT# functions are independent. In the event of an SVID bus problem, the VR_HOT# signal always responds correctly to force thermal throttling to prevent the CPU from catastrophically overheating. The format of the Temperature Zone Register is:

VR_HOT#	THERMISTOR ALERT	COMPARATOR TRIP POINTS AND EXAMPLE TEMPERATURES SCALED TO +100°C = 100%					
B7	B6	B5	B4	B3	B2	B1	B0
100%	97%	94%	91%	88%	85%	82%	75%
EXAMPLE REGISTER CONTENTS FOR +95°C							
0	0	1	1	1	1	1	1

Status2_LastRead (1Ch)

This register contains a copy of the Status2 data that was last read with the GetReg (Status2) command. In the case of a communications error or parity error, when the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T send the payload back to the SVID bus master, the master can read the Status2_LastRead register so the alert data is not lost.

Temp Max (22h)

This register contains the maximum temperature the VR supports prior to issuing a thermal alert or VR_HOT#. Temp MAX is set to +100°C.

The single-temperature threshold applies to both regulators A and B. The data in this register is in 8-bit binary format in degrees C, e.g., 64h = +100°C.

Platform Performance Registers

These registers are programmed on the platform PCB during manufacturing. The data tells the SVID bus master the performance capability of the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T. Multivalued logic inputs are used to set the data in these registers.

ICC_MAX (21h)

This register contains information on the maximum current the motherboard VR supports. ICC_MAX is programmed with the IMAX_ multivalue logic input. The current limit computed from IMAX_ is multiplied by the number of active phases in the regulator to determine the data in the ICC_MAX register. If the voltage applied to the IMAX_ input is not within the defined threshold (e.g., IMAX shorted to ground or V_{CC}) the respective regulator is disabled. The data in this register is 8-bit binary format in amps (1A/LSB), e.g., 4Bh = 75A. See Table 6.

SR Fast (24h)

This register contains the guaranteed minimum fast slew-rate data programmed at the SR multivalued logic input. The default slew rate is 10mV/µs (min). The data is in 8-bit binary format in dV/dt, e.g., 10mV/µs = 0Ah. See Table 7.

If NTC is used in the current-sensing network (CSP_, CSN_), set V_{SR} at 1.5V for 20mV/µs and 0V for 10mV/µs fast slew rate. Otherwise, V_{SR} = 3V sets the fast slew rate at 20mV/µs and V_{SR} = V_{CC} sets it at 10mV/µs.

SR Slow (25h)

This register contains the guaranteed minimum slow slew-rate data, which is 1/4 the value programmed at the SR input. The data is in 8-bit binary format in dV/dt, e.g., 2mV/µs = 02h. See Table 7.

If NTC is used in the current-sensing network (CSP_, CSN_), set V_{SR} at 1.5V for 5mV/µs and 0V for 2.5mV/µs slow slew rate. Otherwise, V_{SR} = 3V sets the slow slew rate at 5mV/µs and V_{SR} = V_{CC} sets it at 2.5mV/µs.

Table 6. Current-Limit Setting (V_{SR} = 0V or V_{SR} = 1.5V)

IMAX_ LEVEL NO.	VOLTAGE LEVEL (V)	R_{SENSE} (mΩ)	REG A MINMUM V_{SENSE} (mV)	REG A PHASE OCP CURRENT (A)	REG A PHASE ICC_MAX REPORT (A)	REG B MiINIMUM V_{SENSE} (mV)	REG B PHASE OCP CURRENT (A)	REG B PHASE ICC_MAX REPORT (A)
0	< 13.65 x V_{CC}/50	—	—	Latched Off	—	—	Latched Off	—
1	14.5 x V_{CC}/50	0.65	22.5	39	35	22.5	39	35
2	15.5 x V_{CC}/50	0.65	21.5	36	33	21.5	36	33
3	16.5 x V_{CC}/50	0.65	17.0	30	27	13.0	23	22
4	17.5 x V_{CC}/50	0.65	15.0	26	22	11.0	20	17
5	18.5 x V_{CC}/50	0.75	27.0	39	35	27.0	39	35
6	19.5 x V_{CC}/50	0.75	25.0	36	33	25.0	36	33
7	20.5 x V_{CC}/50	0.75	20.0	30	27	15.0	23	22
8	21.5 x V_{CC}/50	0.75	17.0	26	22	13.0	20	17
9	22.5 x V_{CC}/50	0.85	30.0	39	35	30.0	39	35
10	23.5 x V_{CC}/50	0.85	28.0	36	33	28.0	36	33
11	24.5 x V_{CC}/50	0.85	22.5	30	27	17.0	23	22

Table 6. Current-Limit Setting (V_{SR} = 0V or V_{SR} = 1.5V) (continued)

IMAX_ LEVEL NO.	VOLTAGE LEVEL (V)	R_{SENSE} (mΩ)	REG A MINMUM V_{SENSE} (mV)	REG A PHASE OCP CURRENT (A)	REG A PHASE ICC_MAX REPORT (A)	REG B MiINIMUM V_{SENSE} (mV)	REG B PHASE OCP CURRENT (A)	REG B PHASE ICC_MAX REPORT (A)
12	25.5 x V_{CC}/50	0.85	20.0	26	22	15.0	20	17
13	26.5 x V_{CC}/50	0.95	33.5	39	35	33.5	39	35
14	27.5 x V_{CC}/50	0.95	31.0	36	33	31.0	36	33
15	28.5 x V_{CC}/50	0.95	25.0	30	27	20.0	23	22
16	29.5 x V_{CC}/50	0.95	21.5	26	22	17.0	20	17
17	> 30.2 x V_{CC}/50	—	—	Latched Off	—	—	Latched Off	—

See the Electrical Characteristics *table for minimum V_{SENSE} for V_{SR} = 3V or V_{SR} = 5V.*

Table 7. Programmed Slew-Rate Data

V_{SR} (V)	NTC for CSP_ SIGNALS	FAST SLEW RATE (MIN) (mV/µs)	MINIMUM VALUE REPORTED IN 24h	SLOW SLEW RATE (MIN) (±mV/µs)	MINIMUM VALUE REPORTED IN 25h
0	Yes	10	0Ah	2.5	02h
1.5	Yes	20	14h	5	04h
3	No	20	14h	5	04h
V_{CC}	No	10	0Ah	2.5	02h

V_{BOOT} (26h)

This register is programmed by the platform designer and contains the boot voltage value. The VID Setting of 00h sets the boot voltage as 0V. With this setting, the output voltage does not ramp up at power-up until the MAX17411/MAX17511/MAX17511T receive a SetVID command. If V_{BOOT} is set to any other code, the output voltage ramps to the selected VID DAC setting on assertion of enable (EN = high). The output voltage maintains its value until a SetVID command sets a new target. The default value for V_{BOOT} register is 00h for the MAX17411/MAX17511/MAX17511T and Reg A of the MAX17511C. The default value for the V_{BOOT} register is ABh for the MAX17511N. It is programmed in an 8-bit binary format. The default value for the V_{BOOT} register is 83h for Reg B of the MAX17511C.

V_{OUT}_MAX (30h)

This register is programmed by the CPU or SVID bus master to the maximum output voltage the CPU load can support. Any attempts to set the SVID above V_{OUT}_MAX are blanked and ignored. The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T respond with “not-supported” acknowledge. The default value is FBh (1.5V).

VID Setting (31h)

This register contains a copy of the currently programmed SVID data. The default value is 00h.

Power State PS_ (32h)

The PS register contains information on the CPU's power-consumption status. The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T support states PS0 through PS3. See the *Power States (PS)* section for a complete description of these states and the resulting operating mode change in the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T. If a power state is requested that is not supported by these devices, they acknowledge with command rejected (11b) back to the SVID bus master. The PS_ register format is:

B7	B6	B5	B4	B3	B2	B1	B0
PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0

Offset Register (33h)

This register contains an offset, which is added to the programmed SVID data. The format of this data is the number of SVID steps/LSBs. For negative offsets, the value is the two's complement of the number of SVID steps. The format of the Offset register is:

OFFSET OR VOLTAGE MARGIN							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Sign 0 = + 1 = -	SVID6	SVID5	SVID4	SVID3	SVID2	SVID1	SVID0

Default = 00h = no offset.

Bit 7 = Sign bit.

00000001 = 01h = +1 LSB Offset.

00000011 = 03h = +3 LSB Offset.

10000001 = 81h = -127 LSB Offset.

Multi-VR Configuration Register (34h)

This register contains the bit-mapped data for configuring multiple regulators that utilize the SVID bus.

Bit 0 (POK 0V) changes the response of the POK_ power-good output. Writing a 0 (default) to this bit enables the standard definition for POK_ response. When a SetVID (0.0V) command is issued, the respective regulator turns off and POK_ deasserts to 0V. Writing a 1 to bit 0 causes POK_ to remain high when SetVID (0.0V) is issued and POK_ only goes low under fault conditions or when the regulator is powered down using EN or the input supplies turn off.

Bit 1 (LOCK VID/PS) controls a lock function for the SVID code and power state PS. When bit 1 is a 0, the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T are in normal mode and the SVID and PS are NOT locked. When bit 1 is a 1, the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T lock the SVID and PS data and reject all SetVID and SetPS commands. Bit 1 must be changed back to 0 before the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T accept new commands. The format of the Multi-VR register is:

MULTI-VR CONFIGURATION (34h)							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
RSV 0b	RSV 0b	RSV 0b	RSV 0b	RSV 0b	RSV 0b	LOCK VID/PS	POK 0V

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SetRegADR Register (35h)

This register is a scratchpad register for temporarily storing the SetRegADR payload. The data is the address pointer for subsequent SetRegDAT commands.

Critical VR12/IMVP-7 Functions

Voltage-Settled Function

The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T include an auxiliary bank of comparators that detect when the SVID transition is complete and the output voltage is within ±10mV (2 LSB) of the new target VID setting. After the output has settled, the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T set the VR_Settled bit in the Status1 register and assert the ALERT# line.

Power States (PS)

The SVID bus can be used to place the MAX17411/MAX17511/M17511C/MAX17511N/MAX17511T into multiple operating states to optimize the efficiency and power delivery capability. These states are entered by issuing a SetPS command and the programmed state is reflected in the power-state register (32h). The power states are listed in order of power savings:

PS0 = Represents full power or active mode.

PS1 = Used in active mode or sleep mode and it represents a low-current state.

PS2 = Used in sleep mode and it represents a low-voltage state and lower current state than PS1.

PS3 = Ultra-low-power sleep mode.

PS4–PS7 are not defined.

The SVID code and power states are independent and can change at any time as determined by the CPU operating state. When the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T exit any low-power state, they automatically enter PS0 for any SVID command (SetVID_Fast/SetVID_Slow) that causes the output to change from the previous value. Note the SVID bus master must reissue a low-power state command to return the MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T to a low-current condition at the new higher voltage.

After exiting a low-power state, the CPU waits 3.3µs prior to entering the full-power mode. Regulators A and B respond identically to the PS_ commands described in Table 8. Regulator B controls phase 1 (MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T) and phase 2 (MAX17411).

Multiphase Quick-PWM Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

Input Voltage Range: The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case high AC adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest input voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.

Maximum Load Current: There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements, and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of the input capacitors, MOSFETs, and other critical heat-contributing components. Modern notebook CPUs generally exhibit $I_{LOAD} = 0.8 \times I_{LOAD(MAX)}$. For multiphase systems, each phase supports a fraction of the load, depending on the current balancing. When properly balanced, the load current is evenly distributed among each phase:

$$I_{LOAD(PHASE)} = \frac{I_{LOAD}}{N_{TOTAL}}$$

where N_{TOTAL} is the total number of active phases.

Table 8. Power State (PS) Control of Regulator Operation

PS_	PHASE 1	PHASE 2	PHASE 3	SKIP	COMMENTS
0	1	1	1	0	Full-power FPWM mode
1	1	0	0	0	1-phase FPWM
2	1	0	0	1	1-phase SKIP
3	1	0	0	1	1-phase SKIP
4–7	—	—	—	—	Not used

Switching Frequency: This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage due to MOSFET switching losses that are proportional to frequency and V_{IN}^2. The optimum frequency is also a moving target due to rapid improvements in MOSFET technology that is making higher frequencies more practical.

Inductor Operation Point: This choice provides trade-offs between size vs. efficiency and transient responses vs. output noise. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output noise due to increased ripple current. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually between 30% and 50% ripple current. For a multiphase core regulator, select an LIR value of ~0.4.

Inductor Selection

The switching frequency and operating point (% ripple current or LIR) determine the inductor value as follows:

$$L = N_{TOTAL}\left(\frac{V_{IN} - V_{OUT}}{f_{SW} \times I_{LOAD(MAX)} \times LIR}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)$$

where N_{TOTAL} is the total number of phases. Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The core must not saturate at the peak-inductor current (I_{PEAK}):

$$I_{PEAK} = \left(\frac{I_{LOAD(MAX)}}{N_{TOTAL}}\right)\left(1 + \frac{LIR}{2}\right)$$

Output Capacitor Selection

Output capacitor selection is determined by the controller stability and the transient soar and sag requirements of the application.

Output Capacitor ESR

The output-filter capacitor must have low enough effective series resistance (ESR) to meet output ripple and load-transient requirements, yet have high-enough ESR to satisfy stability requirements. In CPU V_{CORE} converters and other applications where the output is subject to large-load transients, the size of the output capacitor typically depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$(R_{ESR} + R_{PCB}) \le \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

The output-voltage ripple of a step-down controller equals the total inductor ripple current multiplied by the output-capacitor's ESR. When operating multiphase out-of-phase systems, the peak inductor currents of each phase are staggered, resulting in lower output ripple voltage by reducing the total inductor ripple current. For multiphase operation, the maximum ESR to meet ripple requirements is:

$$R_{ESR} \le \left[\frac{V_{IN} \times f_{SW} \times L}{(V_{IN} - (N_{TOTAL} \times V_{OUT}))\, V_{OUT}}\right] V_{RIPPLE}$$

where N_{TOTAL} is the total number of active phases and f_{SW} is the switching frequency per phase.

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true for polymer types). When using low-capacity ceramic filter capacitors, capacitor size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the V_{SAG} and V_{SOAR} equations in the *Transient Response* section).

Output Capacitor Stability Considerations

For Quick-PWM controllers, stability is determined by the value of the ESR zero relative to the switching frequency. The boundary of instability is given by the following equation:

$$f_{ESR} \le \frac{f_{SW}}{\pi}$$

where:

$$f_{ESR} = \frac{1}{2\pi \times R_{EFF} \times C_{OUT}}$$

and:

$$R_{EFF} = R_{ESR} + R_{DROOP} + R_{PCB}$$

where C_{OUT} is the total output capacitance, R_{ESR} is the total equivalent series resistance, R_{DROOP} is the voltage-positioning gain, and R_{PCB} is the parasitic board

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resistance between the output capacitors and sense resistors.

For a standard 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz. Tantalum, SANYO POSCAP, and Panasonic SP capacitors are widely used and have typical ESR zero frequencies below 50kHz. In the standard application circuit, the ESR needed to support a 30mV$_{P-P}$ ripple is 30mV/(40A x 0.3) = 2.5mΩ. Four 470µF/2.5V Panasonic SP (type SX) capacitors in parallel provide 1.5mΩ (max) ESR. With a 2mΩ droop and 0.5mΩ PCB resistance, the typical combined ESR results in a zero at 30kHz. Ceramic capacitors have a high-ESR zero frequency, but applications with significant voltage positioning can take advantage of their size and low ESR. When using only ceramic output capacitors, output overshoot (V_{SOAR}) typically determines the minimum output capacitance requirement. Their relatively low capacitance value favors high-switching-frequency operation with small inductor values to minimize the energy transferred from inductor to capacitor during load-step recovery. Unstable operation manifests itself in two related but distinctly different ways: double pulsing and feedback loop instability.

Double-Pulsing and Feedback Loop Instability

Double pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output-voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the minimum off-time period has expired. Double pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability can result in oscillations at the output after line or load steps. Such perturbations are usually damped, but can cause the output voltage to rise above or fall below the tolerance limits. The easiest method for checking stability is to apply a very fast 10% to 90% max load transient and carefully observe the output-voltage ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

Transient Response

The inductor ripple current impacts transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The amount of output sag is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time. For a multiphase controller, the worst-case output sag voltage can be determined by:

$$V_{SAG} \approx \frac{L(\Delta I_{LOAD(MAX)})^2}{2N_{TOTAL} \times C_{OUT} \times V_{OUT}} \times \frac{t_{MIN}}{[Kt_{SW} - t_{MIN}]}$$

and:

$$t_{MIN} = t_{ON} + t_{OFF(MIN)}$$

where $t_{OFF(MIN)}$ is the minimum off-time (see the *Electrical Characteristics* table), Kt_{SW} is the programmed switching period, and N_{TOTAL} is the total number of active phases. K = 66% when N_{PH} = 3, and K = 100% when N_{PH} = 2. V_{SAG} must be less than the transient droop $\Delta I_{LOAD(MAX)} \times R_{DROOP}$. The capacitive soar voltage due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{(\Delta I_{LOAD(MAX)})^2 L}{2N_{TOTAL} \times C_{OUT} \times V_{OUT}}$$

The actual peak of the soar voltage depends on the time where the decaying ESR step and rising capacitive soar are at their maximum. This is best simulated or measured.

Input Capacitor Selection

The input capacitor must meet the ripple-current requirement (I_{RMS}) imposed by the switching currents. The multiphase Quick-PWM controllers operate out-of phase, reducing the RMS input. The I_{RMS} requirements can be determined by the following equation:

$$I_{RMS} = \left(\frac{I_{LOAD}}{N_{TOTAL} \times V_{IN}}\right) \times \sqrt{N_{TOTAL} \times V_{OUT}\left(V_{IN} - (N_{TOTAL} \times V_{OUT})\right)}$$

where N_{TOTAL} is the total number of out-of-phase switching regulators. The worst-case RMS current requirement occurs when operating with V_{IN} = 2(N_{TOTAL} x V_{OUT}). Therefore, the above equation simplifies to I_{RMS} = 0.5 x (I_{LOAD}/N_{TOTAL}). Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal circuit longevity.

Power MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high-load-current capability when using high-voltage AC adapters.

High-Side MOSFET Power Dissipation

The conduction loss in the high-side MOSFET (NH) is a function of the duty factor, with the worst-case power dissipation occurring at the minimum input voltage:

$$P_D(NH\ \ Resistive) = \left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{I_{LOAD}}{N_{TOTAL}}\right)^2 R_{DS(ON)}$$

where N_{TOTAL} is the total number of phases. Calculating the switching losses in the NH is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PCB layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on NH:

$$P_D(NHSwitching) = \left(\frac{V_{IN} \times I_{LOAD} \times f_{SW}}{N_{TOTAL}}\right)\left(\frac{Q_{G(SW)}}{I_{GATE}}\right) + \frac{C_{OSS} \times V_{IN}^2 \times f_{SW}}{2}$$

where C_{OSS} is the output capacitance of the high-side MOSFET, $Q_{G(SW)}$ is the charge needed to turn on the NH MOSFET, and I_{GATE} is the peak gate-drive source/sink current. The optimum high-side MOSFET trades the switching losses with the conduction ($R_{DS(ON)}$) losses over the input voltage range. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to losses at $V_{IN(MAX)}$, with lower losses in between. If V_{IN} does not vary over a wide range, the minimum power dissipation occurs where the resistive losses equal the switching losses.

Low-Side MOSFET Power Dissipation

For the low-side MOSFET (NL), the worst-case power dissipation always occurs at maximum input voltage:

$$P_D(NLResistive) = \left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)\right]\left(\frac{I_{LOAD}}{N_{TOTAL}}\right)^2 R_{DS(ON)}$$

The worst case for MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD(MAX)}$ but are not quite high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, the circuit can be overdesigned to tolerate:

$$I_{LOAD} = N_{TOTAL}\left(I_{VALLEY(MAX)} + \frac{\Delta I_{INDUCTOR}}{2}\right)$$

$$= N_{TOTAL}\left(I_{VALLEY(MAX)} + \left(\frac{I_{LOAD(MAX)} \times LIR}{2}\right)\right)$$

where $I_{VALLEY(MAX)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and on-resistance variation. The MOSFET must have a good-size heatsink to handle the overload power dissipation. Choose a low-side MOSFET that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., one or two thermally enhanced 8-pin SO packages), and is reasonably priced. Make sure that the DL_ gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic gate-to-drain capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems might occur (see the *MOSFET Gate Drivers* section). The optional Schottky diode (from DL to ground) should have a low forward voltage and be able to handle the load current per phase during the dead times.

Boost Capacitor

The boost capacitors (C_{BST}) must be selected large enough to handle the gate-charging requirements of the high-side MOSFET. Select the boost capacitors to avoid discharging the capacitor more than 200mV while charging the gate of the high-side MOSFET:

$$C_{BST} = \frac{N \times Q_{GATE}}{200mV}$$

where N is the number of high-side MOSFETs used for one regulator, and Q_{GATE} is the gate charge specified in the data sheet of the MOSFET. For example, assume one FDS6298 n-channel MOSFET is used on the high side. According to the manufacturer's data sheet, a single FDS6298 has a maximum gate charge of 10nC (V_{GS} = 5V). Using the above equation, the required boost capacitance would be:

$$C_{BST} = \frac{1 \times 10nC}{200mV} = 0.05\mu F$$

Selecting the closest standard value, this example requires a 0.1µF ceramic capacitor.

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

Current Limit (IMAX)

The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T have a current limit that is programmed in discrete increments using multivalue logic inputs, IMAX_ and SR. The regulator's maximum current limit, which is the current limit per phase times the maximum number of active phases, is reflected in the ICC_MAX register (21h) for the respective regulator. The IMAX_ voltage determines the valley current-sense threshold. See Table 6.

The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half the ripple current; therefore:

$$I_{VALLEY} > I_{LOAD(MAX)}\left(1-\frac{LIR}{2}\right)$$

where:

$$I_{VALLEY} = \frac{V_{SENSE}}{R_{SENSE}}$$

where R_{SENSE} is the sensing resistor or effective inductor DCR.

To set the current limit:

1) Select the inductor (see the *Inductor Selection* section)
2) Based on the current-sensing element (sense resistor or DCR sensing), calculate CSP_ - CSN_ sensed resistance value. See the *Current Sense* section. Then, use a divider to normalize this value to one of the four R_{SENSE} values in Table 6.
3) Select ICC_MAX for the calculated R_{SENSE} value. Then, program the IMAX_ pin to its specified voltage level in Table 6.
4) SR setting also scales the current limit. Set V_{SR} to one of the four voltages in Table 7 based on using NTC or not using NTC in the current-sensing network. See the *Electrical Characteristics* table.

Slew-Rate Control

The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T have a slew-rate control programmed in discrete increments using a multivalue logic-input SR. Connect SR to a voltage level as defined in Table 7 to set the fast slew rate. The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T digitize the voltage at SR to set one of two discrete slew rates. The regulator's slow slew rate is set automatically relative to the fast slew rate (SR_Slow = 1/4 SR_Fast). The selected fast and slow slew rates are reflected in registers 24h and 25h, respectively. If NTC is used in a current-sensing network (CSP_, CSN_), set V_{SR} at 1.5V for 20mV/µs and 0V for 10mV/µs fast slew rate. Otherwise, V_{SR} = 3V sets the fast slew rate at 20mV/µs and V_{SR} = V_{CC} sets it at 10mV/µs.

Voltage Positioning

Voltage positioning dynamically lowers the output voltage in response to the load current, reducing the output capacitance and processor's power-dissipation requirements. The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T use a transconductance amplifier to set the transient and DC output-voltage droop (Figures 5, 6, and 7) as a function of the load. This adjustability allows flexibility in the selected current-sense resistor value or inductor DCR, and allows smaller current-sense resistance to be used, reducing the overall power dissipated.

Steady-State Voltage Positioning

Connect a resistor ($R_{FB_}$) between FB_ and V_{OUT} to set the DC steady-state droop (load-line) based on the required voltage-positioning slope (R_{DROOP}):

$$R_{FB_} = \frac{R_{DROOP} \times N_{PH}}{R_{SENSE}\, G_{m(FB_)}}$$

where the effective current-sense resistance (R_{SENSE}) depends on the current-sense method (see the *Current Sense* section), and the transconductance ($G_{m(FB_)}$) of the voltage-positioning amplifier is typically 600µS as defined in the *Electrical Characteristics* table. When the inductors' DCR is used as the current-sense element, each current-sense input should include an NTC thermistor to minimize the temperature dependence of the voltage-positioning slope.

Applications Information

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all the power components on the top side of the board with their ground terminals flush against one another. The layouts of the MAX17411/MAX17511/MAX17511N/MAX17511C/MAX17511T are intimately related to the layout of the CPU. The high-current output paths from the regulator must flow cleanly into the high-current inputs on the processor. For VR12/IMVP-7 processors, these inputs are orthogonal. This arrangement effectively forces the regulator to be located diagonally with respect to the processor. Refer to the MAX17411/MAX17511/

MAX17511C/MAX17511N/MAX17511T Evaluation Kits' specifications for layout examples and follow these guidelines for good PCB layout:

- Keep the high-current paths short, especially at the ground terminals. This is essential for stable, jitter-free operation.
- Connect all analog grounds to a separate solid copper plane, which connects to the ground pin of the Quick-PWM controller. This includes the V_{CC} bypass capacitor, FB_, and GNDS bypass capacitors.
- Keep the power traces and load connections short. This is essential for high efficiency. The use of thick copper PCB (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PCB traces is a difficult task that must be approached in terms of fractions of centimeters, where a single mΩ of excess trace resistance causes a measurable efficiency penalty.
- Keep the high-current, gate-driver traces (DL_, DH_, LX_, and BST_) short and wide to minimize trace resistance and inductance. This is essential for high-power MOSFETs that require low-impedance gate drivers to avoid shoot-through currents. CSP_ and CSN_ connections for current limiting and voltage positioning must be made using Kelvin-sense connections to guarantee the current-sense accuracy.
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
- Route high-speed switching nodes away from sensitive analog areas (FB_, CSP_, CSN_, etc.).

Layout Procedure

COMPONENT	DESCRIPTION
Capacitors	The general rule is that capacitors take priority over resistors since they provide a filtering function. The list below is in order of priority. **1) V_{DDA}, V_{DDB}, and V_{CC} Capacitors** Place these near the IC pins with wide traces and good connection to PGND. **2) CSP_AVE - CSN_ Differential Filter** Place the capacitor and the step resistor near the IC pins. This input is most critical because it is used for regulation and load line. **3) CSP_ - CSN_ Differential Filter Capacitors** Place these after placing the CSP_AVE - CSN_ capacitor and step resistor. This input is less critical because it is only used for current limit and current balance. **4) Common-Mode Capacitors** The capacitors to AGND take the next priority. **5) FB_ and GNDS_ Capacitors** The FB_ capacitor will be slightly further from the IC since the FB_ resistor has priority to be closer to the IC.
FB_	The FB_ resistor should be near the respective pin. Keep the trace short to reduce any inductance.
IMAX_ and SR	IMAX_ and SR resistors can be a little further from the IC. The voltages are sampled during the IC initialization time.
DCR Network	The resistor network for CSP_AVE - CSN_ or CSP_ - CSN_ must be placed near the inductors.
Current Sense	Use Kelvin sense connection to the sense element (inductor or sense resistor). Route CSP_AVE-_ as a differential pair as the first priority. Route CSP_ traces near CSN_ as a second priority. Avoid any switching signals, especially DH and LX when routing these current-sensing signals.
Thermistors	The NTC for CSP_AVE - CSN_ and CSPB1 - CSNB (MAX17511/MAX17511C/MAX17511N/MAX17511T) sensing must be placed near the Phase 1 inductor to properly sense the temperature. The NTC for THERM_ sensing should be placed near the power components of the first phase.

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

Layout Procedure (continued)

COMPONENT	DESCRIPTION
Catch Resistors	Catch resistors should be placed near the CPU so that the output voltage trace does not need to route back to the IC. But the GND catch resistor is less critical as it only requires a via to connect to the GND plane.
Remote Sense	Route together in a quiet layer, avoiding any switching signals, especially DH and LX.
Gate Drive	Keep the gate-drive traces short and wide. Use double vias especially for DL. Use 40mil to 50mil traces for DL and 30mil to 40mil traces for DH and LX. DH and LX are a pair, and should run side by side, or one above the other. DL and GND are the other pair. Route DL next to the GND layer. Keep DH and LX away from DL to avoid cross coupling. Also keep DH and LX away from any sensitive signal traces. The DL capacitor should be placed near the low-side MOSFET gate-source pins, and not near the IC DL pins.
Snubbers	Snubbers should be placed at the LX node near the MOSFET or inductor, and not near the IC LX pins.
BST	BST components should be placed near the IC, connecting to LX near the IC pin.
VRHOT#, POKA, POKB	Pullups do not need to be near the IC and can be placed further to make space for other more important components near the IC. Use 10kΩ pullup to +3.3V for POKA and POKB. Use 75Ω pullup to +1.05V for VRHOT#. Refer to Intel specifications for final pullup resistor value and voltage.
SVID	Pullups for VDIO, VCLK, and ALERT# do not need to be too close to the IC and can be placed further to make space for other more important components near the IC. Refer to Intel specifications for final pullup resistor value and voltage. Place a small 0.1µF decoupling capacitor for the +1.05V near the pullup resistors.
AGND	Keep the AGND polygon just large enough to cover AGND components. Do not make it any larger than necessary. The AGND polygon should not run under any gate-drive traces since all AGND connections should be on the other side of the IC, away from the driver pins.
AGND - PGND	AGND - PGND connection should be done away from the PGND pins so as not to be in the path of the gate-drive currents. A good location is near to the V_{CC} pin.
MAX17511/ MAX174511C/ MAX17511N/MAX17511T Exposed Pad	Although the exposed pad is both AGND and PGND, it is better to define the exposed pad in the schematics as PGND. This allows the exposed pad vias to connect to the PGND plane, providing a low-impedance path for the gate-drive currents.
Power Components	Place the power components close to keep the current loop small. Avoid large LX nodes. Use multiple vias to keep the impedance low and to carry the high currents.

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	FEATURE
MAX17511CGTL+	-40°C to +105°C	40 TQFN-EP*	3-/2-/1-Phase + 1-Phase, 0V V_{BOOT} for Reg A, 0.9V V_{BOOT} for Reg B
MAX17511NGTL+	-40°C to +105°C	40 TQFN-EP*	3-/2-/1-Phase + 1-Phase, 1.1V V_{BOOT}
MAX17511TGTL+	-40°C to +105°C	40 TQFN-EP*	3-/2-/1-Phase + 1-Phase, OVP Disabled

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
40 TQFN-EP	T4055+2	21-0140	90-0002
48 TQFN-EP	T4866+1	21-0141	90-0057

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/11	Initial release	—
1	7/11	Added the MAX17511C to the data sheet; updated the *Absolute Maximum Ratings* to include *Package Thermal Characteristics*; changed the conditions in the *Electrical Characteristics* for the *Valley Current-Limit Threshold Voltage* sections.	1, 2, 4, 5, 6, 7, 10, 12, 13, 14, 19, 20, 21, 25,27, 28, 32, 33, 35, 38, 40, 49, 52, 53, 58, 62, 64

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