THE DATASHEET OF

MAX1847EEE+T

MAX1846/MAX1847

High-Efficiency, Current-Mode, Inverting PWM Controller

General Description

MAX1846/MAX1847 high-efficiency PWM inverting controllers allow designers to implement compact, low-noise, negative-output DC-DC converters for telecom and networking applications. Both devices operate from +3V to +16.5V input and generate -500mV to -200V output. To minimize switching noise, both devices feature a current-mode, constant-frequency PWM control scheme. The operating frequency can be set from 100kHz to 500kHz through a resistor.

The MAX1846 is available in an ultra-compact 10-pin µMAX® package. Operation at high frequency, compatibility with ceramic capacitors, and inverting topology without transformers allow for a compact design. Compatibility with electrolytic capacitors and flexibility to operate down to 100kHz allow users to minimize the cost of external components. The high-current output drivers are designed to drive a P-channel MOSFET and allow the converter to deliver up to 30W.

The MAX1847 features clock synchronization and shutdown functions. The MAX1847 can also be configured to operate as an inverting flyback controller with an N-channel MOSFET and a transformer to deliver up to 70W. The MAX1847 is available in a 16-pin QSOP package.

Current-mode control simplifies compensation and provides good transient response. Accurate current-mode control and over current protection are achieved through low-side current sensing.

Applications

- Cellular Base Stations
- Networking Equipment
- Optical Networking Equipment
- SLIC Supplies
- CO DSL Line Driver Supplies
- Industrial Power Supplies
- Servers
- VOIP Supplies

***Pin Configurations* appear at end of data sheet.**

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Features

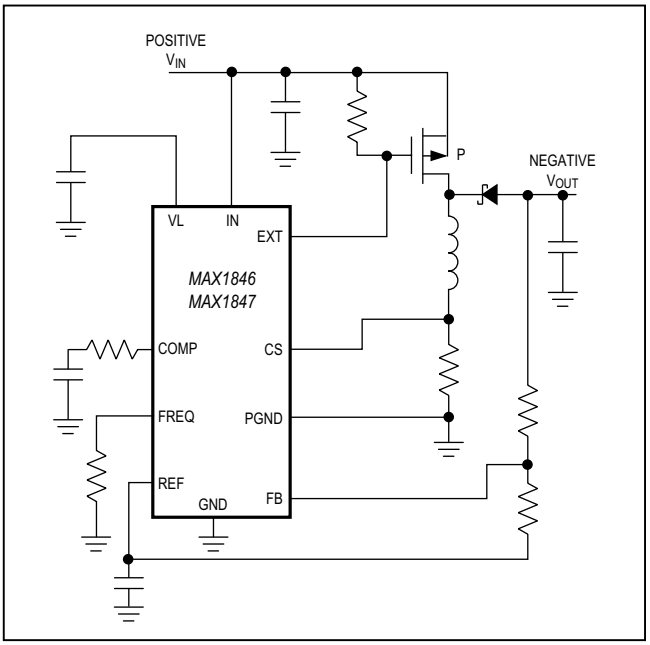
- 90% Efficiency
- +3.0V to +16.5V Input Range
- -500mV to -200V Output
- Drives High-Side P-Channel MOSFET
- 100kHz to 500kHz Switching Frequency
- Current-Mode, PWM Control
- Internal Soft-Start
- Electrolytic or Ceramic Output Capacitor
- The MAX1847 also offers:
  Synchronization to External Clock Shutdown
  N-Channel Inverting Flyback Option

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1846EUB	-40°C to +85°C	10 µMAX
MAX1846EUB+	-40°C to +105°C	10 µMAX
MAX1847EEE	-40°C to +85°C	16 QSOP
MAX1847EEE+	-40°C to +85°C	16 QSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Typical Operating Circuit



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Absolute Maximum Ratings

IN, $\overline{SHDN}$ to GND .....-0.3V to +20V
PGND to GND .....-0.3V to +0.3V
VL to PGND for VIN ≤ 5.7V.....-0.3V to (V_{IN} + 0.3V)
VL to PGND for VIN > 5.7V.....-0.3V to +6V
EXT to PGND .....-0.3V to (V_{IN} + 0.3V)
REF, COMP to GND.....-0.3V to (VL + 0.3V)
CS, FB, FREQ, POL, SYNC to GND .....-0.3V to +6V

Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 5.6mW/°C above +70°C).....444mW
16-Pin QSOP (derate 8.3mW/°C above +70°C).....696mW
Operating Temperature Range..... -40°C to +105°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow)
Lead(Pb)-free.....+260°C
Containing lead(Pb).....+240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

($V_{\overline{SHDN}}$ = V_{IN} = +12V, SYNC = GND, PGND = GND, R_{FREQ} = 147kΩ ±1%, C_{VL} = 0.47µF, C_{REF} = 0.1µF, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER						
Operating Input Voltage Range			3.0		16.5	V
UVLO Threshold	V_{IN} rising	-40°C to ~+85°C		2.8	2.95	V
		-40°C to ~+105°C		2.8	2.96	
	V_{IN} falling	-40°C to ~+85°C	2.6	2.74		
		-40°C to ~+105°C	2.59	2.74		
UVLO Hysteresis				60		mV
FB Threshold	No load		-12	0	12	mV
FB Input Current	V_{FB} = -0.1V		-50	-6	50	nA
Load Regulation	C_{COMP} = 0.068µF, V_{OUT} = -48V, I_{OUT} = 20mA to 200mA (Note 1)		-1		0	%
Line Regulation	C_{COMP} = 0.068µF, V_{OUT} = -48V, V_{IN} = +8V to +16.5V, I_{OUT} = 100mA			0.04		%
Current-Limit Threshold			85	100	115	mV
CS Input Current	CS = GND			10	20	µA
Supply Current	V_{FB} = -0.1V, V_{IN} = +3.0V to +16.5V			0.75	1.2	mA
Shutdown Supply Current	SHDN = GND, V_{IN} = +3.0V to +16.5V V_{IN} = +3.0V to +16.5V			10	25	µA
REFERENCE AND VL REGULATOR						
REF Output Voltage	I_{REF} = 50µA		1.236	1.25	1.264	V
REF Load Regulation	I_{REF} = 0 to 500µA			-2	-15	mV
VL Output Voltage	I_{VL} = 100µA		3.85	4.25	4.65	V
VL Load Regulation	I_{VL} = 0.1mA to 2.0mA			-20	-60	mV

Electrical Characteristics (continued)

($V_{\overline{SHDN}}$ = V_{IN} = +12V, SYNC = GND, PGND = GND, R_{FREQ} = 147kΩ ±1%, C_{VL} = 0.47µF, C_{REF} = 0.1µF, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR					
Oscillator Frequency	R_{FREQ} = 500kΩ ±1%	88	100	112	kHz
	R_{FREQ} = 147kΩ ±1%	255	300	345	
	R_{FREQ} = 76.8kΩ ±1%		500		
Maximum Duty Cycle	R_{FREQ} = 500kΩ ±1%	93	96	98	%
	R_{FREQ} = 147kΩ ±1%	85	88	92	
	R_{FREQ} = 76.8kΩ ±1%		80		
SYNC Input Signal Duty-Cycle Range		7		93	%
Minimum SYNC Input Logic-Low Pulse Width			50	200	ns
SYNC Input Rise/Fall Time	(Note 2)			200	ns
SYNC Input Frequency Range		100		550	kHz
DIGITAL INPUTS					
POL, SYNC, $\overline{SHDN}$ Input High Voltage		2.0			V
POL, SYNC, $\overline{SHDN}$ Input Low Voltage				0.45	V
POL, SYNC Input Current	POL, SYNC = GND or VL		20	40	µA
$\overline{SHDN}$ Input Current	$V_{\overline{SHDN}}$ = +5V or GND	-12	-4	0	µA
	$V_{\overline{SHDN}}$ = +16.5V		1.5	6	
SOFT-START					
Soft-Start Clock Cycles			1024		
Soft-Start Levels			64		
EXT OUTPUT					
EXT Sink/Source Current	V_{IN} = +5V, V_{EXT} forced to +2.5V		1		A
EXT On-Resistance	EXT high or low, tested with 100mA load, V_{IN} = +5V		3	7.5	Ω
	EXT high or low, tested with 100mA load, V_{IN} = +3V		5	12	

Note 1: Production test correlates to operating conditions.
Note 2: Guaranteed by design and characterization.

Electrical Characteristics

($V_{\overline{SHDN}}$ = V_{IN} = +12V, SYNC = GND, PGND = GND, R_{FREQ} = 147kΩ ±1%, C_{VL} = 0.47µF, C_{REF} = 0.1µF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS		MIN	MAX	UNITS
PWM CONTROLLER					
Operating Input Voltage Range			3.0	16.5	V
UVLO Threshold	V_{IN} rising			2.95	V
	V_{IN} falling		2.6		
FB Threshold	No load		-20	+20	mV
FB Input Current	V_{FB} = -0.1V	-40°C to ~+85°C	-50	+50	nA
		-40°C to ~+105°C	-150	+150	
Load Regulation	C_{COMP} = 0.068µF, V_{OUT} = -48V, I_{OUT}= 20mA to 200mA (Note 1)		-2	0	%
Current Limit Threshold			85	115	mV
CS Input Current	CS = GND			20	µA
Supply Current	V_{FB} = -0.1V, V_{IN} = +3.0V to +16.5V			1.2	mA
Shutdown Supply Current	$\overline{SHDN}$ = GND, V_{IN} = +3.0V to +16.5V			25	µA
REFERENCE AND VL REGULATOR					
REF Output Voltage	I_{REF} = 50µA		1.225	1.275	V
REF Load Regulation	I_{REF} = 0 to 500µA			-15	mV
VL Output Voltage	I_{VL} = 100µA		3.85	4.65	V
VL Load Regulation	I_{VL} = 0.1mA to 2.0mA			-60	mV
OSCILLATOR					
Oscillator Frequency	R_{FREQ} = 500kΩ ±1%		84	116	kHz
	R_{FREQ} = 147kΩ ±1%		255	345	
Maximum Duty Cycle	R_{FREQ} = 500kΩ ±1%		93	98	%
	R_{FREQ} = 147kΩ ±1%		84	93	
SYNC Input Signal Duty-Cycle Range			7	93	%
Minimum SYNC Input Logic Low Pulse Width				200	ns
SYNC Input Rise/Fall Time	(Note 2)			200	ns
SYNC Input Frequency Range			100	550	kHz
DIGITAL INPUTS					
POL, SYNC, $\overline{SHDN}$ Input High Voltage			2.0		V
POL, SYNC, $\overline{SHDN}$ Input Low Voltage				0.45	V

Electrical Characteristics (continued)

($V_{\overline{SHDN}}$ = V_{IN} = +12V, SYNC = GND, PGND = GND, R_{FREQ} = 147kΩ ±1%, C_{VL} = 0.47µF, C_{REF} = 0.1µF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

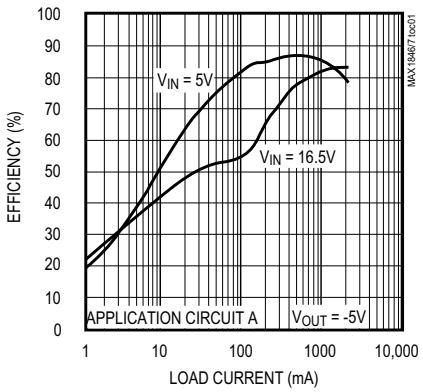
PARAMETER	CONDITIONS		MIN	MAX	UNITS
POL, SYNC Input Current	POL, SYNC = GND or VL			40	µA
$\overline{SHDN}$ Input Current	$V_{\overline{SHDN}}$ = +5V or GND		-12	0	µA
	$V_{\overline{SHDN}}$ = +16.5V			6	
EXT OUTPUT					
EXT On-Resistance	EXT high or low, I_{EXT} = 100mA, V_{IN} = +5V	-40°C to ~+85°C		7.5	Ω
		-40°C to ~+105°C		8.75	
	EXT high or low, I_{EXT} = 100mA, V_{IN} = +3V			12	

Note 3: Parameters to -40°C are guaranteed by design and characterization.

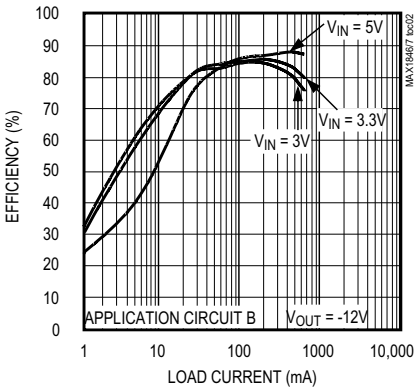
Typical Operating Characteristics

(Circuit references are from Table 1 in the *Main Application Circuits* section, C_{VL} = 0.47µF, C_{REF} = 0.1°F, T_A = +25°C, unless otherwise noted.)

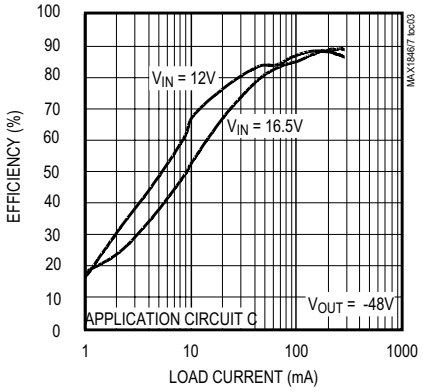
EFFICIENCY vs. LOAD CURRENT



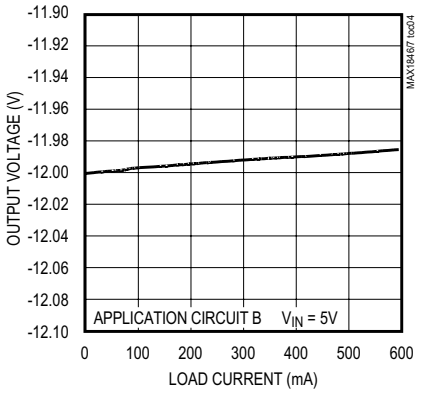
EFFICIENCY vs. LOAD CURRENT



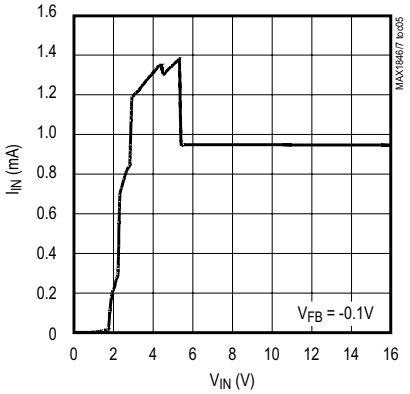
EFFICIENCY vs. LOAD CURRENT



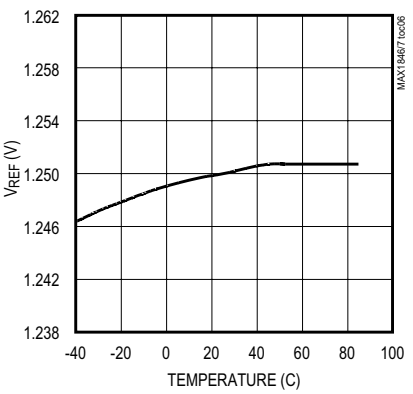
OUTPUT VOLTAGE LOAD REGULATION



SUPPLY CURRENT vs. SUPPLY VOLTAGE



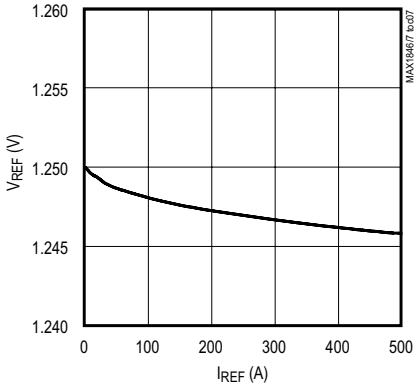
REFERENCE VOLTAGE vs. TEMPERATURE



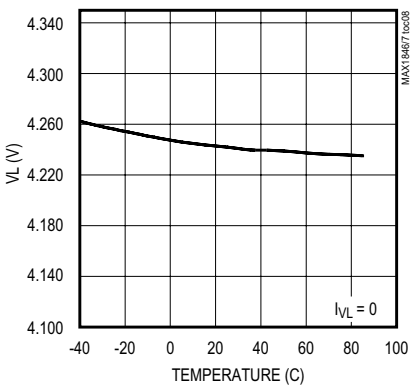
Typical Operating Characteristics (continued)

(Circuit references are from Table 1 in the *Main Application Circuits* section, C_{VL} = 0.47µF, C_{REF} = 0.1°F, T_A = +25°C, unless otherwise noted.)

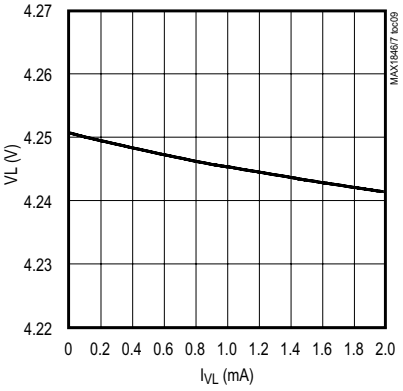
REFERENCE LOAD REGULATION



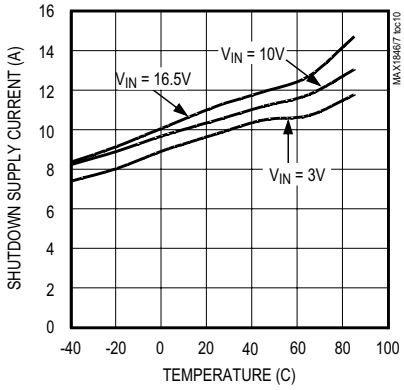
VL VOLTAGE vs. TEMPERATURE



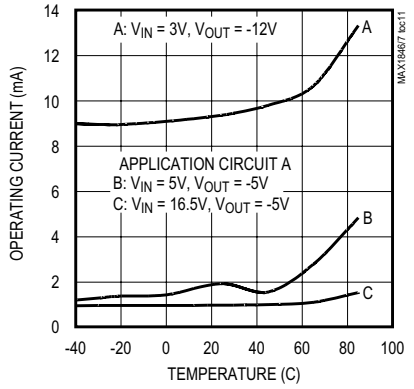
VL LOAD REGULATION



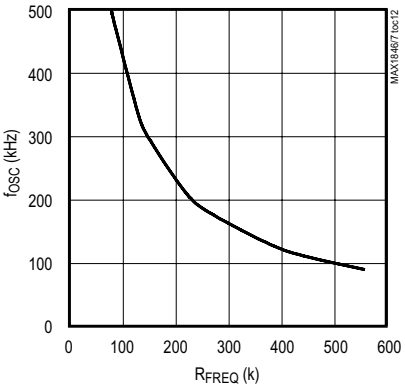
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



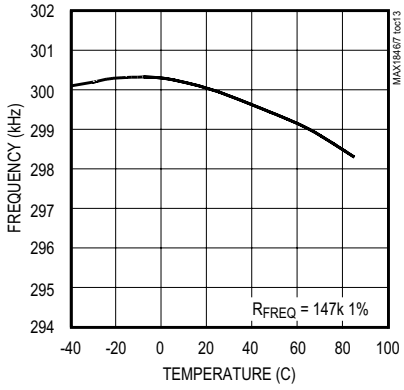
OPERATING CURRENT vs. TEMPERATURE



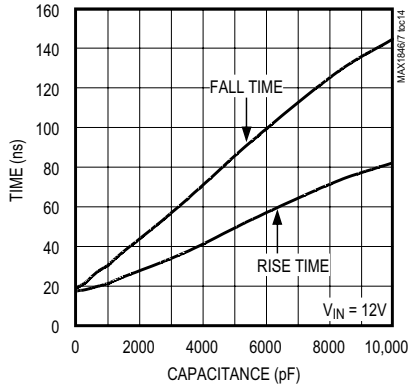
SWITCHING FREQUENCY vs. RFREQ



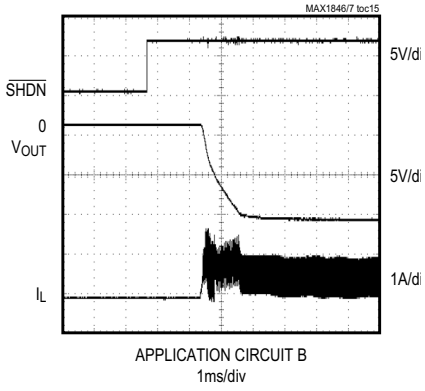
SWITCHING FREQUENCY vs. TEMPERATURE



EXT RISE/FALL TIME vs. CAPACITANCE



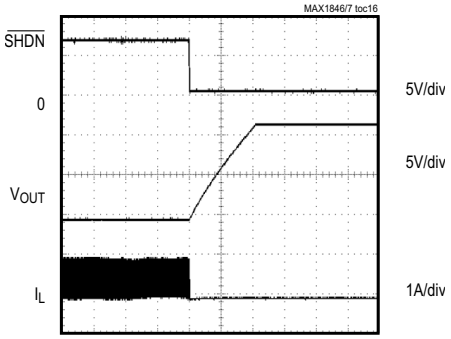
EXITING SHUTDOWN



Typical Operating Characteristics (continued)

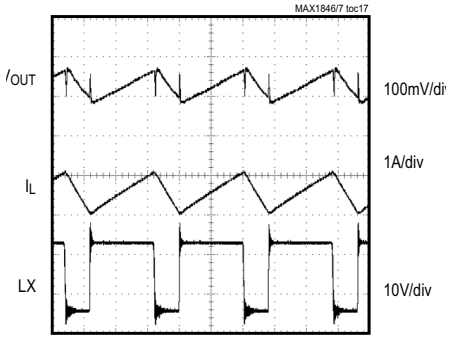
(Circuit references are from Table 1 in the *Main Application Circuits* section, C_{VL} = 0.47µF, C_{REF} = 0.1°F, T_A = +25°C, unless otherwise noted.)

ENTERING SHUTDOWN



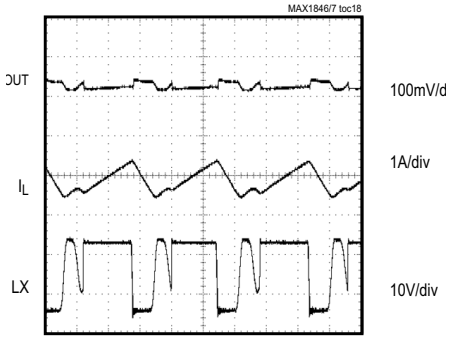
APPLICATION CIRCUIT B
1ms/div

HEAVY-LOAD SWITCHING WAVEFORM



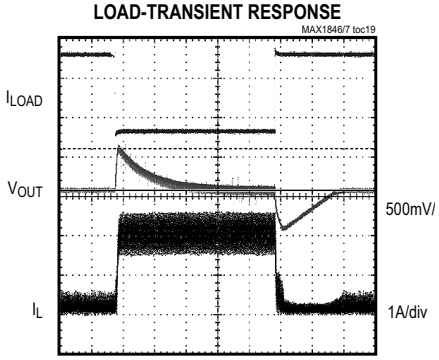
APPLICATION CIRCUIT B
1s/div
I_{LOAD} = 600mA

LIGHT-LOAD SWITCHING WAVEFORM



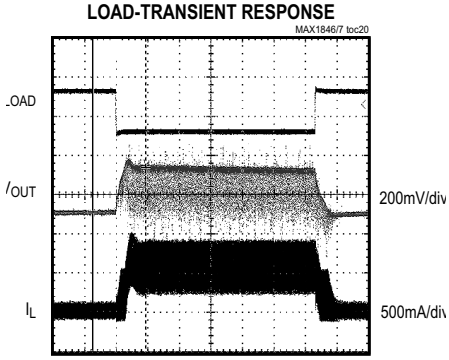
APPLICATION CIRCUIT B
1s/div
I_{LOAD} = 50mA

LOAD-TRANSIENT RESPONSE



APPLICATION CIRCUIT B
2ms/div
I_{LOAD} = 10mA to 400mA

LOAD-TRANSIENT RESPONSE

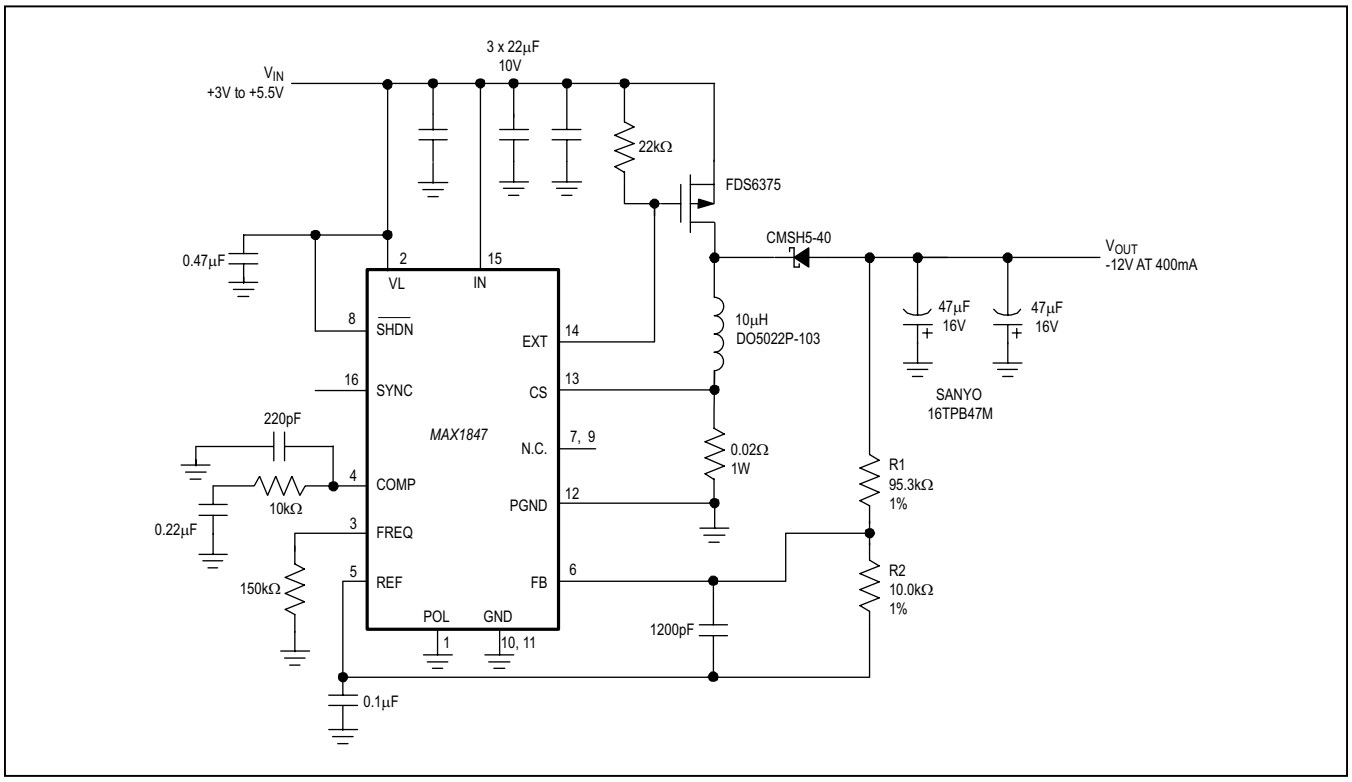


APPLICATION CIRCUIT C
400s/div
I_{LOAD} = 4mA to 100mA

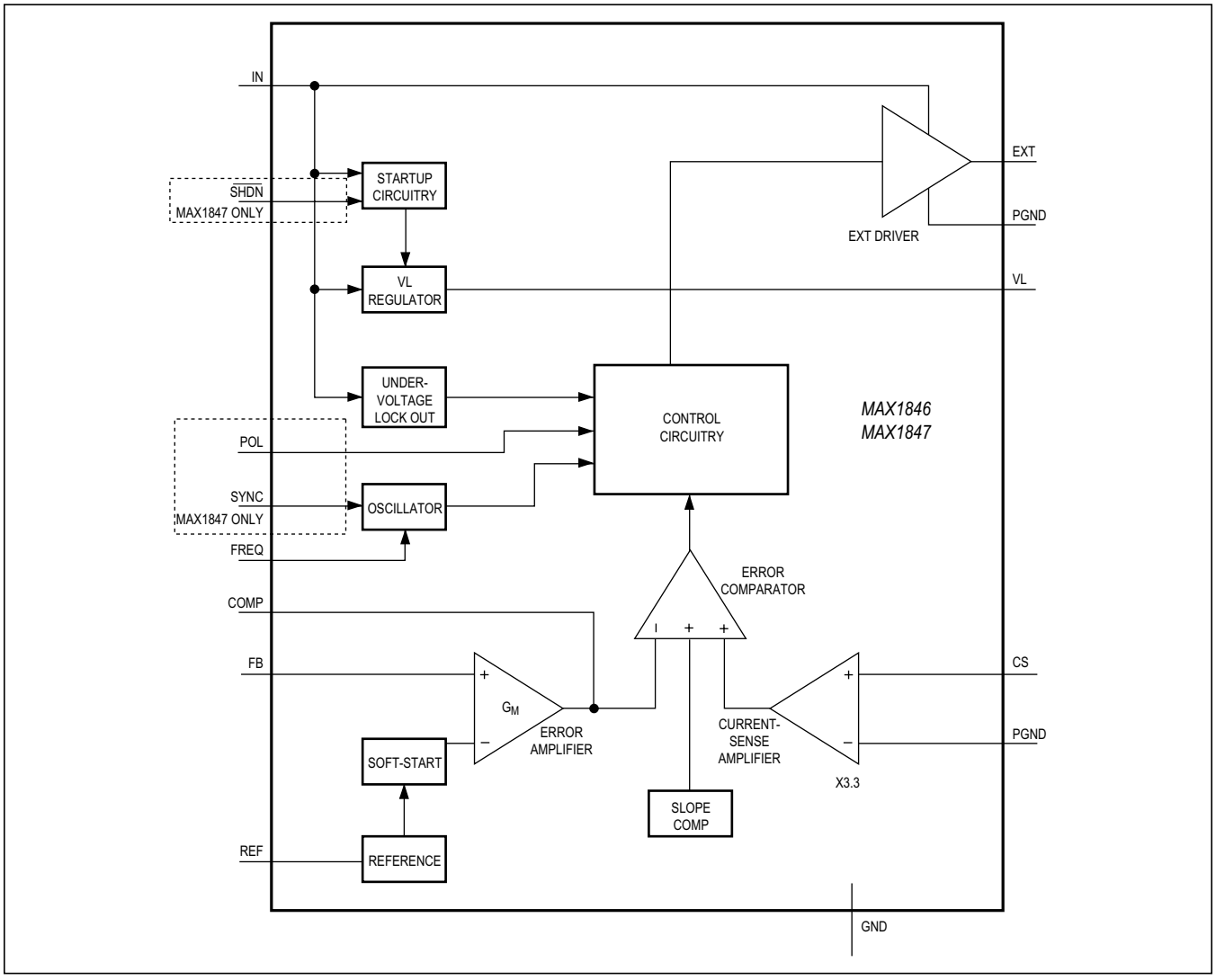
Pin Description

PIN		NAME	FUNCTION
MAX1846	MAX1847		
—	1	POL	Sets polarity of the EXT pin. Connect POL to GND to set EXT for use with an external PMOS high-side FET. Connect POL to VL to set EXT for use with an external NMOS low-side FET in transformer-based applications.
1	2	VL	VL Low-Dropout Regulator. Connect 0.47µF ceramic capacitor from VL to GND.
2	3	FREQ	Oscillator Frequency Set Input. Connect a resistor (R_{FREQ}) from FREQ to GND to set the internal oscillator frequency from 100kHz (R_{FREQ} = 500kΩ) to 500kHz (R_{FREQ} = 76.8kΩ). R_{FREQ} is still required if an external clock is used at SYNC. See *Setting the Operating Frequency* section.
3	4	COMP	Compensation Node for Error Amp/Integrator. Connect a series resistor/capacitor network from COMP to GND for loop compensation. See *Design Procedure*.
4	5	REF	1.25V Reference Output. REF can source up to 500µA. Bypass with a 0.1µF ceramic capacitor from REF to GND.
5	6	FB	Feedback Input. Connect FB to the center of a resistor-divider connected between the output and REF. The FB threshold is 0.
—	7, 9	N.C.	No Connection
—	8	$\overline{SHDN}$	Shutdown Control. Drive $\overline{SHDN}$ low to turn off the DC-DC controller. Drive high or connect to IN for normal operation.
6	10, 11	GND	Analog Ground. Connect to PGND.
7	12	PGND	Negative Rail for EXT Driver and Negative Current-Sense Input. Connect to GND.
8	13	CS	Positive Current-Sense Input. Connect a current-sense resistor (R_{CS}) between CS and PGND.
9	14	EXT	External MOSFET Gate-Driver Output. EXT swings from IN to PGND.
10	15	IN	Power-Supply Input
—	16	SYNC	Operating Frequency Synchronization Control. Drive SYNC low or connect to GND to set the internal oscillator frequency with R_{FREQ}. Drive SYNC with a logic-level clock input signal to externally set the converter's operating frequency. DC-DC conversion cycles initiate on the rising edge of the input clock signal. Note that when driving SYNC with an external signal, R_{FREQ} must still be connected to FREQ.

Typical Application Circuit



Functional Diagram



Detailed Description

The MAX1846/MAX1847 current-mode PWM controllers use an inverting topology that is ideal for generating output voltages from -500mV to -200V. Features include shutdown, adjustable internal operating frequency or synchronization to an external clock, soft-start, adjustable current limit, and a wide (+3V to +16.5V) input range.

PWM Controller

The architecture of the MAX1846/MAX1847 current-mode PWM controller is a BiCMOS multi-input system that simultaneously processes the output-error signal, the current-sense signal, and a slope-compensation ramp (*Functional Diagram*). Slope compensation prevents sub-harmonic oscillation, a potential result in current-mode regulators operating at greater than 50% duty cycle. The controller uses fixed-frequency, current-mode operation where the duty ratio is set by the input-to-output voltage ratio. The current-mode feedback loop regulates peak inductor current as a function of the output error signal.

Internal Regulator

The MAX1846/MAX1847 incorporate an internal low-dropout regulator (LDO). This LDO has a 4.25V output and powers all MAX1846/MAX1847 functions (excluding EXT) for the primary purpose of stabilizing the performance of the IC over a wide input voltage range (+3V to +16.5V). The input to this regulator is connected to IN, and the dropout voltage is typically 100mV, so that when V_{IN} is less than 4.35V, VL is typically V_{IN} minus 100mV. When the LDO is in dropout, the MAX1846/MAX1847 still operate with V_{IN} as low as 3V. For best performance, it is recommended to connect VL to IN when the input supply is less than 4.5V.

Undervoltage Lockout

The MAX1846/MAX1847 have an undervoltage lockout circuit that monitors the voltage at VL. If VL falls below the UVLO threshold (2.8V typ), the control logic turns the P-channel FET off (EXT high impedance). The rest of the IC circuitry is still powered and operating. When VL increases to 60mV above the UVLO threshold, the IC resumes operation from a start up condition (soft-start).

Soft-Start

The MAX1846/MAX1847 feature a “digital” soft-start that is preset and requires no external capacitor. Upon startup, the FB threshold decrements from the reference voltage to 0 in 64 steps over 1024 cycles of f_{OSC} or f_{SYNC}. See the Typical Operating Characteristics for a scope picture of the soft-start operation. Soft-start is implemented: 1) when power is first applied to the IC, 2) when exiting shutdown with power already applied, and 3) when exiting undervoltage lockout.

Shutdown (MAX1847 only)

The MAX1847 shuts down to reduce the supply current to 10µA when $\overline{SHDN}$ is low. In this mode, the internal reference, error amplifier, comparators, and biasing circuitry turn off. The EXT output becomes high impedance and the external pullup resistor connected to EXT pulls V_{EXT} to V_{IN}, turning off the P-channel MOSFET. When in shutdown mode, the converter's output goes to 0.

Frequency Synchronization (MAX1847 only)

The MAX1847 is capable of synchronizing its switching frequency with an external clock source. Drive SYNC with a logic-level clock input signal to synchronize the MAX1847. A switching cycle starts on the rising edge of the signal applied to SYNC. Note that the frequency of the signal applied to SYNC must be higher than the default frequency set by R_{FREQ}. This frequency is required so that the internal clock does not start a switching cycle prematurely. If SYNC is inactive for an entire clock cycle of the internal oscillator, the internal oscillator takes over the switching operation. Choose R_{FREQ} such that f_{OSC} = 0.9 5 f_{SYNC}.

EXT Polarity (MAX1847 only)

The MAX1847 features an option to utilize an N-channel MOSFET configuration, rather than the typical p-channel MOSFET configuration (Figure 1). In order to drive the different polarities of these MOSFETs, the MAX1847 is capable of reversing the phase of EXT by 180 degrees. When driving a P-channel MOSFET, connect POL to GND. When driving an n-channel MOSFET, connect POL to VL. These POL connections ensure the proper polarity for EXT. For design guidance in regard to this application, refer to the MAX1856 data sheet.

Design Procedure

Initial Specifications

In order to start the design procedure, a few parameters must be identified: the minimum input voltage expected ($V_{IN(MIN)}$), the maximum input voltage expected ($V_{IN(MAX)}$), the desired output voltage (V_{OUT}), and the expected maximum load current (I_{LOAD}).

Calculate the Equivalent Load Resistance

This is a simple calculation used to shorten the verification equations:

$$R_{LOAD} = V_{OUT} / I_{LOAD}$$

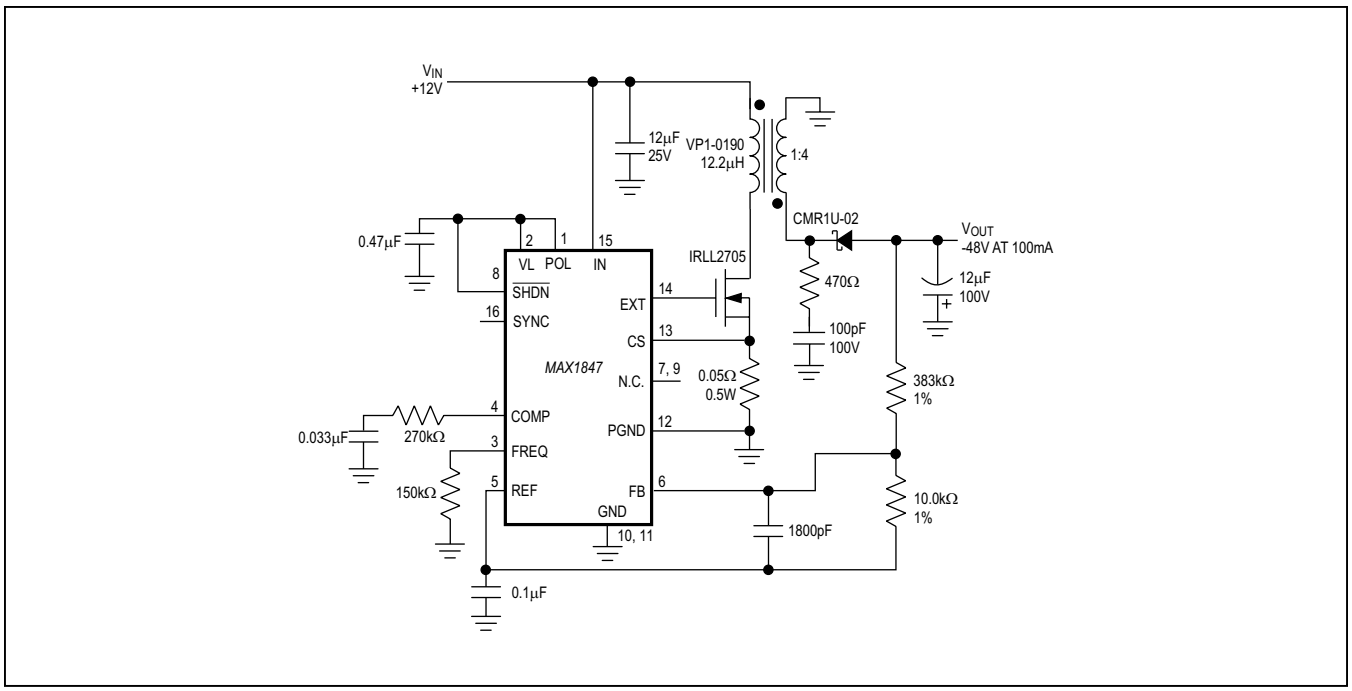


Figure 1. Using an N-Channel MOSFET (MAX1847 only)

Calculate the Duty Cycle

The duty cycle is the ratio of the on-time of the MOSFET switch to the oscillator period. It is determined by the ratio of the input voltage to the output voltage. Since the input voltage typically has a range of operation, a minimum (D_{MIN}) and maximum (D_{MAX}) duty cycle is calculated by:

$$MIN = \frac{-V_{OUT} + V_D}{V_{IN(MAX)} - V_{SW} - V_{LIM} - V_{OUT} + V_D}$$

$$MAX = \frac{-V_{OUT} + V_D}{V_{IN(MIN)} - V_{SW} - V_{LIM} - V_{OUT} + V_D}$$

where V_D is the forward drop across the output diode, V_{SW} is the drop across the external FET when on, and V_{LIM} is the current-limit threshold. To begin with, assume V_D = 0.5V for a Schottky diode, V_{SW} = 100mV, and V_{LIM} = 100mV. Remember that V_{OUT} is negative when using this formula.

Setting the Output Voltage

The output voltage is set using two external resistors to form a resistive-divider to FB between the output and REF (refer to R1 and R2 in Figure 1). V_{REF} is nominally 1.25V and the regulation voltage for FB is nominally 0. The load presented to the reference by the feedback resistors must be less than 500µA to guarantee that V_{REF} is in regulation (see *Electrical Characteristics Table*). Conversely, the current through the feedback resistors must be large enough so that the leakage current of the FB input (50nA) is insignificant. Therefore, select R2 so that I_{R2} is between 50µA and 250µA.

$$I_{R2} = V_{REF} / R2$$

where V_{REF} = 1.25V. A typical value for R2 is 10kΩ.

Once R2 is selected, calculate R1 with the following equation:

$$R1 = R2 \times (-V_{OUT} / V_{REF})$$

Setting the Operating Frequency

The MAX1846/MAX1847 are capable of operating at switching frequencies from 100kHz to 500kHz. Choice of operating frequency depends on a number of factors:

1) Noise considerations may dictate setting (or synchronizing) f_{OSC} above or below a certain frequency or band of frequencies, particularly in RF applications.

2) Higher frequencies allow the use of smaller value (hence smaller size) inductors and capacitors.
3) Higher frequencies consume more operating power both to operate the IC and to charge and discharge the gate at the external FET, which tends to reduce the efficiency at light loads.
4) Higher frequencies may exhibit lower overall efficiency due to more transition losses in the FET; however, this shortcoming can often be nullified by trading some of the inductor and capacitor size benefits for lower-resistance components.
5) High-duty-cycle applications may require lower frequencies to accommodate the controller minimum off-time of 0.4µs. Calculate the maximum oscillator frequency with the following formula:

$$f_{OSC(MAX)} = \frac{V_{IN(MIN)} - V_{SW} - V_{LIM}}{V_{IN(MIN)} - V_{SW} - V_{LIM} - V_{OUT} + V_D} \times \frac{1}{t_{OFF(MIN)}}$$

Remember that V_{OUT} is negative when using this formula. When running at the maximum oscillator frequency ($f_{OSCILLATOR}$) and maximum duty cycle (D_{MAX}), do not exceed the minimum value of D_{MAX} stated in the *Electrical Characteristics* table. For designs that exceed the D_{MAX} and $f_{OSC(MAX)}$, an autotransformer can reduce the duty cycle and allow higher operating frequencies.

The oscillator frequency is set by a resistor, RFREQ, which is connected from FREQ to GND. The relationship between fOSC (in Hz) and RFREQ (in Ω) is slightly nonlinear, as illustrated in the Typical Operating Characteristics. Choose the resistor value from the graph and check the oscillator frequency using the following formula:

$$f_{OSC} = \frac{1}{\left[\left(5.21\times10^{-7}\right) + \left(1.92\times10^{-11}\right)\times R_{FREQ} - \left(4.86\times10^{-19}\right)\times\left(R_{FREQ}\right)^2\right]}$$

External Synchronization (MAX1847 only)

The SYNC input provides external-clock synchronization (if desired). When SYNC is driven with an external clock, the frequency of the clock directly sets the MAX1847's switching frequency. A rising clock edge on SYNC is interpreted as a synchronization input. If the sync signal is lost, the internal oscillator takes over at the end of the last cycle, and the frequency is returned to the rate set by R_{FREQ}. Choose R_{FREQ} such that $f_{OSC} = 0.9 \times f_{SYNC}$.

Choosing Inductance Value

The inductance value determines the operation of the current-mode regulator. Except for low-current applications, most circuits are more efficient and economical operating in continuous mode, which refers to continuous current in the inductor. In continuous mode there is a trade-off between efficiency and transient response. Higher inductance means lower inductor ripple current, lower peak current, lower switching losses, and, therefore, higher efficiency. Lower inductance means higher inductor ripple current and faster transient response. A reasonable compromise is to choose the ratio of inductor ripple current to average continuous current at minimum duty cycle to be 0.4. Calculate the inductor ripple with the following formula:

$$I_{RIPPLE} = \frac{0.4 \times I_{LOAD(MAX)} \times \left(V_{IN(MAX)} - V_{SW} - V_{LIM} - V_{OUT} + V_D\right)}{\left(V_{IN(MAX)} - V_{SW} - V_{LIM}\right)}$$

Then calculate an inductance value:

$$L = (V_{IN(MAX)} / I_{RIPPLE}) \times (D_{MIN} / f_{OSC})$$

Choose the closest standard value. Once again, remember that V_{OUT} is negative when using this formula.

Determining Peak Inductor Current

The peak inductor current required for a particular output is:

$$I_{LPEAK} = I_{LDC} + (I_{LPP} / 2)$$

where I_{LDC} is the average DC inductor current and I_{LPP} is the inductor peak-to-peak ripple current. The I_{LDC} and I_{LPP} terms are determined as follows:

$$I_{LDC} = \frac{I_{LOAD}}{\left(1 - D_{MAX}\right)}$$

$$I_{LPP} = \frac{\left(V_{IN(MIN)} - V_{SW} - V_{LIM}\right) \times D_{MAX}}{L \times f_{OSC}}$$

where L is the selected inductance value. The saturation rating of the selected inductor should meet or exceed the calculated value for I_{LPEAK}, although most coil types can be operated up to 20% over their saturation rating without difficulty. In addition to the saturation criteria, the inductor should have as low a series resistance as possible. For continuous inductor current,

the power loss in the inductor resistance (PLR) is approximated by:

$$P_{LR} \sim R_L x \left(\frac{I_{LOAD}}{I - D_{MAX}} \right)^2$$

where R_L is the inductor series resistance.

Once the peak inductor current is calculated, the current sense resistor, R_{CS}, is determined by:

$$R_{CS} = 85mV / I_{LPEAK}$$

For high peak inductor currents (>1A), Kelvin-sensing connections should be used to connect CS and PGND to RCS. Connect PGND and GND together at the ground side of R_{CS}. A lowpass filter between R_{CS} and CS may be required to prevent switching noise from tripping the current-sense comparator at heavy loads. Connect a 100Ω resistor between CS and the high side of R_{CS}, and connect a 1000pF capacitor between CS and GND.

Checking Slope-Compensation Stability

In a current-mode regulator, the cycle-by-cycle stability is dependent on slope compensation to prevent subharmonic oscillation at duty cycles greater than 50%. For the MAX1846/MAX1847, the internal slope compensation is optimized for a minimum inductor value (L_{MIN}) with respect to duty cycle. For duty cycles greater then 50%, check stability by calculating LMIN using the following equation:

$$L_{MIN} = \left[\left(V_{IN(MIN)} x R_{CS} \right) / M_S \right] x \left[\left(2 x D_{MAX} - 1 \right) / \left(1 - D_{MAX} \right) \right]$$

where $V_{IN(MIN)}$ is the minimum expected input voltage, M_S is the Slope Compensation Ramp (41 mV/µs) and D_{MAX} is the maximum expected duty cycle. If L_{MIN} is larger than L, increase the value of L to the next standard value that is larger than L_{MIN} to ensure slope compensation stability.

Choosing the Inductor Core

Choosing the most cost-effective inductor usually requires optimizing the field and flux with size. With higher output voltages the inductor may require many turns, and this can drive the cost up. Choosing an inductor value at L_{MIN} can provide a good solution if discontinuous inductor current can be tolerated. Powdered iron cores can provide the most economical solution but are larger in size than ferrite.

Power MOSFET Selection

The MAX1846/MAX1847 drive a wide variety of P-channel power MOSFETs (PFETs). The best performance, especially with input voltages below 5V, is achieved with low-threshold PFETs that specify on-resistance with a gate-to-source voltage (V_{GS}) of 2.7V or less. When selecting a PFET, key parameters include:

- Total gate charge (Q_G)
- Reverse transfer capacitance (C_{RSS})
- On-resistance ($_{RDS(ON)}$)
- Maximum drain-to-source voltage ($V_{DS(MAX)}$)
- Minimum threshold voltage ($V_{TH(MIN)}$)

At high-switching rates, dynamic characteristics (parameters 1 and 2 above) that predict switching losses may have more impact on efficiency than $R_{DS(ON)}$, which predicts DC losses. Q_G includes all capacitance associated with charging the gate. In addition, this parameter helps predict the current needed to drive the gate at the selected operating frequency. The power MOSFET in an inverting converter must have a high enough voltage rating to handle the input voltage plus the magnitude of the output voltage and any spikes induced by leakage inductance and ringing.

An RC snubber circuit across the drain to ground might be required to reduce the peak ringing and noise.

Choose $R_{DS(ON)(MAX)}$ specified at $V_{GS} < V_{IN(MIN)}$ to be one to two times R_{CS}. Verify that $V_{IN(MAX)} < V_{GS(MAX)}$ and $V_{DS(MAX)} > V_{IN(MAX)} - V_{OUT} + V_D$. Choose the rise-and-fall times (t_R, t_F) to be less than 50ns.

Output Capacitor Selection

The output capacitor (C_{OUT}) does all the filtering in an inverting converter. The output ripple is created by the variations in the charge stored in the output capacitor with each pulse and the voltage drop across the capacitor's equivalent series resistance (ESR) caused by the current into and out of the capacitor. There are two properties of the output capacitor that affect ripple voltage: the capacitance value, and the capacitor's ESR. The output ripple due to the output capacitor's value is given by:

$$V_{RIPPLE-C} = (I_{LOAD} \times D_{MAX} \times T_{OSC}) / C_{OUT}$$

The output ripple due to the output capacitor's ESR is given by:

$$V_{RIPPLE-R} = I_{LPP} \times R_{ESR}$$

These two ripple voltages are additive and the total output ripple is:

$$V_{RIPPLE-T} = V_{RIPPLE-C} + V_{RIPPLE-R}$$

The ESR-induced ripple usually dominates this last equation, so typically output capacitor selection is based mostly upon the capacitor's ESR, voltage rating, and ripple current rating. Use the following formula to determine the maximum ESR for a desired output ripple voltage ($V_{RIPPLE-D}$):

$$R_{ESR} = V_{RIPPLE-D} / I_{LPP}$$

Select a capacitor with ESR rating less than R_{ESR}. The value of this capacitor is highly dependent on dielectric type, package size, and voltage rating. In general, when choosing a capacitor, it is recommended to use low-ESR capacitor types such as ceramic, organic, or tantalum capacitors. Ensure that the selected capacitor has sufficient margin to safely handle the maximum RMS ripple current.

For continuous inductor current the maximum RMS ripple current in the output filter capacitor is:

$$I_{RMS} = \frac{I_{LOAD}}{1 - D_{MAX}} \times \sqrt{D_{MAX} - D_{MAX}^2}$$

Choosing Compensation Components

The MAX1846/MAX1847 are externally loop-compensated devices. This feature provides flexibility in designs to accommodate a variety of applications. Proper compensation of the control loop is important to prevent excessive output ripple and poor efficiency caused by instability. The goal of compensation is to cancel unwanted poles and zeros in the DC-DC converter's transfer function created by the power-switching and filter elements. More precisely, the objective of compensation is to ensure stability by ensuring that the DC-DC converter's phase shift is less than 180° by a safe margin, at the frequency where the loop gain falls below unity. One method for ensuring adequate phase margin is to introduce corresponding zeros and poles in the feedback network to approximate a single-pole response with a -20dB/decade slope all the way to unity-gain crossover.

Calculating Poles and Zeros

The MAX1846/MAX1847 current-mode architecture takes the double pole caused by the inductor and output capacitor and shifts one of these poles to a much higher frequency to make loop compensation easier. To compensate these devices, we must know the center frequencies of the right-half plane zero (z_{RHP}) and the higher frequency pole (p_{OUT2}). Calculate the z_{RHP} frequency with the following formula:

$$Z_{RHP} = \frac{-\left[(1 - D_{MAX})^2 \times \left(V_{IN(MIN)} - V_{OUT}\right) \times R_{LOAD}\right]}{(2\pi \times V_{OUT} \times L)}$$

The calculations for p_{OUT2} are very complex. For most applications where V_{OUT} does not exceed -48V (in a negative sense), the p_{OUT2} will not be lower than 1/8th of the oscillator frequency and is generally at a higher frequency than z_{RHP}. Therefore:

$$p_{OUT2} \geq 0.125 \times f_{OSC}$$

A pole is created by the output capacitor and the load resistance. This pole must also be compensated and its center frequency is given by the formula:

$$p_{OUT1} = 1 / (2\pi \times R_{LOAD} \times C_{OUT})$$

Finally, there is a zero introduced by the ESR of the output capacitor. This zero is determined from the following equation:

$$zESR = 1 / (2\pi \times C_{OUT} \times R_{ESR})$$

Calculating the Required Pole Frequency

To ensure stability of the MAX1846/MAX1847, the gain of the error amplifier must roll-off the total loop gain to 1 before Z_{RHP} or P_{OUT2} occurs. First, calculate the DC open-loop gain A_{DC}:

$$A_{DC} = \frac{B \times G_M \times R_O \times (1 - D_{MAX}) R_{LOAD}}{A_{CS} \times R_{CS}}$$

where:

A_{CS} is the current-sense amplifier gain = 3.3

B is the feedback-divider attenuation factor =

$$\frac{R2}{R1 + R2}$$

G_M is the error-amplifier transconductance = 400 µA/V

R_O is the error-amplifier output resistance = 3 MΩ

R_{CS} is the selected current-sense resistor

Determining the Compensation Component Values

Select a unity-gain crossover frequency (f_{CROS}), which is lower than z_{RHP} and p_{OUT2} and higher than p_{OUT1}. Using f_{CROS}, calculate the compensation resistor (R_{COMP}).

$$R_{COMP} = \frac{f_{CROS} \times R_O}{A_{DC} \times P_{OUT1} - f_{CROS}}$$

Select the next smaller standard value of resistor and then calculate the compensation capacitor required to cancel out the output-capacitor-induced pole (P_{OUT1}) determined previously.

$$C_{COMP} = \frac{1}{6.28 \times P_{OUT1} \times R_{COMP}}$$

Choose the next larger standard value of capacitor.

In order for p_{COMP} to compensate the loop, the open-loop gain must reach unity at a lower frequency than the right-half-plane zero or the second output pole, whichever is lower in frequency. If the second output pole and the right-half-plane zero are close together in frequency, the higher resulting phase shift at unity gain may require a lower crossover frequency. For duty cycles greater than 50%, slope compensation reduces A_{DC}, reducing the actual crossover frequency from f_{CROS}. It is also a good practice to reduce noise on COMP with a capacitor (C_{COMP2}) to ground. To avoid adding extra phase margin at the crossover, the capacitor (C_{COMP2}) should roll-off noise at five times the crossover frequency. The value for C_{COMP2} can be found using:

$$C_{COMP2} = \frac{R_O + R_{COMP}}{5 \times 6.28 \times f_{CROS} \times R_O \times R_{COMP}}$$

It might require a couple iterations to obtain a suitable combination of compensation components.

Finally, the zero introduced by the output capacitor's ESR must be compensated. This compensation is accomplished by placing a capacitor between REF and FB creating a pole directly in the feedback loop. Calculate the value of this capacitor using the frequency of z_{ESR} and the selected feedback resistor values with the formula:

$$C_{FB} = R_{ESR} \times C_{OUT} \times \frac{R_1 + R_2}{R_1 \times R_2}$$

When using low-ESR, ceramic chip capacitors (MLCCs) at the output, calculate the value of C_{FB} as follows:

$$C_{FB} = \frac{R_1 + R_2}{2 \times 3.14 \times f_{OSC} \times R_1 \times R_2}$$

Applications Information

Maximum Output Power

The maximum output power that the MAX1846/MAX1847 can provide depends on the maximum input power available and the circuit's efficiency:

$$P_{OUT(MAX)} = \text{Efficiency} \times P_{IN(MAX)}$$

Furthermore, the efficiency and input power are both functions of component selection. Efficiency losses can be divided into three categories: 1) resistive losses across the inductor, MOSFET on-resistance, current-sense resistor, rectification diode, and the ESR of the input and output capacitors; 2) switching losses due to the MOSFET's transition region, and charging the MOSFET's gate capacitance; and 3) inductor core losses. Typically, 80% efficiency can be assumed for initial calculations. The required input power depends on the inductor current limit, input voltage, output voltage, output current, inductor value, and the switching frequency. The maximum output power is approximated by the following formula:

$$P_{MAX} = [V_{IN} - (V_{LIM} + I_{LIM} \times R_{DS(ON)})] \times I_{LIM} \times [1 - (LIR / 2)] \times [(-V_{OUT} + V_D) / (V_{IN} - V_{SW} - V_{LIM} - V_{OUT} + V_D)]$$

where I_{LIM} is the peak current limit and LIR is the inductor current-ripple ratio and is calculated by:

$$LIR = I_{LPP} / I_{LDC}$$

Again, remember that V_{OUT} for the MAX1846/MAX1847 is negative.

Diode Selection

The MAX1846/MAX1847's high-switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. Ensure that the diode's average current rating exceeds the peak inductor current by using the diode manufacturer's data. Additionally, the diode's reverse breakdown voltage must exceed the potential difference between V_{OUT} and the input voltage plus the leakage-inductance spikes. For high output voltages (-50V or more), Schottky diodes may not be practical because of this voltage requirement. In these cases, use an ultrafast recovery diode with adequate reverse-breakdown voltage.

Input Filter Capacitor

The input capacitor (C_{IN}) must provide the peak current into the inverter. This capacitor is selected the same way as the output capacitor (C_{OUT}). Under ideal conditions, the RMS current for the input capacitor is the same as the output capacitor. The capacitor value and ESR must be selected to reduce noise to an acceptable value and also handle the ripple current (I_{NRMS} where:

$$I_{NRMS} = \frac{1.2 \times I_O}{(I - D_{MAX})} \times \sqrt{D_{MAX} - D_{MAX}^2}$$

Bypass Capacitor

In addition to C_{IN} and C_{OUT}, other ceramic bypass capacitors are required with the MAX1846/MAX1847. Bypass REF to GND with a 0.1µF or larger capacitor. Bypass V_L to GND with a 0.47µF or larger capacitor. All bypass capacitors should be located as close to their respective pins as possible.

PC Board Layout Guidelines

Good PC board layout and routing are required in high-frequency-switching power supplies to achieve good regulation, high efficiency, and stability. It is strongly recommended that the evaluation kit PC board layouts be followed as closely as possible. Place power components as close together as possible, keeping their traces short, direct, and wide. Avoid interconnecting the ground pins of the power components using vias through an internal ground plane. Instead, keep the power components close together and route them in a “star” ground configuration using component-side copper, then connect the star ground to internal ground using multiple vias.

Main Application Circuits

The MAX1846/MAX1847 are extremely versatile devices. Figure 2 shows a generic schematic of the MAX1846. Table 1 lists component values for several typical applications. These component values also apply to the MAX1847. The first two applications are featured in the MAX1846/MAX1847 EV kit.

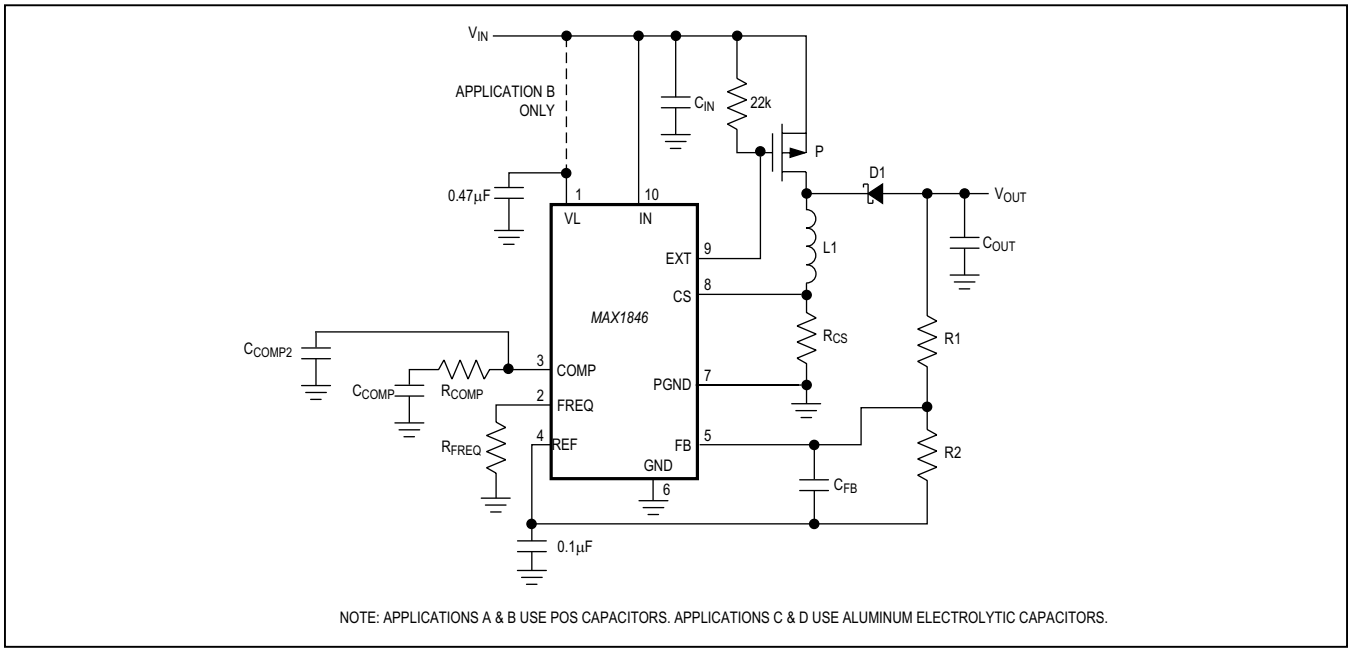


Figure 2. MAX1846 Main Application Circuit

Table 1. Component List for Main Application Circuits

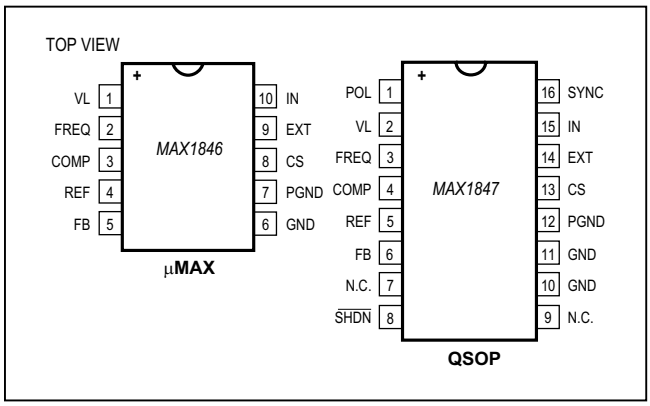
CIRCUIT ID	A	B	C	D
Input (V)	12	3 to 5.5	12	12
Output (V)	-5	-12	-48	-72
Output (A)	2	0.4	0.1	0.1
C_{COMP} (µF)	0.047	0.22	0.1	0.068
C_{IN} (µF)	3 x 10	3 x 22	10	10
C_{OUT} (µF)	2 x 100	2 x 47	39	39
C_{FB} (pF)	390	1200	1000	1000
R1 (kΩ) (1%)	40.2	95.3	383	576
R2 (kΩ) (1%)	10	10	10	10
R_{COMP} (kΩ)	8.2	10	220	470
R_{CS} (Ω)	0.02	0.02	0.05	0.05
R_{FREQ} (kΩ)	150	150	150	150
D1	CMSH5-40	CMSH5-40	CMR1U-02	CMR1U-02
L1 (µH)	10	10	47	82
P1	FDS6685	FDS6375	IRFR5410	IRFR5410
C_{COMP2} (pF)	220	220	22	12

Component Suppliers

SUPPLIER	COMPONENT	PHONE	WEBSITE
AVX	Capacitors	803-946-0690	www.avxcorp.com
Central Semiconductor	Diodes	516-435-1110	www.centralsemi.com
Coilcraft	Inductors	847-639-6400	www.coilcraft.com
Dale	Resistors	402-564-3131	www.vishay.com/company/brands/dale/
Fairchild	MOSFETs	408-721-2181	www.fairchildsemi.com
International Rectifier	MOSFETs	310-322-3331	www.irf.com
IRC	Resistors	512-992-7900	www.irctt.com
Kemet	Capacitors	864-963-6300	www.kemet.com
On Semiconductor	MOSFETs, Diodes	602-303-5454	www.onsemi.com
Panasonic	Capacitors, resistors	201-348-7522	www.panasonic.com
Sanyo	Capacitors	619-661-6835	www.secc.co.jp
Siliconix	MOSFETs	408-988-8000	www.siliconix.com
Sprague	Capacitors	603-224-1961	www.vishay.com/company/brands/sprague/
Sumida	Inductors	847-956-0666	www.remtechcorp.com
Vitramon	Resistors	203-268-6261	www.vishay.com/company/brands/vitramon/

Note: *Indicate that you are using the MAX1846/MAX1847 when contacting these component suppliers.*

Pin Configurations



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
10 µMAX	U10+2	21-0061	90-0330
16 QSOP	E16+1	21-0055	90-0167

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	9/10	Added equation in the *Determining the Compensation Component Values* section	16
3	3/14	Removed automotive application from the *Applications* section	1
4	7/16	Extended maximum operating temperature from +85°C to +105°C	1, 2, 4

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