



**THE DATASHEET OF
MAX4754ETE+T**



0.5Ω, Quad SPDT Switches in UCSP/QFN**General Description**

The MAX4754/MAX4754A/MAX4755/MAX4756/MAX4756A low on-resistance, analog switches operate from a single +1.8V to +5.5V supply. The MAX4754/MAX4754A and MAX4755 are dual, double-pole, double-throw (DPDT) switches. The MAX4756/MAX4756A are quad, single-pole double-throw (SPDT) switches. They are configured to route either audio or data signals.

The MAX4754/MAX4754A have four 0.5Ω SPDT switches for audio-signal routing and two logic control inputs. The MAX4755 has four 0.5Ω SPDT switches (with two switches that have an additional 11Ω series resistor at the NC terminals). This allows users to drive an 8Ω speaker as a 32Ω load (ear speaker). The MAX4756/MAX4756A have four 0.5Ω SPDT switches controlled by one logic control input and an enable input (EN) to disable the switches.

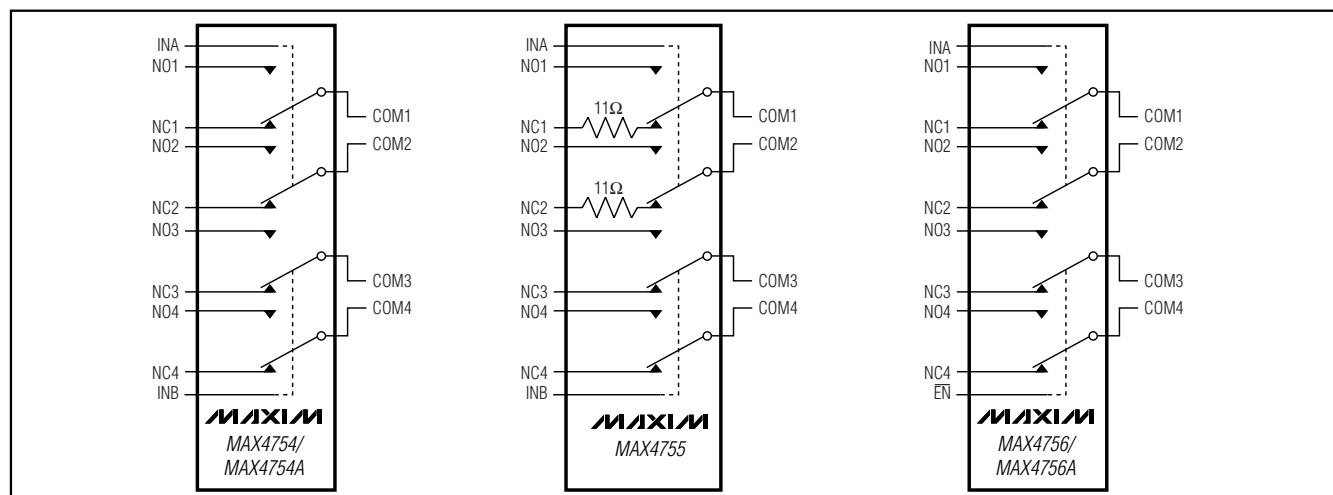
The MAX4754/MAX4754A/MAX4755/MAX4756/MAX4756A are available in a space-saving 16-pin TQFN and a tiny 16-bump, 2mm x 2mm chip-scale package (UCSP™).

Applications

Speaker-Headset Switching
Audio-Signal Routing
Cellular Phones
PDAs/Handheld Devices
Notebook Computers

UCSP is a trademark of Maxim Integrated Products, Inc.

Pin Configurations appear at end of data sheet.

**Features**

- ◆ Data and Audio-Signal Routing
- ◆ Low R_{ON} (0.5Ω typ) Audio Switches
- ◆ 0.1Ω (typ) Channel-to-Channel Matching
- ◆ 0.2Ω (typ) On-Resistance Flatness
- ◆ 0.035% (typ) THD
- ◆ Improved Power-Supply Current for Non-Rail-to-Rail Control Logic Inputs (MAX4754A/MAX4756A)
- ◆ +1.8V to +5.5V Supply Range
- ◆ Rail-to-Rail Signal Handling
- ◆ 16-Bump UCSP (2mm x 2mm)

Ordering Information

PART	PIN-PACKAGE	PKG CODE
MAX4754EBE+T	16 UCSP-16	B16-1
MAX4754ETE+T	16 TQFN-EP**	T1644-4
MAX4754AEBE+T	16 UCSP-16	B16-1
MAX4754AETE+T	16 TQFN-EP**	T1644-4
MAX4755EBE+T*	16 UCSP-16	B16-1
MAX4755ETE+T*	16 TQFN-EP**	T1644-4
MAX4756EBE+T*	16 UCSP-16	B16-1
MAX4756ETE+T*	16 TQFN-EP**	T1644-4
MAX4756AEBE+T*	16 UCSP-16	B16-1
MAX4756AETE+T*	16 TQFN-EP**	T1644-4

Note: These devices operate over the -40°C to +85°C operating temperature range.

*Future product—contact factory for availability.

**EP = Exposed paddle.

+Denotes lead-free package.

Functional Diagrams

0.5Ω, Quad SPDT Switches in UCSP/QFN

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)

V+, IN_, EN_	-0.3V to +6V
COM_, NO_, NC_ (Note 1)	-0.3V to (V+ + 0.3V)
Continuous Current	
NC1, NC2, COM1, COM2 (MAX4755)	±100mA
NO_, NC_, COM_ (remaining terminal connections)	±300mA
Peak Current NC1, NC2, COM1, COM2 (MAX4755)	
(Pulsed at 1ms, 10% duty cycle)	±200mA
(Pulsed at 1ms, 50% duty cycle)	±150mA
Peak Current NO_, NC_,	
COM_ (remaining terminal connections)	
(Pulsed at 1ms, 10% duty cycle)	±500mA
(Pulsed at 1ms, 50% duty cycle)	±400mA

Continuous Power Dissipation (T _A = +70°C)	
16-Bump UCSP (derate 8.2mW/°C above +70°C)660mW
16-Pin TQFN (derate 16.9mW/°C above +70°C)1349mW
ESD per Method 3015.7	±2kV
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Bump Temperature (soldering)	
Infrared (15s)	+220°C
Vapor Phase (60s)	+215°C
Lead Temperature (soldering, 10s)	+300°C

Note 1: Signals on NO_, NC_, COM_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +2.7V to +5.25V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at +3V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		T _A	MIN	TYP	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V _{COM_} , V _{NO_} , V _{NC_}			T _{MIN} to T _{MAX}	0		V+	V
On-Resistance	R _{ON}	V+ = 2.7V, I _{COM_} = 10mA, V _{NC_} or V _{NO_} = 0V or V+ (Note 4)	MAX4755 (NO1, NO2, N_3, N_4), MAX4754/ MAX4754A/MAX4756/ MAX4756A	+25°C		0.5	0.85	Ω
				T _{MIN} to T _{MAX}			1.0	
				+25°C		11.5		
			MAX4755 (NC1, NC2)	T _{MIN} to T _{MAX}	8.0		12.5	
On-Resistance Match Between Channels	ΔR _{ON}	V+ = 2.7V, I _{COM_} = 10mA, V _{NC_} or V _{NO_} = +1.5V (Notes 4, 5)	MAX4755 (NO1, NO2, N_3, N_4) MAX4754/ MAX4756	+25°C		0.1	0.35	Ω
				T _{MIN} to T _{MAX}			0.55	
			MAX4755 (NC1, NC2)	+25°C		0.2	0.4	
				T _{MIN} to T _{MAX}			0.55	
			MAX4754A/MAX4756A	+25°C		0.1	0.35	
				T _{MIN} to T _{MAX}			0.55	
On-Resistance Flatness	R _{FLAT(ON)}	V+ = 3V, I _{COM_} = 10mA, V _{NO_} or V _{NC_} = 0V, 0.6V, or V+ (Note 6)	MAX4755 (NO1, NO2, N_3, N_4, NO1, NO2), MAX4754/ MAX4754A/MAX4756/ MAX4756A	+25°C		0.2	0.4	Ω
				T _{MIN} to T _{MAX}			0.55	

0.5Ω, Quad SPDT Switches in UCSP/QFN

MAX4754/MAX4754A/MAX4755/MAX4755A/MAX4756/MAX4756A

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +2.7V to +5.25V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at +3V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
NO ₋ , NC ₋ Off-Leakage Current	I _{NO_(OFF)} , I _{NC_(OFF)}	V+ = 3.6V; V _{COM_-} = 3.3V, 0.3V; V _{NO_-} or V _{NC_-} = 0.3V, 3.3V MAX4754/MAX4754A/MAX4755/MAX4756/ MAX4756A	+25°C	-4		+4	nA
			T _{MIN} to T _{MAX}	-10		+10	
COM ₋ Off-Leakage Current	I _{COM_(OFF)}	V+ = 3.6V (MAX4756/MAX4756A); V _{COM_-} = 3.3V, 0.3V; V _{NO_-} or V _{NC_-} = 0.3V, 3.3V	+25°C	-6	0.01	+6	Ω
			T _{MIN} to T _{MAX}	-15		+15	
COM ₋ On-Leakage Current	I _{COM_(ON)}	V+ = 3.6V; V _{COM_-} = 3.3V, 0.3V; V _{NO_-} or V _{NC_-} = 3.3V, 0.3V or unconnected	+25°C	-3		+3	nA
			T _{MIN} to T _{MAX}	-15		+15	
DYNAMIC							
Turn-On Time NC ₋	t _{ON, NC}	V+ = 2.7V, V _{NC_-} = 1.5V, R _L = 50Ω, C _L = 35pF (Figure 1) MAX4754A/MAX4756A	+25°C		320	650	ns
			T _{MIN} to T _{MAX}			900	
Turn-Off Time NC ₋	t _{OFF, NC}	V+ = 2.7V, V _{NC_-} = 1.5V, R _L = 50Ω, C _L = 35pF (Figure 1) MAX4754A/MAX4756A	+25°C		27	60	ns
			T _{MIN} to T _{MAX}			70	
Turn-On Time NO ₋	t _{ON, NO}	V+ = 2.7V, V _{NC_-} = 1.5V, R _L = 50Ω, C _L = 35pF (Figure 1) MAX4754A/MAX4756A	+25°C		70	150	ns
			T _{MIN} to T _{MAX}			200	
Turn-Off Time NO ₋	t _{OFF, NO}	V+ = 2.7V, V _{NC_-} = 1.5V, R _L = 50Ω, C _L = 35pF (Figure 1) MAX4754A/MAX4756A	+25°C		300	650	ns
			T _{MIN} to T _{MAX}			900	
Turn-On Time	t _{ON}	V+ = 2.7V, V _{NO_-} or V _{NC_-} = 1.5V; R _L = 50Ω; C _L = 35pF, (Figure 1) MAX4754/MAX4755/MAX4756	+25°C		45	140	ns
			T _{MIN} to T _{MAX}			150	
Turn-Off Time	t _{OFF}	V+ = 2.7V, V _{NO_-} or V _{NC_-} = 1.5V; R _L = 50Ω; C _L = 35pF (Figure 1) MAX4754/MAX4755/MAX4756	+25°C		25	50	ns
			T _{MIN} to T _{MAX}			60	
Break-Before-Make	t _{BBM}	V+ = 2.7V, V _{NO_-} or V _{NC_-} = 1.5V; R _L = 50Ω, C _L = 35pF (Figure 2) (Note 7)	+25°C		15		ns
			T _{MIN} to T _{MAX}		2		
Charge Injection	Q	V _{GEN} = 0V, R _{GEN} = 0, C _L = 1.0nF (Figure 3)	+25°C		300		pC
On-Channel -3dB Bandwidth	BW	Signal = 0dBm, C _L = 50pF, R _s = 50Ω, R _L = 50Ω	+25°C		10		MHz
Off-Isolation	V _{ISO}	C _L = 5pF, R _L = 50Ω, V _{COM_-} = 1V _{P-P} f = 100kHz (Figure 4) (Note 8)	+25°C		-65		dB
Crosstalk	V _{CT}	C _L = 5pF, R _L = 50Ω, V _{COM_-} = 1V _{P-P} f = 100kHz (Figure 4) (Note 9)	+25°C		-90		dB

0.5Ω, Quad SPDT Switches in UCSP/QFN

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +2.7V to +5.25V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at +3V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
Total Harmonic Distortion	THD	f = 20Hz to 20kHz, 1V _{p-p} , R _L = 32Ω, V _{DC} = V+/2	+25°C		0.035		%
NO ₋ , NC ₋ Off-Capacitance	C _{NO_(OFF)} , C _{NC_(OFF)}	V _{NO} , V _{NC} = GND, f = 1MHz (Figure 5)	+25°C		180		pF
COM ₋ Off-Capacitance	C _{COM_(OFF)}	V _{COM} = GND, f = 1MHz (Figure 5)	+25°C		300		pF
COM ₋ On-Capacitance	C _(ON)	V _{COM} = GND, f = 1MHz (Figure 5)	+25°C		400		pF
DIGITAL I/O (IN₋, EN)							
Input Logic-High	V _{IH}	V+ = 2.7V to 3.6V, MAX4754/MAX4755/MAX4756	T _{MIN} to T _{MAX}	1.4			V
		V+ = 2.7V to 5.25V, MAX4754A/MAX4756A	T _{MIN} to T _{MAX}	1.4			
		V+ = 3.6V to 5.25V, MAX4754/MAX4755/MAX4756	T _{MIN} to T _{MAX}	2.0			
Input Logic-Low	V _{IL}	V+ = 2.7V to 3.6V, MAX4754/MAX4755/MAX4756	T _{MIN} to T _{MAX}			0.5	V
		V+ = 2.7V to 5.25V, MAX4754A/MAX4756A	T _{MIN} to T _{MAX}			0.5	
		V+ = 3.6V to 5.25V, MAX4754/MAX4755/MAX4756	T _{MIN} to T _{MAX}			0.6	
Input Leakage Current	I _{IN}	V _{IN} = 0V or V+	T _{MIN} to T _{MAX}			1	μA
POWER SUPPLY							
Power-Supply Range	V+		T _{MIN} to T _{MAX}	1.8		5.5	V
Power-Supply Current	I+	V+ = 5.5V, V _{IN} = 0V or V+, MAX4754/MAX4754A/MAX4755/MAX4756/MAX4756A	+25°C		0.2		μA
			T _{MIN} to T _{MAX}			2	
		V+ = 5.5V, V _{IN} = 0.5V or 1.4V, MAX4754A/MAX4756A	+25°C		6.5		μA
	T _{MIN} to T _{MAX}			12			

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 3: UCSP parts are 100% tested at +25°C and limits across the full temperature range are guaranteed by correlation and design. TQFN parts are 100% tested at +85°C and limits across the full temperature range are guaranteed by correlation and design.

Note 4: R_{ON} and ΔR_{ON} matching specifications are guaranteed by design and correlation.

Note 5: ΔR_{ON} = R_{ON(MAX)} - R_{ON(MIN)}.

Note 6: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Note 7: Guaranteed by design, not production tested.

Note 8: Off-Isolation = 20log₁₀ [V_{COM} / (V_{NO} or V_{NC})], V_{COM} = output, V_{NO} or V_{NC} = input to off switch.

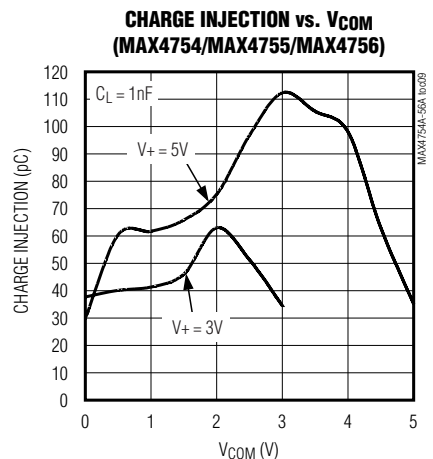
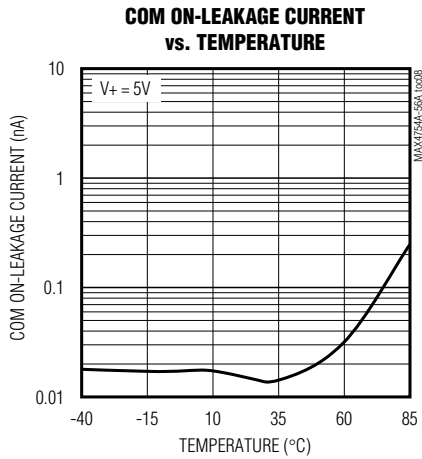
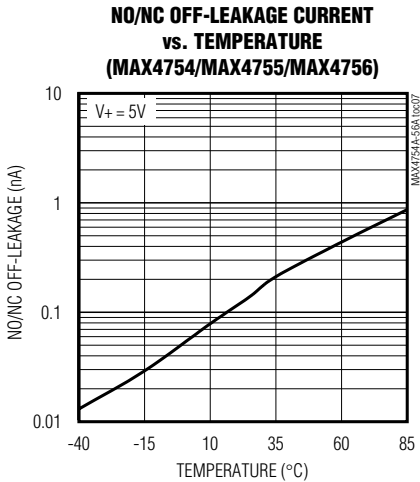
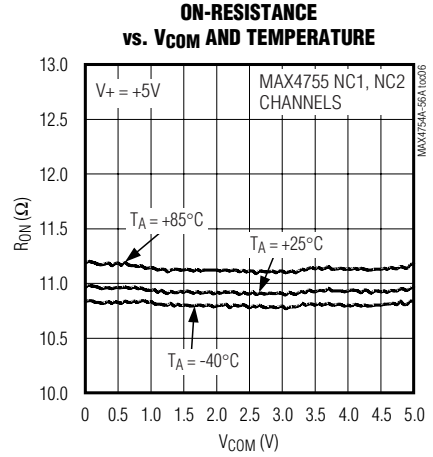
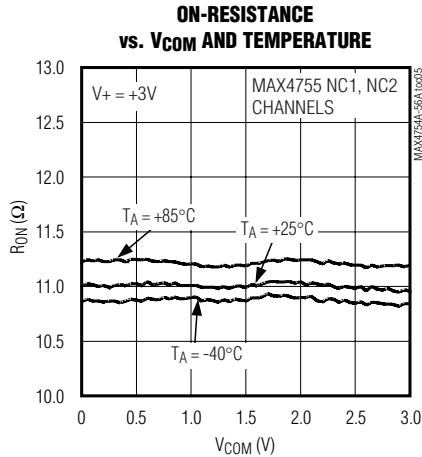
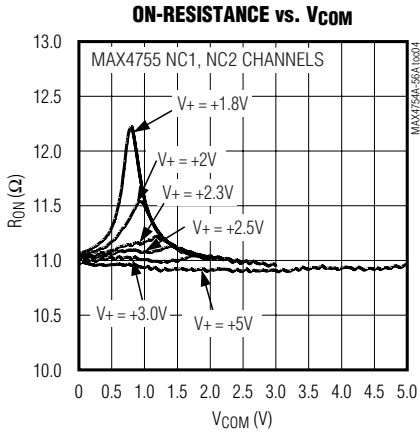
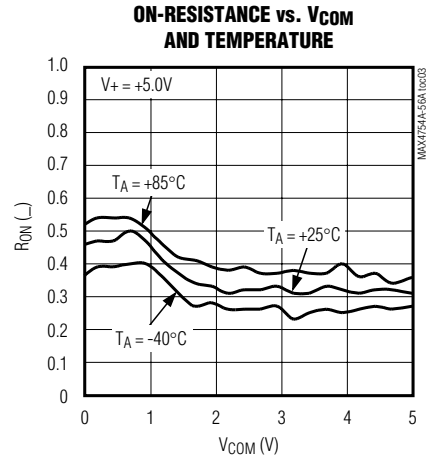
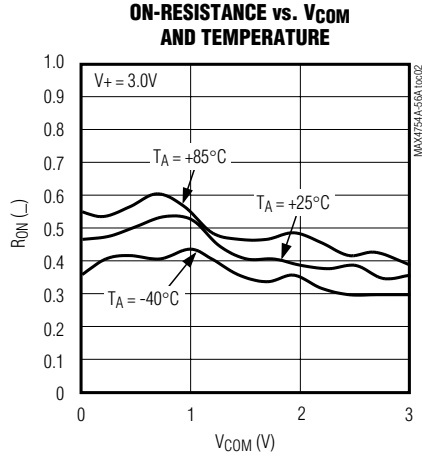
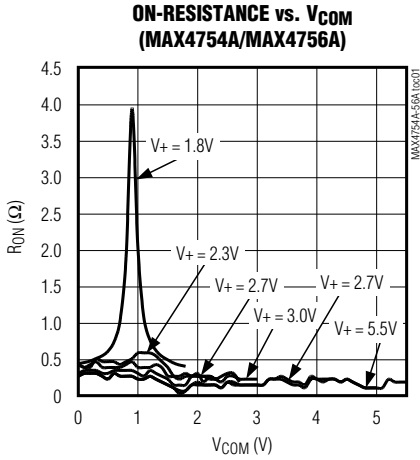
Note 9: Between any two switches.

0.5Ω, Quad SPDT Switches in UCSP/QFN

Typical Operating Characteristics

($V_+ = 3V$, $T_A = +25^\circ C$, unless otherwise noted.)

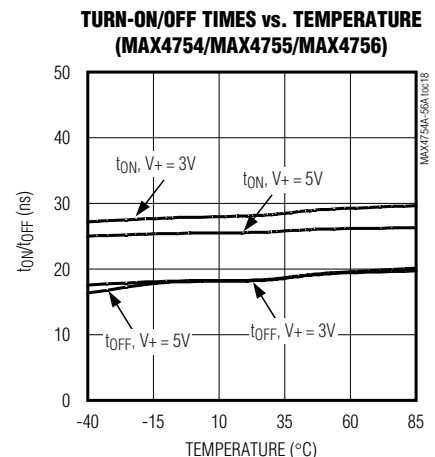
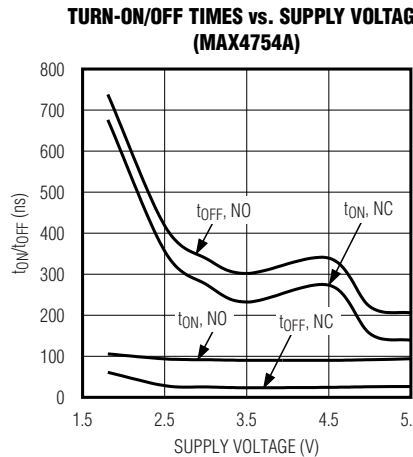
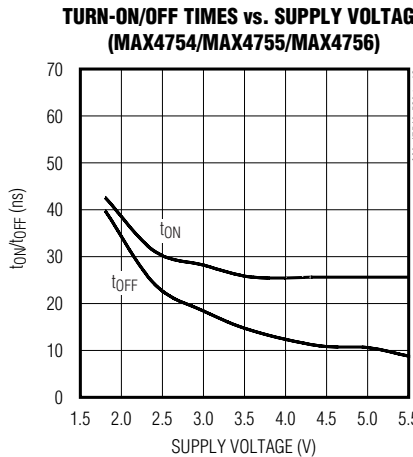
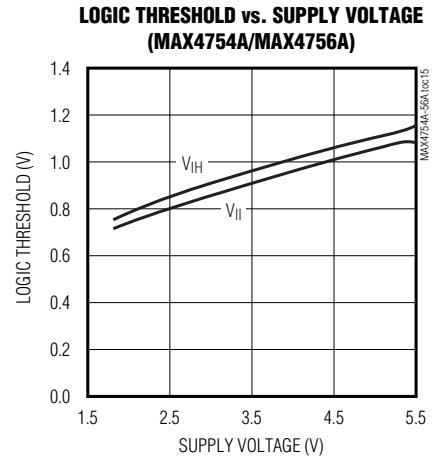
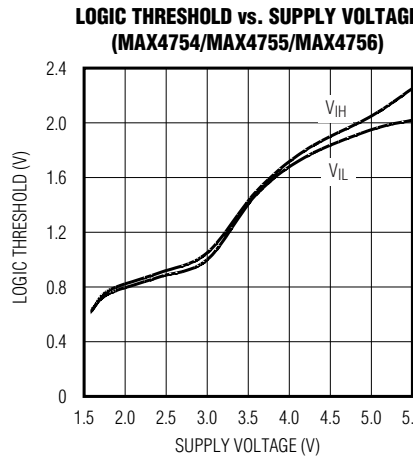
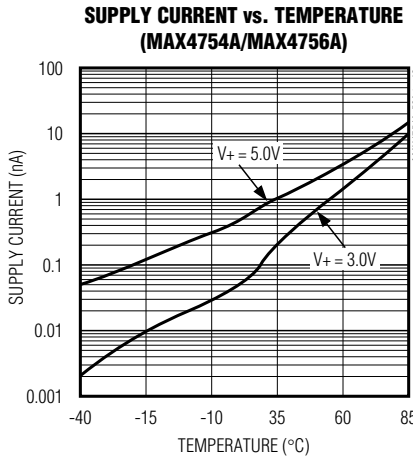
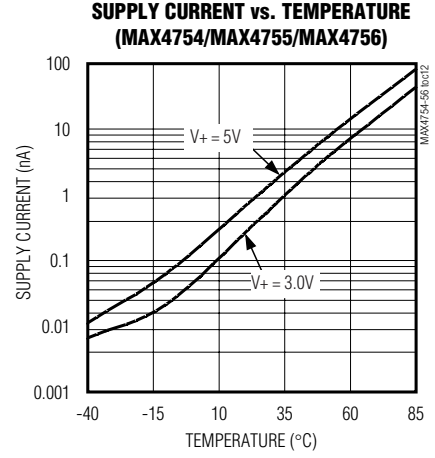
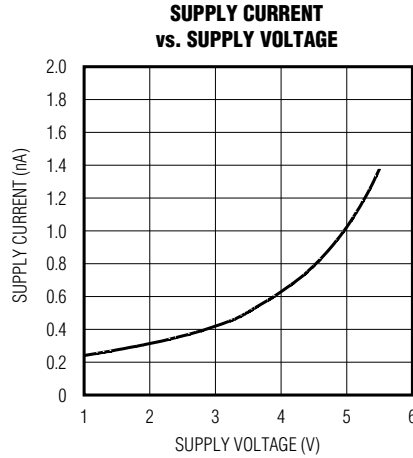
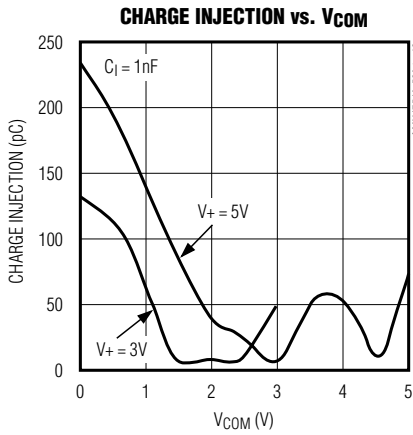
MAX4754/MAX4754A/MAX4755/MAX4755A/MAX4756/MAX4756A



0.5Ω, Quad SPDT Switches in UCSP/QFN

Typical Operating Characteristics (continued)

(V+ = 3V, TA = +25°C, unless otherwise noted.)

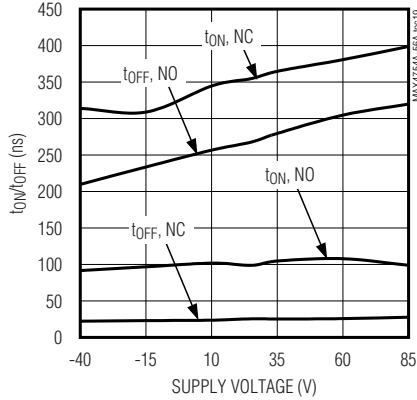


0.5Ω, Quad SPDT Switches in UCSP/QFN

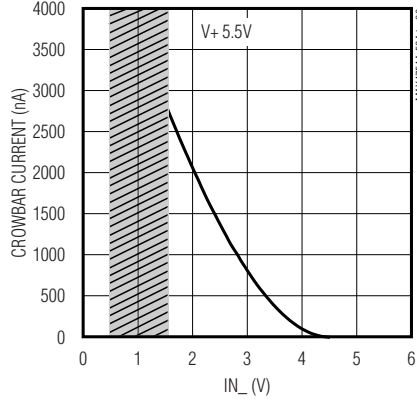
Typical Operating Characteristics (continued)

(V+ = 3V, TA = +25°C, unless otherwise noted.)

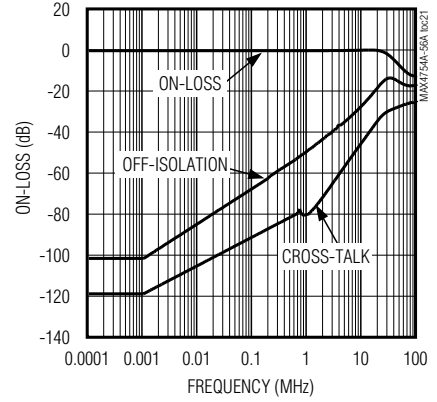
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(MAX4754A)**



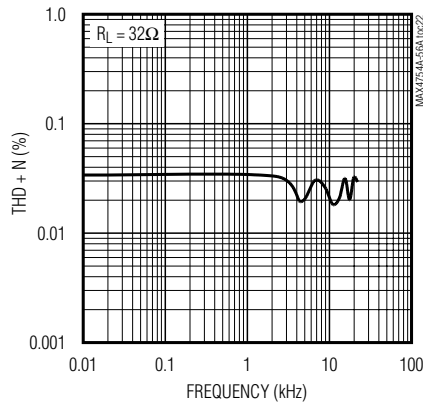
**SUPPLY CURRENT
vs. LOGIC CONTROL INPUT**



FREQUENCY RESPONSE



**TOTAL HARMONIC DISTORTION
PLUS NOISE vs. FREQUENCY**



MAX4754/MAX4754A/MAX4755/MAX4755A/MAX4756/MAX4756A

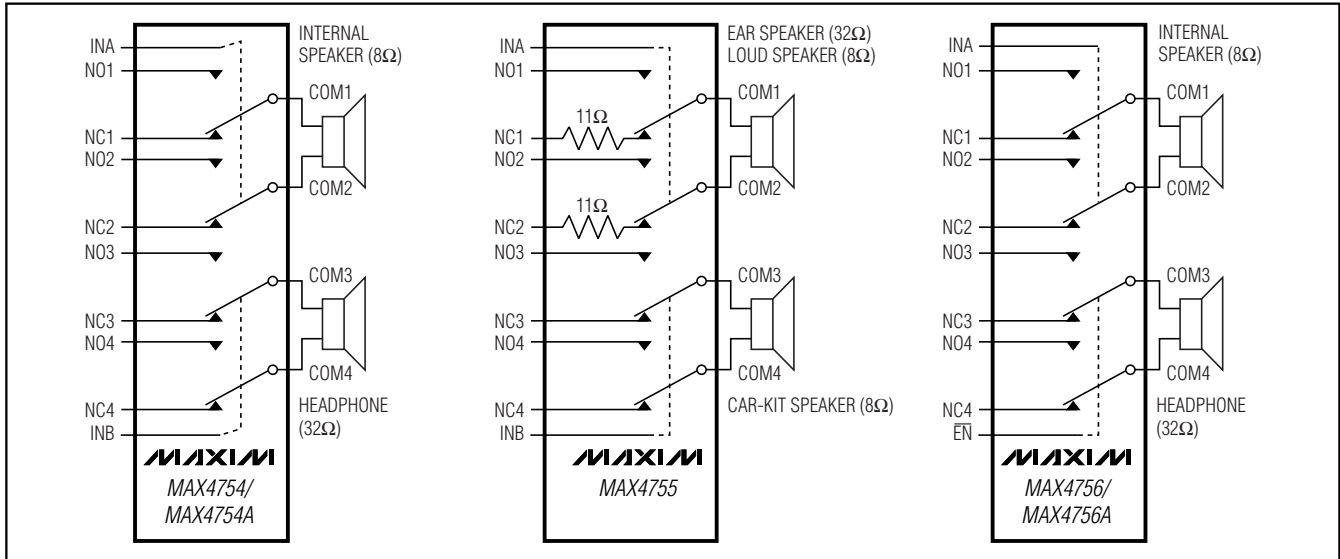
0.5Ω, Quad SPDT Switches in UCSP/QFN

Pin Description

PIN						NAME	FUNCTION
MAX4754/MAX4754A		MAX4755		MAX4756/MAX4756A			
UCSP	QFN	UCSP	QFN	UCSP	QFN		
C1	1	C1	1	C1	1	NO1	Analog Switch 1. Normally open terminal 1.
C2	2	C2	2	C2	2	INA	Logic Control Digital Input for Switches 1 and 2. Digital control input for switches 1–4 for MAX4756.
B1	3	B1	3	B1	3	COM1	Analog Switch 1. Common terminal.
A1	4	A1	4	A1	4	NC1	Analog Switch 1. Normally closed terminal 1.
A2	5	A2	5	A2	5	NO4	Analog Switch 4. Normally open terminal 4.
B2	6	B2	6	B2	6	V+	Positive Supply Voltage
A3	7	A3	7	A3	7	COM4	Analog Switch 4. Common terminal.
A4	8	A4	8	A4	8	NC4	Analog Switch 4. Normally closed terminal 4.
B4	9	B4	9	B4	9	NO2	Analog Switch 2. Normally open terminal 2.
B3	10	B3	10	—	—	INB	Logic Control Digital Input for Switches 3 and 4
—	—	—	—	B3	10	\overline{EN}	Output Enable. Active low.
C4	11	C4	11	C4	11	COM2	Analog Switch 2. Common terminal 2.
D4	12	D4	12	D4	12	NC2	Analog Switch 2. Normally closed terminal 2.
D3	13	D3	13	D3	13	NO3	Analog Switch 3. Normally open terminal 3.
C3	14	C3	14	C3	14	GND	Ground
D2	15	D2	15	D2	15	COM3	Analog Switch 3. Common terminal 3.
D1	16	D1	16	D1	16	NC3	Analog Switch 4. Normally closed terminal 3.
—	EP	—	EP	—	EP	EP	Exposed Paddle. Connect EP to GND.

0.5Ω, Quad SPDT Switches in UCSP/QFN

Typical Operating Circuit



Detailed Description

The MAX4754/MAX4754A/MAX4755/MAX4756/MAX4756A low on-resistance analog switches operate from a single +1.8V to +5.5V supply. The devices are fully specified for nominal 3V applications.

The MAX4754/MAX4754A DPDT switch have two logic control inputs with each input controlling two SPDT switches. Each switch has a 0.5Ω on-resistance in the NO and NC terminals making it ideal for switching audio signals.

The MAX4755 DPDT switch also has four 0.5Ω SPDT switches with the switch pairs 1 and 2 adding an 11.5Ω series resistor to the NC terminal. This feature allows the user to drive an 8Ω speaker as a 32Ω load, allowing it to be used as an ear speaker. Two logic control inputs are used to control the four switches.

The MAX4756/MAX4756A has four 0.5Ω SPDT switches controlled by one logic control input (INA) and \overline{EN} input to disable the switches.

Applications Information

Digital Control Inputs

The MAX4754/MAX4754A/MAX4755/MAX4756/MAX4756A logic inputs accept up to +5.5V regardless of the supply voltage. For example, with a +3.3V supply IN_{-} can be driven low to GND and high to +5.5V, which allows mixed logic levels in a system. Driving the control logic

inputs rail-to-rail also minimizes power consumption. For a +3V supply voltage, the logic thresholds are 0.5V (low) and 1.4V (high).

For the MAX4756/MAX4756A, drive \overline{EN} low to enable the COM₋. When \overline{EN} is high, COM₋ is high impedance.

Analog Signal Levels

Analog signal inputs over the full voltage range (0V to V₊) are passed through the switch with minimal change in on-resistance (see the *Typical Operating Characteristics*). The switches are bidirectional so NO₋, NC₋, and COM₋ can be either inputs or outputs.

Power-Supply Bypassing

Power-supply bypassing improves noise margin and prevents switching noise from propagating from the V₊ supply to other components. A 0.1μF capacitor connected from V₊ to GND is adequate for most applications.

UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape carrier information, printed circuit board techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, go to the Maxim website at www.maxim-ic.com/ucsp for the Application Note: *UCSP—A Wafer-Level Chip-Scale Package*.

MAX4754/MAX4754A/MAX4755/MAX4756/MAX4756A

0.5Ω, Quad SPDT Switches in UCSP/QFN

Timing Circuits/Timing Diagrams

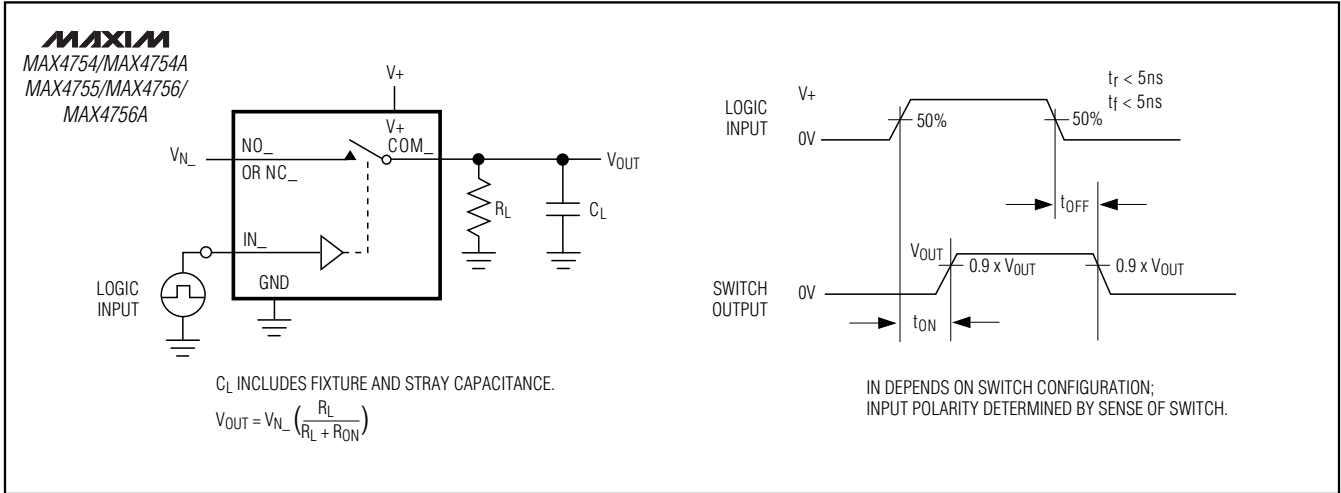


Figure 1. Switching Time

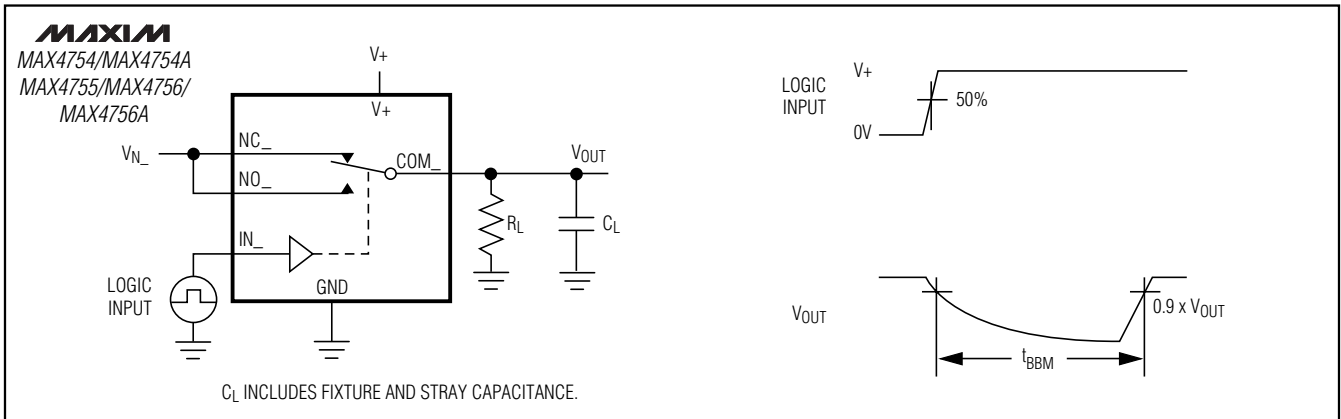


Figure 2. Break-Before-Make Interval

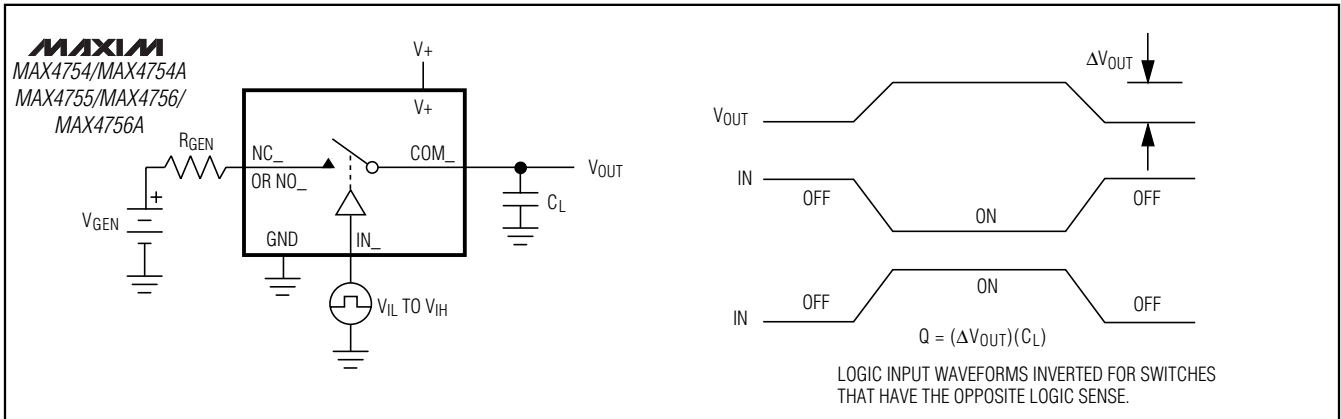


Figure 3. Charge Injection

0.5Ω, Quad SPDT Switches in UCSP/QFN

Timing Circuits/Timing Diagrams (continued)

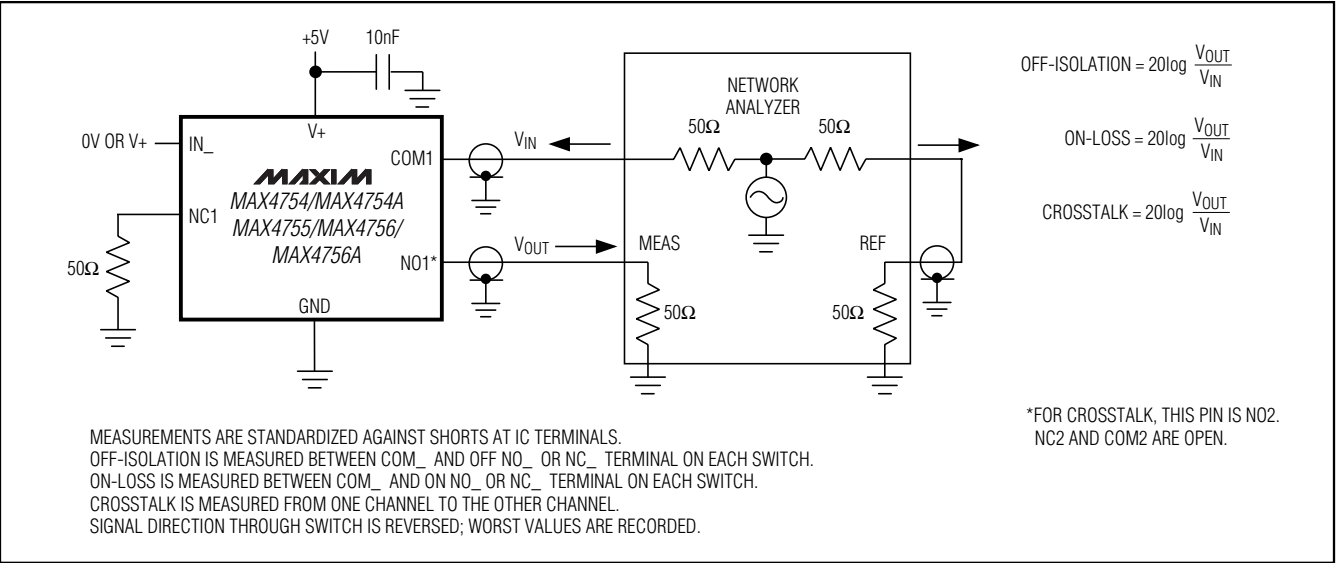


Figure 4. On-Loss, Off-Isolation, and Crosstalk

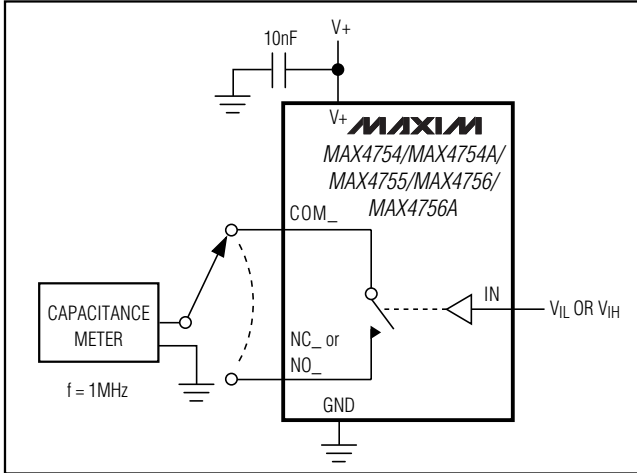


Figure 5. Channel On-/Off-Capacitance

MAX4754/MAX4754A/MAX4755/MAX4756/MAX4756A

0.5Ω, Quad SPDT Switches in UCSP/QFN

Pin Configurations/Truth Tables

TOP VIEW
(BUMP SIDE DOWN)

() FOR MAX4756/MAX4756A.

UCSP

MAX4754/MAX4754A/MAX4755

INA	NO1/NO2	NC1/NC2	NO3/NO4	NC3/NC4
LOW	OFF	ON	—	—
HIGH	ON	OFF	—	—
INB				
LOW	—	—	OFF	ON
HIGH	—	—	ON	OFF

MAXIM
MAX4754
MAX4754A
MAX4755
MAX4756
MAX4756A

TQFN

*EP: EXPOSED PADDLE CONNECTED TO GND.

MAX4756/MAX4756A

EN	INA	NO_	NC_
LOW	LOW	OFF	ON
LOW	HIGH	ON	OFF
HIGH	X	OFF	OFF
HIGH	X	OFF	OFF

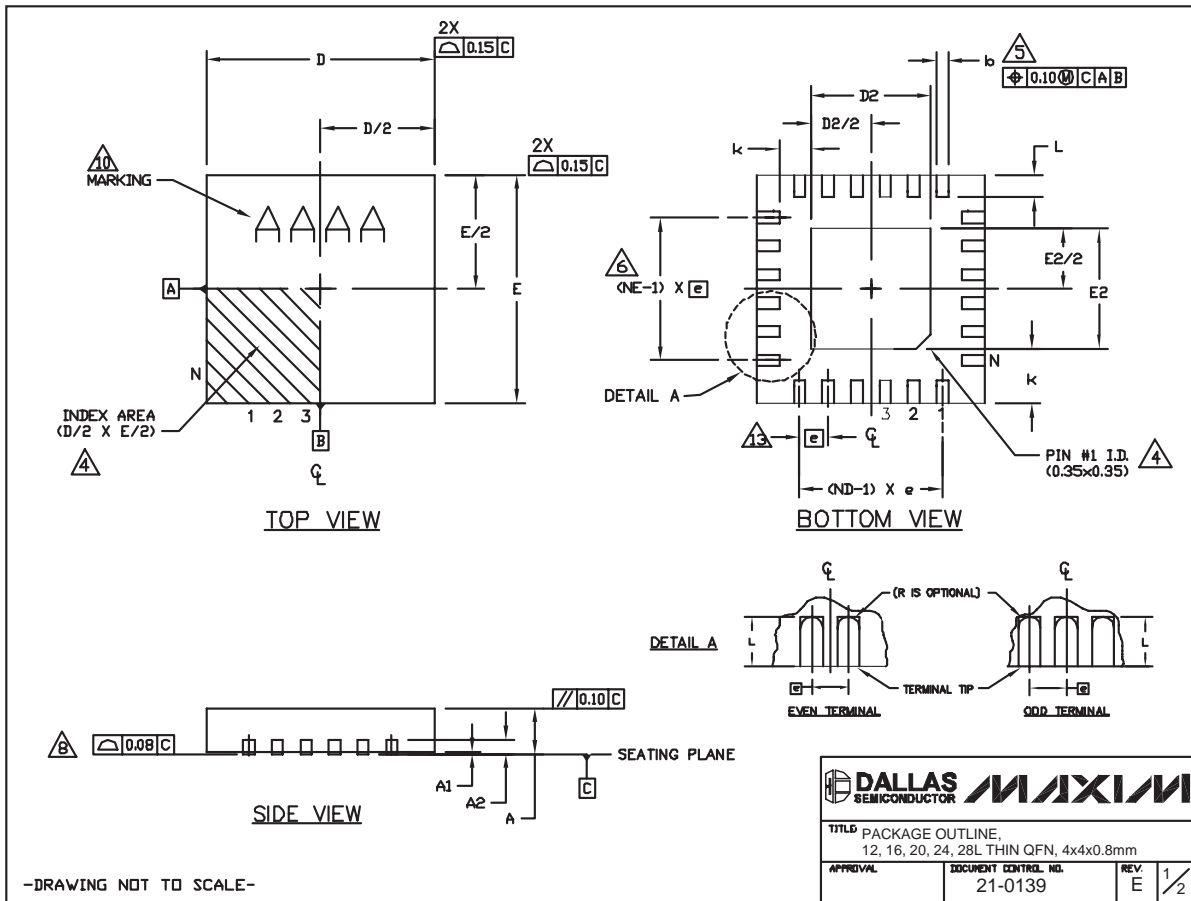
Chip Information

PROCESS: CMOS

0.5Ω, Quad SPDT Switches in UCSP/QFN

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



24L QFN THIN:EPS

MAX4754/MAX4754A/MAX4755/MAX4755A/MAX4756/MAX4756A

0.5Ω, Quad SPDT Switches in UCSP/QFN

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

COMMON DIMENSIONS														EXPOSED PAD VARIATIONS											
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4			PKG. CODES	D2			E2			DOWN BONDS ALLOWED		
REF.	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.		MIN.	NDM.	MAX.	MIN.	NDM.	MAX.			
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES		
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO		
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF			T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25	T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO		
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES		
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO		
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES		
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO		
N	12			16			20			24			28			T2844-1	2.50	2.60	2.70	2.50	2.60	2.70	NO		
ND	3			4			5			6			7												
NE	3			4			5			6			7												
JEDEC Ver.	WGG8			WGC			WGD-1			WGD-2			WGE												

NOTES:

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
- MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
 - COPLANARITY SHALL NOT EXCEED 0.08mm
 - WARPAGE SHALL NOT EXCEED 0.10mm
- LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
- NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

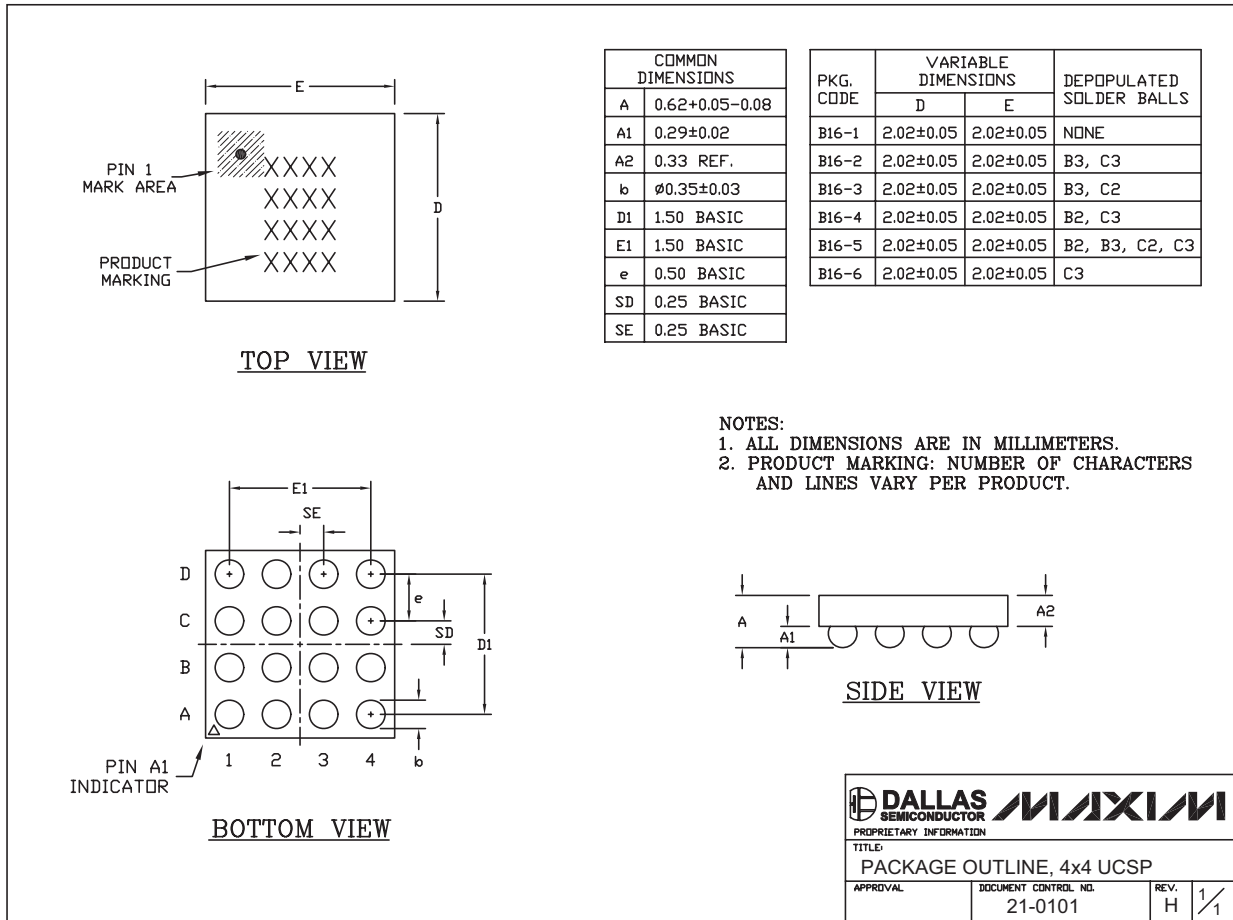
-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM			
TITLE: PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm			
APPROVAL	DOCUMENT CONTROL NO. 21-0139	REV E	2/2

0.5Ω, Quad SPDT Switches in UCSP/QFN

Package Information (continued)

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Revision History

Pages changed at Rev 1: 1-5, 7, 8, 13, 14, 15

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