



**THE DATASHEET OF  
MAX4925ELT+T**





# Overvoltage Protectors with External pFET

MAX4923-MAX4926

## General Description

The MAX4923–MAX4926 overvoltage protection (OVP) controllers protect low-voltage systems against high-voltage faults of up to +28V with an appropriate external pFET. When the input voltage exceeds the overvoltage lockout (OVLO) threshold, or falls below the undervoltage lockout (UVLO) threshold, these devices turn off the pFET to prevent damage to protected components and issue a flag to notify the processor of a fault condition.

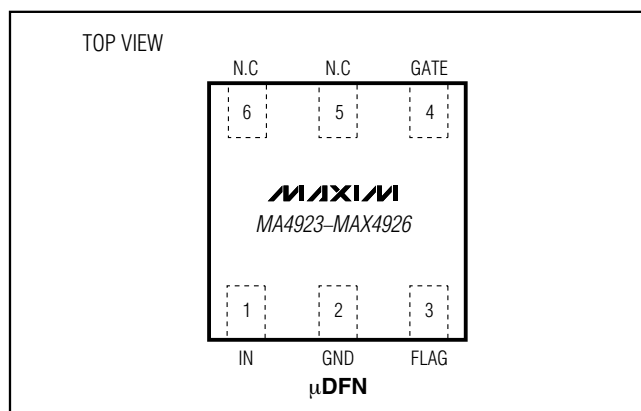
The typical overvoltage trip level is set to 7.18V (MAX4923), 6.16V (MAX4924), 5.65V (MAX4925), and 4.46V (MAX4926). The undervoltage trip level is set to 2.44V (typ) for all devices.

The input (IN) is ESD protected to  $\pm 15\text{kV}$  HBM when bypassed to ground with a  $1\mu\text{F}$  ceramic capacitor. All devices are offered in a small, 6-pin (1.5mm x 1.0mm)  $\mu\text{DFN}$  package and are specified over the extended  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  temperature range.

## Applications

Cell Phones  
Digital Still Cameras  
PDAs and Palmtop Devices  
MP3 Players

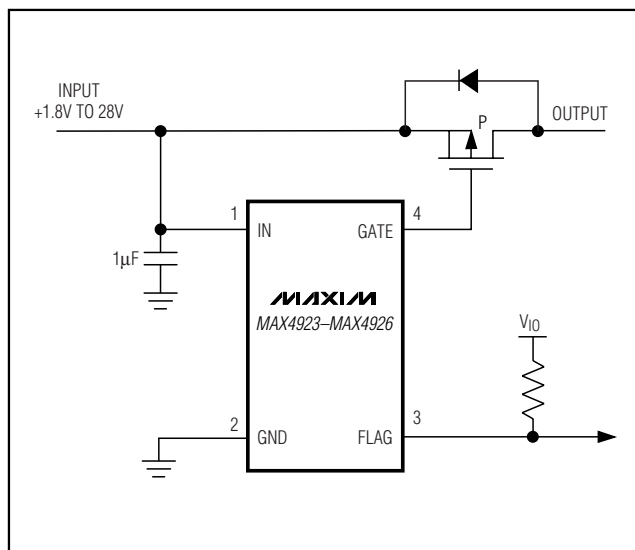
## Pin Configuration



## Features

- ◆ Overvoltage Protection Up to +28V
- ◆ Preset 7.18V, 6.16V, 5.65V, and 4.46V Typical Overvoltage Trip Levels
- ◆ Preset 2.44V Typical Undervoltage Trip Level
- ◆  $\pm 2.5\%$  Accurate Overvoltage/Undervoltage Trip Levels
- ◆ Low  $13\mu\text{A}$  (typ) Supply Current
- ◆ Drives External pFET
- ◆ 20ms Adapter Debounce Time
- ◆ Fault Flag Indicator
- ◆ 6-Pin (1.5mm x 1.0mm)  $\mu\text{DFN}$  Package

## Typical Operating Circuit



## Ordering Information/Selector Guide

PART	PIN-PACKAGE	OVLO (V)	UVLO (V)	TOP MARK	PKG CODE
MAX4923ELT+*	6 $\mu\text{DFN}$	7.18	2.44	LB	L611-1
MAX4924ELT+	6 $\mu\text{DFN}$	6.16	2.44	LC	L611-1
MAX4925ELT+	6 $\mu\text{DFN}$	5.65	2.44	LD	L611-1
MAX4926ELT+	6 $\mu\text{DFN}$	4.46	2.44	LE	L611-1

**Note:** All devices are specified over the  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  operating temperature range.

+Denotes lead-free package.

\*Future Product—contact factory for availability.



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# Overvoltage Protectors with External pFET

## ABSOLUTE MAXIMUM RATINGS

IN, GATE to GND.....	-0.3V to +30V
FLAG to GND .....	-0.3V to +6V
Continuous Power Dissipation (T <sub>A</sub> = +70°C) 6-μDFN (derate 2.1mW/°C above 70°C).....	168mW

Operating Temperature Range .....	-40°C to +85°C
Junction Temperature .....	+150°C
Storage Temperature Range .....	-65°C to +150°C
Lead Temperature (soldering, 10s) .....	+300 °C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>IN</sub> = +5V for MAX4923/MAX4924/MAX4925, V<sub>IN</sub> = +4V for MAX4926, C<sub>GATE</sub> = 500pF to IN, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Input Voltage Range	V <sub>IN</sub>		1.8		28.0	V	
Overvoltage Lockout Level	OVLO	V <sub>IN</sub> rising	MAX4923	7.00	7.18	7.36	V
			MAX4924	6.00	6.16	6.31	
			MAX4925	5.50	5.65	5.79	
			MAX4926	4.35	4.46	4.57	
Overvoltage Lockout Hysteresis		MAX4923		65		mV	
		MAX4924		55			
		MAX4925		50			
		MAX4926		40			
Undervoltage Lockout Level	UVLO	V <sub>IN</sub> falling	2.378	2.439	2.500	V	
Undervoltage Lockout Hysteresis				20		mV	
IN Supply Current	I <sub>IN</sub>	MAX4923/MAX4924/MAX4925		14	25	μA	
		MAX4926		13	23		
GATE Voltage High	V <sub>OH</sub>	V <sub>IN</sub> ≥ 8V, I <sub>SOURCE</sub> = 0.1mA	V <sub>IN</sub> - 0.2			V	
GATE Pulldown Current	I <sub>PD</sub>	V <sub>GATE</sub> = V <sub>IN</sub>	6.5	12		mA	
FLAG Low Voltage	V <sub>OL</sub>	I <sub>SINK</sub> = 1mA			0.4	V	
FLAG Leakage Current	I <sub>LKG</sub>	V <sub>FLAG</sub> = 5.5V	-1		+1	μA	
<b>TIMING CHARACTERISTICS</b>							
Debounce Time	t <sub>DEB</sub>	V <sub>UVLO</sub> < V <sub>IN</sub> < V <sub>OVLO</sub> , time for GATE to go low (Figure 1)	10	20	34	ms	
Gate Turn-on Time	t <sub>GON</sub>	V <sub>GATE</sub> = 5V to 0.5V (MAX4923/MAX4924/MAX4925) or V <sub>GATE</sub> = 4V to 0.5V (MAX4926) (Figure 1)		0.6		μs	
Gate Turn-Off Time	t <sub>GOFF</sub>	V <sub>IN</sub> rising at 1V/μs from 5V to 8V (MAX4923/MAX4924/MAX4925) or from 4V to 7V (MAX4926) to V <sub>GATE</sub> = V <sub>IN</sub> - 0.5V (Figure 1)		5	20	μs	
Flag Assertion Delay	t <sub>FLAG</sub>	V <sub>IN</sub> rising at 1V μs from 5V to 8V (MAX4923/MAX4924/MAX4925) or from 4V to 7V (MAX4926), to V <sub>FLAG</sub> = 2.4V, R <sub>FLAG</sub> = 10kΩ to 3V (Figure 1)		4.5		μs	

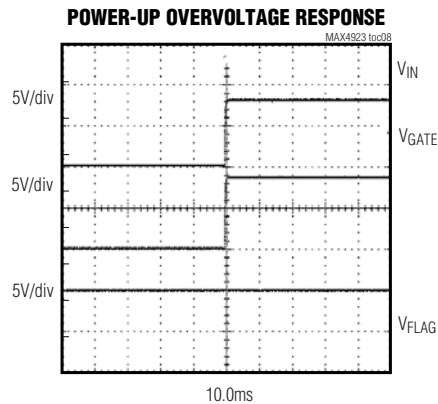
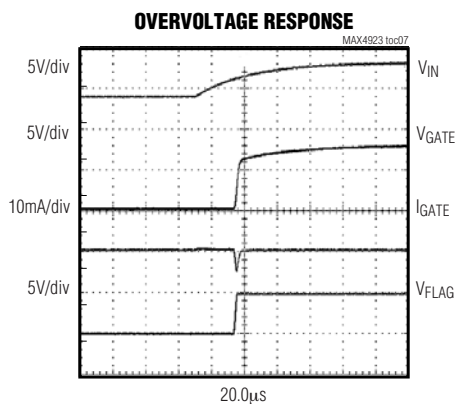
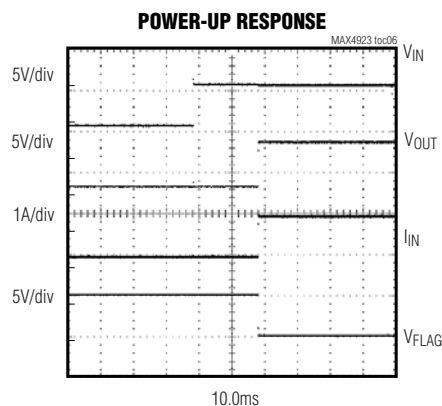
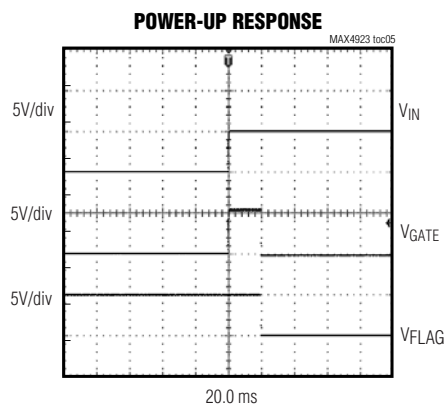
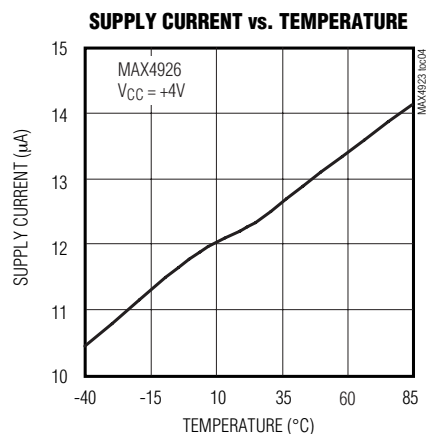
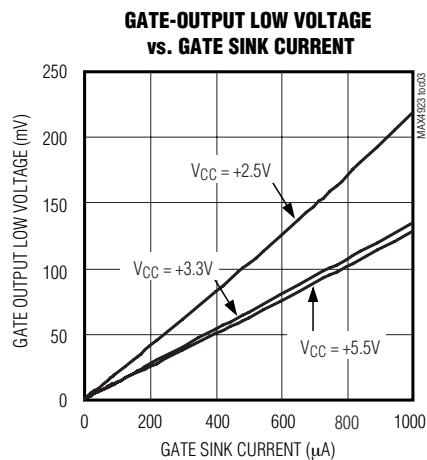
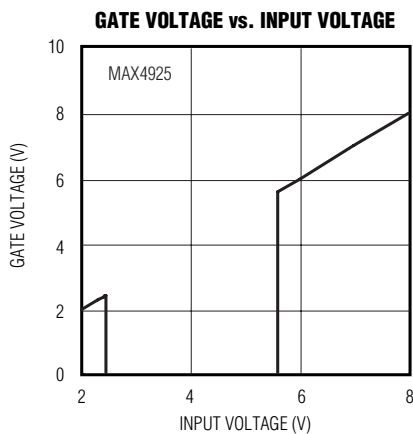
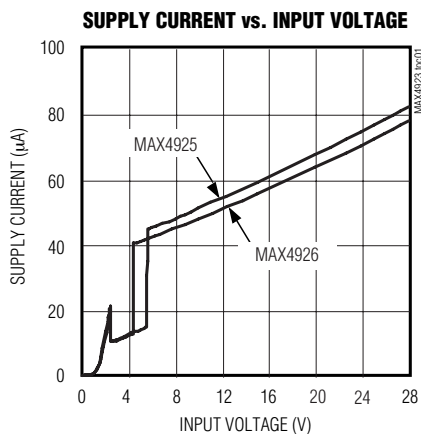
**Note 1:** All devices are 100% tested at +25°C. Electrical limits across the full temperature range are guaranteed by design and characterization.

# Overvoltage Protectors with External pFET

## Typical Operating Characteristics

( $V_{IN} = +5V$  for MAX4923/MAX4924/MAX4925,  $V_{IN} = +4V$  for MAX4926 (pFET = Si6991DQ),  $T_A = +25^\circ C$ , unless otherwise noted.)

MAX4923-MAX4926



# Overvoltage Protectors with External pFET

## Pin Description

PIN	NAME	FUNCTION
1	IN	Voltage Input. IN is both the power-supply input and the overvoltage/undervoltage sense input. Bypass IN to GND with a 1µF ceramic capacitor as close as possible to the device to enable ±15kV (HBM) ESD protection on IN.
2	GND	Ground
3	FLAG	Fault Indication Open-Drain Output. FLAG deasserts high during undervoltage and overvoltage lockout conditions. FLAG asserts low during normal operation.
4	GATE	pFET Gate Drive Output. GATE is driven high during a fault condition to turn off the external pFET. When $V_{UVLO} < V_{IN} < V_{OVLO}$ , GATE is driven low and the external pFET is turned on.
5, 6	N.C.	No Connection. Not internally connected. Leave N.C. unconnected.

## Functional Diagram

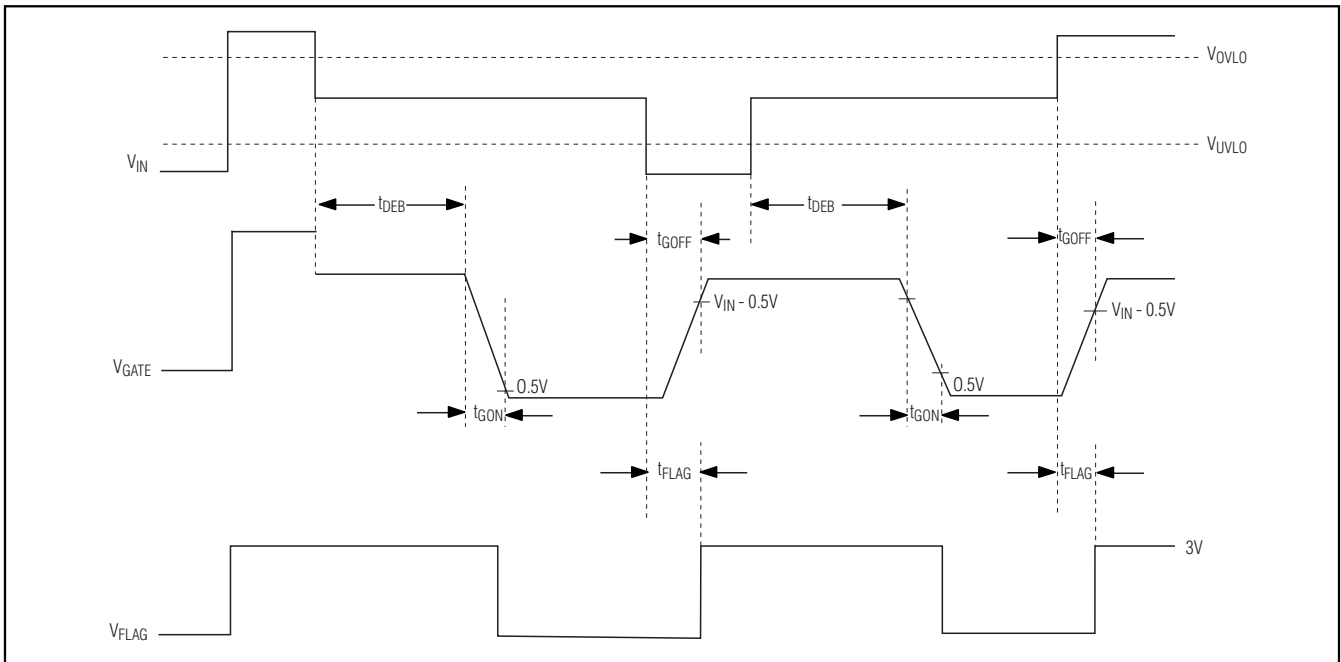
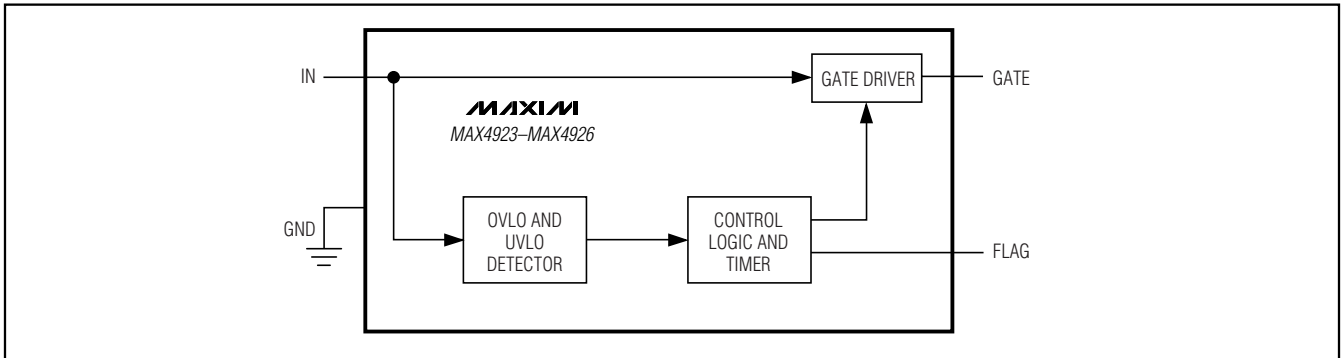


Figure 1. Timing Diagram

# Overvoltage Protectors with External pFET

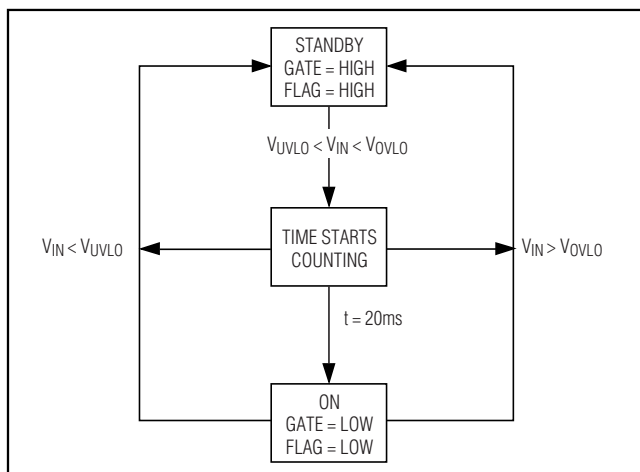


Figure 2. State Machine

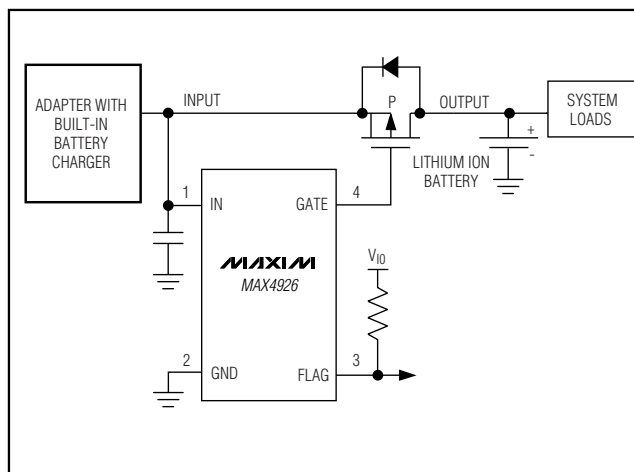


Figure 3. MAX4926 Typical Operating Circuit

## Detailed Description

The MAX4923–MAX4926 overvoltage protection controllers protect low-voltage systems against high-voltage faults of up to +28V when used with a -30V pFET. When the input voltage exceeds the OVLO threshold, these devices turn off the external pFET to prevent damage to protected components.

The typical overvoltage trip level is set to 7.18V (MAX4923), 6.16V (MAX4924), 5.65V (MAX4925), and 4.46V (MAX4926). When the supply drops below the UVLO threshold, the devices turn off the external pFET.

IN is ESD protected to  $\pm 15\text{kV}$  (Human Body Model) when bypassed with a  $1\mu\text{F}$  ceramic capacitor to ground.

### Undervoltage Lockout (UVLO)

The MAX4923–MAX4926 have a fixed 2.44V (typ) UVLO level. When  $V_{IN}$  is less than  $V_{UVLO}$ , GATE is high and FLAG is high.

### Overvoltage Lockout (OVLO)

The MAX4923 has a 7.18V (typ) OVLO; the MAX4924 has a 6.16V (typ) OVLO; the MAX4925 has a 5.65V (typ) OVLO; and the MAX4926 has a 4.46V (typ) OVLO. When  $V_{IN}$  is greater than  $V_{OVLO}$ , GATE is high and FLAG is high.

### FLAG Output

The open-drain FLAG output is used to signal to the host system that there is a fault with the input voltage. FLAG goes high during an overvoltage or undervoltage fault. Connect a pullup resistor from FLAG to the logic I/O voltage of the host system.

## Device Operation

The MAX4923–MAX4926 have an on-board state machine to control device operation. A flowchart is shown in Figure 2. At initial power up, if  $V_{IN} < V_{UVLO}$  or if  $V_{IN} > V_{OVLO}$ , both GATE and FLAG are high. When  $V_{UVLO} < V_{IN} < V_{OVLO}$ , an internal timer starts counting and the device enters its on state after a 20ms delay. At any time if  $V_{IN}$  drops below  $V_{UVLO}$  or above  $V_{OVLO}$ , both GATE and FLAG transition high.

## Application Information

### MAX4926 Application

In a typical application for the MAX4926, an external adapter with built-in battery charger is connected to IN and a battery is connected to the drain of the external FET. When the adapter is unplugged, IN is directly connected to the battery through the external FET. Since the battery voltage is typically greater than  $V_{UVLO}$ , the GATE voltage stays low and the device remains powered by the battery.

### MOSFET Selection

The MAX4923–MAX4926 are designed for use with either a single pFET or dual pFETs in parallel. MOSFETs with  $R_{DS(ON)}$  specified for a  $V_{GS}$  of -4.5V are recommended. For input supplies near the UVLO maximum of 2.5V, use a MOSFET specified for a lower  $V_{GS}$  voltage. Also, the  $V_{DS}$  must be -30V and the  $V_{GS}$  (max) must be higher than the  $V_{OVLO}$  (max) for the MOSFET to withstand the full +28V input range of the MAX4923–MAX4926.

# Overvoltage Protectors with External pFET

**Table 1. MOSFETS Suggestions**

PART	CONFIGURATON/ PACKAGE	V <sub>DS</sub> MAX (V)	R <sub>ON</sub> MAX (mΩ) at V <sub>GS</sub> = -4.5V	MANUFACTURER
Si3993DV	Dual/TSOP-6	-30	245 each	Vishay Siliconix www.vishay.com
Si1433DH	Single/SOT-363	-30	260	
Si3983DV	Dual/TSOP-6	-20	110 each	
Si1413DH	Single/SOT-363	-20	115	
Si5933DC	Dual/1206-8	-20	110 each	
Si6991DQ	Dual/TSSOP-8	-30	68 each	

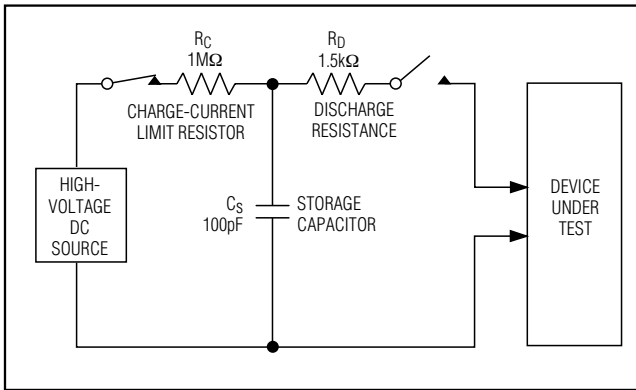


Figure 4. Human Body ESD Test Model

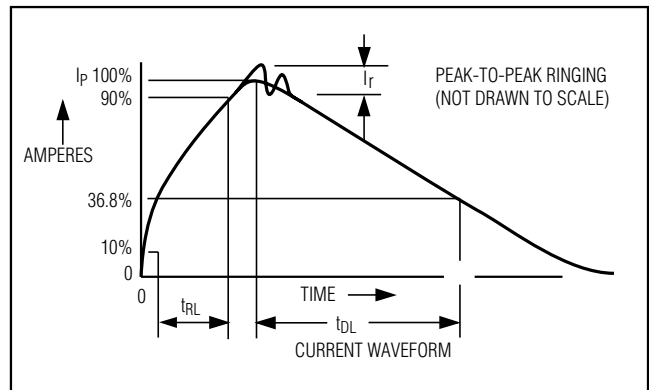


Figure 5. Human Body Model Current Waveform

### IN Bypass Consideration

For most applications, bypass IN to GND with a 1μF ceramic capacitor. If the power source has significant inductance due to long lead length, take care to prevent overshoots due to the LC tank circuit and provide protection if necessary to prevent exceeding the 30V absolute maximum rating on IN.

### ESD Test Conditions

The MAX4923-MAX4926 are ESD protected to ±15kV (typ) Human Body Model on IN when IN is bypassed to ground with a 1μF ceramic capacitor as close as possible to IN.

### Human Body Model

Figure 4 shows the Human Body Model and Figure 5 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kΩ resistor.

## Chip Information

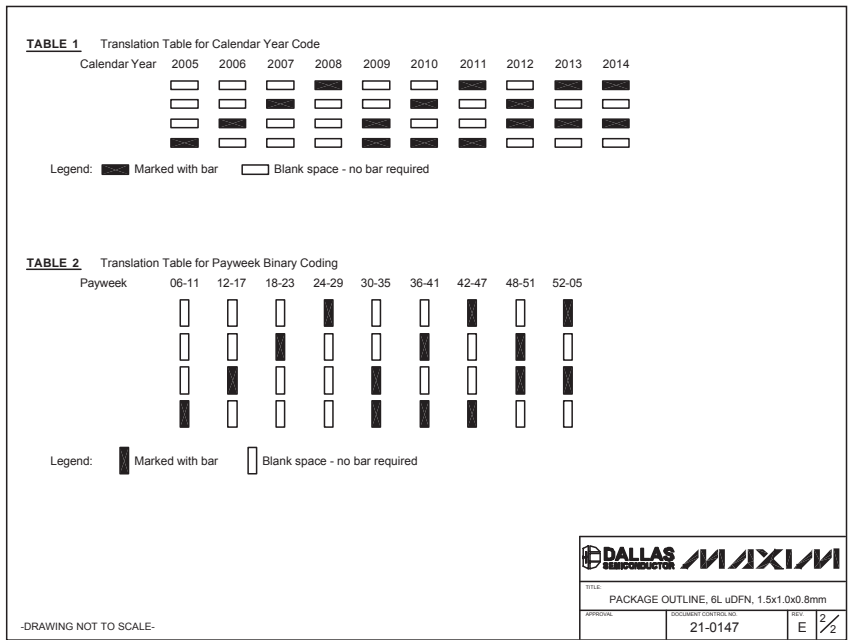
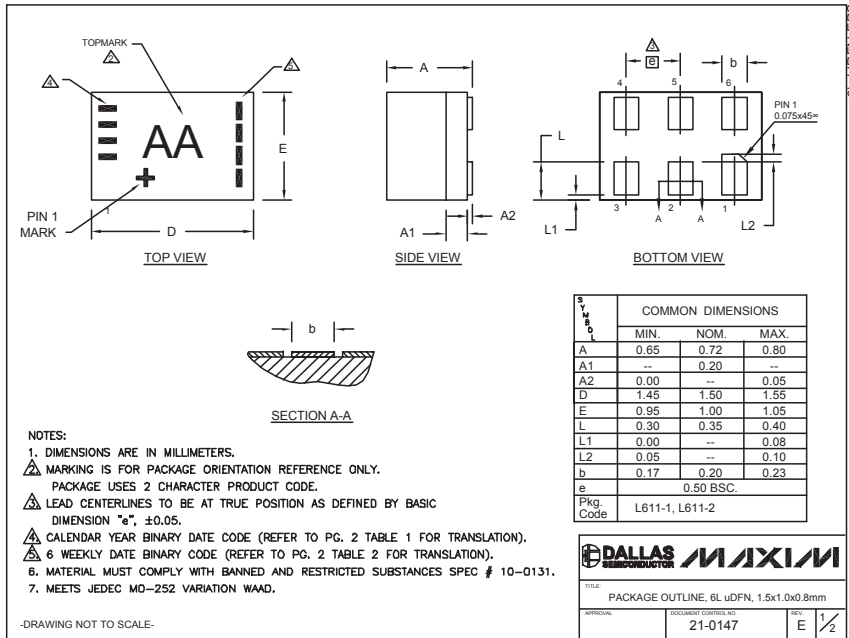
PROCESS: BiCMOS

# Overvoltage Protectors with External pFET

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

MAX4923-MAX4926



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